AN ABSTRACT OF THE DISSERTATION OF

Yao Liu for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on March 8, 2019.

Title: IC-Antenna Co-Integration for Efficient and Scalable Millimeter-Wave Antenna Interfaces

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Millimeter-wave (mm-wave) technology promises high speed, high system capacity and low latency interconnects with reduced cost. Applications like high data-rate wireless links, next generation automotive sensors and security body scanners highly depend on mm-wave technology innovations. As operating frequency moves to higher mm-wave bands, shrinking antenna dimensions enable co-integration of IC and antenna. Limited transistor output power at mm-wave requires multi-element arrays to satisfy communication and radar link budgets. This dissertation presents a wafer-scale compatible IC-antenna co-integration for efficient and scalable mm-wave antenna interfaces. The proposed IC-antenna co-integration approach is demonstrated through single antenna transmitters, a concurrent dual-polarization receiver front-end and polarization-duplex transmitter/receiver front-end.

Chapter 2 discusses the challenge of mm-wave IC-antenna interfaces with prior art including antenna-in-package (AiP) and on-chip antennas. The 60 GHz efficient, scalable and wafer-scale compatible IC-antenna co-integration approach is presented demonstrating wide bandwidth and large efficiency which are comparable to system-level AiP techniques at a lower cost and fabrication complexity.

Chapter 3 extends the proposed approach to a concurrent 60 GHz dual-polarization receiver front-end for short-range imaging/communication applications and polarization-diversity based MIMO links. Active cancellation between orthogonal polarizations is

adopted to achieve $\sim 30\,\mathrm{dB}$ cross-polarization leakage cancellation and concurrent dual-pol reception.

Chapter 4 presents a 60 GHz simultaneous transmit and receive front-end to achieve efficient polarization-duplex operation based on dual-polarization IC-antenna co-integration. Transmitter leakage is suppressed at receiver input and output by intrinsic antenna isolation and a feed-forward passive canceller. Total average self-interference cancellation $>40\,\mathrm{dB}$ is achieved for 1.07 GHz RF bandwidth at 60 GHz in the presence of a reflector.

IC-Antenna Co-Integration for Efficient and Scalable Millimeter-Wave Antenna Interfaces

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I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Yao Liu, Author

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Chapter 1: Introduction

The demand for high wireless network capacity and high-resolution imaging has led to tremendous interest in millimeter-wave (mm-wave) wireless systems in the last decade. Recent interest in mm-wave systems for next generation communication networks ("5G") is one example (Fig. 1.1) of efforts for large-scale mm-wave communication networks. Early commercial deployment of 5G is anticipated to begin in 2019. 5G promises data rates up to 20 Gb/s according to ITU IMT-2020 specification and the 5G NR (New Radio) will be submitted by 3rd Generation Partnership Project (3GPP) as the 5G communication standard proposal [16] where both sub-6GHz and mm-wave range are included as 5G NR frequency bands. In USA, spectrum at frequencies above 6GHz includes 27.5-28.35 GHz, 37-40 GHz and 64-71 GHz [17] bands. Several mm-wave techniques are used in 5G in order to achieve high data rate, reduced latency, cost reduction, higher system capacity and massive device connectivity. These techniques include massive MIMO, small cell and beamforming [16]. 5G technology also benefits Internet-of-Things (IoT) applications that rely on ultra-available, low latency links [18]. In future, mm-Wave links with small physical sizes (due to physically small antennas) can be combined with energy-harvesting techniques and/or RF-powering [19–23] for 5G IoT application that greatly improve the operating lifetime of miniature sensor nodes [24–28].

Fundamentally, the potential high data rates at mm-wave result from the large available bandwidth. For example, 60 GHz Wi-Fi, promoted by Wireless Gigabit Alliance (WiGig), adopts IEEE 802.11ad as its protocol. IEEE 802.11ad enables data rates up to 7 Gb/s, which is roughly comparable to 8-band 802.11ac data rates and over 11x faster than the highest 802.11n data rates [29]. The 60 GHz standard covers the 57 to 71 GHz frequency band and is subdivided into 6 different channels in IEEE 802.11ad, each of which occupies 2160 MHz bandwidth [30]. Integrated CMOS transceiver for 802.11ad has been demonstrated in [31]. With 802.11ay, 4 such channels can be combined to get a even wider bandwidth, 42.24Gb/s data-rate has been demonstrated with integrated CMOS transceiver [32, 33]. The higher data rates provided by mm-wave links are attractive in the context of emerging applications that impose high data demands. For example,

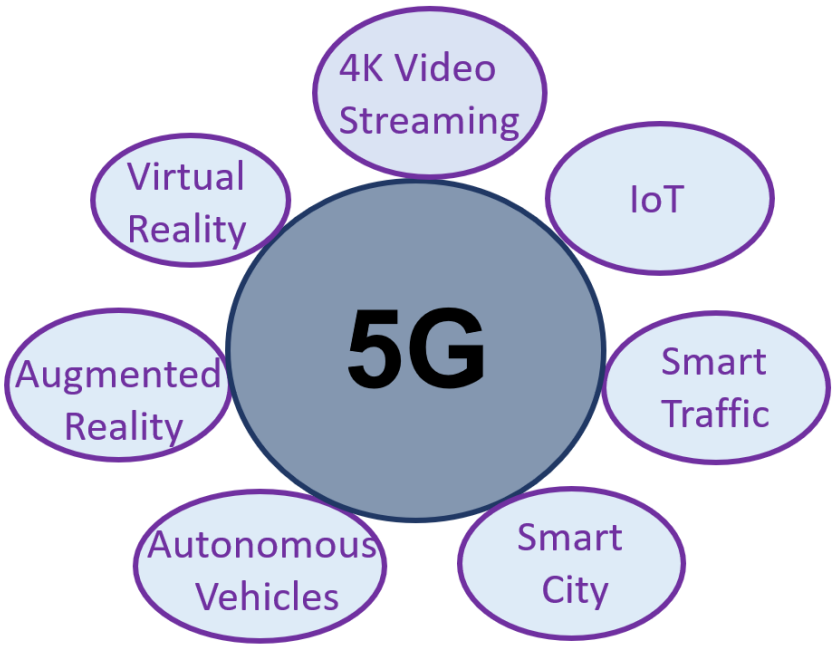


Figure 1.1: 5G vision: Smart city, IoT, autonomous cars etc. with high data rate and low latency [1].

video recording in 4K resolution is becoming standard in almost all cameras and smart phones. Consequently, wireless transfer of 4K video, which contains 4 to 5 times as many pixels as 1080p high-definition (HD) video, requires 8.9 Gb/s data rates [34, 35]. Similarly, today's high-end virtual reality headsets deliver HD videos to player's eyes through a cable which has to be connected to a gaming computer or console. However, this limits player's mobility and can cause entanglement and injury [36]. Eliminating wires, without decreasing video quality, is desirable to provide a truly immersive experience and requires 4 Gb/s data rates [37]. Given the spectrum crunch at frequencies below 6 GHz, mm-wave wireless links are required in order to enable such high data-rate applications.

In addition to communication links, mm-wave systems are also attractive for imaging resolutions due to the high-resolution capabilities associated with short wavelengths. This has led to demonstrations and deployment of radars operating between 76 to 81 GHz (with a corresponding electromagnetic wavelength of 3.7 mm to 3.9 mm) [38] for automotive radar applications with unprecedented accuracy in terms of tracking range, velocity and angle of objects [39]. Such radar technology is critical for advanced driver-assistance systems (ADAS), where the driver can be alerted about potential dangers(Fig. 1.2). Potential ADAS applications include lane-change assistance, blind-spot detection, parking assistance, cross-traffic warning, self-parking, lane-departure warning, adaptive cruise control, braking-assistance, collision avoidance etc. [40]. As ADAS systems evolve to future autonomous driving applications, mm-wave radar technology is considered one of the best options for accurate object detection and millisecond time-frame decision-making [41]. In addition to automative applications, mm-wave radar and imaging also has applications in industrial sensing and security. Currently, mm-wave scanners are used in airports to assess threats. The scanners operate between 70 GHz to 80 GHz [41] and detect hidden objects by providing an outline of the human's body [42].

The extensive commercial and imaging applications at mm-wave has led to interest in development of transceivers operating at these frequencies. In particular, integrating mm-wave transceivers in commercial process technologies can translate to low-cost systems that can be deployed in consumer devices. Techniques and research for low power and high speed communication [43–45], mm-wave channel modeling [46], MIMO array interfaces [47], signal generation [48] and frequency division [49,50] attract a lot of attention. This has also motivated extensive research and development of integrated mm-wave

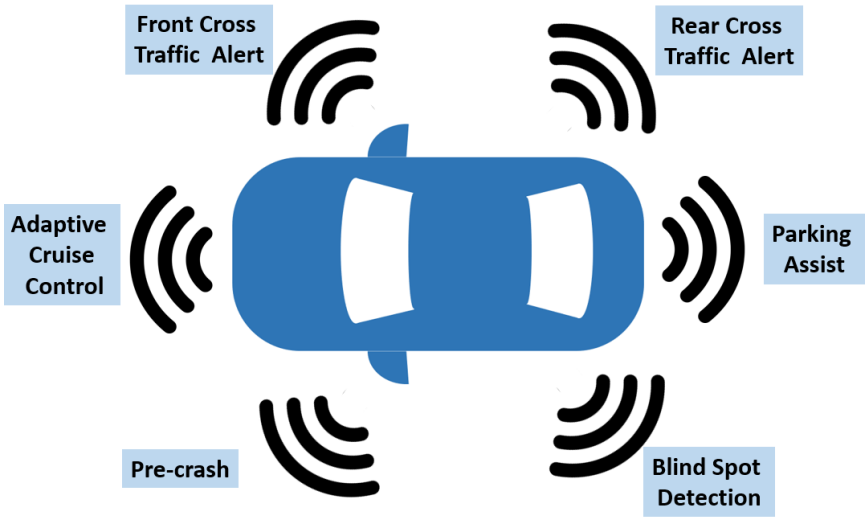


Figure 1.2: Typical automotive mm-wave radar applications and mounting locations [2].

CMOS and SiGe BiCMOS transmitters and receivers at frequencies from 28 GHz [51–53] to beyond 200 GHz [54–58] over the last decade. A key limitation with such integrated implementations is the limited output power of silicon transceivers (due to low breakdown voltages of devices) [59]. Multi-element transmitters have been proposed to leverage phased array beamforming to acheive higher effective isotropic radiated power (EIRP). Fig. 1.3 considers the power required per TX element as a function of number of array elements [3]. As shown in Fig. 1.3, array gain increases with increasing number of elements (10 log N), reducing per-element output power requirements. Considering 60 dBm targeted EIRP, minimum number of elements required can be determined based on device technology capabilities. Higher output power in GaN or GaAs leads to <100 elements. Given silicon output powers that are < 20 dBm, > 200 elements are required to satisfy EIRP targets. In recent years, scalable array architectures have been proposed to achieve such large arrays using repeated unit cell tiles [60–63]. Importantly, achieving such large arrays creates a complex antenna interface and package that lead to significant increase in cost and complexity.

One important characteristic of mm-wave systems is the small physical size of antennas at these frequencies (comparable to chip dimensions). For example, at 900MHz cellular frequency, the length of a half-wave dipole antenna is ∼16 cm (assuming dielec-

tric constant of 1) but this reduces to 2.5 mm at 60 GHz. Antenna size can be further reduced for higher dielectric constants, making antenna comparable to IC size. Shrinking antenna size also enables building large-number elements phased arrays on a single chip [42].

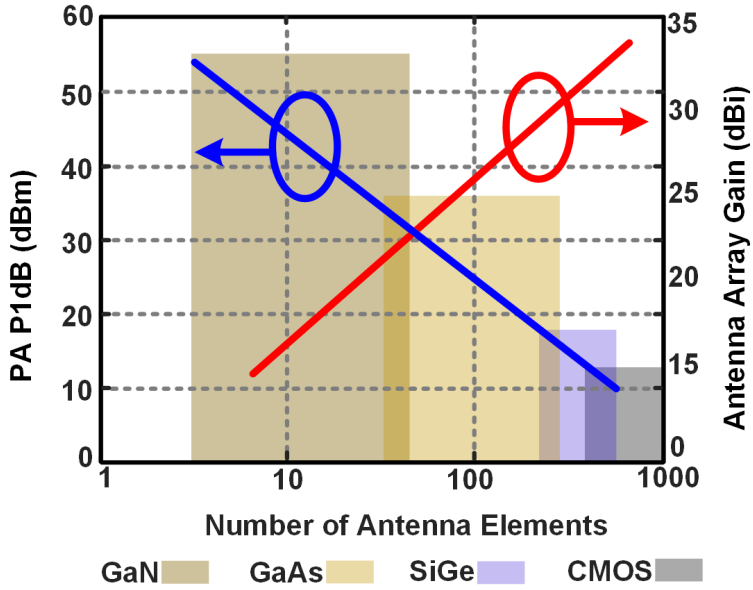


Figure 1.3: Antenna gain and output P1dB requirement for individual PA versus number of elements [3].

Small antenna physical size and necessity of phased array at mm-wave suggest that an efficient IC-antenna interface should be wafer-scale compatible, especially considering large number of mm-wave IO are required in an array. The ideal IC-antenna interface should also achieve good overall efficiency and large bandwidth while significantly simplifying packaging and testing complexity. Considering re-reconfigurability, it should also support dual-polarization capability for TX and RX. For integrated transceiver design, reconfigurability suggests polarization-duplexing based simultaneous TX and RX could be implemented using the IC-antenna interface which leads to higher data rate and spectral efficiency. In the following chapters, an efficient wafer-scale compatible IC-antenna interface is discussed. The IC-antenna interface approach relies on aperture coupling between on-chip feed/ground-plane slot and an antenna-on-substrate to simultaneously

achieve wide bandwidth and high efficiency. This approach ensures mm-wave multi-element arrays with high yields, good inter-element matching and re-reconfigurability for dual-polarization reception and polarization-based duplexing.

1.1 Organization

Chapter 2 introduces the challenge of mm-wave IC-antenna interface. Antenna-in-package (AiP) approach along with design tradeoffs is discussed. Following that, state-of-the-art in IC-Antenna co-integration is reviewed. Following this, an efficient IC-antenna co-integration approach which simultaneously achieves wide bandwidth and high efficiency is then presented. Design details of the aperture-coupled patch antenna and implementation in 0.18 μm SiGe BiCMOS technology at 60 GHz are detailed. Finally, measurements and performance are presented to demonstrate that efficiency and bandwidths of proposed approach is comparable to system-level performance with AiP techniques.

Chapter 3 extends the proposed IC-antenna co-integration approach to a 60 GHz concurrent dual-polarization receiver front-end in 0.18 μm SiGe CMOS for short-range imaging/communication applications and polarization-diversity based MIMO links [61]. The details of design and implementation of dual-polarization antenna are presented. Increasing the isolation between different polarizations requires active cancellation of the coupling between vertical and horizontal polarizations. The proposed active canceller provides $\sim$ 50 dB gain variation and full 360° phase variation. Finally, measured performance is presented demonstrating $\sim$ 30 dB cross-polarization leakage cancellation and concurrent dual-pol reception.

Chapter 4 presents a 60 GHz simultaneous transmit and receive front-end to achieve efficient polarization-duplex based on dual-polarization IC-antenna co-integration. The proposed antenna approach provides broadside radiation through the substrate and is compatible with low-res silicon substrates. The orthogonal-polarization feeds provide >40 dB simulated isolation between TX and RX around 60 GHz. Subsequent TX self-interference cancellation (SIC) at the LNA output is achieved with part of the TX signal coupled to a cancellation path which provides >20 dB gain variation and full 360° variable phase shift. Finally, measured performance shows total average SIC >40 dB is achieved for 1.07 GHz RF bandwidth at 60 GHz in the presence of a reflector.

Chapter 5 concludes the research with a summary and discussion of potential future work.

Chapter 2: Millimeter-Wave IC-Antenna Co-Integration for Integrated Transmitters and Receivers

2.1 Introduction

A wireless transceiver can be divided into four major functional blocks (Fig. 2.1): (a) the digital baseband performing digital signal processing, (b) the mixed-signal block responsible for signal amplification, filtering at low frequency and digital-to-analog or analog-to-digital conversion, (c) the radio frequency (RF) front-end providing signal modulation, filtering, amplification, transmission/reception at high frequency, and (d) the antenna serving as an interface between transmitter/receiver and the air medium. Historically, the digital baseband is implemented in complementary metal-oxide-semiconductor (CMOS) technology due to low static power consumption as well as reductions in dynamic power consumption due to technology scaling. The lower parasitics associated with nm-scale CMOS also result in lower power consumption for the mixed-signal blocks. On the other hand, compared to high electron mobility transistor (HEMT) or bipolar junction transistor (BJT), CMOS is inferior in terms of power gain at RF and mm-wave frequencies. In several applications, BJT and HEMT are preferred for RF building blocks. Multichip modules (MCMs) are popular choices to integrate these functional blocks on a package. As shown in Fig. 2.2, MCMs integrate different ICs horizontally [64]. If the system contains an antenna, the antenna is implemented on a separate low-loss printed circuit board (PCB) and its size is much larger than chip size if working at low RF frequency. For example, electromagnetic wavelength at 2.4 GHz is 12.5 cm. Even with substrate with high dielectric constants, antenna size for 2.4 GHz can still be of the order of several centimeters.

Figure 2.1: Typical wireless transceiver functional blocks.

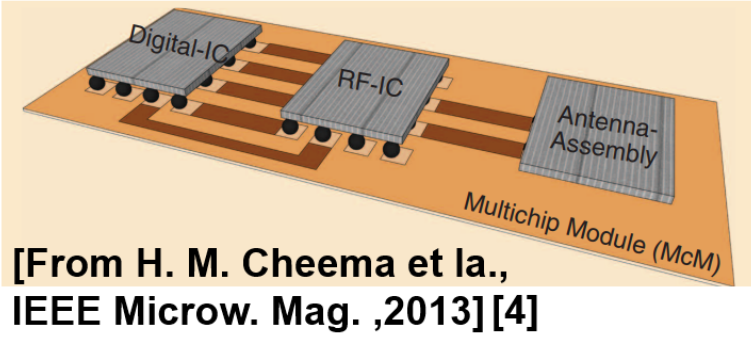


Figure 2.2: An MCM example [4].

With CMOS technology scaling, RF performance of CMOS transistors in nm-scale CMOS is sufficient for RF integration of several critical blocks. For example, 65 nm CMOS technology achieves 360 GHz/420 GHz f_t/f_{max} [65] which translates to reasonable power gain even at mm-wave frequencies. For example, the maximum power gain G_p from a device can be calculated as [66],

$$G_p = 10\log_{10}\left(\frac{f_{max}}{f}\right)^2 \tag{2.1}$$

which translates to 16.9 dB gain where f is working frequency (60 GHz) and f_{max} is 420 GHz. Therefore, CMOS transistors can potentially achieve sufficient performance in advanced technology nodes, making higher system-level integration of transmitters and receivers feasible. While design of commercial transmitters and receivers in CMOS/BiCMOS at RF is well-established commercially, millimeter-wave CMOS and BiCMOS ICs with high levels of integration have been demonstrated in the last decade [32,33,51–58,60–63, 67]. As shown in Fig. 2.3, a system-on-chip (SoC) with on-chip integration of mm-wave front-ends, eliminating lossy and area-inefficient interconnects and transitions from one IC to another.

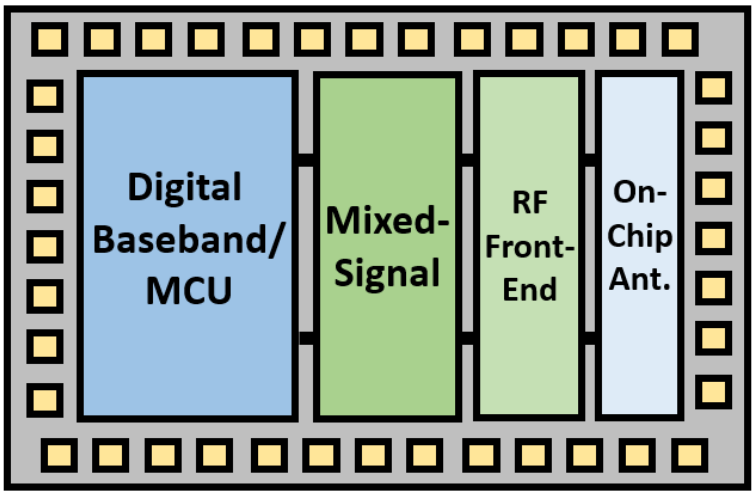


Figure 2.3: An SoC example.

From link budget perspective, as discussed in Chapter. 1, phased arrays are necessary at mm-wave. Integrated mm-wave transmitter and receiver arrays have been implemented in SiGe BiCMOS and CMOS, demonstrating the feasibility of low-cost multi-functional arrays for communication/imaging applications [61, 68, 69]. Silicon integration results in excellent yields and gain/phase matching for complex arrays. This has led to increasing interest in scalable, large-scale arrays with hundreds of elements built using multi-element unit-cells tiled in X and Y dimensions [61, 68]. While silicon ICs can achieve high yields, the mm-wave interface between the IC and the antenna is challenging for large number of mm-wave IO. As shown in Chapter. 1, at high mm-wave frequencies, for example 60 GHz, antenna size (∼1.5 mm @ 60 GHz with substrate) is comparable to chip size which suggests an efficient IC-antenna interface is possible.

2.2 Challenges for Antenna-in-Package mm-Wave Antennas

In order to achieve compact integration of the IC with antenna, one approach is antenna-in-package (AiP) where antenna is incorporated into the same package with the ICs. AiP approaches have to deal with package-level coupling and mismatches which may degrade antenna efficiency and bandwidth [5]. AiP approaches have been investigated for single-element and multi-element mm-wave ICs using low-temperature co-fired ceramics

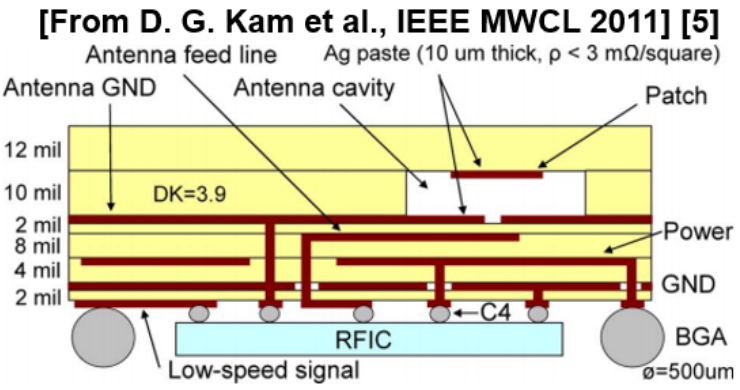


Figure 2.4: AiP implemented on LTCC [5].

(LTCC) and multi-layer organic laminates (MLO) [5, 6, 70].

An example of AiP implemented in LTCC is shown in Fig. 2.4 [5]. LTCC offers low-loss at mm-wave compared to conventional PCB and also provides high degree of integration [5]. In this work, an aperture-coupled patch antenna has been implemented inside the package where air cavity is used between patch antenna and ground plane to improve bandwidth and efficiency. Due to multi-layer routing, the power plane underneath antenna feed-line reflects backside radiation, improving front to back ratio [5].

AiP approach can provide higher gain and bandwidth comparing to direct on-chip antenna integration due to the ability to incorporate package level cavities and multi-layer design. AiP is also suitable for multi-element phased array applications. For example, [6] demonstrates a 64 element dual-polarization antenna embedded in a multilayer organic substrate package as shown in Fig. 2.5.

However, as the number of elements increases, the number of impedance-controlled lines being routed in a compact area on a package also increases. This could lead to significant element-to-element mismatches. For a phased array system, either amplitude or phase mismatch to/from antenna leads to degraded beam-forming performance and reduced gain. Also, AiP with large number of elements requires large number of impedance-controlled vias, which means significant routing losses and higher fabrication cost. For example, >1.5-dB interconnect loss in [6] reduces overall efficiency to 63% even if 90% antennas efficiency is assumed.

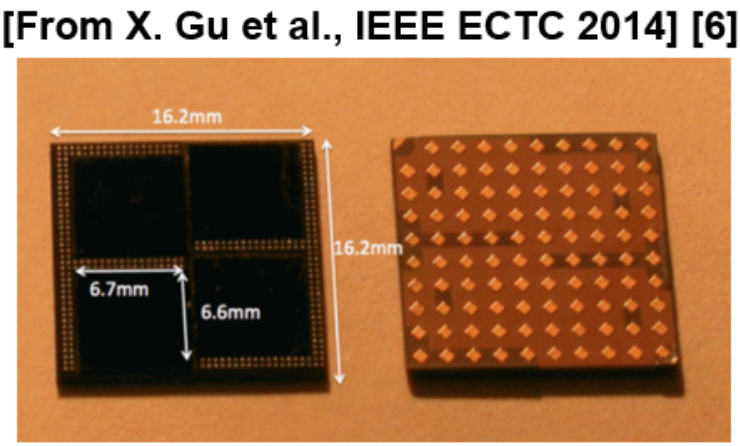


Figure 2.5: AiP with 64-element antenna arrays [6].

2.3 IC-Antenna Co-Integration State-of-the-Art

Another approach for IC-antenna interface is directly integrating antenna with the IC. Among them on-chip antenna has been investigated extensively. On-chip antennas are attractive for multi-element mm-wave arrays if comparable system performance can be achieved. However, silicon substrate has high dielectric constant ($\sim$ 11.7) and often low resistivity ($\sim$ 10Ω-cm), leading to low efficiency if EM energy is confined inside the substrate by the antenna. As discussed in [7] which is shown in Fig. 2.6, the ratio of the power radiated to the air mediumP_{air} to the total radiated power P_{total} (including power absorbed by substrate and power transmitted to air) can be expressed as

$$\frac{P_{air}}{P_{total}} = \frac{1}{\epsilon^{3/2}} \tag{2.2}$$

where ϵ is substrate dielectric constant. Since silicon substrate has a large ϵ ($\sim$11.7), most energy is confined inside the silicon substrate instead of radiating out into air which leads to a low radiation efficiency. Another approach is utilizing on-chip ground plane to isolate silicon substrate from the antenna so that most energy won't be trapped inside silicon as shown in Fig. 2.7 [7]. In most modern process technologies, the distance

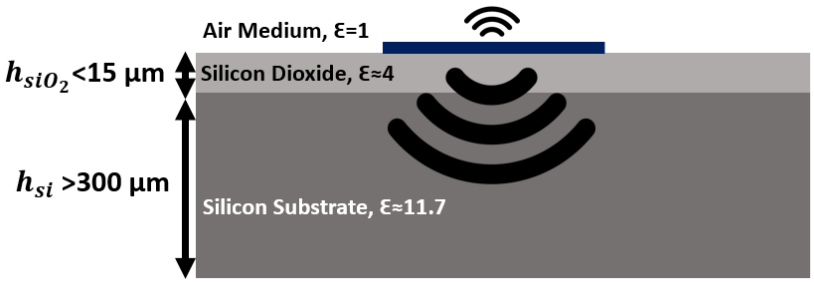


Figure 2.6: On-chip antenna radiating from top side of IC [7].

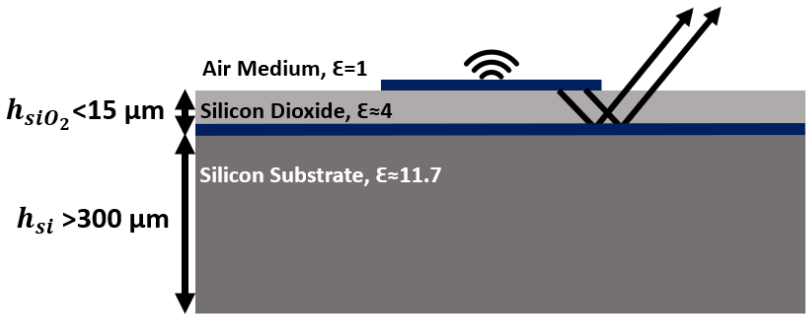


Figure 2.7: On-chip antenna radiating from top side of IC adding on-chip ground shielding [7].

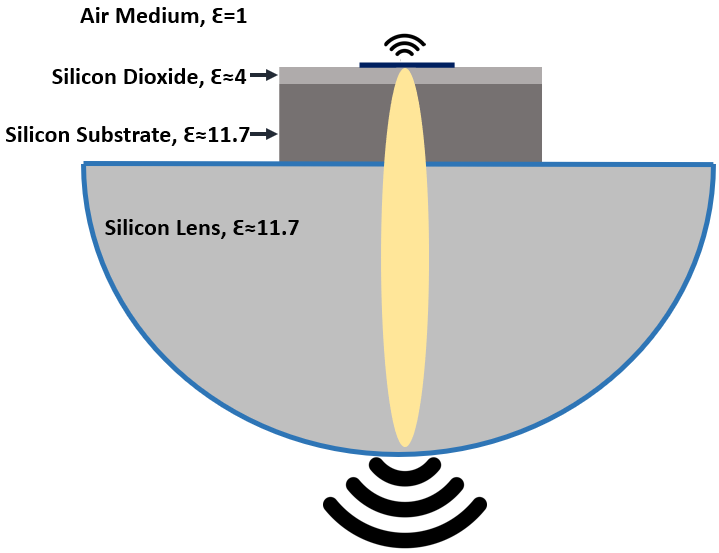


Figure 2.8: On-chip antenna radiation from bottom side of IC with a hemispherical silicon lens [7].

between on-chip top metal layer (which is also antenna metalization layer) and on-chip bottom metal layer (which is also on-chip ground shielding layer) is usually below 15 μm [7]. The small antenna-ground spacing leads to strong image current which partially cancels the antenna radiation field. This means that with on-chip ground, the antenna cannot achieve high efficiency and large bandwidths. A hemispherical silicon lens has been used to demonstrate improved radiation efficiency by reducing the energy absorbed by the silicon as substrate waves. A quarter wavelength matching layer using the lens can convert the substrate wave into radiating power as shown in Fig. 2.8 [7].

Even though radiation efficiency and gain can be improved by using backside silicon lens, the large size and potential mechanical instability limits its application. Another approach to enhance on-chip-antenna efficiency is to add a superstrate on top of the antenna as shown in Fig. 2.9 [8] or to proximity couple to an antenna on a superstrate as shown in Fig. 2.10 [9].

While antenna performance can be improved by using superstrate on top of IC, these approaches also present large-scale packaging challenges since all other IO must also be accessed through wirebond and flip-chip pads on the front side of the IC. While

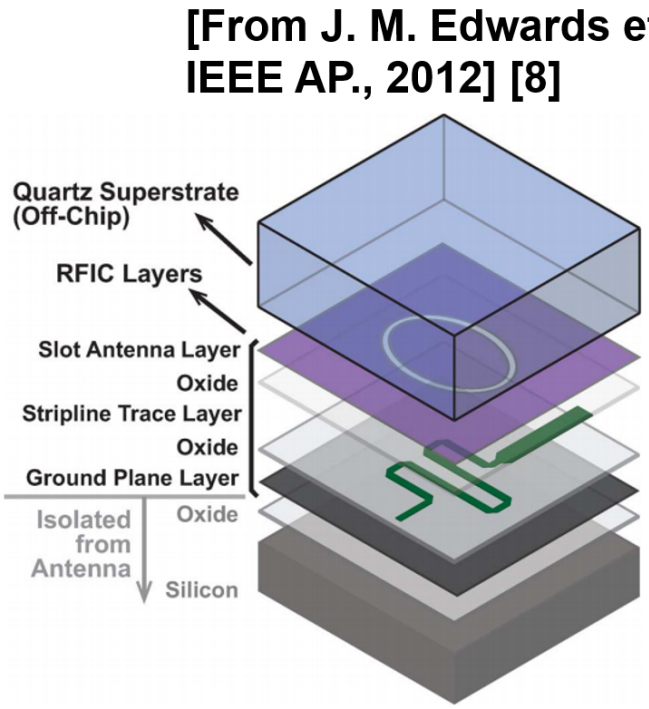


Figure 2.9: On-chip elliptical slot antenna with quartz superstrate on top [8].

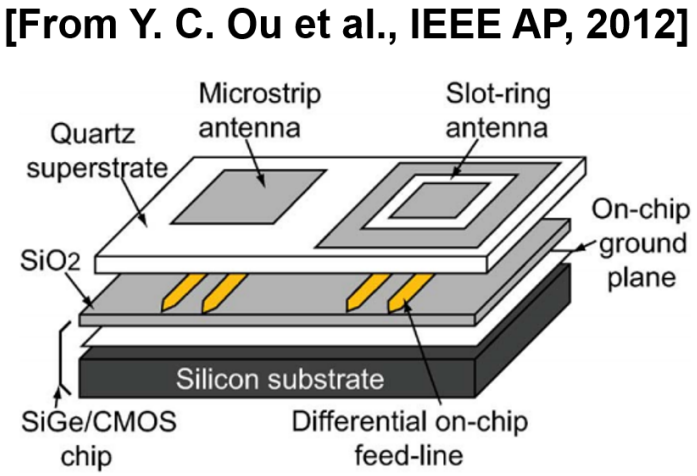


Figure 2.10: Differential microstrip and slot-ring antennas with quartz superstrate underneath [9].

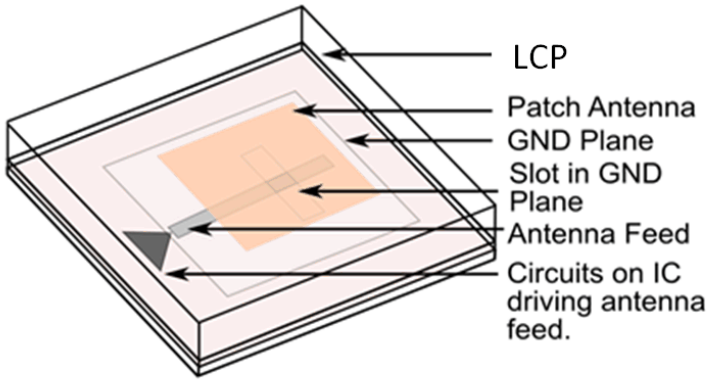


Figure 2.11: Proposed antenna-cointegration scheme 3D view with on-chip feed and slot aperture-coupled to antenna on LCP substrate bonded to backside of die.

a wafer-scale approach has been proposed with custom lithography in [71], performance is affected if IO and supply/ground routing is restricted to the periphery as opposed to internal supply and IO pads, similar to [6].

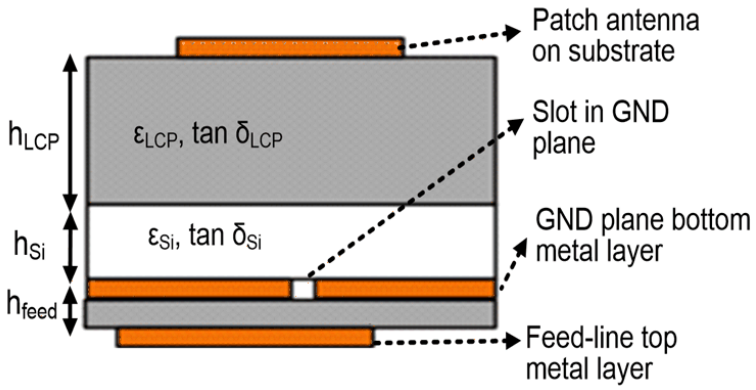


Figure 2.12: Proposed antenna-cointegration scheme cross-section.

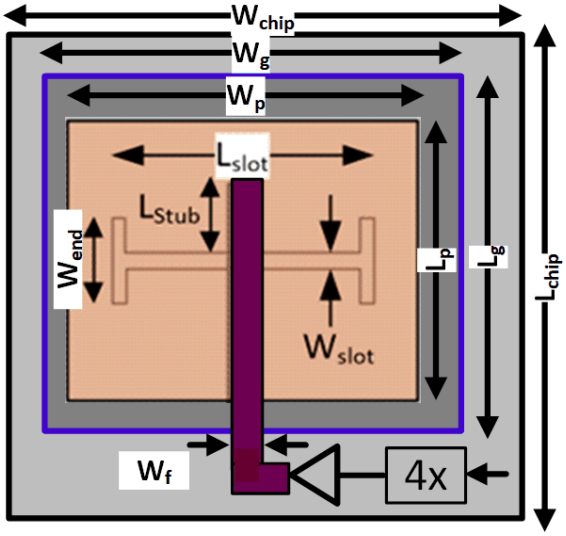


Figure 2.13: Proposed antenna-cointegration scheme top view.

2.4 Aperture-Coupled Antenna Co-Integration Approach

In this work [72], we propose a wafer-scale compatible IC-antenna co-integration approach that significantly simplifies mm-wave packaging and test by eliminating mm-wave I/O to/from the IC while potentially achieving ∼50% efficiency and ∼15% bandwidth simultaneously (Fig. 2.11). This performance is competitive with overall efficiencies achieved with state-of-the-art MLO and LTCC packaging.

The traditional aperture-coupled patch antenna can be found in [73]. Fig. 2.11 shows the 3D view of the proposed wafer-scale compatible antenna-cointegration scheme that relies on aperture-coupling between the on-chip feed and the patch antenna on a substrate that is bonded to a thinned silicon IC. The proposed approach is demonstrated with a 60 GHz prototype which has been implemented in TowerJazz 0.18 μm SiGe BiCMOS. As shown in Fig. 2.12, the thick top-metal layer (which in this technology process is metal 6) on the IC is used for antenna feed and accompanying ground plane is created using the lower metal layers (which are metal 1 through metal 3 in this technology process). Backend metalization photo-lithography allows the creation of a precise slot (on the order of nanometer) in the ground-plane that aperture-couples the feed to a patch antenna on the substrate without the need for any off-chip vias that conduct mm-wave

signal as shown in Fig. 2.13. The silicon die (or wafer) with circuits is thinned to reduce loss as is described in details in section 2.6. The patch antenna metalization is created on the off-chip substrate, and the die (or wafer) and substrate can be bonded together using well-established non-conductive adhesive techniques. From an antenna performance perspective, this technique preserves all the benefits of aperture coupling - wide bandwidth as well as isolation between the antenna layer and feed line layer due to the ground plane shielding, which allows for transmission-line structures to be created without interfering with antenna performance. Due to the flexibility of the proposed approach, bandwidth enhancement techniques such as stacked aperture-coupled patches [74] are also potentially feasible. While the slot and ground-plane occupy large IC area, this is common to other antenna-on-chip approaches [8, 9]. The proposed backside-radiation scheme is relatively insensitive to metal-fill rules, compatible with wirebonding/flip-chip packaging, and is well-suited for CMOS or SiGe wafer-scale post-processing since only wafer-thinning is required.

2.5 Antenna Design Methodology

As shown in Fig. 2.13, design variables include patch and slot dimensions (L_p, W_p, W_{slot}, L_{slot}, and W_{end}), on-chip ground plane size (W_g and L_g), feed structure parameters (L_{stub}) and substrate parameters (ϵ_{LCP}, h_{LCP} and h_{si}).

For a rectangular microstrip patch antenna, patch dimensions (L_p, W_p) are the most important parameters. Patch length L_p determines resonant frequency f_r from a zeroth-order approximation. The relation between resonant frequency f_r and L_p is given by

$$f_r = \frac{c}{2\left(L + 2\Delta L\right)\sqrt{\epsilon_{re}}} \tag{2.3}$$

Where ϵ_{re} is the effective dielectric constant of the microstrip patch, ΔL is the extended length due to the fringing fields on two open ends [75]. Patch width W_p mainly impacts the input resistance R_{in} and bandwidth. From a zeroth-order approximation, as W_p increases, R_{in} decreases, bandwidth increases, and radiation efficiency increases. The ratio of $\frac{W_p}{L_p}$ is between one and two in order to get good bandwidth and efficiency without degrading cross-polarization and generating undesired modes [76, 77].

In order to keep wide bandwidth and high efficiency, choosing a proper antenna

substrate is critical. A good candidate for the antenna substrate should have a small value of dielectric constant ϵ_r, large thickness h, and small loss tangent $tan\delta$. A small value of ϵ_r leads to a larger fringing field at the open ends of a patch, leading to higher radiated power, larger bandwidth and higher radiation efficiency. Increasing h has a similar effect as lowering the dielectric constant. However, a very thick substrate also leads to a degradation of radiation efficiency because of increased surface-wave loss P_{sur}. The radiation efficiency e_r of a patch antenna is defined as the ratio of the radiated power P_r to the input power P_i as (2.4)

$$e_r = \frac{P_r}{P_i} \tag{2.4}$$

The input power distributes in the form of radiated power P_r, conductor loss P_c, dielectric loss P_d and surface wave loss P_{sur}. Therefore, (2.4) can be written as (2.5).

$$e_r = \frac{P_r}{P_r + P_c + P_d + P_{sur}} \tag{2.5}$$

The coupling level between the microstrip feed line and patch antenna as well as the front to back ratio is primarily determined by the length of the slot/aperture L_{slot} [78]. In order to increase the coupling level, a large L_{slot} is desirable. However, this also leads to a degraded front to back ratio, cross polarization level and more spurious radiation. To solve this problem, a dog-bone shape slot is used to boost coupling between feed-line and patch, while also ensuring high front-to-back ratio and low spurious radiation level [79].

In order to understand the physical mechanism of aperture coupling and to build intuition on antenna design methodology, an equivalent model assuming a homogeneous air dielectric based on transmission line models has been built, as shown in Fig. 2.14. Patch antenna is essentially a transmission line with both ends open. The two open-ends can be represented by radiating slots on both ends to model antenna radiation, where, the radiated power of the two slots is represented by conductance G_P. The power dissipated in G_P is same as that radiated by the two slots. G_P is calculated by [80]

$$G_P = \frac{1}{\pi}\sqrt{\frac{\varepsilon}{\mu}}\int_0^{\pi} \frac{sin^2(\frac{\pi W_p}{\lambda_0}cos\theta)}{cos^2\theta} sin^3\theta d\theta \tag{2.6}$$

Capacitors are used to model the length extension due to fringing fields on both ends.

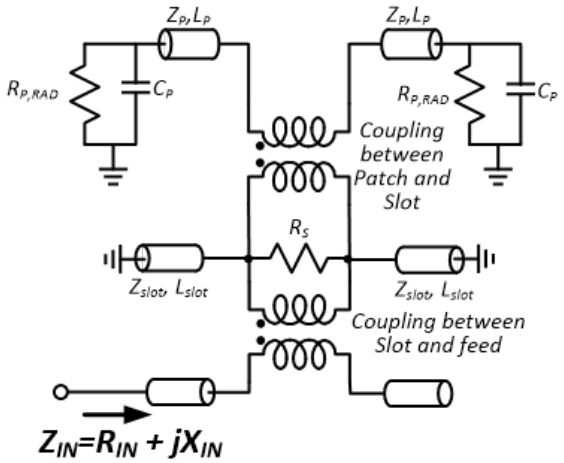


Figure 2.14: Equivalent circuit model for aperture coupled patch antenna.

The equivalent end capacitance is

$$C_P = \frac{\Delta L}{v Z_0} \tag{2.7}$$

Where v is phase velocity, Z_0 is characteristic impedance and ΔL is length extension which can be calculated by [80]

$$\Delta L = 0.412h \frac{\epsilon_e + 0.3}{\epsilon_e - 0.258} \frac{W_p/h + 0.262}{W_p/h + 0.813} \tag{2.8}$$

where h is substrate thickness. G_P and C_P are impedance-transferred to the center of the patch where the coupling aperture is located. The summation of the impedance from both sides provides total patch admittance. The coupling mechanism between patch and aperture and that between microstrip feed-line and aperture are modeled using two transformers with turns ratio n_1 and n_2 respectively as computed in [81]. Aperture in the ground plane is represented by conductance and susceptance which stand for energy radiated and energy stored in the aperture respectively. The conductance can be calculated using (2.6). Susceptance can be computed by combining admittance of two grounded slot lines with certain characteristic impedance and propagation constant [82]. Note that conventionally aperture in the ground plane is only modeled as susceptance for energy storage, however, in our case, to broaden the bandwidth, aperture is also

radiating, which is taken into account by a real conductance.

In order to get the impedance at the feed-line input, the patch admittance is first transformed by the top transformer and added with the slot admittance. The summation is then transformed by the bottom transformer. After combining the effect of open transmission line on the bottom and taking the transmission line length into account, the input impedance can be computed. Fig.2.15 shows the comparison of input impedance from the equivalent model and EM simulation using ANSYS High Frequency Structure Simulator (HFSS) [83].

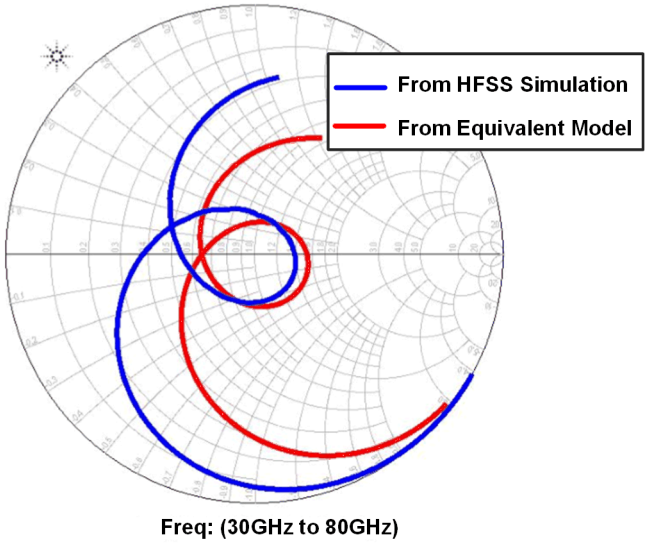


Figure 2.15: Equivalent circuit model and EM simulation comparison for aperture-coupled patch antenna input impedance.

The equivalent model is used for predicting the input impedance seen from feed-line. Wide bandwidth can be achieved by adjusting components' values inside the model and then deriving physical geometries.

Another important consideration during the process of antenna design is the size of the ground plane (W_g and L_g). In order to save die area, ground plane can not be too large. Simulated antenna ground plane impact on S11 and efficiency are shown in Fig. 2.16 and Fig. 2.17. Simulations show that when ground plane size is increased from 1.2 mm$\times$1.2 mm to 2 mm $\times$ 2 mm, f_0 varies from 60.6 GHz to 63.1 GHz, and efficiency

increases from 44% to 51%. Ground plane impact can also be viewed in the context of typical micro-strip antennas as predicted in [84] - in this work, the ground plane is limited to 1.6 mm $\times$ 1.6 mm to limit die size.

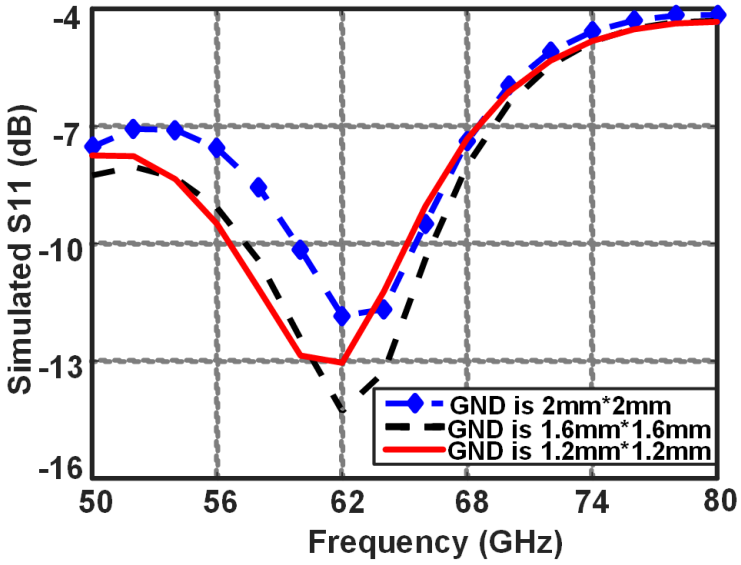


Figure 2.16: Antenna S11 variation with different ground plane size.

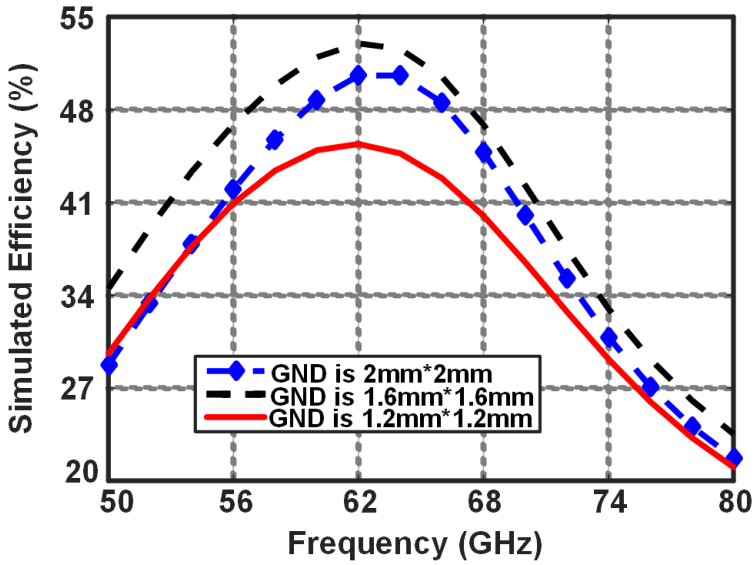


Figure 2.17: Antenna efficiency variation with different ground plane size.

2.6 Antenna Implementation in 0.18 μm SiGe BiCMOS

Since wafer-scale compatibility is targeted, the patch substrate material must have low dielectric constant, low loss at mm-wave and silicon-compatible coefficient of thermal expansion. Silicon substrate is usually $500 - 600\mu m$ thick which introduces significant surface wave loss P_{sur}. To alleviate the disadvantages of the lossy silicon substrate, we thin it to about $75\mu m$ to reduce the loss. On the back of silicon substrate, liquid crystal polymer (LCP) has been identified as a potential low-cost, high performance, mm-wave substrate [85] and is selected in this work. Notably, similar performance is also achieved in simulation with quartz as the substrate. LCP has a low dielectric constant ($\epsilon_{LCP} \sim 3.1$) and low loss at mm-wave ($\tan\delta_{LCP} \sim 0.003$) which is comparable to LTCC. While increasing LCP substrate thickness can initially lead to higher radiation efficiency and bandwidth, a very thick substrate leads to lower efficiency due to surface-wave loss. The impact of silicon and LCP thickness on antenna performance is discussed below. The effect of silicon thickness on antenna efficiency is shown in Fig. 2.18. Reducing silicon thickness improves efficiency, for example, changing thickness from 150 μm to 50 μm

improves efficiency from 38% to >50%. From S11 perspective, changing silicon thickness also moves antenna resonant frequency as shown in Fig. 2.19, where changing thickness from 150 μm to 50 μm moves resonant frequency from 56 GHz to 65 Ghz, a significant shift for antenna working frequency. Silicon thickness has to be reduced and antenna redesigned to ensure desired resonant frequency and improve antenna efficiency. While thinning silicon dies can lead to reliability challenges, 3D IC integration has motivated research into die thinning and bonding techniques for robust packaging.

The impact of LCP thickness on antenna efficiency is shown in Fig. 2.20. Increasing LCP thickness improves efficiency. In the simulation, increasing LCP thickness from 75 μm to 150 μm improves efficiency from 45% to 60%. The LCP thickness doesn't shift antenna resonant frequency as shown in Fig. 2.21. However, increasing LCP thickness does improve antenna bandwidth. For example, increasing LCP thickness from 75 μm to 150 μm improves bandwidth from 3 GHz to 10 GHz.

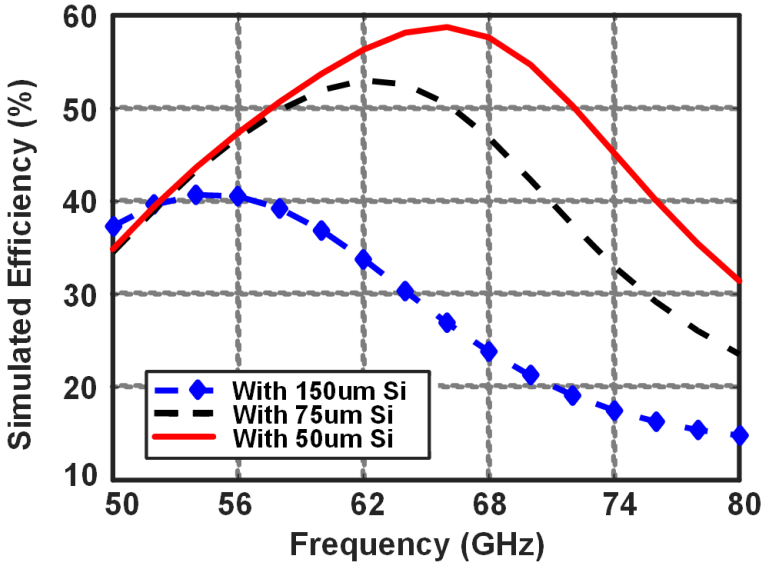


Figure 2.18: Antenna efficiency variation with different silicon substrate thickness.

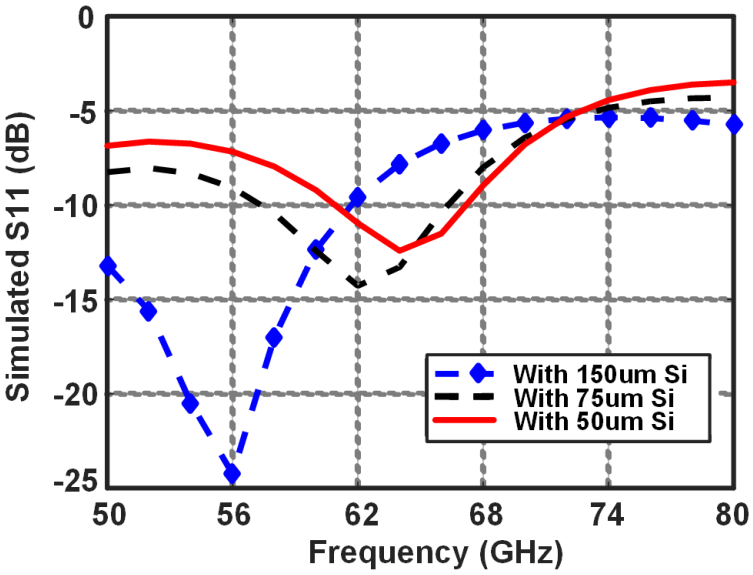


Figure 2.19: Antenna S11 variation with different silicon substrate thickness.

In the prototype, silicon thickness of $\sim$75 μm is selected to balance efficiency with ease of chip handling for packaging. Readily-available LCP material with 100 um thickness (Rogers 3850) is used, leading to 52% efficiency and 9-GHz bandwidth in simulation.

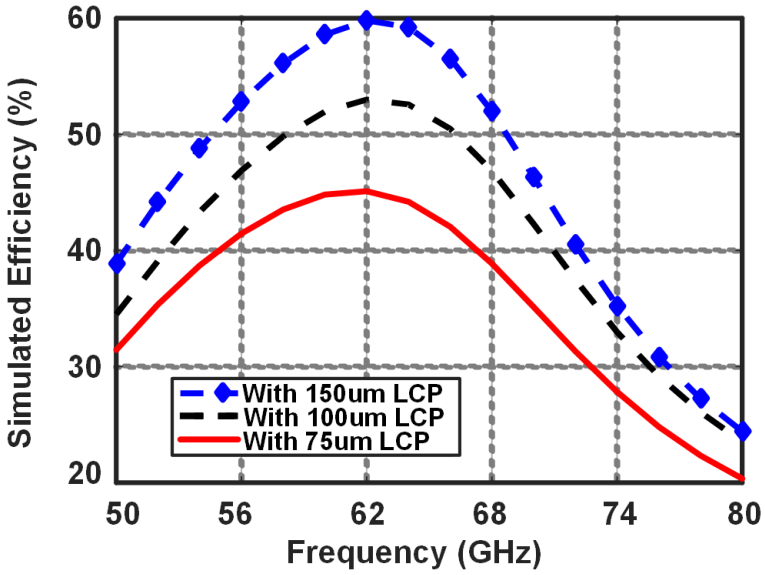


Figure 2.20: Antenna efficiency variation with different LCP substrate thickness.

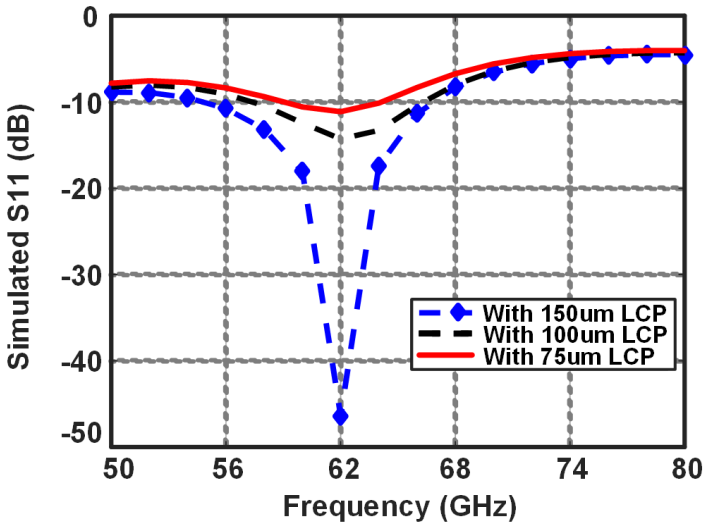


Figure 2.21: Antenna S11 variation with different LCP substrate thickness.

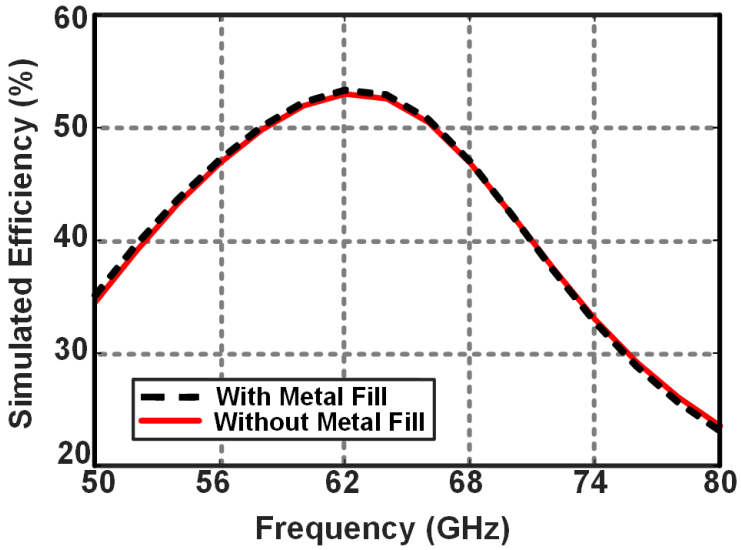


Figure 2.22: Metal fill effect on antenna efficiency.

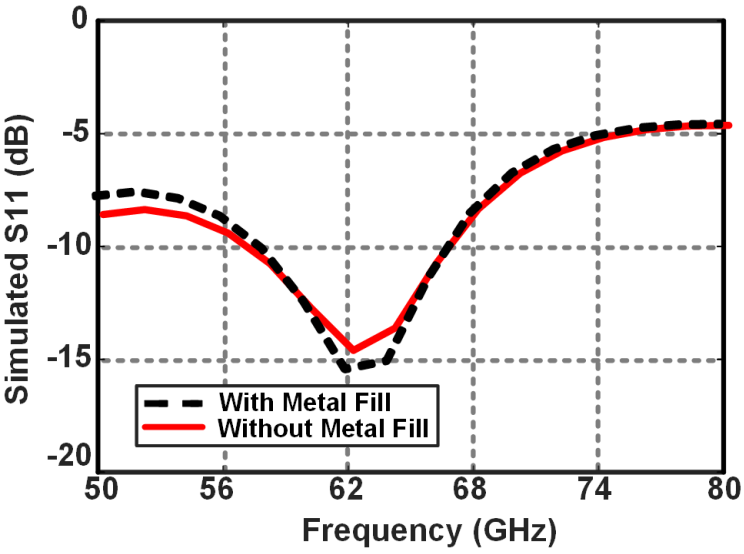


Figure 2.23: Metal fill effect on antenna S11.

Floating metal-fill structures are placed in each metalization layer to satisfy metal

Table 2.1: IC-antenna co-integration design parameters.

Parameter	Value	Parameter	Value
W_p	1.25 mm	L_g	1.6 mm
L_p	0.95 mm	h_{LCP}	100 μm
W_{slot}	60 μm	ϵ_{LCP}	3.14
L_{slot}	650 μm	$\tan\delta_{LCP}$	0.0025
W_{end}	365 μm	ϵ_{si}	11.7
L_{stub}	375 μm	$\tan\delta_{si}$	0.015
W_g	1.6 mm	h_{si}	75 μm

density rules to ensure performance/yield of interconnect in silicon, particularly in advanced process technologies. Such rules can require density >10% and can impact antenna performance. For example, metal-fill reduces efficiency in [8] from 40% to 29%. The proposed approach is relatively insensitive to metal fill since the ground plane in the lowest three metal layers shields the antenna from the higher metal layers. Simulations with floating metal structures have negligible impact on performance. Fig. 2.22 shows antenna efficiency variation with and without metal fills. Simulation shows negligible change in radiation efficiency. Similarly, metal fill impact on antenna input matching S11 is show in Fig. 2.23. No significant change of S11 due to metal fill is observed in simulation. Insensitive to metal fills demonstrates the advantages of this approach for IC-antenna co-integration.

Density rules also require slots in the ground plane, a continuous ground plane is achieved by stitching together the lowest three metal layers using lower level vias. Table. 2.1 shows all design parameters. As shown in Fig. 2.18 and Fig. 2.19, the structure achieves 52% simulated efficiency (including antenna feed, with 2.8-μm top-metal thickness and loss of 10.5 $m\Omega$/sq) and > 9-GHz bandwidth at 60 GHz.

2.7 Measured Performance

The proposed antenna and IC co-integration is implemented in 0.18 μm TowerJazz SiGe technology. Fig. 2.24 shows the IC layout which includes 60 GHz antenna feed and

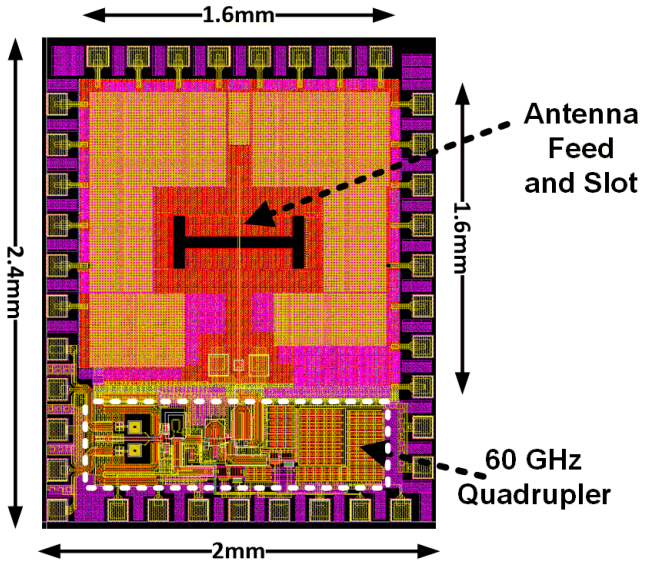


Figure 2.24: Layout of 60-GHz IC-antenna co-integration with on-chip feed/slot and active circuits (quadrupler and power amplifier).

slot structures. Antenna testing is simplified by integrating a 60 GHz quadrupler and power amplifier (PA) along with the antenna. The quadrupler requires a 15 GHz input signal. The technology has a 2.8 μm thick top metal layer and 0.52 μm bottom layers. Test pads are included in the structure to measure the quadrupler/PA output power, and hence, the input power to the antenna feed (Fig. 2.25). In this measurement, the antenna-feed is disconnected using ion-beam trimming and test pads are accessed in a probe-based setup as shown in Fig. 2.26 and Fig. 2.27. To verify the quadrupler input matching design, the probe-based measurement setup as shown in Fig. 2.28 is used. The quadrupler input match across frequency is shown in Fig. 2.29. As shown in Fig. 2.31, the DC bias and input power settings are varied to achieve ∼-10 dBm at quadrupler/PA output across the 60 GHz band in the probe-based setup shown in Fig. 2.30.

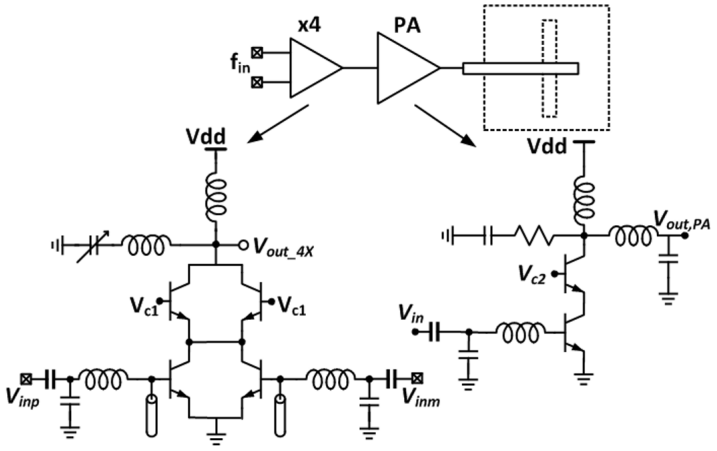


Figure 2.25: 60 GHz quadrupler and power amplifier to simplify mm-wave testing.

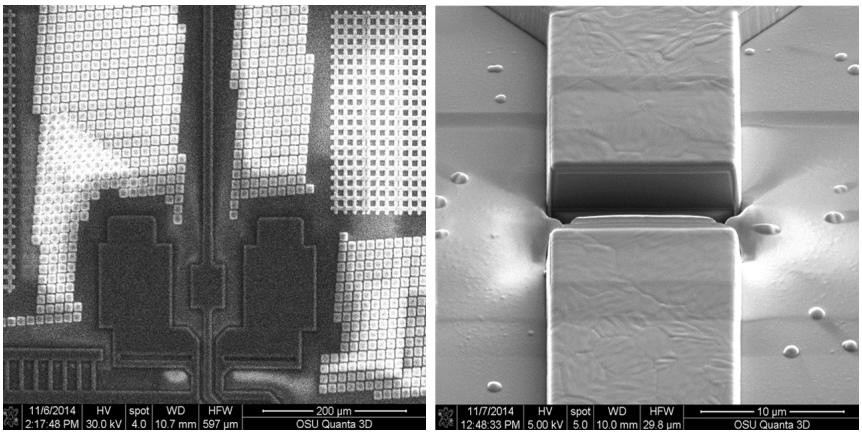


Figure 2.26: Micro-photo of focused-ion beam used for antenna feed line trimming.

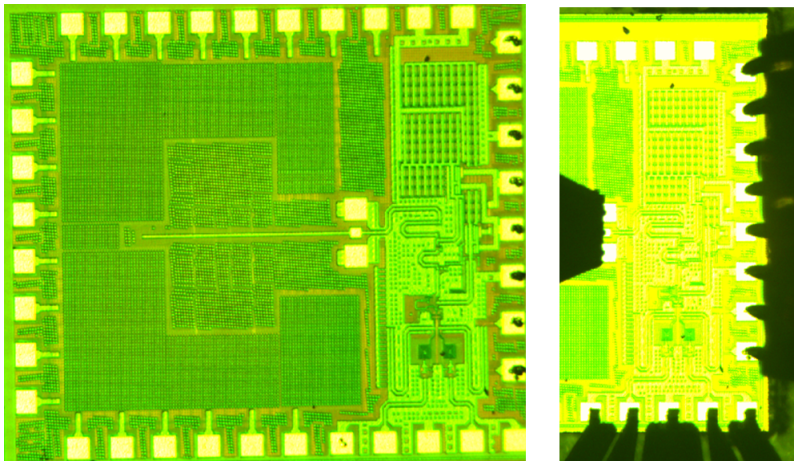


Figure 2.27: Die photo of 60 GHz IC-antnena co-integration where probe measurement is supported by test pads.

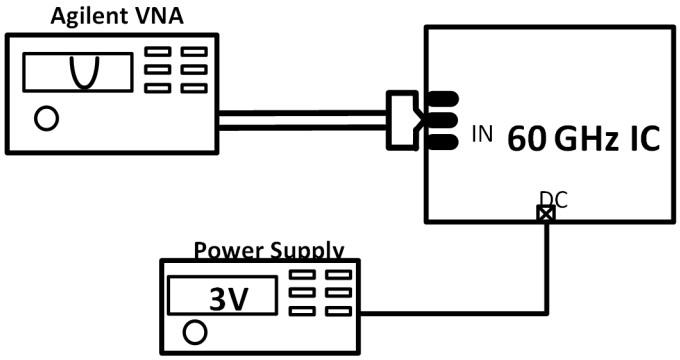


Figure 2.28: Probe-based test setup to measure quadrupler input matching S11.

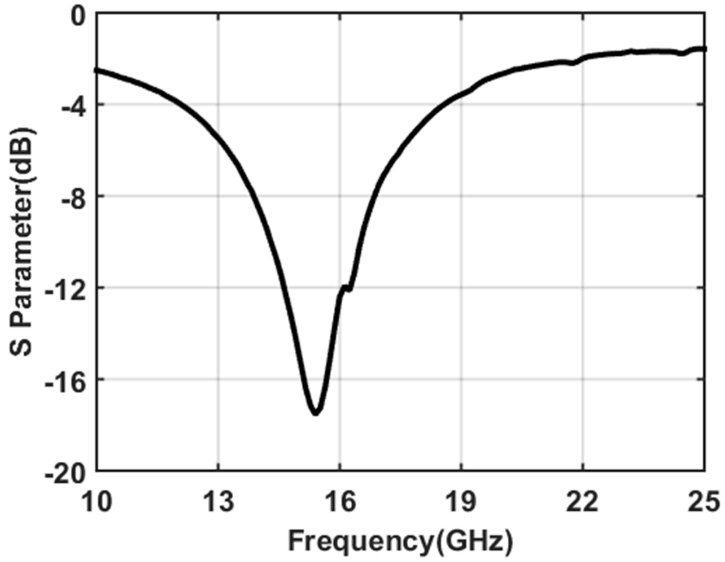


Figure 2.29: Measured 60 GHz quadrupler input matching S11.

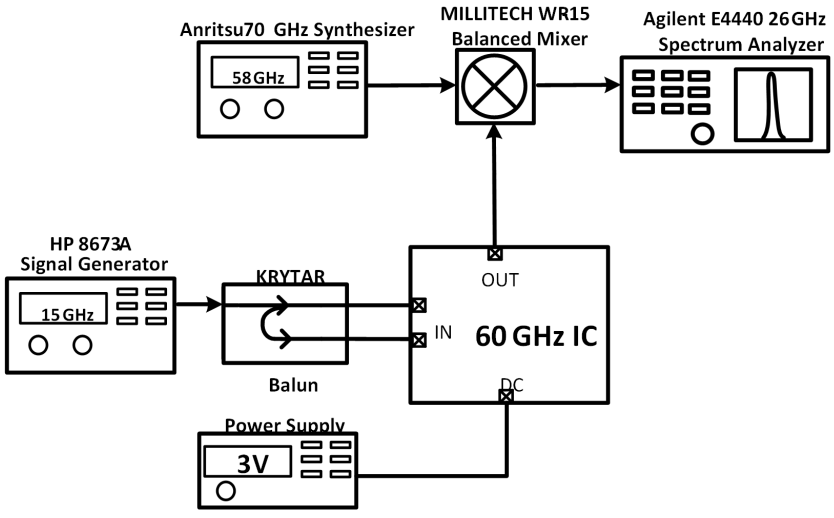


Figure 2.30: Probe-based test setup to measure quadrupler/PA output power.

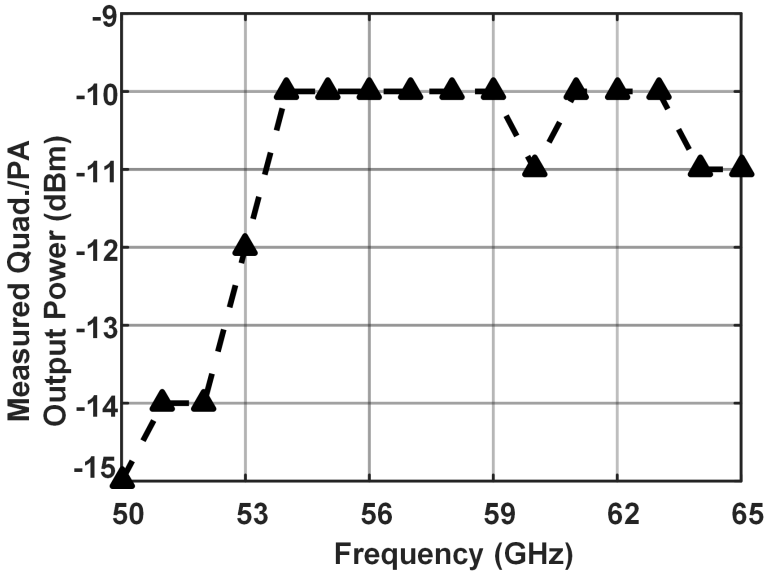


Figure 2.31: Measured 60 GHz quadrupler/PA output power.

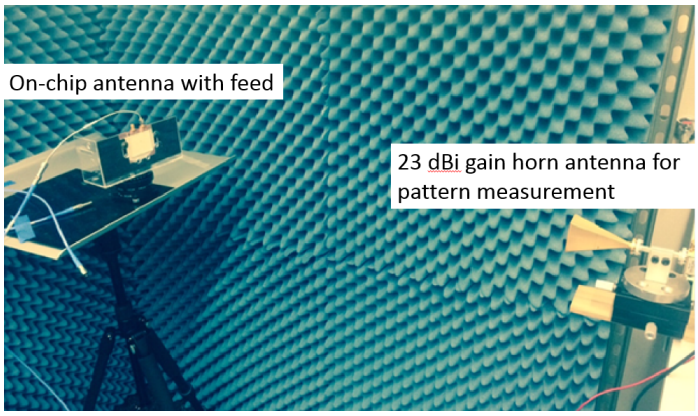


Figure 2.32: Measurement setup to characterize 60-GHz antenna pattern and gain.

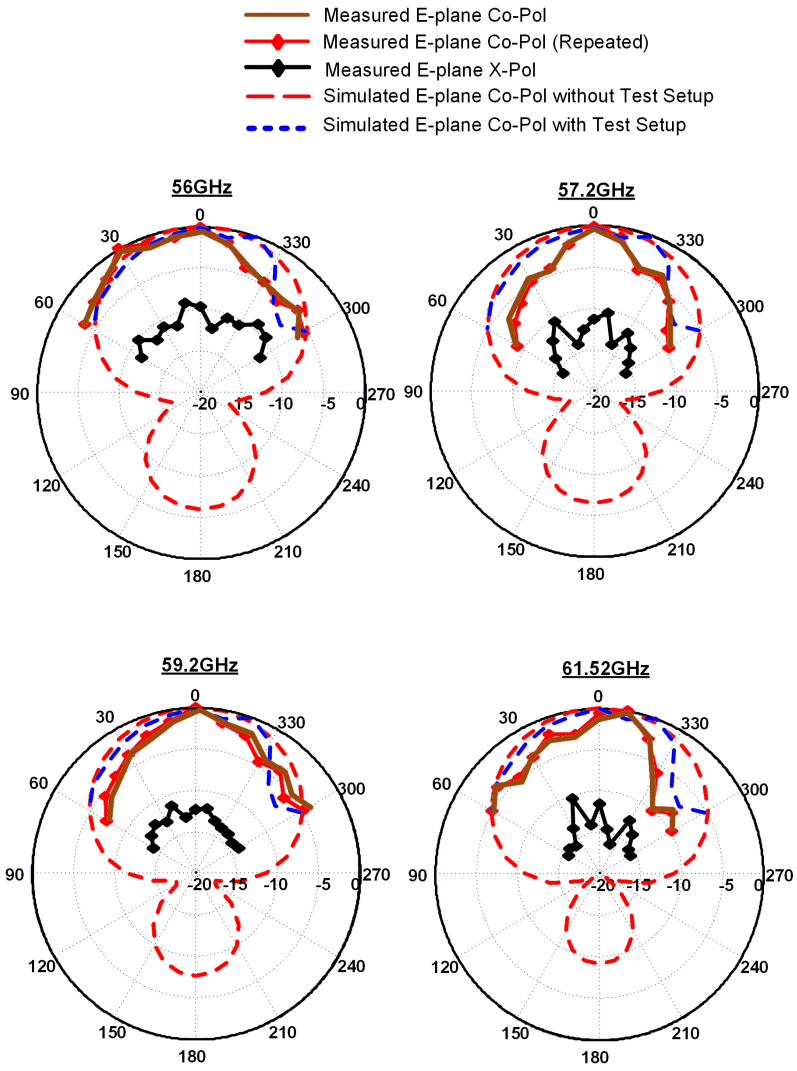


Figure 2.33: E-plane co-pol and cross-pol patterns at 56 GHz, 57.2 GHz, 59.2 GHz and 61.5 GHz.

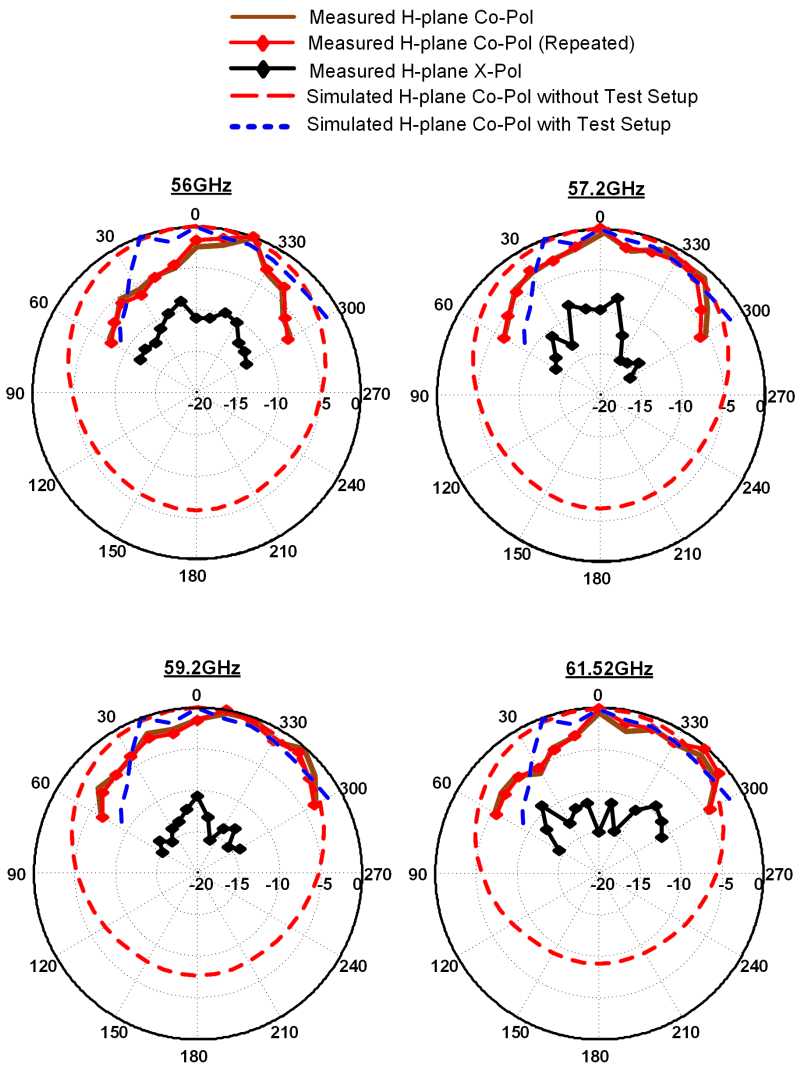


Figure 2.34: H-plane co-pol and cross-pol patterns at 56 GHz, 57.2 GHz, 59.2 GHz and 61.5 GHz.

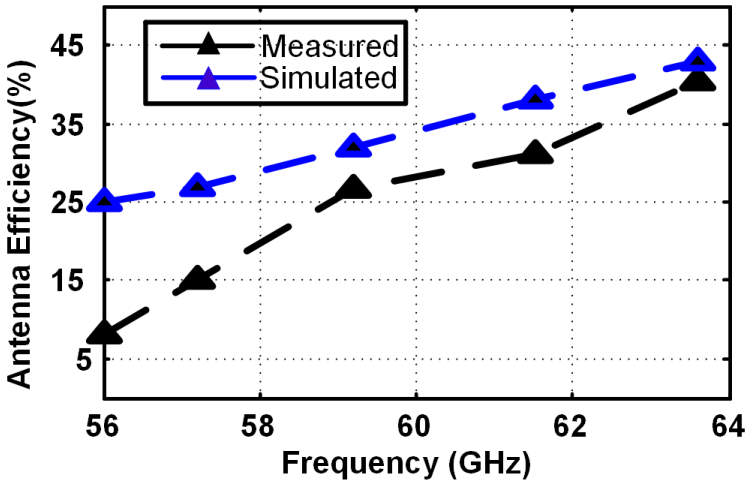


Figure 2.35: Measured antenna efficiency based on pattern in Fig. 2.33 and Fig. 2.31.

The antenna and IC are characterized using a test fixture shown in Fig. 2.32 where 3 sides are coverd by electromagnetic absorbing material to reduce the reflections. Measured antenna patterns are shown at 56 GHz, 57.2 GHz, 59.2 GHz and 61.52 GHz in Fig. 2.33 and Fig. 2.34. Measured performance is compared to simulations with and without the measurement setup. In simulation and measurement, the setup introduces assymmetry in measured patterns and limits correlation, particularly at oblique angles. Data from two measurements is plotted to verify repeatability.

As discussed in Section 2.5 the slot-structure causes radiation from the top of the IC as well due to the bidirectional radiation nature of the slot. The measured front-to-back ratio of ∼6-8 dB at four different frequencies. The measured antenna efficiency (Fig. 2.35) is estimated by averaging the output power in $\pm 20^o$ in the E and H plane to calculate the effective radiated power and compared to simulations including measurement setup.

Table 2.2 shows comparison with the state-of-the-art demonstrating efficiency higher than purely on-chip antenna approaches and comparable to superstrate approaches [9], while providing simpler packaging, less cost, less sensitivity to on-chip metal fills and is also wafer-scale compatible.

Table 2.2: Comparison with state-of-the-art IC-antenna co-integration

Ref.	Approach	Freq (GHz)	BW (GHz)	Gain (dBi) (Eff.)
This work	Aperture-coupled to patch on LCP substrate	60	8	0 (40%)
[9]	Proximity-coupling to patch on quarz superstrate	94	7.5	3 (50%)
[86]	Leaky-wave thin AMC	94	10	-2.5
[8]	Elliptical Slot with quartz superstrate	94	3.6	0.7 (26%)
[87]	Slot-folded dipole antenna	94	33	-4 (20%)

2.8 Conclusion

A wafer-scale compatible mm-wave IC-antenna co-integration approach is presented that demonstrated efficiency and bandwidths comparable to system-level performance with AiP techniques. A 60-GHz prototype using the proposed aperture-coupled backside radiation approach was fabricated with an on-chip quadrupler and antenna feed. The prototype achieves 0-dBi gain, 40% efficiency, and 10-dB cross-pol ratio and is well-suited for wafer-scale packaging. Further improvements in bandwidths are feasible with stacked patches and polarization ratio can be improved with better alignment between the patch and on-chip slot. The proposed approach can enable on-chip calibration for large-scale mm-wave arrays.

Chapter 3: 60 GHz Concurrent Dual-Polarization RX Front-End in SiGe BiCMOS with IC-Antenna Co-Integration

3.1 Introduction

As discussed in Chapter 2, the IC-antenna interface represents one of the key challenges at mm-wave, particularly for communication and radar applications based on multiple-element arrays that require extensive routing of mm-wave signals on package. Antenna-in-package (AiP) array approaches [5,70] have >1.5 dB interconnect losses leading to overall efficiency of ∼60% even with 90% stand-alone antenna efficiency. While on-chip antennas promise substantially simplified packaging, poor efficiency and bandwidth limit performance. Superstrate approaches have been proposed to address this challenge - however, coupling signals from the top of the IC complicates packaging for power, digital and baseband IO [8,9]. In Chapter 2 ([72]), we presented an antenna co-integration approach using aperture coupling where on-chip transmission-line is coupled to an antenna through the back side of the IC using a slot in the on-chip ground plane. While this wafer-scale compatible approach leads to system-level efficiencies comparable to AiP approach and is also cost effective, the implementation (as well as superstrate on-chip antenna schemes in [8,9]) is area-inefficient since the ground plane ($\sim 1.6\,\text{mm} \times 1.6\,\text{mm}$) area is not utilized, leading to large IC area.

In this work, we extend the approach in [72] to a dual-polarization approach with orthogonal slots and dual feeds. Therefore, by using the same antenna footprint, concurrent dual-polarization reception or transmission can be achieved doubling overall network capacity. Secondly, we address the challenge of area inefficiency by implementing transmission line based circuits in the ground plane area. Given the aperture-coupled approach, the ground plane separates the antenna and the transmission line based circuits, allowing the ground plane area to be reused for circuits, provided interconnect and matching networks are implemented using transmission lines. Grounded coplanar waveguide is adopted as transmission-line in order to ensure a continuous ground plane coverage on the whole chip and also provide a good signal shielding and reduce cross-

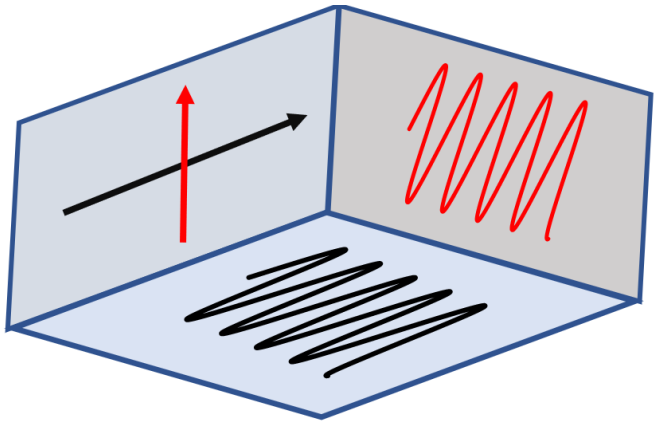


Figure 3.1: Rectangular patch antenna supports two orthogonal polarization (horizontal and vertical in this case) [10] .

coupling. This is detailed in Section 3.2. Integrating the feed network on the ICs enables architectures that leverage the ability to integrate large-scale complex circuits on silicon.

A rectangular patch antenna is linearly polarized, which implies that the electric field vector varies alone one axis. The polarization axis is perpendicular to the wave propagation direction for a transverse electromagnetic (TEM) wave. For a rectangular patch antenna, by using two feed structures, two orthogonal polarization can be achieved as shown in Fig. 3.1 [10]. Orthogonality of the two polarizations implies that dual polarization can be implemented to achieve concurrent transmission or reception on the two polarizations without interfering with each other while occupying only a single antenna footprint.

However, practical antennas have finite cross-polarization which implies that when transmitting or receiving on dual polarizations, one transmitter or receiver antenna interferes with the other which degrades system performance. This cross-polarization interference can occur across multiple antennas in multi-element phased arrays. In both single-element and multi-element dual-pol transceivers, active cancellation is required to improve isolation between orthogonal polarizations.

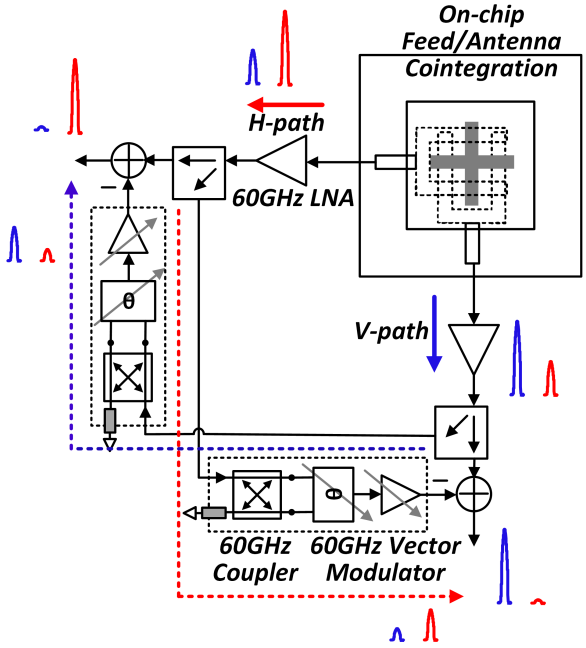


Figure 3.2: Proposed 60 GHz dual-pol RXFE with antenna feed and slot coupled to patch on back side of the IC and cross-polarization cancellation.

3.2 60GHz Dual-Polarized IC-Antenna Co-Integration

In this work [88], the dual-pol antenna feed is used to implement a dual-pol 60 GHz RX front-end (RXFE) with cross-pol cancellation using integration of antenna feeds, ground plane and active circuity as discussed before. The architecture of the implemented 60 GHz dual-pol RXFE is shown in Fig. 3.2. A square patch antenna (top view shown in Fig. 3.3, layout shown in Fig. 3.4) is designed with orthogonal dual-polarization capability. The simulated co-polarization and cross-polarization radiation pattern in both polarization plane is shown in Fig. 3.5 (Vertical polarization plane) and Fig. 3.6 (Horizontal polarization plane), demonstrating simulated -30 dB cross-polarization level in maximum radiation direction. However, this optimistic cross-pol level is not achievable considering non-ideal antenna/slot alignment during fabrication. In order to cancel the cross-pol coupling, active cancellation is used in the proposed RXFE enabling concurrent dual-pol reception at mm-wave, which is useful for communication, radar systems and polarization-diversity based MIMO links [61].

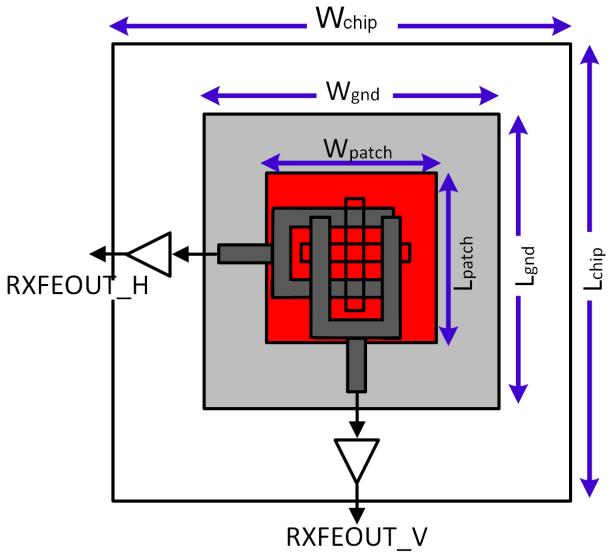


Figure 3.3: Dual-pol patch antenna top view with RXFE on both polarizatons.

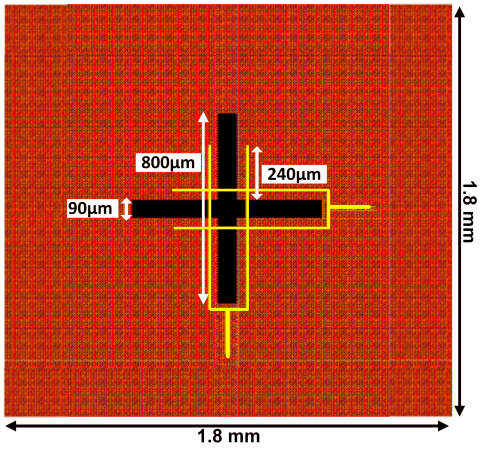


Figure 3.4: Dual-pol patch antenna layout in TowerJazz 0.18 μm SiGe BiCMOS with cross-slot and fork-shaped feed lines.

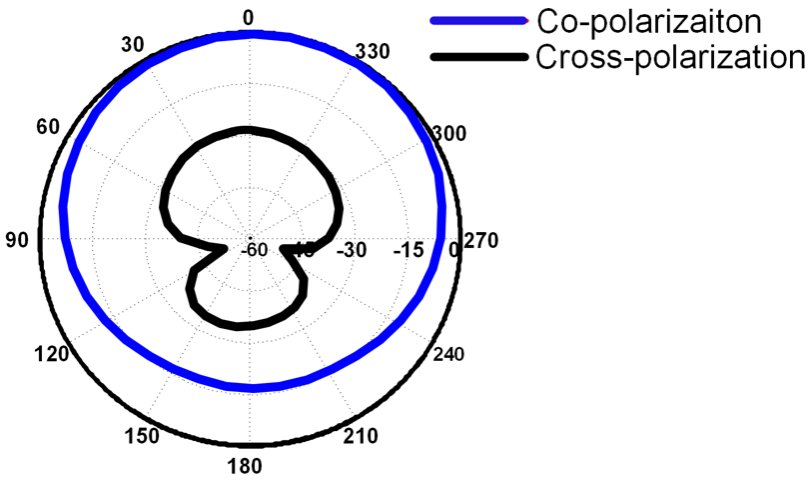


Figure 3.5: Simulated vertical plane radiation pattern.

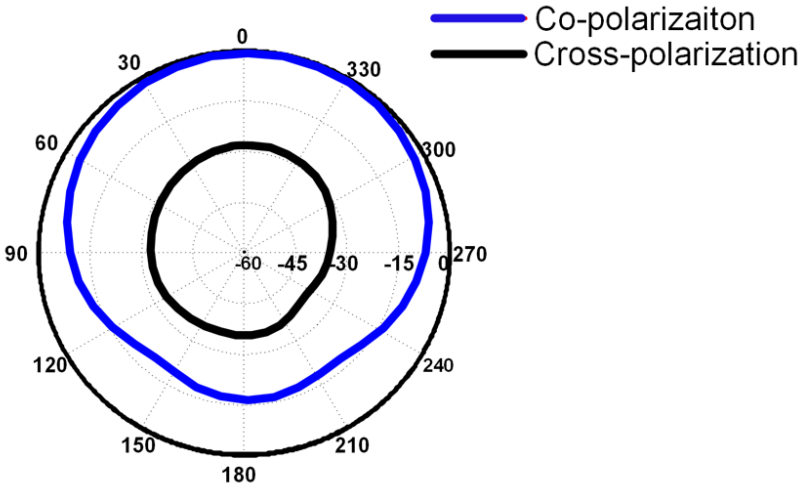


Figure 3.6: Simulated horizontal plane radiation pattern.

The antenna feed drives a 60 GHz LNA in the vertical patch (V-path) and the horizontal path (H-path). The LNA is input-matched to the 50 Ω antenna impedance using a transmission-line matching network. The final stage of the LNA splits the input signal into two paths. The first path is direct RXFE output with coupling from orthogonal cancellation path to minimize cross-polarization. The second path drives an active canceller to generate required cancellation signal for orthogonal polarization RXFE output. While the leakage signal is typically at least 10 dB lower than the desired signal as can be seen in the measurement results (Section 3.4), the amplitude and phase of the leakage signal cannot be predicted apriori. Therefore, the cancellation path must incorporate variable gain and phase shift. In this work, an active vector modulator approach is adopted to provide variable attenuation and phase shift in a single stage.

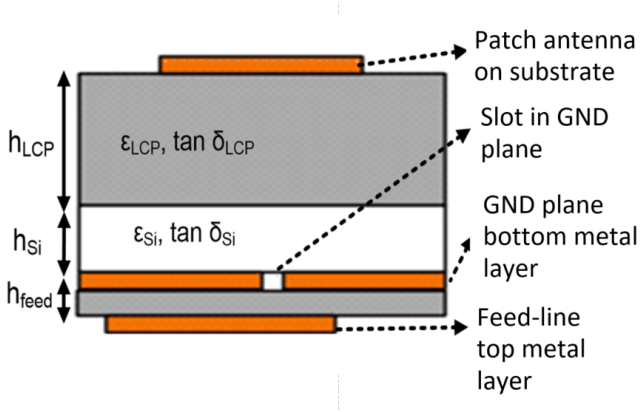


Figure 3.7: Dual-pol antenna co-integration cross section.

The antenna co-integration uses similar approach as described in Chapter 2 [72] with cross-section shown in Fig. 3.7. Following die thinning, the IC is bonded to an LCP substrate with a patch antenna on the bottom. The transmisstion line feed networks are designed with a top-metal signal layer (metal 6 in this process technology) and lower-metal (metal 1 through metal 3 in this process technology) ground-plane. The feed lines couple to the antenna on the backside of the IC through the slot in the on-chip ground plane. While the LCP substrate (thickness = 175 μm, dielectric constant = 3.1, loss tangent = 0.003) is relatively low-loss at mm-wave [85], the lossy silicon substrate (resistivity of $\sim$ 10 Ω-cm) leads to coupling losses. Thinning the silicon can reduce this efficiency degradation, with thickness of 75 μm leading to efficiency of 50% as discussed

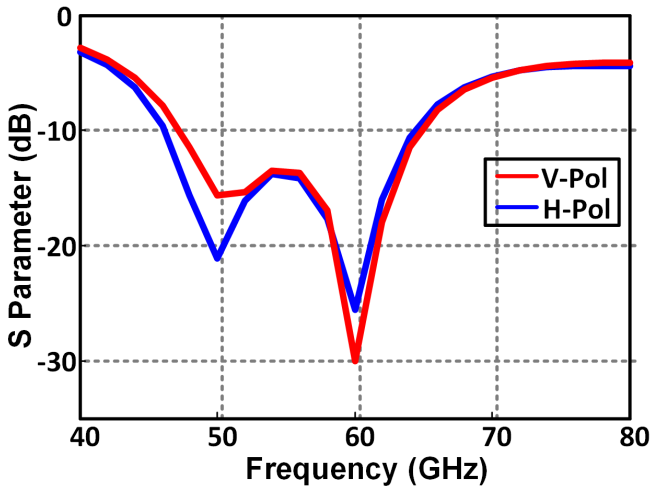


Figure 3.8: Simulated input matching (S11) of vertical polarization (V-pol) and horizontal polarization (H-pol) antenna.

in Chapter 2 [72].

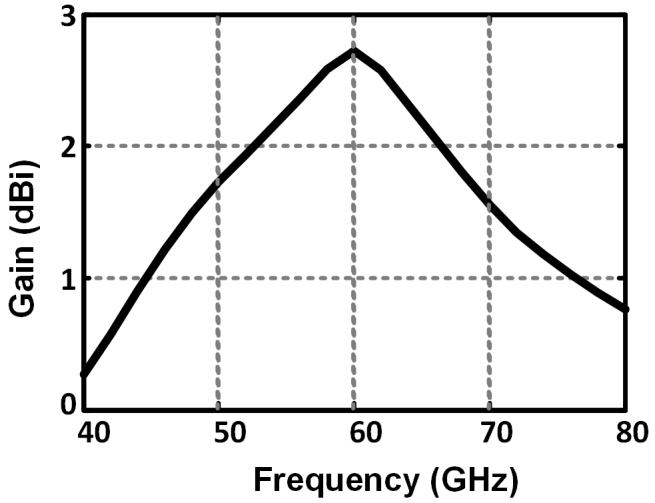


Figure 3.9: Simulated gain of dual-pol antenna-IC co-integration.

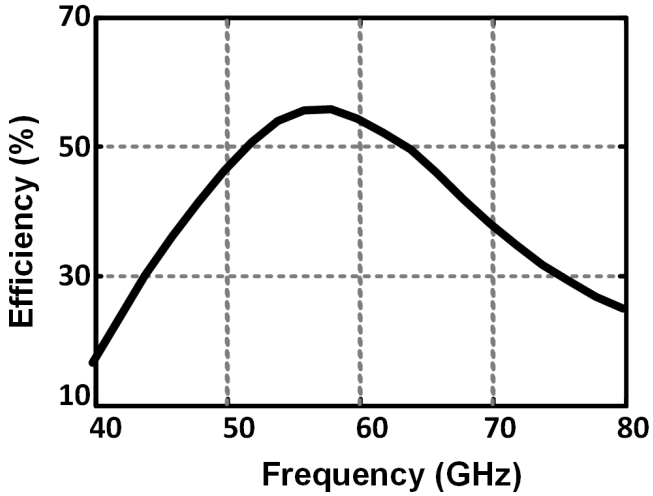


Figure 3.10: Simulated efficiency of dual-pol antenna-IC co-integration.

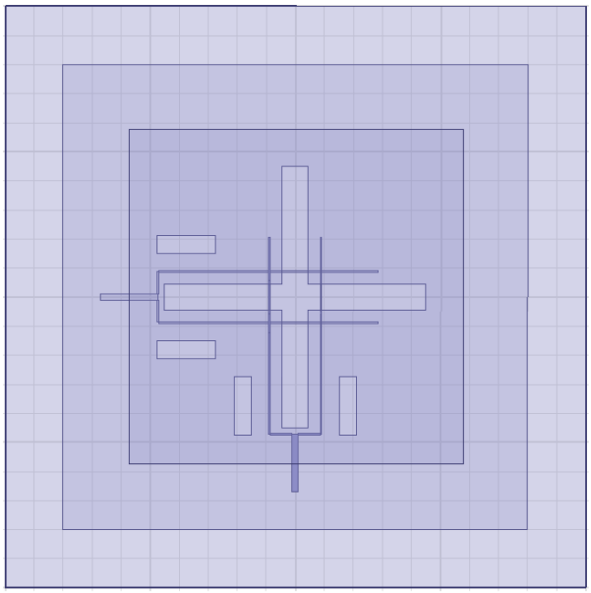


Figure 3.11: HFSS simulation in order to verify effects of ground-slot on antenna performance.

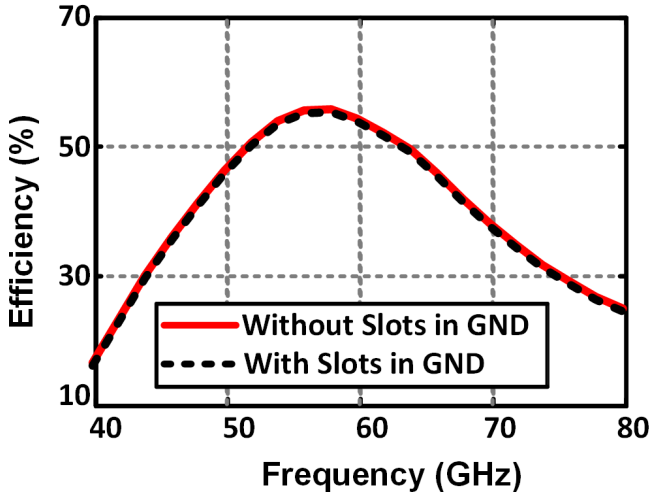


Figure 3.12: Simulated antenna radiation efficiency with and without ground slots.

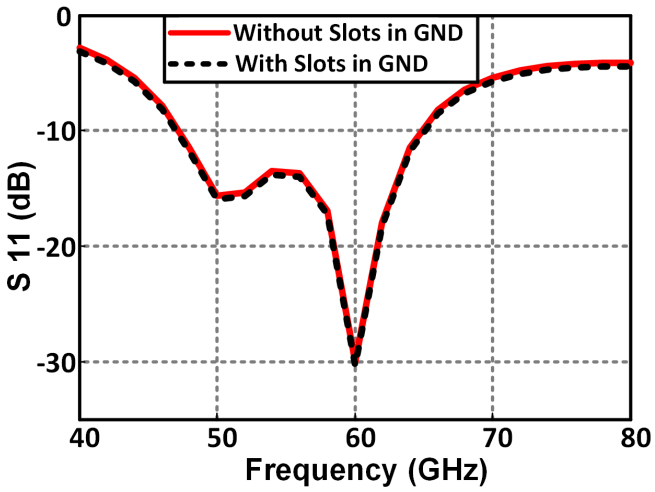


Figure 3.13: Simulated antenna input matching with and without ground slots.

In order to achieve 60 GHz dual-pol operation, orthogonal slots were designed in the ground plane with slot length of 800 μm and slot width of 90 μm(Fig. 3.4). A forked dual-pol feed structure, as shown in Fig. 3.3 and Fig. 3.4, is designed for each antenna with

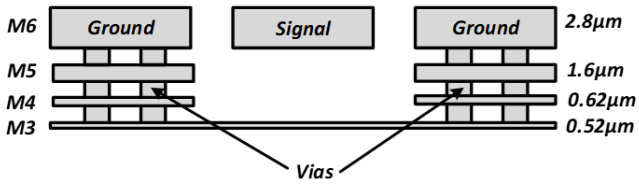


Figure 3.14: Grounded co-planar waveguide used to ensure continuous ground plane as well as negligible cross-coupling.

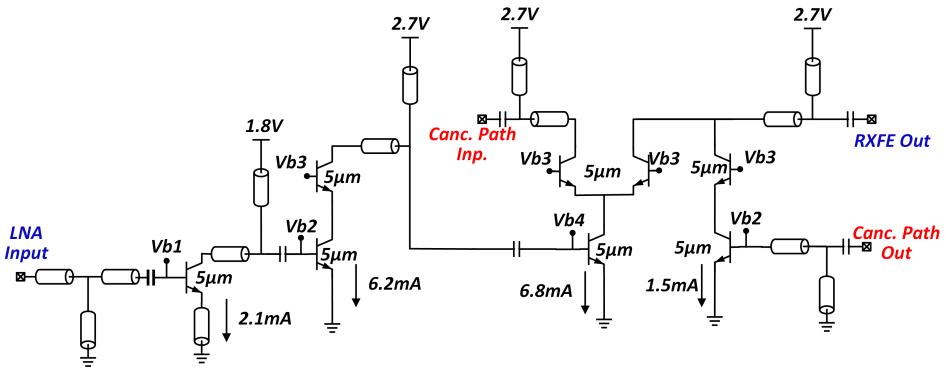


Figure 3.15: 60 GHz 3-stage LNA with signal division in the output stage between signal-path and cancellation-path.

width and length to ensure 50 Ω input impedance for each feed. Fig. 3.8 shows simulated dual-pol antenna s-parameters at 60 GHz demonstrating good impedance matching at 60 GHz for both V-pol and H-pol. The simulated ∼50% overall radiation efficiency and 2.7 dBi gain at mm-wave are shown in Fig. 3.10 and Fig. 3.9, assuming 75 μm silicon thickness and 175 μm LCP thickness.

As described in Sec. 3.1, the antenna ground plane area is unutilized in the single-pol feed structure described in Chapter. 2 ([72]). In the aperture-coupled approach, the transmission lines with the signal layer on the top metal layer are separated from the antenna by the ground plane. Therefore, on-chip transmission line networks can be designed that reuse the ground plane. Active devices can be considered to be placed in slots in the ground plane (1.8 mm×1.8 mm) that are relatively small compared to the

wavelength (as shown in Fig. 3.11) has been verified by simulations. Fig. 3.12 and Fig. 3.13 show that electrical-small on-ground slots have minimum impact on antenna efficiency and input matching S11. Therefore, circuits can potentially be integrated in the ground plane if grounded co-planar waveguide (GCPW) based transmission line networks are used. Show in Fig. 3.14 is the GCPW that has been adopted as on-chip transmission line to achieve continuous antenna ground plane as well as good shielding between signals.

3.3 60GHz Concurrent Dual-Pol Receiver Frontend with Cross-Polarization Cancellation

For the 60 GHz receiver front-end (RXFE), LNA is critical for noise according to the formula:

$$F_{system} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... + \frac{F_n - 1}{G_1 G_2 ... G_{n-1}} \tag{3.1}$$

where F_{system} is the total system noise factor, F_i and G_i are the noise factor and available power gain of the i th stage of the receiver chain. Therefore, 1^{st} stage of the RXFE has to provide enough power gain with minimum noise introduced. The LNA adopted in this work is a 3-stage structure with common emitter as 1^{st} stage and cascode as 2^{nd} and 3^{rd} stage to reduce overall noise while achieving enough gain as shown in Fig 3.15. The 1^{st} stage LNA consumes 2.1 mA at 1.8 V and 2^{nd} and 3^{rd} stage LNA consume 13 mA at 2.7 V. As discussed in Section 3.2, LNA output is divided into direct RXFE otuput signal path and cancellation path. As shown in Fig 3.15, the RXFE output signal path is combined with a transconductance stage which takes output from the other polarization cancellation path. When needed, canceller signal from the other polarization will be summed in current domain with this main RXFE output providing clean received signal of this polarization. The transconductance stage serves as both a buffer and an variable gain amplifier which is a part of the active canceller. The other LNA output connects to canceller path generating cancellation signal for orthogonal polarization. The active canceller following LNA output is a hybrid coupler, an active balun and a vector modulator.

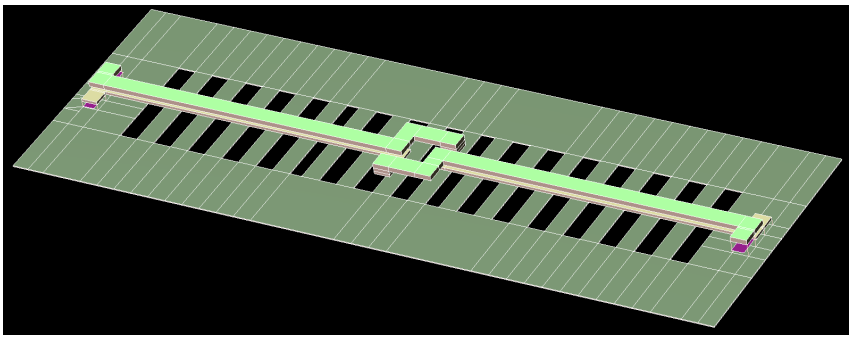


Figure 3.16: 60 GHz hybrid coupler 3D view in IE3D.

A hybrid coupler is a four-port component which generates quadrature output with ideally equal amplitude. Shown in Fig. 3.16 is a 3D view of the hybrid coupler that has been adopted in this work. The coupler occupies 400 μm $\times$ 120 μm and is simulated in Mentor Graphics IE3D [89]. The coupling is achieved using coupled microstrip transmission lines on top two metal layers. In order to ensure matching to an impedance Z_0, the coupler's characteristic impedance must be Z_0. Using [90]

$$Z_0 = \sqrt{Z_{0e} Z_{0o}} \tag{3.2}$$

where Z_{0e} and Z_{0o} are even mode and odd mode transmission line characteristic impedance. The voltage coupling coefficient C (in this case 3dB or 0.707), can be calculated as

$$C = \frac{Z_{0e} - Z_{0o}}{Z_{0e} + Z_{0o}} \tag{3.3}$$

The simulated hybrid coupler output phase difference and amplitude imbalance is shown in Fig. 3.17 and Fig. 3.18 respectively, demonstrating <0.5 dB through and coupled port amplitude imbalance across a 10 GHz bandwidth.

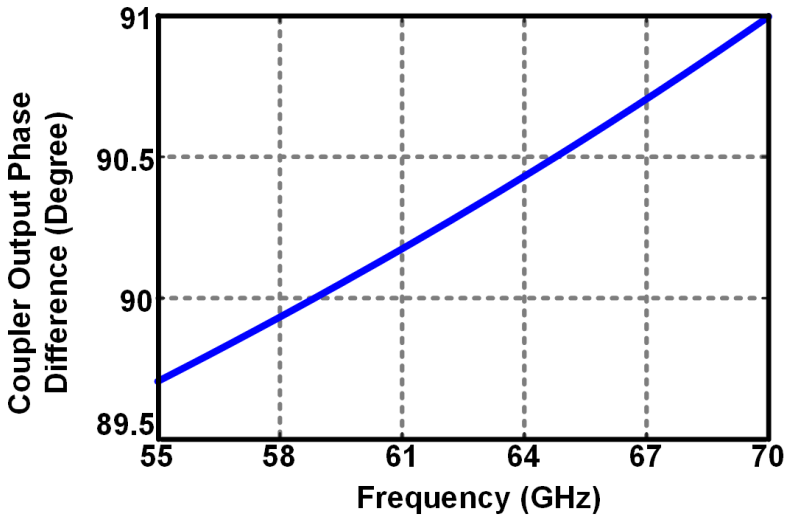


Figure 3.17: Simulated 60 GHz hybrid coupler output phase difference.

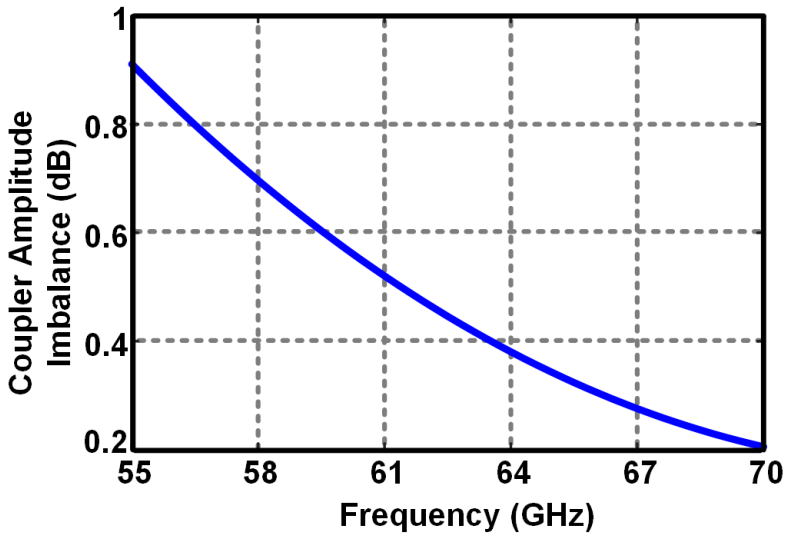


Figure 3.18: Simulated 60 GHz hybrid coupler output amplitude imbalance.

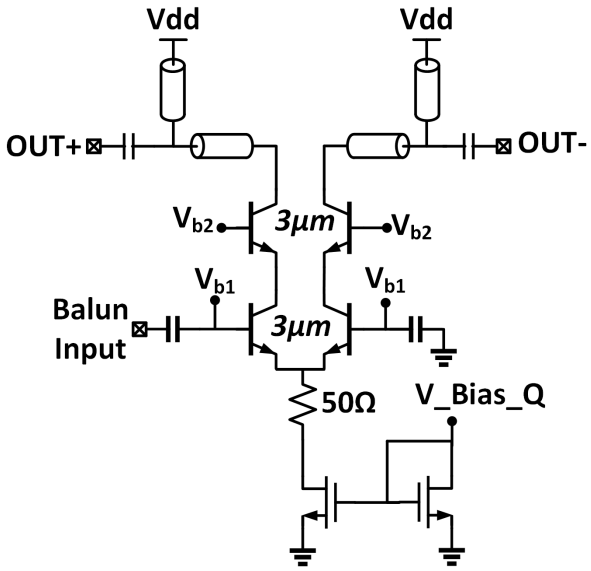


Figure 3.19: 60 GHz active balun for differential signal generation.

Active balun following the hybrid coupler (as shown in Fig. 3.19) in the I and Q paths generates quadrature differential signals that drive a vector modulator. A 50 Ω resistor is added at the common emitter to increase common-mode rejection at the expense of reduced headroom. The vector modulator interpolates between I and Q phases to provide variable phase shift as shown in Fig. 3.20 and Fig. 3.21. Changing the relative weight of I and Q signals also leads to variable amplitude. The single-ended vector-modulator output drives a transconductance stage which combines the LNA output and cancellation path output to achieve cross-polarization leakage cancellation. The canceller path shown in Fig. 3.22 (i.e. the passive hybrid coupler, the active balun and the vector modulator) consumes 36 mA at 2.7 V.

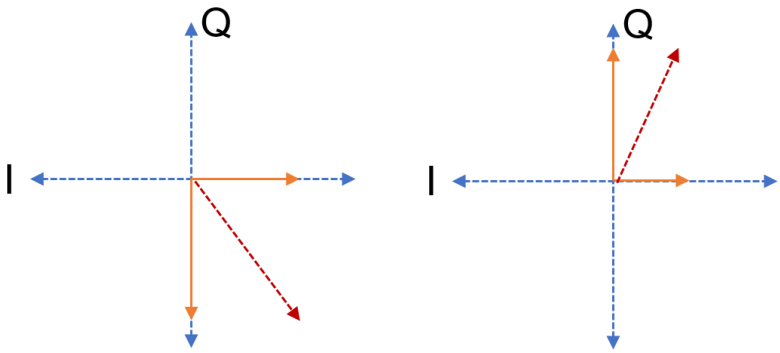


Figure 3.20: Vector modulator interpolates between I and Q phases to provide variable phase shift.

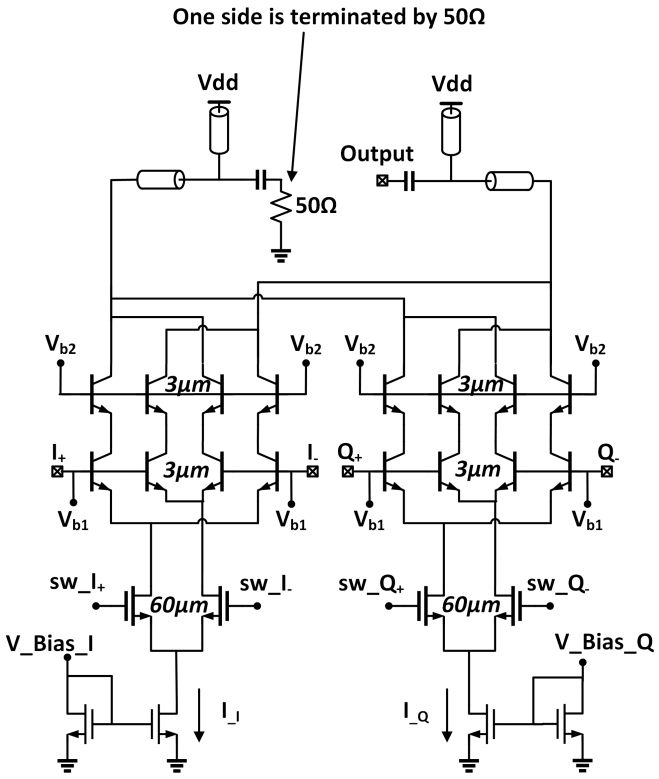


Figure 3.21: Vector modulator structure used to change I and Q component relative weight.

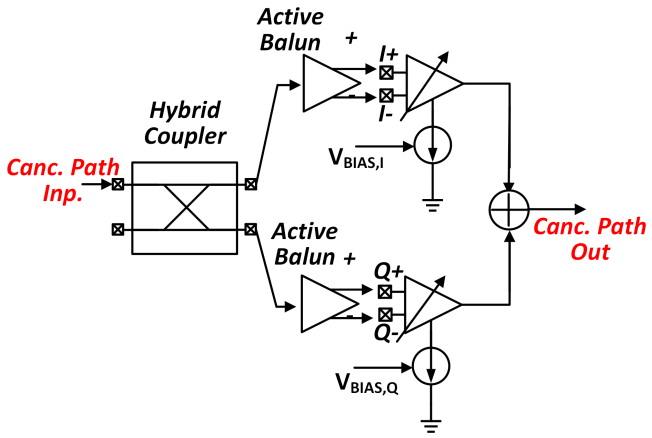


Figure 3.22: The cancellation path includes a hybrid coupler, an active balun and a vector modulator to achieve 360° phase variation.

3.4 Measurements and Performance

The proposed approach was implemented in the TowerJazz 0.18 μm SiGe BiCMOS process technology (with six metal layers). The layout is shown in Fig. 3.23 to demonstrate the compact layout of the antenna-cointegrated dual-polarization RXFE. The total chip size is 2.2 mm $\times$ 2.2 mm where antenna ground plane dimension is 1.8 mm $\times$ 1.8 mm. The IC layout supports probe testing of each polarization path including LNA path and active canceller path as shown in Fig. 3.24. Probe testings are enabled by focused-ion beam trimming of the antenna feed lines as shown in Fig. 3.25. Extensive ground plane reuse leads to compact area where the whole dual-pol RXFE is designed inside the ground plane of the antenna. The measured LNA S11 and S22 are shown in Fig. 3.26, demonstrating reasonable input and output matching around 60 GHz. Measured LNA S21 is shown in Fig. 3.27 demonstrating 11 dB gain. However, the measured gain is lower than simulated gain and shifted to higher frequency which has been traced to simulation inaccuracies in transmission line matching networks. A revised design with longer transmission lines has been fabricated and measured and is presented in Chapter 4. The measured 60 GHz cancellation path phase shift is shown in Fig. 3.28, demonstrating a full 360^o phase shift range across a wide bandwidth. Fig. 3.29 shows measured canceller gain varies from 20 dB to -30 dB, demonstrating capability to match the cross-

polarization leakage signal level. The overall measured active canceller performance is shown in Fig. 3.30. Measured LNA path noise figure is <8 dB as show in Fig. 3.31.

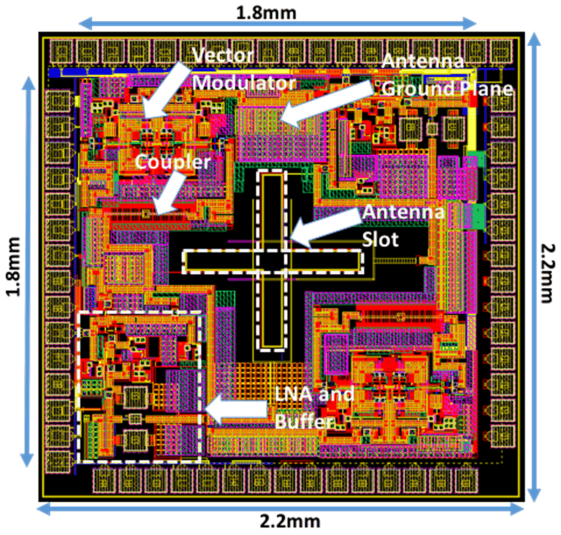


Figure 3.23: Dual-polarized IC-antenna co-integrated RXFE layout with ground plane extensively reused by active circuits implemented in TowerJazz 0.18 μm SiGe BiCMOS process technology.

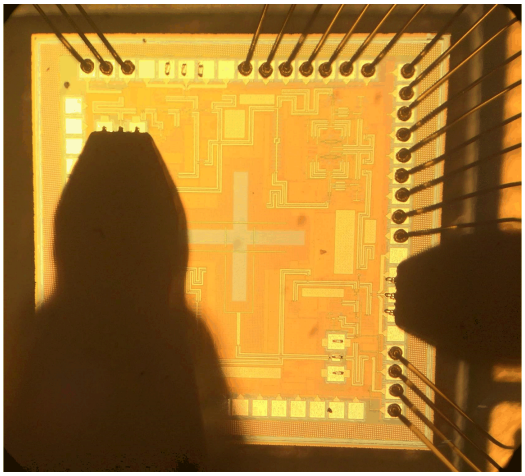


Figure 3.24: Probe testing of V-path and H-path following focused-ion beam trimming.

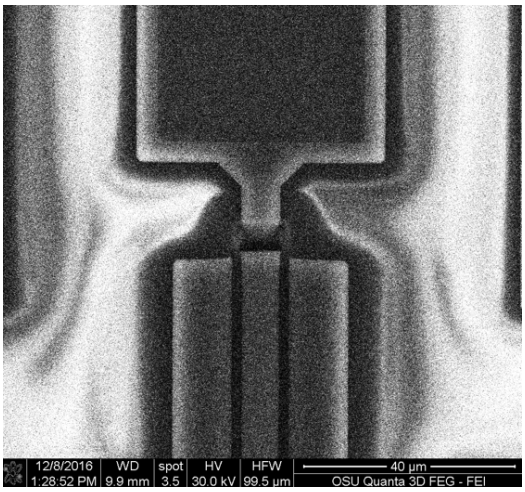


Figure 3.25: Micro-photo of focused-ion beam trimming for antenna feed lines.

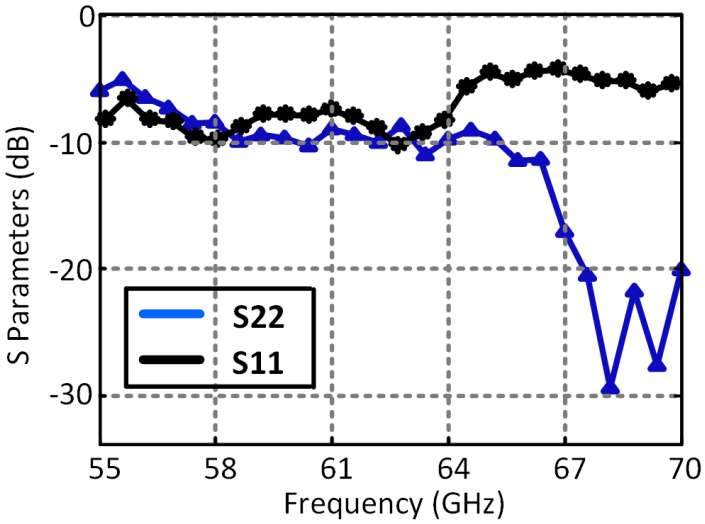


Figure 3.26: Measured LNA input and output matching.

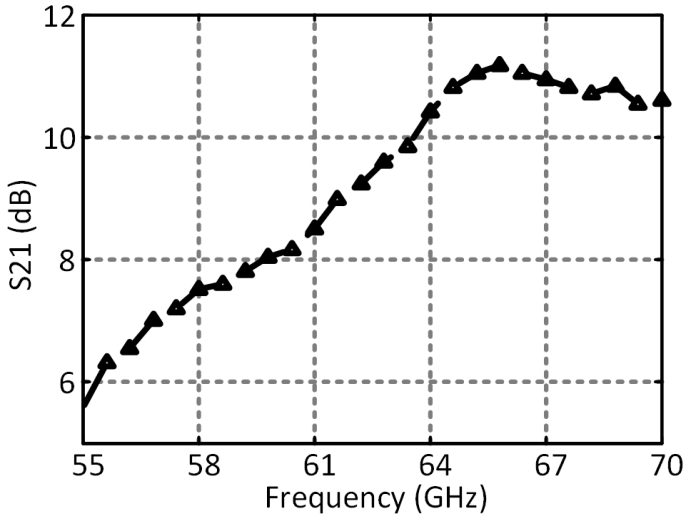


Figure 3.27: Measured LNA gain across frequency.

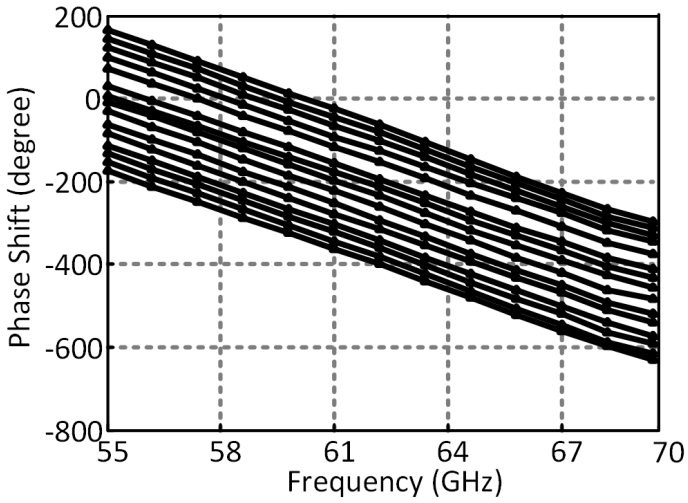


Figure 3.28: Measured cancellation path variable phase shift demonstrating 360^o variable phase shift range across wide bandwidth.

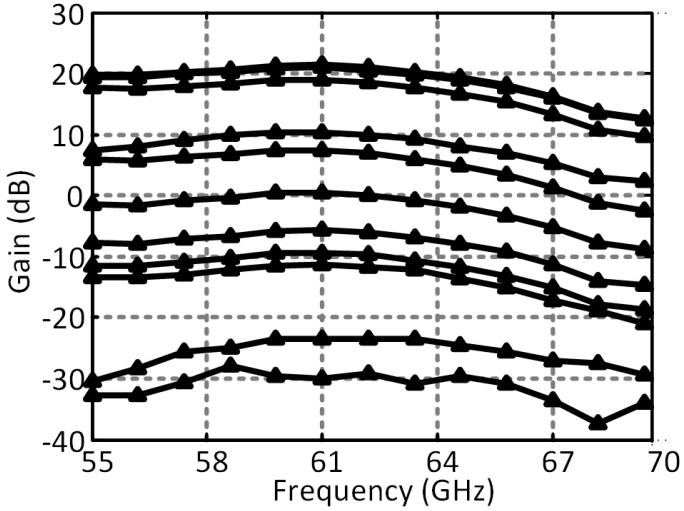


Figure 3.29: Measured cancellation path gain around 60 GHz.

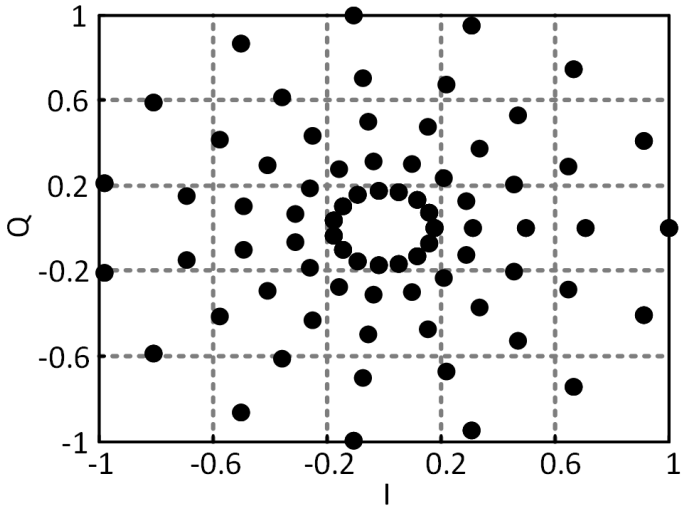


Figure 3.30: Measured canceller performance demonstrating variable gain and phase shift.

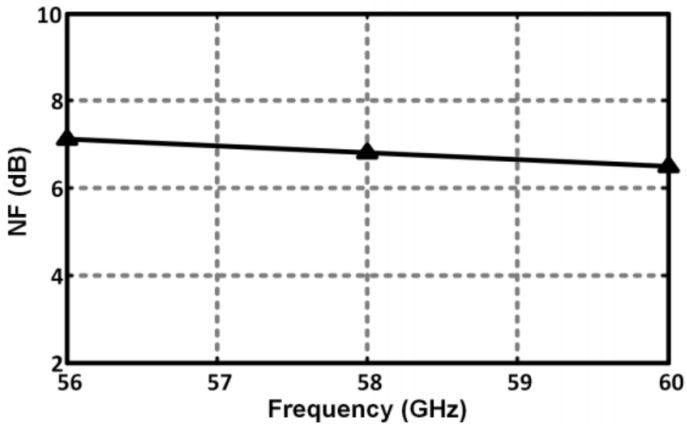


Figure 3.31: Measured LNA noise figure across frequency.

The IC is thinned to 75 μm and packaged with 175 μm LCP using the approach outlined in Fig. 3.7 [72]. The patch antenna metal (1000 μm$\times$1000 μm) is defined on the Rogers 3850 LCP. The packaging cross-section and top view are shown in Fig. 3.32 and Fig. 3.33. The wireless measurement setup is shown in Fig. 3.34. Fig. 3.35 plots the normalized cross-polarized signal leakage power with and without cancellation across frequency when the cancellation is optimized at one frequency (60 GHz). The variable gain/phase cancellation path is able to achieve $\sim$30 dB cross-pol cancellation with a 10 dB attenuation bandwidth of 1 GHz (this attenuation is additive to the $\sim$-10dB cross-pol ratio). Fig. 3.36 shows the measured antenna pattern with and without the cancellation when the cancellation is optimized for one particular direction (0°). Measured co-pol and cross-pol signals under this condition demonstrate that the cross-pol cancellation can achieve <-40dB cross-pol ratios in the targeted direction.

Concurrent reception of dual-polarized signals is measured with the H-pol and V-pol signals at 60 GHz and 60.004 GHz respectively. The cancellation-path in each pol are independently optimized to cancel the corresponding cross-leakage as shown in Fig. 3.37 and Fig. 3.39. Cross-polarization cancellation results are shown in Fig. 3.38 and Fig. 3.40, where concurrent -30 dB lower cross-pol signal is achieved at each polarization output demonstrating the suitability of this approach for concurrent dual-pol mm-wave receivers for communication and radar.

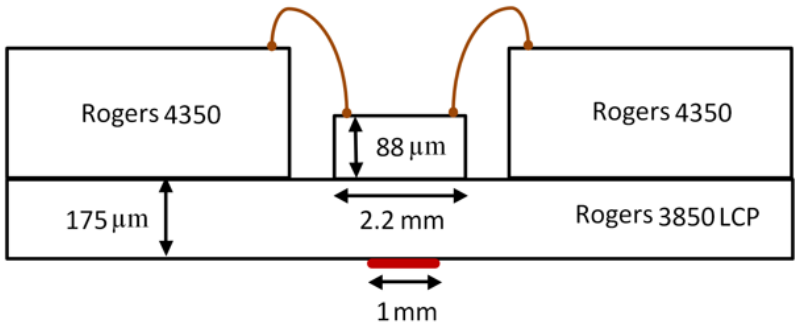


Figure 3.32: Dual-pol IC-antenna co-integration packaging cross-section.

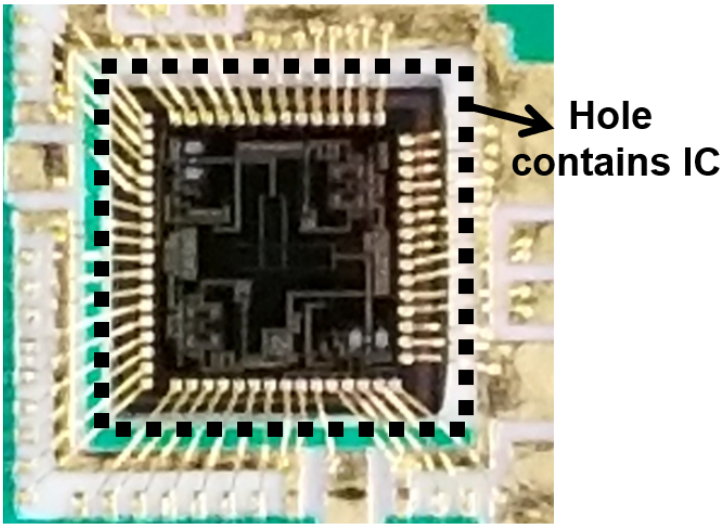


Figure 3.33: Dual-pol IC-antenna co-integration packaging top-view.

3.5 Conclusion

A dual-polarization mm-wave IC-antenna co-integration approach is presented that demonstrates efficiency and bandwidths comparable to system-level performance with AiP techniques. A 60-GHz prototype using the proposed dual-pol feeds and aperture-

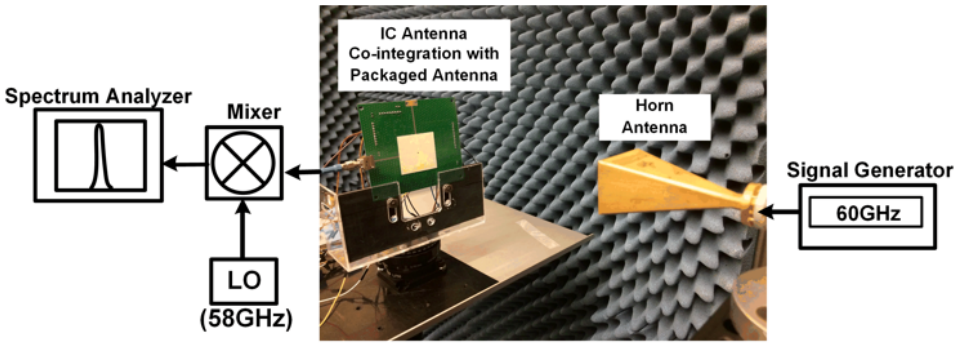


Figure 3.34: Wireless measurement setup following antenna co-integration

coupled backside radiation is implemented in the context of a 60 GHz dual-pol RXFE. The prototype demonstrates concurrent dual-pol reception with > 30 dB cross-pol cancellation (-40 dB total cross-polarization level) while also ensuring extensive ground plane reuse to minimize silicon area. Further improvements in bandwidths are feasible with stacked patches and intrinsic antenna cross-polarization level can be improved with better alignment between the patch and on-chip slot.

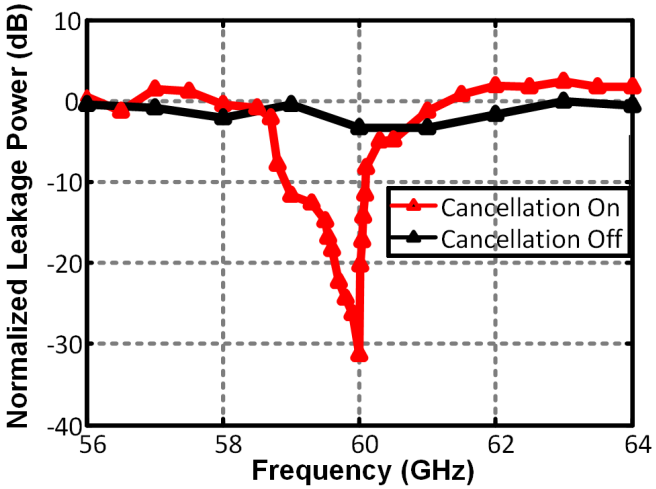


Figure 3.35: Measured polarization cancellation: Normalized leakage power across frequency with cancellation optimized at 60 GHz.

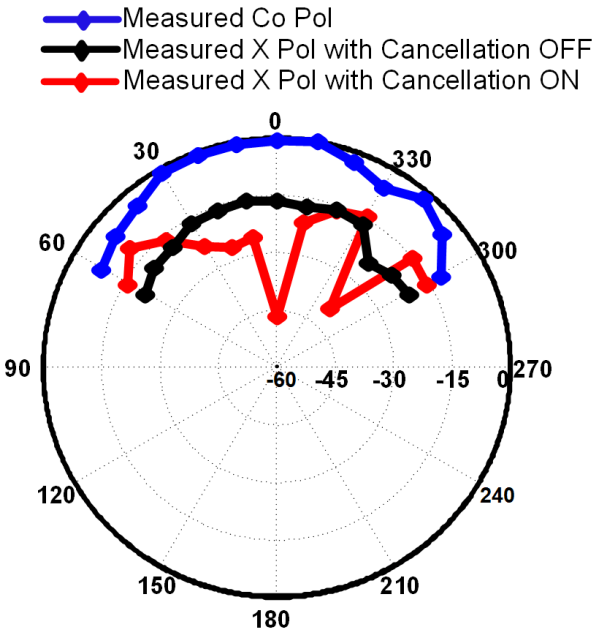


Figure 3.36: Measured polarization cancellation performance: Co-pol and cross-pol radiation pattern with cancellation optimized at 0° angle.

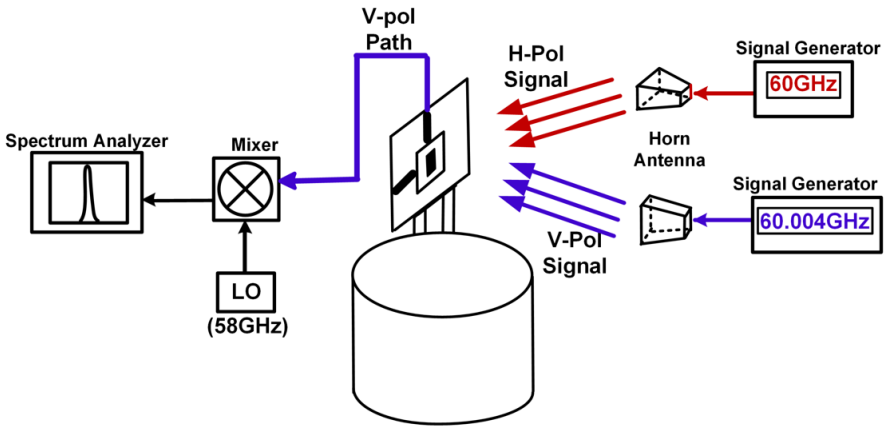


Figure 3.37: Measurement setup to demonstrate V-path cross-polarization cancellation performance.

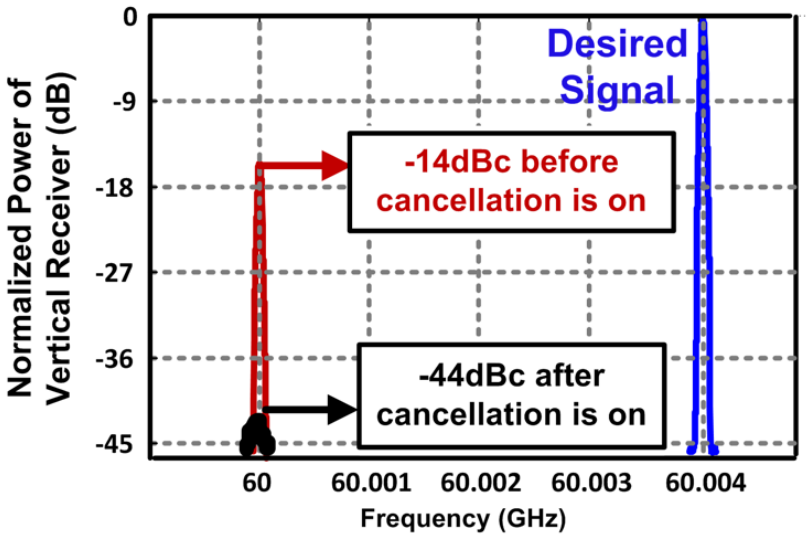


Figure 3.38: Measured polarization cancellation performance: Dual-pol RXFE measurements demonstrating ∼30 dB cancellation of cross-pol signals in V-path.

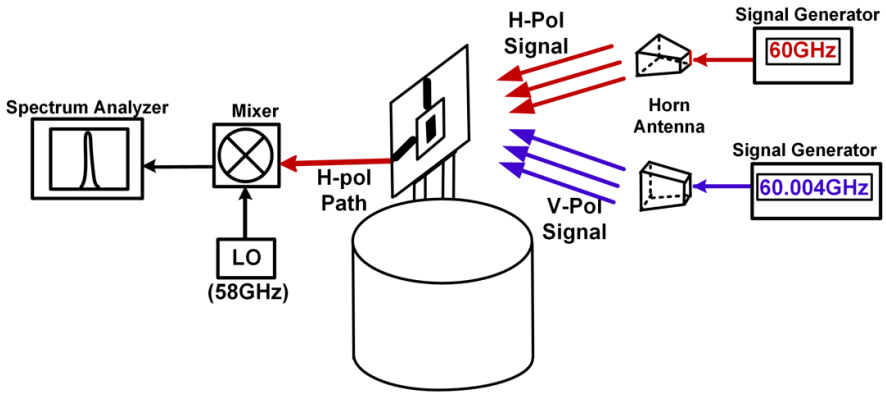


Figure 3.39: Measurement setup to demonstrate H-path cross-polarization cancellation performance.

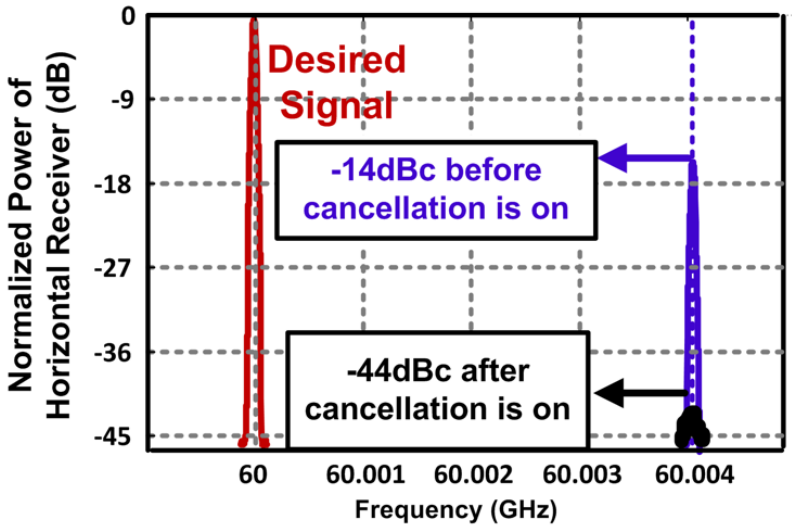


Figure 3.40: Measured polarization cancellation performance: Dual-pol RXFE measurements demonstrating ∼30 dB cancellation of cross-pol signals in H-path.

Chapter 4: 60 GHz Polarization-Duplex TX/RX Front-End in SiGe BiCMOS with Dual-Pol Antenna Co-Integration

4.1 Introduction

It has been more than a decade since the introduction of fully-integrated mm-wave transceivers (TRX) and arrays in CMOS and SiGe [91, 92]. However, ubiquitous consumer mm-wave communication links have been limited by a (a) challenging propagation channel at mm-wave that often requires a line-of-sight (LOS) or reflected LOS path and large-element arrays for closing link budget, and, (b) high power consumption and packaging costs for such large mm-wave arrays, particularly if multiple array TX/RX are required to support multiple mobile device orientations. Additionally, while mm-wave radar applications are maturing, increasing number of sensors will require TX/RX to operate in environments/applications with significant interference.

Path loss is critical for communication links especially at mm-wave. Measurements on 5G links at mm-wave demonstrate that measured path loss is 25dB-30dB higher for NLOS as compared to LOS links at mm-wave, which have close to free space path loss [11] as shown in Fig. 4.1. Therefore, link budgets would need to accommodate 30dB higher loss. If such link budgets are targeted using TX and RX arrays it implies an 10x increase in array size to accommodate NLOS compared to LOS links. Relays/repeaters are well-known for extending the range of wireless links as shown in Fig. 4.2. This approach seems particularly well-suited for mm-wave applications that are sensitive to shadowing but at the same time must satisfy mobile form factors and power budgets. The most spectrally efficient and low-latency way to achieve relay operation is a full-duplex (FD) TRX. A frequency-domain duplex (FDD) TRX trades-off spectral efficiency for ease of implementation but still maintains low latency. Broadly, simultaneous transmit and receive (STAR) architectures that support FD and FDD are critical for such mm-wave low-latency relays in communication links.

The challenge of STAR operation is also very relevant for radar systems for automotive and robotic navigation applications. While frequency-modulated continuous-wave

(FMCW)/pulse-modulation approaches enable high energy and high-resolution simultaneously, a critical challenge is that the RX must detect reflected signal while TX is operating. In this case, there are two main sources of interference in the RX as shown in Fig. 4.3: (a) self-interference (SI) from the transmitter (which is particularly critical for shared-antenna systems) and (b) reflections for nearby objects that can be strong enough to saturate the RX. These constraints demand that in order to keep LNA and mixer operate with high linearity, the TX/RX isolation has to be increased with the increasing TX output power as shown in Fig. 4.4. Fig. 4.5 presents the trade-off between noise and TX/RX isolation. It can be seen that to achieve low noise figure, LNA gain has to be increased, which leads to higher required TX/RX isolation. Canceling the reflections and self-interference is a promising approach to reject these interferences and increase TX/RX isolation. However, a critical challenge is that such cancellation must achieve wide bandwidth, low noise and small form factor.

[From G. R. MacCartney et al., IEEE PIMRC 2014] [11]

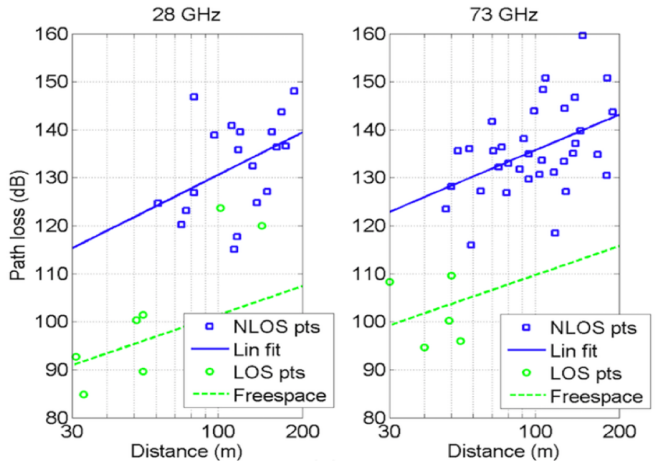


Figure 4.1: Shadowing loss in NLOS at mm-wave communication links [11].

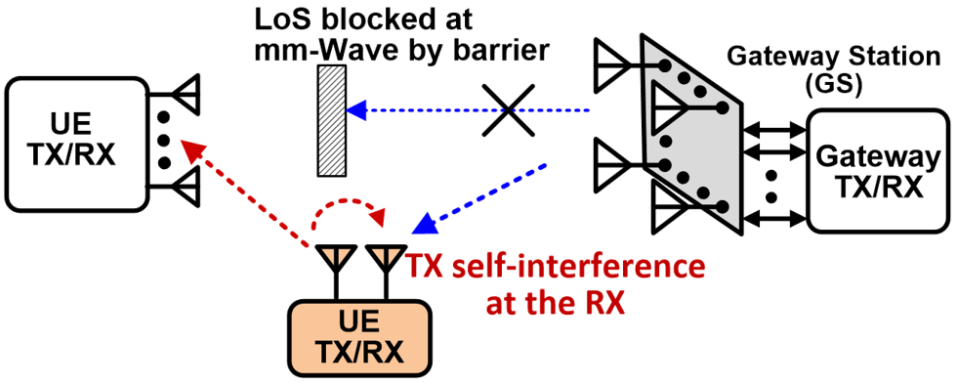


Figure 4.2: Mm-wave relays extend link range using STAR TRX while achieving low latency high data-rate link.

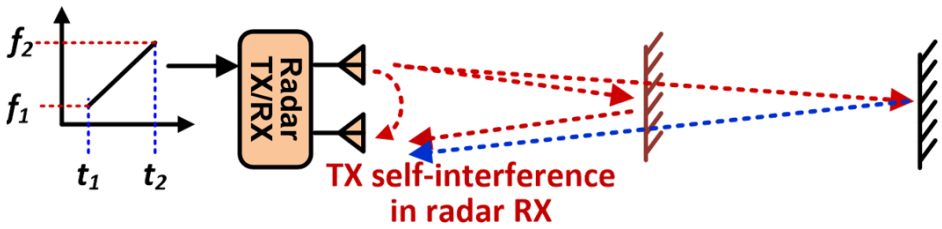


Figure 4.3: Interference problems in radar system.

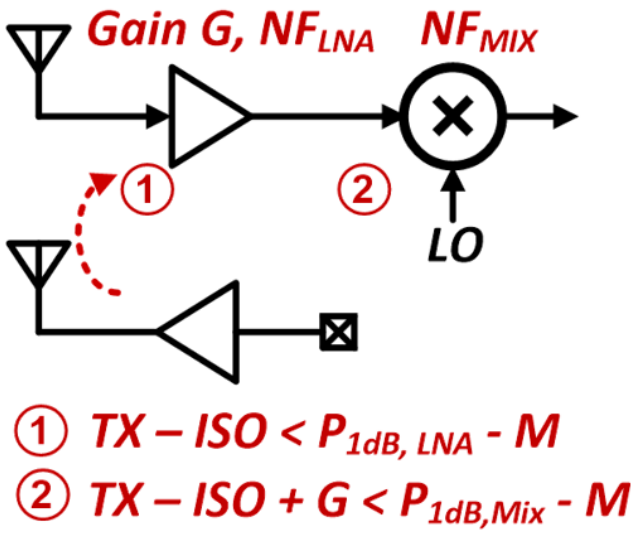


Figure 4.4: Requirements for TX power and TX/RX isolation in order to keep LNA and mixer operate with high linearity.

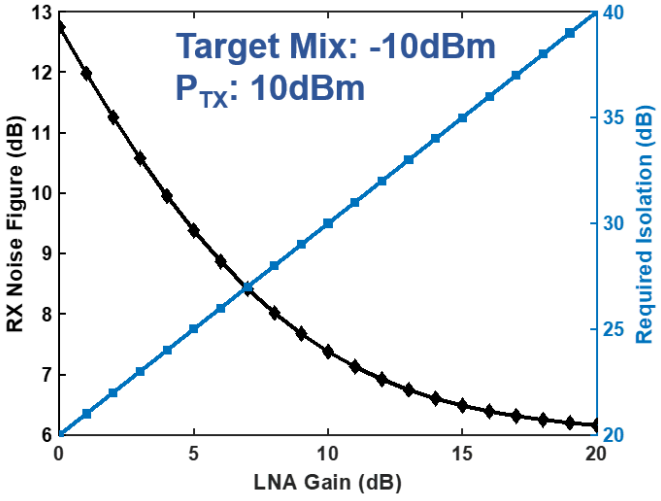
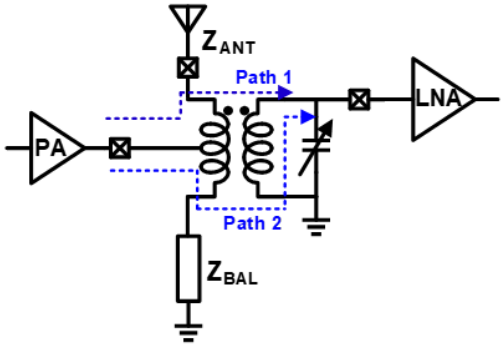


Figure 4.5: Required TX/RX isolation to accommodate LNA gain for reducing RX noise figure.

4.2 Simultaneous-Transmit-and-Receive State-of-the-Art

Several antenna self-interference cancellation (SIC) techniques have been demonstrated targeting wide bandwidth and low-noise SIC [12–15]. An electrical-balance duplexer is demonstrated [12] (Fig. 4.6) operating at 2 GHz. It achieves high linearity with >70 dBm IIP3. However, the 3 dB fundamental signal loss directly adds to RX noise figure and also degrades TX output power.

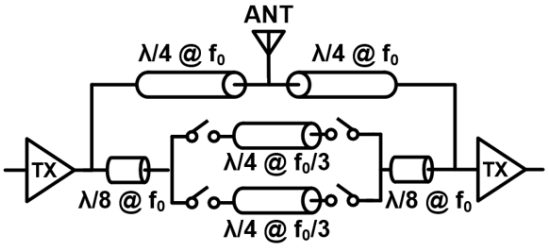
Non-reciprocal magnetic-free passive CMOS circulator has also been demonstrated as shown in Fig. 4.7 [13]. It supports shared antenna duplexer structure and presents no fundamental source of loss. However, it doesn't support FDD operation and in practice >3 dB TX to antenna and antenna to RX loss also degrades TX output power and RX noise figure. It also requires power-hungry LO driving circuitry at higher frequency mm-wave band.



Tech	0.18μmSOI CMOS
Freq.	1.9-2.2GHz
TX to Ant	-3.7dB
Ant to RX	-3.9dB
TX to RX Isolation	> 50dB

Figure 4.6: Single-ended electrical-balance duplexer at 1.9–2.2 GHz with 70 dBm IIP3 [12].

Another way to implement high isolation TX/RX SIC is to utilize antenna intrinsic isolation. As discussed in Chapter 3, dual-polarization provides orthogonality between each polarization leading to reasonable intrinsic isolation. Therefore, dual polarization can be adopted for concurrent transmitting, concurrent receiving or simultaneous transmit and receive. Such a dual-polarization TX/RX capability in mm-wave transceivers (TRX) promises increased data rates for given antenna area as well as the ability to



Tech	45nm SOI CMOS
Freq.	25GHz
TX to Ant	-3.3dB
Ant to RX	-3.2dB
TX to RX Isolation	> 18.5dB

Figure 4.7: Magnetic-free non-reciprocal passive CMOS circulator at 25 GHz [13].

perform dual-pol imaging in radar transceivers. Integrated dual-pol TRX have been demonstrated in SiGe [60, 61] and CMOS [14, 15, 93] at 28 GHz, 60 GHz and 94 GHz.

In [14], dual-polarized slot loop TX/RX antenna has been implemented on PCB to take advantage of the intrinsic dual-pol antenna isolation as shown in Fig. 4.8. It achieves 32–36 dB isolation across 54–66 GHz frequency band. To further increase the isolation, an auxiliary port on the RX antenna has been introduced. This leads to an additional coupling path from TX to RX whose coupling level depends on the auxiliary reflective termination. Similar to a 3-port network, the isolation between TX port and RX port can be reconfigured by auxiliary port termination at different environment scattering which lead to a wideband SI cancellation. A second RF cancellation path has also been implemented to further supress residual SI to achieve >70 dB SI suppression.

This on-PCB antenna dual-polarization antenna plus auxiliary port approach achieves wideband SI supression with reconfigurability. However, implementing both TX and RX antenna on PCB occupies large area leading to integration difficulty when scalability to large number of array elements is requried. Also, this auxiliary reflective termination degrades TX antenna gain and RX noise figure by 1.1 dB and 0.52 dB respectively, resulting to lower TX EIRP and increased RX noise figure.

In order to eliminate the challenging mm-wave IC-antenna interface and reduce antenna footprint, [15] demonstrates an simultaneous transmit and receive with on-chip antenna. An multi-feed on-chip slot loop antenna with high TX/RX isolation and passive RF cancellation path has been implemented on 45 nm CMOS SOI technology with high resistivity substrate as shown in Fig. 4.9. Antenna SIC >35 dB and total antenna+RF SIC >60 dB at several frequency range has been acheived.

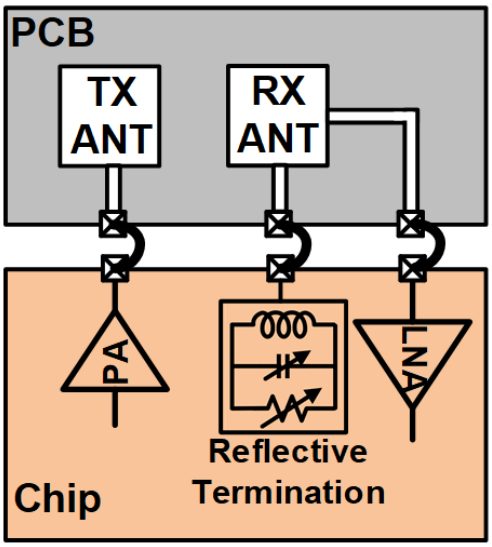


Figure 4.8: On-PCB TX/RX dual-polarization antenna pairs with auxiliary port to demonstrate polarization based duplexing [14].

This polarization-based duplexing approach greatly reduced antenna footprint and creates an highly integrated IC-antenna interface which is suitable for multi-element phased arrays or MIMO systems. However, the high on-chip antenna efficiency is due to high resistivity of SOI technology, which is not the case for bulk CMOS process. Also the antenna radiation pattern of this approach is end-fire which presents a challenge from link packaging perspective for array applications.

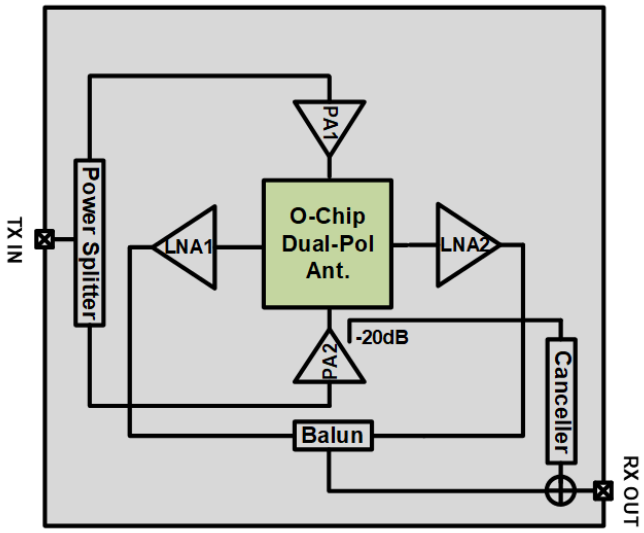


Figure 4.9: On-chip multifeed dual-polarization antenna with passive cancellation to demonstrate polarization-based duplexing [15].

Therefore, a simultaneous transmit and receive approach with efficient IC-antenna interface and wafer-scale compatibility is desirable for multi-element phased array and MIMO. The desired approach should also accommodate bulk CMOS process with broadside radiation pattern for efficient array packaging.

4.3 60 GHz Dual-Polarized IC-Antenna Co-Integration with High Polarization Isolation

A wafer-scale dual-pol antenna-cointegration approach has been demonstrated in [72, 88] where on-chip feed line is aperture-coupled through on-chip slot to a patch antenna through the substrate. In this approach, the feed co-integration eliminates mm-wave IO to/from the IC simplifying packaging for mm-wave arrays while achieving overall efficiency comparable to efficiency including package/routing in off-chip antenna arrays. In this work [94], similar IC-antenna co-integration has been extended to a 60 GHz integrated polarization-duplex front-end as shown in Fig. 4.10 . The proposed STAR TRX

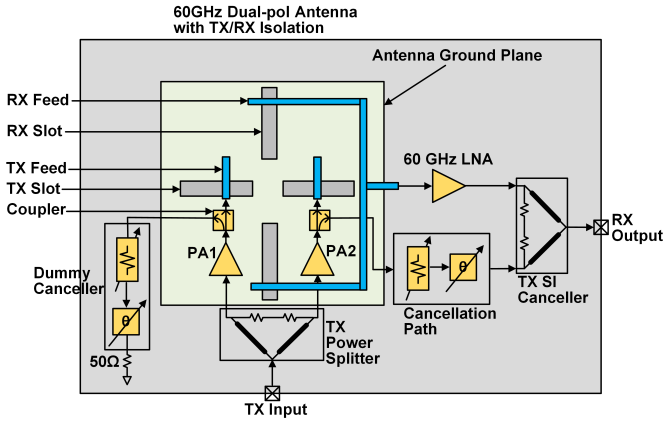


Figure 4.10: Proposed 60 GHz STAR TRX Architecture: Dual-polarization antenna with high TX/RX isolation and passive canceler are used to provide two stage TX self-interference cancellation.

frontend is compatible with low-resistivity substrates (suitable for bulk silicon) and also provides broadside radiation for both polarizations (desirable for array packaging). The dual-polarization antenna is designed to increase isolation between orthogonal polarizations. The intrinsic dual-polarization isolation is then combined with TX self-interference cancellation through a all passive variable gain/phase shift path. The approach achieves 27 dB to 38 dB isolation between antenna feeds alone across 56 GHz to 68 GHz. The passive cancellation path provides additional SIC, with total average SIC >40 dB for 1 GHz RF bandwidth at 60 GHz.

Fig. 4.11 shows the IC-antenna co-integration cross section similar to Chapter 3. Fig. 4.12 shows the top view of proposed antenna structure with cross-pol feed and dual-pol slots in the ground plane of the IC with its design parameters shown in Table. 4.1. Fig. 4.13 shows the 3D view of the proposed dual-pol antenna. The antenna feeds are implemented in top metal layer while the ground plane (with slots) is implemented in lower-metal layers (metal 1 through metal 3 in this technology process). The antenna structure is based on an approach where the 10 Ω-cm silicon substrate is thinned to 75 μm. A 175 μm LCP layer with the patch antenna is bonded to the substrate using an non-conductive adhesive layer. While the LCP substrate (thickness = 175 μm, dielectric constant = 3.1, loss tangent = 0.003) is relatively low-loss at mm-wave [85], the lossy

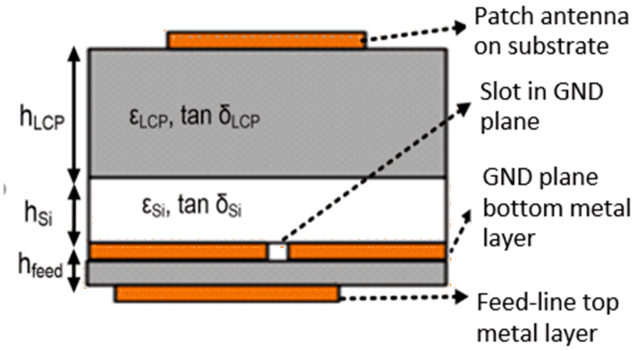


Figure 4.11: Antenna co-integration with high isolation dual-pol on-chip feeds and slot that are aperture-coupled to antenna on LCP through the backside of the die.

silicon substrate (resistivity of $\sim 10\,\Omega$-cm) leads to coupling losses. Thinning the silicon to $75\,\mu$m can reduce this efficiency degradation. Simulated antenna efficiency including the substrate and LCP loss is 49% for the RX and 64% for the TX (Fig. 4.14), with the difference due to the longer length of the RX feed network. Similarly, TX antenna achieves higher gain compared to RX antenna as shown in Fig. 4.15. Integrating the antenna feed with the circuits provides design freedom for impedance matching to the LNA and PA. For example, the TX antenna feed layers are matched to 29-j*28 Ω across 56 GHz to 67 GHz as shown in Fig. 4.16. Both TX and RX antenna achieves wideband impedance matching. The TX antenna has two feed-lines so that two identical PAs drive the same antenna at different feed point achieving lossless power combining in antenna far field to increase total TX EIRP and efficiency [95]. The simulated TX and RX radiation patterns are shown in Fig. 4.17 and Fig. 4.18.

Table 4.1: Dual-pol high isolation IC-antenna co-inegration design parameters.

Parameter	Value	Parameter	Value
W_{chip}	3 mm	W_{s_RX}	80 μm
L_{chip}	3 mm	L_{s_RX}	700 μm
W_{gnd}	2.6 mm	W_{s_TX}	100 μm
L_{gnd}	2.6 mm	L_{s_TX}	600 μm
W_p	1.05 mm	L_{stub_RX}	440 μm
L_p	1.05 mm	L_{stub_TX}	300 μm

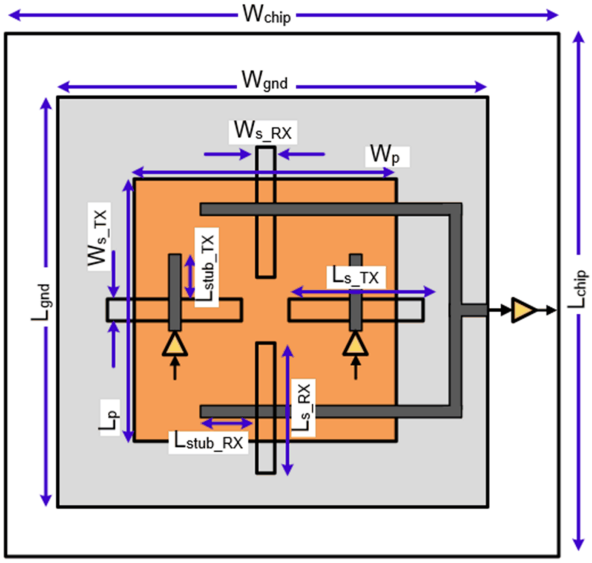


Figure 4.12: Dual-pol high isolation IC-antenna co-integration top view.

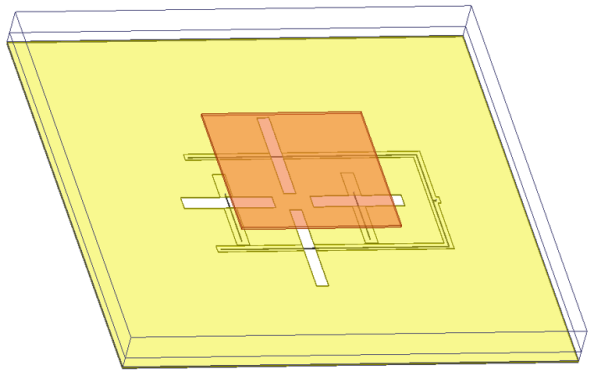


Figure 4.13: Dual-pol high isolation IC-antenna co-inegration 3D view.

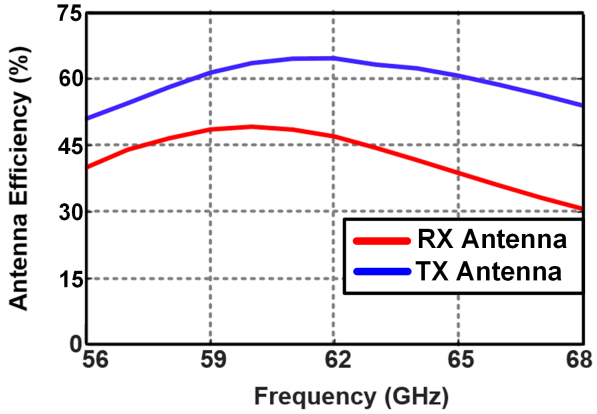


Figure 4.14: Simulated TX and RX antenna radiation efficiency including losses in the on-chip feed networks.

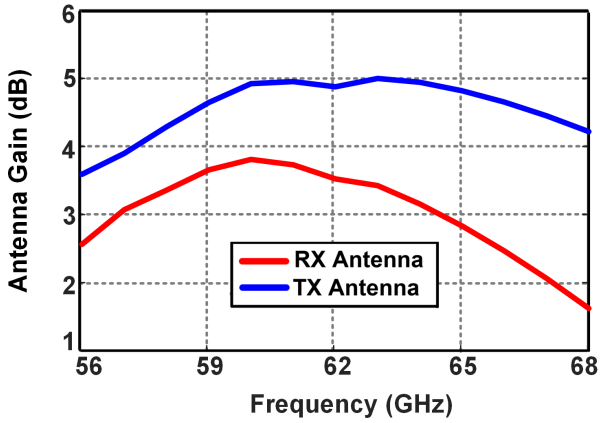


Figure 4.15: Simulated TX and RX antenna gain including losses in the on-chip feed networks.

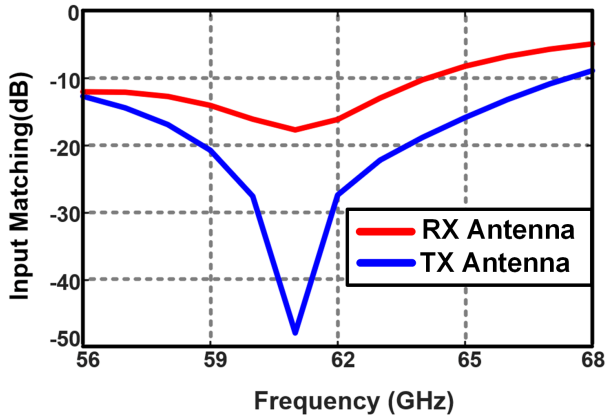


Figure 4.16: Simulated antenna input impedance matching for both TX and RX antenna.

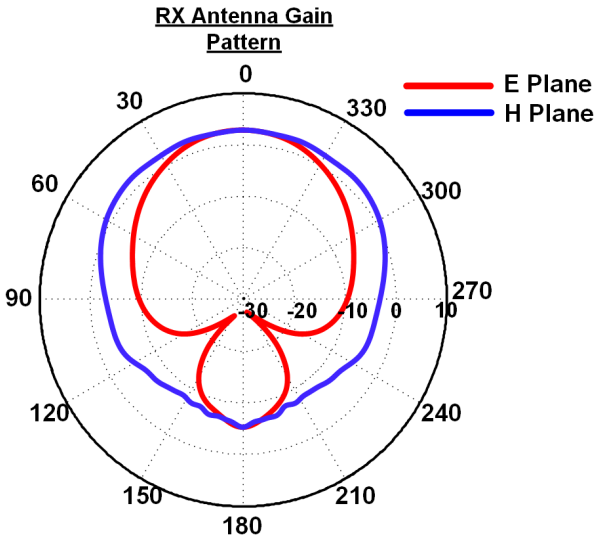


Figure 4.17: Simulated RX antenna radiation pattern.

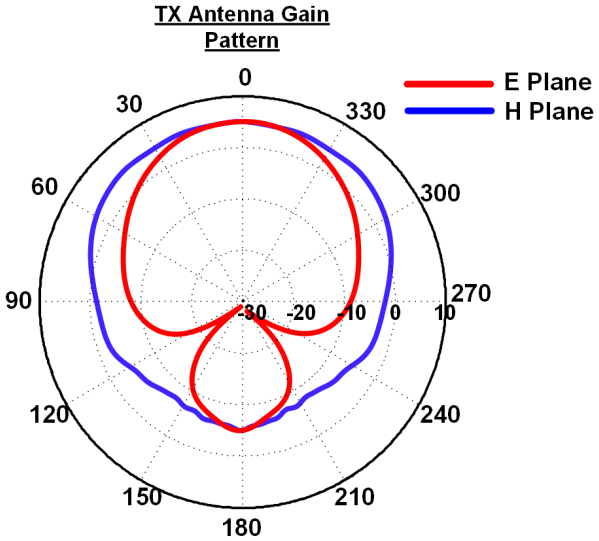


Figure 4.18: Simulated TX antenna radiation pattern.

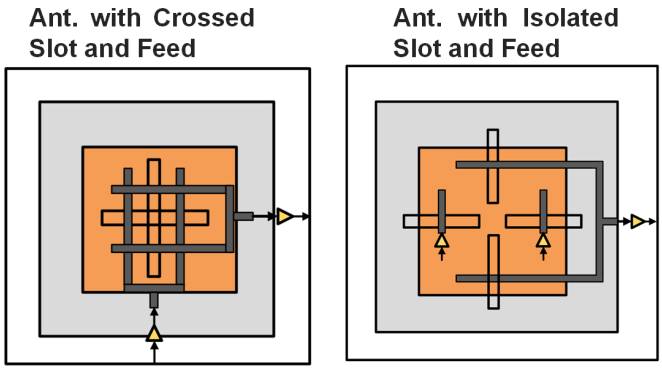


Figure 4.19: Design optimization compared to similar dual-pol antenna in Chapter 3.

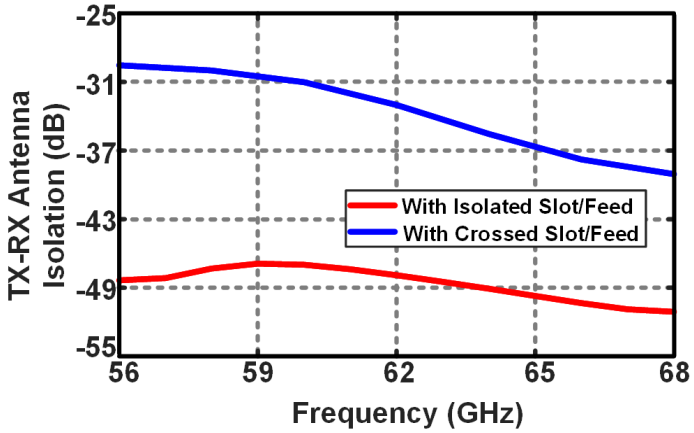


Figure 4.20: Increased dual-polarization isolation compared to similar dual-pol antenna in Chapter 3 leading to optimum design for STAR TRX.

Integrated approach also enables design optimization with precise metallization. Shown in Fig. 4.19 is the comparison of similar dual-pol antenna design in Chapter 3 [88] and this work. To achieve an optimum design of STAR TRX frontend, dual-pol isolation has to be maximized. This can be done by redesigning the feedline and slot in the on-chip ground plane. As shown in Fig. 4.20, by eliminating overlap between TX/RX feedlines and separate TX/RX coupling slot, the dual-pol isolation between TX and RX has been increased by more than 10 dB close to the final simulated isolation of

-50 dB across the 60 GHz.

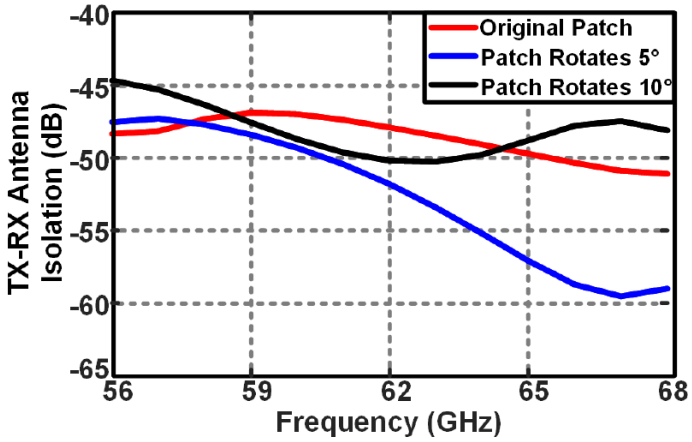


Figure 4.21: Simulated TX/RX antenna isolation sensitivity to rotation between patch antenna and on-chip slot.

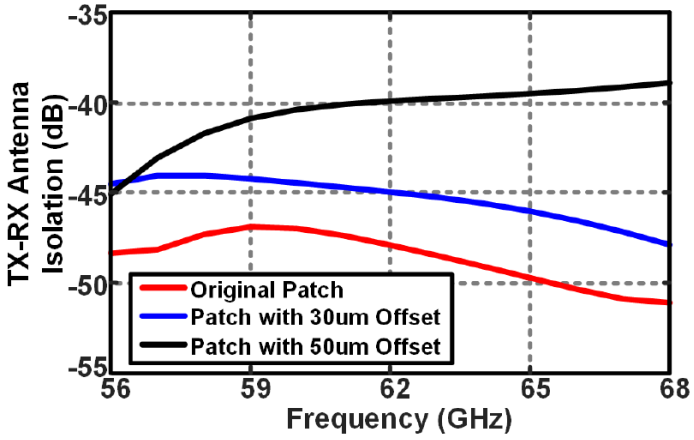


Figure 4.22: Simulated TX/RX antenna isolation sensitivity to offsets between center of patch antenna and center of on-chip slot.

Fabrication error tolerance is important for actual implementation. Sensitivity of dual-pol isolation to packaging errors is also considered. Fig. 4.21 shows the impact of the rotation of off-chip patch with respect to the on-chip slot. Rotation up to 10°

doesn't introduce substantial degradation of dual-pol isolation. Fig. 4.22 shows the effect of offset between the center of patch and the center of on-chip slot. Increasing offset does lead to worse dual-pol isolation, but up to 50 μm offset, the isolation is still acceptable (-40 dB).

A critical challenge is area-efficiency of the antenna structure due to the large antenna ground plane. Similar as discussed in Chapter 3, in the aperture-coupled structure, the feed layer is separated from the antenna layer by the ground plane. This allows circuits to be designed using transmission lines that are implemented with respect to the ground plane leading to a compact implementation.

4.4 60 GHz Transceiver Frontend with Self-Interference Cancellation

The 60GHz STAR TRX with SIC architecture based on the antenna co-integration is shown in Fig. 4.10. Two-step SIC has been implemented. TX SI is first suppressed by initial intrinsic antenna isolation provided by the dual-pol approach which is >40 dB in simulation. On top of that, part of TX power is coupled at PA output (~ -10 dB), going through a passive canceller and combined with RX output to cancel residual TX SI. The canceller includes variable gain and phase shift blocks to generate the required cancellation signal. The TX input drives two identical PAs through a Wilkinson power splitter. The two PAs generate identical in-phase TX output driving two on-chip antenna feedlines to achieve on-antenna power combing [95]. On the RX side, cancellation path is combined with leakage residual SI at LNA output through a Wilkinson combiner.

Fig. 4.23 shows the 3-stage LNA with 14 dB gain. The similar LNA mentioned in Chapter 3 is reused and modified (Shunt resonating transmission line length increased) to correct the simulation and measurement discrepancy as well as the peak gain frequency shift as discussed in Chapter 3. The comparison of gain between original Gen1 LNA and modified Gen2 LNA is shown in Fig. 4.34. A similar LNA achieves <8 dB NF based on stand-alone measurements as presented in Chapter 3. The 1^{st} stage(common emitter) consumes 2.1 mA from 1.8 V and 2^{nd} and 3^{rd} stage(cascode) consume 12.4 mA from 2.7 V.

Fig. 4.24 shows the TX design. A 3-stage class AB PA is used to generate ~8 dBm output power at 60 GHz with a cascode structure in each stage to provide higher reverse isolation at mm-wave. Transistor sizes are scaled up from input to output to ensure

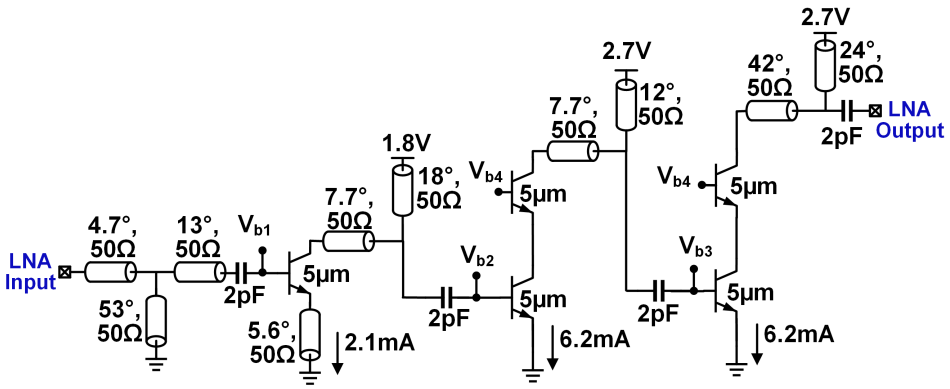


Figure 4.23: 60 GHz 3-stage Gen2 LNA with 14 dB gain.

sufficient linearity and output power. Transmission lines and on-chip metal-insulator-metal (MIM) capacitors are used for both output matching and inter-stage matching. The PA consumes 72 mA from 2.7 V and provides 20 dB gain, 8 dBm saturated output power with -20 dBm input referred P1dB.

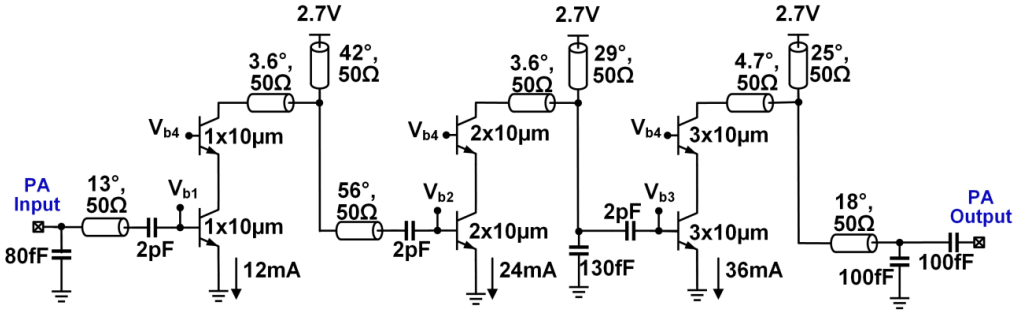


Figure 4.24: 60 GHz 3 stage class AB PA providing ∼8 dBm output power.

The TX output is driving TX antenna with partial signal coupled to the variable gain/phase cancellation stage using a custom capacitive coupler in the top two metal layers (with thickness 2.8 μm and 1.6 μm) as shown in Fig. 4.25 and Fig. 4.26. Parasitic capacitance between metal layers provides ∼-10 dB coupling ratio across 60 GHz frequency band as shown in Fig. 4.27.

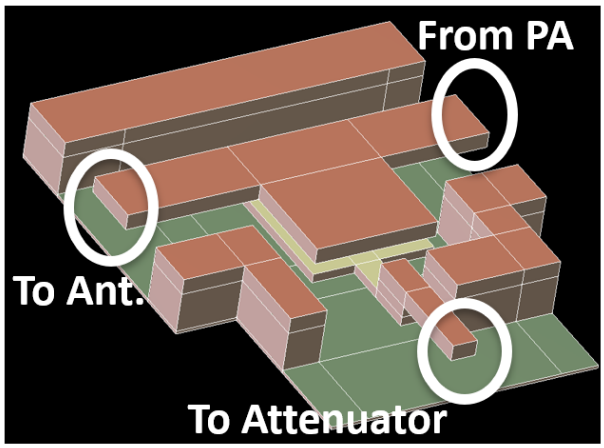


Figure 4.25: 60 GHz custom -10 dB capacitive coupler in the top two metal layers: 3D view.

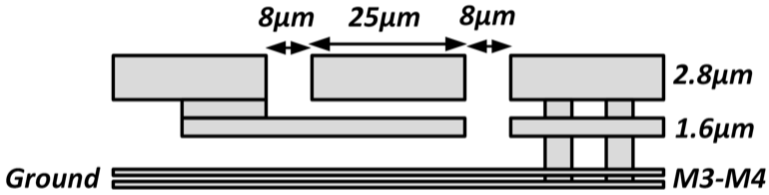


Figure 4.26: 60 GHz custom -10 dB capacitive coupler in the top two metal layers: Cross section.

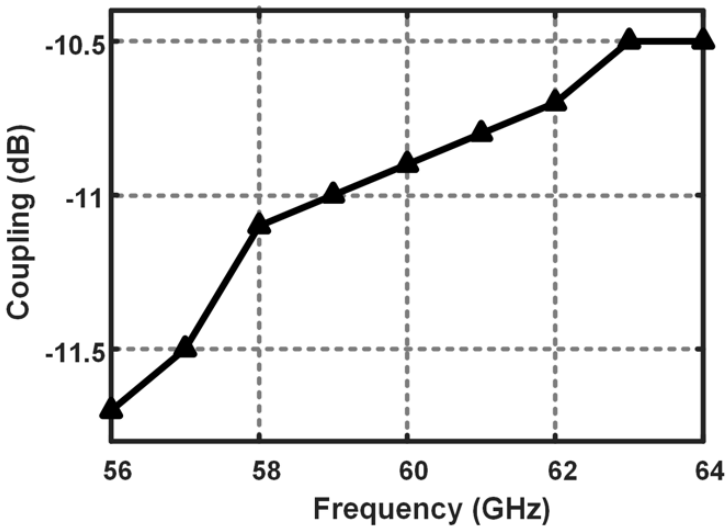


Figure 4.27: Simulated 60 GHz custom capacitive coupler coupling ratio across frequency.

The coupler drives a reflection-type attenuator (RTA) whose phase shift, $\Delta\Phi$, depends upon the termination impedance, Z_T:

$$\Delta\Phi = -90^\circ + \angle\Gamma \text{ where } \Gamma = \frac{Z_T - Z_0}{Z_T + Z_0}. \tag{4.1}$$

The termination impedance is varied using load transistor in Fig. 4.28. A stand alone attenuator with simple load transistor has also been used with simulated attenuation from -3 dB to -17 dB at 60 GHz as shown in Fig. 4.29. The RTA is used to provide 0° or 180° discrete phase shift based on $Z_T > Z_0$ or $Z_T < Z_0$. The design of load transistor involves the trade-off of R_{ON} and R_{OFF}. When transistor size increases, smaller R_{ON} leads to a more ideal short, which is desirable for small insertion loss for 180° phase generation (180° at load terminal, actual phase shift provided by RTA is 90°). However, large transistor size also leads to lower R_{OFF}, leading to worse open which is sub-optimum for insertion loss for 0° phase generation (0° phase at load terminal, actual phase shift provided by RTA is -90°). Device sizes are selected based on simulations across R_{ON} and R_{OFF} for targeted 180° phase shift and minimum insertion loss variation.

The output of the attenuator drives a passive reflection-type phase shifter (RTPS) (Fig. 4.30). The passive RTPS uses a two-capacitor load structure designed using the

approach in [96] to enable low-loss variation while achieving the targeted 180° phase shift range. In simulation, the RTPS provides >180° variable shift with 7 dB ± 1 dB insertion loss as shown in Fig. 4.31.

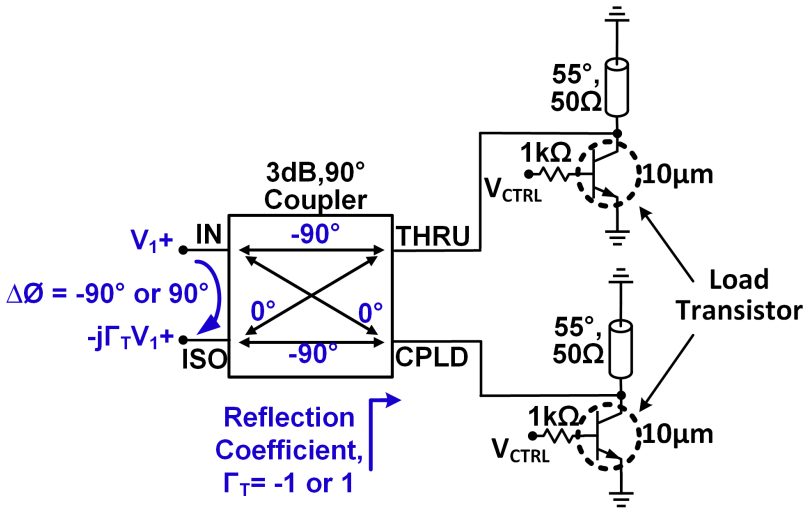


Figure 4.28: 60 GHz RTA: Coupler terminated by tunable resistor for $0/180^o$ discrete phase shift.

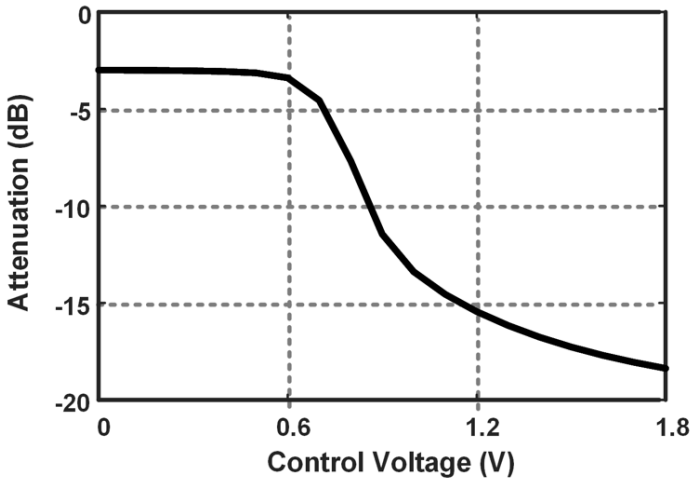


Figure 4.29: Simulated variable attenuation provided by stand alone load-transistor based attenuator at 60 GHz.

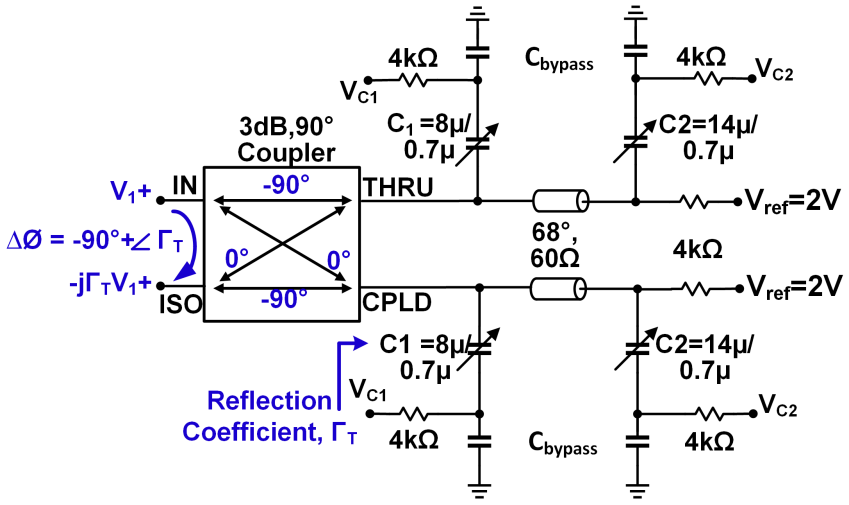


Figure 4.30: 60 GHz RTPS: Coupler with reflective load provides $>180^o$ continuous phase shift with low gain variation.

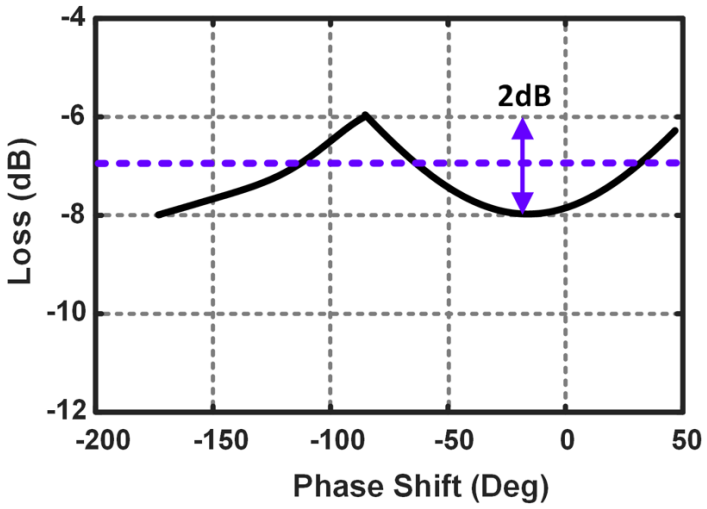


Figure 4.31: Simulated 60 GHz RTPS insertion loss varies from -6dB to -8dB across $>180^o$ phase shift range.

4.5 Measurements and Performance

The IC is implemented in the TowerJazz 0.18 μm SiGe process with 2.8 μm top thick metal layers. As described in Chapter. 3, the ground plane is reused by transmission lines and active circuits to achieve the compact layout as shown in Fig. 4.32 with die size 3 mm × 3 mm. Probe-based measurements are performed to verify performance of Gen2 LNA, attenuator and phase shifter.

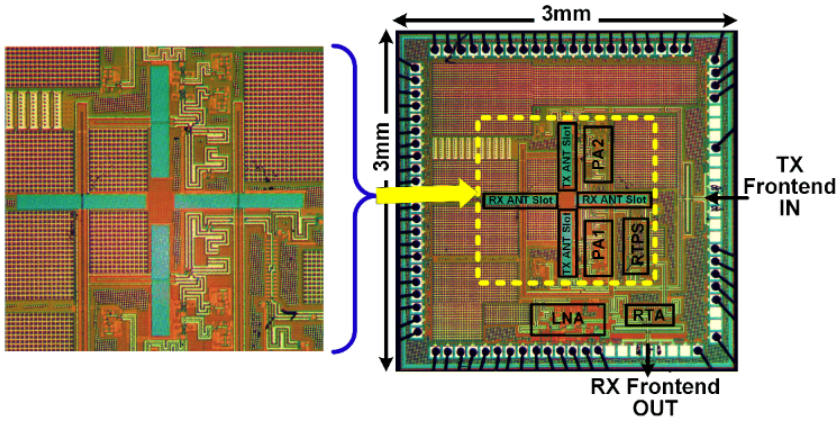


Figure 4.32: 60 GHz STAR TRX die photo showing ground plane extensively reused by active circuits implemented in TowerJazz SiGe process technology.

As discussed in Section 4.4, Gen2 LNA is designed based on similar LNA in Chapter 3 with one section of transmission modified to correct the peak gain frequency shift and discrepancy between simulation and measurement as shown in Fig. 4.33 with gain comparison shown in Fig. 4.34. The Gen2 LNA input and output matching and noise figure are similar to Gen1 LNA as presented in Chapter 3, where <8 dB NF has been achieved while consuming 12.4 mA from 2.7 V and 2.1 mA from 1.8 V.

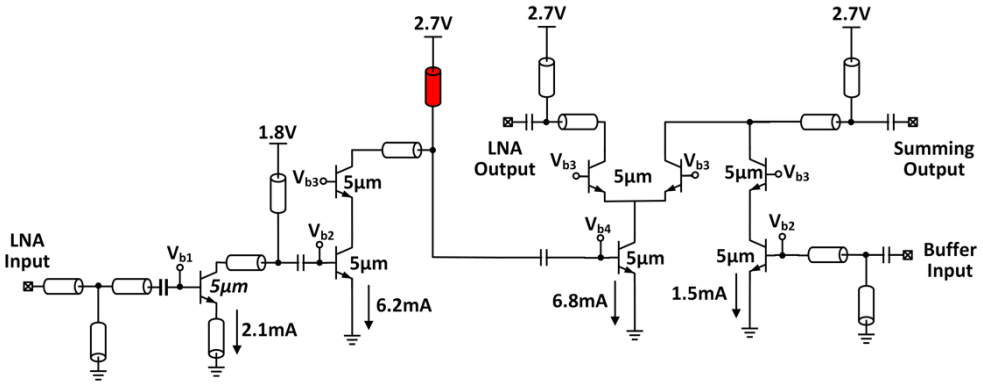


Figure 4.33: Gen2 LNA is designed by modifying one section of transmission line (highlighted in red) of Gen1 LNA.

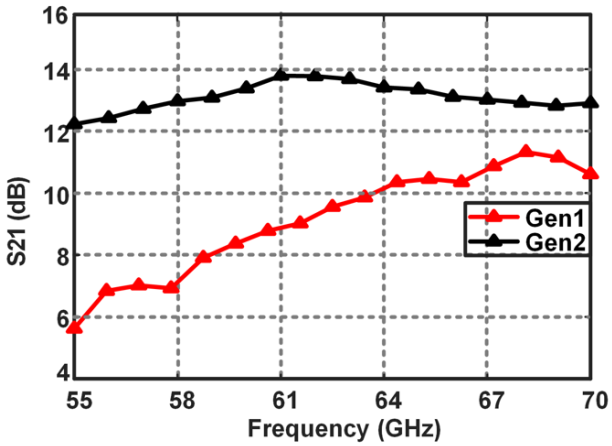


Figure 4.34: Measured gain comparison between Gen1 LNA and Gen2 LNA.

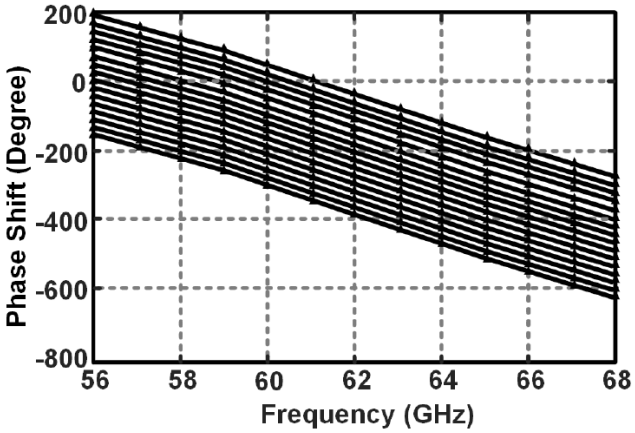


Figure 4.35: Measured canceler phase shift demonstrating 360^o phase shift across frequency.

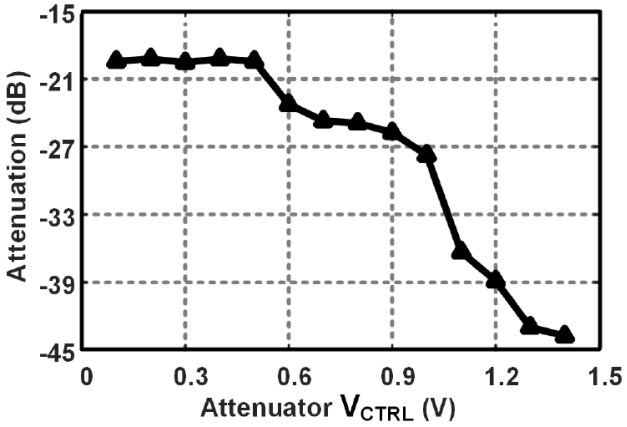


Figure 4.36: Measured variable attenuation from stand alone attenuator across different control voltage.

The performance of the passive cancellation path is also measured through probe testing. Shown in Fig. 4.35 is the measured phase shift across frequency. The passive phase shifter including RTPS and RTA provides full 360° phase shift where continuous 0 to 180° from RTPS and discrete 0/180° from RTA. On-chip 60 GHz attenuator performance is shown in Fig. 4.36 where >20 dB attenuation range has been achieved.

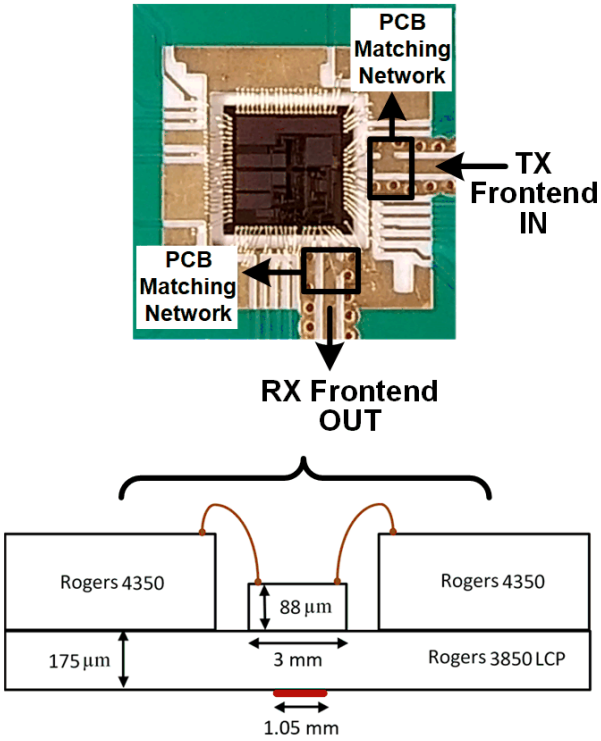


Figure 4.37: Dual-pol IC-antenna co-integration packaging with patch antenna integrated on a Rogers 3850 LCP substrate and on-PCB matching network on Rogers 4350 material.

The IC is packaged with a patch antenna integrated on a Rogers 3850 LCP substrate as shown in Fig. 4.37. Low-loss Rogers 4350 material is used for on-PCB mm-wave TX frontend input and RX frondend output routing. On-PCB transmission-line matching networks are used for mm-wave impedance matching enabling wireless measurement. The TX performance is measured wirelessly as shown in Fig. 4.38, where TX is driven by a continuous wave (CW) signal from signal generator. To characterize the TX performance, a standard horn antenna is used to receive the TX output power followed by downconversion and measured by spectrum analyzer. Saturated EIRP (including both PAs) across frequency after de-embedding 60GHz path loss is shown in Fig. 4.39, where maximum EIRP (∼13 dBm) can be achieved at 65 GHz. Measured EIRP across input power at 65 GHz is shown in Fig. 4.40, where OP_{1dB} is about 4 dBm when P_{in} is -20 dBm.

The small-signal PA gain is shown in Fig. 4.41 where maximum 20 dB gain is achieved at 65 GHz.

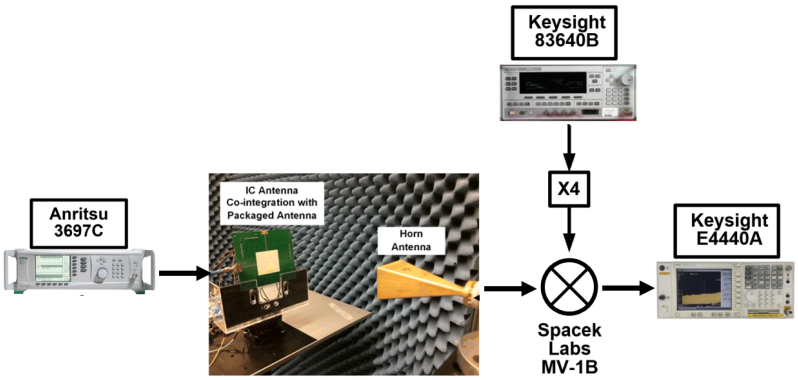


Figure 4.38: Wireless measurement setup to characterize TX performance.

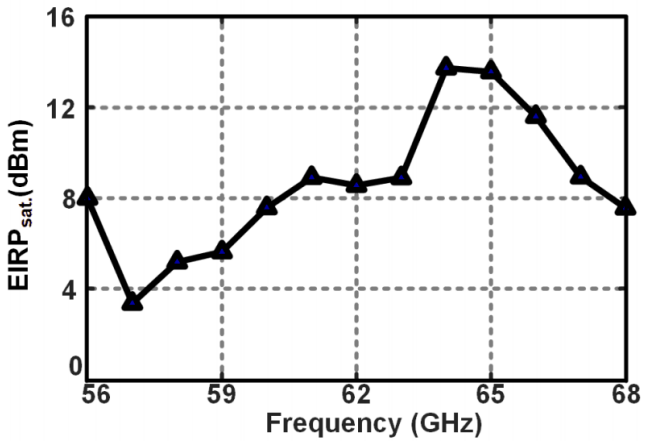


Figure 4.39: Measured saturated EIRP across frequency after de-embedding 60GHz path loss.

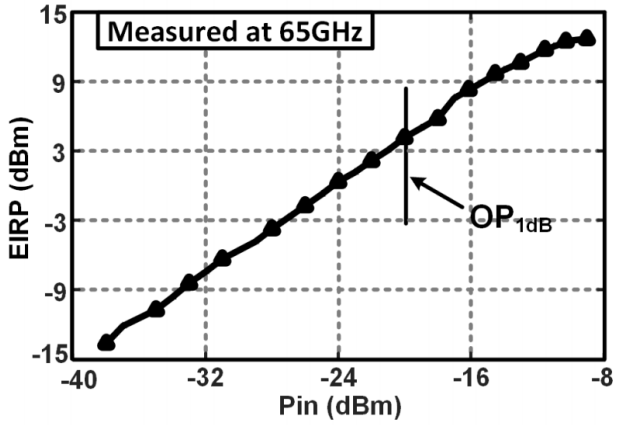


Figure 4.40: Measured EIRP across input power at 65 GHz.

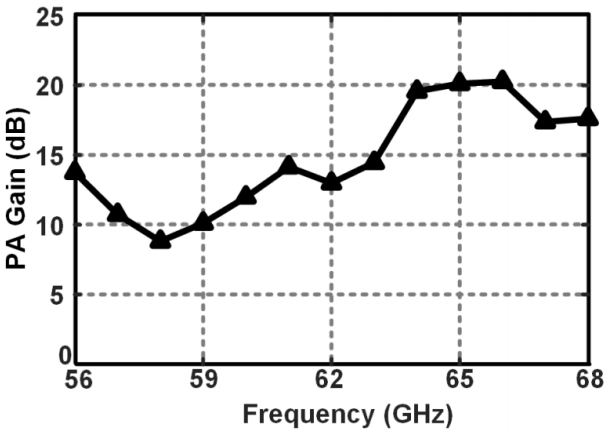


Figure 4.41: Measured small-signal PA gain across frequency.

Given the degrees of freedom in the phase shifter and the the attenuator, Fig. 4.42 plots canceller insertion loss and phase shift for a range of > 20 dB and full 360° demonstrating that the attenuator path can be configured to match leakage signal amplitude and phase.

SIC measurements were carried out wirelessly while including a blocker to demonstrate the impact of reflections using the setup shown in Fig. 4.43 where TX is driven

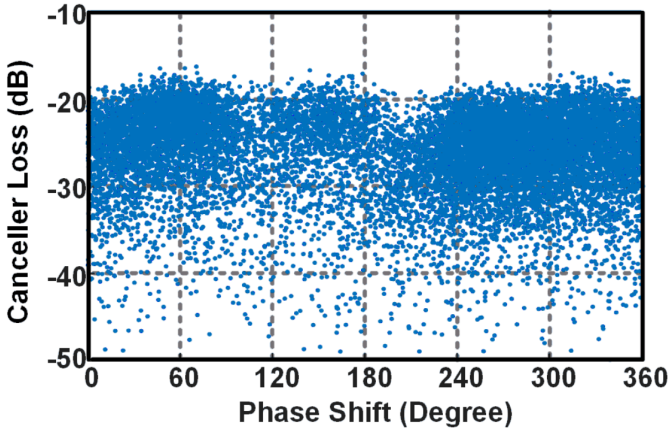


Figure 4.42: Measured canceller loss versus phase shift demonstrating >20 dB attenuation and 360° phase shift range.

by a CW signal from signal generator and SI at LNA output is downconverted and measured using Keysight spectrum analyzer. Measurements were carried out at 3 dBm EIRP. Measured isolation between the feeds (antenna alone) is shown in Fig. 4.44 demonstrating 34 dB SIC at 60 GHz (27 dB to 38 dB across frequency band). The passive canceller provides additional SIC, leading to total average SIC of >40 dB for 1.07 GHz BW at 60 GHz. The IC is compared to state-of-the-art in Table. 4.2, demonstrating >40 dB SIC with bulk silicon antenna co-integration and broadside radiation.

4.6 Conclusion

A 60 GHz simultaneous transmit and receive TRX front-end with co-integrated antennas to achieve efficient polarization-duplex mm-wave front-end is presented. The proposed antenna approach provides broadside radiation through the substrate and is compatible with low-res silicon substrates. On-chip slot structures are driven by PAs with antenna power combining for increased output power and efficiency. The orthogonal-polarization feeds provide >40 dB simulated isolation between TX and RX around 60 GHz. Subsequent TX SIC at the LNA output is achieved with part of the TX signal coupled to a cancellation path, includes a attenuator, a RTA and a RTPS that provides >20 dB gain variation and full 360° variable phase shift. Overall, total

average SIC >40 dB is achieved for 1.07 GHz RF bandwidth at 60 GHz in the presence of a reflector.

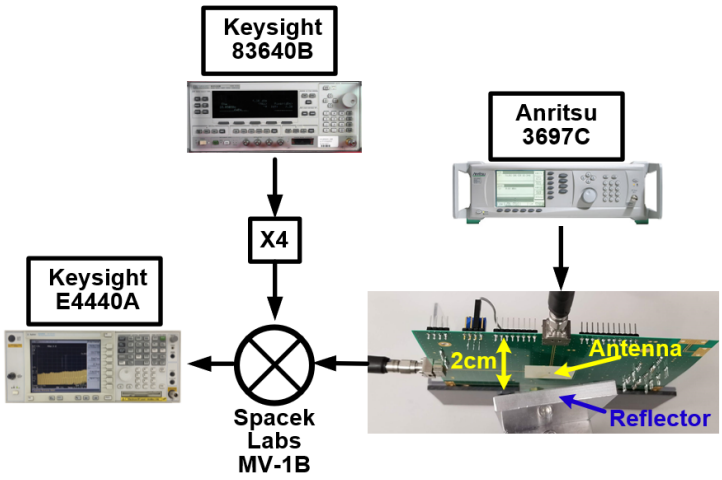


Figure 4.43: Wireless measurement setup with reflector to demonstrate TX SIC.

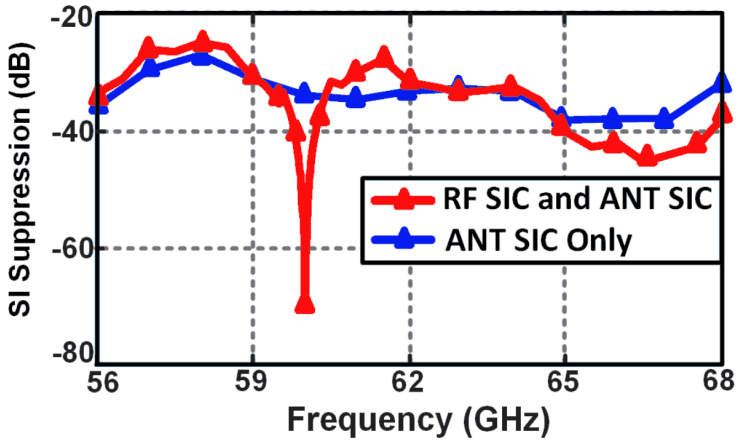


Figure 4.44: SIC measurements demonstrating 34 dB antenna SIC and ~70 dB system SIC.

Table 4.2: Comparision to state-of-the-art mm-wave pol-duplex TRX

	This Work	[15]	[14]
Architecture	One Ant. Footprint	One Ant. Footprint	Dual TX/RX Ant. on PCB
Technology	0.18 μm SiGe BiCMOS with 10 Ω-cm sub. res.	45nm CMOS SOI with high res. sub.	45nm CMOS SOI
Ant. Type	Aperture-coupled Patch Ant.	Slot Loop Ant. on Chip	Slot Loop Ant. on PCB
Chip Area	3 mm $\times$ 3 mm	2.7 mm $\times$ 2.7 mm	1.3 mm $\times$ 3.4 mm (TRX Chip) 2.4 mm $\times$ 3.4 mm (PCB Ant.)
Frequency Range	56–68 GHz	60–75 GHz	57–66 GHz
Ant. SIC	27–38 dB	>35 dB	N/A
Ant. + RF SIC	70 dB	>60 dB	>65 dB
Canceller DC Power	0	0	44 mW
Ant. SIC Loss	0	0	1.1 dB (TX)/0.52 dB (RX)
Ant. Radiation Pattern	Broadside	Endfire	Broadside
Radiation Efficiency	64% (TX)/49% (RX)	91%	N/A

Chapter 5: Conclusion

Millimeter-wave(mm-wave) wireless links are attractive for applications where high data rates and low latency are required. Extensive academic and commercial research and development has led to demonstrations of large-scale mm-wave arrays for practical commercial communication and imaging applications. An efficient IC-antenna interface has been a major barrier for system-on-chip (SoC) applications. Antenna-in-package (AiP) has been explored to achieve high radiation efficiency and bandwidth at the cost of high fabrication complexity and high interconnect loss. On-chip-antenna shows low efficiency since silicon substrate is not well suited for antenna radiation. The proposed IC-antenna co-integration shows AiP-comparable system efficiency (40%) with less sensitivity to metal-fill rules, greater scalability, lower fabrication cost and complexity demonstrating an efficient IC-antenna interface well suited for large element arrays.

For mm-wave short-range imaging/communication phased arrays and polarization-diversity based MIMO links, cross-polarization leakage degrades system performance. Based on the efficient IC-antenna co-integration approach, dual-polarization antenna feeds co-integrated with IC have been implemented to demonstrate concurrent dual-polarization reception. With intrinsic $\sim$-10 dB cross-polarization and active 30 dB cross-polarization cancellation, <-40 dB cross-polarization ratio has been achieved. Antenna ground plane has also been extensively reused by active circuity and transmission lines leading to a minimized silicon area.

Millimeter-wave shadowing and self-interference has been a major challenge for communication and radar applications. On-chip-antenna based simultaneous transmit and receive TRX front-end solves the integration and scalability problem but is not suitable for bulk CMOS process and its radiation pattern is also not desirable for array packaging. The efficient dual-polarization IC-antenna co-integration approach has been extended to polarization-duplex transceiver front-end for mm-wave simultaneous transmit and receive TRX. Design of the dual-polarization antenna has been optimized for high intrinsic isolation. With additional passive cancellation path, total average SIC >40 dB is achieved for 1.07 GHz RF bandwidth at 60 GHz in the presence of a reflector demonstrating an

efficient simultaneous transmit and receive TRX front-end with polarization-duplex at mm-wave. Compatibility with low-resistivity bulk silicon substrate and broadside radiation pattern makes the proposed approach an excellent candidate for mm-wave relays to extend communication link operation range and for mm-wave radars to operate in a simultaneous transmit and receive manner.

Future work include stacked patches for bandwidth improvement, better alignment between patch antenna and on-chip slot for lower cross-polarization ratio and investigating better antenna structures for higher polarization isolation. In addition, future research must address thermal dissipation issues associated with addition of a substrate to the backside of the IC. The proposed IC-antenna co-integration approach can be used for large-scale mm-wave phased-arrays and MIMO to achieve higher system efficiency with reduced cost and fabrication complexity.

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