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We present a new circuit design for adaptive offset cancellation in a fully differential 2.4 GHz CMOS direct conversion mixer. Our circuit structure is a modification of a Gilbert cell mixer in which offsets are cancelled by injecting cancellation currents into the legs of the mixer by dynamically varying the bias on the active loads. We present analysis and simulation results of our mixer with offsets present. Offsets create non-linearities in any circuit by differentially shifting the small-signal bias point of a matched pair; forcing once symmetrical transistors to operate in different bias regions and create second order distortion. We focus our design to minimize second order distortion while simultaneously canceling the large offsets found in direct conversion receivers. Simulation results for the mixer canceling a wide range of offsets are included. Our mixer has a gain of 6.4dB, an IIP3 of 17dBm and a noise figure of 17dB as simulated in a .5μm HP Mosis CMOS process.

A Direct-Conversion Offset-Cancellation Mixer in 2.4GHz CMOS

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

A Direct-Conversion Offset-Cancellation Mixer in 2.4GHz CMOS

INTRODUCTION

In the continuing effort to minimize wireless transceiver size and power consumption great hopes exist for the eventual shift of receiver architectures from heterodyne to direct conversion. The primary advantage of direct conversion over heterodyne is the improved amenability to monolithic integration of the entire receiver system. There are two fundamental problems with full integration of heterodyne receivers. First, heterodyne receivers require a discrete component RF image-reject filter. Second, it is difficult to realize IF channel select filters with the low-Q available in CMOS - the technology seen as the path to affordable integration. Both problems are circumvented by the direct conversion implementation, the system shown in Fig. 1. Direct conversion is highly touted to be the low power receiver solution [1, 2]. Channel select filtering is performed in the base-band with high-Q switched-capacitor low-pass filters. The entire CMOS direct conversion transceiver can be implemented alongside the base-band DSP in a single inexpensive microchip. However, direct conversion introduces its own set of problems.

The major impediment in using direct conversion is the DC offset problem [1-3]. Insufficient on-chip isolation allows strong LO signals to couple through the substrate to the antenna, low noise amplifier, and the RF port of the mixer. The

coupled LO signals are amplified as they follow the signal path to the mixer where they 'self mix,' causing energy to be superimposed onto the down-converted signal in the form of a DC offset. Coupling of the LO to the LNA and RF port of the mixer cause static or fixed offsets. When the LO couples to the antenna, radiates and reflects off moving objects back to the antenna a time varying or dynamic offset is created [1]. The DC offsets created at the output port of the mixer, are often 20 to 30 dB larger than the desired signal levels. If not removed these offsets will saturate downstream gain stages desensitizing the receiver and destroying performance. It is the goal of this work to address the removal of these offsets to promote the Direct Conversion architecture.

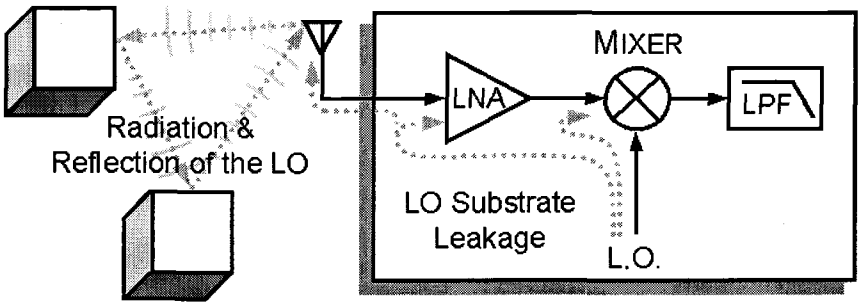


Figure 1 Dynamic and static sources of DC Offset

LITERATURE REVIEW

The benefits and challenges of direct conversion receivers (DCRs') are discussed by Abidi [2]. He compares the super heterodyne and homodyne receiver structures, pointing out the strengths and weaknesses of each. The large number of off-chip components necessary in super heterodyne receivers limit its amenability to monolithic integration and increase its power consumption and cost. He shows how the Weaver architecture can be used for on-chip super heterodyne implementations of image reject filters but is limited by phase and gain mismatches. His excellent figures show that for typical 1^{o} quadrature phase error and 1dB gain mismatch, 30dB is the upper bound for image rejection. He also shows that these same mismatches only slightly affect the SNR in a homodyne implementation, which does not need image rejection. High order active filters operating in the baseband are also shown to consume significantly less power than their IF counterparts with the same selectivity. Other papers reinforce the comparisons between the direct conversion and the super heterodyne receiver architectures [1,3,30] and summarize the super heterodyne receiver's weaknesses of power consumption and the need for high-Q passives on-chip.

To minimize the devastating effects of even-order distortion, Abidi [2] cites the necessity for differential circuitry. Although differentially balanced front-ends typically draw more current, the system power savings of a DCR exceeds the power consumed to otherwise reduce the second-order distortion. Alternatively,

Razavi [1,30], states that the noise contributed by a balun preceding the LNA, outweighs the even-order performance of balanced operation. Since objectives can differ, it appears that in all but the most sensitive of wireless standards, balanced operation is preferred.

DCRs need more linearity than super heterodyne systems [2]. This is clear from a discussion of Blocking Dynamic Range (BDR) which is the range over which a weak signal is passed without blocking (i.e. spreading) of a strong co-channel interferer. Razavvi [1] gives excellent examples of BDR budget planning and compares potential receiver chains with the amplification in various locations. It becomes obvious from his in-depth analysis, that the amount of amplification available after the mixer is specific to the spectral mask of each individual wireless standard. If large co-channel interferers exist little or no amplification can be had and the noise figure of the channel select filter will begin to dominate the system sensitivity. If the spectral mask prohibits adjacent channel interferers, then additional gain following the mixer will easily reduce the filter's contribution to system noise figure.

Time variant offset are discussed in each paper [1-3, 30]. Abidi focuses on FSK systems and their compatibility to wide band notching. For modulation schemes with spectral energy centered at DC, Abidi suggests digital memory cancellation that is a method specific to TDMA where test sequences may be used to cancel offsets during rest cycles. Razavi [1, 30] extends the analysis by including examples of typical leakage levels and showing how the receiver

amplification chain becomes limited by unreduced offsets. In [30], he shows how kT/C noise limits the notching method by creating a need for large capacitors. Each paper on DCRs mentions the time varying offsets produced from changes in a receivers location and orientation. In the next section several published offset cancellation methods are reviewed.

Offset Cancellation Methods

The first on-chip offset cancellation was performed by Vance [31]. His wide-band FSK system with a low data rate easily tolerated off-chip ac coupling without significant loss in BER. Where spectral efficiency is not a concern this simple method has proven quite effective and is utilized in millions of pagers today. Although modern processing costs limit the feasibility of off-chip components, many still utilize this solution [8-13].

A second place where ac coupling is a reasonable solution to offset cancellation is in wide spread spectrum applications. In these situations the notch may remove less than 0.1% of the band, having little effect on the BER. However, as Razavi pointed out in [30], kT/C noise could force the notching so far downstream that dynamic range is still compromised. Most of the following papers employ some form of notch above 1kHz where either FSK or spread spectrum modulation are used.

In Abidi, *et al.* [9], an 80kHz corner is used for the low pass filter. The offset is cancelled through a feedback loop containing a low pass filter with an off-chip 140μF capacitor. In addition to the undesirable off-chip component, the location of the cancellation is wrought with trouble. Following the mixer where offsets are several tens of millivolts [1], the passband experiences 38dB of gain. This gain raises the few tens of millivolts into a few volts which will easily rail out a 3 volt system. At this point the system is already saturated and feeding back the

offset signal is pointless. Although a frequently cited work, these crucial mistakes would prohibit this approach from ever being used in production.

Hull, *et al.* [13], also wait to cancel offsets until too late in the system (the final amplification stage). A 22kHz high pass corner is used in a cancellation feedback loop. Off-chip filters and high pass capacitors are also used.

Cho, *et al.* [10] distribute offset cancellation in stages. The first offset cancellation stage does follow the anti-alias filter, but the mixer and anti-alias filter gain are not reported so it is unclear how much dynamic range, if any, is lost. A second offset cancellation stage occurs after the channel select filter to provide stronger attenuation of the offset. Dynamic offsets are tracked and cancelled digitally in the AGC which utilizes peak detectors. The authors have taken precaution to cancel offsets and have a potentially feasible approach.

In Wilson, *et al.* [8], a 150Hz high pass corner is created with a large 330pF on-chip capacitor for use in an FSK system with 15kHz bandwidth. The notch filter is cascaded several times throughout the amplifier chain, which provides 75dB of attenuation. Wilson does not report individual stage gains, so no BDR analysis can be performed.

Pärssinen, *et al.* [11, 12] present a wide band CDMA direct conversion receiver. External 220nF capacitors form a 2kHz high pass corner, which is used to drive an offset feedback loop around the base-band processing. The mixer is reported capable of handling up to 300mV offsets. The mixer IIP2 is reported to be 60dBm; however, no data is reported for IIP2 in the presence of offset handling.

Razavi [14], presents an offset cancellation DCR which notches the first 200kHz from a wide 11MHz spread QPSK channel. The new approach in this design is that it is the only complete DCR without off-chip components. An extremely high impedance node is used with a 10pF on-chip capacitor to perform AC coupling. The noise figure of the high pass filter presented is 67dB. To overcome such a large value at least 40dB of gain is needed between the mixer and the high pass filter, which Razavi does include. This of course results in the situation of Abidi [9] where the 20mVpk-pk mixer output grows to 2Volts and clips subsequent gain stages. Thus this work may be difficult to implement in a realistic system.

Several methods of offset cancellation have been reviewed. Of those reviewed, all except Razavi [14] relied on production costly off-chip components. Although some of the works presented are potentially reasonable offset cancellation schemes for low integration [10, 12], further investigation is still needed to find a low cost on-chip solution. Since no paper included IIP2 performance in the presence of typical offsets, this must also be considered. Additional papers [15-19] present methods based on training sequences for TDMA offset cancellation. Since these are only focused on training sequences which remove static offsets they are not reviewed herein. In the next section, several possible CMOS mixer structures are reviewed from the literature.

CMOS Mixer Review

Maas [7] gives an excellent overview of various mixer topologies. He points out that active mixers have the advantage of conversion gain, and compatibility with monolithic processes. Their disadvantage comes in their process variability and their need for baluns in balanced circuits.

He reviews single device mixers and clearly explains the roots of distortion and how suck-outs isolate the ports. The need for an LO-RF diplexer and IF filters limit the use of these mixers in monolithic applications. However, dual gate mixers, which operate similarly, also modulate G_m, and are a frequently used structure [4,34]. Dual gate mixers do not require a diplexer or baluns and have good LO to RF isolation. However, they have mediocre noise and distortion performance and are especially prone to substrate noise coupling. Maas suggests that these mixers are very useful for low-cost integrated circuits in applicatoins where performance is not critical.

The doubly balanced MOSFET mixer, or more commonly "modified Gilbert cell" is the best performing active mixer according to Maas. It has excellent IIP3, and good noise performance. The switching transistors are fully commutated by the LO making them much less sensitive to LO-AM noise. The LO power consumption is the highest among the active mixers and the balanced nature doubles the current used. The necessity of baluns could be a large drawback when a single ended antenna is used. However, when other system clocks share the same substrate, it is worth having the differential configuration to reduce common

mode clock coupling. Apart from substrate coupling the single balance FET mixer has similar performance without the additional noise added by baluns.

In Sullivan, *et al.* [4], both a balanced dual gate mixer and a Gilbert cell mixer are constructed in CMOS, which makes for good comparison. The authors focus on minimizing LO drive and resultantly trade-off other mixer performance measures. The paper contains numerous curves comparing noise figure and gain to LO power and current consumption.

Rudell, *et al.* [35], give a clear explaination of their construction of a modified CMOS Gilbert cell. Their architecture features a cascode transconductance cells. This cascoding improves LO-RF isolation by reducing capacitive coupling. This mixer also shows CMFB circuitry and gain control. Excellent analysis of LO power versus switching loss is presented.

Rofougaran, *et al.* [5], present a modified CMOS Gilbert cell without a tail current mirror. Maas [7] suggests this approach for Gilbert cells operating at more than several GHz as a simplification to the capacitively mismatched layouts typical at these speeds. Analysis of the numbers presented for this mixer shows where unclear. When using the same MOSIS process models we were unable to replicate their simulation results.

Crols *et al.* [36], present a CMOS mixer with longer gate line lengths. The structure they use consists of four switches modulating the input to an amplifier. The switches, which operate in the MOS linear (triode) region, can be highly overdriven and thus made small. This produces a very fast, extremely linear

mixer. The results Crols presents are an IP3 of 45.2dBm, gain of 18dB and a noise figure of 32dB. This noise figure is of course, unacceptably high for most applications. This structure does not seem appropriate for the low noise needed in a front-end mixer.

Karanicolas [32], modifies the traditional single balanced FET mixer to achieve a very efficient low power structure. The included bias circuitry is interesting for reference. The entire paper is based on the current re-use method, which replaces a traditional differential pair and active loads with both NMOS and PMOS differential pairs pushing against each other. The difference can also be seen in the conversion of a source follower to an inverter. With the current re-use method applied to a mixer both N and P type transconductors and switches are used. Even though not mentioned by the author, the difficulty with this approach is matching. Trying to balance N and P type switches to simultaneously change states across process is difficult. Distortion introduced by irregular switching is likely to be devastating. Few results for this mixer are given.

Razavi [37], uses a single balanced FET mixer. As pointed out earlier, this structure has the system advantage of not needing baluns to convert a single ended antenna to a differential LNA. Razavi does add some useful features to his mixer. He capacitivley couples the RF signal from the common source to the differential switches. To establish bias currents and reduce current noise in the switches he bypasses a current mirror with an inductor. Capacitive bypassing is also used to limit out of band gain. This paper provides results for a single balance structure,

although the results are embedded within extra amplification stages preceding and following the actual mixer.

After reviewing all of these mixer structures, we decided that for low cost CMOS DCR's, where integration is important and operation with on-chip digital circuitry must be tolerated, a modified Gilbert cell will have the best performance.

CMOS Low Noise Amplifiers

Recent work toward the goal of integration has driven research in CMOS LNA design [21, 32, 33]. As with the more traditional bipolar and GaAs analog processes, CMOS LNA design addresses competing goals of: minimizing noise figure, maintaining high gain with reasonable linearity, and matching input impedance [21]. This section is far from exhaustive but helps to define typical performance metrics for an LNA which might preceed our mixer in a hypothetical low-cost system.

To maintain low noise figure while achieving a minimal power consumption of 20mW, Karanicolas [32] uses a current re-use approach. The basic building block of current re-use is an NMOS and PMOS pair with common drain connected in an inverter configuration. To maintain a well centered voltage bias, the output of each inverter is fed back through a single stage transconductance amplifier to a current mirror. The feedback structure operates on very little power and has a slow frequency response so as to avoid the feedback loop tracking the RF signal. The reduction of power, one half, due to the use of a pair of transistors as active loads achieves an LNA with good performance; Gain 15.6dB, NF 2.8dB, IIP3 -3.2dBm

and power dissipation 20mW from a 2.7V supply. Not discussed by the author are the potential production difficulties caused by process variation of threshold voltage which seem critical to their architecture.

Shaeffer & Lee [21] do an excellent job reviewing various LNA circuit structures used in all processes. They first review common base LNA's which achieve their 50 Ohm impedance by setting the $1/g_m$ value, their input impedance. They show this topology to have a lower bound noise figure of 2.2dB in CMOS. Second, they present analysis of a shunt resistor feedback topology. They shows that wide-band operation come at the expense of considerable power consumption, more than 115mW. For high performance and a low noise figure, less than 2dB NF, the optimal structure is shown to be a common-source using inductive degeneration. This structure is implemented but the noise contributed by the low-Q of the CMOS inductors causes the noise figure to be 3.5dB. Additionally, a gain of 22dB, and IIP3 of -9.3dBm are achieved for a 1.5V supply delivering 30mW.

It is reasonable to assume that with submicron CMOS technology, a monolithic LNA can be constructed to at least meet moderate sensitivity demands. Low inductor Q, as well as additional CMOS noise sources such as the hot electron effect prevent realistic goals for LNA noise figures much below 2.5dB. Because DCRs do not need to drive 50Ohms loads, improved power and gain performance could be achieved with direct matching. For out hypothetical system, we will assume performance measures for the CMOS LNA powered by a 3Volt supply to be: Gain 20dB, noise figure 3dB, IIP3 0dBm, power consumption 30mW. To

complete the picture of the system in which our mixer will operate, channel select filters are briefly discussed next.

Channel Select Filters

Both continuous time and switched capacitor filters have been used in direct conversion receivers [9-14]. A review of continuous time filters, including gyrator filters and MOSFET-C filters, is found in Tsividis [25]. Shaeffer, *et al.* [27] also has an excellent section on gyrator filter design. For layout of switched-cap filter stages Cho, *et al,*[23] have a detailed explanation with helpful figures. The table below includes results from three papers which included results for CMOS DCR channel select filters.

	noise figure	IIP3	Type
Chang *et al.* [22]	37.7dB	30dBm	CMOS SC
Cho *et al.* [23]	33.7dB	30dBm	CMOS SC
Khorramabadi *et al.* [24]	33.8dB	34dBm	Active RC

Table I - Comparison of channel select filters

From these results, it is reasonable to assume that an on-chip channel select filter with a noise figure of 40dB and an IIP3 of 30dBm would typically be included with a low cost DCR system.

As will be shown in our mixer design these specifications help to determine the optimal gain, noise figure and IIP3 for the mixer.

Having reviewed the literature on the topics of direct conversion architectures, CMOS mixers, LNA's and channel select filters, the next section presents our offset cancellation mixer.

A Direct-Conversion Offset-Cancellation Mixer in 2.4GHz CMOS

RESEARCH INTRODUCTION

Recently, there has been an explosion of wireless products, with a promise of many more to come. Standards like Bluetooth and HomeRF are creating a market for wireless products at 2.4GHz for which low cost and low power consumption are the key elements. These requirements are a natural match to using CMOS and to using the direct conversion architecture. The fundamental advantage of direct conversion over the more traditional heterodyne architecture for these emerging applications is its amenability to greater monolithic integration and reduction in power consumption [1-3]. In this paper, we present a direct conversion mixer architecture that overcomes the offset problem for direct conversion – one of the problems that has limited its use in commercial products.

The mixer we present in this paper is a modification of a differential Gilbert cell mixer that has been presented in many other papers [4-6]. This structure was chosen as the starting point because of its many intrinsic properties; The conversion gain of a Gilbert cell mixer with active loads helps to overcome noisy following stages. The DCR mixer need not drive a 50Ω load but can drive a higher impedance. Being doubly balanced and differential, the DCR mixer operates well in the presence of digital clock noise, power supply noise and other common mode noise sources. Because mixing occurs by switching, turning

transistors completely on and off, the Gilbert cell has excellent LO AM noise rejection, which helps to reduce RF to LO coupling and hinders large adjacent channel interferers from self mixing. Finally, the Gilbert cell yields the best gain and linearity of active doubly balanced mixers [7].

However, before discussing our new mixer architecture it is useful to explore how and why offsets arise in direct conversion, why they limit the performance of this architecture and why the term DC offset is a bit of a misnomer. The offsets that are generated in direct conversion mixers can be classified as being either static or dynamic in nature. Static offsets arise when insufficient on-chip isolation couples the strong LO signal (which is often 70 dB above the desired RF signal) through the substrate into the signal path at various points: the antenna, the input of the LNA, and RF port of the mixer. The LO signals that get coupled into the signal path 'self mix' in the mixer, resulting in a down-converted DC (or slowly varying) offset signal. Consider the mixer in Figure 2, where LO leakage couples from the LO port to the RF inputs. The addition of the LO power to the input transistors causes differential current offsets to appear in the drains of M1 and M2. This differential current appears in the baseband loads, labeled *Offset Current*. Mathematically, this can be described by the leaked LO wave $M(t)\cos 2\pi f_{LO}t$ which is self modulated in the switches giving $[M(t)\cos 2\pi f_{LO}t]^2$. Using the trigonometric identity:

$$[M(t)\cos f_{LO}]^2 = \frac{M^2(t)}{2} + \frac{M^2(t)}{2}\cos(2\cdot 2\pi f_{LO}t) \qquad (1)$$

it is seen that an offset $\frac{M^2(t)}{2}$ and a second harmonic are generated. These are filtered by the limited bandwidth of the large load FETs. Offsets resulting from coupling of the LO to the LNA and RF port of the mixer creates a static or very low frequency dynamic offsets.

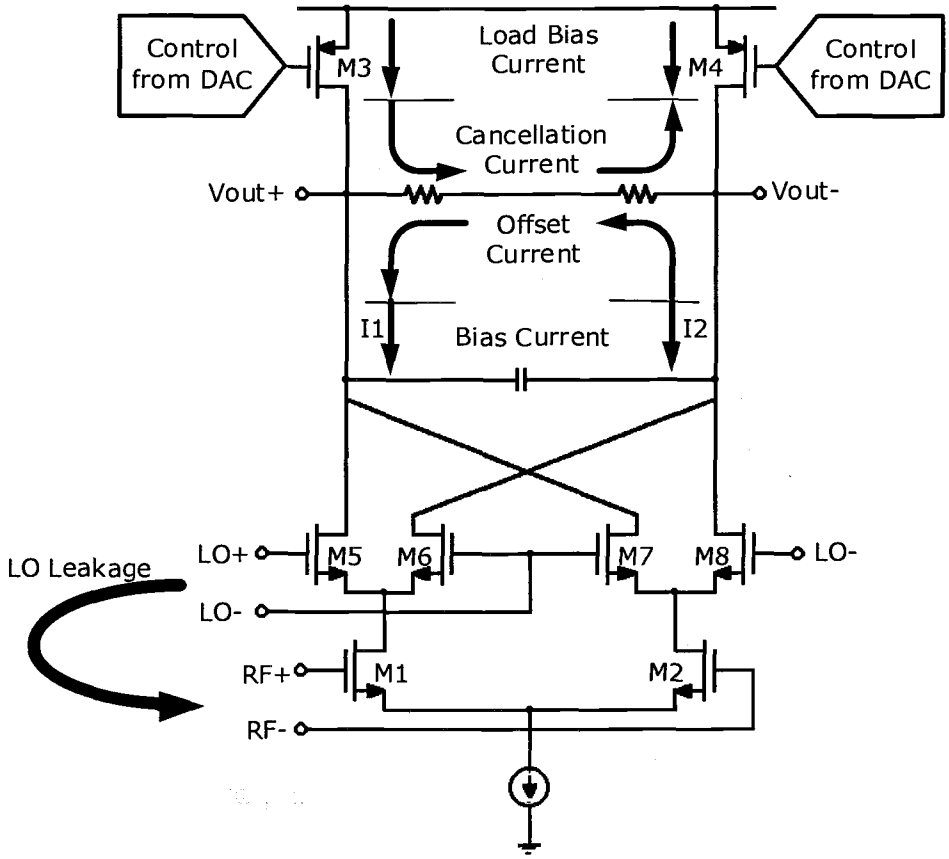


Figure 2 Leakage creates differential current offsets in the Gilbert cell.

Dynamic (time-varying) offsets can arise from several sources. One way in which dynamic offsets arise is when the LO couples to and radiates out of the antenna (leaks out of the antenna), reflects off moving objects (or off stationary objects while the receiver is moving) and re-enters the receiver. This signal then passes through the desired RF signal path, and sees the gain of the LNA before self-mixing [1], as shown in Figure 1. A second source of dynamic offset is when the user touches the antenna. This results in an impedance mismatch between the LNA and the antenna, which changes the coupling mechanism of the static offset and thus creates a dynamic offset. A third source of dynamic offsets is when a nearby user's LO radiates out of their antenna and is received in the front end of the radio. This is especially problematic when the handset is far from the basestation (weak desired signal) and the AGC is maxed out.

With this understanding of the mechanisms by which offsets are created we move on to explore why they are so problematic in direct conversion receivers. First, the offsets that appear at the output of an RF mixer can easily be 20 to 30 dB larger than the desired signal levels. This is true for mixers both in direct conversion and in heterodyne receivers. However, in a heterodyne receiver the offset signal (which is at DC) is far from the IF (to where the desired signal is mixed) and thus can be easily removed by bandpass filtering or capacitive coupling. In direct conversion the desired signal is converted to DC (thus the name zero IF) and the offset appears in the middle of the desired channel. It is extremely

difficult to remove this offset without distorting the desired signal, especially for narrowband signals. Unfortunately, if not removed the offset will saturate downstream gain stages, desensitize the receiver, rail out the A/D converter and destroy the performance of the receiver. Second, offsets degrade the IIP2 performance. Offsets exploit circuit non-linearities by differentially shifting the small-signal bias point of a matched pair, forcing once symmetrical transistors to operate in different bias regions. This creates unbalance, generating second order distortion [1, 2, 19]. If we do not cancel the differential offset until some later downstream stage, each intermediate stage will be bias shifted and additionally contribute to the overall second order distortion for the system.

Previously published offset cancellation schemes have compromised receiver cost and performance in one of two ways. They either cancel offsets downstream of the mixer, or cancel offsets at the mixer but with large off-chip capacitors. Off-chip components add significant cost to the high volume production receiver. In order to tolerate low frequency notching of the offset, two methods are used. One is to reduce signal energy around DC with spectrally inefficient FSK based modulation schemes [8-10]. Alternatively, if licensing allows, wide band systems [9-14] with channel bandwidths in excess of 1MHz are used to reduce the ratio of discarded information to channel bandwidth. In both cases low frequency energy is wasted just to remove the infrequent steps in offset which briefly consumes considerable bandwidth. Creating the low RC time constant needed for on-chip high pass filtering is difficult. Because of the kT/C noise of large CMOS

capacitors, a large on-chip capacitor must be used only after many amplification [14]. Considering that a 1nF capacitor must be preceded by approximately 40dB of gain following the mixer, it seems infeasible to attempt to notch any reasonably low frequency on-chip. Thus to remove offsets without off-chip components, a better solution than simple passive notching must be found.

This work is focused on developing a method to track and cancel dynamic offsets at the location where they appear, the mixer. By performing offset cancellation in the mixer, the dynamic range of the entire receiver chain is maximized and sensitivities are not compromised. An offset cancellation mixer which easily integrates with a low noise digital filter to track the offset is desirable. Furthermore, through the use of adaptive filtering, low frequency energy need only be removed for the occasional jump change in offset. During normal operation, only the DC energy componet will need to be removed.

Having shown that offset cancellation is best when performed in the mixer, we discuss the function of a Gilbert cell mixer and focus on how offsets arise in this architecture (Figure 2). The basic operation of the Gilbert cell is easily seen if one initially neglects the switches M5-M8. In this case, the Gilbert cell reduces to a differential amplifier. If we reintroduce the switches into our hypothetical case, we see that they serve to commutate the signal from the drains of M1, M2 back and forth between the loads M3 and M4. This commutating action causes the signal to be both upconverted to the 2^{nd} harmonic of the LO, and downconverted to the baseband. Because of the parasitic capacitance of the large load transistors M3

and M4, no RF signal can pass and the upconverted image is removed. Thus at the loads only the baseband portion of the mixing products is found.

Having understood the basic operation of the Gilbert cell, we now discuss how offsets arise (in anticipation of the presentation of our offset cancellation technique). Recall that offsets generally arise in mixers due to the problem of self-mixing. For the Gilbert cell mixer shown in Figure 2 this can be envisioned as a coupling (either time-varying or static) of the LO signal into the RF port (M1, M2) of the mixer. This coupled signal may or may not be in phase with the LO signal; however, it is the in-phase portion of the coupled signal that creates the offset.

For example, consider an LO of 0dBm driving the switching quad of a Gilbert cell. A -30dB coupling to the RF port of the mixer would produce an attenuated LO signal with amplitude 20mV_{pk-pk}. A transconductance of 5mA/V in M1 would cause a $100\mu\text{A}_{pk-pk}$ current to appear through M1 as shown in the left of Figure 3a. Since M5-M8 act to switch the commutation of the signal, they are represented by the switching waveform in the middle of Figure 3a. The waveform on the right shows the product of the leaked LO current signal and the original LO switching signal as a rectified sinusoid with a dc component of $35\mu\text{A}$. The sequence of waveforms in Figure 3b show the generation of a $46\mu\text{A}$ dc offset from a square LO. In either case the offset first appears in the baseband transistors as a differential current offset as shown in Figure 2. However, the offset does not appear in the switches or the input pair due to the modulating nature of the switching quad.

In the remaining sections of this paper we present a new circuit design to cancel offsets. Section II examines circuit structures to inject the cancellation current. Section III presents HSPICE simulation results. Finally, in Section IV, we discuss our results and conclusions.

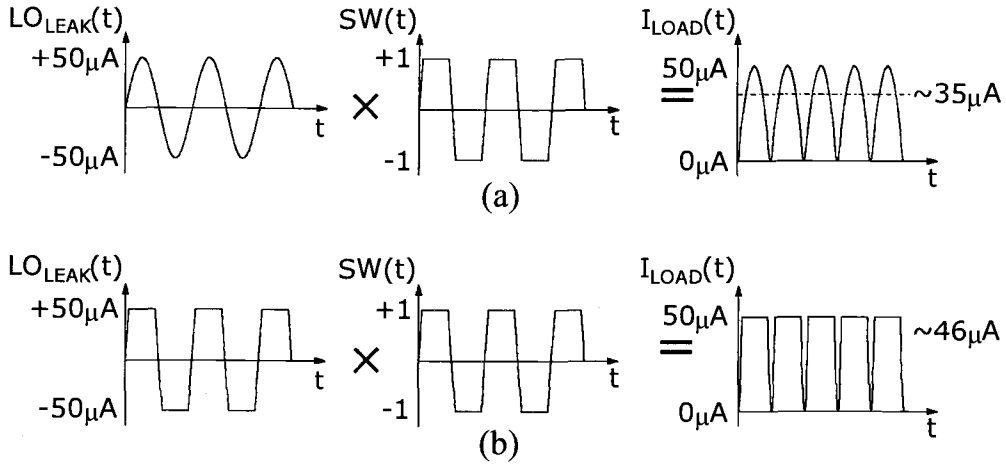


Fig. 3 Example of two different LO waveforms self mixing.

SYSTEM LEVEL MIXER DESIGN

In the previous section we reviewed the basic operation and function of a Gilbert cell mixer. In doing so, we observed how offsets arise when self-mixing occurs. We also noted that from a systems point of view it is best to cancel offsets before they propagate to downstream components and reduce the dynamic range of a receiver. Since a mixer is just one stage in a receiver's chain, we optimize our mixer within the context of feasible, assumed receiver. For the purposes of our research, we designed our mixer assuming that it was preceded by an LNA [20, 21] that has a gain of 20dB and a noise figure of 3dB and was followed by a channel select filter [22-27] with a noise figure of 40dB. We also assumed a 3 volt power supply to add relevance to dynamic range considerations. Given this assumed configuration we strove to develop a set of specifications for the mixer such that it was neither over-designed, nor was a performance bottleneck. The target specs for our mixer were a gain of 6dB, a noise figure that is less than 20dB and the largest IIP3 possible. The level diagram shown in Figure 5 shows how this set of specs meets our desire to neither waste nor inhibit performance. However, we must also be aware that, as stated earlier, offsets and offset cancellation create imbalance, which makes IIP2 a critical design parameter. This will be examined in our final design.

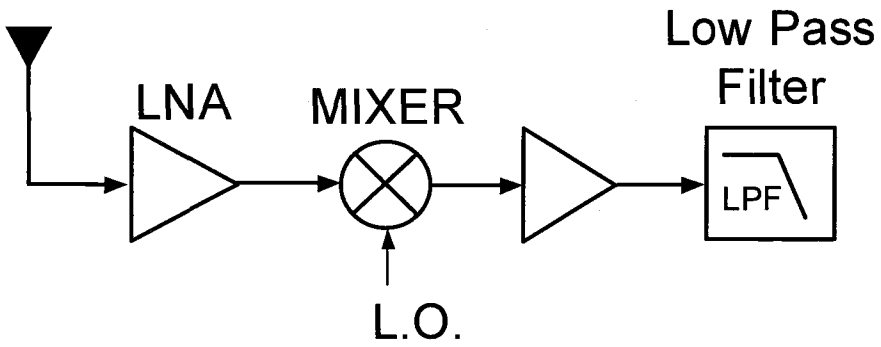


Figure 4 Direct conversion receiver chain components where blocking dynamic range is critical.

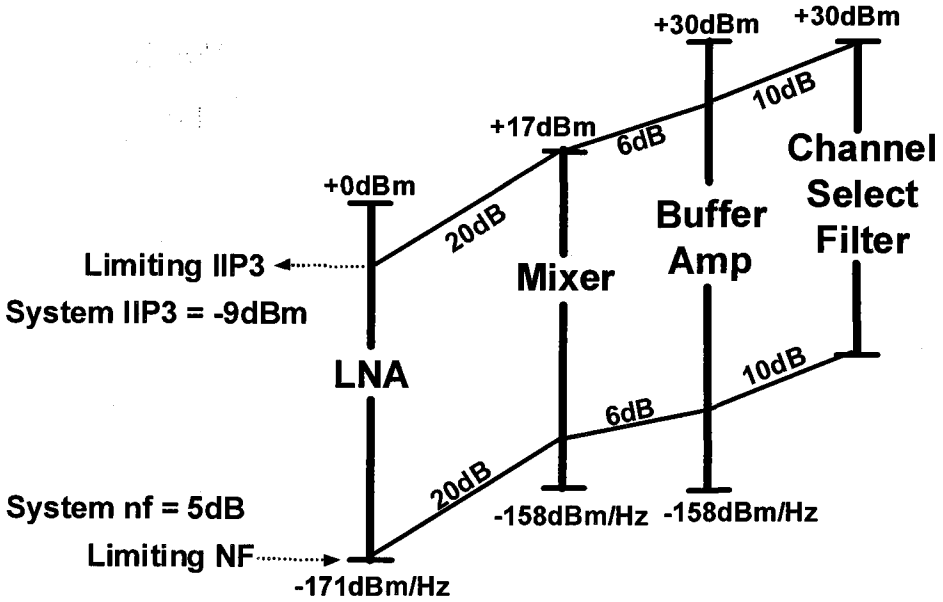


Figure 5 Link budget for IIP3 and noise figure.

CIRCUIT DESIGN

In this section we describe in detail our circuit design for the offset cancellation mixer that meets the previously defined specifications. The focus of this discussion will be on the tradeoffs of our design and on the operation and performance of the mixer when the bias of the mixer loads is adjusted to the "best" cancellation value. The best cancellation value need not exactly cancel the offset. Alternatively, the cancellation value need cancel the offset only to within the order of magnitude of the envelope of the desired signal. With digital circuitry four bits of accuracy should be necessary to center the even weak signals. It is preferred to used a digital feedback loop for averaging, since long averages can be utilized to create low frequency poles which would be difficult with analog equivalents. Additionally, the greatest advantage of digital filtering is having adaptive filter corners. It is quite feasible to have multiple simultaneous averaging loops which track both slow and fast offsets and are switched into operation by an adaptive algorithm when needed. To implement digital filtering a DAC must be integrated into the mixer to inject the cancellation value and reduce the offset.

Design for Offsets

In the Gilbert cell mixer, the best place to inject an offset cancellation signal is in the loads. In many fields of engineering as in this case, it is often the simple solution which best fixes the problem. We could find a complex solution to attempt to cancel the offsets in the RF, but doing so would inevitably incur

numerous difficulties. Canceling offsets in the loads of the mixer removes offsets at the earliest possible location in the receiver chain without maligning the RF circuitry. Canceling offsets in the mixer allows maximum signal gain without distortion downstream. We use a current DAC and a current mirror to inject the offset cancellation signal as shown in Figure 7. By manipulating the DAC, a cancellation current is passed through the current mirror to provide the mixer output with the current necessary to cancel the offset. Figure 2, shows the currents in the load transistors M3-M4 in more detail.

Before determining transistor sizing and biasing for our mixer we introduce a metric by which to fairly evaluate the offset current. Since the differential branches must operate with the imbalance created by both the offset current and the cancellation current we define a new quantity,

$$\delta I = \frac{\text{differential offset current}}{\text{bias current } I} \times 100\% \qquad (2)$$

For our cancellation scheme to be effective it must allow the mixer to perform well at reasonable imbalance levels δI . To determine the range of δI we present HSPICE simulation results for typical levels of LO coupling found in our mixer. In this example, which uses similar values to our final design, the tail current was 2.5mA, the LO power was 0dBm, the transconductance of M1, M2 was each 2.7mA/V, and the loss in the switches was 0.41A/A . Figure 6 shows δI for all reasonable levels of coupled LO re-injected into the RF port of the mixer. The x-

axis maximum of -10dBc (worst case we are considering) could occur when there is 30dB of isolation between the LO and the input of an LNA which has a gain of 20dB. We have designed our mixer to operate with good performance up to the expected maximum δI of 8%.

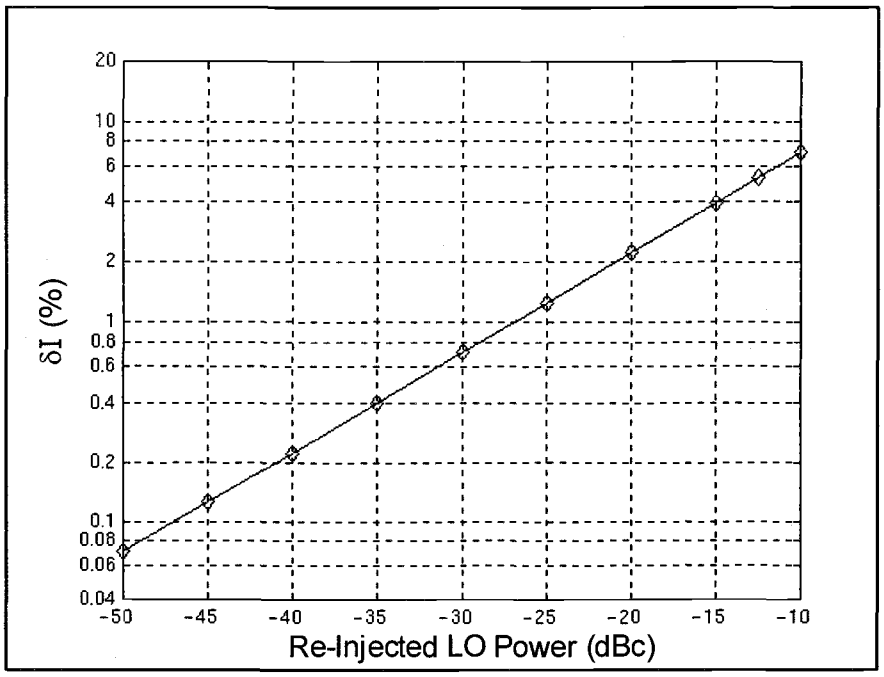


Figure 6 Percent ratio of offset current to bias current caused by Re-Injected LO Power.

After considering this example with our new metric, an obvious conclusion is that mixers operating with less bias current will have more difficulty with offsets. Furthermore, a Gilbert mixer which distributes it's gain with less transconductance and a higher load impedance will improve δI performance since the created offset current will see less gain and thereby be smaller when cancelled. Reducing LO drive will reduce δI simply because less LO will be coupled through. However, lower LO drive increases switch noise and reduces mixer IIP3 performance. It becomes apparent that δI is another design parameter with tradeoffs potentially competing for power, sensitivity, distortion, and sizing. In the next section we show the circuit which we chose for it ability to maintain good overall performance in the presence of typical levels of δI .

Circuit Description

Figure 7, contains a schematic for our mixer. It comprises a standard Gilbert cell, a differential DAC which dynamically controls the mixer loads, and common-mode feedback (CMFB) circuitry. To maintain our goal of low power consumption we set the mixer tail current to 2.5mA. Planning for the addition of approximately another milli-amp for the DAC and CMFB circuitry this makes for a very reasonable power consumption in half micron CMOS. To improve IIP2, IIP3 and reduce δI , the input transistors have been scaled fairly small. The cost of small transistors is that they must operate with increased current density and therefor

increased noise[6]. A $20\mu m$ width was the best size to handle the current density and maintain f_t. Since in direct conversion, the mixer output is no longer limited to 50 Ohms, gain can be increased with a large load resistance. To set the target gain of 6dB the poly-silicon

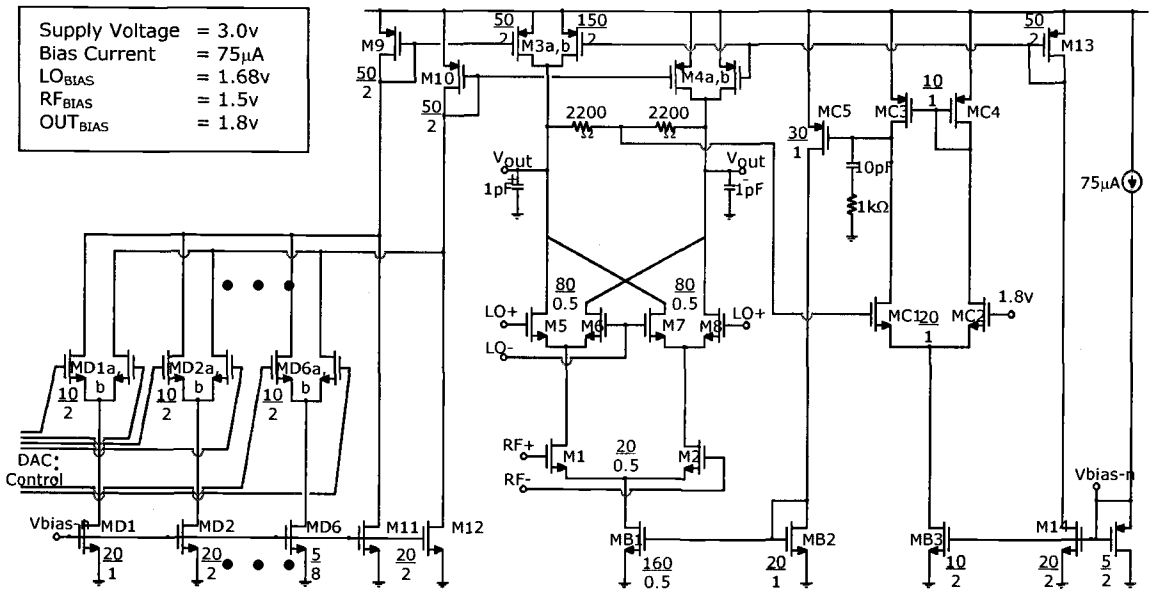


Figure 7 - Circuit diagram of adaptive cancellation mixer.

resistors are made to be 2200Ω which sets the combined resistance at the output node to 1800Ω. This allows significant improvements in gain performance for the overall mixer even though such small input FETs are used. The switching quad M5-M8 are sized as large as possible to minimize flicker noise [6], yet they must be fast enough to completely switch while operating at 2.4GHz. Truly these become the most critical transistors in the entire circuit. Great care must be taken in their layout to reduce unbalance and parasitic capacitance. The 1pF capacitors seen at the loads add both compensation to the CMFB loop and low pass filtering to unwanted RF signals.

Common Mode Feedback

Good common mode feedback is essential for unbalanced operation of any differential circuit. Since in our application differential offsets shift bias points and create even further unbalance, common mode feedback becomes the key to maintaining decent even-order distortion performance [28]. The key to CMFB is to accurately measure the common mode signal independent from the differential signal. Since the Gilbert cell already chosen, has differential load resistors, these can be used to measure the common mode signal. As can be seen in Figure 7, the common mode sense point is measured (sensed) between the two load resistors. The inverted common mode signal is re-injected into the tail current of the mixer instead of the loads to take advantage of the additional gain seen from the cascoded transistors above the current mirror MB1. The total loop gain is 60dB.

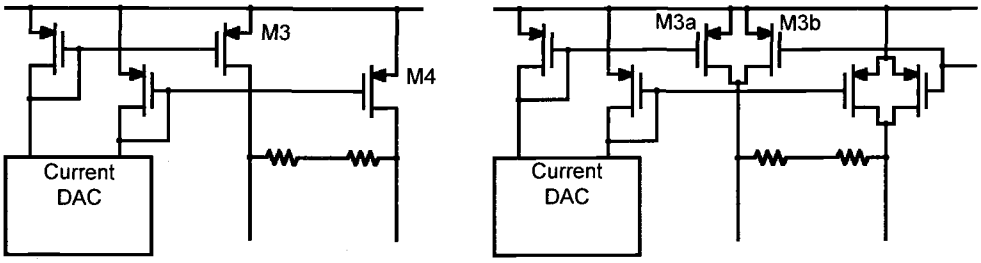
A 10pF capacitor in series with a 1kΩ resistor is used to compensate the loop to give a phase margin of 60°.

When the mixer is operating at large δI, the unbalance between M3 and M4 will cause a difference in their channel resistances. This resistive mismatch will effectively unbalance the resistance seen at each side of the common mode sense point. The common mode loop will then track and cancel a small portion of the differential signal. Thus, when operating with large levels of offset cancellation we expect to see a slight roll-off in the mixer gain. Additionally this will cause the CMFB to become less effective at canceling even order distortions. This is a potential weakness in our circuitry. To minimize the potential for resistive mismatch at the loads, long channel transistors of $2\mu m$ have been utilized for their large channel resistance.

Cancellation DAC

In this section we will discuss the cancellation DAC and the design tradeoffs that were made in its development. The current DAC must use some form of current mirror to inject the cancellation current into the mixer loads instead of being directly coupled to the mixer output so as to maintain signal swing at the mixer output nodes. This keeps the DAC from consuming mixer headroom and maintains IIP3 performance. Additionally this helps to buffer variations in the DAC's output resistance that would cause the mixer gain to vary with δI.

Figure 8a shows the approach of injecting offset cancellation current from the DAC through a current mirror. This has a minimal effect on output signal swing, and completely buffers the DAC output impedance from the mixer output nodes. Unfortunately, when noise is considered, it becomes apparent that the current in the DAC must be equal to the mixer tail current to avoid amplifying the DAC noise being mapped into the mixer. Since we do not wish to consume 2.5mA in the DAC a tradeoff is made as shown in Figure 8b. This approach splits the load transistors, M3-M4, and allows less



(a) (b)

Figure 8 Three methods of injecting cancellation current into a Gilbert cell mixer.

than a milli-amp of current to be necessary for the DAC. The tradeoff is that linearity at large δI is sacrificed. When the now smaller load M3a is driven to cancel an offset, it's gate must be driven harder to generate the same cancellation current that the larger M3 would have made. With a larger gate voltage of M3a, headroom in the mixer output is reduced. We chose a balance between mixer IIP3 and DAC power consumption by splitting M3 3:1 with M3a one third the size of M3b.

Even after the previous design tradeoff we still must take efforts to the minimize the DAC thermal and flicker noise contributions. We use a minimum of $2\mu m$ gate length FETs in the entire DAC to reduce flicker noise. The DAC mirrors are biased with minimal gate voltage to reduce thermal noise. Simulations show, that in the end our DAC contributes an insignificant amount of noise to the mixer output and is trivial when compared to the input referred noise of the channel select filter (typically around 30dB).

Analysis

Before presenting simulation results it is informative to present hand calculated estimates of predicted performance values. We use the mixer gain equation:

$$\text{Mixer Gain} = \left(\frac{2}{\pi} dty\right) g_{m1,2} R_L$$

where $2/\pi$ is the switching loss for an ideal square LO. For a more realistic LO waveform we add the duty cycle (*dty*). We used *dty* = 70%. Thus for $g_{m1,2} = 2.74mA/V$, and $R_L = 1800\Omega$ the mixer gain is ~6.8dB.

To estimate the noise figure we will make the assumption that M1-M2 and M3-M4 contribute most of the thermal noise. This is a good assumption since the switches operate primarily in the triode with low on resistance. Additionally, the CMFB circuitry primarily adds only common mode noise and is negligible. Thus for a first order approximation of the input referred noise the following equation can be used.

$$\hat{v}_n^2 = 4kT\left[\frac{\gamma_1}{g_{m1}} + \gamma_3\left(\frac{\pi}{2dty}\right)^2\frac{g_{m3}}{g_{m1}^2}\right]$$

Here $g_{m3} = 3.33mA/V$, $\gamma_1 = 1.18$ and $\gamma_3 = .667$ are used to account for current density based on figures shown in Terrovitis [6]. The resulting input referred noise is $ni = 4.24nV/\sqrt{Hz}$, or a noise figure of $nf = 13.6\text{dB}$. With the addition of flicker noise we can expect this value to increase several dB.

Through hand calculating we can estimate an upper bound for IIP3. Since the gain of the mixer is much greater than unity we can assume the output of the mixer is responsible for gain compression. The simplest calculation comes when we consider the output DC voltage of 1.8V which is 1.2V from the upper rail and is limited by $(V_{gs3} - V_{t3})$ as M3 enters triode operation. This leaves a remaining swing of ~.9V_{pk} above the output node before compression occurs. Converting

this value to dBm, adding 11dB for the P1dB to IIP3 conversion and adding 6.8dB for gain gives ~27dBm as an upper bound for IIP3. Of course if we get within half that value, 21dBm, we are doing good!

Having walked through the hand calculated estimates for our mixer, in the next section we present simulation results.

SIMULATION RESULTS

Transient Measurements

The circuit (Fig. 7) has been simulated in HSPICE using both BSIM3v3 models 'tuned' for RF and BSIM3v3 models available from MOSIS for a .5μm HP CMOS process. Gain, bandwidth, noise figure and distortion performances were also checked in SpectreRF. The agreement between hand analysis and two different simulators gives us confidence in our simulated results.

To demonstrate the functionality of our offset cancellation mixer we first show a hypothetical bit stream (with no modulation) as it encounters an offset, and the mixer is then driven to cancel it. This is shown in Figure 9. On the left side of the figure the mixer is operating with no offset. Shown in the middle of the figure a step change in LO of –30dBc is added in phase to the RF input and a step offset results. After some delay the feedback loop is driven to cancel the offset to within an order of magnitude of the original signal level as shown on the right side of the figure. This example is only used to demonstrate the concept behind offset cancellation. Building upon this concept of adding an LO to the RF input and canceling the offset, we simulated our mixer at various levels of LO coupling and measured the mixer performance.

To measure IIP2, IIP3 and Gain we simulated an RF input consisting of two sinusoidal tones spaced 1MHz apart near 2.4GHz. To find the intermodulation levels, transient results were taken from HSPICE and fast fourier transformed. A

typical figure used to measure IIP3 is shown in Figure 10. To simulate re-injected or coupled LO we added in phase an attenuated version of the LO drive signal. Figures 11-13 plot the simulated Gain, IIP3, and IIP2 against the amount of LO coupling added to the RF input. In Figure 10, Gain appears to have little variation with LO coupling. Above –15dBC coupled LO, the gain does appear to compress some as we predicted due to the CMFB tracking a small portion of the differential signal. Figure 11 shows IIP3 versus LO coupling. Typical simulation error levels can be seen in this plot as the data points shift up and down. If any IIP3 compression or enhancement exists as a function of the coupled LO it is small and buried in the variance of the measurement.

The IIP2 graph shows the even order distortion growing with LO coupling. As discussed earlier in the paper, differential non-linear devices generate 2^{nd} order distortion as their biases shift differentially. Even though we are canceling the offset voltage at the mixer output, the current offset with the mixer is creating 2^{nd} order distortion. As discussed earlier we designed our mixer with emphasis much more on distortion performance than upon noise or gain. Even with a maximum re-injected LO power of –10dBc, the IIP2 is still above 28dBm. Results given by Takahasi [19] suggest that when mixer IIP2 drops below 30dBm this begins to dominate receiver distortion. Thus we see the importance of predicting the worst-case coupled LO power and designing the mixer to yield decent IIP2 performance at this level.

Table II compares our mixer performance against a similar Gilbert cell without the offset cancellation circuitry. As can be seen the primary cost of offset cancellation is an additional 0.9dB of noise figure and 1.8mW of power in our .5μm HP CMOS process.

	Mixer w/o cancellation circuitry	Mixer w/ cancellation circuitry
Gain	6.4dB	6.4dB
IIP3	17dB	17dB
noise figure	16.1dB	17.0dB
linear output range	$2.4V_{pk\text{-}pk}$	$2.4V_{pk\text{-}pk}$
LO Power	0dBm	0dBm
CMRR	34dB	34dB
Current Consumption	3.4mA	4.0mA
Power Consumption	10.2mW	12.0mW

Table II – Comparison of mixer characteristics

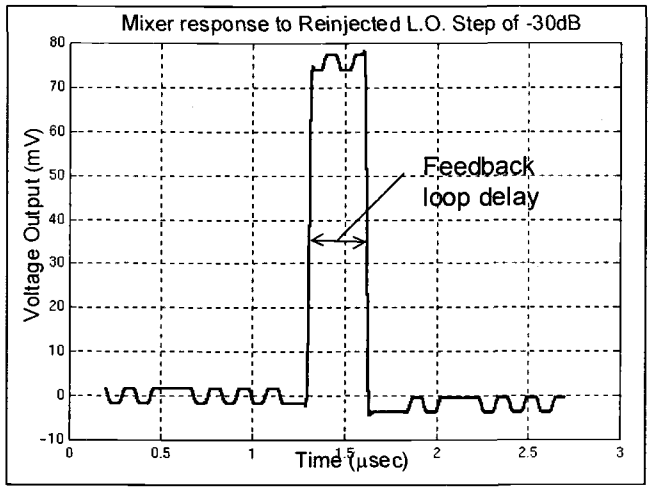


Figure 9 HSPICE Simulation of the mixer down-converting a bit-stream. A step LO is re-injected and after a delay the mixer DAC is driven to cancel the offset.

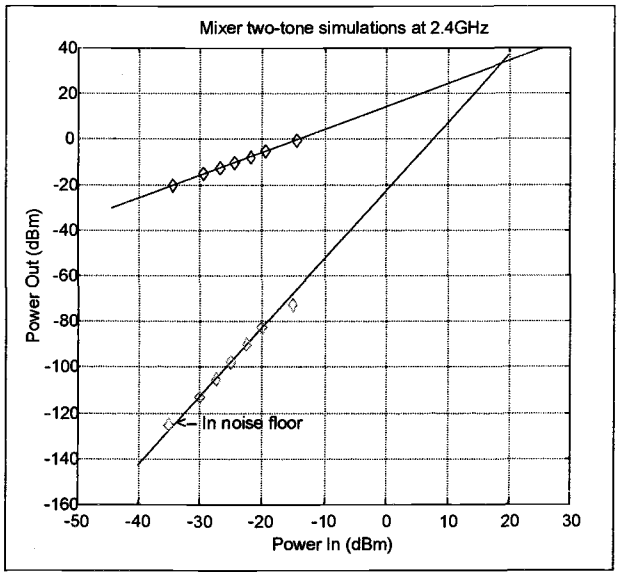


Figure 10 Intercept plot for third order distortion.

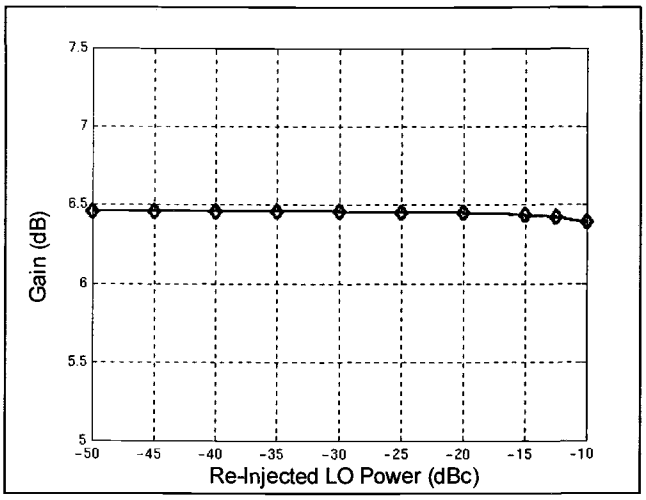


Figure 11 - Gain versus re-injected LO power

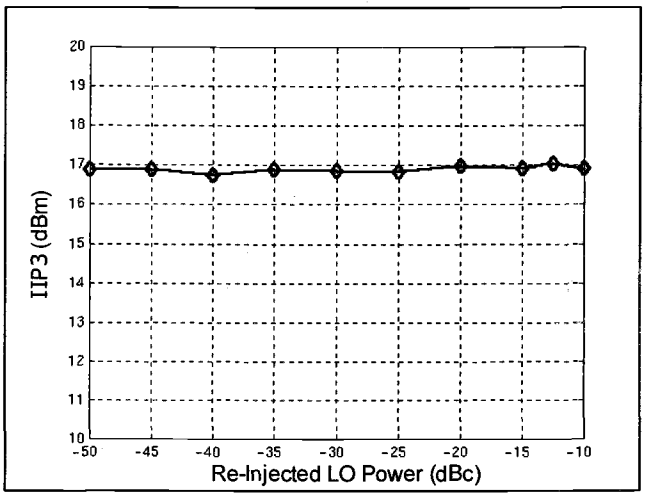


Fig. 12 - IIP3 versus re-injected LO power

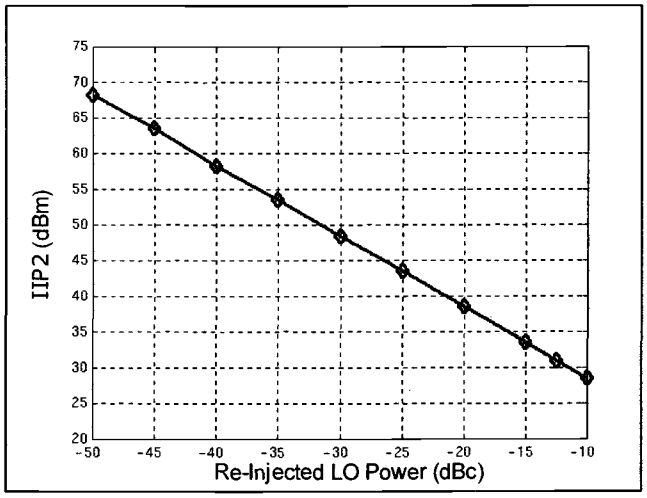


Fig. 13 - IIP2 versus re-injected LO power

Mismatch Considerations

Since we have shown that unbalance caused by offsets affects mixer IIP2 performance, it is insightful to show Monte Carlo results for the same mixer when process variations are included in the simulation. We used statistical process data, found in Foty [29] to vary the four fundamental process parameters: gate oxide thickness TOX, channel length variation LD, channel width variation WD and threshold voltage variation DELVTO across their three sigma range. Using these variations, each transistor, resistor and capacitor in the circuit was randomized and twenty separate circuit models were generated. For each circuit model the same intermodulation measurements from the previous sections were taken, repeating the simulations in figures 11-13.

Gain and IIP3 continued to be independent of re-injected LO power for each simulation and only varied with process. The standard deviation of the measured Gain was 1.1dB and the standard deviation of IIP3 was 4dB. These are both typical numbers for a production mixer.

Figure 14 shows a three-dimensional plot of IIP2 versus LO coupling. This is a very similar plot to the one in Figure 13, except that this one displays on the z-axis several IIP2 curves each corresponding to a randomized circuit. To make viewing easier we sorted these curves from the lowest to highest.

Now we can make some observations from this figure. When no offset exists in a perfectly balanced circuit the IIP2 is infinite. Additionally, as previously discussed, the unbalance created in the circuit by the offset cancellation lowers the IIP2. However, for the case of a circuit which has inherent unbalance the optimal IIP2 performance will occur for some finite amount of cancelled offset. Thus if we observe the back half of the curves in Figure 14 we see that IIP2 peaks at a finite level of offset and thus a finite level of re-injected LO power. In our simulations we always added the re-inject LO in phase with the RF signal. It is presumable that for some inherently unbalanced circuits an out of phase re-injected LO would be needed to maximize the IIP2. The first ten curves show this situation.

Of course in a multipath environment the re-injected LO phase will be jumping around from 0° to 360° phase shift and no real-life circuit will remain in a "sweet spot" for long. Thus for this circuit design it appears 40dBm is the best IIP2 that can be expected for re-inject LO levels below -20dBc.

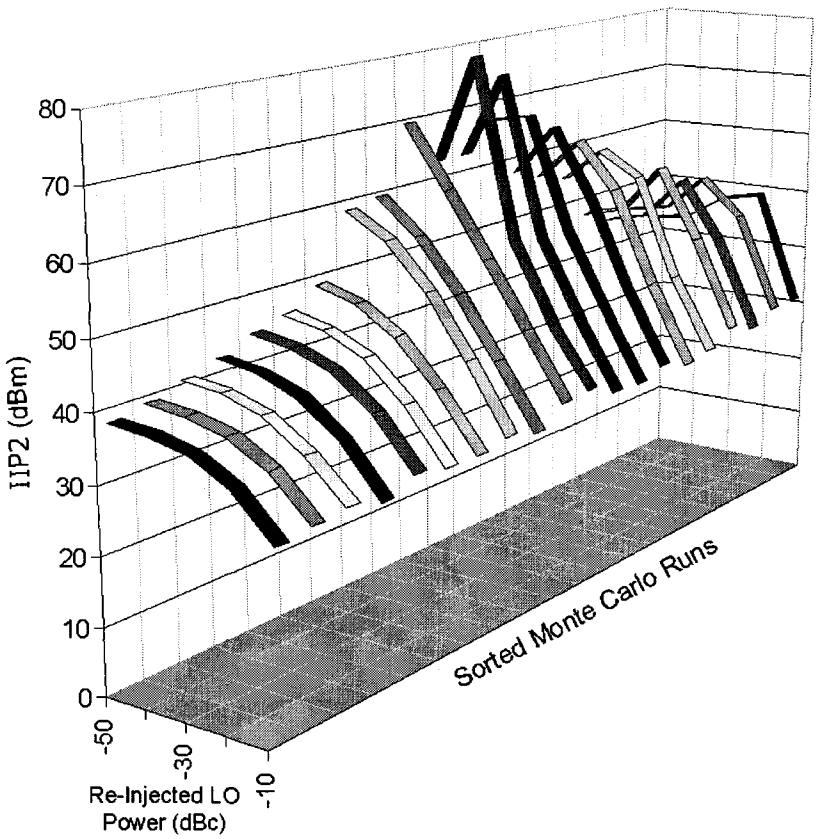


Fig. 14 Monte-Carlo analysis adds insight into the relationship between IIP2 performance and transistor mismatch.

CONCLUSION

In this paper an offset cancellation mixer was presented. Relevant mixer design issues were discussed in the light of heightened distortion performance requirements caused by mixer operation under offset cancellation. Emphasis was placed on minimizing even order distortions. Simulation results show good mixer performance during the cancellation of any reasonable offset. Our simulation results show a mixer gain of 6.4dB, 12 mW of power consumption, IIP3 of 17dBm and a noise figure of 17dB. We hope that this work helps to facilitate low power receiver designs as transceiver integration becomes more prevalent.

BIBLIOGRAPHY

[1] B. Razavi, "Design Considerations for Direct Conversion Receivers," *IEEE Trans. on Circuits and Systems, Part II*, vol. 44, pp. 428-435, June 1997.

[2] A. A. Abidi, "Direct-conversion radio transceivers for digital communications," *IEEE J. of Solid-State Circuits*, vol. 30, no. 12, pp. 1399-1410, 1995.

[3] P. R. Gray *et al.*, "Recent Developments in High Integration Multi-Standard CMOS Transceivers for Personal Communication Systems," *Int. Symp. on Low Power Electronics*, Monterey, Ca, August 1998.

[4] P. J. Sullivan, W. H. Ku, "Active Doubly Balanced Mixers for CMOS RFICs," *Microwave Journal,* pp. 22-38, October 1997.

[5] A. Rofougaran, J. Y-C. Chang, M. Rofougaran, and A. A. Abidi, "A 1 GHz CMOS RF Front-End IC for a Direct-Conversion Wireless Receiver", *IEEE J. of Solid-State Circuits*, vol. 31, no. 7, pp. 880-889, 1996.

[6] M. Terrovitis, R. G. Meyer, "Noise in Current-Commutating CMOS Mixers," *IEEE J. of Solid-State Circuits*, vol. 34, no. 6, pp. 772-783, 1999.

[7] S. A. Maas, "Mixers for Wireless Applications," *RF and Microwave Circuit Design for Wireless Communications.* Norwood, MA: Artech House, pp. 282, 1997.

[8] J. F. Wilson, R. Youell, T. H. Richards, G. Luff, and R. Pilaski, "A Single-Chip VHF and UHF Receiver for Radio Paging," *IEEE J. of Solid-State Circuits*, vol. 26, no. 12, pp. 1944-1950, 1991.

[9] A. Rofougaran, *et al.*, "A Single-Chip 900-MHz Spread-Spectrum Wireless Transceiver in 1-μm CMOS Part II: Receiver Design," *IEEE J. of Solid-State Circuits*, vol. 33, no. 4, pp. 535-547, 1998.

[10] T. Cho, E. Dukatz, M. Mack, D. MacNally, M. Marringa, S. Mehta, C. Nilson, L. Plouvier, S. Rabii, "A Single-Chip CMOS Direct-Conversion Transceiver for 900MHz Spread-Spectrum Digital Cordless Phones," *ISSCC Dig. Tech. Papers*, pp. 228-229, Feb. 1999.

[11] A. Parssinen, J. Jussila, J. Ryynanen, L. Sumanen, K. Halonen, "A Wide-Band Direct Conversion Receiver for WCDMA Applications," *ISSCC Dig. Tech. Papers*, pp. 220-221, Feb. 1999.

[12] A. Parssinen, J. Jussila, J. Ryynanen, L. Sumanen, K. Halonen, "A 2-GHz Wide-Band Direct Conversion Receiver for WCDMA Applications," *IEEE J. of Solid-State Circuits*, vol. 34, no. 12, pp. 1893-1903, 1999.

[13] C. D. Hull, J. L. Tham, R. R. Chu, "A Direct-Conversion Receiver for 900 MHz (ISM Band) Spread-Spectrum Digital Cordless Telephone," *IEEE J. of Solid-State Circuits*, vol. 31, no. 12, pp. 1955-1963, 1996.

[14] B. Razavi, "A 2.4-GHz CMOS Receiver for IEEE 802.11 Wireless LAN's," *IEEE J. of Solid-State Circuits*, vol. 34, no. 10, pp. 1382-1385, 1999.

[15] S. Sampei, K. Feher, "Adaptive DC-offset compensation algorithm for burst mode operated direct conversion receivers," *Proc. IEEE Vehicular Technology Conf.*, pp. 93-96, May 1992.

[16] H. Tsurumi, Y. Suzuki, "Broadband RF Stage Architecture for Software-Defined Radio in Handheld Terminal Applications," *IEEE Communications Magazine*, pp. 90-95, February 1999.

[17] P. Eastbrook, B. B. Lusignan, "The design of a mobile radio receiver using a direct conversion architecture," *Proc. IEEE Vehicular Technology Conf.*, pp. 63-72, May 1989.

[18] B. Lindquist, M. Isberg, and P.W. Dent, "A new approach to eliminate the DC offset in TDMA direct conversion receiver," *Proc. IEEE Vehicular Technology Conf.*, pp. 754-757, May 1993.

[19] C. Takahasi, R. Fujimoto, S. Arai, T. Itakura, T. Ueno, H. Tsurumi, H. Tanimoto, S. Watanabe, K. Hirakawa, "A 1.9GHz Si Direct Coversion Receiver IC for QPSK Modulation Systems," *Int. Solid-State Circuits Conf.*, San Fransico, pp. 139-139, 1995.

[20] B. K. Ko, K. Lee, "A Comparative Study on the Various Monolithic Low Noise Amplifier Circuit Topologies for RF and Microwave Applications," *IEEE J. of Solid-State Circuits*, vol. 31, no. 8, pp. 1220-1225, 1996.

[21] D. Shaeffer, T. H. Lee, "A 1.5-V, 1.5GHz CMOS Low Noise Amplifier," *IEEE J. of Solid-State Circuits*, vol. 32, no. 5, pp. 745-759, 1997.

[22] P. J. Chang, A. Rofougaran, A. A. Abidi, "A CMOS Channel-Select Filter for a Direct-Conversion Wireless Receiver," *IEEE J. of Solid-State Circuits*, vol. 32, no. 5, pp. 722-729, 1997.

[23] T. B. Cho, G. Chein, F. Brianti, P. R. Gray, "A Power-Optimized CMOS Baseband Channel Filter and ADC for Cordless Applications," *VLSI Circuit Conference Digest 96*, June 1996.

[24] H. Khorramabadi, M. J. Tarsia, N. S. Woo, "Baseband Filters for IS-95 CDMA Receiver Applications Featuring Digital Automatic Frequency Tuning," *ISSCC Dig. Tech. Papers*, pp. 172-173, Feb. 1996.

[25] Y. P. Tsividis, "Integrated Continuous-Time Filter Design- An Overview," *IEEE J. of Solid-State Circuits*, vol. 29, no. 3, pp. 166-176, 1994.

[26] A. Baschirotto, R. Castello, "A 1-V 1.8MHz CMOS Switched-Opamp SC Filter with Rail-to-Rail Output Swing," *IEEE J. of Solid-State Circuits*, vol. 32, no. 12, pp. 1979-1986, 1997.

[27] D. K. Shaeffer, *et al.,* "A 115-mW, 0.5-μm CMOS GPS Receiver with Wide Dynamic-Range Active Filters," *IEEE J. of Solid-State Circuits*, vol. 33, no. 12, pp. 2219-2231, 1998.

[28] F. O. Eynde, P. Wambacq, W. Sansen, "On the Relationship Between the CMRR or PSRR and the Second Harmonic Distortion of Differential Input Amplifiers," *IEEE J. of Solid-State Circuits*, vol. 24, no. 6, pp. 1740-1744, 1989.

[29] D. P. Foty, "Accounting for systematic process variations," *MOSFET modeling with Spice Principles and Practice.* Prentice Hall, Upper Saddle River, NJ. 1997.

[30] B. Razavi, "Challenges in Portable RF Transceiver Design," *Circuits & Devices*, pp. 12-25, Sept. 1996.

[31] I. A. W. Vance, "Fully integrated radio paging receiver," *IEE Proc. Part F*, vol. 129, no. 1, pp. 2-6, 1982.

[32] A. N. Karanicolas, "A 2.7-V 900-MHz CMOS LNA and Mixer,"

[33] J. Y. Chang, A. A. Abidi, M. Gaitan, "Large suspended inductors on silicon and their use in a 2-um CMOS RF amplifier," *IEEE Electron Device Lett.,* vol. 14, pp. 246-248, May 1993.

[34] P. J. Sullivan, B. A. Xavier, and W. H. Ku, "Doubly Balance Dual-Gate CMOS Mixer," *IEEE J. of Solid-State Circuits*, vol. 34, no. 6, pp. 878-885, 1999.

[35] J. C. Rudell, J. Ou, T. B. Cho, G. Chein, F. Brianti, J. A. Weldon, P. R. Gray, "A 1.9-GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications," *IEEE J. of Solid-State Circuits*, vol. 32, no. 12, pp. 2071-2088, 1997.

[36] J. Crols, M. S. J. Steyaert, "A 1.5GHz Highly Linear CMOS Downconversion Mixer," *IEEE J. of Solid-State Circuits*, vol. 30, no. 7, pp. 736-742, 1995.

[37] B. Razavi, "A 900-MHz CMOS Direct Conversion Receiver," *Symp. on VLSI Circuits Digest*, pp. 113-114, June 1997.