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Title: Drain Current Transient Characterization of P-Channel GaAs MESFET

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GaAs MESFETs are widely used in high speed integrated circuits (ICs) and microwave circuits. Due to the materials and processing methods used in GaAs MESFET fabrication, deep level traps in the substrate materials have a strong influence on device performance.

In this work we used the drain current transient characterization to study the material defect effects on p-channel GaAs MESFETs. We characterized the devices under DC conditions and determined the proper bias conditions for transient measurements. Then we performed the drain current transient characterization at different temperatures. From the temperature dependent current transient results, we used a one-level model to extract the activation energies and capture cross sections for deep levels both in the channel region and in the substrate region. We associated the level in the channel region with an antisite defect $E_{+/++}(As_{Ga})$ and the level in the substrate region with another antisite defect $E_{0/+}(As_{Ga})$. Both levels are related to the EL2 complex.

Drain Current Transient Characterization of P-Channel GaAs MESFET

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DRAIN CURRENT TRANSIENT CHARACTERIZATION OF P-CHANNEL GaAs MESFET

1. INTRODUCTION

The metal-semiconductor field-effect transistor (MESFET) was proposed by Mead in 1966 and subsequently fabricated by Hooper and Lehrer using a GaAs epitaxial layer on semi-insulating (SI) GaAs substrate [1, 2]. The MESFET is basically a voltage-controlled resistor. A metal-semiconductor rectifying contact is used for the gate electrode. The basic advantages of GaAs MESFETs include a higher electron velocity, leading to smaller transit time and fast response, and semi-insulating GaAs substrates, which allow one to decrease the parasitic capacitance and simplify the fabrication process.

Since their introduction, GaAs MESFETs have occupied an important niche in the microwave industry [3, 4]. GaAs MESFET amplifiers, oscillators, and switches are widely used and the monolithic microwave integrated circuits (MMICs) based on GaAs MESFET have been developed. High speed digital integrated circuits(ICs) is another very promising application of GaAs MESFETs [5-7]. The gate delays as short as 15ps for logic based on self-aligned GaAs MESFETs at 300K have been achieved.

Apart from the basic advantages mentioned above, GaAs has other properties which make it attractive:

• It is more radiation hard than silicon, and this is an advantage for defence and space applications.

• GaAs ICs can be operated at higher temperatures than their silicon counterparts; a factor of interest to the nuclear and automotive industries.

• GaAs and its related ternary and quaternary compounds can be used as lasers and photodetectors. Thus it is possible to envisage integrated optoelectronic chips which can be interconnected by optical fibre.

For integrated circuit processing, MESFETs are typically fabricated by direct ion implantation into a semi-insulating GaAs substrate [8]. Due to the materials and processing methods used in GaAs MESFET fabrication, there are some general properties with the device, such as backgating or side-gating effect [9], frequency-dependent transient effects [10-12], and low-frequency oscillations [13]. These properties are often intimately related to deep level defects in the substrate materials or the interface states [14].

Liquid encapsulated Czochralski (LEC) semi-insulating GaAs is one of the most commonly used substrate materials. The high resistivity in these materials is achieved by charge compensation of shallow donor, acceptor levels and deep levels [15]. The concentrations of deep levels are carefully controlled by doping and growth ambient, and they can be as high as ~10E16. These highly concentrated deep level defects are essential for SI-GaAs, but they can also seriously affect the device performances.

The work described in this thesis is mainly focused on frequency-dependent transient effects, which are studied by drain current transient characterization. This method has been used to study n-channel GaAs MESFET [12]. Now we employ it to study p-channel GaAs MESFET and a temperature-dependent measurement is performed. The project topic and experimental method choice are based on the following considerations. First, from the success of complimentary circuits of silicon metal-oxide transistor (CMOS) in both digital and analog IC design, people start thinking about the possibility of implementing the same technique to GaAs MESFET. The conventional GaAs circuits are using either depletion mode MESFETs or enhancement mode MESFETs. Most of the devices are n-channel ones due to the high saturation velocity of

electrons in GaAs. To realize complimentary circuits, p-channel MESFETs must be employed. Secondly, previous studies were mostly on n-channel devices. For IC design, a precise device model is very necessary and a better understanding of the specialities of p-channel MESFET is fundamental for developing correct device models. Thirdly, output conductance is a very important parameter in circuit design. The output conductance frequency dispersion and drain current transient are basically the same effect observed in either frequency domain or time domain. We choose the time domain approach because transient responses give us more information about deep levels than frequency responses. The current transients are caused by thermal emission and capture processes so that a temperature-dependent measurement can give us better understanding of these processes.

The organization of this thesis is as follows: Chapter II describes the physics and theoretical models for GaAs MESFET and explains the causes of drain current transient. Section 2.1 introduces two DC characteristic models for GaAs MESFET: a basic gradual channel model and followed by a practical "square law" model. Section 2.2 contains background knowledge on electron and hole thermal emission and capture processes around deep trap levels and the origins of drain current transients. Chapter III shows device structure and experimental setups. Chapter IV presents the results and followed by an analysis in Chapter V. The last chapter, Chapter VI concludes this thesis with summary of present work, relevant issues concerning p-channel GaAs MESFET drain current transient, and suggestions for future work.

2. REVIEW OF MESFET OPERATION AND TRAP EFFECTS ON DRAIN CURRENT TRANSIENT

2.1 MESFET Operation

2.1.1 Introduction

A field effect transistor was analyzed by W. Shockley in early 1950s [16,17]. A schematic diagram showing a metal-semiconductor field-effect transistor is presented in Fig. 2-1-1. The Schottky barrier depletion region under the gate controls the cross section of the conduction channel, modulating the channel conductivity and hence the drain-to-source current (drain current). We consider here a p-channel MESFET. In the normal operation mode, the Schottky barrier must be reversely biased. This means for a p-channel device the gate bias voltage V_{gs} is positive with respect to source (or slightly negative but without turning on the gate Schottky diode) and the drain bias voltage V_{ds} is negative with respect to source.

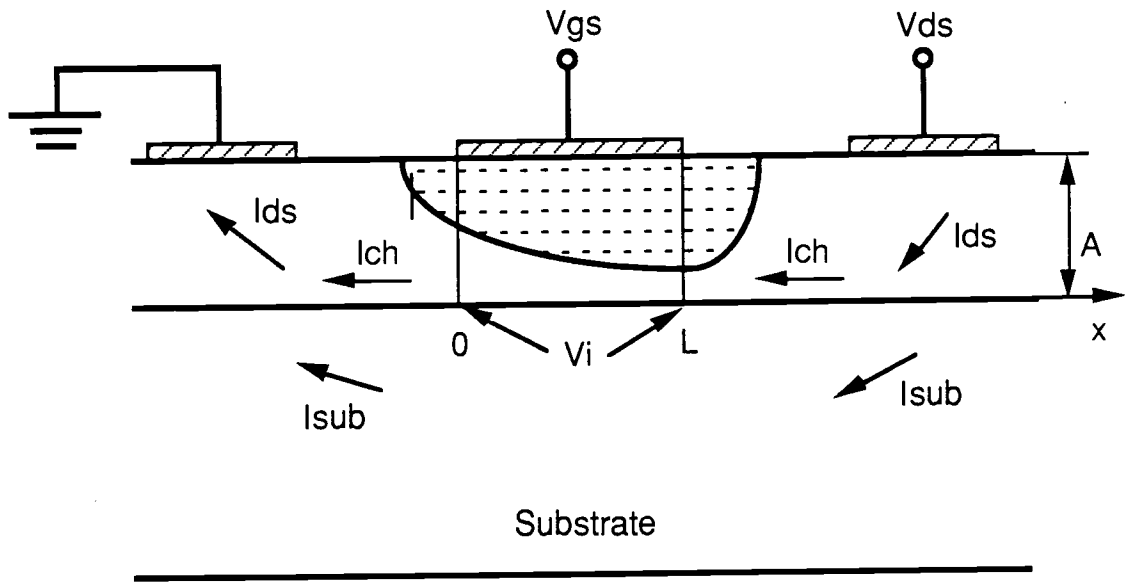


Fig. 2-1-1 Cross section of GaAs MESFET

The depletion region is wider close to the drain because the reverse bias voltage across the channel-to-gate depletion layer is larger there.

When the gate voltage V_G becomes greater than

$$V_T = -V_{po} + V_{bi} \qquad (2\text{-}1\text{-}1)$$

the current practically drops to zero, thus V_T is defined as threshold voltage. Here V_{po} is the pinch-off voltage

$$V_{po} = \frac{-qN_a A^2}{2\varepsilon} \qquad (2\text{-}1\text{-}2)$$

V_{bi} is the built-in voltage which is caused by Fermi-level pinning at surface, A is the channel thickness width (see Fig. 2-1-1), and N_a is the effective acceptor density, which we assume to be equal to the hole concentration p in the undepleted portion of the channel. For simplicity we assume a uniform doping profile.

When V_G is smaller than V_T the increase in drain-to-source voltage $|V_{ds}|$ above the saturation voltage $|V_{ds}|_{sat}$ leads to current saturation.

2.1.2 Gradual channel model

There are a number of models describing the I-V characteristics of MESFETs [16,18-20]. A simple model, which people usually use to introduce the operation of a MESFET, is the so called Shockley model based on gradual channel approximation [16]. This model assumes the drift velocity of conduction carriers

$$v = \mu F \qquad (2\text{-}1\text{-}3)$$

is proportional to the longitudinal electric field F up to the point where the channel is pinched off at the drain side of the gate, which happens when

$$V_{gs} - V_{ds} \geq V_T \qquad (2\text{-}1\text{-}4)$$

Here μ is the low field mobility.

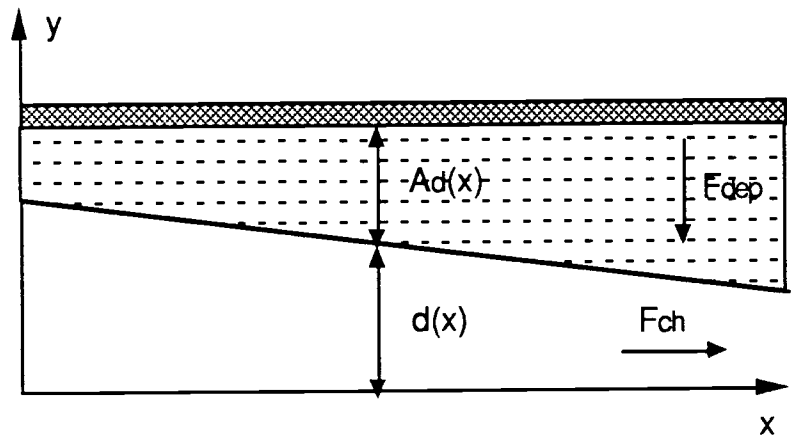
The gradual channel approximation used in this model is based on the assumption that the bias of the gate junction is a slowly varying function of position, as shown in Fig. 2-1-2. We assume that the conduction channel is neutral, the region under the gate is totally depleted, the electric field F_{ch} in the channel is in x direction, the electric field in the depleted region F_{dep} is in the y direction, the boundary between the neutral channel and the depleted region is sharp, and the potential across the channel varies so slowly that at each point the thickness of the depleted area can be found from the solution of the Poisson equation valid for a one-dimensional junction. Using such these assumptions the channel current can be written as

$$I = q v_{p0} F W [\, A - A_d(x) \,]$$

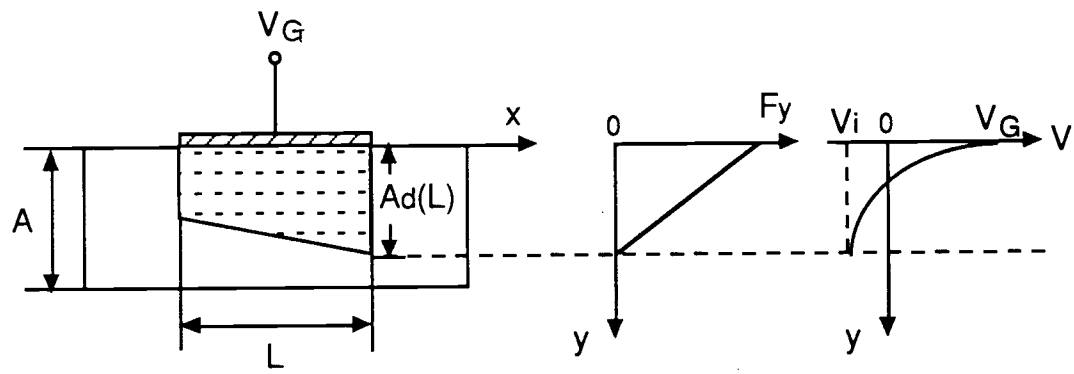
$$= q \mu N_a \left(- \frac{dV}{dx} \right) W [\, A - A_d(x) \,] \qquad (2\text{-}1\text{-}5)$$

where (-dV/dx) is the drifting field, $A_d(x)$ is the thickness of the depletion layer (see Fig. 2-1-2), and W is the gate width. $A_d(x)$ is given by

$$A_d(x) = \left\{ \frac{2\varepsilon [\, V(x) + V_{bi} - V_G \,]}{-q N_a} \right\}^{1/2} \qquad (2\text{-}1\text{-}6)$$



(a)



(b)

Fig. 2-1-2 Depletion region and conducting channel under gate. (a) Section of a gradually varying channel under gate; (b) charge, electric field and potential distributions in the depletion region.

Substituting Eq. (2-1-6) into Eq. (2-1-5) and integrating with respect to x from 0 (the source side of gate) to L (the drain side of gate), we derive the fundamental equation of MESFETs:

$$I = g_0\left\{ V_i + \frac{2}{3}\frac{\left[(-V_i+V_G-V_{bi})^{3/2} - (V_G-V_{bi})^{3/2}\right]}{(-V_{po})^{1/2}} \right\} \qquad (2\text{-}1\text{-}7)$$

where V_i is the voltage drop in the channel across the gate region,

$$g_0 = -\frac{q\mu N_a WA}{L} \qquad (2\text{-}1\text{-}8)$$

g_0 is the conductance of the channel, and L is the gate length. If we neglect the series resistances of the source and drain regions, then $V_i = V_{ds}$. Equation (2-1-7) is only valid before the channel becomes pinched off, i.e.,

$$A_d(L) \equiv A_0 \equiv \left\{\frac{2\varepsilon\,|\,V_i + V_{bi} - V_G|}{-qN_a}\right\}^{1/2} \le A \qquad (2\text{-}1\text{-}9)$$

It is assumed that when $A_d(L) = A$ (the pinch-off condition) current saturation occurs. Thus the saturation voltage $(V_i)^S_{sat}$ predicted by the Shockley model is given by

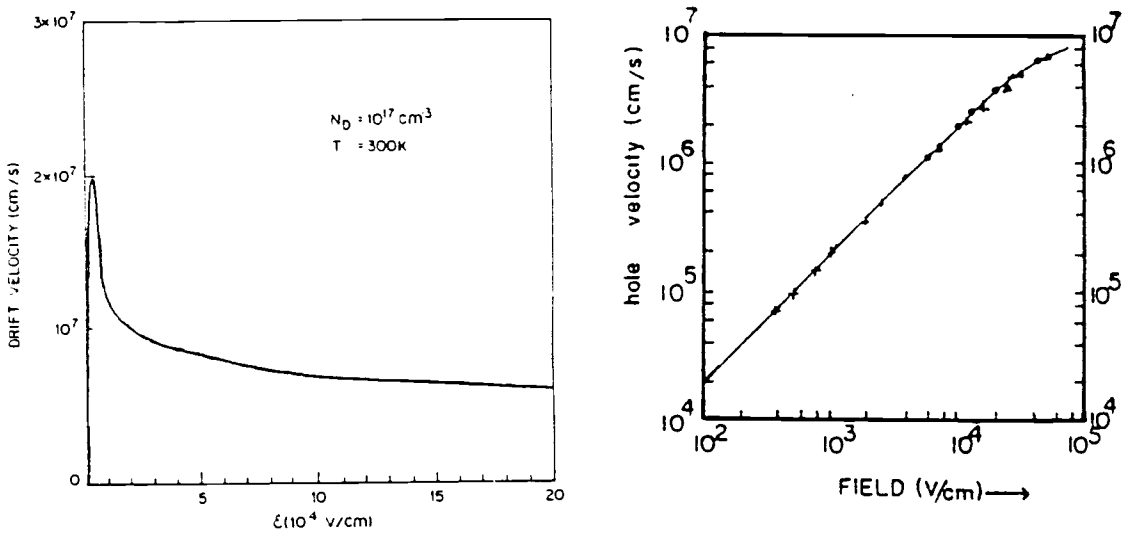
$$(V_i)^S_{sat} = V_{po} - V_{bi} + V_G \qquad (2\text{-}1\text{-}10)$$

(the index S stands for Shockley), which is in agree with Eq. (2-1-4). Substitution of Eq. (2-1-10) into Eq. (2-1-7) leads to the following expression for the saturation current:

$$(I)^S_{sat} = g_0\left[\frac{1}{3}V_{po} - \frac{2}{3}\frac{(V_G-V_{bi})^{3/2}}{(-V_{po})^{1/2}} - V_{bi} + V_G\right] \qquad (2\text{-}1\text{-}11)$$

2.1.3 "Square law" model

According to the Shockley model, current saturation occurs when a conducting channel is pinched-off at the drain side of the gate. At this point the cross section of the conducting channel is zero and hence the electron velocity has to be infinitely high in order to maintain the finite drain current. In reality the electron and hole velocity saturate in a high electric field [21,22] as shown in Fig. 2-1-3 (a,b).



(a) (b)

Fig. 2-1-3 (a) Electron velocity vs. electric field in GaAs (after P. Smith, M. Inoue, and J. Frey in Ref: 21) and (b) Hole velocity vs. electric field in GaAs (after V. L. Dalal in Ref: 22)

For electron the drift velocity first reaches a peak value and then decreases toward a constant velocity of about 7 x 10^6 cm/s at 300K. The hole drift velocity saturates close to 1 x 10^7 cm/s. The velocity saturation field for hole is considerably larger than that for electron. This field dependence of carrier mobility is very important in field effect transistors. Many theoretical models have been developed based on this concept. For GaAs MESFETs, the current saturation is actually caused by drift velocity saturation instead of channel pinch-off.

Next we introduce the "square law" model [18]. This model provides an accurate description of GaAs MESFETs with low pinch-off voltages (less than 2V or so for GaAs devices with a 1-μm gate) and an approximate description of GaAs MESFETs with higher pinch-off voltages.

We use a simple approximation for the field dependence of carrier velocity by assuming that the velocity is proportional to the electric field until the value of the saturation velocity v_S is reached at $F = F_S$ and then becomes constant (Fig. 2-1-4) [19]:

$$v = \begin{cases} \mu F, & F < F_S \\ v_S, & F \geq F_S \end{cases} \qquad (2\text{-}1\text{-}12)$$

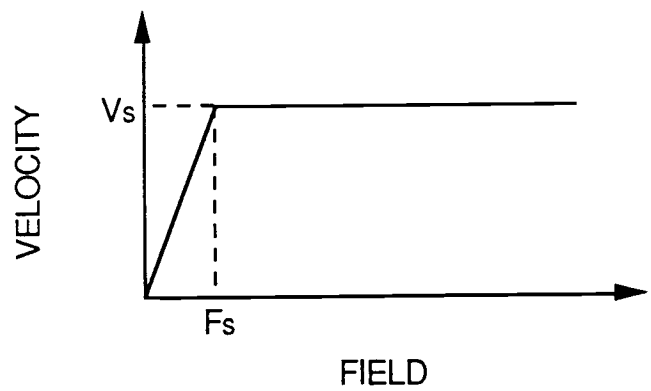


Fig. 2-1-4 Simplified velocity-electric field dependence

The velocity saturation is first reached at the drain side of the gate when

$$F(L) = - (dV(x) / dx) |_{x=L} = F_S \qquad (2\text{-}1\text{-}13)$$

where F(L) is the electric field in the conducting channel at the drain side of the gate.

When $|V_{ds}|$ is smaller than the saturation voltage, the electric field in the channel can be found according to Shockley model. Substituting Eq.(2-1-6) and Eq.(2-1-7) into Eq.(2-1-5) we get,

$$-\frac{dV(x)}{dx} = -\frac{V_{po}}{L}\left\{\frac{u_i + \frac{2}{3}\left[(-u_i+u_G-u_{bi})^{3/2}-(u_G-u_{bi})^{3/2}\right]}{1-\left[-u(x)+u_G-u_{bi}\right]^{1/2}}\right\} \qquad (2\text{-}1\text{-}14)$$

where $u_i = V_i / (-V_{po})$, $u(x) = V(x) / (-V_{po})$, $u_G = V_G / (-V_{po})$ and $u_{bi} = V_{bi} / (-V_{po})$ are the normalized voltages. The saturation voltage is then determined from Eq.(2-1-13),

$$F_S = -\frac{V_{po}}{L}\left\{\frac{u_{sat}+\frac{2}{3}\left[(-u_{sat}+u_G-u_{bi})^{3/2}-(u_G-u_{bi})^{3/2}\right]}{1-\left[-u_{sat}+u_G-u_{bi}\right]^{1/2}}\right\} \qquad (2\text{-}1\text{-}15)$$

where $u_{sat} = V_{sat} / (-V_{po})$. When $F_S << (-V_{po}) / L$, which corresponds to the short channel and relative high pinch-off voltage case, the saturation voltage has a simple form:

$$V_{sat} = F_S L \qquad (2\text{-}1\text{-}16)$$

This shows the velocity saturation. The opposite limitation, $F_S >> (-V_{po}) / L$, gives V_{sat} the same expression of Eq. (2-1-10), which is result of Shockley model.

The saturation current is given by

$$I_{sat} = -qN_a v_s W [A - A_d(L)] \qquad (2\text{-}1\text{-}17)$$

where the depletion width $A_d(L)$ at the drain side is given by

$$A_d(L) = A\left(-u_{sat} + u_G - u_{bi}\right)^{1/2} \qquad (2\text{-}1\text{-}18)$$

Substituting Eq.(2-1-18) into Eq.(2-1-7) I_{sat} becomes

$$I_{sat} = g_0 F_s L\left[1 - \left(-u_{sat} + u_G - u_{bi}\right)^{1/2}\right] \qquad (2\text{-}1\text{-}19)$$

In the short channel limitation, $F_s << (-V_{po}) / L$, this reduces to

$$I_{sat} = g_0 F_s L\left[1 - \left(u_G - u_{bi}\right)^{1/2}\right] \qquad (2\text{-}1\text{-}20)$$

or

$$I_{sat} = I_0\left[1 - \sqrt{\frac{V_G - V_{bi}}{-V_{po}}}\right] \qquad (2\text{-}1\text{-}20a)$$

where $I_0 = g_0 F_s L = -q \mu F_s N_a W A$. It can be shown that in the opposite limitation, $F_s >> (-V_{po}) / L$, Eq. (2-1-19) reduces to Shockley model result, Eq. (2-1-11).

There is an another commonly used expression for I_{sat} in computer simulation models such as the SPICE model, which is derived for JFET [23],

$$I_{sat} = \frac{I_0}{1 + 3 F_s L / (-V_{po})}\left[1 - \frac{V_G - V_{bi}}{-V_{po}}\right]^2 \qquad (2\text{-}1\text{-}21)$$

or in a general form

$$I_{sat} = \beta (V_G - V_T)^2 \qquad (2\text{-}1\text{-}21a)$$

when we recall $V_T = - V_{po} + V_{bi}$, and choose the transconductance parameter

$$\beta = \frac{2\varepsilon\mu v_s W}{A\left(\mu V_{po} + 3v_s L\right)} \qquad (2\text{-}1\text{-}22)$$

Eq.(2-1-20a) and Eq.(2-1-21a) appear to be quite different; however, in most cases, they are quite similar. This can be seen by the following illustration. Assume a MESFET exactly follows Eq.(2-1-20a). Fig. 2-1-5 is a graph of $\sqrt{I_{sat}/I_0}$ as a function of $(V_G-V_{bi})/(-V_{po})$. Notice that it is nearly a linear function between ordinate values of 0.1 and 0.9.

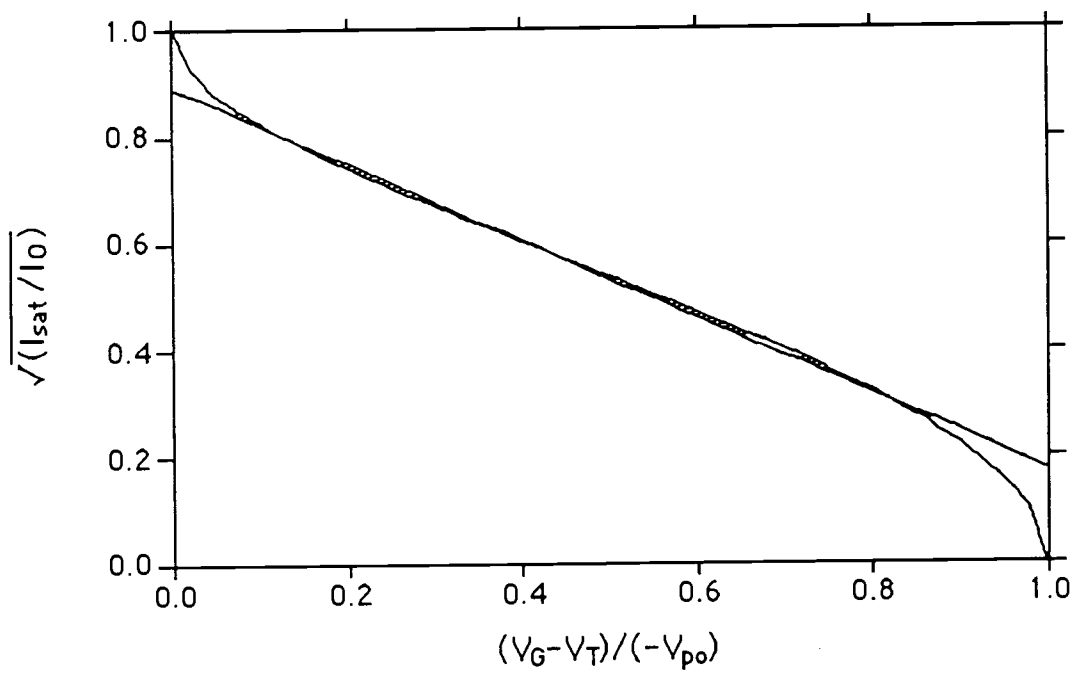


Fig. 2-1-5 Values of $\sqrt{I_{sat}/I_0}$ as a function of gate bias voltage for MESFETs obeying Eq.(2-1-20a). The straight line has expression as Eq.(2-1-23)

The straight line approximation shown in Fig. 2-1-5 has the following equation

$$I_{sat} = 0.8\, I_0 \left[1 - \frac{V_G - V_{bi}}{1.25(-V_{po})} \right]^2 \qquad (2\text{-}1\text{-}23)$$

This equation is simply Eq.(2-1-21) with I_0 and V_{po} multiplied by constants. These constants have no significance since I_0 and V_{po} would be determined from experimental data for $I_{sat}(V_G)$. Eq.(2-1-21) or Eq.(2-1-21a) is the basic equation for the "square law" model.

The analysis above only applies to the values of the drain current at the onset of the current saturation when the carrier velocity becomes equal to the saturation velocity at the drain side of the gate. At higher V_{ds} the electric field in the conducting channel increases, leading to velocity saturation in lager fraction of the channel. Thus, with larger V_{ds}, the effective gate length L_{eff} is smaller than L and I_{sat} increases according to Eq.(2-1-21a). This is the so called gate length modulation effect. Careful field distribution analysis also shows that high V_{ds} can affect the effective channel opening. As indicated in Lehovec and Miller's paper [24], the channel opening is reversely proportional to the effective gate length L_{eff}. This means that higher V_{ds} produces a larger channel opening, which also increase I_{sat}. Combining all these effects a general formula, I_{ds} can written as

$$I_{ds} = I_{sat} (1 + \lambda V_i) \tanh (\alpha V_i) \qquad (2\text{-}1\text{-}24)$$

where I_{sat} is given by Eq.(2-1-21), α and λ are constants, and V_i is the voltage drop across the channel. The hyperbolic tangent function makes this equation useful even below saturation. This is the more general form for the "square law" model.

Up to now we did not consider the source and drain series resistances R_s and R_d. If we incorporate them into the "square law" model, the gate-to-source voltage V_{gs} is given by

$$V_{gs} = V_G + I_{sat} R_s \qquad (2\text{-}1\text{-}25)$$

The drain-to-source voltage V_{ds} is given by

$$V_{ds} = V_i + I_{sat} (R_s + R_d) \qquad (2\text{-}1\text{-}26)$$

Eq.(2-1-21a) and Eqs.(2-1-24)-(2-1-26) form a complete set of equations of the analytical "square law" model.

2.2 Drain Current Transients of GaAs MESFET

2.2.1 Deep trap levels in semi-insulating GaAs

Since most GaAs integrated circuits are fabricated directly on semi-insulating GaAs substrates, the deep trap levels introduced into the substrates during growth will affect the device performance. Drain current transient is one of the effects.

High resistivity GaAs material is achieved by liquid encapsulated Czochralski (LEC) growth without intentional doping [15]. This technique has been extensively studied and several models have been developed to explain the high resistivity property of the resulting material [15, 25-27]. Here we consider the three-level model [15], which consists of a shallow donor N_{SD}, a deep donor N_{DD}, and a shallow acceptor N_{SA}. Carbon is the main source of shallow acceptors. A very heavily concentrated deep level, labeled as EL2, is the deep donor level. The shallow donor is attributed to unintentionally incorporated impurities such as S and Si. The requirement for semi-insulating material is then

$$N_{SA} > N_{SD} \tag{2-2-1}$$

$$N_{DD} > (N_{SA} - N_{SD}) \tag{2-2-2}$$

Considering the charge neutrality condition for SI GaAs material, the electron concentration n is given by

$$n = N_{SA} - N_{SD} - N_{DD}^{+} \tag{2-2-3}$$

Using Fermi-Dirac distribution, the ionized deep donor concentration is given by

$$\frac{N_{DD}^{+}}{N_{DD}} = 1 - \left\{ 1 + \frac{1}{2} \exp\left[-\left(\frac{E_F - E_{DD}}{k_B T} \right) \right] \right\}^{-1} \qquad (2\text{-}2\text{-}4)$$

At room temperature this ratio is about 0.02 [14]. N_{DD} is approximately $2\times10^{16}\,cm^{-3}$ so that $N_{DD}^{+} \approx 4\times10^{14}\,cm^{-3}$. Returning back to Eq.(2-2-3), n can clearly be ignored and we obtain

$$N_{DD}^{+} = N_{SA} - N_{SD} \qquad (2\text{-}2\text{-}5)$$

From this equation we can see that the charge balance in SI material is established by two types of fixed charges; that due to shallow and deep impurity levels. The deep level plays an important role in semi-insulating GaAs.

2.2.2 Emission and capture processes at a trap level

Before discussing current transient, an introduction of the emission and capture processes at a trap level is necessary. Let us consider a trap level with energy E_T. Only thermal stimulated processes are considered here. Fig. 2-2-1 shows the possible processes.

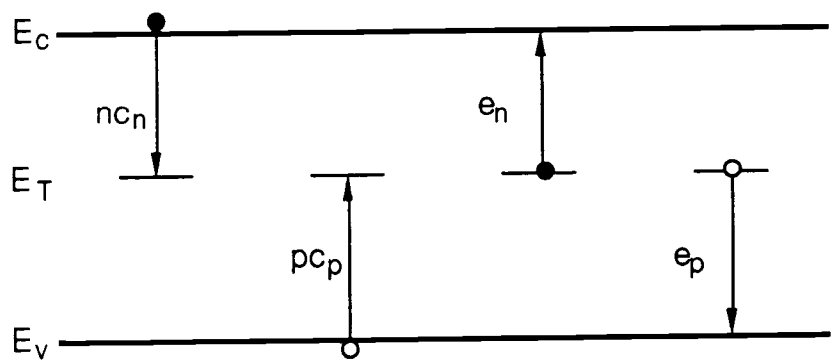


Fig. 2-2-1 Emission and capture processes at a deep level of energy E_T. The quantities near the arrows are the rates (in s^{-1}) of the processes.

The subscripts n and p denote electron and hole transitions. The symbol e is an emission rate, c a capture constant, n and p the concentrations of free electrons and holes in the conduction band (at energy E_c) and valence band (at energy E_v).

The rate of n_T, the density of traps occupied by a hole, is

$$dn_T / dt = (p\, c_p + e_n) (N_T - n_T) - (n\, c_n + e_p)\, n_T \qquad (2\text{-}2\text{-}6)$$

where N_T is the total density of traps, c_n and c_p are capture constants for electron and hole, and e_n and e_p are emission rates respectively.

The thermally activated emission rate for holes can be written as

$$e_p = (\sigma_p \nu_{th} N_v / g) \exp(-\Delta E_a / k_B T) \qquad (2\text{-}2\text{-}7)$$

where σ_p is capture cross section of the trap, $\nu_{th}=\sqrt{3k_B T/m_p}$ is the average thermal velocity of a hole, $N_v = 2(2\pi m_p k_B T/h^2)^{3/2}$ is the density of states in the valence band edge, where k_B is Boltzman constant, g is the degeneracy of the deep level, and $\Delta E_a = E_T - E_v$ is the activation energy of the trap level. The capture constant for hole is proportional to the capture cross section

$$c_p = \sigma_p \nu_{th} \qquad (2\text{-}2\text{-}8)$$

Then the corresponding time constants for emission and capture, τ^e and τ^c can be expressed as

$$\tau^c = (\sigma_p \nu_{th} N_v / g)^{-1} \exp (\Delta E_a / k_B T) \qquad (2\text{-}2\text{-}9)$$

and

$$\tau^c = (\sigma_p v_{th} p)^{-1} \qquad (2\text{-}2\text{-}10)$$

Similar equations hold for electron if we replace p by n in the subscripts, N_v by conduction band edge density of states N_c, and $\Delta E_a = E_c - E_T$.

2.2.3 The channel-substrate interface

In our discussion of GaAs MESFETs we have neglected so far the effects related to junction between the active channel and the semi-insulating substrate beneath the channel. In fact, a finite depletion region exists at this interface in the channel side. The space-charge distribution for the channel-substrate interface resembles that of a p-n junction; negative charge due to ionized acceptors on the channel side of the interface is balanced by positive charge on the substrate side of the interface. Here we follow the discussions in Wager and McCamant's paper [14].

The origin of the positive charge on substrate side can be understood, for LEC GaAs, in terms of the three-level model. To form this space-charge region, holes (majority carriers) must be injected across the interface barrier (high-level injection) and trapped in the deep level EL2, which increases the density of ionized EL2 and exposes positive space charge to the negative charge in channel side. Fig. 2-2-2 shows the band diagram and charge distribution for channel-substrate interface.

The relative depletion widths of the channel W_c and the substrate W_s are determined by charge balance condition for the interface

$$N_a W_c = N_{DD} W_s \qquad (2\text{-}2\text{-}11)$$

If N_a is approximately 10^{17} / cm^3 and $N_{DD} \approx 2 \times 10^{14}$ /cm^3, we find that $W_s \approx 500 W_c$ and the interface depletion region is very similar to an abrupt p^+-n junction where the depletion region exists mostly on low doped side.

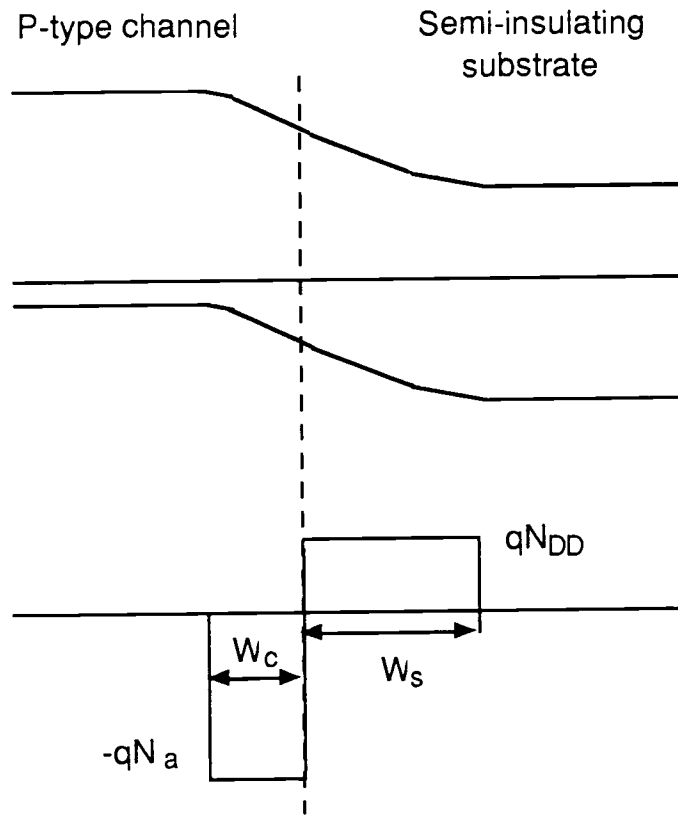


Fig. 2-2-2 The band diagram and charge distribution for channel-substrate interface

Notice there are still some fundamental differences between the channel-substrate interface and a p-n junction. A p-n junction is a bipolar device consisting of regions where electrons and holes are majority carriers. In contrast, the channel-substrate interface is a unipolar device in that holes are majority carriers on both sides. Charge neutrality is established by balance of free carriers and fixed charges from ionized shallow impurities for a p-n junction on both sides, and for the channel-substrate interface, as we mentioned above, by only fixed charge balance on the substrate side. Another distinguishing feature of p-n junction compared with the channel-substrate interface is the time response associated with the change of the space-charge region

thickness. For a p-n junction this is corresponds to the dielectric relaxation time which normally quite short. The response time for the channel-substrate interface is much longer and corresponds to the capture or emission time of a hole from EL2 or the dielectric relaxation time, whichever is longer.

2.2.4 Effects of deep trap levels on GaAs MESFET drain current transient

Considering the results in previous sections, now let us discuss about the drain current transient effect. Look at the I-V curve of a p-channel GaAs MESFET (Fig. 2-2-3). Assume we change the drain bias from V_1 to V_2, the current should follow from I_1 to I_2.

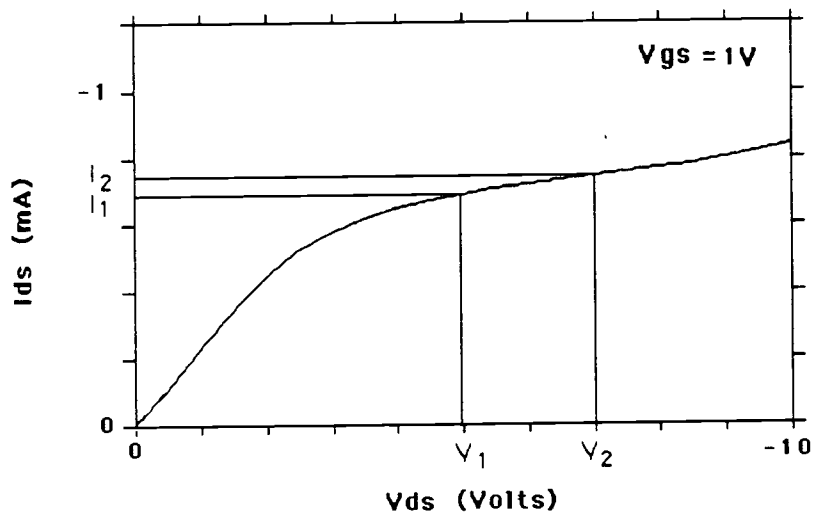


Fig. 2-2-3 I-V curve of a p-channel GaAs MESFET. I_1 and I_2 are drain currents at drain biases V_1 and V_2, respectively.

In reality, this current change is not a simultaneous response. The carriers in the channel need to travel from source to drain to establish the new current level. This delay is called transit time. For a 1-μm p-channel device, the transit time is about $1\mu m / v_s(p) \approx (1 \times 10^{-4}\ cm)/(10^7\ cm/s) = 10ps$. In the measured response, we see the drain current first overshoot above the steady-state value and then decay back with a very long time constant ($\Delta t \gg 10ps$), as shown in Fig. 2-2-4. This is the drain current transient we are interested in. From the following analysis, we will see that this kind of current transient is caused by deep trap levels in the channel or in the substrate side of channel-substrate interface.

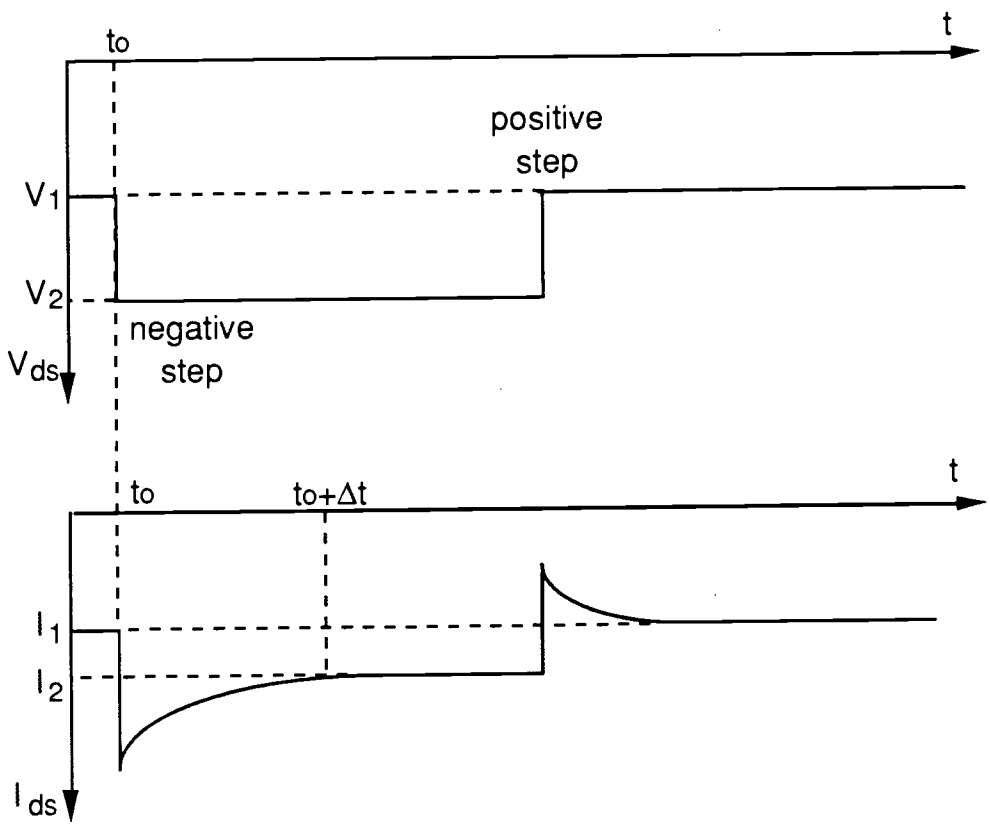


Fig. 2-2-4 Drain current response to step drain bias change

Fig. 2-2-5 shows the band diagram of a p-channel MESFET. Under equilibrium there are no holes in both the gate depletion region and the depletion region on the channel side of the channel-substrate interface, so that the EL2 levels in these regions is not filled with holes and thus they are not ionized. In the channel the EL2 levels are filled with holes and they are positively charged. On the substrate side of the interface the EL2 levels trap holes injecting from the channel so that they are also positively charged and form the space-charge region.

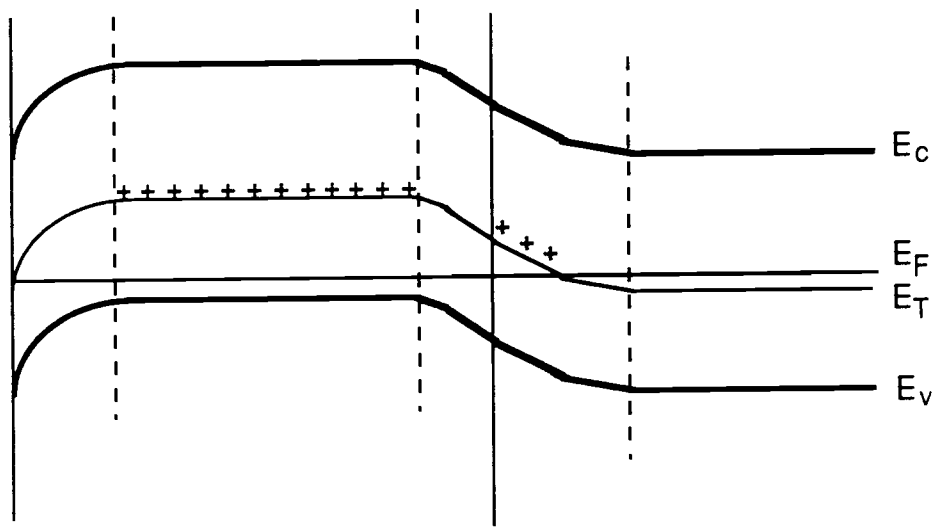


Fig. 2-2-5 Band diagram of a p-channel GaAs MESFET. E_c and E_v are the conduction band and valence band respectively. E_F is the Fermi level and E_T is the deep trap level, i.e. EL2.

We assume $|V_2| > |V_1|$ and V_1 changes to V_2 at $t = t_0$ (negative step), the depletion region under the gate near the drain side increases due to the increase of reverse bias of the Schottky barrier on this side. When the depletion region expands, the

originally ionized EL2 levels fall into the depletion region and contribute some positive charges. To generate the necessary voltage drop, the depletion region has to expand more than without these positive charges. This is equivalent to a higher drain bias voltage applied and from the I-V curve we can see a larger current (absolute value) is expected. This explains the overshoot in the drain current response curve. The holes trapped in the EL2 levels inside the depletion region eventually emit and the depletion region width changes to the steady-state case with a time constant of emission, as does the current.

When we change drain bias voltage from V_2 to V_1 (positive step), the opposite process happens with the depletion region under the gate. The depletion region near the drain side decreases due to the decrease of reverse bias of the Schottky barrier on this side. Some EL2 levels without trapping holes are pushed out from the depletion region and they are exposed to holes. They will capture holes and become positively charged. To compensate this positive charge the depletion region needs to increase a bit. If we remember that smaller depletion width on drain side means smaller drain bias voltage hence smaller drain current, then we can describe the drain current response as first a decrease followed by a change back to the steady-state value with a time constant of capture, as shown in Fig. 2-2-4.

The the space-charge region of the channel-substrate interface has the same effect on the value of drain current. As we recall from section 2-2-3, the depletion region exists mostly on the substrate side which is formed by hole injecting into the substrate and captured by EL2. When the drain bias changes from V_1 to V_2, the depletion region expands. This means that more holes need to be captured by the EL2 levels in the substrate. This transient will be characteristic by the capture time constant of hole. Similarly, when the drain bias changes form V_2 to V_1, the current transient is

characteristic by the emission time constant of hole. Table 2-2-1 summarizes the processes causing the drain current transients.

The object of this work is to study the deep trap levels effects on p-channel GaAs MESFET through drain current transients.

Table 2-2-1 The processes causing the drain current transients

	Negative step	Positive step
Channel region	Hole emission	Hole capture
Substrate	Hole capture	Hole emission

3. EXPERIMENT

3.1 Device Structure

The device used in this experiment was fabricated by TriQuint Semiconductor, Inc. [28] and has the following geometric structure (Fig. 3-1-1a,b).

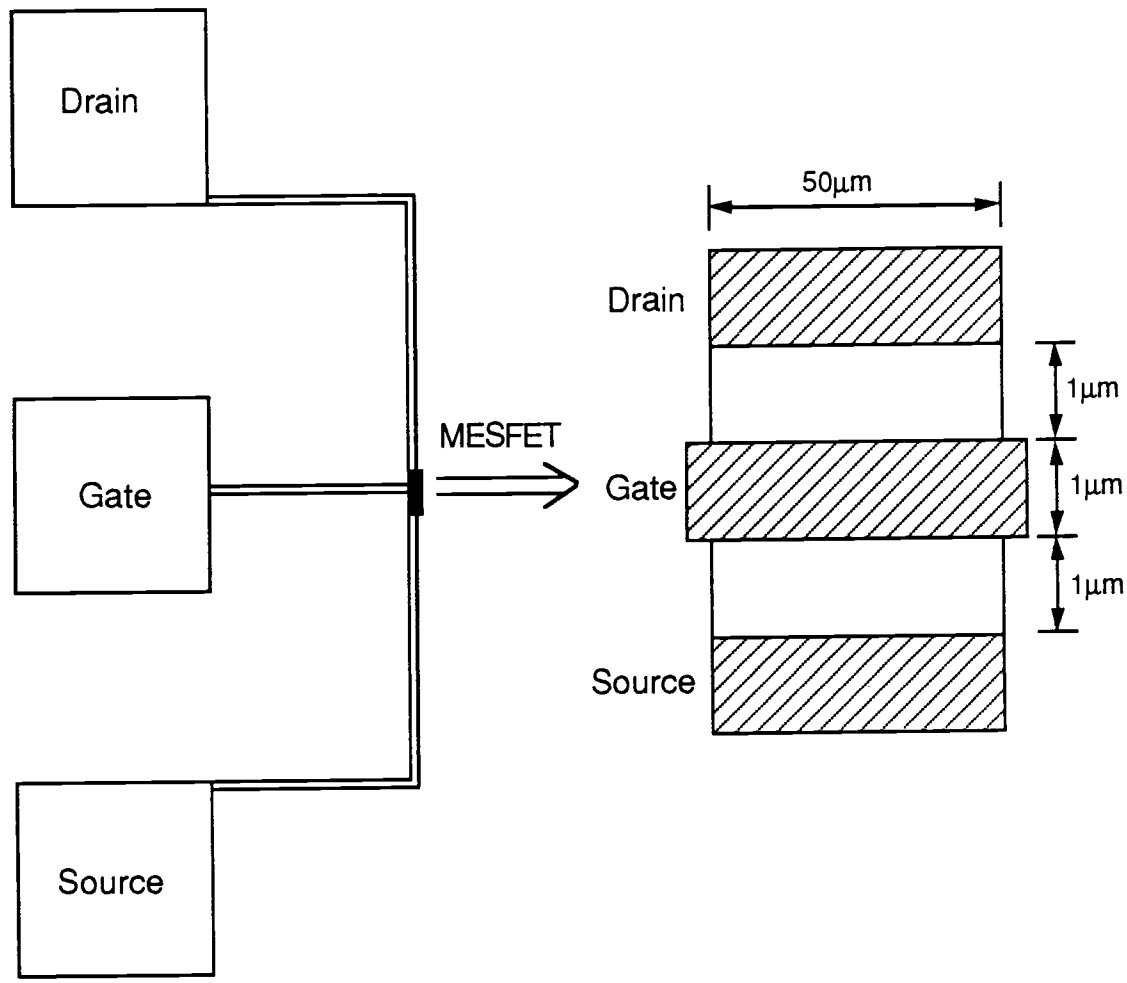


Fig. 3-1-1a Over looking view of the p-channel MESFET

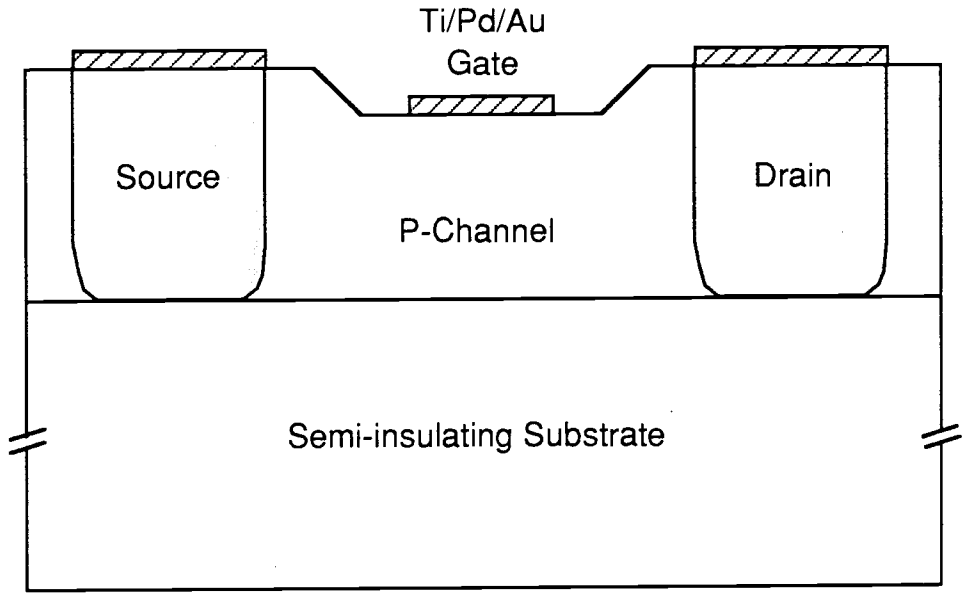


Fig. 3-1-1b Cross section view of the p-channel MESFET

This is a standard non-self-aligned structure, which means a separated mask was used to define the source and drain regions and there are spaces between the gate and the source or the gate and the drain. The gate length, gate-source separation and drain-source separation are all 1μm. The gate width is 50μm. All contact pads are 100μm x 100μm.

The device was fabricated on an undoped liquid encapsulated Czochralski (LEC) <100> SI-GaAs substrate with $\rho \sim 10^7\ \Omega$ cm by ion implantations. The channel region was formed by beryllium implantation at energy 140 keV with a dose of 2.3×10^{12} cm^{-2}. The doping profile is shown in Fig. 3-1-2. The peak concentration is about 5×10^{16} cm^{-3} in the channel. The gate region was back etched to adjust the threshold voltage. A Schottky barrier was then formed by using E-beam evaporation of Ti/Pd/Au. The whole wafer is 3 inches in diameter and contains 58 identical dies.

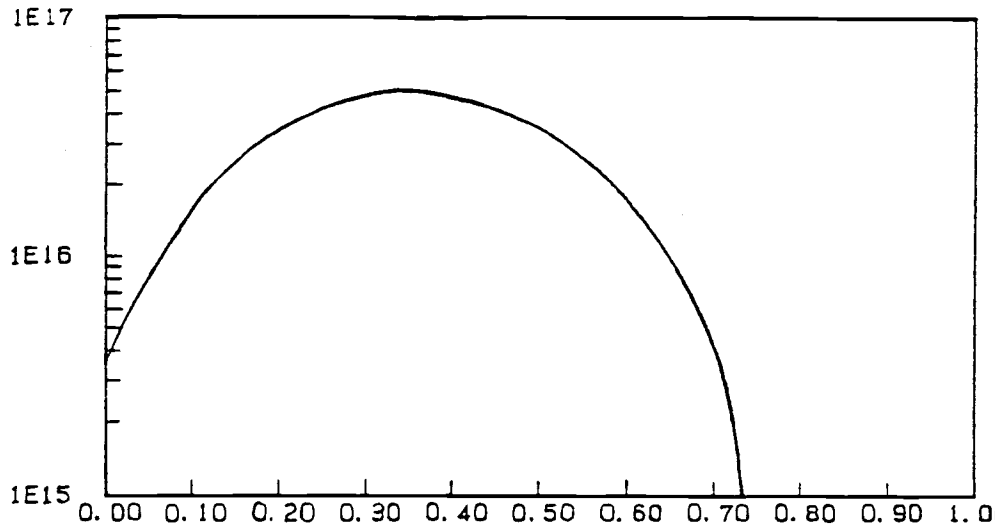


Fig. 3-1-2 Channel doping profile. Be implantation at energy 140 keV with a dose of 2.3×10^{12} cm^{-2}

3.2 DC Characterizations

To perform drain current measurements, we have to specify certain bias conditions for the device. Furthermore we have to know the current and voltage levels so that proper experimental instrument and techniques can be determined. So we need to

know the DC characteristics of our device first. We measured the I-V curve and threshold voltage of the p-channel GaAs MESFET.

A Hewlett-Packard Model 4145B Semiconductor Parameter Analyzer was used to characterize the DC performance of the device. The HP 4145B is a fully automatic, high performance, programmable test instrument designed to measure, analyze, and graphically display the DC characteristics of semiconductor devices. It is equipped with four programmable Source/Monitor units (SMU), two programmable voltage source units (Vs), two voltage monitor units (Vm), a fully interactive graphics display, removable flexible-disc storage, softkeys, full arithmetic keyboard, and HP-IB (GPIB). For device stimulation and characteristics measurement, the 4145B has eight channels. Channels 1 through 4 are Source/Monitor units (SMU); channels 5 and 6 are voltage source units (Vs); and channels 7 and 8 are voltage monitor units (Vm). Since our device is a three terminal device, we only use three of the four SMU channels, which are channels 1 through 3. Each SMU channel has three modes of operation: voltage source/current monitor (V), current source/voltage monitor (I), and common (COM). Source voltage and source current can be held constant or swept linearly or logarithmically. We connect drain, gate and source to SMU1, and SMU2 and SMU3, respectively. SMU1 and SMU2 are in V mode. SMU3 is in COM mode which means the source is grounded.

To measure I_{ds} dependency of V_{ds} at different gate bias, we define V_{ds} as variable 1 and V_{gs} as variable 2, then linearly scan V_{ds} in a desired range with a fine step (e.g. 0.1 V) and change V_{gs} with a fixed step (e.g. 0.5 V).

To measure I_{ds} dependency of V_{gs} at a certain drain bias, we define V_{gs} as variable 1 and V_{ds} as variable 2, then linearly scan V_{gs} in a desired range with a fine step (e.g. 0.1 V) and hold V_{gs} to a constant (e.g. -7 V). If we assume the I-V characteristics obeying "square law" model and neglect the source and drain resistances, the threshold

voltage can be determined from the intercept of $\sqrt{abs(I_{ds})} - V_{gs}$ curve according to Eq.(2-1-21a) when the device is biased in saturation region. Fig. 3-2-3. shows this concept.

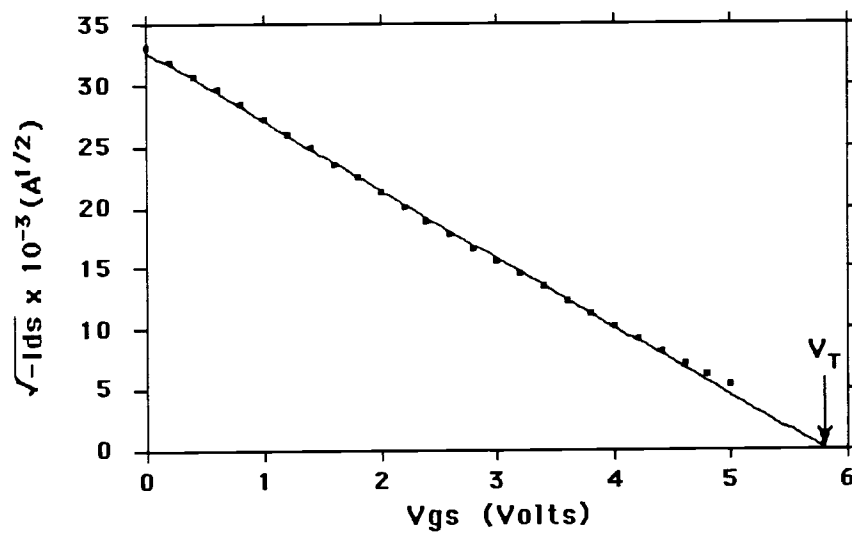


Fig. 3-2-3 Threshold voltage V_T extracted from $\sqrt{abs(I_{ds})} - V_{gs}$ curve according to "square law" model

3.3 Drain Current Transient Characterization

To measure the drain current we actually measure the voltage drop across a sense resistor R_S, as shown in Fig. 3-3-1. The choice of the resistance value is based on the following considerations: it has to be much smaller than the drain output impedance so that most of the voltage drops across the transistor; and it has to be sensitive enough to pick up the transient signal. The value we chose is 10.2 Ω.

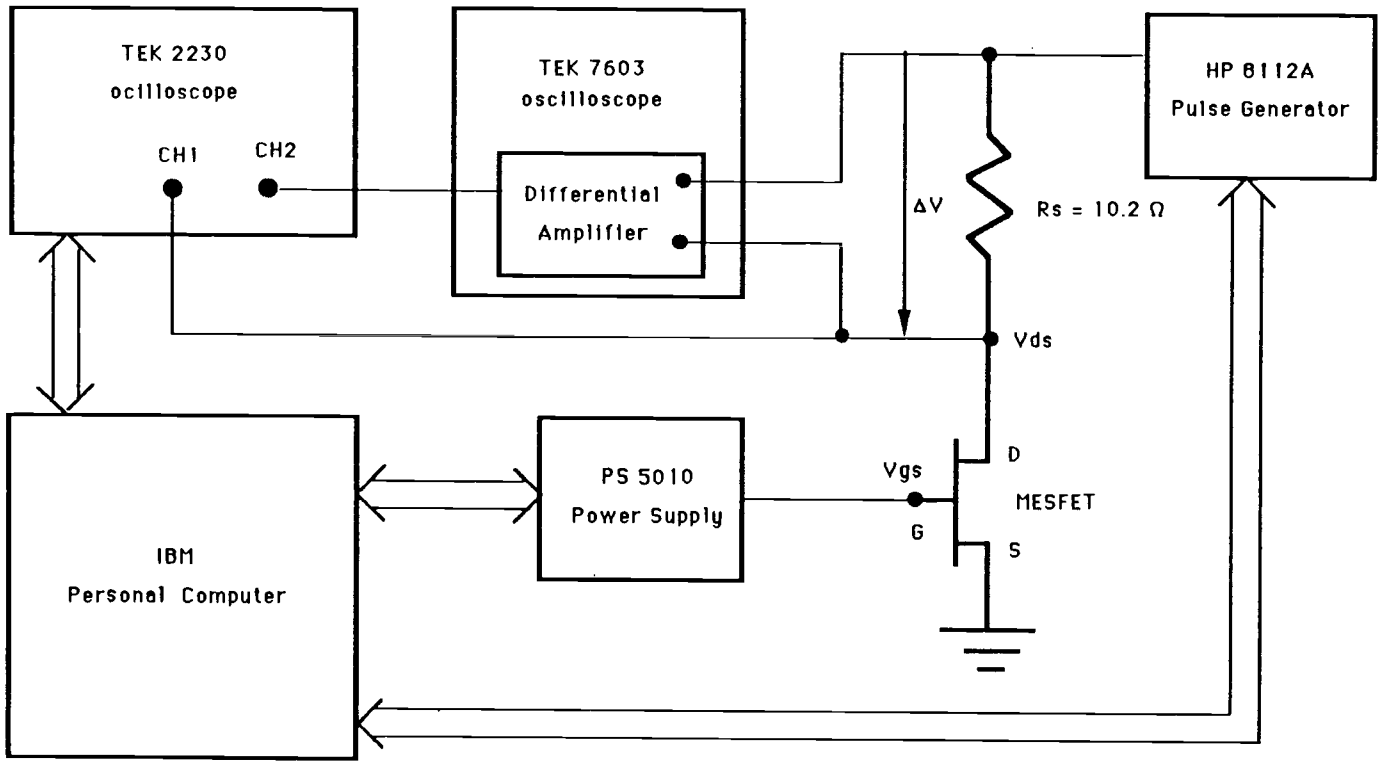


Fig. 3-3-1 Experimental Setup for Drain Current transient Measurement

The whole setup is depicted in Fig. 3-3-1. The wafer is placed on a probe stage. Coaxial cables are used to connect the probes and input/output of instrument to avoid noise and time delays. We use a TEK PS 5010 programmable power supply to bias the gate and an HP 8112A pulse generator to supply the step bias on the drain. The drain current signal, which is actually the voltage drop across R_S, is first picked up by the differential amplifier of a TEK 7603 oscilloscope. The output of this oscilloscope then enters channel 2 of a TEK 2230 digital oscilloscope, which is connected to an IBM PC through GPIB bus. Channel 1 of the TEK 2230 is the actual drain bias voltage. The computer also connects to PS5010 power supply and HP 8112A pulse generator. All experimental data are taken by computer and formatted into proper data files. The limitation of this setup is determined by the response time of the differential amplifier, which is 1μs.

There are several considerations for the choice of step voltage. First we want to compare transient data to output conductance frequency-dependent data which are usually small signal responses. So we try to make the step as small as possible. Second we want to keep the device operating in saturation region. So we choose the step from -6V to -7V which keep the device in saturation for any gate bias. The step rise and fall times are chosen to be much smaller than the differential amplifier response time which is 1μs.

Temperature dependency of drain current transient is one of the most effective ways to study the deep trap level effects. We did the measurement from room temperature to 90°C. The temperature change is realized by a hot chuck in the probe stage. We control the temperature by changing the voltage of a power supply for the hot chuck. To cool down the temperature we run tap water through the hot chuck. The temperature of the probe stage is measured by a Type-J thermocouple which is made of iron-constantan.

4. RESULTS

4.1 DC Characteristic Results

Fig. 4-1-1 is the measured I-V curve at room temperature. We can see that this is a depletion mode device. The breakdown voltage is above -10V. When the gate bias approaches V_T, the breakdown tends to happen at lower $|V_{ds}|$. We will discuss this in Chapter V.

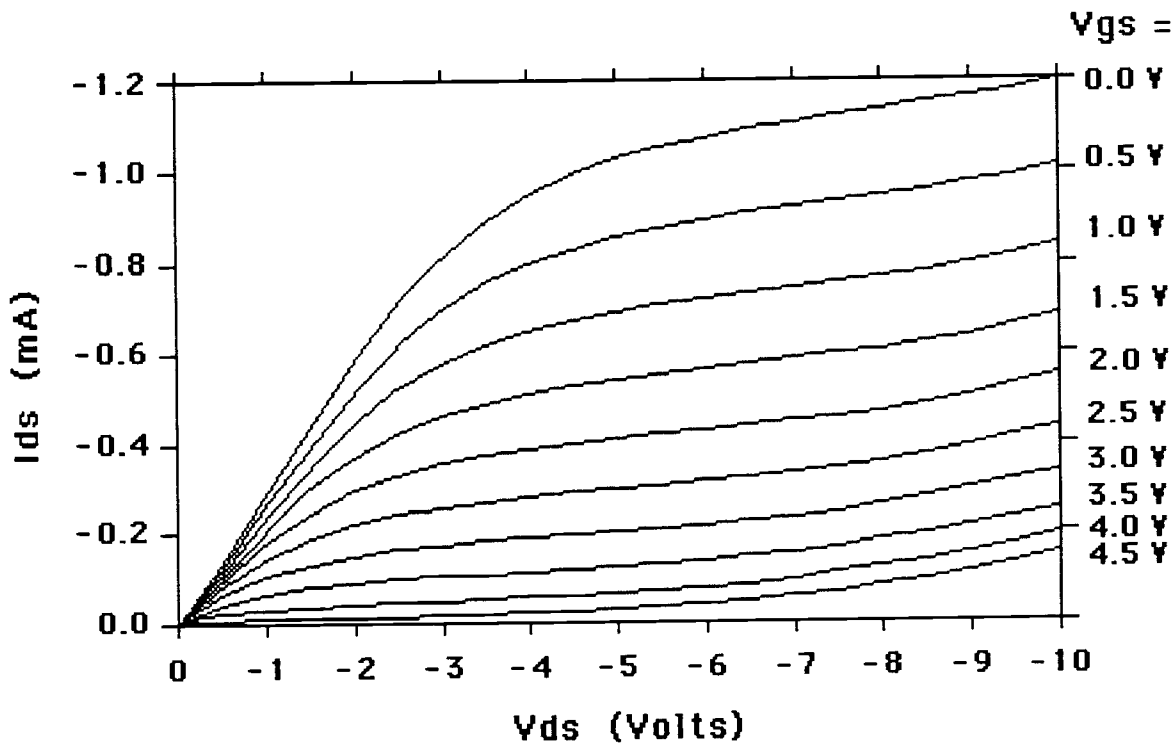


Fig. 4-1-1 Measured I - V curve for p-channel GaAs MESFET

Fig. 4-1-2 shows the I-V_{gs} curve at V_{ds} = -7V and room temperature. From both Fig.4-1-1 and Fig. 4-1-2 we know the threshold voltage at room temperature is about 5 volts. If we assume that this device follows the "square law" model and we neglect the drain and source resistances, as pointed out in the previous chapter, we can determine the threshold voltage from the intercept of $\sqrt{abs(Ids)} - V_{gs}$ curve. Using this method we measured V_T under different temperatures and different drain biases, which are shown in Fig. 4-1-3 and Fig. 4-1-4 respectively. The threshold voltage does not change very much in 40°C - 90°C range. At room temperature it is about 1 volt higher. The threshold voltage changes with gate bias, too. It can be represented by a linearity dependency.

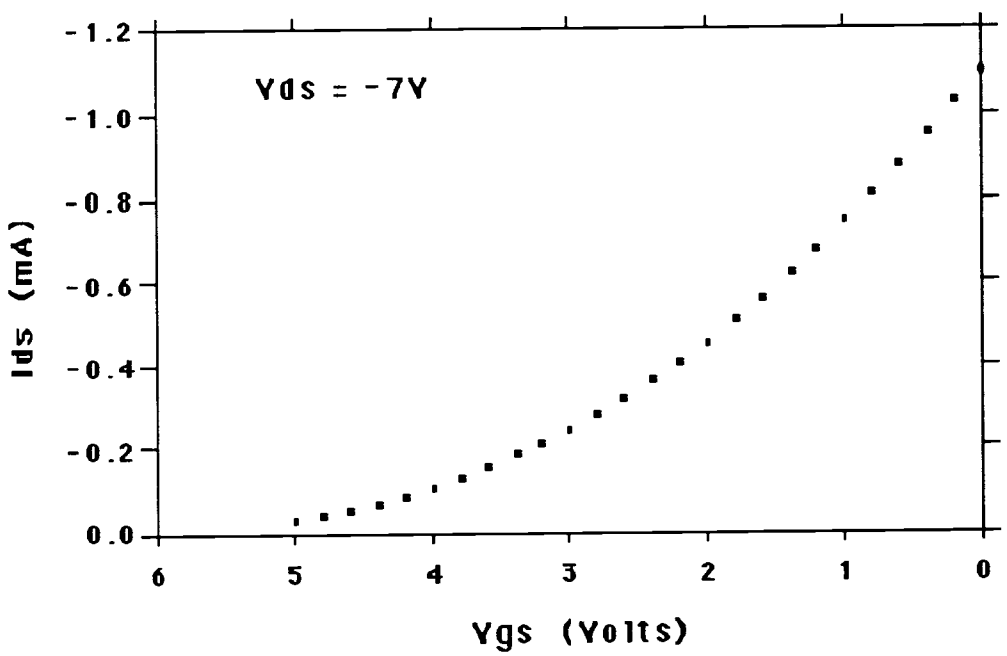


Fig. 4-1-2 Measured I - V_{gs} curve for p-channel GaAs MESFET at V_{ds} = -7V

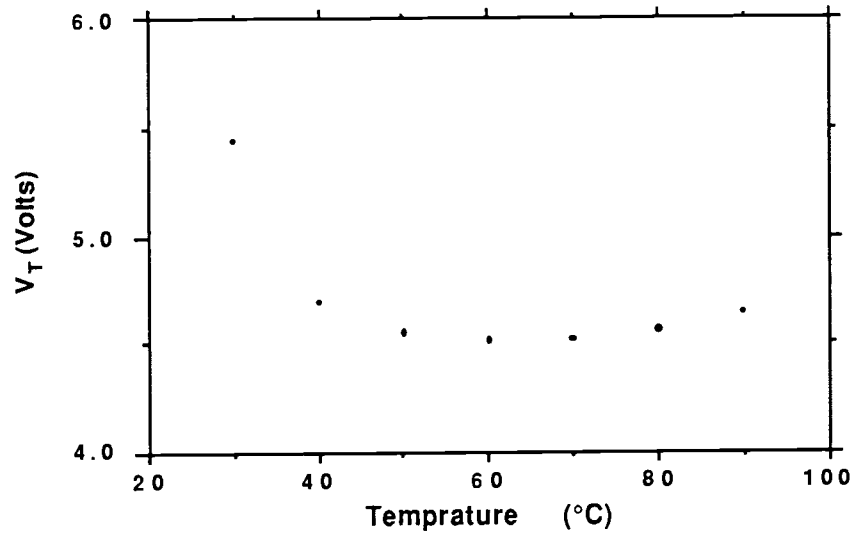


Fig. 4-1-3 Temperature dependency of threshold voltage at bias V_{ds} = -7V

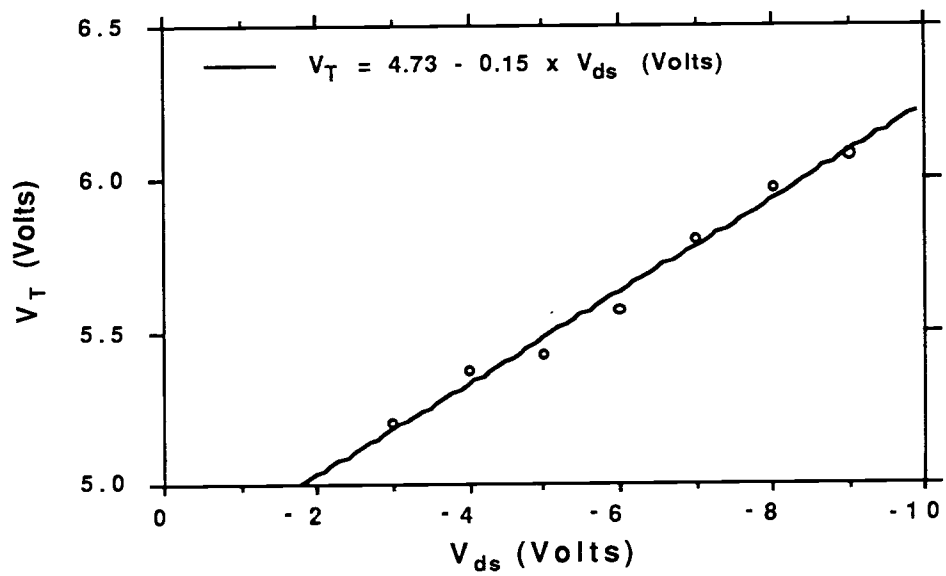


Fig. 4-1-4 Threshold voltage at different drain biases and at room temperature

4.2 Drain Current Transient Results

We measured drain current transients for drain step bias from -7V to -6V (positive step) and from -6V to -7V (negative step). Fig. 4-2-1 shows one of the measured curves. We define the change of I_{ds} as ΔI_{ds} , which is composed of two parts: the overshoot part ΔI_{ds1} and the steady-state change ΔI_{ds0}.

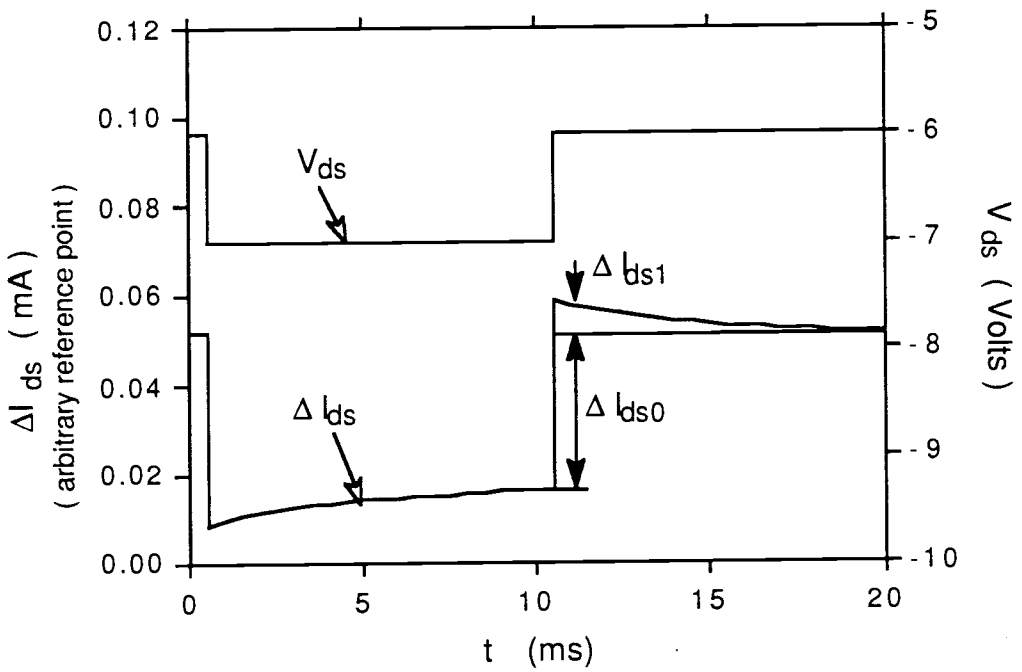


Fig. 4-2-1 Drain current response at room temperature and gate biased at 1V

Fig. 4-2-2 shows ΔI_{ds1} for different temperatures with fixed gate bias at 1V and Fig. 4-2-3 for different gate biases at room temperature. Table 4-2-1 and Table 4-2-2 are the ΔI_{ds0} values respectively. We can see from Fig. 4-2-2 that the transient time constant is very sensitive to temperature change. In the range from room temperature to 90°C, the transient time constant changes about an order for both positive step response and negative step response. Fig. 4-2-3 shows that the transient time constant is less sensitive to gate bias change but the overshoot values are increasing with increased gate bias voltage $|V_{gs}-V_T|$.

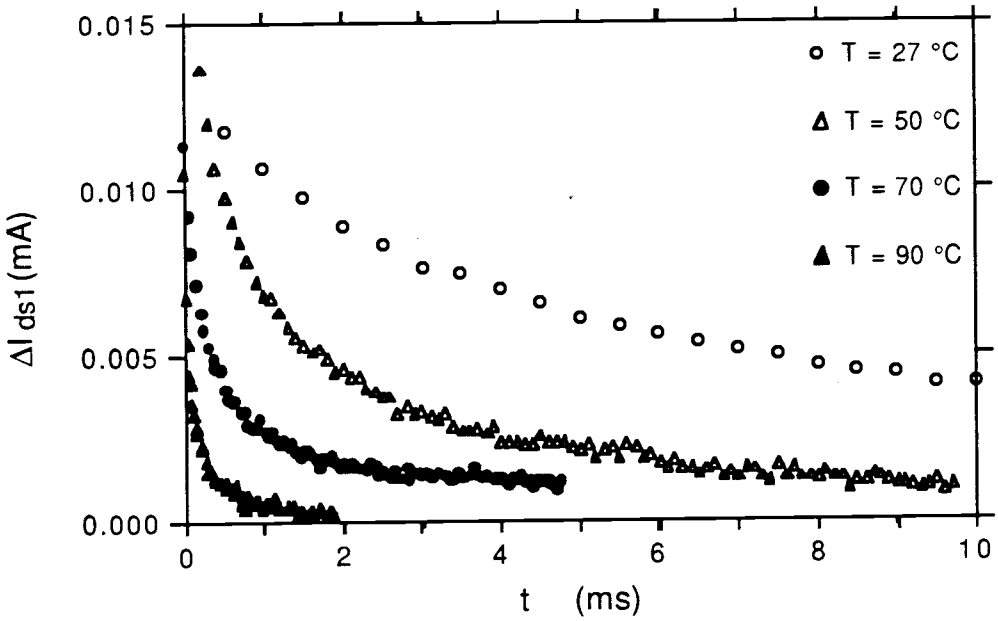
Table 4-2-1 The steady-state drain current change ΔI_{ds0} at different temperatures with $V_{gs} = 1V$

Temperature (°C)	30*	40*	50	60*	70	80*	90
ΔI_{ds0} (mA)	0.028	0.012	0.011	0.0091	0.0088	0.0080	0.0083

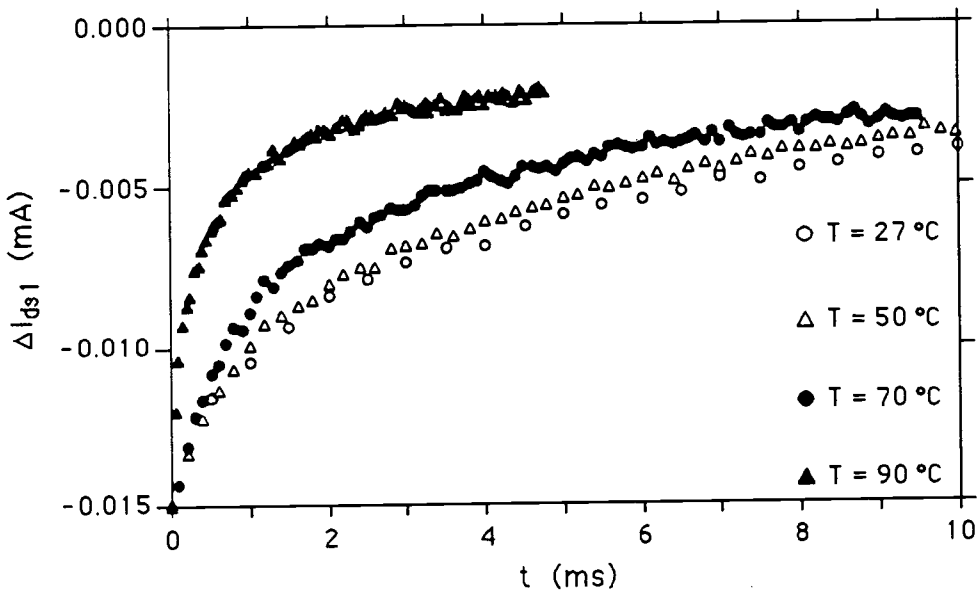
* Transients are also measured at these temperatures but the ΔI_{ds1} curves are not shown in Fig. 4-2-2

Table 4-2-2 The steady-state drain current change ΔI_{ds0} under different V_{gs} at room temperature

V_{gs} (Volts)	0.0	0.5	1.0	1.5	2.0	2.5	3.0
ΔI_{ds0} (mA)	0.025	0.021	0.018	0.014	0.012	0.0087	0.0061



(a)



(b)

Fig. 4-2-2 ΔI_{ds1} for different temperatures with gate biased at 1V. (a) response to positive step V_{ds}: -7V -> -6V; (b) response to negative step V_{ds}: -6V -> -7V

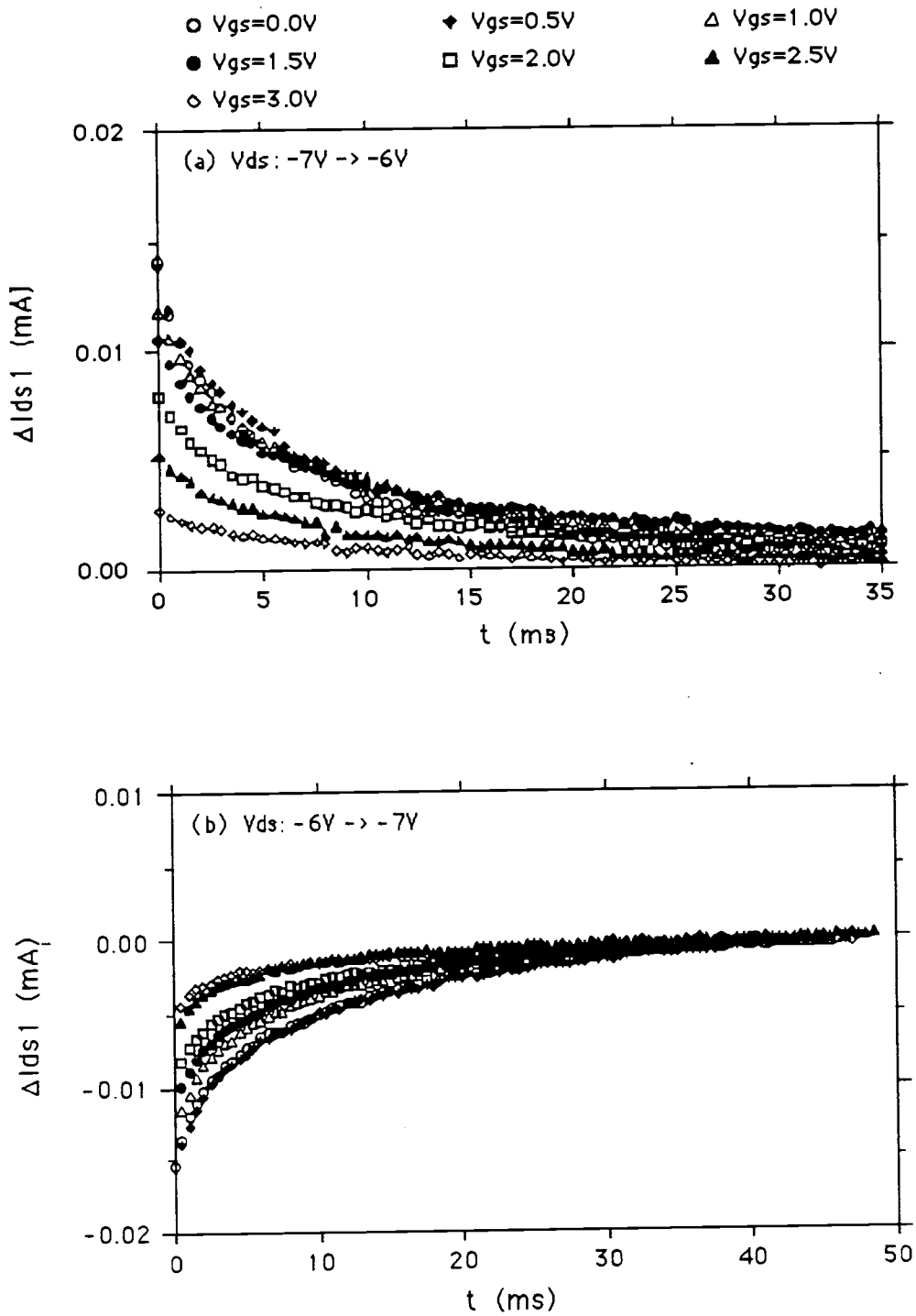


Fig. 4-2-3 ΔI_{ds1} for different gate biases at room temperature. (a) response to positive step V_{ds}; (b) response to negative step V_{ds}

5. ANALYSIS

5.1 DC Characteristics

In this section we will discuss the DC characterization results of the p-channel MESFET. From the discussion we will see that the bias conditions we chose for the transient measurements are reasonable.

5.1.1 The value of threshold voltage V_T

As shown in last chapter, the threshold voltage V_T of this p-channel GaAs MESFET is about 5V at room temperature, which is relatively high. When we recall the relationship between threshold voltage and pinch-off voltage V_{po} (the voltage needed to deplete the whole channel) from chapter two, Eq.(2-1-1), we know that they only differ by a sign and a built-in voltage V_{bi}, which is about 0.6V for p-type GaAs(ref). So higher V_T means higher V_{po} (the absolute value), which implies that the channel of the MESFET is hard to deplete. This can be understood by the the relatively low doping level of the channel.

These devices are built on the same wafer with a number of other devices. The fabrication processes are usually standard for a company so that it is not feasible to choose optimum process conditions for each individual device. The channel implantation of this p-channel MESFET is the same as the well implantation for a n-channel MESFET. The implantation energy is relatively high and dose is relatively low, which makes the doping profile deeper and peak value lower. This gives a higher pinch-off voltage (see Eq.(2-1-2)).

5.1.2 The breakdown voltage

The breakdown voltage of this p-channel MESFET is above -10V and tends to have lower breakdown voltage for higher gate biased, as shown in Fig. 4-1-1.

The breakdown happens as the gate Schottky junction breaks down, which can be caused by either avalanche multiplication or tunneling mechanism [29]. The breakdown usually first occurs at the drain side since the reverse bias at this side is the highest. When the gate bias voltage V_{gs} approaches threshold voltage V_T, or $|V_{gs}-V_T|$ approaches zero, the gate reverse bias is increasing, so smaller drain bias voltage $|V_{ds}|$ is needed to reach the breakdown.

We choose the drain step bias voltage from -6V to -7V or vice versa. These biases are used for all gate bias voltages and we know from the I-V curve that they will keep the device in saturation region and below breakdown voltages.

5.1.3 Threshold voltage V_T as a function of temperature and drain bias voltage

From the previous chapter we know that the threshold voltage V_T is a function of both temperature and drain-to-source bias voltage. This means that we can only define a value for V_T for specific conditions. But when we do the transient measurement, we do not want to change the bias condition (e.g. $|V_{gs}-V_T|$) too much as we adjust some other parameter (e.g. temperature), or we want to control the bias condition (e.g. knowing $|V_{gs}-V_T|$ or knowing V_T). So it is necessary to know how the threshold voltage changes with temperature and drain-to-source voltage.

In Fig. 4-1-3 we see that the threshold voltage does not change very much in the temperature range 40°C - 90°C. But when cooled to room temperature the threshold voltage starts to increase. Let us rewrite the definition for threshold voltage:

$$V_T = -V_{po} + V_{bi} \qquad (2\text{-}1\text{-}1)$$

where V_{po} is the pinch-off voltage and V_{bi} is the built-in voltage. V_{po} is only a function of doping level and depth (see Eq.(2-1-2)). It is nearly independent of temperature. The only thing making V_T a function of temperature is the temperature dependency of V_{bi}. Fig. 5-1-1 shows us see how V_{bi} is defined.

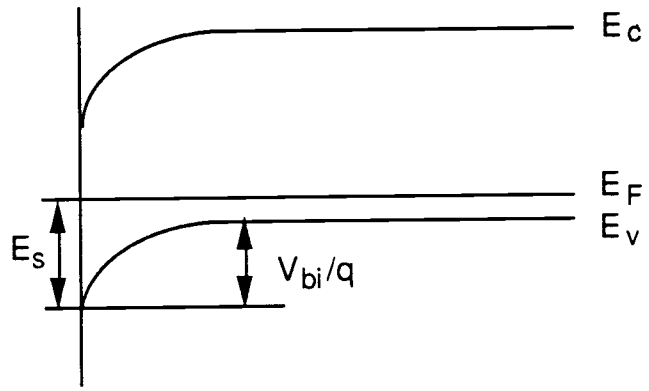


Fig. 5-1-1 The definition of built-in voltage V_{bi}. E_S is the Fermi level pinning energy on surface.

It is easy to see that the relation between built-in voltage and Fermi level position is

$$V_{bi} = qE_s - q(E_F - E_v) \tag{5-1-1}$$

where (E_F - E_v) is dependent on the hole concentration

$$p = N_v \exp\left(-\frac{E_F - E_v}{k_B T} \right) \tag{5-1-2}$$

or

$$E_F - E_V = k_B T \ln\left(\frac{N_V}{p}\right) \qquad (5\text{-}1\text{-}3)$$

If we assume that the Fermi level pinning energy E_S changes with temperature in a similar rate as the bandgap, E_S decreases about 0.026V when temperature changes from 27°C to 90°C [30].

In Eq.(5-1-3) the logarithm of N_V changes very slowly although N_V is a function of temperature ($N_V \propto T^{3/2}$). In the temperature range from 27°C to 90°C, the hole concentration mainly comes from the dopants, so we have $p \approx N_a$ which is a constant. Thus (E_F - E_V) is proportional to temperature T. According to Eq.(5-1-3), (E_F - E_V) increases 0.027V as temperature changes from 27°C to 90°C. Then the calculated change of V_T is about 0.053V in the temperature range from 27°C to 90°C. The measured values for V_T in Fig. 4-1-3 is almost a constant in the temperature range from 40°C to 90°C and has a big jump (~1V) in room temperature which may be due to experimental errors.

From these analyses we know that the threshold voltage V_T does not change very much in the temperature range from 27°C to 90°C. When we choose a constant V_{gs} under different temperatures in range from room temperature to 90°C, the gate bias condition $|V_{gs}-V_T|$ can be regarded as constant.

Although the threshold voltage is also a function of drain bias V_{ds}, as long as we keep V_{ds} constant there will be linear dependency of gate bias $|V_{gs}-V_T|$ on V_{gs}.

5.2 Temperature Dependent Drain Current Transient Characteristics

This section will discuss the temperature dependent drain current transient results. First we will introduce a one-level model for the defect in channel region and substrate region. With this model and other simplification assumptions, the transient curves are fitted and the activation energies and the capture cross sections of the defect

levels are obtained. Then we will identify the levels from available data in the literature. Finally we will discuss the the limitations of the fitting model, the differences between p-channel and n-channel GaAs MESFET transients, and how the time domain drain current transient relates to frequency dependent output conductance.

5.2.1 Fitting of drain current transient data

To interpret the drain current transient curve, we need to make several assumptions. First we assume there is only one deep trap level in both the channel region and the semi-insulating GaAs substrate. Secondly we assume that the capture time of the this deep level is much faster than the emission time and both of them are faster than the dielectric relaxation time. So we can fit the transient with only one time constant. Under these assumptions and using the discussion in Section 2.2.4, we can conclude that the non-steady-state part of the drain current change ΔI_{ds1} is due to hole emission in the substrate for positive V_{ds} step and due to hole emission in the channel region for negative V_{ds} step. It should be an exponential decay with a characteristic time constant.

Using this very simple model, we fit the current transient curves by least-square method to the following equation

$$\Delta I_{ds} = C_0 + C_1 \exp (-t / \tau) \qquad (5\text{-}2\text{-}1)$$

where C_0 is the steady-state change ΔI_{ds0}, $C_1 \exp (-t / \tau)$ is the non-steady-state change ΔI_{ds1}, and the step change of V_{ds} has to start at $t = 0$. Fig. 5-2-1 shows the fitted curves and Table 5-2-1 gives the results for different temperatures. Notice that the time constants for positive response and negative response are similar but not equal. This

could be due to a difference between the deep level in the channel and that in the substrate.

Table 5-2-1 The fitted parameters C_1 and τ under different temperatures

(a) From transient corresponding to positive step change of V_{ds}

Temperature (°C)	27	30	40	49.5	62.5	68	80	90
τ (msec)	11.3	7.12	2.71	1.52	0.780	0.467	0.243	0.123
C1 (μA)	15.4	14.5	7.47	10.9	6.48	9.20	5.72	8.73

(b) From transient corresponding to positive step change of V_{ds}

Temperature (°C)	27	40	49.5	62.5	68	80	90
τ (msec)	22.5	9.21	4.38	2.58	1.82	1.32	0.709
C1 (μA)	-15.5	-7.87	-10.1	-8.04	-11.2	-6.78	-9.44

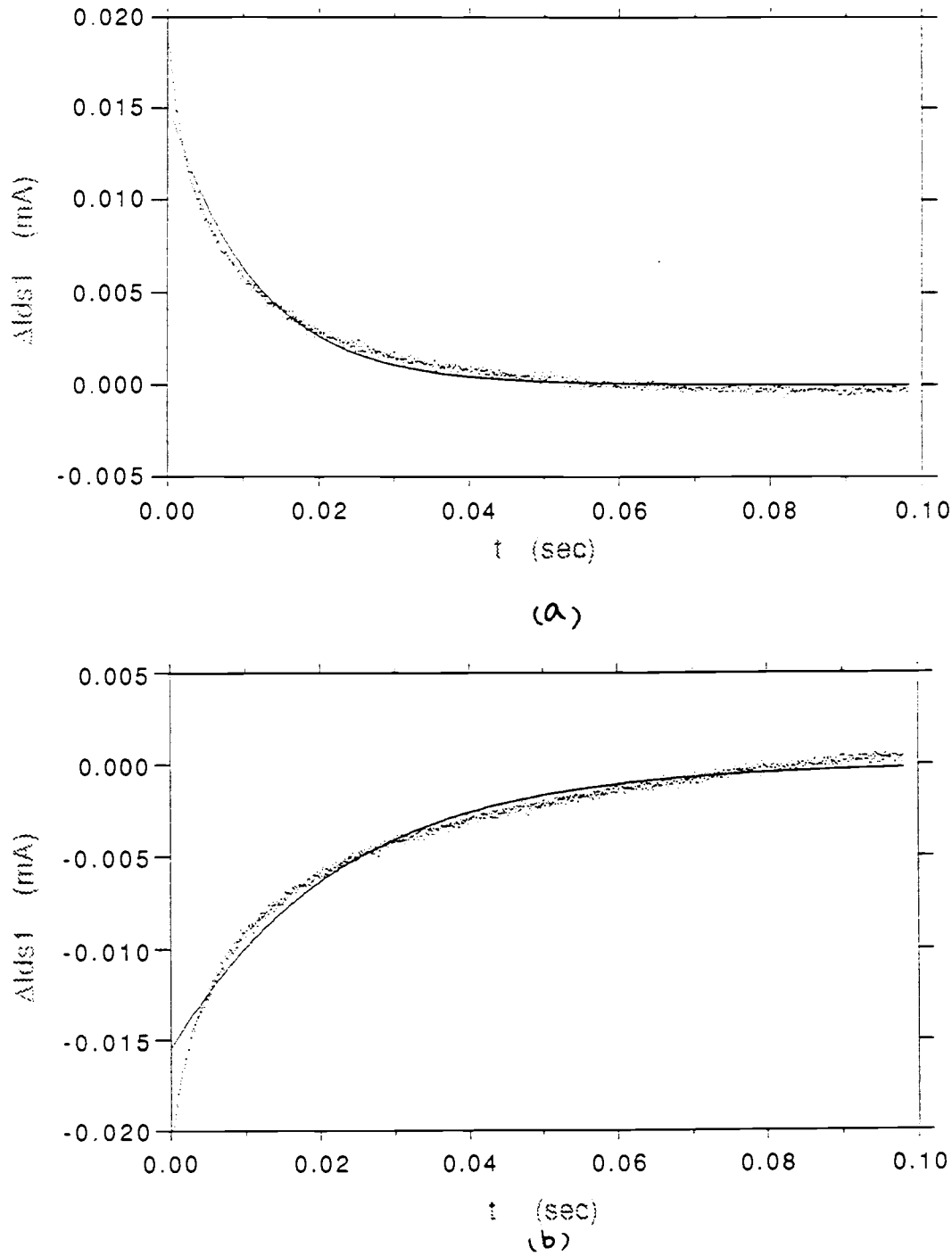


Fig. 5-2-1 The fitting of drain current transients by one-level model. The dots are measured data and the solid lines are the fitted curves. (a) response to drain voltage change from -7V to -6V; (b) response to drain voltage change from -6V to -7V

The emission time of a deep level is expressed in Eq.(2-2-9).

$$\tau^e = (\sigma_p \nu_{th} N_v / g)^{-1} \exp(\Delta E_a / k_B T) \qquad (2\text{-}2\text{-}9)$$

where $\nu_{th} = \sqrt{3 k_B T / m_p}$ is the thermal velocity of the hole and $N_v = 2(2\pi m_p k_B T / h^2)^{3/2}$ is the density of states in valence band. The temperature dependency of emission time τ^e can be further expressed as

$$\tau^e = \alpha T^{-2} \exp(\Delta E_a / k_B T) \qquad (5\text{-}2\text{-}2)$$

where α is inversely proportional to the capture cross section of the deep trap level σ_p. If we substitute all the values for constants (see Appendix I), we have this relation

$$\alpha = (1.53 \times 10^{21} \sigma_p)^{-1} \qquad (5\text{-}2\text{-}3)$$

Using Eq.(5-2-2), we can find the activation energy ΔE_a and capture cross section σ_p from the emission time constants τ^e under different temperatures. If we plot $\log(\tau^e T^2)$ vs. (1/T), we should get a straight line, as shown in Fig. 5-2-2. From the slope we get $(\Delta E_a / k_B)$ so that ΔE_a is determined. From the x-axis-intercept of this curve we get $\ln(\alpha)$ so that σ_p can be calculated by Eq.(5-2-3). The activation energies and cross sections we obtained in this method are given in Table 5-2-2.

Table 5-2-2 The activation energy ΔE_a and cross section σ_p for deep levels

	ΔEa (eV) = EDD - Ev	σ_p (cm^2)
deep level in the substrate (from positive step transient)	0.58	4.0×10^{-15}
deep level in the channel (from negative step transient)	0.43	7.5×10^{-18}

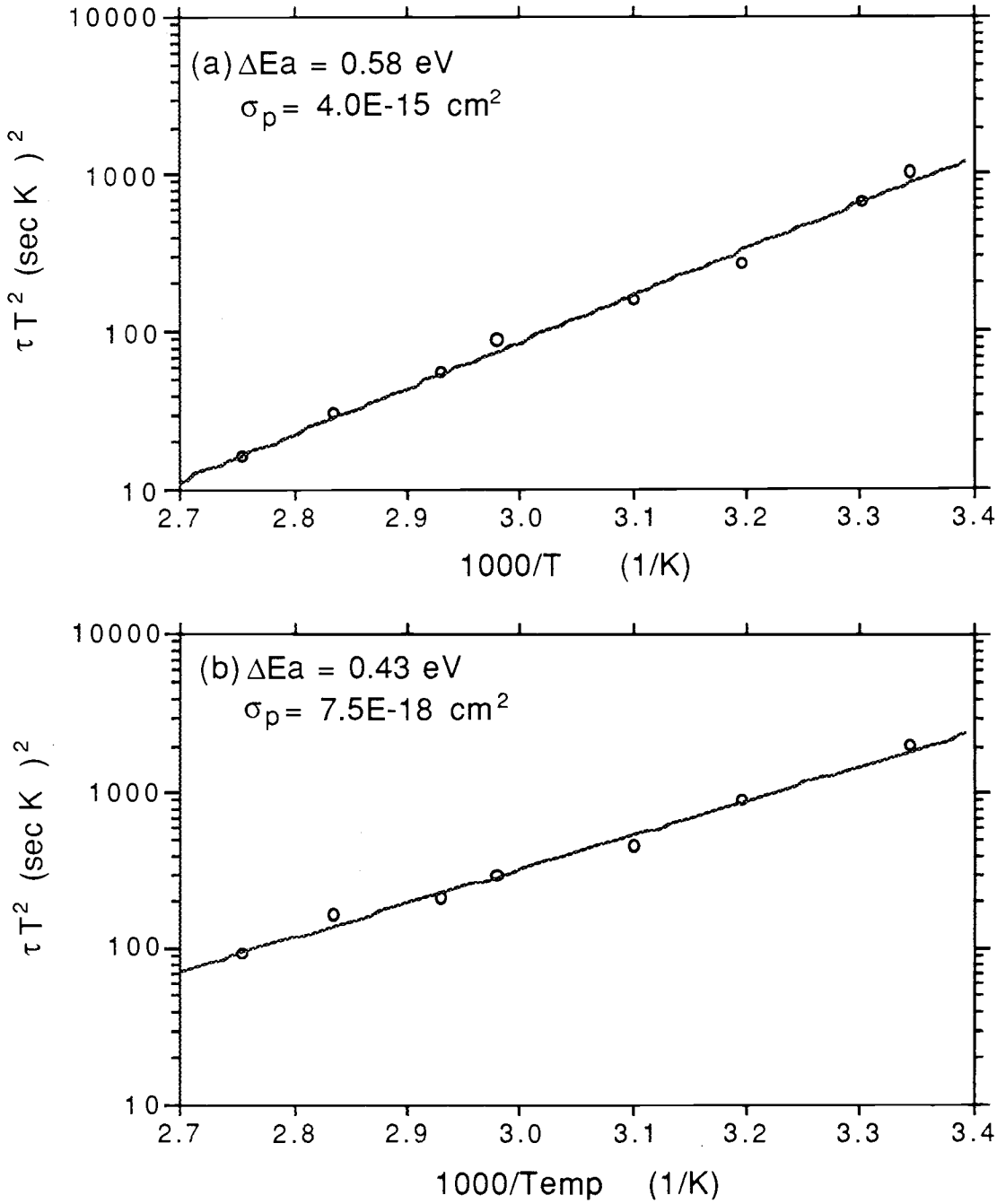


Fig. 5-2-2 ($\tau^e T^2$) vs. (1000/T) curves. Open circles are the experimental data. The straight lines are fitted curves of Eq.(5-2-2). (a) Data from positive transient; (b) Data from negative transient

5.2.2 Identification of trap levels

Now we know the activation energies and cross sections of the deep levels responsible for the drain current transients for both positive and negative step voltage of drain V_{ds}, or of the deep levels in substrate and in channel region, respectively. We related these deep levels to the EL2 defect in GaAs in Chapter II. The following discussion relates these results to previous work on EL2 defect levels described in the literature.

Although the atomic identity of EL2 is controversial, there seems to be a consensus emerging among both experimentalists and theorists that EL2 is a complex involving an As-on-Ga-site antisite defect, As_{Ga}, as one of its constituents. There is also indications that EL2 is not a unique complex, but a family of related complexes. In this work, we will use the model of J.F. Wager and J.A. Van Vechten [31]. They assumed that EL2 is composed of three point defects, Ga vacancy V_{Ga}, As vacancy V_{As}, and antisite defect As_{Ga}, as shown in Fig. 5-2-3. The ionization levels or activation energies are taken from the best available empirical determinations, which are given by Eq.(5-2-4) to (5-2-7),

$$E_{0/+}(As_{Ga}) = E_c - 0.82\,eV \quad [Ref: 32] \tag{5-2-4}$$

$$E_{+/++}(As_{Ga}) = E_c - 1.00\,eV \quad [Ref: 33] \tag{5-2-5}$$

$$E_{0/+}(V_{As}) = E_c - 0.45\,eV \quad [Ref: 34] \tag{5-2-6}$$

$$E_{-/0}(V_{Ga}) = E_v + 0.01\,eV \quad [Ref: 35] \tag{5-2-7}$$

where Eq.(5-2-5) was obtained from experiment conducted at T = 6 K, for which the GaAs bandgap E_{cv} = 1.52 eV. Others were measured at room temperature.

The net charge of each level depends on its relative position to Fermi level E_F. When E_F is above the level, it has the charge indicated above the level, and visa versa.

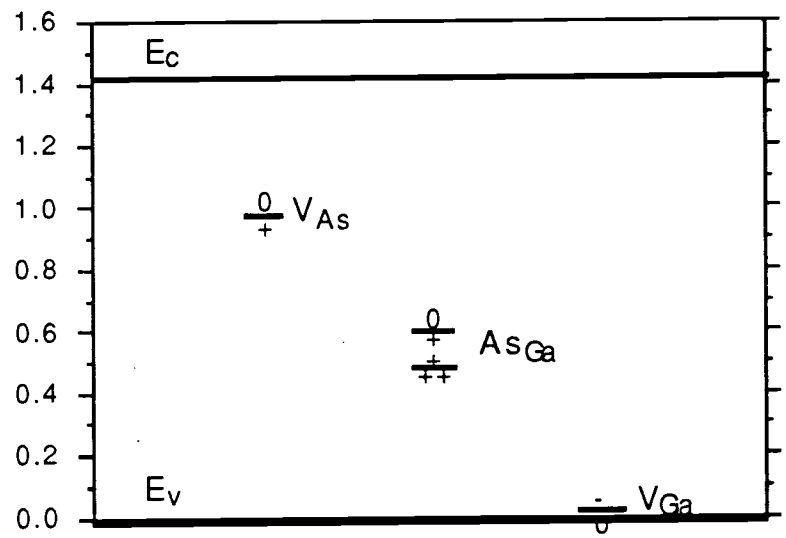


Fig. 5-2-3 Literature values for the level positions of vacancies and antisite defect of EL2 complex in GaAs at T = 300 K.

At room temperature the GaAs bandgap is E_{cv} = 1.42 eV. From Eq.(5-2-4) we get $E_{0/+}(As_{Ga})$ = 0.60 eV above the valence band. Since we do not have the value for $E_{+/++}(As_{Ga})$ level at room temperature, we assume that $E_{+/++}(As_{Ga})$ changes in the same rate as E_{cv},and thus we estimate $E_{+/++}(As_{Ga})$ = 0.48 eV above the valence band at room temperature. From Eq.(5-2-6) and Eq.(5-2-7), $E_{0/+}(V_{As})$ and $E_{-/0}(V_{Ga})$ are 0.97 eV and 0.01 eV above the valence band, respectively. The level positions shown in Fig. 5-2-3 are according to the above values.

To identify the deep levels we derived from the drain current transient data with the above EL2 model, we should recall that only those levels which cross the Fermi level have contributions to drain current transients. In Fig. 5-2-4 we draw the levels in the EL2 model of J.F. Wager and J.A. Van Vechten in a MESFET band diagram. At room temperature the GaAs band gap E_{cv} = 1.42 eV. With the doping concentration E_a = 5 x 10^{15} cm^{-3}, the Fermi level is 0.19eV above the valence band in channel region. The Fermi level position in semi-insulating GaAs substrate is 0.6 eV below the conduction band [14]. We can see that in the channel region only the level $E_{+/++}(As_{Ga})$ crosses the Fermi level and in the substrate region the level $E_{0/+}(As_{Ga})$ crosses the Fermi level. So we conclude that the level we measured for the channel region is level $E_{+/++}(As_{Ga})$ and the level we measured for the substrate region is level $E_{0/+}(As_{Ga})$. We can see that there are quite good agreements in the activation energies. The level in the channel region has activation energy 0.43 eV and level $E_{+/++}(As_{Ga})$ = 0.48 eV. The level in the substrate region has activation energy 0.58 eV and level $E_{0/+}(As_{Ga})$ = 0.60 eV.

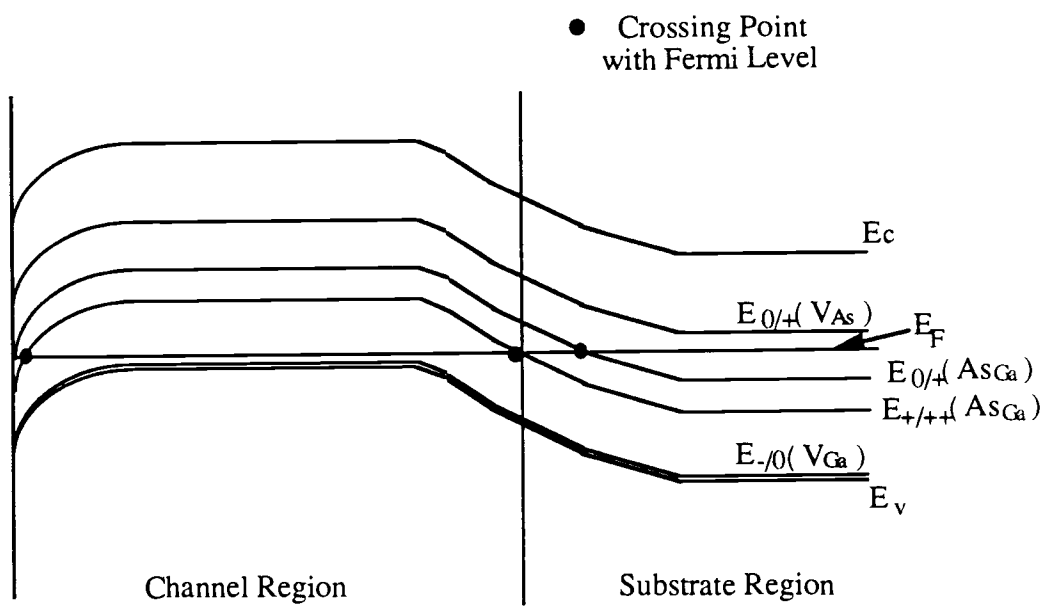


Fig.5-2-4 Band diagram for p-channel GaAs MESFET with defect levels

There is other evidence which supports this identification. A deep level has a certain charge state and the differences between the charge of a deep level and the charge of a carrier (electron or hole) may result in quite different capture cross sections. If the level is of opposite charge to the carrier, the two are attractive to each other so that the capture cross section is large. If the level is neutral, the capture cross section is smaller. And if the level has the same charge, the capture cross section is even smaller. There is an approximation [36] which gives the order of the capture cross sections under different situations and is shown in Table 5-2-3.

Table 5-2-3 Approximation for the capture cross sections of deep levels with different charge

Type of charge for the deep level	- (attractive)	0 (neutral)	+ (repulsive)
Order of capture cross section (cm^2)	$\sim 10^{-12}$	$\sim 10^{-15}$	$\sim 10^{-18}$

The capture cross section for the level in the channel is 7.5×10^{-18} cm^2. We identified it as the level $E_{+/++}(As_{Ga})$, which should have capture cross section in the order of 10^{-18} cm^2 according to this approximation. We see that there is good agreement. Similarly, the capture cross section for the level in the substrate is 4.0×10^{-15} cm^2 and which was identified as $E_{0/+}(As_{Ga})$. The capture cross section should be in the order of 10^{-15} cm^2 according to this approximation and it also agrees very well.

6. CONCLUSIONS AND DISCUSSIONS

6.1 Summary

In this work we discussed the drain current transient characterization of p-channel GaAs MESFET. We characterized the device under DC conditions and determined the proper bias conditions for transient measurements. Then we performed the drain current transient characterization at different temperatures. From the temperature dependent current transient results, we used a one-level model to extract the activation energies and capture cross sections for deep levels both in the channel region and in the substrate region. We associated the level in the channel region with an antisite defect $E_{+/++}(As_{Ga})$ and the level in the substrate region with another antisite defect $E_{0/+}(As_{Ga})$. Both levels are related to EL2 complex.

6.2 Relevant Issues of P-Channel GaAs MESFET Drain Current Transients

In this section we will discuss several issues related to p-channel GaAs MESFET drain current transients. First we will discuss the limitation of our fitting model for drain current transients. Then we will compare the p-channel GaAs MESFET drain current transients with the n-channel ones, from which we will see the differences of the deep trap level effects on the two devices. Finally we will demonstrate a simple method to relate the drain current transients to conductances in the frequency domain.

6.2.1 Non-exponential effects

We fitted the drain current transients basically to an exponential function (Eq.(5-2-1)). In the fitting graphs (see Fig. 5-2-1) we notice that our model could not fit very

well in the short time range. We describe this error as due to non-exponential effects. There are several reasons for these effects.

First, our model is a one-level model which assumes only one deep level may affect the drain current transient. This assumption may not be true. If we look at Fig. 5-2-4, we find that $E_{0/+}(As_{Ga})$ is very close to the Fermi-level in channel region near the surface, which implies that it may affect the drain current transient to negative step change in V_{ds}. Near the channel-substrate interface, the level $E_{+/++}(As_{Ga})$ crosses the Fermi-level. It may affect the occupation of this level in the substrate side, which will affect the drain current transient to positive step change in V_{ds}.

Secondly, we only use the corresponding emission process in our fitting model because we assume the capture process has much shorter time constant. From the discussion in Chapter II we know that capture processes also affect the drain current transients (see Table 2-2-1). In the channel region the hole concentration is relatively high, so that the capture process in channel region has a short time constant, which contributes to the positive step transient. In the substrate region the hole concentration changes with distance to the channel-substrate interface, and can be very small deep inside. Thus the capture constants for deep level in the substrate region may vary from very short to very long (even longer than emission time), which causes the non-exponential behavior in the negative step transient.

6.2.2 Differences between n-channel and p-channel GaAs MESFETs

Similar studies on n-channel GaAs MESFETs [12] show that the transients for positive and negative step on drain voltage change have a much larger difference than that for p-channel devices. The experimental results of Canfield are given in Fig. 6-2-1.

The transient corresponding to positive step change on drain voltage has a very short dominant time constant and a long tail. Canfield [12] suggested this was due to absence of EL2 levels in channel region because of high concentration of electrons [32], so that the transient is determined by a capture process in the substrate. The long tail was caused by different capture time due to a different electron concentrations in the substrate (refer to Eq.(2-2-8)). The transient corresponding to negative step change on drain voltage is very similar to that of the p-channel device reported here.

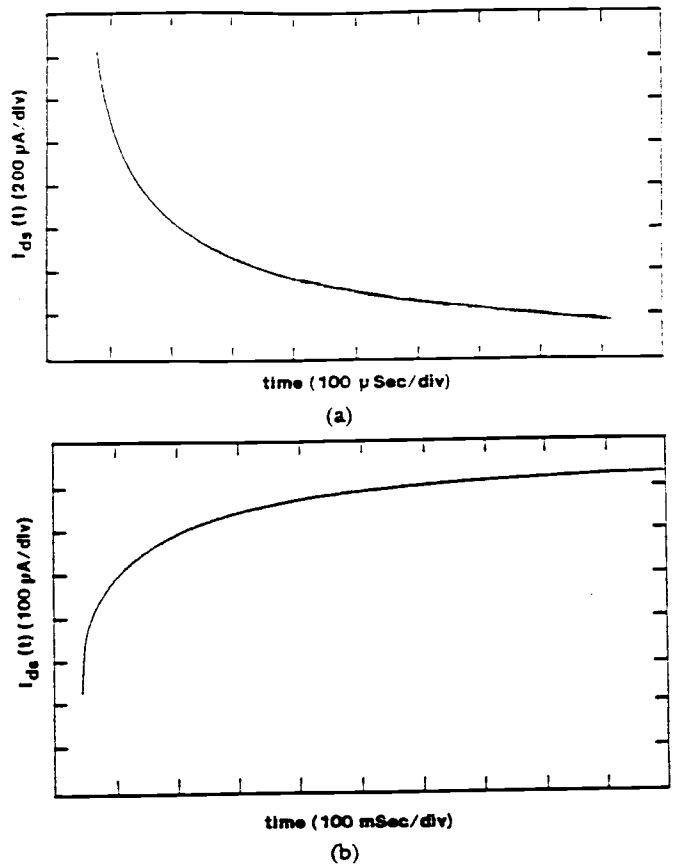


Fig. 6-2-1 Drain current transient of a 1μm gate-length GaAs MESFET with a 300μm gate width. (a) a drain voltage step from 1 to 2 V and (b) a step from 2 to 1V. (Results after P.C. Canfield, S. C.F. Lam, and D. J. Allstot, Ref: 12)

It is important to notice the differences between n-channel and p-channel GaAs MESFETs. For the n-channel device since the EL2 can be annihilated by shallow donors, the channel region does not have high concentration defects. People [37] have proposed a p-well technique which will eliminate the trap effects near the channel-well interface. For the p-channel device the EL2 defects can not be annihilated by shallow acceptor, so they will exist in the channel region. This is a fundamental limitation for high frequency application of the p-channel device. One of the ways to solve this problem is to grow an epitaxial GaAs layer on top of the substrate by molecular beam epitaxy (MBE) method and fabricate the devices on this epi-layer. MBE can produce high purity materials by careful control of Ga and As concentration during growth [38].

6.2.3 The relation between drain current transient and output conductance in the frequency domain

In the introduction chapter we mentioned that the purpose of this work is to understand the deep trap level effect on output conductance G_{ds}. The approach we chose was to study drain current transients in time domain. For analog circuit design, an equivalent circuit or expression for output conductance in the frequency domain is desired. A convenient method for estimating the frequency dependence of G_{ds} is to superimpose the transients to determine the relative time required for drain current to reach steady-state after both positive and negative steps (Fig. 6-2-2). At low frequencies when period of the signal is much greater than the emission time constants, traps can "follow" the applied signal. This results in measuring a total change in the drain current of ΔI_{ds0} in steady-state after both a positive and negative step. At higher frequencies, the holes trapped in EL2 levels cannot emit fast enough to follow the signal, resulting in a change in drain current of ΔI_{ds}. Since $\Delta I_{ds} > \Delta I_{ds0}$, by definition $G_{ds}=(\Delta I_{ds}/\Delta V_{ds})\,|_{\Delta V_{ds}\to 0}$, so G_{ds} is expected to increase at high frequency.

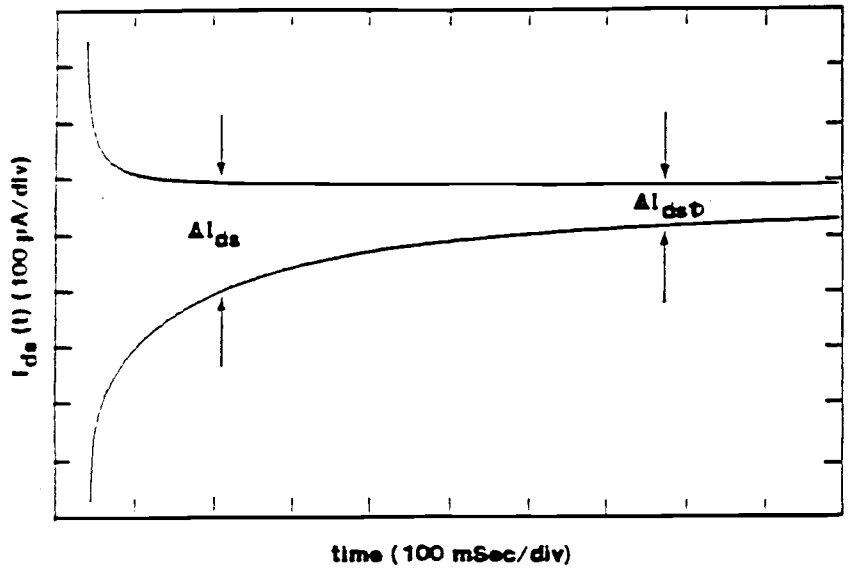


Fig. 6-2-2 Superposition of positive and negative step transients to determine ΔIds. (n-channel GaAs MESFET data, Ref: 12)

6.3 Future Work

In Section 6.2.3 we discussed a simple method to relate the drain current transient results to G_{ds} in the frequency domain. It is necessary to do the measurement of G_{ds} in the frequency domain to get more precise results and confirm the simple method. This work is in process now. Furthermore a small signal model for p-channel GaAs MESFET needs to develop to include the deep level trap effects.

In Section 6.2.2 we also discussed the limitation of p-channel device for high frequency applications and we suggested to use MBE grown materials to eliminate defect effects. This work can be done in the future.

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