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Abstract approved:

 James C. Looney

This paper is concerned with the design of a 21-bit metal-oxide-semiconductor field-effect transistor (MOSFET) integrated circuit static shift register.

This circuit consists of three separate 1, 4, and 16-bit static shift registers constructed on a single monolithic chip, each with independent input and output terminals.

Type D flip-flops are used to implement each bit of delay, enabling data to be stored indefinitely between clock pulses.

This design requires only one power supply and one external clock. Three clocks are generated internally. By appropriate connections, 1 bit, 4 bits, 5 bits, 16 bits, 17 bits, 20 bits and 21 bits may be obtained.

The circuit operates between DC and 800 KHz clock rates. It consists of 162 devices on a chip size of 62 mils x 47 mils.

A MOSFET INTEGRATED CIRCUIT SHIFT REGISTER

by

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# A MOSFET INTEGRATED CIRCUIT SHIFT REGISTER

## I. INTRODUCTION

Metal-oxide-semiconductor field-effect transistor (MOSFET) shift registers are at present the most popular MOSFET digital integrated circuit. They offer large bit capacities with attendant advantages of small size, low power consumption, and low cost as compared to other shift register devices. In addition to replacing existing shift registers in many applications they can be used to perform functions that were not practical with conventional components. High capacity digital delay lines and recirculating memories are among the most obvious applications. Industrial uses involving serial data transmission and storage can also benefit from the utilization of MOSFET shift registers.

This paper is intended to present the theoretical analysis, design methods, and results of the design of a 21-bit MOSFET static shift register.

## II. THEORETICAL ANALYSIS

### a. MOSFET Characteristics

The basic structure of a typical p-channel MOSFET is shown in Figure 1. The substrate is a chip of N-type silicon which serves as the supporting structure for the device. The two  $p^+$  regions, called the source and drain, respectively, are obtained by diffusing two wells of boron impurity into the substrate. In operation, these regions are connected by an induced p region known as the "channel."

The surface of the silicon is covered by a protective layer of silicon oxide formed during the silicon planar process. The gate, which is the control element of the MOSFET, consists of a layer of aluminum covering the surface between the source and drain. It is electrically insulated from the source and drain by the oxide, which is much thinner in this region than elsewhere and is therefore called the "thin-oxide" region to distinguish it from the surrounding "thick-oxide" regions. Aluminum contacts to the source and drain are provided.

If the gate, source, and substrate are grounded and a negative voltage is applied to the drain, no current will flow between source and drain, since the source and drain are isolated from each other by the reverse-biased drain-to-substrate p-n junction. If a voltage more negative than a certain threshold value,  $V_T$ , is applied to the gate, the

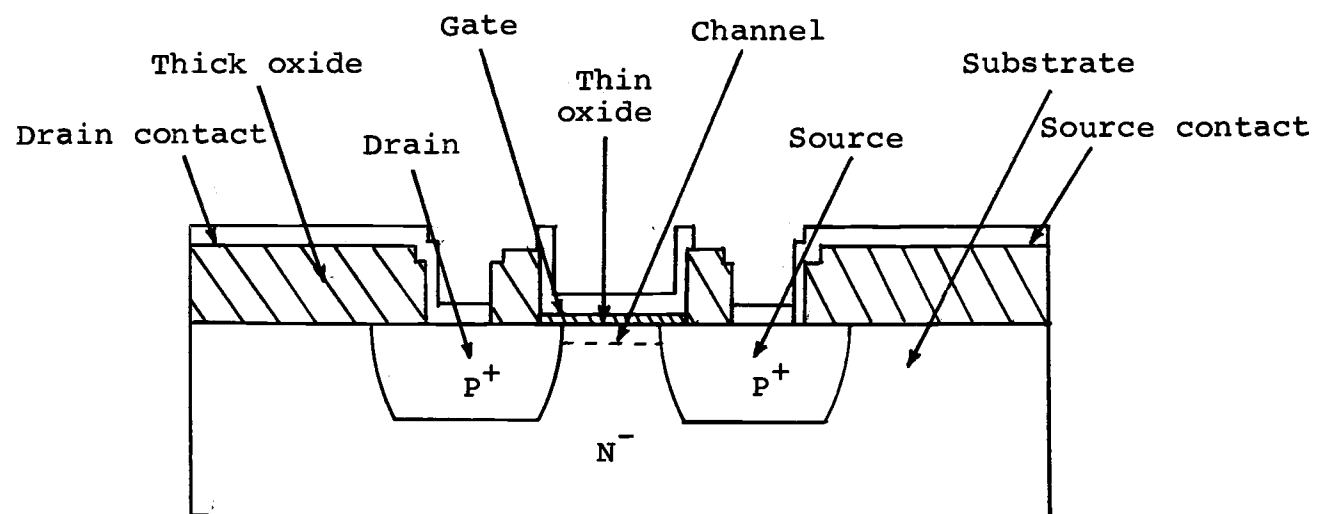


Figure 1. P-channel MOSFET.

surface of the N-type silicon "inverts," becoming p-type. This inverted region, called the "channel," connects the source and drain, providing a path for conduction of charge carriers between them.

The type of channel is determined classically by the type of majority carrier in the channel, and the mode of operation is related to the state of the channel at zero gate bias. If the channel must be formed before conduction can occur, it is called "enhancement-mode." A P-channel enhancement-mode MOSFET structure is assumed throughout this paper.

A useful feature of the MOSFET is that the gate-to-source capacitance can be used as a temporary memory storage element. Thus even if the gate supply is temporarily removed, the voltage remains stored on the gate.

#### (i) Drain Current

The active region of operation for the MOSFET is divided into two parts shown in Figure 2: the non-saturation region and the saturation region. The theoretical drain current expressions in each of these regions are given as follows (4):

$$I_D = \frac{\bar{\mu}_p \epsilon_{ox}}{2 t_{ox}} \frac{W}{L} \left[ 2(V_{GS} - V_T) V_{DS} - V_{DS}^2 \right],$$

$$\left| V_{GS} - V_T \right| \geq \left| V_{DS} \right| \quad (\text{non-saturated region}).$$

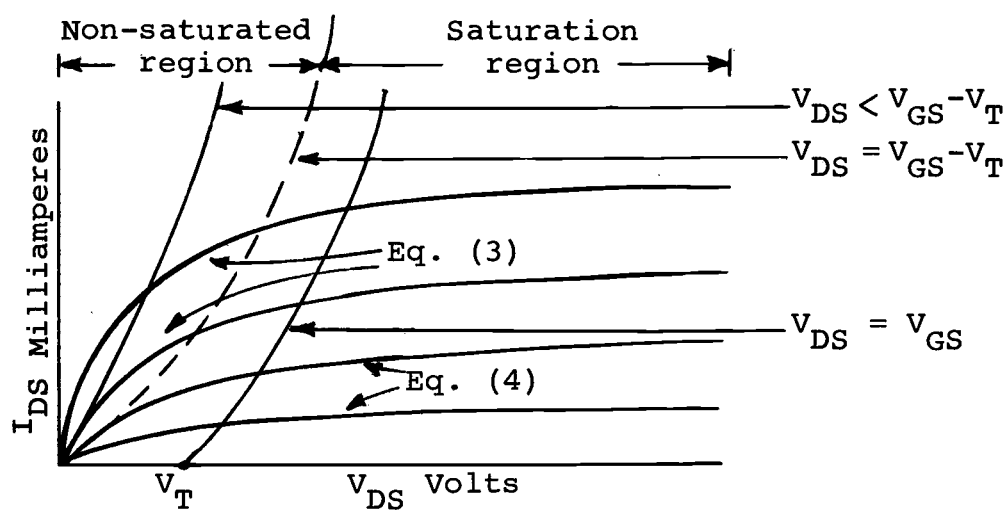


Figure 2. Active region of operation for the MOSFET.

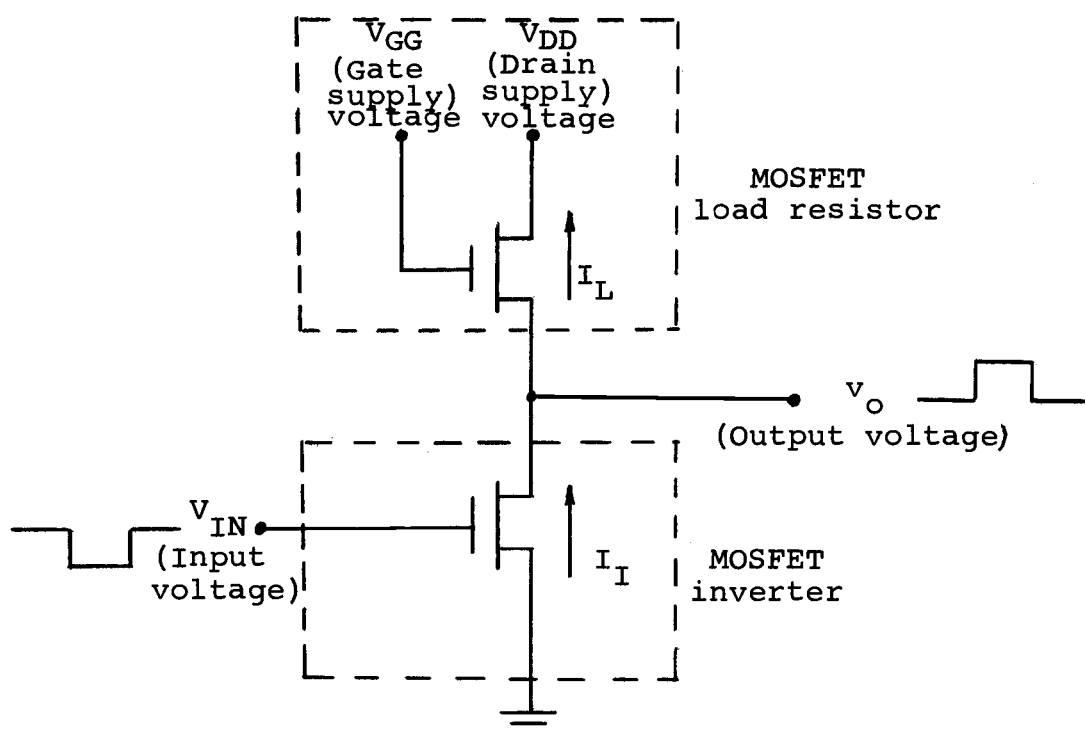


Figure 3. A typical MOSFET inverter circuit with a MOSFET as a load resistor.

$$I_D = \frac{\bar{\mu}_p \epsilon_{ox}}{2t_{ox}} \left[ \frac{W}{L} (V_{GS} - V_T)^2 \right],$$

$$\left| V_{GS} - V_T \right| \leq \left| V_{DS} \right| \quad (\text{saturated region}) .$$

Where:

$\bar{\mu}_p$  is the average surface mobility of holes in the channel.

$185 \frac{\text{cm}^2}{\text{v-sec}}$  is typical for (111) material (13).

$\epsilon_{ox}$  is the dielectric constant of the oxide layer.

$3.38 \times 10^{-13} \frac{\text{farad}}{\text{cm}}$  is the value used here.

$t_{ox}$  is the thickness of the oxide under the gate, typically  $1200\text{\AA}$ .

$W$  is the width of the channel.

$L$  is the length of the channel in the direction of current flow.

$V_{GS}$  is the voltage from gate to source.

$V_T$  is the threshold voltage.

$V_{DS}$  is the voltage from drain to source.

To simplify these equations, it is convenient to define two new parameters,  $K$  and  $K'$ , as follows:

$$K = K' \frac{W}{L}, \text{ and} \tag{1}$$

$$K' = \frac{\bar{\mu}_p \epsilon_{ox}}{2t_{ox}} . \tag{2}$$

The drain current expressions become

$$I_D = K \left[ 2(V_{GS} - V_T) V_{DS} - V_{DS}^2 \right] \quad (3)$$

for  $|V_{GS} - V_T| \geq |V_{DS}|$ , and

$$I_D = K \left[ V_{GS} - V_T \right]^2 \quad (4)$$

for  $|V_{GS} - V_T| \leq |V_{DS}|$ .

The parameter  $K'$  is fixed by the process; it is not a design variable. The parameter  $K$ , on the other hand, is determined by the device topology. A typical value of  $K'$  for normal processing is  $2.6 \frac{\mu\text{mhos}}{\text{volt}}$ .

Theoretical drain characteristics can be determined from the equations. The fact that the characteristics of the device depend upon the ratio  $W/L$  is of major importance in the procedures for design of MOSFET circuits.

#### (ii) Conductance and Turn-on Resistance

Normally the parameter of transconductance is determined in the active operating region of the device, which is the saturation region. In this region it can be evaluated from the theoretical current expressions:

$$g_m = \left. \frac{\partial I_D}{\partial V_G} \right|_{V_{DS}} = 2K [V_{GS} - V_T]. \quad (5)$$

The theoretical expression for  $g_m$  shows that this parameter is directly proportional to the ratio of  $W/L$  and also to the voltage  $(V_{GS} - V_T)$ .

Another parameter which is of interest in switching

applications is the resistance  $R_{on}$  of the device when it is turned on and operating in the non-saturated region.

This is defined as

$$R_{on} = \left. \frac{\partial V_D}{\partial I_D} \right|_{V_{GS}} = \frac{1}{K [2 (V_{GS} - V_T) - 2V_{DS}]} .$$

Since the current curves are nearly linear over much of the non-saturated region, this value can be approximated by the value at the origin (i.e., as  $V_{DS}$  goes to 0), giving

$$R_{on} \approx \frac{1}{2K(V_{GS} - V_T)} = \frac{1}{g_m} . \quad (6)$$

### (iii) Capacitance

There are two kinds of capacitance associated with the MOSFET: intrinsic and parasitic capacitance.

The intrinsic capacitance is due to the charge stored on the gate and in the channel of the device. It is defined as the total value of the gate-oxide-silicon parallel plate capacitance. It depends upon the oxide thickness, and is given by the expression (4):

$$C_o = \frac{\epsilon_{oxide}}{t_{oxide}} \quad (\text{area of gate}) . \quad (7)$$

For an oxide thickness of  $1200\text{\AA}$

$$C_o = 0.19 \frac{\text{pf}}{\text{mil}^2} .$$

The parasitic capacitances fall into two areas: The junction capacitance which is related to the back-bias diffused junctions of the drain and source, and the

overlap capacitance due to the gate metal overlapping into the drain and source areas. Junction capacitance is dependent on the amount of reverse bias and is found to be given approximately by the formula

$$C = \frac{0.08}{\sqrt[3]{0.6+V_R}} \text{ pf/mil}^2, \quad (8)$$

where  $V_R$  is the amount of the reverse bias voltage (13).  $0.05\text{pf/mil}^2$  is the average value of parasitic junction capacitance used here. A value of  $0.19\text{pf/mil}^2$  is used here for the parasitic overlap capacitance.

#### b. MOSFET Inverter

A typical MOSFET inverter circuit with a MOSFET as a load resistor is shown in Figure 3 (page 5). The circuit is normally operated with the drain tied to a negative voltage through the load resistor and the source lead grounded. Application of a negative voltage to the gate in excess of  $V_T$  turns the device on and pulls the output voltage from  $V_{DD}$  to ground, thereby causing a simple inversion at the output.

The theoretical expression for the voltage transfer characteristics of a MOSFET inverter device and its associated load will be developed.

The analysis will be done for two different types of loads: (1) a MOSFET device biased in the saturated mode; and (2) a MOSFET device biased in the non-saturated mode.

The method is outlined below.

(1) Write the equation for current in the inverter device. Since the inverter device will be in a saturated condition when the input voltage is small, and will enter a non-saturated condition as the input voltage increases, this step will require two equations. As a result, the analysis must be done in two parts to include both inverter conditions. This is illustrated in Figure 4 and Figure 5.

(2) Write the equation for the current in the load.

(3) Equate the current in the inverter device to the current in the load, since the current expressions will be functions only of the device parameters, the bias conditions, the input voltage, and the output voltage; the resulting equation will contain the voltage transfer characteristics.

(4) Normalize the output voltage and input voltage in these equations to the off-level output voltage.

(5) Calculate values and plot the transfer curves.

First consider the inverter shown in Figure 6. From the figure it is clear that

$$V_{GS} = V_{IN} , \text{ and} \quad (9)$$

$$V_{DS} = v_o . \quad (10)$$

The theoretical expression for the current in the inverter can be found by substituting equations (9) and (10) into equations (3) and (4), as follows:

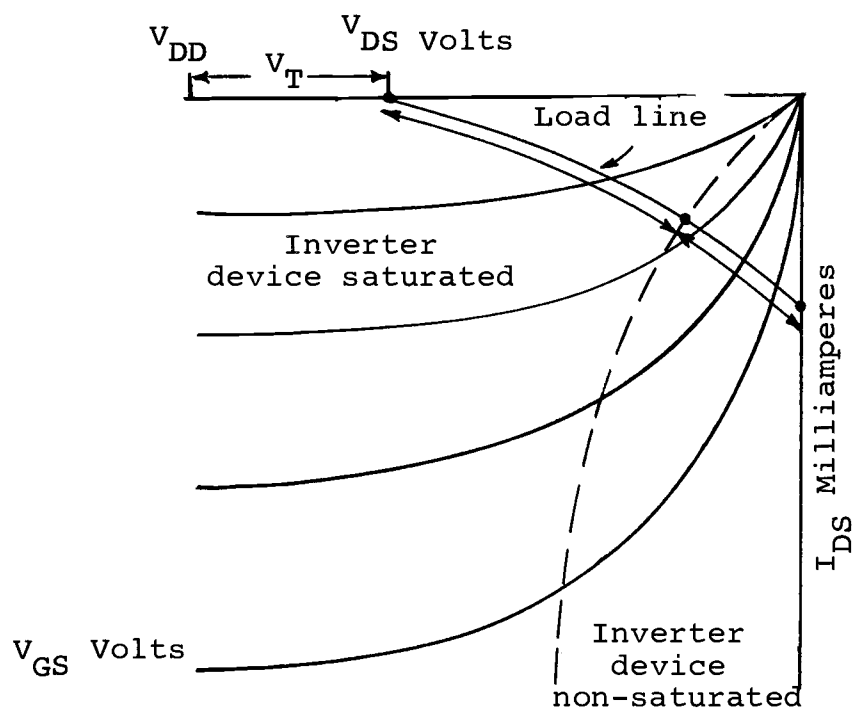


Figure 4. Drain characteristics of MOSFET inverter with load line.

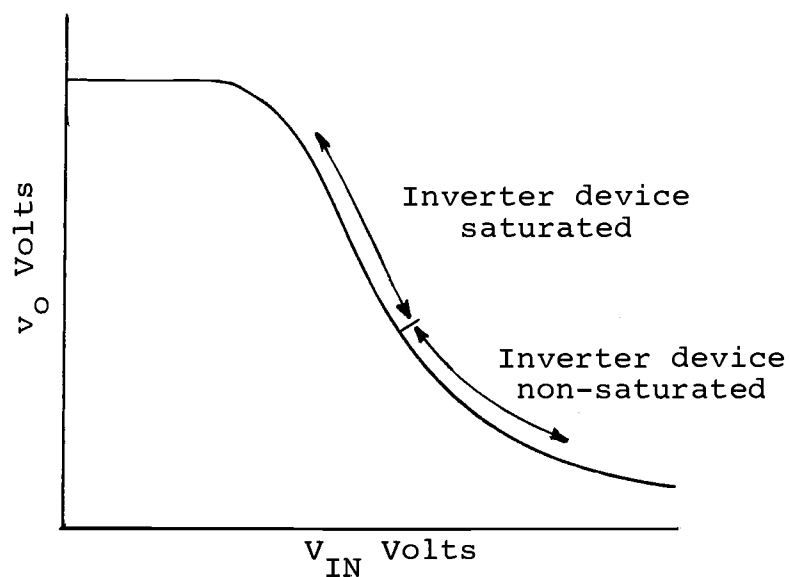


Figure 5. Transfer characteristic of MOSFET inverter with a load resistor.

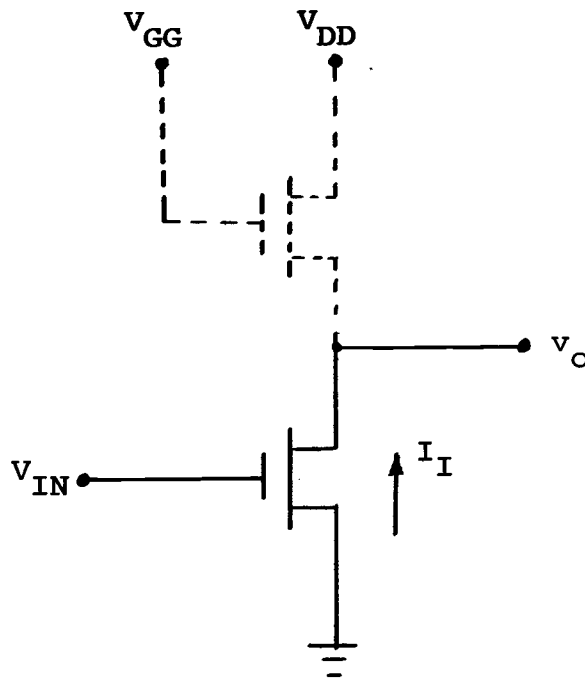


Figure 6. The direction of current flow in a MOSFET inverter.

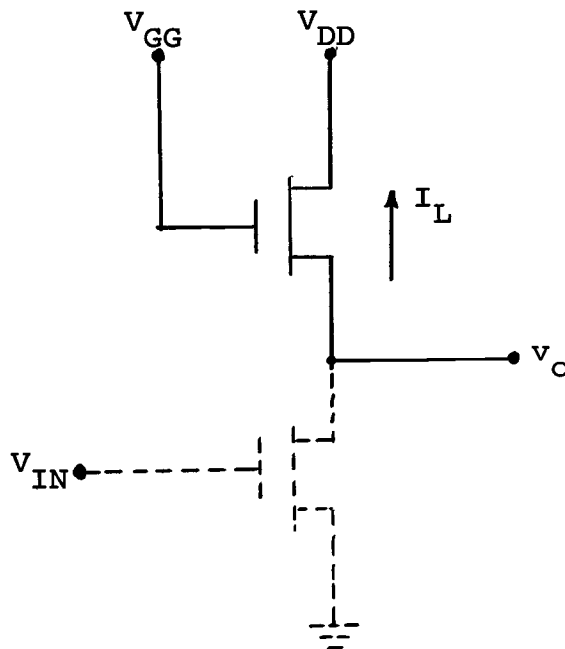


Figure 7. The direction of current flow in a MOSFET load device.

$$I_I = K_I (V_{in} - V_T)^2 \quad (11)$$

for  $|V_{in} - V_T| \leq |V_O|$  (saturated region), and

$$I_I = K_I \left[ 2(V_{in} - V_T)V_O - V_O^2 \right] \quad (12)$$

for  $|V_{in} - V_T| > |V_O|$  (non-saturated region).

### (i) Saturated MOSFET Load Device

Consider the case where a saturated MOSFET device is used as the load for the MOSFET inverter as shown in Figure 7 (page 12).

In order to insure saturation of the load device, the biasing must satisfy the condition that

$$|V_{GG} - V_T| \leq |V_{DD}|.$$

From Figure 7,

$$V_{GS} = V_{GG} - V_O, \text{ and} \quad (13)$$

$$V_{DS} = V_{DD} - V_O. \quad (14)$$

The theoretical expression for the current in the saturated device can be found by substituting (13) and (14) into equation (4), then

$$I_L = K_L \left[ (V_{GG} - V_O) - V_T \right]^2. \quad (15)$$

Setting  $I_L = I_I$  results in the equations:

$$K_L \left[ (V_{GG} - V_O) - V_T \right]^2 = K_I (V_{in} - V_T)^2 \quad (16)$$

for  $|V_{in} - V_T| \leq |V_O|$ , and

$$K_L \left[ (V_{GG} - V_O) - V_T \right]^2 = K_I \left[ 2(V_{in} - V_T)V_O - V_O^2 \right] \quad (17)$$

for  $|V_{in} - V_T| > |V_O|$ .

If  $v_o$  and  $(V_{in} - V_T)$  are normalized to  $(V_{GG} - V_T)$  and the terms rearranged, equations (16) and (17) become

$$\left(1 - \frac{v_o}{V_{GG} - V_T}\right)^2 = \frac{K_I}{K_L} \left(\frac{V_{in} - V_T}{V_{GG} - V_T}\right)^2 \quad (18)$$

$$\text{for } \left| \frac{V_{in} - V_T}{V_{GG} - V_T} \right| < \left| \frac{v_o}{V_{GG} - V_T} \right|, \text{ and}$$

$$\left(1 - \frac{v_o}{V_{GG} - V_T}\right)^2 = \frac{K_I}{K_L} \left[ 2 \left(\frac{V_{in} - V_T}{V_{GG} - V_T}\right) \left(\frac{v_o}{V_{GG} - V_T}\right) - \left(\frac{v_o}{V_{GG} - V_T}\right)^2 \right] \quad (19)$$

$$\text{for } \left| \frac{V_{in} - V_T}{V_{GG} - V_T} \right| > \left| \frac{v_o}{V_{GG} - V_T} \right|.$$

For a given value of the coefficient  $K_I/K_L$ , the curve of normalized output voltage  $v_o/(V_{GG} - V_T)$  versus normalized input voltage  $(V_{in} - V_T)/(V_{GG} - V_T)$  can be calculated using equations (18) and (19). These curves are shown for various values of parameter  $K_I/K_L$  in Figure 8.

Note that decreasing the W/L ratio of the load increases the value of  $K_I/K_L$  and that this has the same effect on the transfer characteristics as increasing the load resistance -- a steeper slope and a lower final value. It is also important to realize that the Off-level voltage  $(V_{GG} - V_T)$  is different for different values of  $V_{GG}$ . The only saturated load devices normally used have gate and drain connected together so that  $V_{GG} = V_{DD}$ .

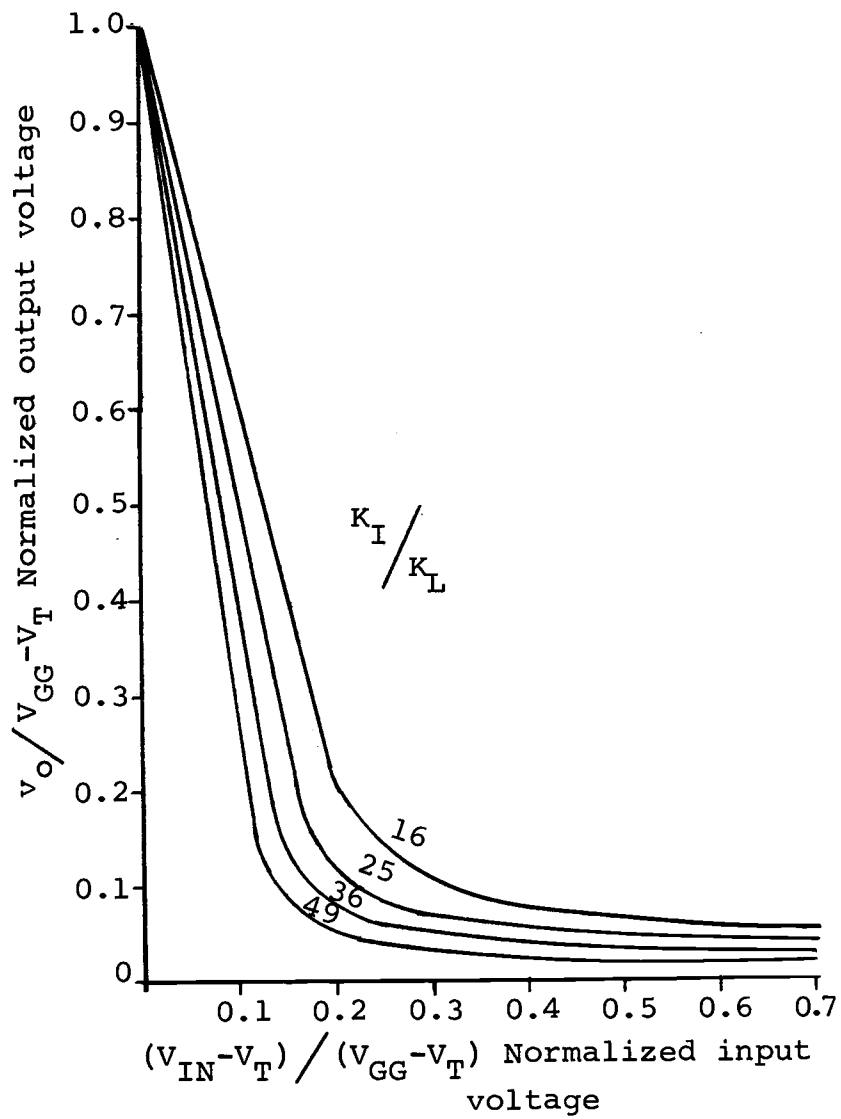


Figure 8. Normalized theoretical voltage transfer characteristics for a saturated MOSFET load device (4).

### (ii) Non-saturated MOSFET Load Device

Consider the case where a non-saturated MOSFET device is used as the load on the MOSFET inverter device. To insure that the load device is not saturated, the biasing must satisfy the condition  $|V_{GG} - V_T| \geq |V_{DD}|$ . The theoretical expression for the current in the non-saturated load device can be found by substituting equations (13) and (14) into equation (3) as follows:

$$I_L = K_L \left[ 2(V_{GG} - v_o - V_T)(V_{DD} - v_o) - (V_{DD} - v_o)^2 \right]. \quad (20)$$

Equation (20) can be rewritten:

$$\begin{aligned} I_L &= K_L \left( \left[ V_{DD} - v_o \right] \left[ 2(V_{GG} - V_T) - V_{DD} - v_o \right] \right) \quad (21) \\ &= K_L \left[ 2(V_{GG} - V_T) - V_{DD} \right] \left( \left[ V_{DD} - v_o \right] \left[ 1 - \frac{v_o}{2(V_{GG} - V_T) - V_{DD}} \right] \right) \\ &= K_L V_{DD}^2 \frac{[2(V_{GG} - V_T) - V_{DD}]}{V_{DD}} \\ &\quad \left( \left[ 1 - \frac{v_o}{V_{DD}} \right] \left[ 1 - \frac{V_{DD}}{2(V_{GG} - V_T) - V_{DD}} \frac{v_o}{V_{DD}} \right] \right). \end{aligned}$$

To simplify the algebra, it is convenient to introduce into the equation a biasing parameter,  $m$ , defined as follows:

$$m = \frac{V_{DD}}{2(V_{GG} - V_T) - V_{DD}}. \quad (22)$$

Equation (21) then becomes:

$$I_L = \frac{K_L V_{DD}^2}{m} \left( 1 - \frac{v_o}{V_{DD}} \right) \left( 1 - m \frac{v_o}{V_{DD}} \right). \quad (23)$$

The biasing parameter  $m$  has no real physical meaning. It is merely a convenient parameter to express the biasing

conditions. This parameter has meaning only if the load device is non-saturated; the voltage must satisfy the relation  $|V_{GG} - V_T| \geq |V_{DD}|$ . The maximum value of  $m$  occurs when  $V_{GG} - V_T = V_{DD}$  where  $m = V_{DD} / (2V_{DD} - V_{DD}) = 1.0$ .

The value of  $m$  decreases as the gate voltage is made more negative and  $m \rightarrow 0$  as  $V_{GG} \rightarrow -\infty$ .

Setting  $I_I = I_L$  results in the equations

$$\frac{K_L V_{DD}^2}{m} \left(1 - \frac{v_o}{V_{DD}}\right) \left(1 - m \frac{v_o}{V_{DD}}\right) = K_I (V_{in} - V_T)^2 \quad (24)$$

for  $|V_{in} - V_T| \leq |v_o|$ , and

$$\frac{K_L V_{DD}^2}{m} \left(1 - \frac{v_o}{V_{DD}}\right) \left(1 - m \frac{v_o}{V_{DD}}\right) = K_I \left[2(V_{in} - V_T)v_o - v_o^2\right] \quad (25)$$

for  $|V_{in} - V_T| \geq |v_o|$ .

Note that both types of load can be described by a single general equation

$$I_L = I_{sc} \left(1 - \frac{v_o}{V_0}\right) \left(1 - m \frac{v_o}{V_0}\right), \quad (26)$$

where  $I_{sc}$  is the short-circuit current, i.e.,

$I_{sc} = I_L|_{v_o = 0}$ , and  $v_o = V_0$ , when the inverter is turned off. The value of  $I_{sc}$ ,  $m$  and  $V_0$  for each case are defined in Table I.

Table I. Expressions for  $I_{sc}$ ,  $m$ , and  $V_0$ .

	$I_{sc}$	$m$	$V_0$
Saturated MOSFET load	$K_L (V_{GG} - V_T)^2$	1	$V_{GG} - V_T$
Non-saturated MOSFET load	$\frac{K_L V_{DD}^2}{m}$	$\frac{V_{DD}}{2(V_{GG} - V_T) - V_{DD}}$	$V_{DD}$

(iii) Power Consumption of MOSFET Inverter

The DC power associated with the current flow in the saturated region is as follows:

$$P = V_{DD} K (V_{GS} - V_T)^2 \text{ watts.} \quad (27)$$

In the non-saturated region the DC power associated with the current flow is as follows:

$$P = V_{DD} K \left[ 2(V_{GS} - V_T) V_{DS} - V_{DS}^2 \right]. \quad (28)$$

c. Transient Response

Theoretical expressions will be obtained for both turn-off and turn-on characteristics of the circuit.

(i) Turn-off Time

For the turn-off case shown in Figure 9, the inverter will be assumed to switch from the conducting state to a completely nonconducting state at the beginning of the transient. Thus it is assumed that the input is a step function and that the device itself has no inherent time delay. The currents are  $I_L$ , shown in equation (26) and

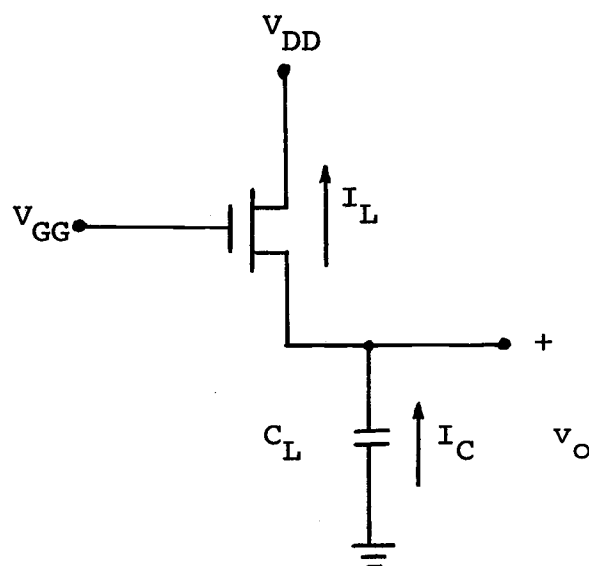


Figure 9. Turn-off case of a MOSFET inverter.

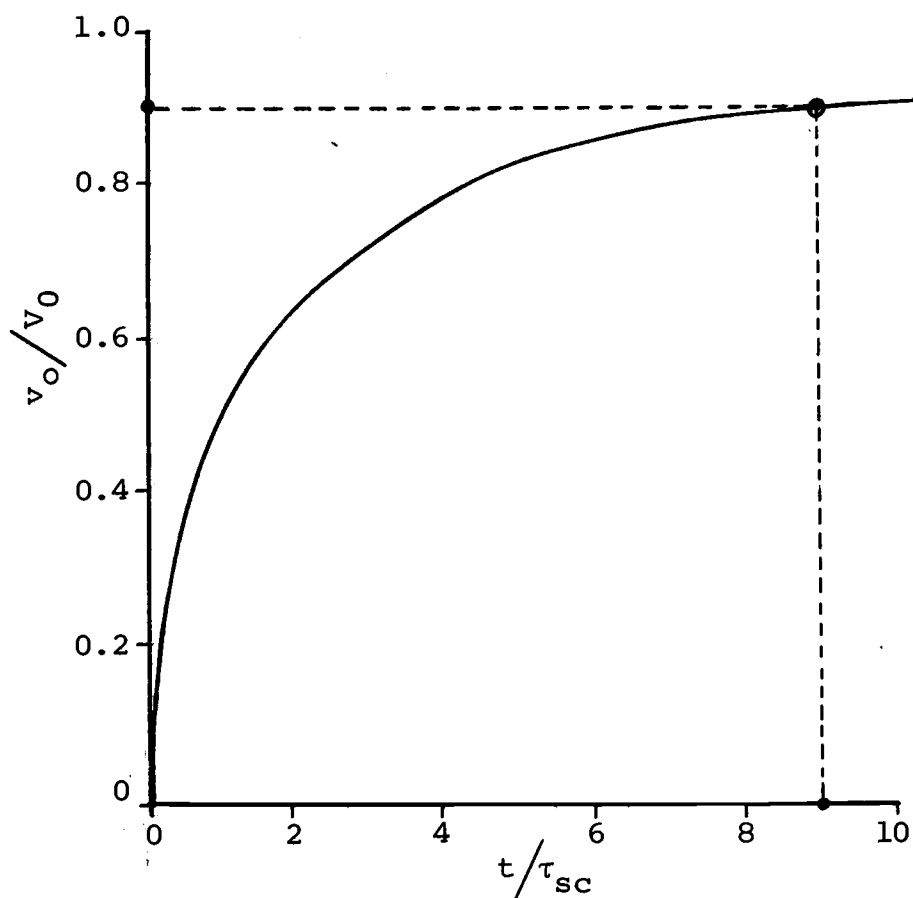


Figure 10. Turn-off characteristics. Normalized output voltage  $v_o/V_0$  as a function of the normalized time  $t/\tau_{sec}$ .

$$I_C = -C_L \frac{dv_o}{dt} . \quad (29)$$

Equating the currents at the output node will give the differential equation describing the transient condition.

This gives  $I_L = I_C$ ,

$$I_{sc} \left(1 - \frac{v_o}{V_0}\right) \left(1 - m \frac{v_o}{V_0}\right) = -C_L \left(\frac{dv_o}{dt}\right) . \quad (30)$$

If the short-circuit resistance is defined as

$$R_{sc} = \frac{-V_0}{I_{sc}} , \quad (31)$$

equation (30) becomes

$$\left(1 - \frac{v_o}{V_0}\right) \left(1 - m \frac{v_o}{V_0}\right) = R_{sc} C_L \frac{d\left(\frac{v_o}{V_0}\right)}{dt} .$$

Rearranging and integrating yields

$$\int dt = \int (R_{sc} C_L) \frac{d\left(\frac{v_o}{V_0}\right)}{\left(1 - \frac{v_o}{V_0}\right) \left(1 - m \frac{v_o}{V_0}\right)} .$$

From a table of integrals,

$$\int \frac{dx}{(1-x)(1-mx)} = \frac{1}{-m+1} \ln\left(\frac{1-mx}{1-x}\right) .$$

The equation therefore becomes

$$t = R_{sc} C_L \left(\frac{1}{1-m}\right) \ln\left[\frac{1 - m \frac{v_o}{V_0}}{1 - \frac{v_o}{V_0}}\right] .$$

Hence,

$$\epsilon^{\left(\frac{1-m}{R_{sc}C_L}\right)t} = \frac{1-m\left(\frac{v_o}{V_0}\right)}{1-\left(\frac{v_o}{V_0}\right)} .$$

Finally, solving for  $v_o/V_0$ :

$$\frac{v_o}{V_0} = \frac{1-\epsilon^{-\left(\frac{1-m}{R_{sc}C_L}\right)t}}{1-m\epsilon^{-\left(\frac{1-m}{R_{sc}C_L}\right)t}} = \frac{1-\epsilon^{-(1-m)t/\tau_{sc}}}{1-m\epsilon^{-(1-m)t/\tau_{sc}}} , \quad (32)$$

$$\text{where } \tau_{sc} = R_{sc}C_L . \quad (33)$$

When the load device is saturated, i.e.,  $m = 1$ , the limit of the above solution may be obtained by using L'Hospital's rule:

$$\begin{aligned} \left. \frac{v_o}{V_0} \right|_{m=1} &= \lim_{m \rightarrow 1} \frac{1-\epsilon^{-\left(\frac{1-m}{\tau_{sc}}\right)t}}{1-m\epsilon^{-\left(\frac{1-m}{\tau_{sc}}\right)t}} \\ &= \frac{\frac{t}{\tau_{sc}}}{1+\frac{t}{\tau_{sc}}} . \end{aligned} \quad (34)$$

The curve of  $v_o/V_0$  as a function of  $t/\tau_{sc}$  can be calculated and plotted as shown in Figure 10 (page 19). As seen in Figure 10,  $t/\tau_{sc} = 9$  when  $v_o/V_0 = 90\%$ . Therefore for a saturated device,  $t_{off} = 9R_{sc}C_L$ .

For the saturated device, combining equations (1), (15), (31), (33) and Table I gives

$$\frac{W}{L} = \frac{C_L}{\tau_{sc}(V_{GS}-V_T)K'} . \quad (35)$$

### (ii) Turn-on Time

For the turn-on case shown in Figure 11, the inverter will be assumed to switch from the nonconducting state to a completely conducting state at the beginning of the transient. Thus it is assumed that the input is a step function and that the device itself has no inherent time delay.

It will be assumed that the MOSFET load device is biased for operation in the non-saturated mode. The solution of the problem for the saturated MOS load device will be obtained as the limiting case of the solution for the non-saturated MOSFET load device. As a result the circuit for  $t \leq 0$  becomes as in Figure 11.

The current equations are given by equations (11), (12), (26), (29) and Table I. Summing currents at the output node will give two differential equations describing the transient condition. This gives  $I_L = I_I + I_C$ ,

$$\frac{K_L V_0^2}{m} \left(1 - \frac{v_o}{V_0}\right) \left(1 - m \frac{v_o}{V_0}\right) = K_I (V_{in} - V_T)^2 - C_L \frac{dv_o}{dt} \quad (36)$$

$$\text{for } |v_o| \geq |V_{in} - V_T|, \text{ and}$$

$$\begin{aligned} \frac{K_L V_0^2}{m} \left(1 - \frac{v_o}{V_0}\right) \left(1 - m \frac{v_o}{V_0}\right) \\ = K_I \left[ 2 (V_{in} - V_T) v_o - v_o^2 \right] - C_L \frac{dv_o}{dt} \end{aligned} \quad (37)$$

$$\text{for } |v_o| \leq |V_{in} - V_T|.$$

If  $V_{in} - V_T$  is normalized to  $V_0$  and the terms rearranged, equation (36) becomes:

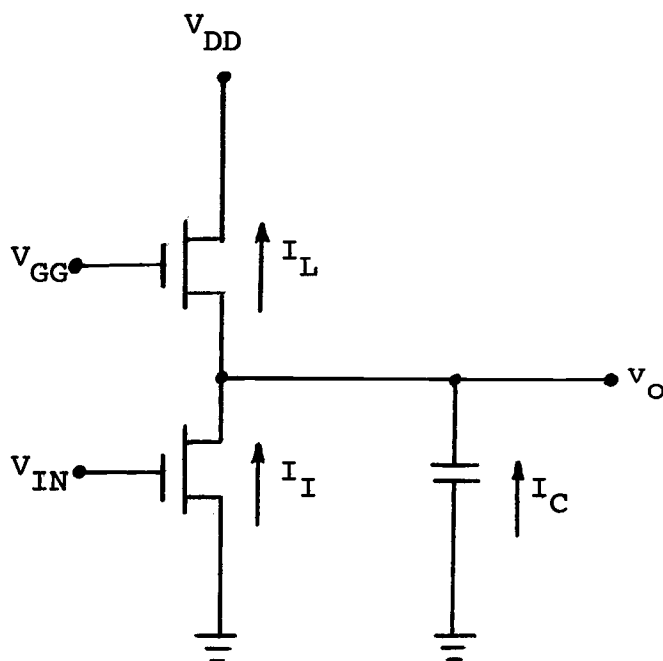


Figure 11. Turn-on case of a MOSFET inverter.

$$\frac{v_o}{V_0} = \frac{1}{2c_s} \left[ -b_s + \sqrt{-q_s} \tanh \left( -\frac{t}{R_{sc}C_L} \frac{\sqrt{-q_s}}{2} + K_s \right) \right] \quad (38)$$

$$\text{for } \left| \frac{v_o}{V_0} \right| \geq \left| \frac{V_{in}-V_T}{V_0} \right|.$$

Where:

$$a_s = 1 - m \frac{K_I}{K_L} \left( \frac{V_{in}-V_T}{V_0} \right)^2.$$

$$b_s = -(1+m) \cdot c_s = m.$$

$$q_s = 4 a_s c_s - b_s^2.$$

$$K_s = \tanh^{-1} \left( \frac{2c_s + b_s}{\sqrt{-q_s}} \right).$$

The output voltage will follow the resulting equation until it has reached the value  $\left| v_o/V_0 \right| = \left| \frac{V_{in}-V_T}{V_0} \right|$ . Then the inverter passes from saturated into unsaturated operation, and the current equation must be changed. The time at which  $\left| v_o/V_0 \right| = \left| \frac{V_{in}-V_T}{V_0} \right|$  will be designated as  $t'$ .

Next the solution will be found for  $t \geq t'$  during the time interval when the inverter is non-saturated by rearranging equation (37), and normalizing  $V_{in}-V_T$  to  $V_0$ . This gives

$$\frac{v_o}{V_0} = \frac{1}{2c_n} \left[ -b_n + \sqrt{-q_n} \tanh \left( -\frac{(t-t')}{R_{sc}C_L} \frac{\sqrt{-q_n}}{2} + K'_n \right) \right] \quad (39)$$

$$\text{for } \left| \frac{v_o}{V_0} \right| \leq \left| \frac{V_{in}-V_T}{V_0} \right|.$$

Where:

$$a_n = 1.$$

$$b_n = - \left[ 1 + m + m \frac{K_I}{K_L} 2 \left( \frac{V_{in} - V_T}{V_0} \right) \right] .$$

$$c_n = m \left( 1 + \frac{K_I}{K_L} \right) .$$

$$q_n = 4 a_n c_n - b_n^2 .$$

The value of  $K'_n$  can be found from the relation that

$\left| v_o / V_0 \right| = \left| \frac{V_{in} - V_T}{V_0} \right|$  at  $(t - t') = 0$  where  $t'$  is the time at which the inverter enters the non-saturated region of operation.

Solving equations (38) and (39) with

$$V_{in} = -15v,$$

$$V_0 = -21v,$$

$$V_T = -6v,$$

$$\frac{K_I}{K_L} = 20,$$

$$m = 1,$$

gives  $t_{on} \approx 0.35 R_{sc} C_L$  which are the values used for the following design for  $v_o / V_0 = 10\%$ . Since the turn-on time is normally much faster than the turn-off time, the turn-on time can usually be neglected.

#### d. Static Shift Register

An analysis of static shift register circuit operation follows. A static shift register stage and clock waveforms shown as a timing reference are illustrated in Figure 12.

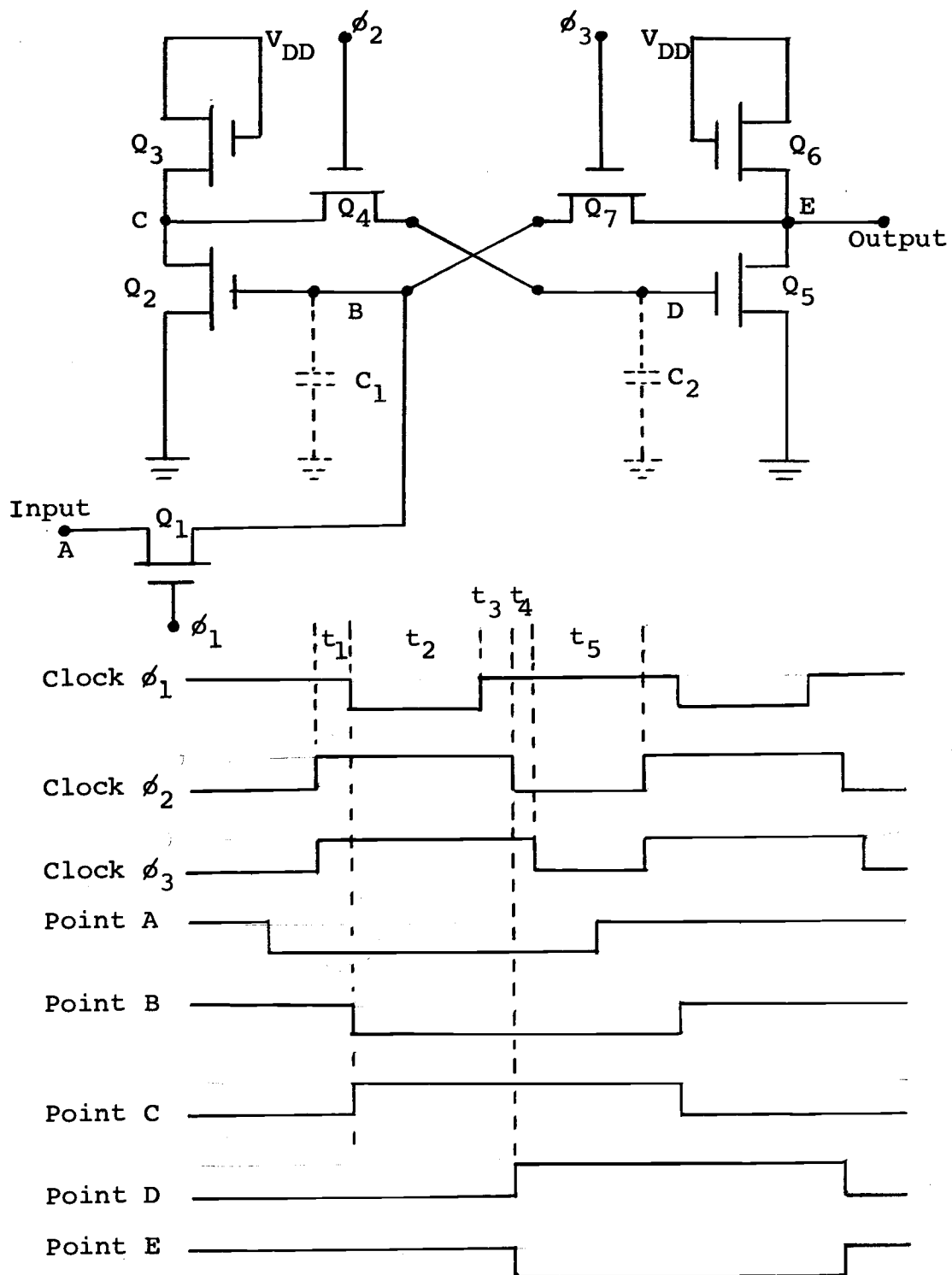


Figure 12. Static shift register with clock waveforms shown as a timing reference.

A logic "1" input to the register appears as a negative voltage at point A. During  $t_1$  time period,  $\phi_2$  and  $\phi_3$  are at ground. This turns off  $Q_4$  and  $Q_7$ . Information stored on capacitors  $C_1$  and  $C_2$  remains unchanged and the register output appears at point E. During  $t_2$ , data is transferred to the gate of  $Q_2$  (point B) because of the conduction of  $Q_1$ . As  $C_1$  is charged to the negative input,  $Q_2$  turns on and point C approaches ground potential. As  $t_3$  begins,  $\phi_1$  returns to ground, cutting off  $Q_1$ , but  $C_1$  remains charged negative holding the drain of  $Q_2$  (point C) near ground. As  $t_4$  begins,  $\phi_2$  goes negative and  $Q_4$  turns on, bringing the gate of  $Q_5$  to the potential of the drain of  $Q_2$  (point C). This turns  $Q_5$  off and point E now rises to within one threshold voltage of  $V_{DD}$ . As  $t_5$  begins,  $\phi_3$  goes negative and  $Q_7$  turns on. Then the voltage from point E is coupled back through  $Q_7$  to the gate of  $Q_2$ , latching  $Q_2$  in the on state. For transferring a logic "0" into the register the sequence is repeated starting with a ground signal at point A.

### III. DESIGN OF A 21-BIT MOSFET STATIC SHIFT REGISTER

A highly versatile 21-bit static shift register was designed by combining three separate 1, 4, and 16-bit MOSFET static shift registers with independent input and output terminals.

To make it easier to understand, it is shown in logic block diagram form (Figure 13).

The 16-bit static shift register uses 16 single static shift registers and one buffer to get a 16-bit delay. The input and  $\phi_1$  of the first bit go through an AND gate into the first static shift register. The output of the first bit appears at Q, forming the input to the next stage. The output of the last bit goes through a buffer to aid in driving an external load. The function of the 4-bit static shift register and 1-bit static shift register is the same as the 16-bit static shift register.

The clock generator provides the timing signals necessary to operate the static shift registers. One external clock ( $\phi$ ) is required for operation with three clocks ( $\phi_1$ ,  $\phi_2$ , and  $\phi_3$ ) generated internally.  $\phi_1$  is generated in phase with  $\phi$  but is delayed by using two inverters.  $\phi_2$  is generated 180 degrees out of phase with  $\phi$  by a NOR gate, and  $\phi_3$  is produced by delaying  $\phi_2$  slightly.

The design was performed for worst-case conditions.

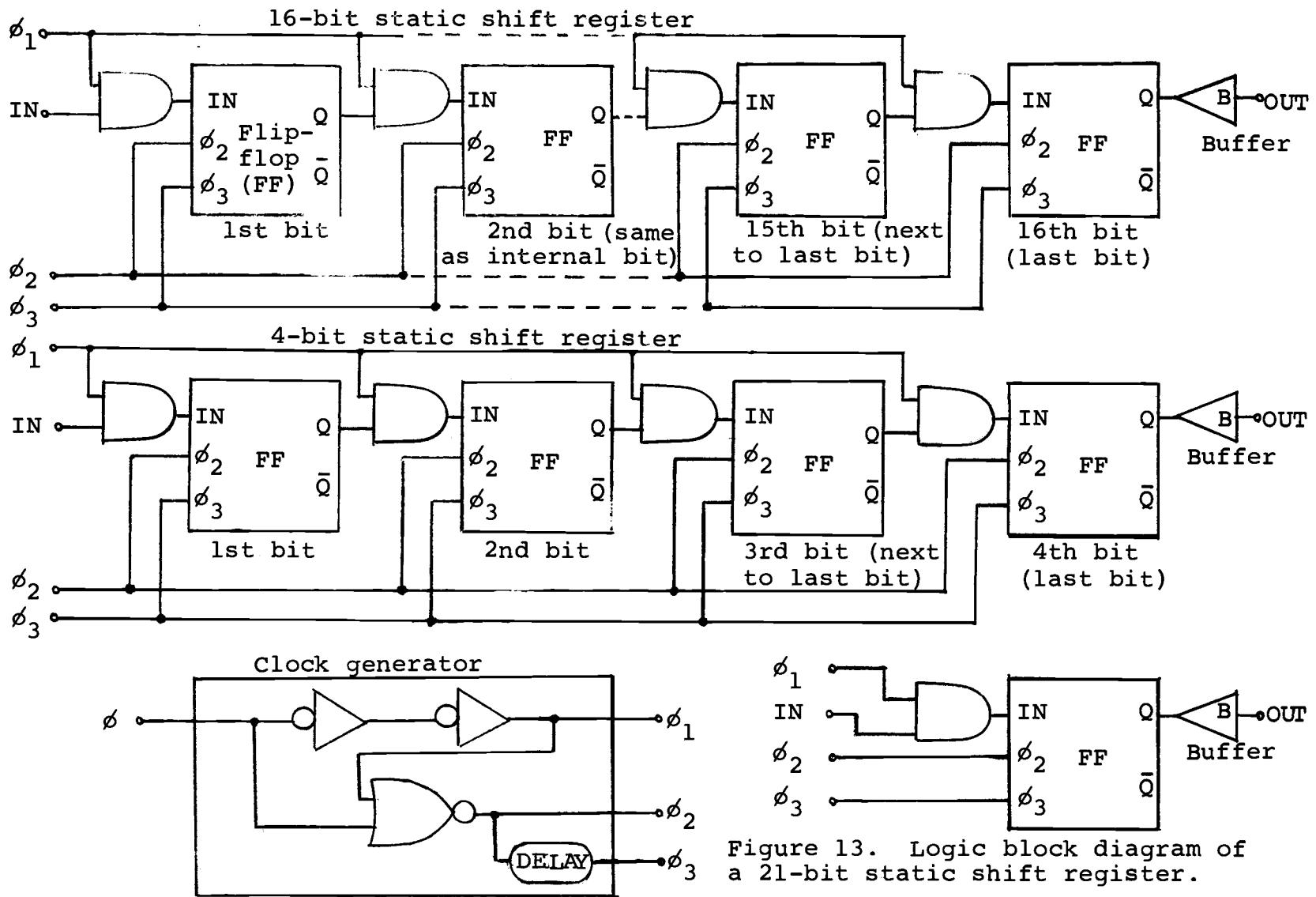


Figure 13. Logic block diagram of a 21-bit static shift register.

The following discussion explains the worst conditions of temperature and voltage.

#### High Temperature

Since  $\bar{\mu}_p$  decreases with increasing temperature,  $I_L$  decreases with increasing temperature. A lower charging current results in lower speed.

#### Low $V_{DD}$

With a lower  $V_{DD}$ ,  $C_L$  charges to a smaller final voltage and therefore takes longer to reach the voltage defined as a logic "1".

#### Low $V_{GG}$

A low  $V_{GG}$  means a higher value of  $m$  and therefore slower switching.

#### High $V_T$

High  $V_T$  means less effective gate drive voltage, and again, less speed. The worst case parameters of this design were assumed as follows:

$$V_{DD} = V_{GG} = -27 \text{ volts},$$

$$V_O = -27 \text{ volts},$$

$$V_T = -6 \text{ volts},$$

$$V_{in} = -11 \text{ volts},$$

$$V_0 = -15 \text{ volts},$$

$$F_{\phi} = 800 \text{ KHz},$$

$$\phi = -11 \text{ volts},$$

$$P = 260 \text{ mw},$$

$$C_L = 20 \text{ pF},$$

$$v_O' = -1.5 \text{ volts},$$

$$t_{\text{oxide}} = 1200 \text{ \AA},$$

where:

$$V_{DD} = \text{drain supply voltage},$$

$$V_{GG} = \text{gate supply voltage},$$

$$V_O = \text{buffer supply voltage},$$

$$V_T = \text{threshold voltage},$$

$$V_{in} = \text{data input voltage},$$

$$V_0 = \text{off level data output voltage (final value)},$$

$$F_{\phi} = \text{clock frequency},$$

$$\phi = \text{clock input voltage},$$

$$P = \text{power consumption},$$

$$C_L = \text{load capacitance},$$

$$v_O' = \text{on level voltage},$$

$$t_{\text{oxide}} = \text{the thickness of oxide under the gate}.$$

It was assumed that the voltage range for a logic "1" would be from -8v to -15v. Any input voltage within this

range should turn on an inverter. For logic "0" a voltage range from 0v to -4v was assumed. Any input voltage within this range should turn off an inverter.

#### a. Output Buffer and Last Bit

To aid the last bit in driving an external load, a push-pull buffer is used. It is illustrated in Figure 14.

A logic "1" at the point E turns  $Q_{30}$  on and  $Q_{29}$  off, allowing the external capacitor  $C_L$  to charge to logic "1". A logic "0" at the point E causes  $Q_{30}$  to turn off and  $Q_{29}$  to turn on, allowing the capacitance to discharge to ground. Since  $Q_{30}$  and  $Q_{29}$  never turn on simultaneously, there is no quiescent power consumption in this stage.

With  $Q_{30}$  saturated, equation (35) gives

$$\frac{W}{L} = \frac{C_L}{\tau_{sc} (V_{GS} - V_T) K'}$$

Assuming  $v_o/V_0 = 90\%$ , Figure 10 or equation (34) gives

$$t_r = 9 \tau_{sc},$$

where  $t_r$  is the time required to charge  $C_L$  to 90% of  $V_0$  and  $v_o$  is the instantaneous value of the output voltage.

Equation (35) becomes

$$\frac{W}{L} = \frac{9 C_L}{t_r (V_{GS} - V_T) K'} \quad (40)$$

The rise time of the circuit is limited by the output buffer and last bit.  $t_r$  should be as small as possible but is limited by the dimensions of  $Q_{30}$ . Taking



this into account, a desired rise time of 80 nsec was selected. The W/L ratio of  $Q_{30}$  is then

$$\left(\frac{W}{L}\right)_{30} = \frac{(9)(20)(10^{-12})}{(80)(10^{-9})(15)(2.6)(10^{-6})} = 60 .$$

$t_f$  is the time required to discharge  $C_L$  to 10% of  $V_0$ .  $t'$  is the time that  $Q_{29}$  changes from saturated into non-saturated operation. For  $0 \leq t \leq t'$ ,  $Q_{29}$  is saturated. Combining equations (4) and (29) gives

$$C \frac{dv_o}{dt} = K (V_{GS} - V_T)^2, \text{ and integrating} \quad (41)$$

$$\frac{C_L}{K(V_{GS} - V_T)^2} \int_{-15}^{-9} dv_o = \int_0^{t'} dt .$$

$$t' = \frac{6C}{81K}$$

For  $t' \leq t \leq t_f$ ,  $Q_{29}$  is non-saturated. Combining equations (3) and (29):

$$C \frac{dv_o}{dt} = K \left[ 2(V_{GS} - V_T)v_o - v_o^2 \right], \text{ and integrating} \quad (42)$$

$$\int_{-9}^{-1.5} \frac{dv_o}{-v_o^2 + 2(-9)v_o} = \frac{K}{C} \int_{t'}^{t_f} dt, \text{ therefore}$$

$$t_f - t' = - \frac{C}{9K} \tanh^{-1} \frac{-v_o - 9}{9} \Bigg|_{-9}^{-1.5}$$

$$= - \frac{C}{9K} (-1.2), \text{ and}$$

$$t_f = \frac{1.2C}{9K} + \frac{6C}{81K} = \frac{16.8C}{81K} = \frac{16.8C}{81K' \frac{W}{L}} . \quad (43)$$

For the same reason a small value was selected of

$t_f = 55$  nsec. Then the W/L ratio of  $Q_{29}$  is given by

equation (43):

$$\left(\frac{W}{L}\right)_{29} = \frac{(16.8)(20)(10^{-12})}{(81)(55)(10^{-9})(2.6)(10^{-6})} = 30 .$$

For the last bit of this shift register illustrated in Figure 14, one inverter of the pair is always conducting DC. When point E goes to a logical "1", the current from  $Q_{27}$  goes to charge  $C_9$  and  $Q_{27}$  is saturated.

Equation (40) gives

$$\frac{W}{L} = \frac{9 C_9}{t(V_{GS} - V_T)K'}$$

Assuming the duty cycle is 40%, then

$$t = \frac{1}{800KC} \times 40\% = 0.5 \mu\text{sec}.$$

From equations (7) and (8) the capacitance of  $C_9$ , which is due to the gate area of  $Q_{30}$  and the diffused area which is common to  $Q_{27}$ ,  $Q_{26}$ , and  $Q_{28}$ , is estimated to be 2.1 pf.

Therefore

$$\left(\frac{W}{L}\right)_{27} = \frac{(9)(2.1)(10^{-12})}{(0.5)(10^{-6})(27-6-1.5)(2.6)(10^{-6})} = 0.75$$

When point E goes to a logical "0", current flows through the load  $Q_{27}$  and the inverter  $Q_{26}$ .

From equation (27) the power consumption is

$$\begin{aligned} P &= V_{DD}K(V_{GS} - V_T)^2 \\ &= (27)(0.75)(2.6)(10^{-6})(27-1.506)^2 = 20 \text{ mw}. \end{aligned}$$

In order to calculate the  $W/L$  of  $Q_{26}$ , the normalized input and output voltages have to be determined.  $Q_{27}$  is

saturated and the on-level is assumed to be -1.5 volts, which gives a normalized output voltage of

$$\frac{v'_o}{V_{GG}-V_T} = \frac{-1.5}{-(27-6)} = \frac{1.5}{21} = 0.0713 .$$

The normalized input voltage is

$$\frac{V_{in}-V_T}{V_{GG}-V_T} = \frac{-(15-6)}{-(27-6)} = \frac{9}{21} = 0.428 .$$

Next, using the above results in equation (19) or Figure 8, we find

$$\frac{K_I}{K_L} = \frac{\left(\frac{W}{L}\right)_{26}}{\left(\frac{W}{L}\right)_{27}} = 16 .$$

However, as a margin of safety to insure that  $v'_o$  will be somewhat less than 1.5 volts, let

$$\frac{K_I}{K_L} = \frac{\left(\frac{W}{L}\right)_{26}}{\left(\frac{W}{L}\right)_{27}} = 20 .$$

Therefore,

$$(W/L)_{26} = (20)(0.75) = 15 .$$

The capacitance that  $Q_{24}$  must drive,  $C_g$ , is estimated to be 2.0 pf.

From equation (40),

$$(W/L)_{24} = 0.70 .$$

For the 4-bit and the 16-bit registers, the input is -15 volts.

From equation (19),

$$K_I/K_L = 20 .$$

Therefore,

$$(W/L)_{23} = (20)(W/L)_{24} = (20)(0.7) = 14 .$$

The effect of the resistance of  $Q_{25}$  may be neglected when  $Q_{23}$  turns off if  $(W/L)_{25}/(W/L)_{24} \geq 5$  because the resistance of  $Q_{25}$  will be 1/5 that of  $Q_{24}$ . Choosing  $(W/L)_{25} = 4$  satisfies the above requirement that  $(W/L)_{25}/(W/L)_{24} \geq 5$ .

By the same reasoning,

$$(W/L)_{28} = 4 ,$$

$$(W/L)_{22} \geq 5(W/L)_{20} .$$

For the 1-bit register, the input is -11 volts, giving

$$\frac{v_o'}{V_{GG} - V_T} = 0.0713, \text{ and}$$

$$\frac{V_{in} - V_T}{V_{GG} - V_T} = \frac{-(11-6)}{-21} = 0.248 .$$

From equation (19),

$$K_I/K_L = 34 .$$

Therefore,

$$(W/L)_{23} = 34(W/L)_{24} = (34)(0.7) = 24 .$$

The W/L ratios of the other devices in the 1-bit are identical to the W/L ratios in the 4-bit and the 16-bit.

#### b. Next to Last Bit

The next to last bit is shown in Figure 15. The capacitance that  $Q_{20}$  must drive,  $C_7$ , is estimated to be 0.85 pf. Using equations (40), (27), and (19),

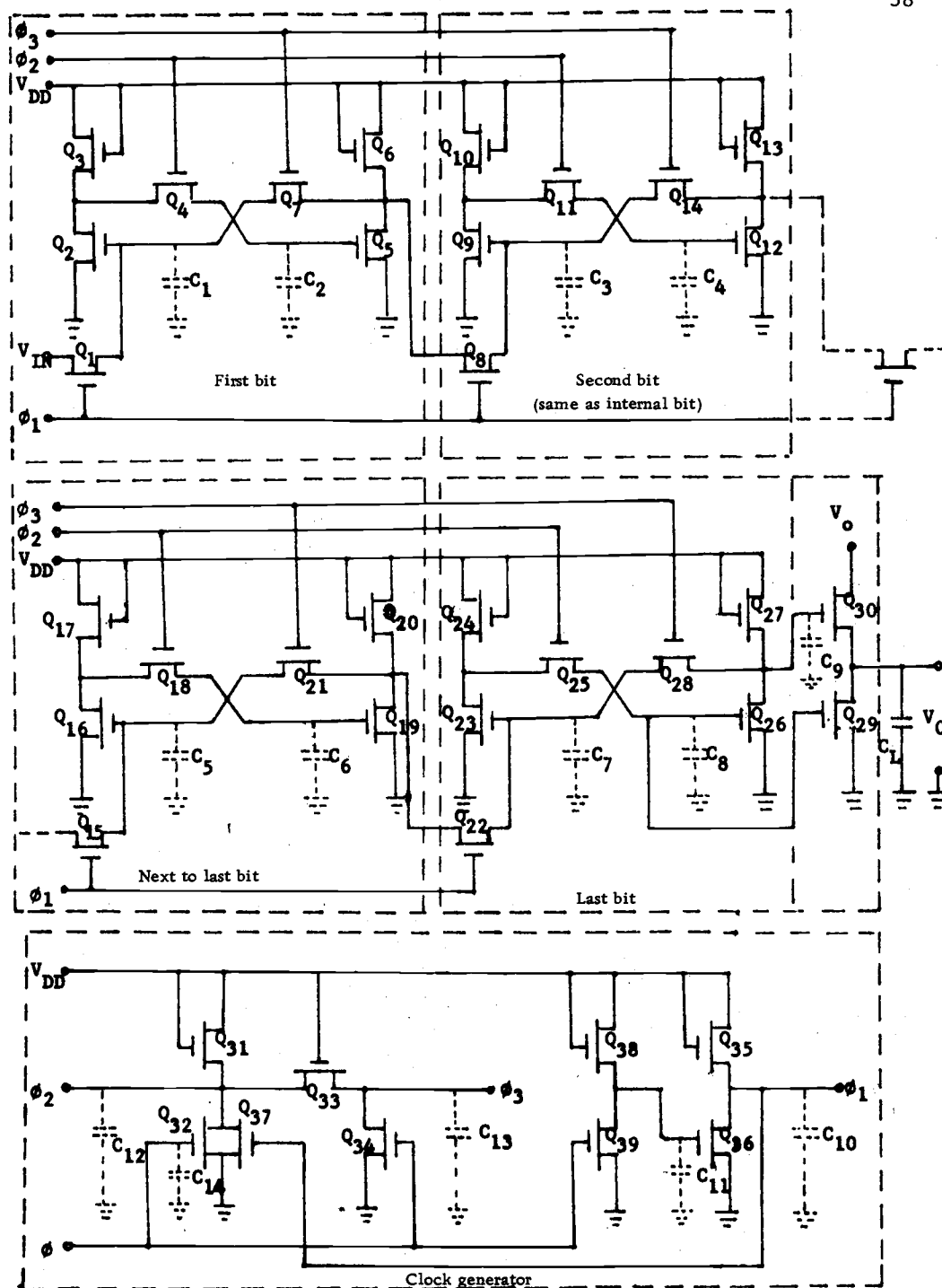


Figure 15. Circuit diagram of 21-bit static shift register.

$$(W/L)_{20} = 0.3,$$

$P = 5\text{mw}$ , and

$$(W/L)_{19} = (20)(0.3) = 6 .$$

$$(W/L)_{22} \geq 5(W/L)_{20} = 2 .$$

The capacitance that  $Q_{17}$  must drive,  $C_6$ , is estimated to be 0.42 pf. Therefore,

$$(W/L)_{17} = 0.15, \text{ and}$$

$$(W/L)_{16} = (20)(0.15) = 3 .$$

By the same reasoning used for  $Q_{25}$ ,

$$(W/L)_{21} = 2 ,$$

$$(W/L)_{18} = 2 ,$$

$$(W/L)_{15} = 1.5 .$$

### c. Internal Bit and First Bit

The first and internal bits are shown in Figure 15. For a typical internal bit, the capacitance is estimated to be 0.3 pf.

Repeating the calculations used above, we get

$$(W/L)_{13} = (W/L)_{10} = 0.1,$$

$$(W/L)_{12} = (W/L)_9 = 2 ,$$

$$(W/L)_{11} = 1.5,$$

$$(W/L)_{14} = 1.0,$$

$$(W/L)_8 = 1.5,$$

$$P = 2.7 \text{ mw} .$$

With the exception of  $Q_2$ , the  $W/L$  ratios of the devices in the first bit are identical to the  $W/L$  ratios in the

internal bits. The W/L ratio of  $Q_2$  in the first bit is different because the input voltage is -11 volts.

Using the same calculation as for  $Q_{23}$  of the 1-bit register,

$$(W/L)_2 = 4 .$$

The total power consumption of 21 bits is  
 $(20)(3) + (5)(2) + (2.7)(16) = 113.2 \text{ mw}.$

#### d. Clock Generator

For long-term data storage in the register shown in Figure 12 both clocks,  $\phi_2$  and  $\phi_3$ , must be present to lock the flip-flop in a stable state. This requires  $\phi_2$  and  $\phi_3$  to be at a negative level (logic 1) and  $\phi_1$  at zero level (logic 0). However, during the transfer of information into the register,  $\phi_2$  and  $\phi_3$  are required to be at a zero level (logic 0) and  $\phi_1$  at negative level (logic 1).

Based on the requirements described above, a generator circuit is shown in Figure 16.

This circuit requires only one external clock input,  $\phi$ , for operation. Three clocks,  $\phi_1$ ,  $\phi_2$  and  $\phi_3$  are generated internally.  $\phi_1$  is generated in phase with  $\phi$ .  $\phi_2$  and  $\phi_3$  are generated 180 degrees out of phase with  $\phi$ .  $\phi_3$  is delayed slightly with respect to  $\phi_2$  to eliminate a race condition. The time delay is generated by the RC time constant consisting of  $Q_{31}$ ,  $Q_{33}$ ,  $C_{12}$  and  $C_{13}$ .

The capacitance that  $Q_{35}$  must drive,  $C_{10}$ , is

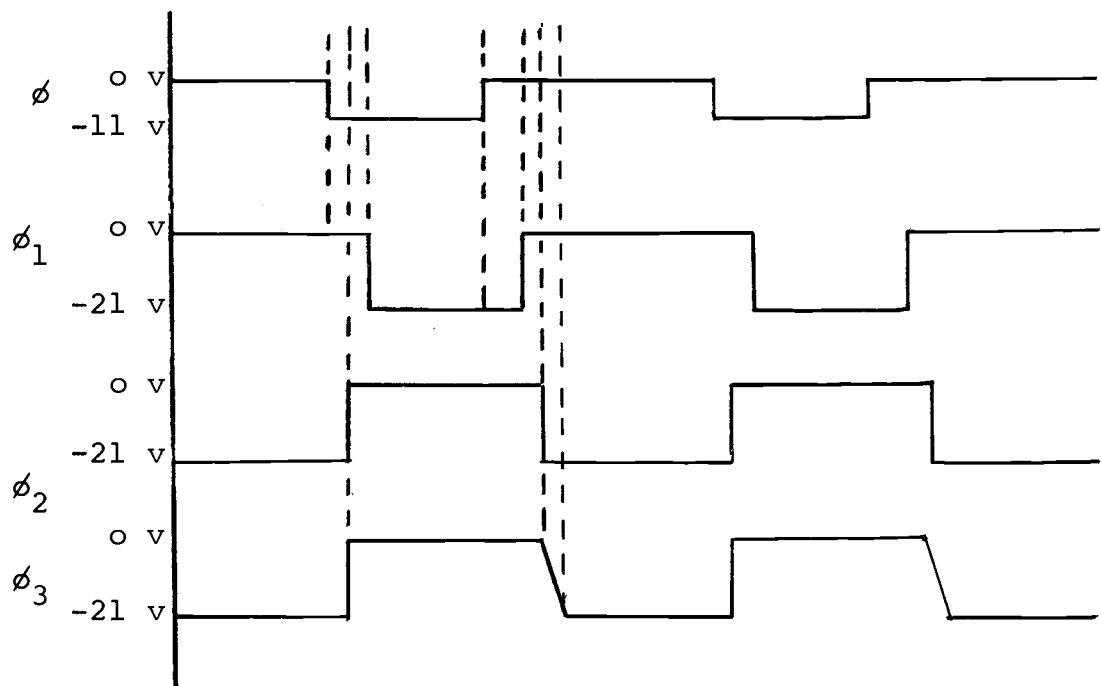
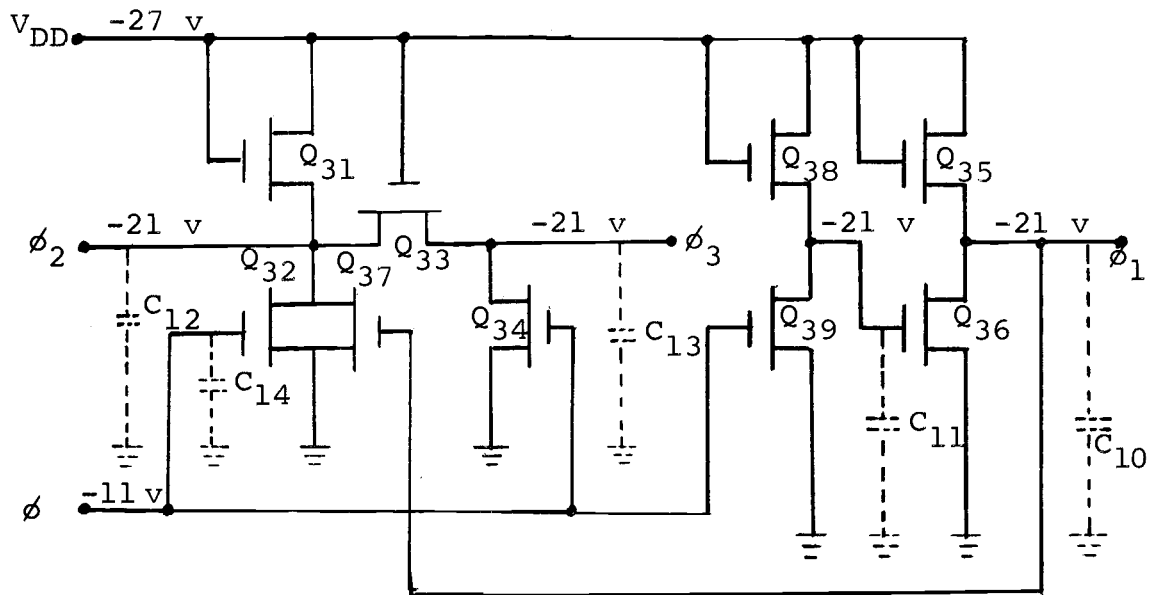


Figure 16. Circuit diagram of internal clock generation with timing diagram of the four clock phases.

approximately 2.8 pf. Using equations (40) and (27),

$$(W/L)_{35} = 1.0, \text{ and}$$

$$P = 27 \text{ mw.}$$

The input voltage is -21 volts. Thus from equation (19),

$$(W/L)_{36} = 20 .$$

The capacitance that  $Q_{38}$  must drive,  $C_{11}$ , is estimated to be 0.9 pf. Therefore,

$$(W/L)_{38} = 0.33, \text{ and}$$

$$P = 9 \text{ mw.}$$

The input voltage is -11 volts. Then

$$(W/L)_{39} = 15 .$$

The capacitance that  $Q_{31}$  must drive,  $C_{12}$  and  $C_{13}$ , is estimated to be 3.3 pf. Therefore,

$$(W/L)_{31} = 1.2, \text{ and}$$

$$P = 32 \text{ mw.}$$

The input voltage is -11 volts. Then

$$(W/L)_{32} = (W/L)_{37} = 42 .$$

The power consumption of the generator is

$$P_G = 27+9+32 = 68 \text{ mw.}$$

$Q_{31}$  is saturated. From equation (5),

$$\begin{aligned} (g_m) &= 2K(V_{GS}-V_T) \\ &= (2)(2.6)(10^{-6})(1.2)(-27+1.5+6) \\ &= 122(10^{-6}) \text{ mho.} \end{aligned}$$

The gates that  $\phi_3$  operate are only effective at frequencies below 10 KHz. They are not needed at the higher frequencies, therefore the charging time of  $\phi_3$  can be

much slower than  $\phi_2$ . To insure that  $\phi_3$  is delayed with respect to  $\phi_2$  (assuming that the charging time of  $\phi_2$  is 20 times faster than  $\phi_3$ ), then

$$20 R_{31} C_{12} = (R_{31} + R_{33}) C_{13},$$

$$(20) \left[ \frac{C_{12}}{(g_m)_{31}} \right] = \left[ \frac{1}{(g_m)_{31}} + \frac{1}{(g_m)_{33}} \right] C_{13},$$

where

$$C_{12} = 1.217 \text{ pf},$$

$$C_{13} = 1.32 \text{ pf},$$

$$(g_m)_{33} = 6.9 (10^{-6}) \text{ mho}.$$

From equation (5):

$$(W/L)_{33} = \frac{(g_m)_{33}}{2K'(V_{GS} - V_T)} = 0.068.$$

To prevent  $\phi_3$  from turning on  $Q_7$ ,  $Q_{14}$ ,  $Q_{22}$ , and  $Q_{28}$  while  $\phi_1$  is negative (logic 1) the W/L ratio from  $Q_{34}$  is found from equation (19) to be

$$(W/L)_{34} = 7.$$

#### IV. EXPERIMENTAL RESULTS

##### a. Design

The total power consumption of the entire circuit is  
 $P_T = 113.2 \text{ mw} + 68 \text{ mw} = 181.2 \text{ mw}.$

The W/L ratios of the devices of the 21-bit static shift register in this design are shown in Table II. The widths and lengths shown in the table are the dimensions of the first oxidation removal patterns on the fabrication mask. The lateral diffusion of p-regions beyond the oxide edges is approximately 0.1 mil. Consequently, 0.2 mils must be subtracted from the first oxide removal dimensions.

The basic cells were first drawn by hand as shown in Figure 17. Using punch cards, this information was fed into a computer which drew the basic cells shown in Figures 18 to 23. The scale is 500:1 (1 inch = 500 mils). The computer then generated the total physical layout shown in Figure 24 and also cut the Rubylith. Mask making and processing were done by standard Texas Instruments procedures.

Table II. W/L Ratios of 21-bit Static Shift Register

First Bit of 4-bit S.R. and 16-bit S.R.      Second Bit of 4-bit S.R. and 16-bit S.R.  
(Same as internal bit)

Devices	W/L	W <sup>(2nd)</sup> (OR.mils)	L <sup>(1st)</sup> (OR.mils)
Q <sub>1</sub>	1.5	0.3	0.4
Q <sub>2</sub>	4.0	0.8	0.4
Q <sub>3</sub>	0.1	0.3	3.2
Q <sub>4</sub>	1.5	0.3	0.4
Q <sub>5</sub>	2.0	0.4	0.4
Q <sub>6</sub>	0.1	0.3	3.2
Q <sub>7</sub>	1.0	0.3	0.5

Devices	W/L	W <sup>(2nd)</sup> (OR.mils)	L <sup>(1st)</sup> (OR.mils)
Q <sub>8</sub>	1.5	0.3	0.4
Q <sub>9</sub>	2.0	0.4	0.4
Q <sub>10</sub>	0.1	0.3	3.2
Q <sub>11</sub>	1.5	0.3	0.4
Q <sub>12</sub>	2.0	0.4	0.4
Q <sub>13</sub>	0.1	0.3	3.2
Q <sub>14</sub>	1.0	0.3	0.5

Next to Last Bit of 4-bit S.R. and  
16-bit S.R.

Devices	W/L	W <sup>(2nd)</sup> (OR.mils)	L <sup>(1st)</sup> (OR.mils)
Q <sub>15</sub>	1.5	0.3	0.4
Q <sub>16</sub>	3.0	0.6	0.4
Q <sub>17</sub>	0.15	0.3	2.2
Q <sub>18</sub>	2.0	0.4	0.4
Q <sub>19</sub>	6.0	1.2	0.4
Q <sub>20</sub>	0.3	0.3	1.2
Q <sub>21</sub>	2.0	0.4	0.4

Last Bit of 4-bit S.R. and 16-bit S.R.

Devices	W/L	W <sup>(2nd)</sup> (OR.mils)	L <sup>(1st)</sup> (OR.mils)
Q <sub>22</sub>	2.0	0.4	0.4
Q <sub>23</sub>	14.0	2.8	0.4
Q <sub>24</sub>	0.7	0.3	0.6
Q <sub>25</sub>	4.0	0.8	0.4
Q <sub>26</sub>	15.0	3.0	0.4
Q <sub>27</sub>	0.75	0.3	0.6
Q <sub>28</sub>	4.0	0.8	0.4

Table II (Continued).

Last Bit of 1-bit S.R.			
Devices	W/L	W (2nd OR.mils)	L (1st OR.mils)
Q <sub>22</sub>	2.0	0.4	0.4
Q <sub>23</sub>	24.0	4.8	0.4
Q <sub>24</sub>	0.7	0.3	0.6
Q <sub>25</sub>	4.0	0.8	0.4
Q <sub>26</sub>	15.0	3.0	0.4
Q <sub>27</sub>	0.75	0.3	0.6
Q <sub>28</sub>	4.0	0.8	0.4

Output Buffer			
Devices	W/L	W (2nd OR.mils)	L (1st OR.mils)
Q <sub>29</sub>	30.0	6.0	0.4
Q <sub>30</sub>	60.0	12.0	0.4

Clock Generator			
Devices	W/L	W (2nd OR.mils)	L (1st OR.mils)
Q <sub>31</sub>	1.2	0.3	0.45
Q <sub>32</sub>	42.0	8.4	0.4
Q <sub>33</sub>	0.068	0.3	4.6
Q <sub>34</sub>	7.0	1.4	0.4
Q <sub>35</sub>	1.0	0.3	0.50
Q <sub>36</sub>	20.0	4.0	0.4
Q <sub>37</sub>	42.0	8.4	0.4
Q <sub>38</sub>	0.33	0.3	1.2
Q <sub>39</sub>	15.0	3.0	0.4

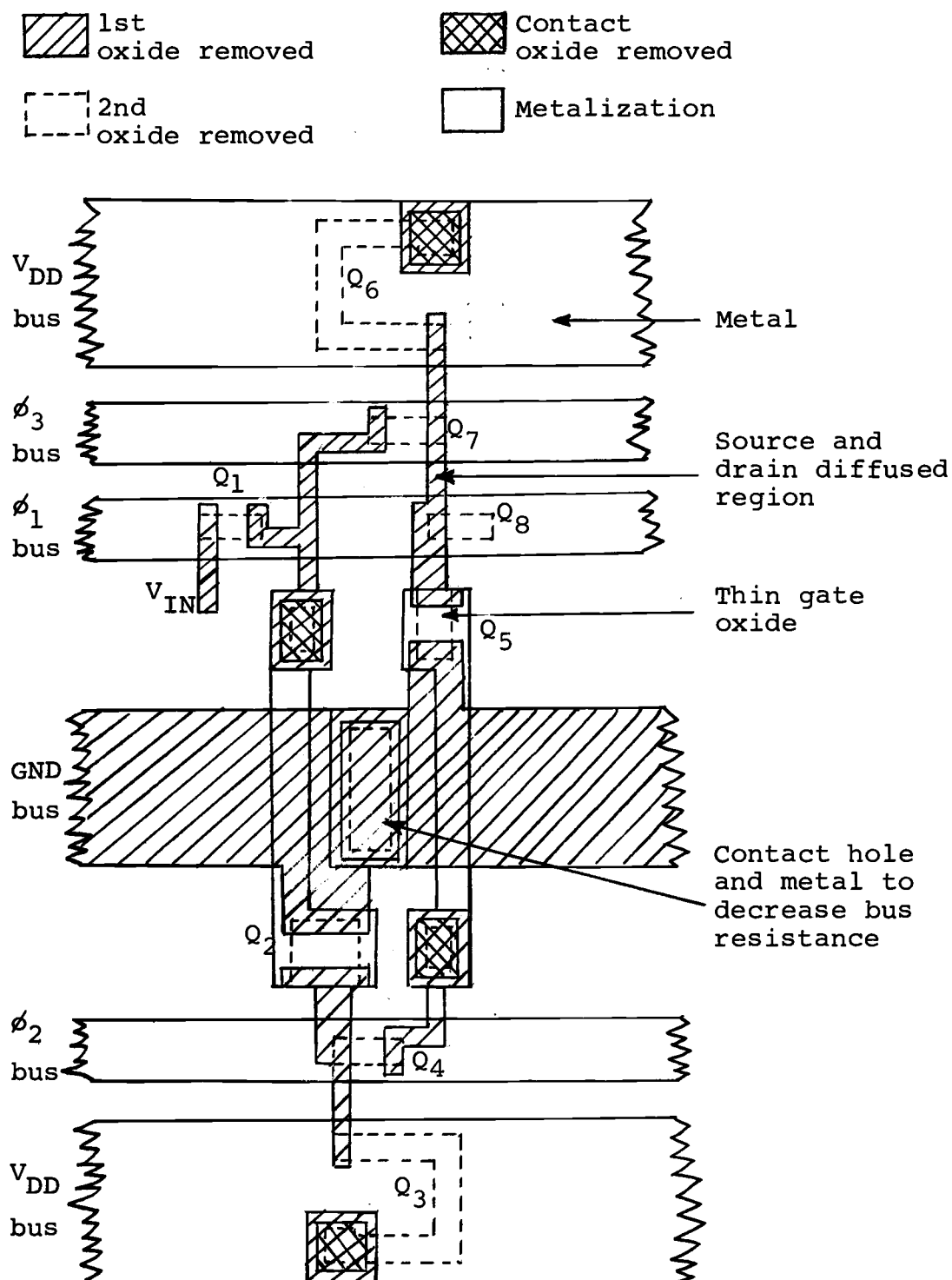


Figure 17. Basic cell of first bit of 4-bit static shift register and 16-bit static shift register (Scale 500:1).

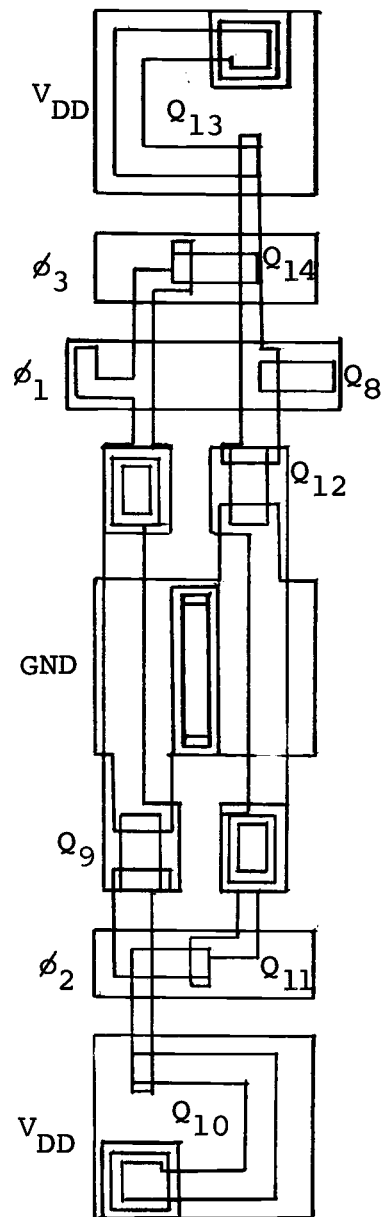


Figure 18. Basic cell of second bit of 4-bit static shift register and 16-bit static shift register (Scale 500:1). (Print of computer drawn diagram)

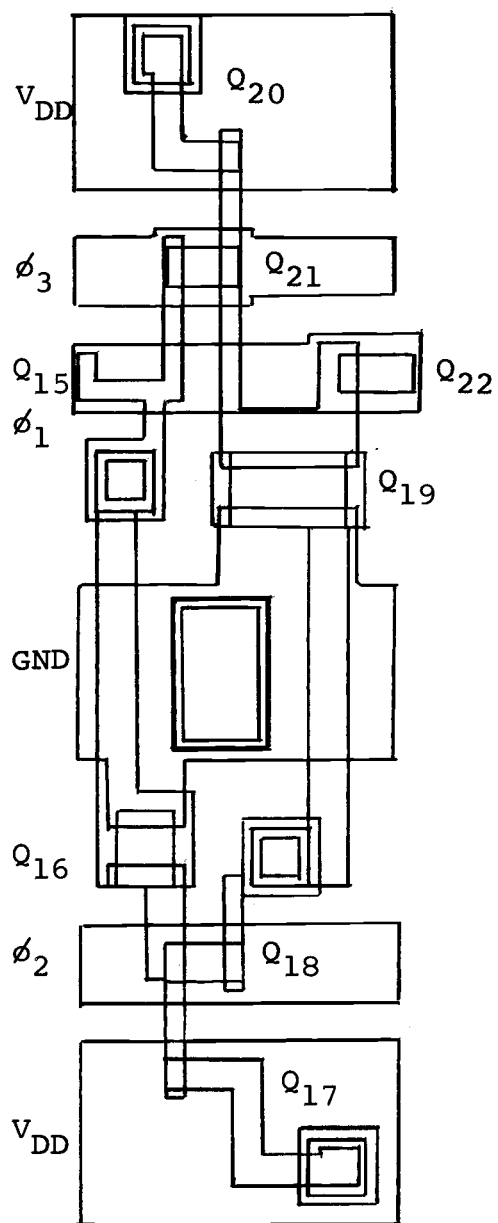


Figure 19. Basic cell of next to last bit of 4-bit static shift register and 16-bit static shift register (Scale 500:1). (Print of computer drawn diagram)

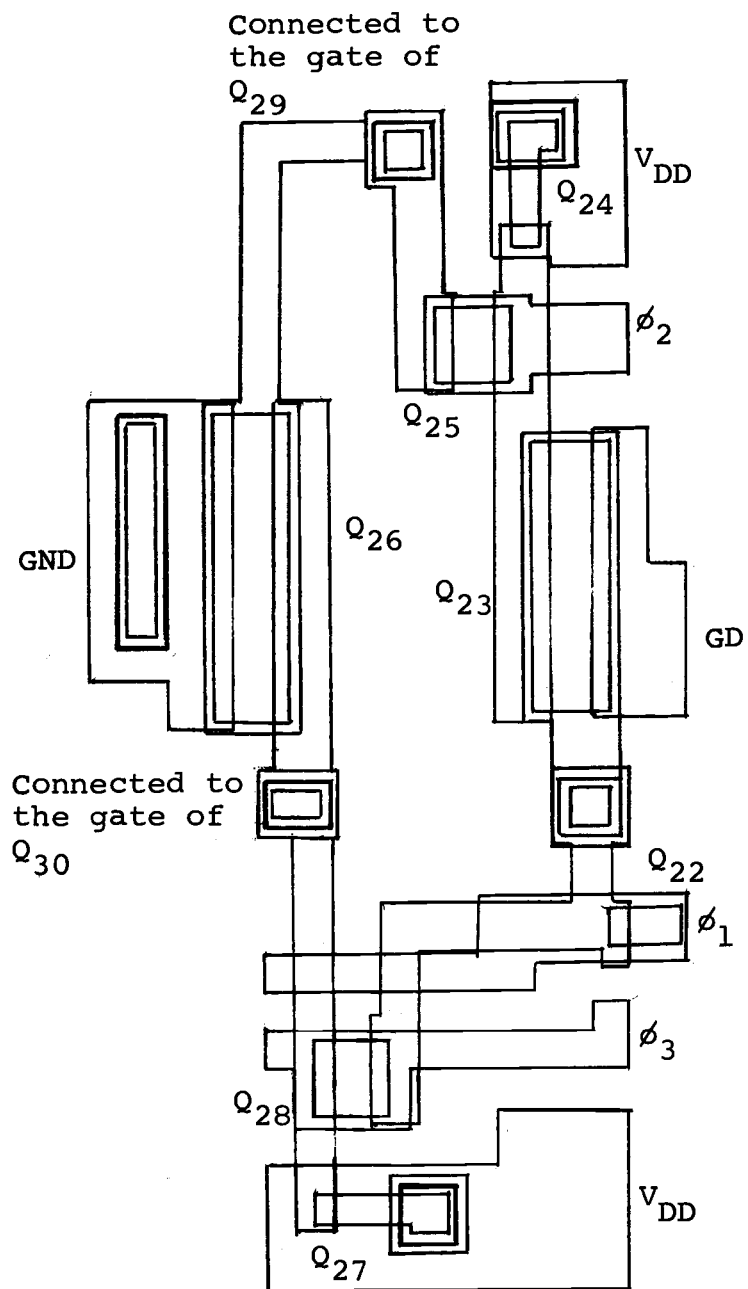


Figure 20. Basic cell of last bit of 4-bit static shift register and 16-bit static shift register (Scale 500:1). (Print of computer drawn diagram)

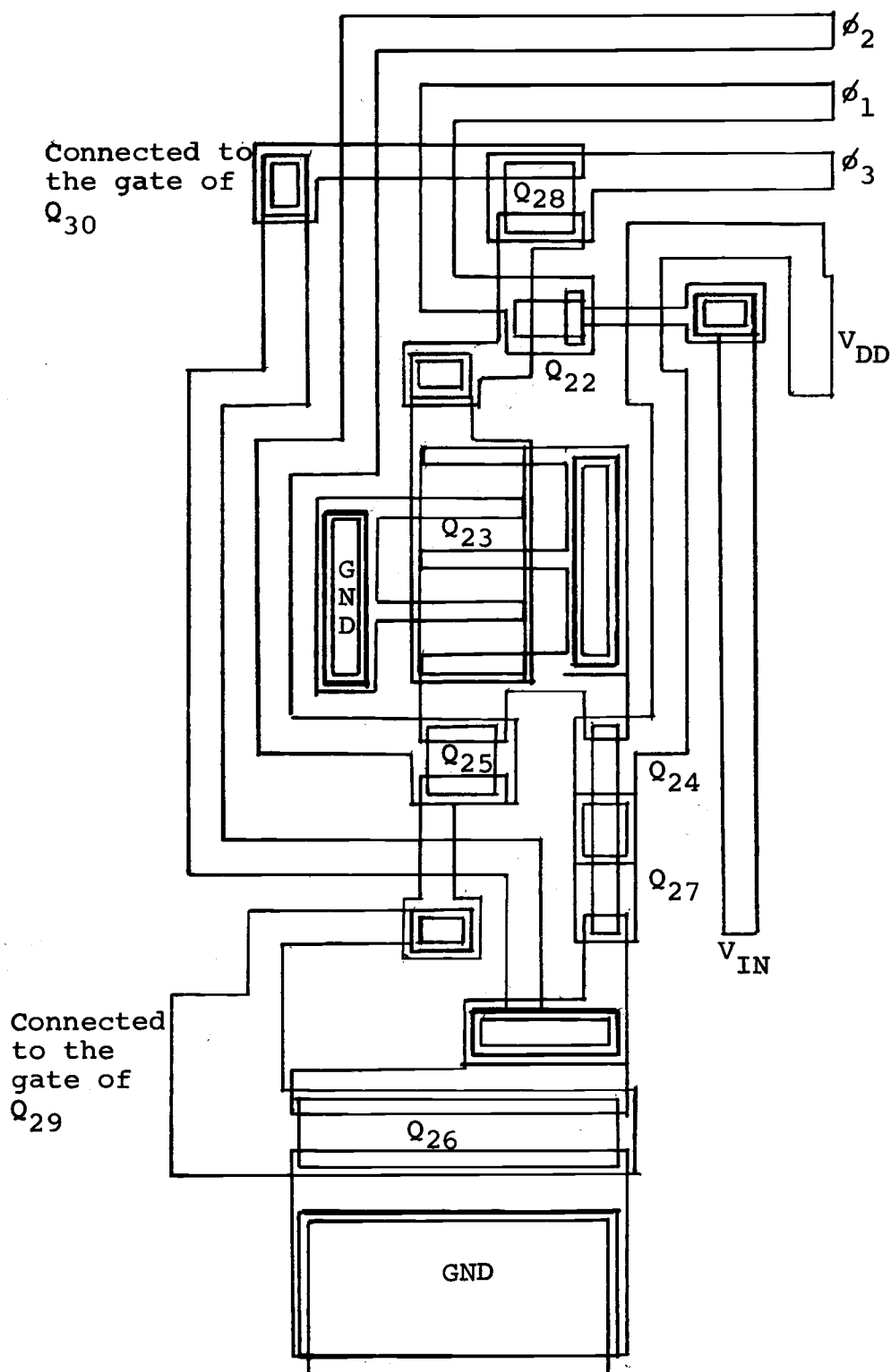


Figure 21. Basic cell of last bit of 1-bit static shift register (Scale 500:1). (Print of computer drawn diagram)

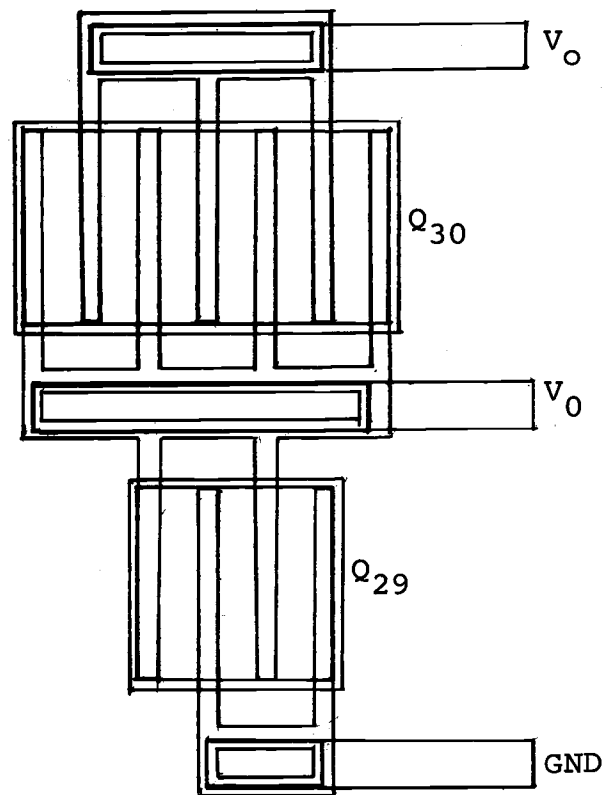


Figure 22. Basic cell of output push-pull buffer (Scale 500:1).  
(Print of computer drawn diagram)

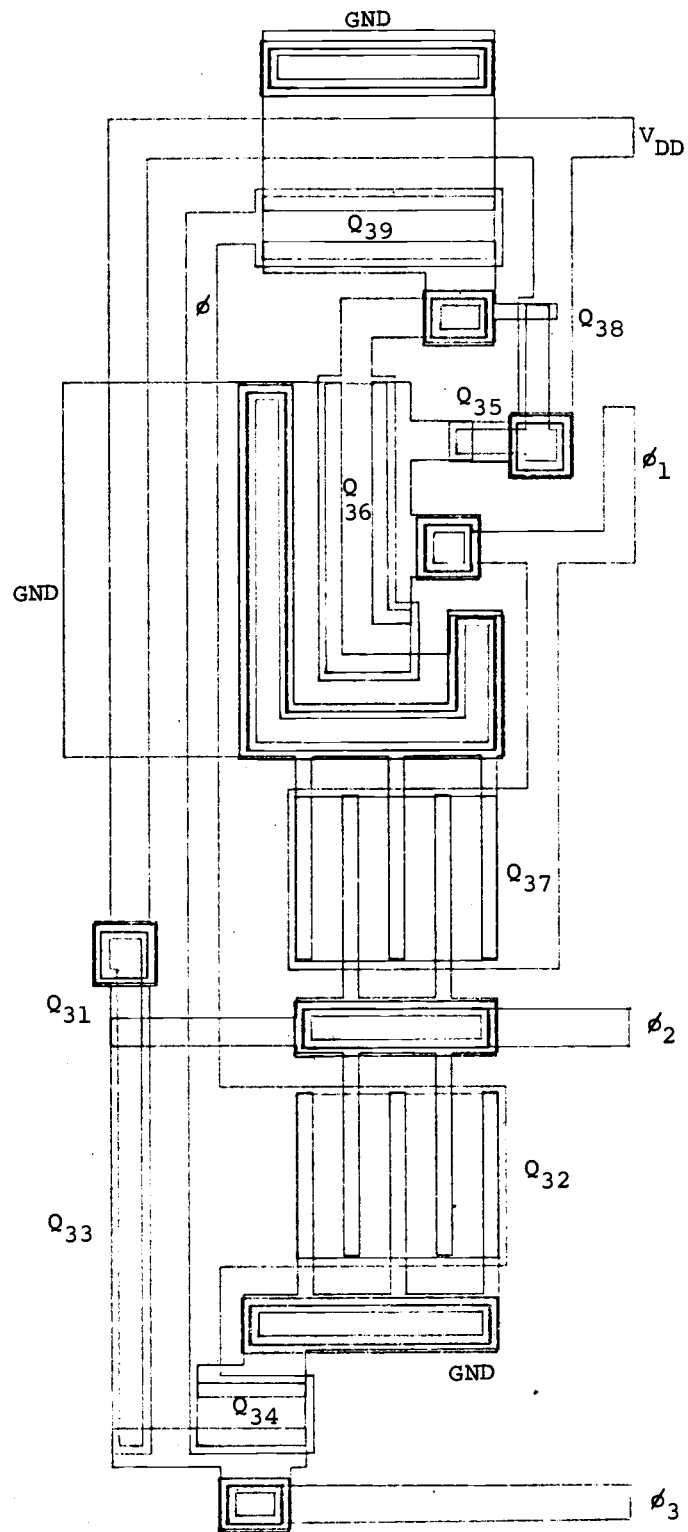


Figure 23. Basic cell of clock generator.  
(Print of computer drawn diagram)

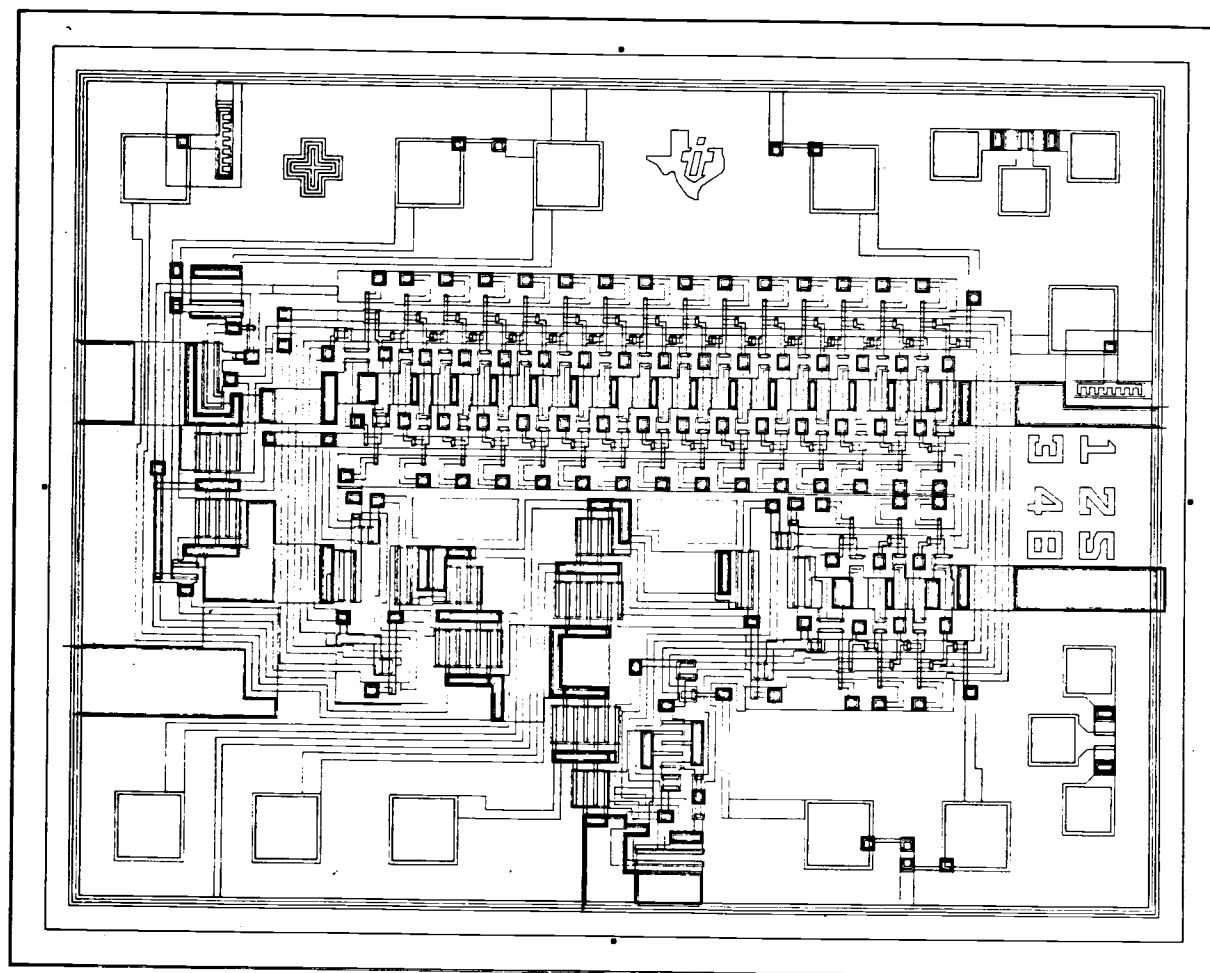


Figure 24. Physical layout of 21-bit static shift register.  
(Print of computer drawn diagram)

The functions of the terminals shown in Figure 25 are as follows:

<u>Terminal Number</u>	<u>Function</u>
1	Data input of 16-bit static shift register.
2	Clock input ( $\phi$ ).
3	Buffer supply voltage ( $-V_O$ ).
4	Data output of 16-bit static shift register.
5	Ground.
6	Data output of 4-bit static shift register.
7	Data output of 1-bit static shift register.
8	Data input of 1-bit static shift register.
9	Data input of 4-bit static shift register.
10	Drain voltage ( $-V_{DD}$ ).

Data entered into an n bit static shift register will appear at the output n clock pulses later.

To obtain a 1-bit static shift register use terminals 8 and 7. To obtain a 4-bit static shift register, use terminals 9 and 6. To obtain a 16-bit static shift register, use terminals 1 and 4. To obtain a 5-bit static shift register use terminals 9 and 7, connect terminal 6 to terminal 8. To obtain a 17-bit static shift register use terminals 1 and 7, connect terminal 4 to terminal 8. To obtain a 20-bit static shift register use terminals 1 and 6, connect terminal 4 to terminal 9. And to obtain a 21-bit static shift register use terminals 1 and 7, connect terminal 4 to terminal 9 and terminal 6 to terminal 8.

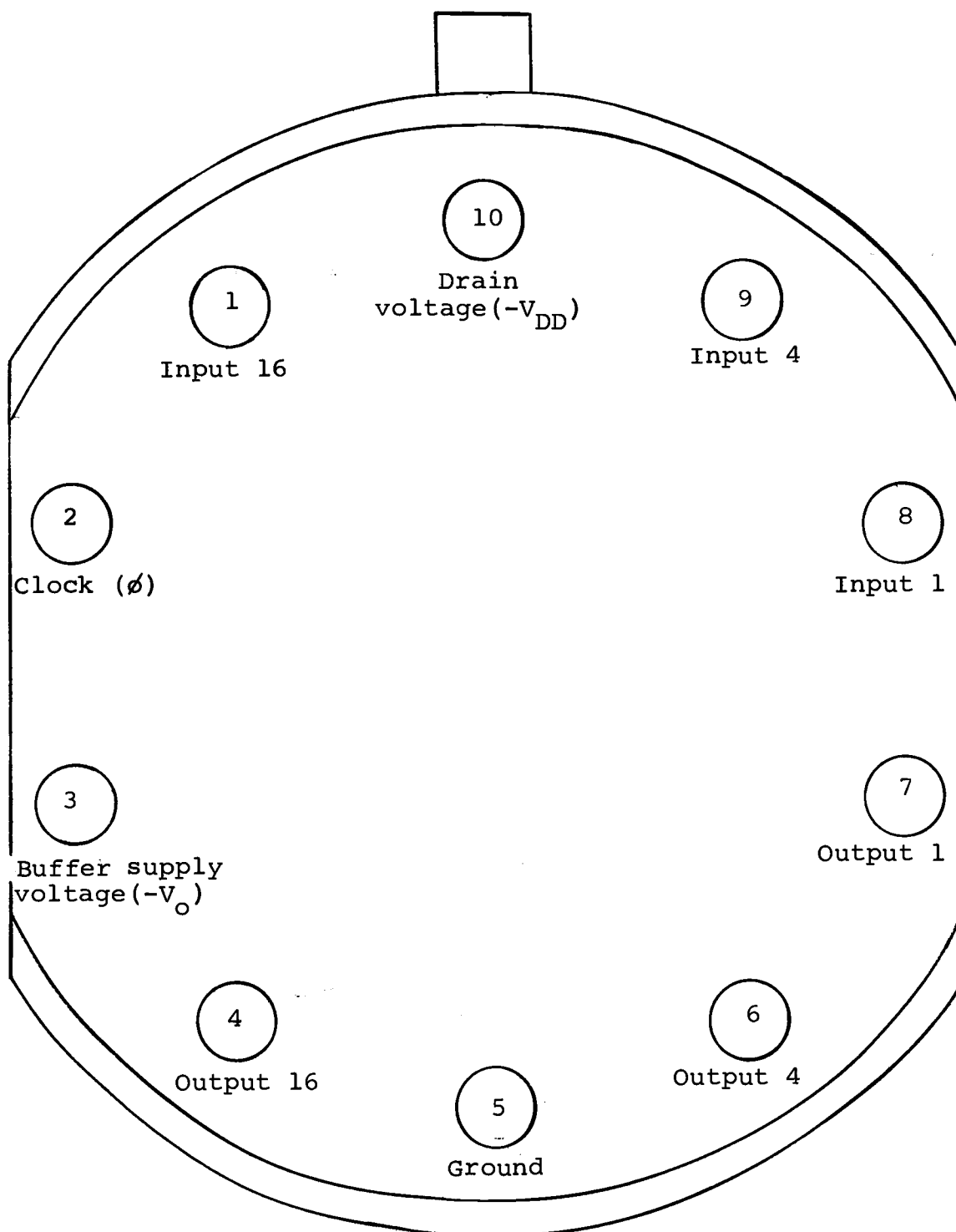


Figure 25. Connection diagram of 21-bit static shift register. (Top view)

### b. Electrical Characteristics

The following is a tabulation of the calculated and experimental electrical characteristics for the 21-bit static shift register. Figure 26 shows the calculated timing diagram, and Figures 27 to 34 show the experimental waveforms. The calculated results agree with those obtained experimentally. The data were obtained from measurements on five circuits with the average values shown.

A statistical analysis was used to determine the linear regression line of best fit to the data for power consumption versus drain supply voltage. The regression line is shown in Figure 35. The linear regression was  $Y = -346.96 + 19.1X$ , with variance about regression line  $S^2 = 7.48$ .

# OPERATING CONDITIONS

$V_{DD} = -28 \text{ Volts} \pm 1 \text{ Volt}$ ,  $V_O = -28 \text{ Volts} \pm 1 \text{ Volt}$

Load = 10 M $\Omega$  and 10 pf,  $T_A = 0^\circ\text{C}$  to  $+85^\circ\text{C}$

Characteristics	Min.	Typ $T_A=25^\circ\text{C}$	Max.	Experimental Measurements	Units	Conditions
Clock Repetition Rate	D.C.	---	0.8	DC-1.4	MHz	
Clock Pulse Widths ( $\phi$ pw)	0.8	---	10	0.6-12	$\mu\text{s}$	See Figure 26
Clock Pulse Rise and Fall Time ( $t_{rc}$ and $t_{fc}$ )	---	---	4	4	$\mu\text{s}$	See Figure 26
Clock Pulse Logic Levels ( $\phi$ )						
Logic "0"	---	0	-2.0	0	Volts	See Figure 26
Logic "1"	-10	-11		-11	Volts	See Figure 26
Clock Pulse Input Capacitance ( $\phi$ )	---	4.0	6.0	3.5	pF	$\phi=0 \text{ Volts}$ , $T_A=25^\circ\text{C}$
Clock Input Leakage Current	---	---	1.0	$1 \times 10^{-3}$	$\mu\text{A}$	$V_{in} = -20 \text{ Volts}$
Data Pulse Width (Dpw)	1.0	---	---	0.8	$\mu\text{s}$	See Figure 26

Operating Conditions (continued)

Characteristics	Min.	Typ $T_A=25^{\circ}\text{C}$	Max.	Experimental Measurements	Units	Conditions
Data Input Logic Levels						
Logic "0"	---	0	-2.0	0	Volts	
Logic "1"	-10	-11	---	-11	Volts	
Data Input Capacitance	---	1.5	2.0	1.5	pF	$V_{in}=0$ Volts, $T_A=25^{\circ}\text{C}$
Data Input Leakage Current	---	---	1.0	$1 \times 10^{-3}$	$\mu\text{A}$	$V_{in}= -20$ Volts
Output Logic Levels						
Logic "0"	---	0	-1.0	0	Volts	
Logic "1"	-11	-15	---	-17	Volts	
Output Logic "1" Response Time ( $t_1$ )	---	---	0.80	0.7	$\mu\text{s}$	See Figure 26
Output Logic "0" Response Time ( $t_0$ )	---	---	0.45	0.4	$\mu\text{s}$	See Figure 26
Output Impedance to Ground		1.2	3.0	1.2	$\text{K}\Omega$	Output Logic "0"
Output Drive Capability	-10	-11	---	-11	Volts	$R_L=17$ K to Ground
Output Drive Capability	-5.0	-8	---	-8	Volts	$R_L=4$ K to Ground
Power Supply Current Drain		6.7	9.1	6.3	mA	$V_{DD}= -27$ Volts

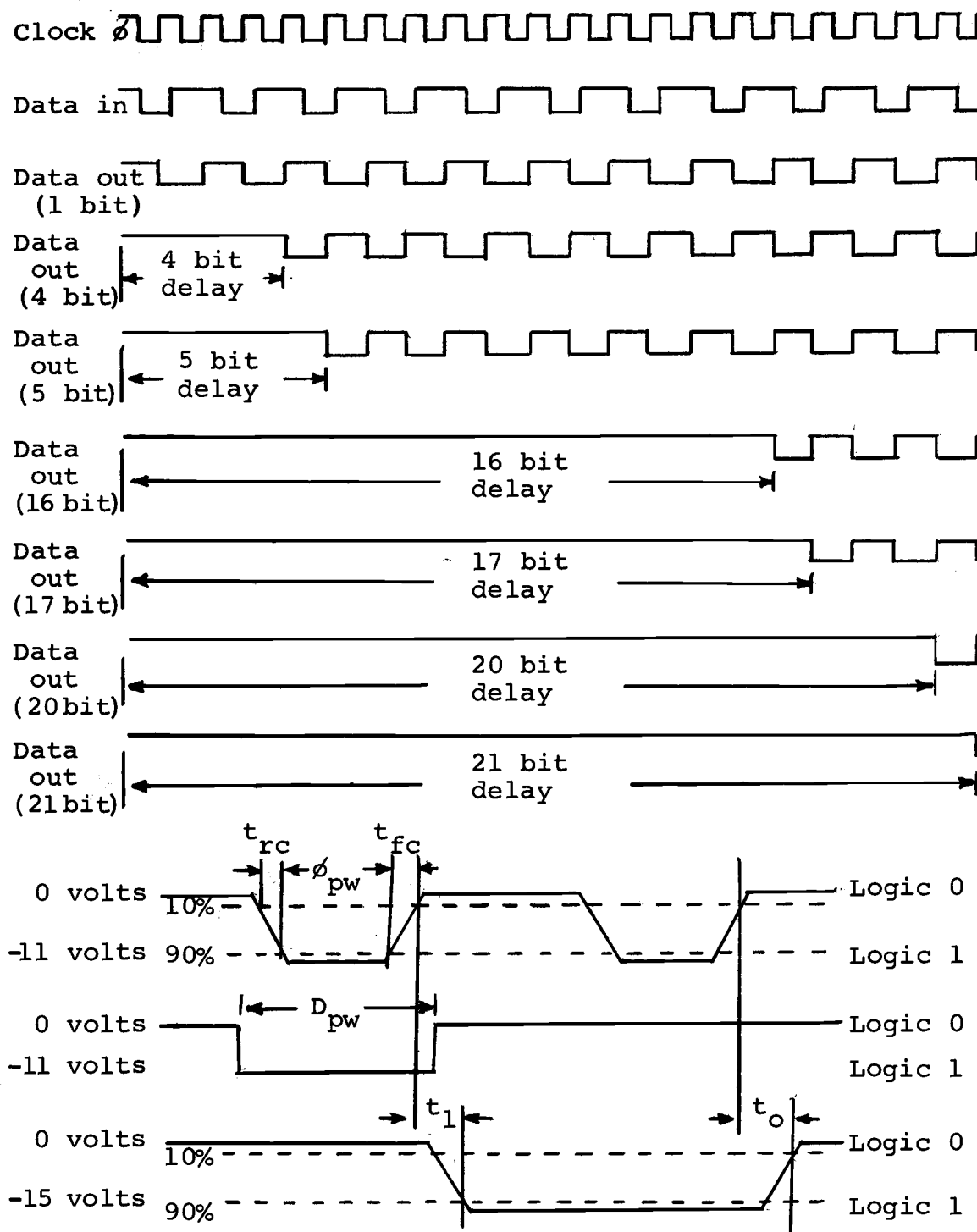


Figure 26. Typical timing diagram of 21-bit static shift register.

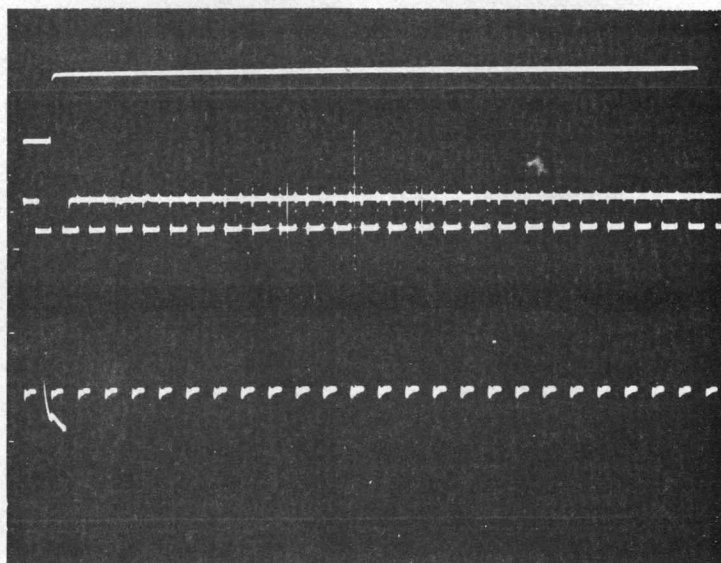


Figure 27. 1-bit static shift register waveforms. Top-input, center-output, bottom-clock.  
(hor.=5  $\mu$ sec/Div.,  
vert.= 5 volts/Div.)

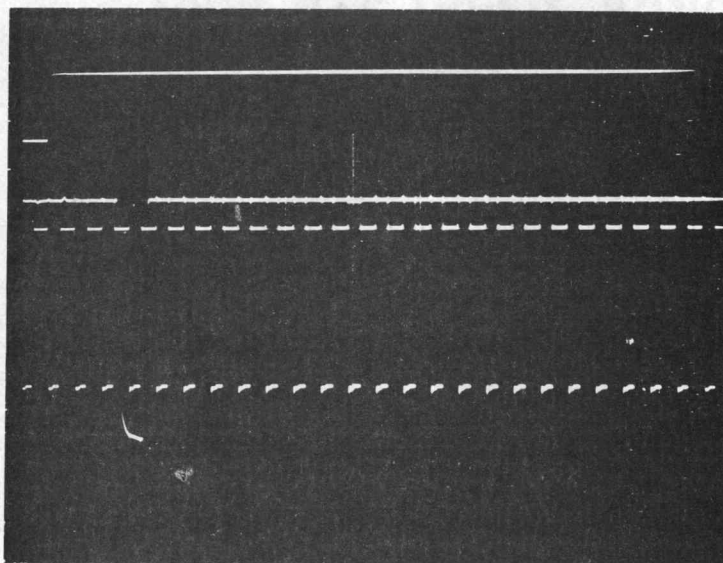


Figure 28. 4-bit static shift register waveforms.  
(hor.=5  $\mu$ sec/Div., vert.=5 volts/Div.)

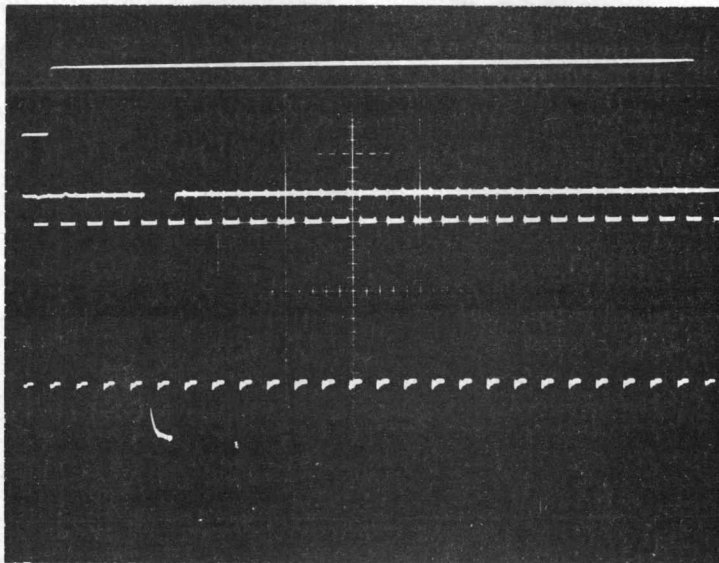


Figure 29. 5-bit static shift register waveforms.  
(hor.=5  $\mu$ sec/Div., vert.=5 volts/Div.)

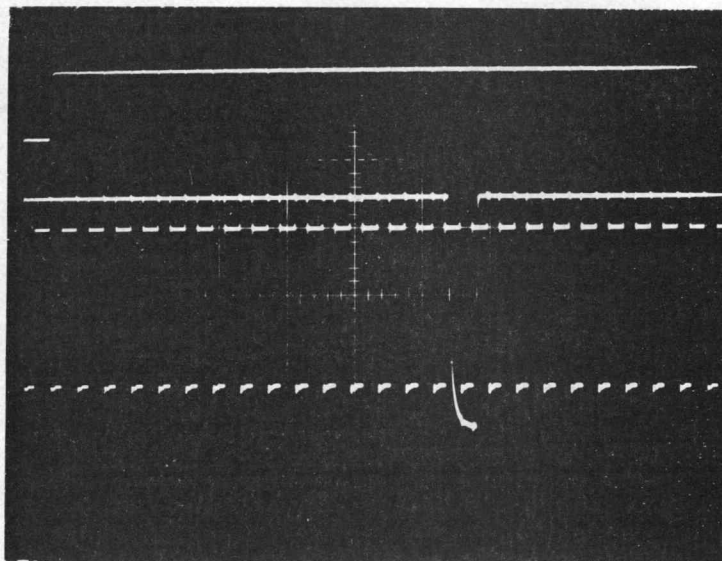


Figure 30. 16-bit static shift register waveforms.  
(hor.=5  $\mu$ sec/Div., vert.=5 volts/Div.)

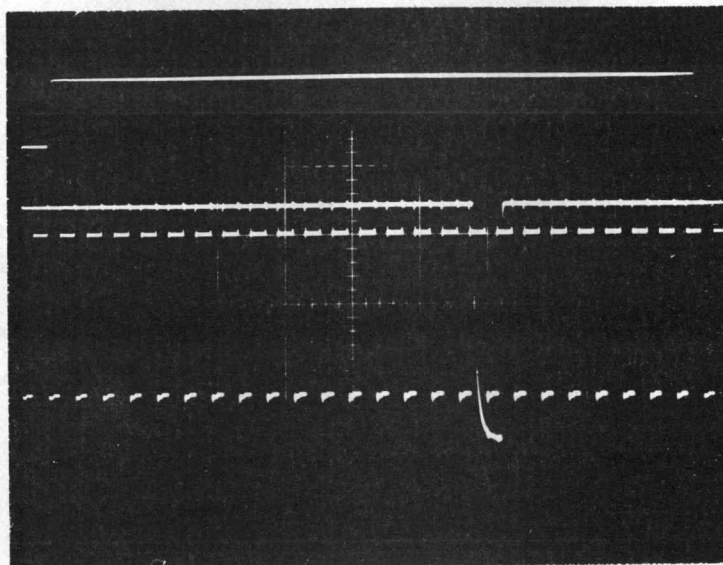


Figure 31. 17-bit static shift register waveforms.  
(hor.=5  $\mu$ sec/Div., vert.=5 volts/Div.)

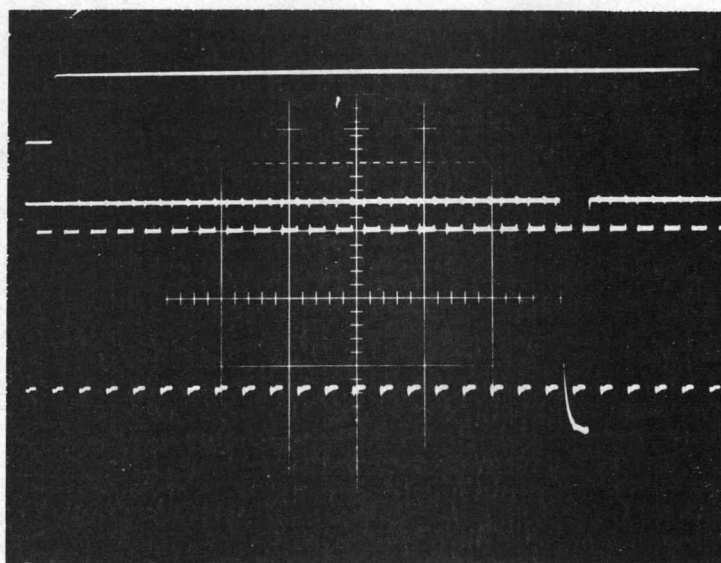


Figure 32. 20-bit static shift register waveforms.  
(hor.=5  $\mu$ sec/Div., vert.=5 volts/Div.)

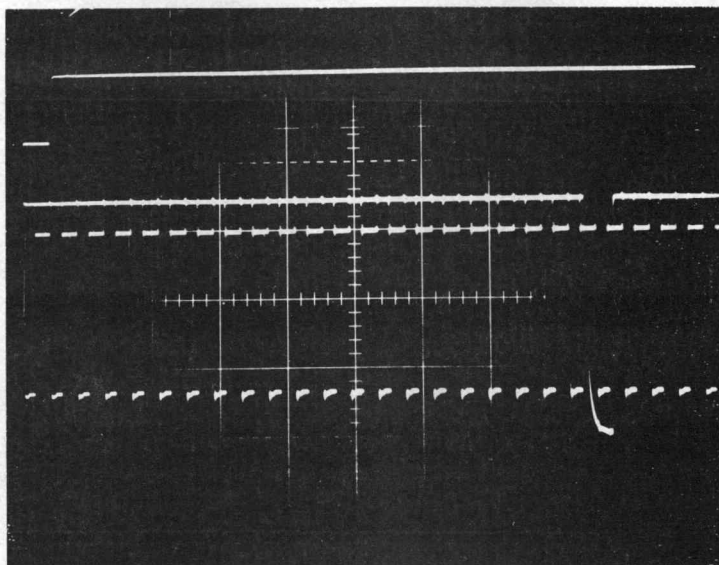


Figure 33. 21-bit static shift register waveforms.  
(hor.=5  $\mu$ sec., vert.=5 volts/Div.)

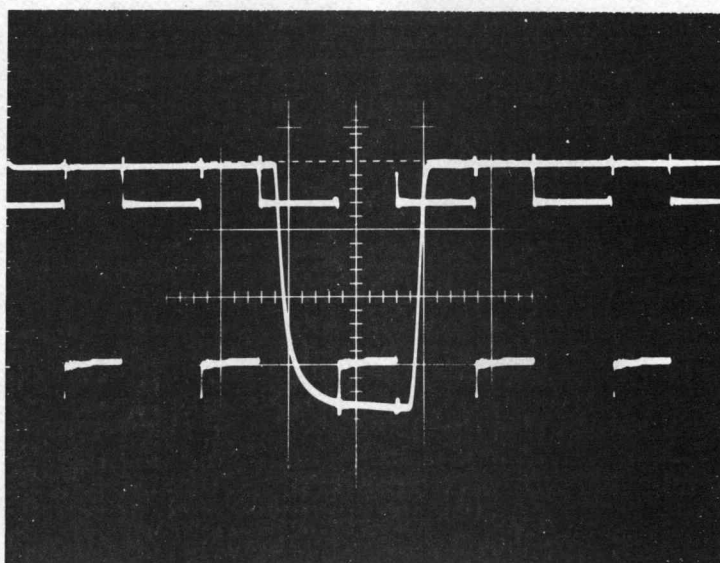


Figure 34. Rise and fall time of the output wave (top) with clock (bottom).  
(hor.=1  $\mu$ sec/Div., vert.= 5 volts/Div.)

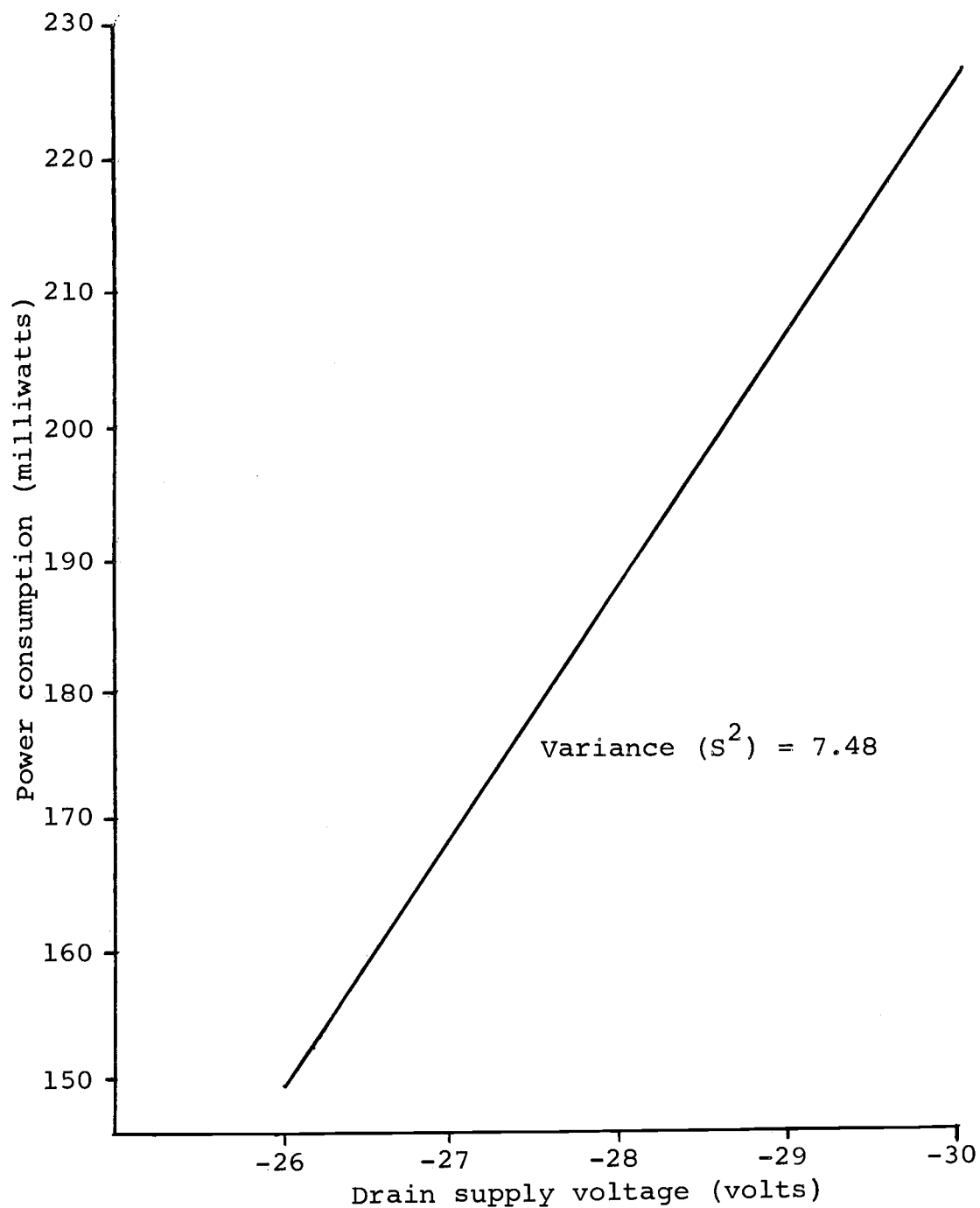


Figure 35. Linear regression line of best fit to the data for the power consumption versus drain supply voltage.

## V. CONCLUSIONS

This design, using a MOSFET static shift register with 162 active devices for multiple-bit serial operation, is a relatively complex circuit put on a single monolithic chip. It requires only one power supply and one external clock. Seven different bit lengths may be obtained by appropriate connections. The circuit performed very well, giving experimental results which agreed with those calculated. The frequency response and output level were actually better since the design was for worst-case conditions.

The use of MOSFET integrated circuits is increasing exponentially, their potential economy is being realized, and new areas of application will inevitably be opened. The economic advantages are due to structural compactness and fabrication simplicity; these factors favor economy through their beneficial effect on yield. The advantages of MOSFET shift registers, both in simplicity and in comparatively good performance, will insure an increasing use in the design of systems in the future.

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