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Un-Ku Moon

The world market for sensors is several hundred million dollars growing at an annual rate of 20 percent with accelerometers comprising 19 percent of the market. With an increasing market, a wide range of applications with varying degrees of resolution are in demand. Therefore, there is sufficient motivation for developing new architectures that are more accurate, reliable, less costly, and easy to implement in any given application. This research investigates a new proposed architecture intended to improve each of the mentioned motivations.

Capacitive sensors and their electrical interfaces measure the displacement of a suspended beam mass in response to an input acceleration. The studied architecture is a two-chip solution with the capacitive sensor and electrical interface fabricated independently. This two-chip approach has several advantages. The micro-machining process for capacitive sensors is difficult with lower yields than most VLSI technologies. By fabricating the electrical interface in a different process with higher yields and smaller geometries, the cost of the architecture is reduced. As micro-machining yields improve, this advantage will diminish in favor of single-chip integration of the sensor and interface. If the production volumes are high and a single-chip solution is best suited for a particular application, this architecture can be easily integrated on one chip. Another advantage of a two-chip solution is the ease of implementation. The sensor is able to be placed at the point of interest while the electrical interface can be placed in a more convenient location. Also, several sensors can be multiplexed to one electrical interface. Sensors can be replaced while keeping the interface circuitry intact. This lowers cost and increases reliability of the system. Given its flexibility, the architecture is easy to implement and maintain in most applications.

Over-sampling techniques through delta sigma modulation are used extensively in implementations of analog interfaces on VLSI technologies. The electrical interface to a capacitive sensor is no exception. There are several architectures available that measure capacitive displacement. Two popular approaches for the electrical interface are a demodulator and delta-sigma modulator architecture. The demodulator architecture is commercially used by Analog Devices Inc. in their ADXL50 and ADXL05 products. To further improve the accuracy of available sensors, the delta-sigma architecture is used in this investigation. There are techniques used in this research that improve the resolution of current delta-sigma interface architectures. The architecture is a third order delta-sigma modulator. With a higher order modulator, the quantization noise is further suppressed in the signal band increasing the accuracy. The integrator implements correlated double sampling (CDS) in order to suppress the negative affects of input offset due to mismatch and flicker (1/f) noise on dynamic range and SNDR. With the use of force-feedback and a digital differentiator, a third order system is realized. The force-feedback has three levels which can result in linearity degradation. To improve the linearity, a mismatch shaping scheme was implemented. The interface circuit was implemented in a 1.6-um, 5-volt, CMOS process.

The initial fabricated design experienced instability and functional problems. This research involved improving analog blocks in the electrical interface and implementing test structures and methods to determine the root cause of the original design performance. Through this research it is shown that the combination of using a surface-machined capacitive senor and the parasitic capacitance associated with a two-chip implementation has a detrimental effect on the integrator of the electrical interface.

Investigation of a Noise-Shaping Accelerometer Interface Circuit for Two-Chip Implementation

by
Jacob W. Zechmann

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Chapter 1.

INTRODUCTION

Worldwide revenues for micro-electromechanical systems (MEMS) will grow from $3.9 billion in 2001 to $9.6 billion in 2006 as predicted by In-Stat/MDR [1]. MEMS such as, accelerometers are capable of sensing changes in movements relative to a particular reference point. The low-G, high-resolution, accelerometer market in particular is experiencing rapid growth. These sensors are needed for gaming devices, touch pads, and crash detection systems. Some other accelerometer applications include: computer hard-drive protection, personal navigation systems, physical therapy and rehabilitation equipment, seismic detectors, and industrial vibration measurement [1]. Original equipment manufacturers are using low-G accelerometers to differentiate their products with safety, security and convenience features. Hence, there is significant motivation for improving sensitivity, cost, reliability, and convenience.

One architecture implementation decision that affects the cost and convenience is whether to integrate the capacitive sensor and electrical interface on the same substrate. Factors that would influence this decision are production volume and application. For example, industrial vibration measurement applications benefit from a two-chip solution where the sensor is placed on the industrial machinery. If the volumes are sufficiently large, fabrication of a single-chip may have a lower cost than fabricating the electrical interface separately with a cost effective VLSI technology. However, there is a tradeoff in design difficulty between the single and two-chip implementations. The large and often mismatched parasitic capacitance found between the sensor and interface of a two-chip implementation reduces sensitivity and dynamic range of an accelerometer.

Delta-sigma modulation is a stable implementation of high-resolution, analog-to-digital converters in a VLSI technology. It is an excellent approach for accelerometers, given their low-G sensing demand. With delta-sigma modulation, over-sampling and feedback techniques can be used to shape the electrical noise out of the signal band thereby increasing the resolution.

This research investigates the design of an over-sampled, third order, delta-sigma modulator that consists of a two-chip implementation. The interface design consists of a correlated double sampling CDS integrator, inter-loop feedback DAC, force-feedback and mismatch shaping logic, switches, and clock generation. The sample capacitors of the integrator, force-feedback capacitors, and associated switches are found on the sensor chip. The system design contains a number of techniques that are useful for lowering the signal band noise, improving linearity, and maximizing dynamic range. The goal is to demonstrate that a two-chip implementation of a third order delta-sigma modulator is stable and has a high dynamic range and SNDR over a 200 Hz signal bandwidth. The initial fabricated design experienced instability and functional problems. This research involved improving analog blocks in the electrical interface and implementing test structures and methods to determine the root cause of the original design performance. Through this research it is shown that the combination of a surface-machined, capacitive senor and the parasitic capacitance associated with a two-chip implementation has a detrimental effect on the integrator performance of the electrical interface.

The electrical interface circuitry is fabricated in a standard, 5-volt, 1.6-um, CMOS technology. Analog Devices Inc. fabricated the capacitive sensor through their surface micromachining technology.

1.1 Organization

Chapter 2 discusses two differences in capacitive sensor fabrication. This chapter describes the fundamental behavior of a capacitive sensor, such as, displacement of a suspended beam mass through acceleration stimulus. The design principles of capacitive sensors will be discussed including the mechanical modeling of the physical device and its electrical behavior. Noise poses a threat to the resolution of any data converter. The noise associated with capacitive sensors will be briefly stated.

Chapter 3 discusses the system level design. The objective of this chapter is to theoretically describe each block of the third order delta-sigma modulator. The integrator and mismatch shaping are discussed. Building on the modeling of capacitive sensors, the integrator function, feedback, and the performance of the system is presented.

Chapter 4 addresses the interface design. Discussions include the integrator amplifier, common mode feedback, switch capacitor architecture, and switch design. The important parameters of gain, unity gain bandwidth, slew rate, and noise are derived. The new design discussed provides a combination of derivations and transistor level simulations. Given the noise sources of each block, complete noise contributions of the integrator are determined. As well as noise, gain error is an important design consideration for the interface implementation.

Chapter 5 is focused on testing the interface design. The test structures implemented on the interface chip are presented. Due to the stability and functional problems of the initial design, a first order test methodology is discussed in this chapter. This methodology is used to simplify the system in order to debug selected blocks.

Experimental results are presented in chapter 6. This chapter begins with the pad problems of the initial fabrication. In Chapter 6, two major testing results are presented. The first is the implementation effects on the input common mode voltage of the amplifier. Finally, the measurement results of the first order test structure are shown.

The conclusion summarizes the investigation of this research, and is found in Chapter 7. Possible future work and focus with this interface design is discussed.

1.2 Simulation Details

The results included in this research were generated from behavioral and transistor level simulations. Matlab's Simulink performed the over all system performance and stability simulations. Spectra density estimation was determined through a fast Fourier transform (FFT) with Hamming window. FFT's are performed on the digital modulator's output, 1 to -1. No decimation filtering was implemented in the system or on silicon, nor in simulations or measurements. Spectre was used to simulate the transistor level block implementation and system performance.

Chapter 2.

CAPACITIVE SENSORS

2.1 Bulk vs. Surface Micro-Machined Sensors

A detailed discussion of micromachining is beyond the scope of this research. However, it is informative to describe the main two types of displacement accelerometers relevant to this research. These types of accelerometers, capacitive sensors, are capacitive position sensing. Capacitive sensors measure the displacement of a proof mass, the beam, in response to an external force or acceleration. Capacitive sensors are used in high resolution applications. Other advantages include their low intrinsic temperature coefficient and ease of integration with CMOS fabrication [2]. The system performance is sensitive to the presence of parasitic capacitance at the amplifier input to the interface circuit. This sensitivity is an important consideration that sets design parameters and limits achievable results.

This sensitivity varies between the bulk and surface micro-machined capacitive sensors. Interconnect capacitance can degrade the sensitivity of capacitive sensors significantly by several orders of magnitude. In cases such as two-chip solutions where a large interconnect parasitic capacitance is present between the sensor and the electrical interface circuit, bulk micro-machined sensors are preferred [2]. Bulk sensors have large sense capacitance with similar magnitude as the parasitic capacitance, making it suitable for two-chip solutions.

Surface micro-machining is a more sophisticated technique than bulk. The surface, micromachining process creates much smaller and more intricate, precisely, patterned structures [3]. Surface-machined devices are around 1 to 2μm similar to the dimensions of electronic CMOS circuitry. Therefore, surface-machined devices are about 20 times smaller than bulk-machined devices, and their sense capacitors are much smaller and more sensitive to parasitic capacitance than bulk-machined. The bulk-machined process can not be integrated with electronic CMOS technology, making it non-ideal in certain applications [3].

2.2 Damped Mass-Spring Behavior

Capacitive sensors behave as damped mass-springs. A beam is suspended above the substrate by compliant springs. The two sense capacitors are formed between the beam and a corresponding stationary plate as shown in Figure 2.1. The figure shows the capacitive sensor with and without applied acceleration [4]. Under applied acceleration, the beam will displace from its nominal position. The displacement of the beam is reflected in a change in the sense capacitors, C_{S1} and C_{S2}. As the figure shows, the change in distance between the plates, displacement, of the sense capacitors will change equally but in the opposite direction for each sense capacitor.

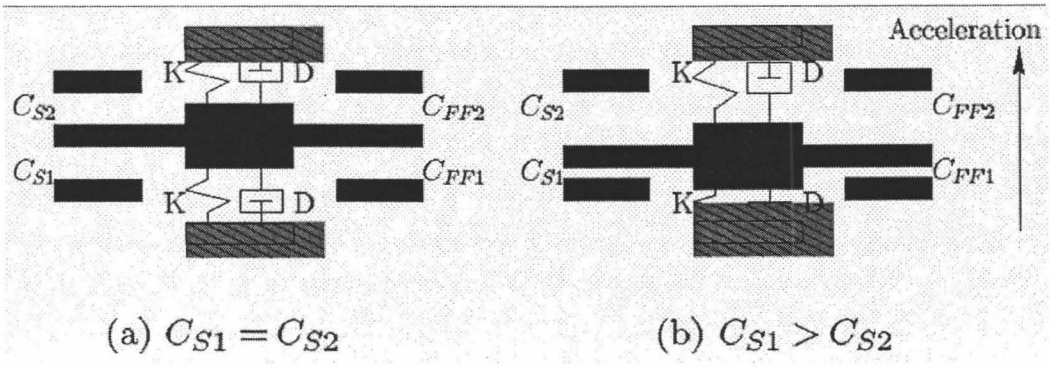

Figure 2.1 Capacitive Sensor shown with mass-spring modeling.

From the figure, K is the spring constant and D is the damping factor for the beam. There are three forces that influence the beam expressed in Equation 2.1 under steady state conditions. The differential equation is presented in Equation 2.2 where M is the mass of the beam, and X is the displacement of the beam.

$$0 = Mass \cdot Acceleration + D \cdot Velocity + K \cdot displacement \tag{2.1}$$

$$0 = M \cdot \frac{d^2X}{dt^2} + D \cdot \frac{dX}{dt} + K \cdot X \tag{2.2}$$

These forces are the acceleration on the beam's mass with the spring constant and damping factor apposing the beam's acceleration. When an external force, F_{EXT}, is applied to the beam, the forces are related in Equation 2.3.

$$F_{EXT} = M \cdot \frac{d^2X}{dt^2} + D \cdot \frac{dX}{dt} + K \cdot X \tag{2.3}$$

For simplicity, assume the external force is sinusoidal and the solution for X is $X=xe^{(jwt)}$. Where x is a complex number indicating the maximum displacement and phase with respect to the external force. Therefore, Equation 2.3 can be transformed from the time domain to the frequency domain [5].

$$F_{EXT} \cdot e^{(jwt)} = M \cdot \frac{d^2 xe^{(jwt)}}{dt^2} + D \cdot \frac{dxe^{(jwt)}}{dt} + K \cdot xe^{(jwt)} \tag{2.4}$$

$$F_{EXT} = -M\omega^2 x + D\omega xj + Kx \tag{2.5}$$

The frequency the mass-spring would oscillate without mechanical damping is called the natural frequency, ω_0.

$$\omega_0 = \sqrt{\frac{K}{M}} \tag{2.6}$$

The quality factor, Q, is the efficiency at natural frequency.

$$Q = \frac{\sqrt{MK}}{D} \tag{2.7}$$

Using Equations 2.5 through 2.7, the following continuous time transfer function from acceleration to displacement is derived.

$$H(s) = \frac{X(s)}{\alpha(s)} = \frac{1}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{2.8}$$

A surface-machined sensor was fabricated for the purpose of initial research which I am investigating. Analog Devices Inc. (ADI) provided the sensor using their surface micromachining process. Figure 2.2 shows the structural diagram of ADI's capacitive senor. The nominal value for the sense capacitors, C_{S1} and C_{S2}, are 100fF. The beam has a mass of 0.1μg. The quality factor, Q, and natural frequency, ω_0, are 4 and 2π(25e3) respectively. The nominal distance between the beam and the stationary plate of each sense capacitor, d_1 and d_2, is 1μm [6].

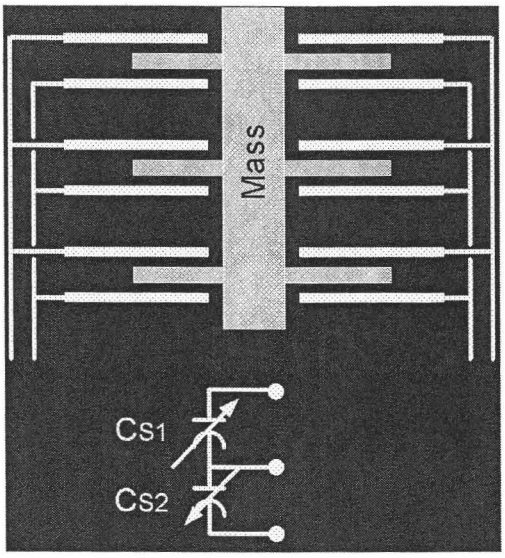

Figure 2.2 Structural diagram of ADI's capacitive sensor.

2.3 Sense Capacitance

As previously discussed, the beam mass behaves mechanically and is modeled as a damped mass-spring. Electrically, the sensor behaves as a variable capacitor subject to external force. The value of each sense capacitor changes according to the displacement of the beam as shown in Equation 2.9.

$$C_{S1} = \frac{\varepsilon A}{d_1 + X} = \frac{C_0 \cdot d_1}{d_1 + X}, C_{S2} = \frac{\varepsilon A}{d_2 - X} = \frac{C_0 \cdot d_2}{d_2 - X} \tag{2.9}$$

This equation illustrates beam displacement will increase one sense capacitance and decrease the other. The permittivity of the sensor capacitor is ε. A is the total surface area of overlap between the stationary sense and beam plates. The nominal distance for d_1 and d_2 is d_0 = 1μm. X is the displacement of the beam under applied external force.

2.4 Brownian Noise

One source of noise at the accelerometer output is due to the suspended beam mass. The beam is subject to viscous damping by air molecules causing noticeable energy dissipation and creating what is called Brownian noise. Mechanical damping is caused from both gas and structural losses. Given that structural losses are a few orders of magnitude lower than gas-damping effects, they may be ignored. A few methods available for lowering Brownian noise

includes reducing the air damping and increasing the sense-element mass. In order to reduce the air damping, vacuum packaging is needed [2].

The sensor provided for this research did not include special micromachining procedures to increase the beam mass or vacuum packaging. These considerations are out of the scope of this research.

Chapter 3.

SYSTEM ARCHITECTURE

A block diagram of the two-chip system architecture investigated is shown in Figure 3.1 [4]. The dashed line through the center of the diagram divides the continuous-time world of the accelerometer and the discrete-time implementation of the interface circuit. Following the flow of the block diagram, the external acceleration is applied to the accelerometer. The force resulting from this acceleration is added to the negative force-feedback. This final force is applied to the accelerometer and results in displacement of the beam changing the sense capacitance. A difference in capacitance between sense capacitors produces an integrated differential voltage. The charge sampled by the sensor capacitors is added to the negative feedback through k_4. A digital compensator or differentiator, H_C, is needed to match the order of the system at the input of the sensor.

The following sub chapters will discuss the modeling of each block in the system and the implementation of blocks in the interface circuit.

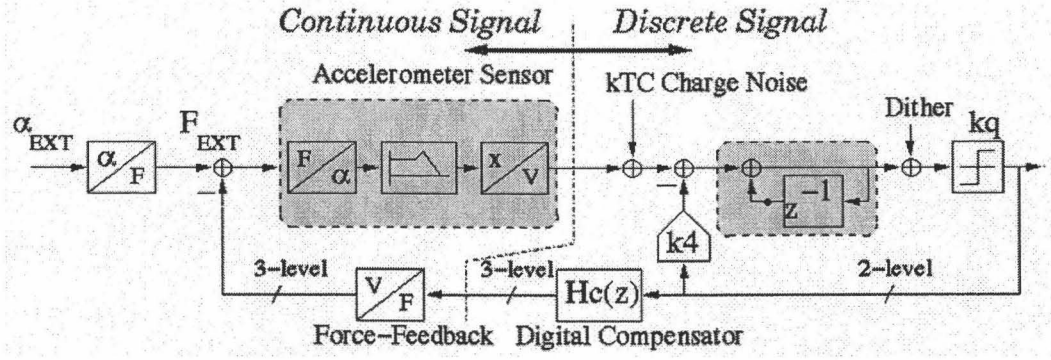

Figure 3.1 Block diagram of the system architecture.

3.1 k_0: Conversion from α_{EXT} to F_{EXT}

The external acceleration, α_{EXT}, is expressed in gravity, G. One G is equal to 9.83 m/s^2. The accelerometer's beam has a mass of 0.1μg. Given that force equals mass multiplied by acceleration, k_0 is derived as shown in Equation 3.1. Constant k_0 is used to convert the external acceleration to force by multiplying this constant by the number of Gs applied to sensor.

$$k_0 = \frac{F_{EXT}}{\alpha_{EXT}} = M \cdot 9.83\left(m/s^2\right) = 0.1e-9(kg) \cdot 9.83\left(m/s^2\right) = 9.83e-10\left(kg \cdot m/s^2\right) \quad (3.1)$$

3.2 k_2: Conversion from Force to Acceleration

In order to convert the external force summed with the force-feedback to acceleration, k_2 is modeled. Using the relationship that force equals mass multiplied by acceleration, the acceleration can be determined by dividing the force by the mass of the beam. This is shown in Equation 3.2.

$$k_2 = \frac{\alpha}{F} = \frac{1}{M} = \frac{1}{0.1e-9(kg)} = 1e10\left(1/kg\right) \quad (3.2)$$

3.3 Accelerometer Transfer Function

The discrete-time function is derived from the continuous-time damped mass-spring function previously reviewed. This transfer function determines the beam displacement from the applied acceleration. The continuous-time transfer function is shown in Equation 3.3.

$$H(s) = \frac{X(s)}{\alpha(s)} = \frac{1}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \quad (3.3)$$

This architecture was modeled and simulated in discrete-time. The continuous-time transfer function presented above was converted to discrete-time using MATLAB's c2d function [4]. Equation 3.4 shows the second order discrete-time representation of the sensor transfer function.

$$H(z) = \frac{B(z)}{A(z)} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}} \quad (3.4)$$

Substituting the quality factor and natural frequency provided by ADI into Equation 3.3 and applying the c2d function the following discrete time function is used to mode the sensor in the system.

$$H(z)=\frac{B(z)}{A(z)}=\frac{1.495e-11z+1.381e-11}{z^2-1.084z+0.7937} \tag{3.5}$$

From Equation 3.3, the DC gain of the accelerometer is computed in Equation 3.6.

$$A_{DC}=\frac{X}{\alpha_{gravity}}=\frac{1}{\omega_0^2}=\frac{1}{(2\pi\cdot 25e3)^2}=4.0528e-11 \tag{3.6}$$

This gain is needed to determine the amount of displacement for a given acceleration and the corresponding sensor capacitor values. Given the modeling constants derived, the beam displacement can be determined for any acceleration input in terms of G's. For a one G input, the beam displacement is 0.3984nm as shown in Equation 3.7.

$$X=1\cdot k_0\cdot k_1\cdot A_{DC}=1\cdot 9.83e-10\cdot 1e10\cdot\frac{1}{(2\pi\cdot 25e3)^2}=3.984e-10(m) \tag{3.7}$$

From Equation 2.9, the corresponding sensor capacitor value due to a 0.3984nm displacement is determined in Equations 3.8 and 3.9.

$$C_{S1}=\frac{C_0\cdot d_1}{d_1+X}=\frac{100e-15\cdot 1e-6}{1e-6+3.984e-10}=99.96018\,fF \tag{3.8}$$

$$C_{S2}=\frac{C_0\cdot d_2}{d_2-X}=\frac{100e-15\cdot 1e-6}{1e-6-3.984e-10}=100.03982\,fF \tag{3.9}$$

Therefore, one G of acceleration results in about 40aF of increase and decrease sense capacitance. This is an extremely small capacitance to detect. The next sub chapter will determine the resulting integrated voltage from 40aF of sense capacitance. Figure 3.2 is a plot of the sensor capacitance verses the input acceleration in G's. From the chart, 50G of acceleration is equivalent to a 2fF change in sense capacitance. For this type of capacitive sensor, 50G is the maximum input specification from the ADI ADXL50 catalog accelerometer.

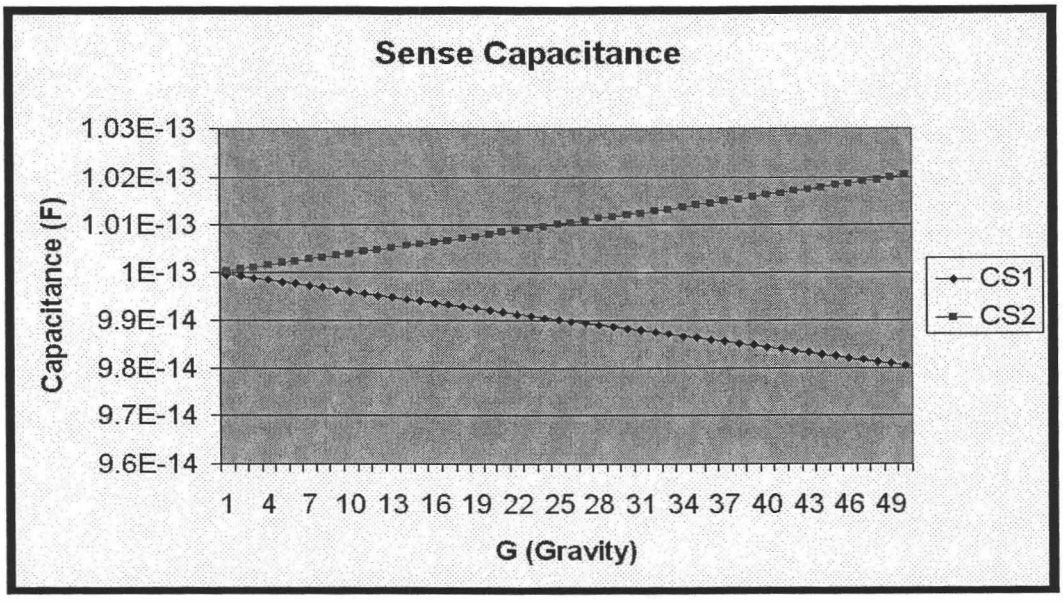

Figure 3.2 Sensor capacitance changes as a function of acceleration.

3.4 Integrated Voltage from Displacement

The sensor beam displacement needs to be converted to voltage. The gain of the interface integrator is derived in the following discussion. The previous Equations 3.8 and 3.9 show the sensor capacitor value in terms of displacement. These equations will be substituted into the integrator gain equation. The final result will be integrated voltage as a function of beam displacement.

To simplify the integrator gain analysis, the switch capacitor, feedback network implementing correlated double sampling will be replaced with a single non-switched feedback capacitor, C_{fb}. Another simplification is to ignore the transition from phase $\Phi 4$ to $\Phi 1$ and $\Phi 2$ to $\Phi 3$. These phases are used to cross couple the sense and parasitic capacitor mismatch in order to remove DC offset due to mismatch in sense and interconnect parasitic capacitance. Figure 3.3 is the switch capacitor, integrator circuit used in this analysis.

Transitioning from $\Phi 1$ to $\Phi 2$, Equations 3.10 and 3.11 show the delta gain of the plus and minus output terminals of the integrator. During $\Phi 1$, node 2 is switched to ground. Therefore, the integrated output voltage is the ratio of C_{S2}/C_{fb} multiplied by VREF [7], 0V. For $\Phi 2$, VREF is switched to node 2 and the integrated output voltage is C_{S2}/C_{fb} multiplied by VREF. The integrated voltage from $\Phi 1$ to $\Phi 2$ is derived in Equations 3.10 and 3.11, and the differential, integrated voltage is derived in Equation 3.12.

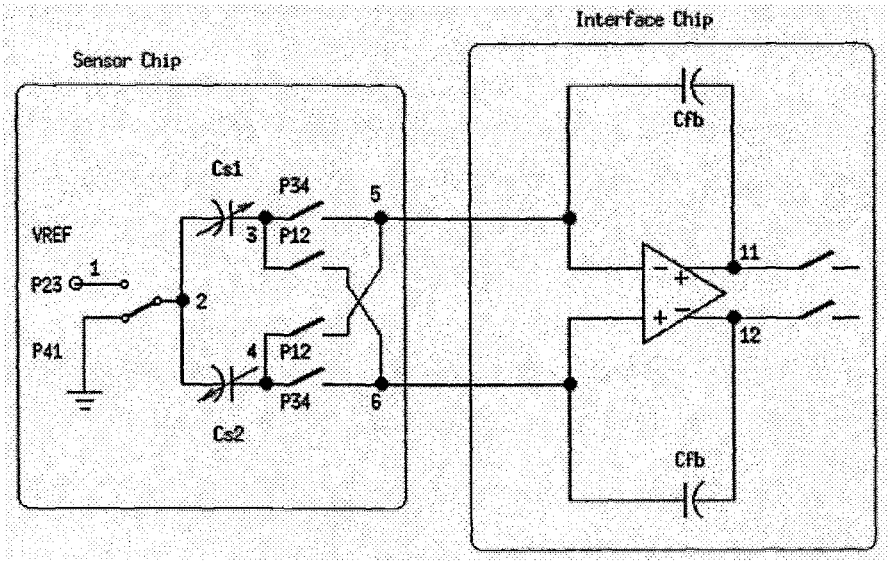

Figure 3.3 Simplified version of the interface integrator without CDS.

$$\Delta Voutp_{12} = -\frac{C_{S2}}{C_{fb}} \cdot V_{REF} - \left(-\frac{C_{S2}}{C_{fb}} \cdot 0 \right) = -\frac{C_{S2}}{C_{fb}} \cdot V_{REF} \tag{3.10}$$

$$\Delta Voutm_{12} = -\frac{C_{S1}}{C_{fb}} \cdot V_{REF} - \left(-\frac{C_{S1}}{C_{fb}} \cdot 0 \right) = -\frac{C_{S1}}{C_{fb}} \cdot V_{REF} \tag{3.11}$$

$$\Delta Voutdiff_{12} = V_{REF} \cdot \left(-\frac{C_{S2}}{C_{fb}} - \left(-\frac{C_{S1}}{C_{fb}} \right) \right) = \frac{V_{REF}}{C_{fb}} \cdot \left(C_{S1} - C_{S2} \right) \tag{3.12}$$

Transitioning from Φ3 to Φ4, Equations 3.13 and 3.14 show the delta gain of the plus and minus output terminals of the integrator. The same approach is taken in determining the differential integrated voltage from Φ3 to Φ4 resulting in Equation 3.15.

$$\Delta Voutp_{34} = -\frac{C_{S1}}{C_{fb}} \cdot 0 - \left(-\frac{C_{S1}}{C_{fb}} \cdot V_{REF} \right) = \frac{C_{S1}}{C_{fb}} \cdot V_{REF} \tag{3.13}$$

$$\Delta Voutm_{34} = -\frac{C_{S2}}{C_{fb}} \cdot 0 - \left(-\frac{C_{S2}}{C_{fb}} \cdot V_{REF} \right) = \frac{C_{S2}}{C_{fb}} \cdot V_{REF} \tag{3.14}$$

$$\Delta Voutdiff_{34} = V_{REF} \cdot \left(\frac{C_{S1}}{C_{fb}} - \frac{C_{S2}}{C_{fb}} \right) = \frac{V_{REF}}{C_{fb}} \cdot \left(C_{S1} - C_{S2} \right) \tag{3.15}$$

The total integrated voltage after the four phases of each integration cycle is determined by summing the differential integrated voltages form Φ34 and Φ12 as shown in Equation 3.16.

$$Voutdiff = \Delta Voutdiff_{34} + \Delta Voutdiff_{12} = \frac{2 \cdot V_{REF}}{C_{fb}} \cdot (C_{S1} - C_{S2}) \tag{3.16}$$

With a small change in sensor capacitance, the integrated voltage will be small as well. To increase the output voltage, the input sampling sensor capacitors are cross coupled between Φ12 and Φ34. Equation 3.16 shows a gain factor of two as a result of double sampling the cross coupled connection. The integrated voltage in terms of displacement is derived by substituting the sense capacitance from Equation 2.9 into Equation 3.16. The resulting expression is provided in Equation 3.17.

$$Voutdiff = \frac{2 \cdot V_{REF}}{C_{fb}} \cdot (C_{S1} - C_{S2}) = \frac{2 \cdot V_{REF}}{C_{fb}} \cdot \left(\frac{\varepsilon A}{d_1 + X} - \frac{\varepsilon A}{d_2 - X} \right) \tag{3.17}$$

Making the following assumptions that the beam displacement is much smaller than the nominal distance between sense capacitor plates and that the actual C_{S1} and C_{S2} distances are equal, the following equation is valid.

$$Voutdiff = \frac{2 \cdot \varepsilon A \cdot V_{REF}}{C_{fb}} \cdot \left(\frac{1}{d_0 \cdot \left(1 + \frac{X}{d_0}\right)} - \frac{1}{d_0 \cdot \left(1 - \frac{X}{d_0}\right)} \right) \tag{3.18}$$

Re-arranging Equation 3.18 provides a relationship between the beam displacement and integrated voltage.

$$Voutdiff \cong \frac{2 \cdot V_{REF}}{C_{fb}} \cdot \frac{\varepsilon A}{d_0} \cdot \left(\left(1 - \frac{X}{d_0}\right) - \left(1 + \frac{X}{d_0}\right) \right) = -\frac{2 \cdot V_{REF} \cdot C_0}{C_{fb}} \cdot \frac{2 \cdot X}{d_0} \tag{3.19}$$

$$Voutdiff \cong -\frac{4 \cdot V_{REF} \cdot C_0 \cdot X}{C_{fb} \cdot d_0} \tag{3.20}$$

Using the ADI's surface-machined capacitive sensor parameters, a VREF equal to 5V, and an integrator feedback capacitor equal to 200fF, the numerical constant is determined in Equation 3.21.

$$k_2 = \frac{Vout}{X} = \frac{4 \cdot V_{REF} \cdot C_0}{C_{fb} \cdot d_0} = \frac{4 \cdot 5V \cdot 100fF}{200fF \cdot 1\mu m} = 1e7\left(V/m\right) \tag{3.21}$$

A more sophisticated model for system simulations is to use the expression in Equation 3.18.

3.5 Integrator Transfer Function

The next block modeled in the system is the integrator's discrete-time transfer function. The gain which determines the sampled integrated voltage is added to the negative feedback of the inner loop, k_4. This voltage will be integrated as determined from the following analysis.

A straight forward derivation of the transfer function is possible if we simplify the integrator as shown in Figure 3.4. As in the gain derivation, the CDS has been removed. Another simplification in Figure 3.4 is the single-ended representation of the differential integrator. Observing the charge equations from phase Φ1 to Φ2 is all that is necessary to determine the z-transfer function of the integrator. Despite the implemented integrator taking four phases to obtain the final integrated voltage per cycle, it is still only considered one clock cycle in system simulations through modeling.

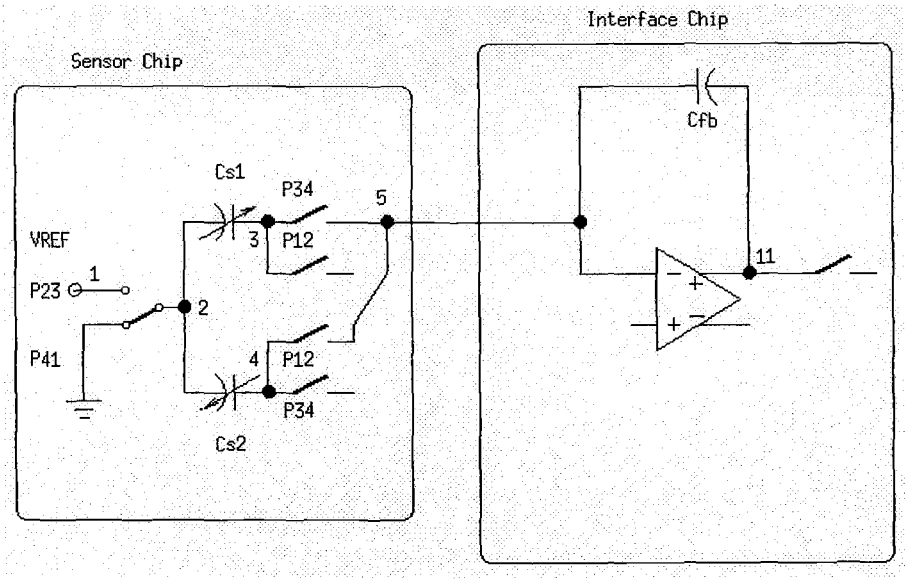

Figure 3.4 Single-ended version of the integrator without CDS.

The charge equations for C_{S2} and C_{fb} in phase Φ1 are provided in Equations 3.22 and 3.23. Charge equations are simply the voltage across the capacitor multiplied by the capacitance of the capacitor.

$$QC_{S2} = (V_5 - 0)C_{S2} \tag{3.22}$$

The voltage across C_{fb} in phase $\Phi 1$ is V_5 and V_{OUTP}. Node voltage V_5 is associated with the node numbered 5 in Figure 3.4. Node voltage V_{OUTP} is the positive output shown on the differential amplifier in Figure 3.4 also labeled node 11. Node 5 is assumed to not vary over time, a constant, since it is held by the gain of the amplifier. However, V_{OUTP} is time-varying or signal dependent, and the time V_{OUTP} is considered must be noted [7] as shown in Equation 3.23.

$$QC_{fb} = (V_5 - V_{OUTP}(nT - \frac{T}{2}))C_{fb} \tag{3.23}$$

The charge equations for C_{S2} and C_{fb} in phase $\Phi 2$ are provided in Equations 3.24 and 3.25.

$$QC_{S2} = (V_5 - V_{REF})C_{S2} \tag{3.24}$$

$$QC_{fb} = (V_5 - V_{OUTP}(nT))C_{fb} \tag{3.25}$$

The next step in the switch capacitor analysis is to determine the change in charge across each capacitor transitioning from phase $\Phi 1$ to $\Phi 2$.

$$\Delta QC_{S2} = -V_{REF}C_{S2} \tag{3.26}$$

$$\Delta QC_{fb} = (-V_{OUTP}(nT) + V_{OUTP}(nT - \frac{T}{2}))C_{fb} \tag{3.27}$$

Due to charge conservation, summing the delta charge across C_{S2} and C_{fb} will result in zero excess charge. However, this equation should reflect whether the integrator is inverting or non-inverting.

$$\Delta QC_{S2} + \Delta QC_{fb} = 0 \tag{3.28}$$

Equation 3.29 shows the delta charges equations for C_{S2} and C_{fb} substituted into Equation 3.28.

$$-V_{REF}C_{S2} + (-V_{OUTP}(nT) + V_{OUTP}(nT - \frac{T}{2}))C_{fb} = 0 \tag{3.29}$$

Note that the integrator output is only valid after phase $\Phi 2$ in this analysis representing the completion of the implemented integration cycle. Therefore, the voltage at V_{OUTP} at the end of $\Phi 1$ is the same as the last valid integrated voltage in the previous $\Phi 2$ phase. Under this condition Equation 3.30 is correct and Equation 3.29 can be rewritten into Equation 3.31.

$$V_{OUTP}(n\frac{T}{2} - \frac{T}{2}) = V_{OUTP}(nT - T) \tag{3.30}$$

$$\frac{-V_{REF}C_{S2}}{C_{fb}} = V_{OUTP}(nT) - V_{OUTP}(nT - T) \tag{3.31}$$

Taking the z-transform of Equation 3.31, the charge equation is transformed into the discrete z-domain in Equation 3.32.

$$\frac{-V_{REF}C_{S2}}{C_{fb}} = V_{OUTP}(z)(1-z^{-1}) \tag{3.32}$$

Re-arranging the previous equation, leads to Equation 3.33. This transfer function indicates that the integrator is inverting and non-delaying. Since the sampling capacitor is always connected to the input of the amplifier, both the sampling and integration occur in the same phase. In this situation, the integrator is non-delaying as reflected in Equation 3.35.

$$V_{OUTP}(z) = \frac{-V_{REF}C_{S2}}{C_{fb}} \cdot \frac{1}{(1-z^{-1})} \tag{3.33}$$

The input voltage of the integrator is the step voltage sampled, V_{REF}.

$$\frac{\Delta Voutdiff}{\Delta Vindiff} = \frac{\Delta Voutdiff}{V_{REF}-0} = \frac{\Delta Voutdiff}{V_{REF}} \tag{3.34}$$

In order to complete the integrator's transfer function, multiply the integrator gain derived in the last chapter by the z-domain transfer function presented in Equation 3.35.

$$\frac{\Delta Voutdiff}{V_{REF}} = \frac{2}{C_{fb}} \cdot (C_{S1}-C_{S2}) \cdot \frac{1}{(1-z^{-1})} \tag{3.35}$$

The system block diagram illustrated in Figure 3.1 contains the block diagram representation for the integrator show in Figure 3.5. The transfer function is verified through the following three equations. The transfer function presented in Equation 3.38 matches the z-domain transfer function presented in Equation 3.35.

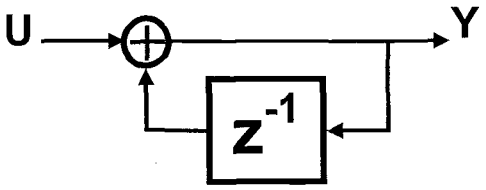

Figure 3.5 Block diagram of the integrator's z-transfer function.

$$Y = U + Yz^{-1} \tag{3.36}$$

$$Y(1-z^{-1}) = U \tag{3.37}$$

$$\frac{Y}{U} = 1/(1-z^{-1}) \tag{3.38}$$

3.6 Dither

It is well known that first order modulators produce tones. Dither is used to reduce the amount of idle tones [8]. There are two concerns when using dither. Dither must have a white-noise type spectrum and must not saturate the quantizer. Dither is added prior to the quantizer. Therefore, the dither noise can be noise shaped along with the quantization noise [7]. Injecting dither into the integrator output is done with the structure shown in Figure 3.6 [4]. One important point to make about this structure is the division of the difference between V_{INTP} or V_{INTM} and signal ground by two due to charge sharing when C1, C2, C3, and C4 are equal. However, the gain of the single bit quantizer will adjust as needed for the required loop gain. The disadvantage is the reduction in differential integrator output voltage to be quantized. Switch control signals Φ1P and Φ1N are driven from a Random Number Generator (RNG) shown in Figure 3.7. This pseudo RNG gives the dither a white-noise property.

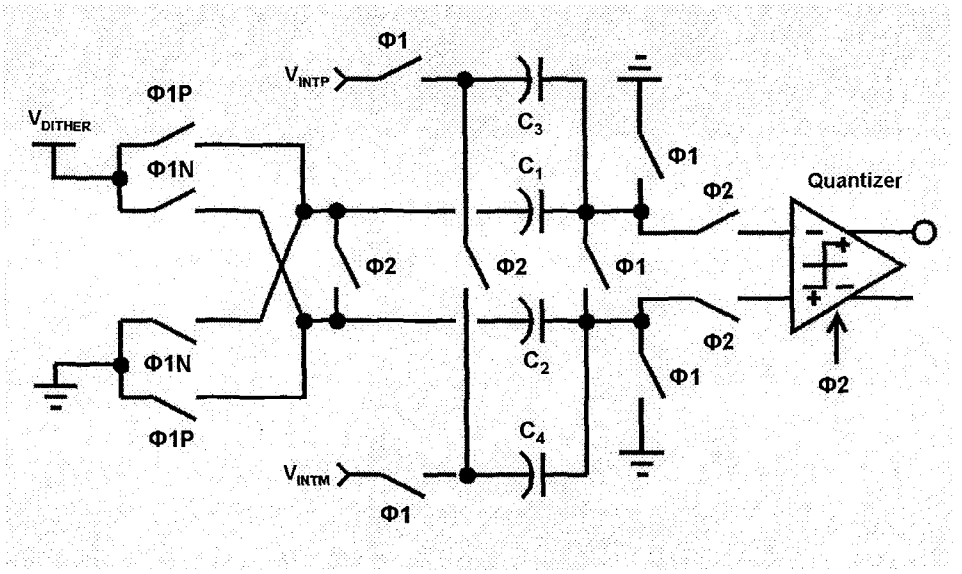

Figure 3.6 Implemented SC Dither Structure.

With an on-chip RNG, dither can be provided reducing test board area and complexity. This is a major concern when using a shaker table for testing and in application. The dither circuit needs two phases in order to perform the dithering.

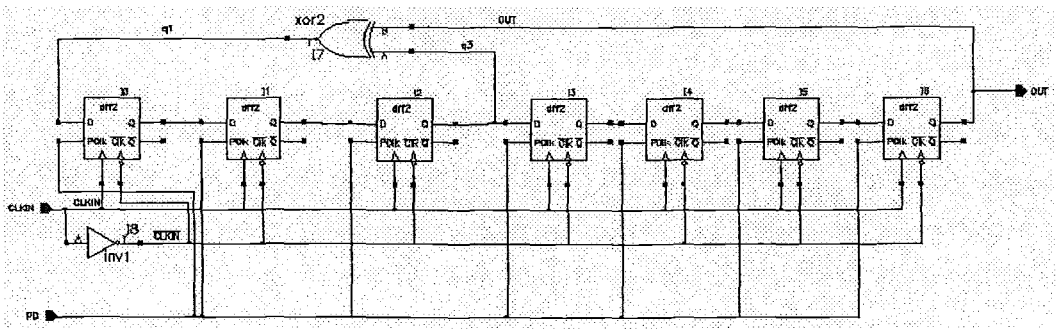

Figure 3.7 Single-bit pseudo RNG used for dither.

The single-bit, pseudo random number generator was implemented using a Linear Feedback Shift Register (LFSR). The generated pattern will repeat every predetermined clock cycles according to the number of flip flops, m, in the architecture [9]. This is known as the period of the generator. Equation 3.39 relates the number of flip flops in the RNG to its period.

$$period = 2^m - 1 \tag{3.39}$$

For both test chips, seven D-type Flip Flops (DFFs) were used to implement the RNG. From this implementation, the pattern will repeat every 127 cycles. A 3MHz master clock corresponds to a 600 kHz system frequency when you consider there are 5 phases or master clock cycles per integration cycle. The RNG period is 127 cycles multiplied by the period of one integration cycle, 1.667us. This equates to a 211.667μs period corresponding to a frequency of 4.724 kHz. This repetition at 4.724 kHz will be seen in the spectrum of the system when the dither is activated. The signal power will depend on the dither voltage applied. Therefore, to avoid SNDR degradation, this frequency should not fall in the signal band of interest. For this architecture, the signal band is DC to 200Hz. The simulation result showing that the RNG pattern repeats every 127 cycles is provided in Figure 3.8. From a clock period of 200ns, the simulation verifies the expected RNG period of 25.4μs.

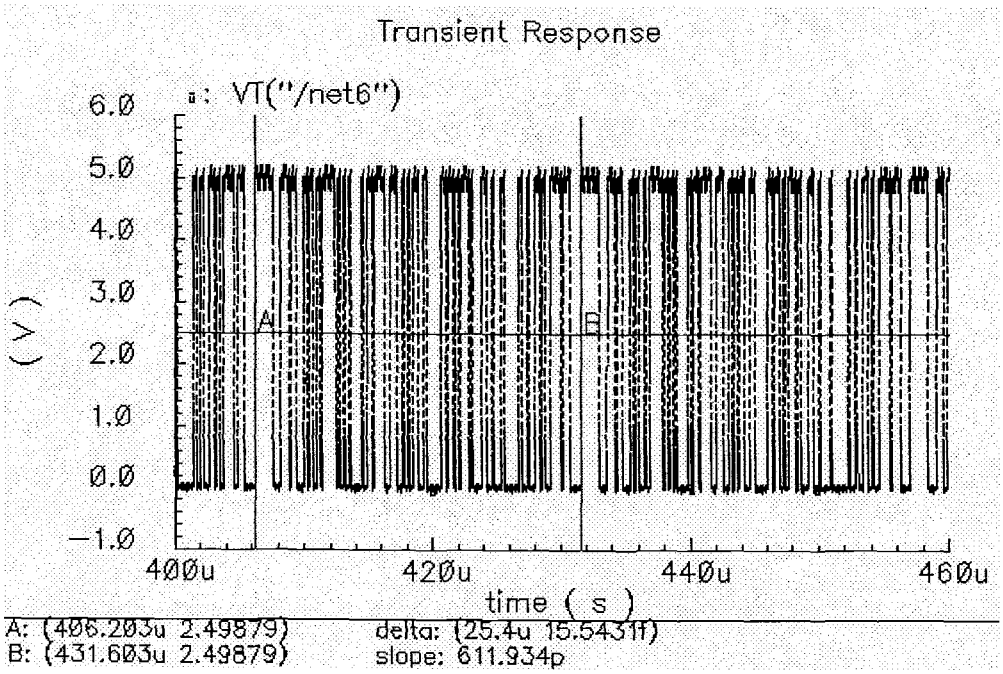

Figure 3.8 Implemented RNG simulation results.

3.7 kq: 1-Bit Quantizer

The quantizer of a delta sigma system is the Analog to Digital Converter (ADC). The differential outputs of the integrator are compared resulting in digital output bit stream that modulates. The gain of a 1-bit quantizer is linear and self adjusting within the loop of the delta sigma system. This is an advantage of two-level ADC's. For multi-level quantizers the gain must be determined according to system stability requirements and implemented with adequate linearity.

A different comparator shown in Figure 3.9 was implemented in the second revision that has a symmetric error bounded by +(1/2) and -(1/2). The advantage of symmetric quantization error is maximum dynamic range. Another advantage of this comparator is that it consumes less die area.

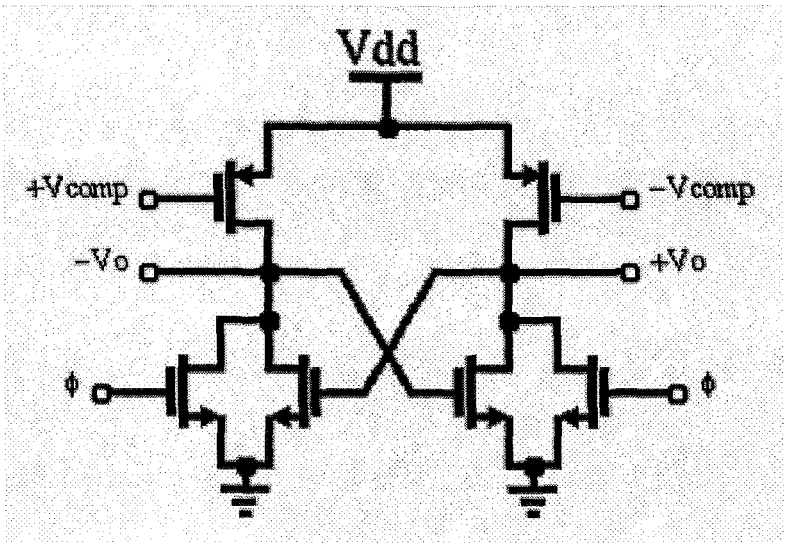

Figure 3.9 Comparator schematic implementing the single-bit quantizer.

Prior to making a comparison, +Vcomp and -Vcomp shown in the figure are charged to the integrator output Common Mode (CM) voltage. The Φ signal is high and creating a current path form Vdd to ground thereby grounding outputs, +Vo and –Vo, and resetting the comparator. If power consumption is a concern, this comparator design is not optimum. When grounding the outputs of the comparator, a constant current consumption is present. When making a comparison, +Vcomp and -Vcomp are valid integrator outputs. The comparator reset signal, Φ, is released allowing the cross coupled, positive feedback to drive +Vo and –Vo to opposite rails depending on the value of +Vcomp and –Vcomp. If +Vcomp is greater than –Vcomp, +Vo is pulled to Vdd and –Vo is pulled low.

3.8 k4: Feedback DAC

The constant, k4 feedback is determined by multiplying the differential reference voltage by the DAC integrator gain. Equation 3.40 represents the differential value for k4. The polarity of the feedback depends on the quantizer output.

$$|k4| = (V_{REF} - -V_{REF}) \cdot \frac{C_{REF}}{C_{fb}} = 2 \cdot V_{REF} \cdot \frac{100fF}{200fF} = V_{REF} \tag{3.40}$$

The magnitude of the k4 determines the full scale voltage of the interface integrator, and is adjusted by varying V_{REF}. Depending on the input signal level, k4 is adjusted accordingly not to saturate the integrator or cause distortion.

The initial design of the inner-loop feedback DAC changes between a non-inverting and an inverting switch capacitor (SC) structure. The reference voltage, V_{REF}, is integrated either positively or negatively depending on the control of the switches. This DAC architecture is not ideal. Given that each terminal of the differential feedback has a different SC network while integrating, creates a potential for offset due to mismatch and a reduction in dynamic range due to gain error.

The DAC could have been implemented by using the same SC network, but reversing the polarity of the reference voltage. For example the positive reference voltage would be V_{REF} to ground, and the negative reference would be ground to V_{REF}. This architecture has the advantage of limiting the need for extra reference voltages and logic for controlling the switches.

A third solution shown in Figure 3.10 was implemented in the second design revision. This structure uses the same two inverting feedback structures for each differential input. Nodes CS1 and CS2 are the differential inputs to the amplifier of the integrator. During $\Phi 1$, the reference capacitors are reset, and during $\Phi 2$ the reference voltage is sampled and integrated creating an inverting SC structure. For this implementation a second reference, $-V_{REF}$, is needed which could be set to ground. Considering the common mode and stability problems of the initial design, it was preferred to balance the DAC as much as possible. Using the same inverting switch capacitor structure, the $+V_{REF}$ and $-V_{REF}$ reference voltages are switched before the DAC. The reference voltage switch polarity is determined by the quantizer output.

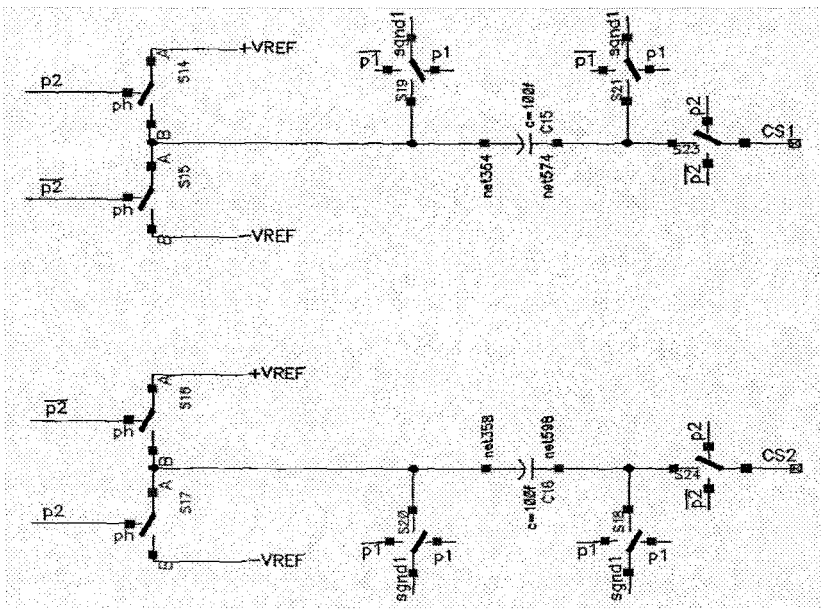

Figure 3.10 DAC schematic implementing the k4 feedback.

3.9 $H_C(z)$ Digital Compensator

The accelerometer is a second order system as described in the mass-spring discussion. The sense capacitors are the sampling capacitors of the integrator. This provides the interface between the accelerometer and integrator. An integrator is a first order system. Therefore, the output of the quantizer is a third order response. A compensator or differentiator is needed to reduce the order of the quantized output, so that a required second order signal is feedback to the accelerometer.

The two different approaches to implementing the compensator block are analog or digital. The investigated architecture used a digital compensator [4]. The advantage of a digital compensator is its simplicity. The transfer function of the digital differentiator is provided in Equation 3.41.

$$H_C(z) = 1 - z^{-1} \tag{3.41}$$

The output of the quantizer or input to the compensator is +1 and -1. After passing through the digital compensator's transfer function, the output is +2, 0, and -2. The fact that the output is multi-level having three possible values is one disadvantage of a digital compensator. Adequate linearity of the multi-level force-feedback is necessary in order to minimize system distortion. The inner loop DAC feedback, k_4, is inherently linear since only a straight line exists between two

possible outputs from the quantizer. The linearity of the three-level force-feedback is improved with a new proposed mismatch shaping scheme [10]. The force-feedback mismatch shaping scheme is presented in Table 3.1. Using the compensator output, the polarity of the force-feedback and the applied phase can be determined.

Table 3.1 Implemented digital compensator output and force-feedback polarity.

Digital Compensator Output	Mismatch Shaping Control	Force-Feedback Φ5	Force-Feedback Φ6
2	y_H	F_{FB+}	F_{FB+}
0	Y_M (Alternate)	F_{FB+}	F_{FB-}
		F_{FB-}	F_{FB+}
-2	Y_L	F_{FB-}	F_{FB-}

3.10 Three-Level Force-Feedback

The external force applied to the capacitive sensor is subtracted by the force-feedback of the system's outer loop. The schematic shown in Figure 3.11 is the implementation of the force-feedback.

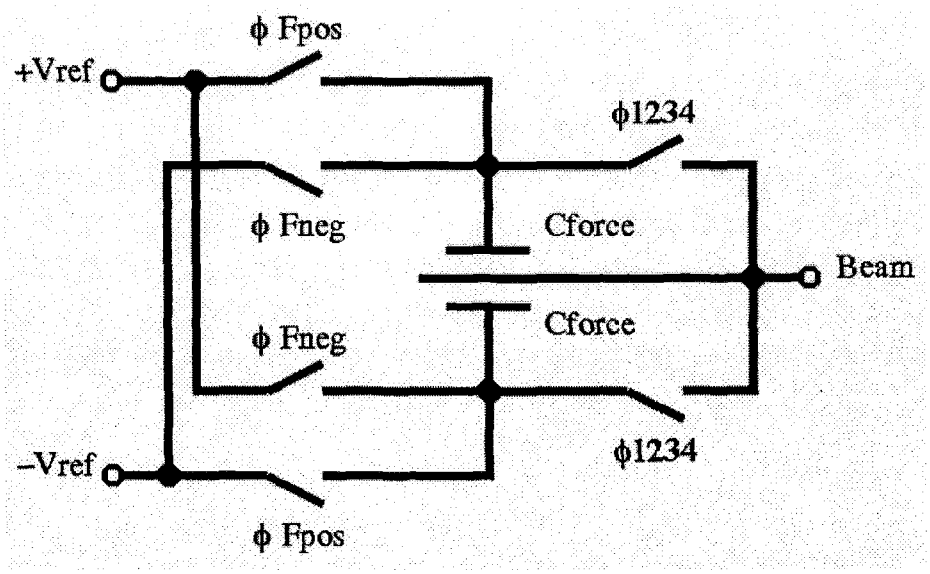

Figure 3.11 Force-Feedback schematic showing the capacitors, switches, and references.

The sense capacitors, C_{S1} and C_{S2}, change in value as the beam is displaced due to an external force. However, during force-feedback a charge is placed across the C_{FORCE} capacitors in order to electrically force a beam displacement. The C_{FORCE} capacitors are additional capacitors identical to the sense capacitors, C_{S1} and C_{S2}, but with a nominal capacitance of 10fF as compared to 100fF of sense capacitance. In the initial design while the integrator is sampling the acceleration of the sensor, the force-feedback terminals of the sensor are floating. Therefore, an uncontrolled potential of the two force-feedback capacitors could inadvertently create an unwanted electrostatic force. During phase Φ1 through Φ4, the interface circuit is completing one cycle of integration. During this period, the C_{FORCE} capacitors should not have an affect on the displacement of the beam while the effects of the external force are being sampled. Therefore, the beam and stationary plate of the C_{FORCE} capacitors are connected together resulting in zero charge across the capacitors. The accompanying positive and negative reference voltages and switches are used to place different charges on the C_{FORCE} capacitors in order to create an electro-static force that displaces the beam. The switches are driven in Φ5. After the four phases needed for integration, the fifth and final phase of the system is use to apply the force feedback. The polarity of the force-feedback switches are determined by the digital compensator and mismatch shaping scheme.

The following discussion will derive the electro-static force equations necessary for modeling the system force-feedback. The energy stored on a capacitor is expressed in Equation 3.42.

$$Energy = \frac{1}{2}Q \cdot V_{TOP} - \frac{1}{2}Q \cdot V_{BOTTOM} = \frac{1}{2}Q \cdot V_{ACROSS} = \frac{1}{2}C_0 \cdot V \cdot V \qquad (3.42)$$

By taking the derivative of the previous equation with respect to the distance between the two plates of the C_{FORCE} capacitor, d, the electro-static force is determined as shown in Equation 3.43.

$$Force = \frac{\partial Energy}{\partial d} = \frac{V^2}{2} \cdot \frac{\partial C}{\partial d} = \frac{V^2}{2} \cdot \frac{\partial\left(\frac{\varepsilon A}{d}\right)}{\partial d} = -\frac{\varepsilon A \cdot V^2}{2d^2} \qquad (3.43)$$

In terms of C_{FORCE}, the electrostatic force becomes:

$$Force = -\frac{\varepsilon A \cdot V^2}{2d^2} = -\frac{C_{FORCE}}{2d}V^2 \qquad (3.44)$$

It is standard practice to use linearity enhancements for multi-level feedback DACs or in this case digital to force converters (DFC). Several algorithms schemes exist to implement dynamic element matching [11]. The only elements available are the two force-feedback

capacitors. The electrostatic force equations for the implemented mismatch shaping scheme are presented below. The 0 output of the digital differentiator corresponds to the y_M of the mismatch shaping scheme. In order to maintain adequate linearity due to mismatch in the distances between the C_{FORCE} and sense capacitor, stationary plates and the beam, force-feedback is time averaged [10]. To implement the time averaging the force-feedback is alternated between F_{FB+} in Φ5 with F_{FB-} in Φ6 and F_{FB-} in Φ5 with F_{FB+} in Φ6 as shown in Table 3.1. The mismatch or difference between d_1 and d_2 is averaged to zero over time for the middle level of the DFC by alternating the sequence of applied positive and negative electro-static forces.

$$y_H = 1, F_{FB+} = -\frac{\varepsilon A}{2} \cdot \left[\left(\frac{V_1 - V_{BEAM}}{d_1 + x} \right)^2 - \left(\frac{V_{BEAM} - V_2}{d_2 - x} \right)^2 \right] \tag{3.45}$$

$$y_L = 1, F_{FB-} = -\frac{\varepsilon A}{2} \cdot \left[\left(\frac{V_{BEAM} - V_2}{d_1 + x} \right)^2 - \left(\frac{V_1 - V_{BEAM}}{d_2 - x} \right)^2 \right] \tag{3.46}$$

Figure 3.12 illustrates the positive and negative force-feedback Equations 3.45 and 3.46.

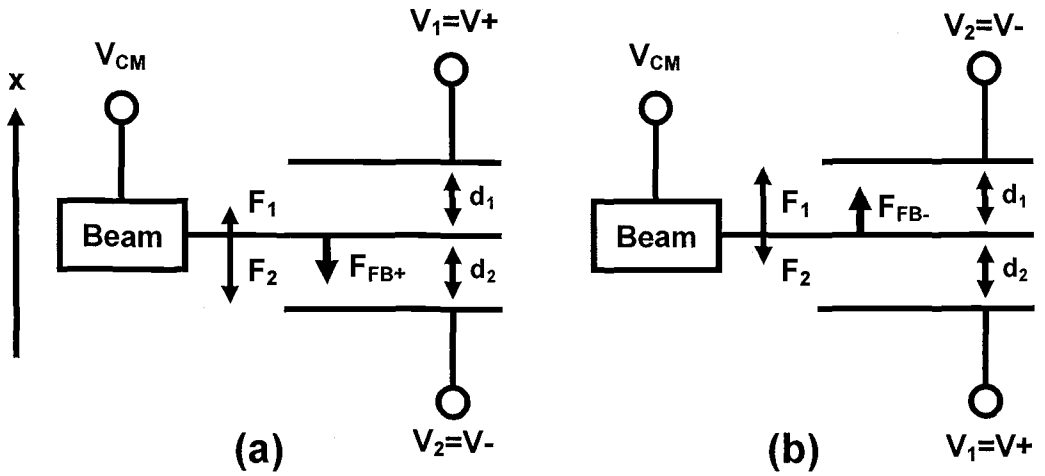

Figure 3.12 Implemented (a) positive and (b) negative force-feedback.

3.11 Five Phase Integration Cycle

The cycle time of the DS modulator was reduced from six master clock cycles to five. Currently, the fifth and sixth phase used to perform the multi-level force-feedback will now be completed in only the fifth phase of the master clock. The two functions needed to be completed are now finished in two phases of the master clock and not two master clock cycles. The amount

of time used to apply the force-feedback is independent of the first four phases used by the CDS circuit. Reducing the time force-feedback is applied, will increase the DS sampling rate and improve the SNR. An implication due to the fifth phase of this system architecture clocking, is that the sampling of the integrator is non-uniform. The sense capacitors are sampled and integrated in phases two and four. Phase Φ4, Φ5 and Φ1 need to be finished before the next sample and integration. Through system simulations this non-uniformity does not have a significant affect on performance.

3.12 System Simulations

System stability and performance was analyzed and determined through MATLAB Simulink simulation. Each block in the architecture was modeled according to the previous discussions. Figure 3.13 shows the block diagram of the simulation schematic used in Simulink. The advantages of modeling simulations are speed and ease of use. Sensitivity analysis was performed by degrading the linearity of the force-feedback, finite amplifier gain, and mismatch in sense capacitance and distance between beam and stationary plates. Other analog non-idealities, such as amplifier thermal noise and KT/C noise were included in some Simulink simulations.

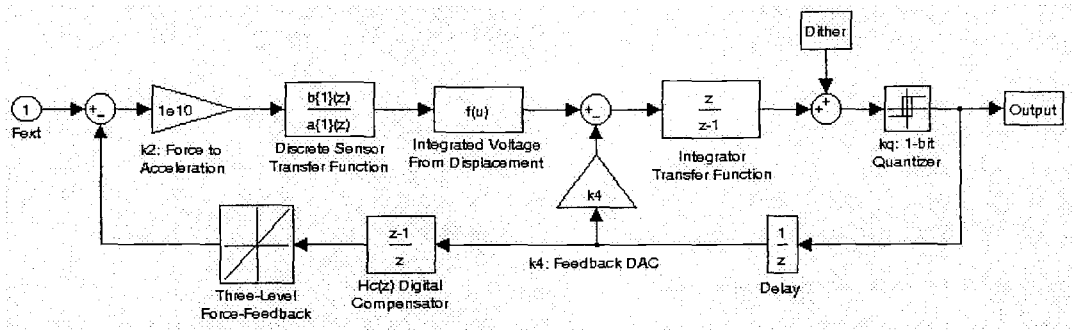

Figure 3.13 System simulation Simulink schematic.

An FFT of the system performance under ideal conditions is presented in Figure 3.14. The force-feedback is linear, sense capacitance and distances d_1 and d_2 are nominal, and the feedback DAC, k_4, was 0.25V differential. The noise is shaped 20dB per decade or first order shaping due to the interface integrator. This noise shaping would not be present if an amplifier was implemented instead of an integrator. Given a one G input and a sample rate of 600 kHz, the simulated Signal to Noise Ratio (SNR) is 57.5dB for a signal bandwidth of 200 Hz.

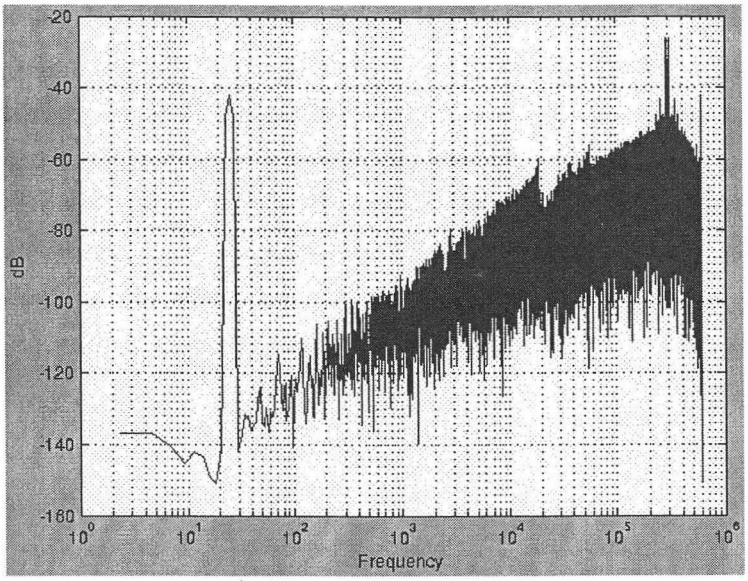

Figure 3.14 System simulation results.

Figure 3.15 shows the block diagram of the Simulink schematic with the amplifier thermal noise injected in the summing node of the integrator. This Simulink simulation technique was presented by Franco Maloberti for modeling amplifier non-idealities [12].

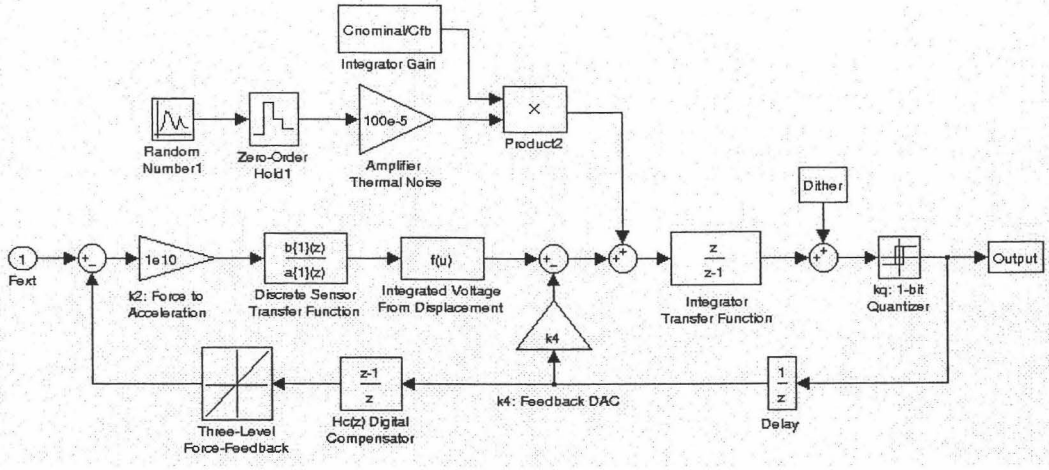

Figure 3.15 System simulation Simulink schematic with amplifier thermal noise.

The FFT provided in Figure 3.16 shows that the noise floor has increased from an ideal system of -140dB to a system with amplifier thermal noise of -110dB. The thermal noise injected into the system was 100e-5Vrms. Even though the noise floor was increased due to the included

amplifier thermal noise, a good portion of this noise was shape. Since the noise floor did not significantly increase, due to the large root mean squared (RMS) noise voltage injected in the system.

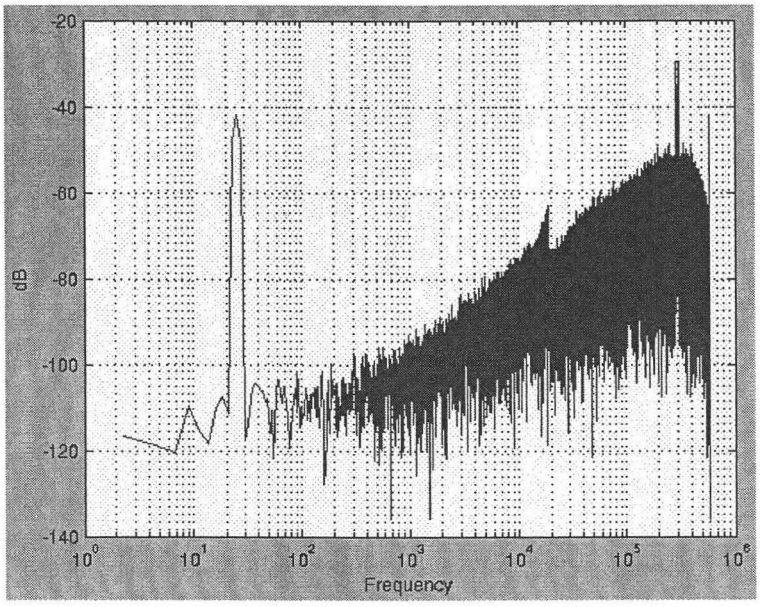

Figure 3.16 System simulation results with amplifier thermal noise.

Chapter 4.

INTERFACE IMPLEMENTATION

4.1 Process and Simulation Corners

Fabrication of the electrical interface chip was done by American Microsystems Inc. (AMI). AMI is vendor for MOSIS, a low-cost prototyping and small-volume production service for IC development. The interface design was fabricated in a 1.6μm, the minimum MOSFET gate length process.

The Spectre simulator through Cadence was used to simulate the analog blocks of the interface design. The Spectre models available through MOSIS are BSIM3. The models include only the nominal process at room temperature, 27 degrees Celsius, for the NMOS and PMOS devices. No other device process models are present including capacitors and resistors. Noise parameters were not available within the provided models in order to simulate the amplifier thermal and flicker (1/f) noise.

4.2 Amplifier Bandwidth Challenges

The amplifier bandwidth requirement depends on the distortion performance needed. A 90dB distortion requirement equates to 31.6228μVrms voltage error as shown in Equation 4.1.

$$error = 1e^{\frac{-Ts}{\tau}} = 90dB = 31.6228\mu V \tag{4.1}$$

The required unity gain bandwidth is derived from Equation 4.2 resulting in Equation 4.3. Solving τ, the settling time constant, from Equation 4.1 and the feedback factor, β, of the amplifier from Equation 4.5 are used to determine ω_{ugbw}.

$$\tau = \frac{1}{\beta w_{ugbw}} \tag{4.2}$$

$$w_{ugbw} = \frac{1}{\tau \cdot \beta} \tag{4.3}$$

Equation 4.1 is re-arranged in Equation 4.4 to solve for τ. Ts represents the time period available for the voltage to settle. This period is the clock period of the switch capacitor sampling clock, Fs. There are four phase in each integration cycle of the integrator. During each phase the node voltages must settle within the determined error voltage of the desired value. With a sampling clock frequency of 3MHz, the corresponding τ is equal to 32.17ns.

$$-Ts = \tau \ln(error) \Rightarrow \tau = \frac{-Ts}{\ln(error)} = 32.17ns \tag{4.4}$$

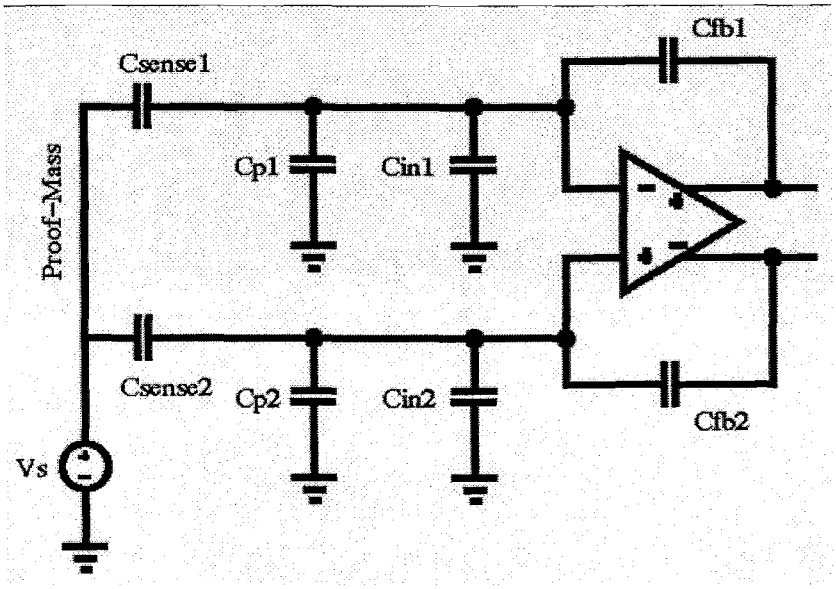

Figure 4.1 Integrator schematic showing the sampling, integrating, and parasitic capacitance.

In order to determine the feedback factor, the capacitive network of the integrator is analyzed in Figure 4.1. C_{sense} is the sense capacitor of the sensor and sampling capacitor of the interface integrator. C_p is the sum of the interconnect capacitances associated with this two-chip implementation. The input parasitic capacitance of the amplifier is represented by C_{in}. The integrating feedback capacitor is C_{fb}. From the integrator output back to the amplifier input is a capacitive divider representing the closed loop feedback factor of the amplifier as expressed in Equation 4.5.

$$\beta = \frac{C_{fb1}}{C_{fb1} + C_{sense1} + C_{p1} + C_{in1}} \tag{4.5}$$

The following two equations assume the parasitic capacitance C_{p1} of 5pF and 20pF. The other capacitances C_{fb1}, C_{sense1}, and C_{in1} are 200fF, 100fF, and 3pF respectively.

$$f_{ugbw} = \frac{1}{2\pi \cdot \tau \cdot \beta} = \frac{1}{2\pi \cdot 32.17ns \cdot 0.0240964} = 205.3MHz \tag{4.6}$$

$$f_{ugbw} = \frac{1}{2\pi \cdot \tau \cdot \beta} = \frac{1}{2\pi \cdot 32.17ns \cdot 0.0085837} = 576.4MHz \tag{4.7}$$

The required amplifier bandwidths are extremely fast and difficult to meet with the AMI 1.6μm process. The feedback factor, β, is extremely small in this application. From Equation 4.5, the effects of large interconnect parasitic capacitances experienced in this two-chip application can easily be seen on β. There are two negative effects on the amplifier requirements due to small feedback factors. The unity gain frequency bandwidth has been identified. The second is the closed loop gain of the amplifier is greatly reduced. A reduction in loop gain has a detrimental effect of the amplifier's distortion and noise in the integrator.

The initial interface amplifier's open and closed loop gain and phase responses are provided in Figures 4.2 and 4.3.

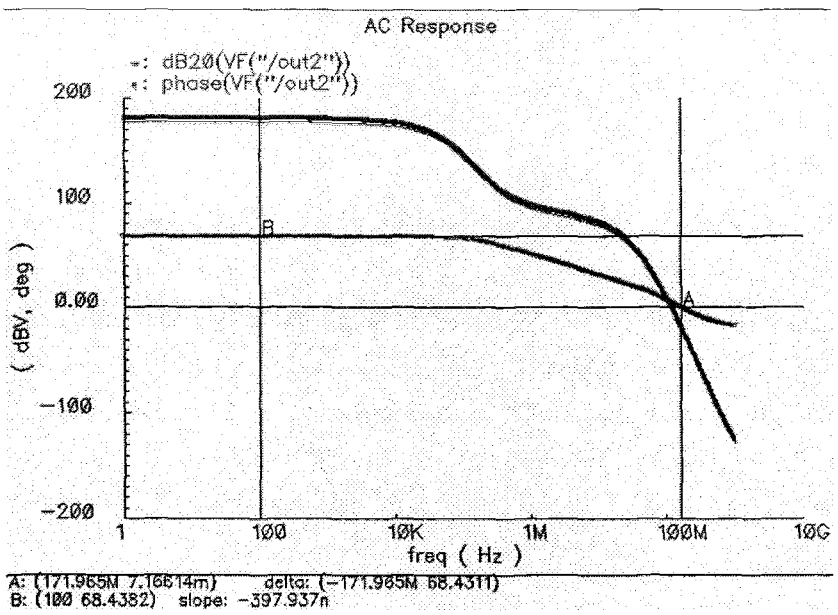

Figure 4.2 Open loop frequency response simulated for the initial interface amplifier.

From the open loop frequency response we can see that the DC gain is 68dB and the unity gain bandwidth is 172MHz with negative phase margin. Negative phase margin in any system will not be stable. However, these simulation results are from an open loop configuration. When determining the stability of a system, the closed loop which includes the feedback factor should be analyzed. Given that the feedback factor in this application is small, the closed loop frequency response is stable. The closed loop gain response is the open loop gain response multiplied by β. Since β is small, the open loop gain is shifted down lowering the gain and bandwidth but increasing the phase margin. This effect can be seen in Figure 4.3 showing the closed loop response.

From the closed loop frequency response we can see that the DC gain has reduced to 30.6dB and the unity gain bandwidth is 6MHz with plenty of positive phase margin. In the second interface design revision, the amplifier's gain and bandwidth were improved.

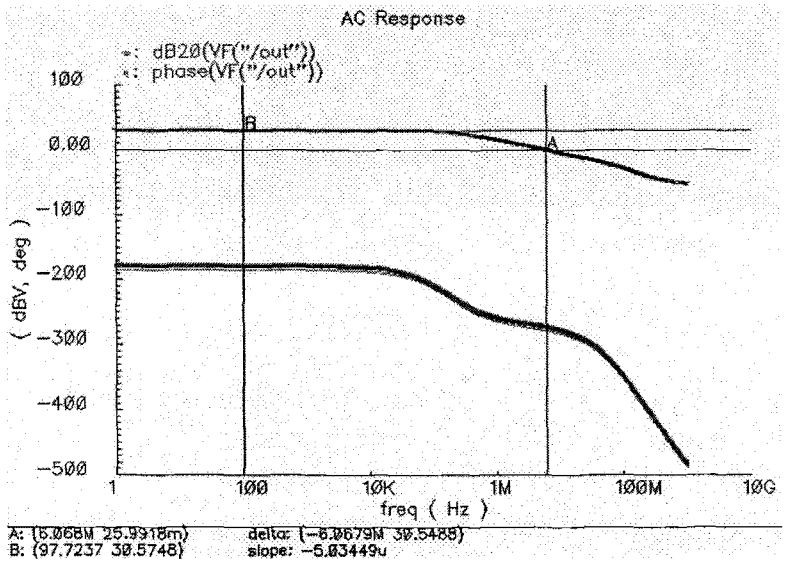

Figure 4.3 Closed loop frequency response simulated for the initial interface amplifier.

4.3 Amplifier Design

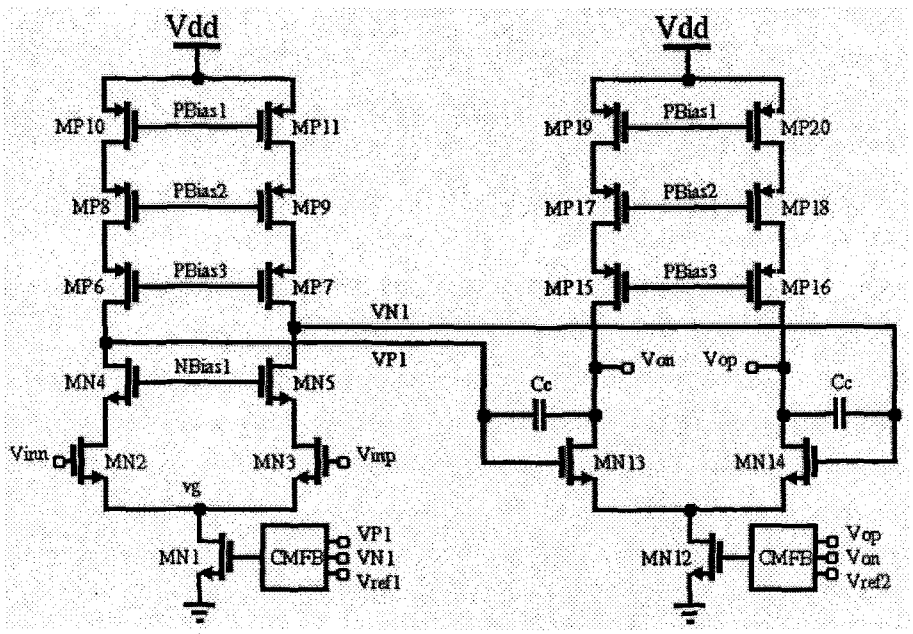

Figure 4.4 Amplifier schematic was implemented in the second design revision.

The integrator amplifier was redesigned in the second interface design as shown in figure 4.4. The two main parameters that needed to be met were the DC gain and unity gain bandwidth. Both of these parameters relate to the distortion and stability performance of the system. Other important amplifier parameters are thermal noise and slew rate. In order to achieve a high DC gain, a large amount of current was needed to increase the input transistor's gm. As a result, the thermal noise is lowered, and the slewing capability of the amplifier is increased with the increase in needed current.

The amplifier has two stages. The first stage is a telescopic amplifier with double cascode PMOS loads. The second stage is a standard differential amplifier with double cascode PMOS loads. A Miller compensation capacitor is present between the two stages for stability.

The gain of a multistage amplifier is the gain of each stage multiplied together. The telescopic stage's gain is expressed in Equation 4.8, and the second stage's gain is provided in Equation 4.9 [13].

$$-gm_{MN2}\left[\left(gm_{MN4}ro_{MN4}ro_{MN2}\right)//\left(gm_{MP6}ro_{MP6}gm_{MP8}ro_{MP8}ro_{MP10}\right)\right] \tag{4.8}$$

$$-gm_{MN13}\left[\left(ro_{MN13}\right)//\left(gm_{MP15}ro_{MP15}gm_{MP17}ro_{MP17}ro_{MP19}\right)\right] \tag{4.9}$$

Using the AMI 1.6μm process parameters, the gain can be calculated. The following three equations are used to determine the gain. The transconductance, gm, is determined in Equation 4.10 were β is derived from Equation 4.11. The output resistances, ro, are computed using Equation 4.12. The DC current, I_D, is the nominal bias current. For the second revision design the bias current for each amplifier is 1mA. Lambda, λ, is assumed to be 0.1. This is a reasonable assumption since the process is older with large, channel lengths.

$$gm = \sqrt{2\beta I_D} \tag{4.10}$$

$$\beta = KP \cdot \left(W/L\right) \tag{4.11}$$

$$r_0 = \frac{1}{\lambda \cdot I_D} \tag{4.12}$$

The NMOS and PMOS KP parameters are presented in Equations 4.13 and 4.14 respectively.

$$KP_{NMOS} = 35.9\mu A/V^2 \tag{4.13}$$

$$KP_{PMOS} = 12.1\mu A/V^2 \tag{4.14}$$

NMOS devices 2, 4, and 13 for simplicity are assumed to have the same gm. The amplifier's MOSFETs are sized such that aside from the tail currents all of the NMOS devices have the same W/L, and all of the PMOS devices have the same W/L. This is a reasonable assumption since the devices have the same dimension and I_D current.

$$gm_{MN13} = gm_{MN2} = gm_{MN4} = \sqrt{2 \cdot 35.9\left(\mu A/V^2\right) \cdot \left(1120\mu m/1.6\mu m\right) \cdot 1mA} \tag{4.15}$$

Therefore, the NMOS transconductance, gm_N, is computed and presented in then following equation.

$$gm_N = 7.0894e-3\left(A/V\right) \tag{4.16}$$

The same argument holds for the PMOS transconductance. The gm_P is computed in the next two equations.

$$gm_{MP15} = gm_{MP17} = gm_{MP6} = gm_{MP8} = \sqrt{2 \cdot 12.1\left(\mu A/V^2\right) \cdot \left(1472\mu m/1.6\mu m\right) \cdot 1mA} \tag{4.17}$$

$$gm_P = 4.7185e-3\left(A/V\right) \tag{4.18}$$

The output transistor resistances for both NMOS and PMOS devices are approximately 10kΩ.

$$ro_N = ro_P = \frac{1}{0.1 \cdot 1mA} = 10k\Omega \tag{4.19}$$

Using the previous relationships, the open loop gain of the amplifier is 110.76dB. The actual simulated open loop DC gain was 101.3dB indicating that the approximations and hand calculations are reasonable.

The Unity Gain Bandwidth (UGBW) for a two stage amplifier with a compensation capacitor can be approximated as shown in the following discussion [7]. The equivalent compensation capacitor as seen by the first stage is the following equivalent capacitance using Miller's Theorem derived in Equation 4.20.

$$C_{EQ} = C_C(1 + A_{2ndStage}) \cong C_C \cdot A_{2ndStage} \tag{4.20}$$

The gain of the first stage is the gm of MN2 and the output impedance of the first stage. The output impedance is the output resistance in parallel with the equivalent capacitance as presented below.

$$A_{1stStage} = -gm_{MN2} \cdot Z_{OUT1} = -gm_{MN2} \cdot \left(R_{OUT1} // \frac{1}{sC_{EQ}} \right) \tag{4.21}$$

For mid-band frequencies, the equivalent capacitance will dominate the output impedance as shown in Equation 4.22. The equation also shows the equivalent capacitance in terms of the compensation capacitor and the second stage gain.

$$A_{1stStage} \cong -gm_{MN2} \cdot \frac{1}{sC_{EQ}} = -gm_{MN2} \cdot \frac{1}{sC_C A_{2ndStage}} \tag{4.22}$$

The total gain of the amplifier is the first and second cascaded stages multiplied together. The resulting amplifier gain is shown in Equation 4.23.

$$A(s) = A_{1stStage} \cdot A_{2ndStage} = gm_{MN2} \cdot \frac{1}{sC_C A_{2ndStage}} \cdot A_{2ndStage} = \frac{gm_{MN2}}{sC_C} \tag{4.23}$$

In order to determine the unity gain bandwidth, the magnitude of the amplifier gain is set to one.

$$|A(jw)| = 1(UGBW) \tag{4.24}$$

From this relationship, the UGBW frequency is 564.2MHz.

$$\therefore f_{UGBW} = \frac{gm_{MN2}}{2\pi \cdot C_C} = \frac{7.0894e-3}{2\pi \cdot 2pF} = 564.16MHz \tag{4.25}$$

The simulation results for the gain and phase responses are shown in the next figures. The open loop, simulation results provided in Figure 4.5 confirm that the second revision amplifier has improved the DC gain and the UGBW. As expected, the open loop phase margin is negative. Figure 4.6 shows that the closed loop phase margin of the amplifier when applied in the system is positive and stable. The DC gain and unity bandwidth of this op-amp has been significantly increased over the initial fabricated design.

Due to the design requirements of the integrator, the amplifier has several layers of cascode. There is a need for the bias circuit to bias each device of the cascode without significantly degrading the output swing of the amplifier. A negative effects of interconnect parasitic capacitance is an increase in gain error. The extra voltage integrated due to gain error demands as large an output swing as possible. A wide-swing current mirror was implemented for this reason.

In any system, trying to achieve high accuracy noise is important. In switch capacitor networks, the thermal noise of the amplifier is sampled on the sampling and reference capacitors. The thermal noise of the amplifier is also sampled on interconnect parasitic capacitance. This is contrary to the initial design understanding and will be discussed later in this chapter and shown through experimental results in Chapter 6.

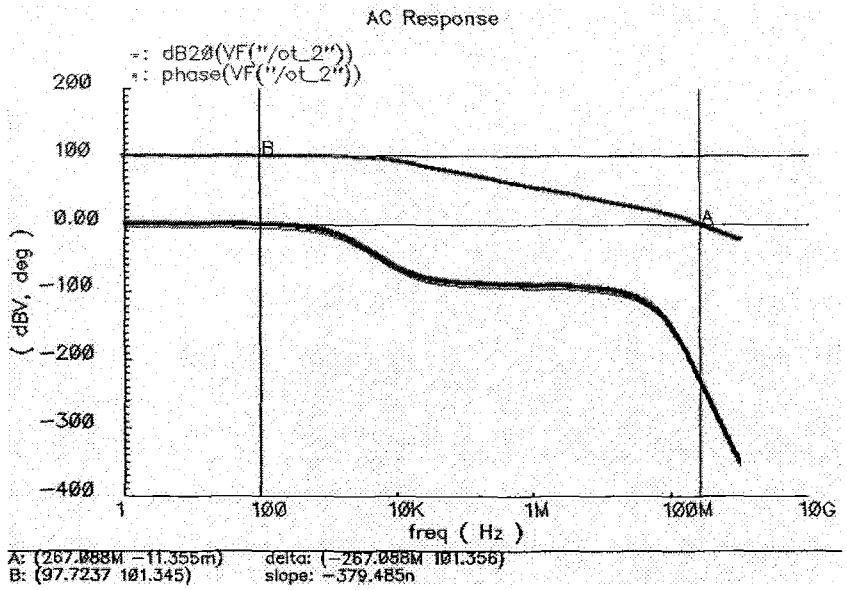

Figure 4.5 Open loop frequency response simulated for the re-designed interface amplifier.

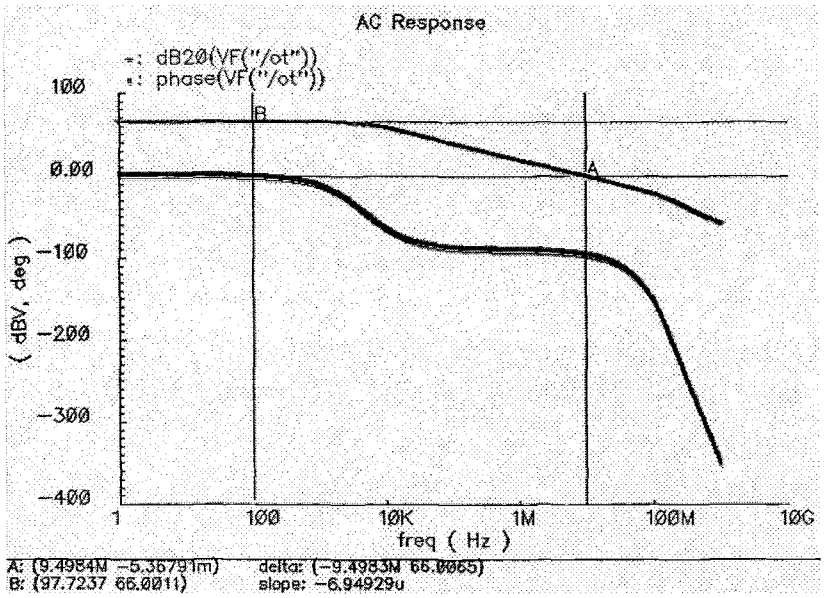

Figure 4.6 Closed loop frequency response simulated for the re-designed interface amplifier.

For this research, hand calculations of the amplifier thermal noise were relied upon. The Spectre models provided by AMI did not include noise model parameters for simulation. The flicker noise is not computed since the integrator implementation reduces flicker noise through correlated double sampling (CDS).

The following comments need to be considered when computing thermal noise [14]. There are several devices in an amplifier design, and only the devices in the signal path are important for noise analysis. For example, bias circuitry is not significant and should not be considered as noise sources. The noise in the second stage of a two-stage amplifier, as in this design, is not a significant noise source. When the noise generated in the second stage is referred to the input, it is divided by the square of the first stage gain. The noise from the tail current device, MN1, can be canceled with proper, layout techniques through symmetry and matching. Therefore, the noise sources to be considered are MN2-MN5 and MP6-MP11 of the telescopic, first stage amplifier.

$$\overline{i_{ON}^2} = gm_{N2}^2 \cdot \overline{v_{N2}^2} + gm_{N3}^2 \cdot \overline{v_{N3}^2} + gm_{N4}^2 \cdot \overline{v_{N4}^2} + gm_{N5}^2 \cdot \overline{v_{N5}^2} \tag{4.26}$$

$$\overline{i_{OP}^2} = gm_{P6}^2 \cdot \overline{v_{P6}^2} + gm_{P7}^2 \cdot \overline{v_{P7}^2} + gm_{P8}^2 \cdot \overline{v_{P8}^2} + gm_{P9}^2 \cdot \overline{v_{P9}^2} + gm_{P10}^2 \cdot \overline{v_{P10}^2} + gm_{P11}^2 \cdot \overline{v_{P11}^2} \tag{4.27}$$

$$\overline{i_O^2} = \overline{i_{ON}^2} + \overline{i_{OP}^2} \tag{4.28}$$

Through layout techniques of symmetry and matching, Equations 4.26 and 4.27 can be simplified.

$$\overline{i_O^2} = 2gm_{N3}^2 \cdot \overline{v_{N3}^2} + 2gm_{N5}^2 \cdot \overline{v_{N5}^2} + 2gm_{P7}^2 \cdot \overline{v_{P7}^2} + 2gm_{P9}^2 \cdot \overline{v_{P9}^2} + 2gm_{P11}^2 \cdot \overline{v_{P11}^2} \quad (4.29)$$

Equation 4.29 is output referred noise in terms of drain current. The input referred thermal noise is represented in Equation 4.30.

$$\overline{v_{NIN}^2} = \frac{\overline{i_O^2}}{gm_{N3}} = 2\left[\overline{v_{N3}^2} + \frac{gm_{N5}^2}{gm_{N3}^2} \cdot \overline{v_{N5}^2} + \frac{gm_{P7}^2}{gm_{N3}^2} \cdot \overline{v_{P7}^2} + \frac{gm_{P9}^2}{gm_{N3}^2} \cdot \overline{v_{P9}^2} + \frac{gm_{P11}^2}{gm_{N3}^2} \cdot \overline{v_{P11}^2}\right] \quad (4.30)$$

The input referred noise voltage for a transistor in saturation is show in Equation 4.31. If the bulk and source do not have the same potential, then Equation 4.32 applies. The temperature, T, is in Kelvins and typically 300 degrees. K is the Boltzmann constant equal to $1.38\text{x}10^{-23}$ (J/K), and f_{SBW} is the signal band of interest.

$$\overline{v_{NT}^2} = 4KT\frac{2}{3}gm \cdot f_{SBW} \quad (4.31)$$

$$\overline{v_{NT}^2} = 4KT\frac{2}{3}(gm + gmbs) \cdot f_{SBW} \quad (4.32)$$

Using Equations 4.30 and 4.31 and the value for gm computed previously for the gain, a noise power approximation for the amplifier is 9.0305E-20 square voltage per hertz for a 200Hz signal band.

In sampled systems the out of signal band noise is folded in band [15]. Assuming a single pole AC characteristic, the noise bandwidth of the amplifier is $\pi/2 \cdot f_{UGBW}$ where f_{UGBW} is the unity gain bandwidth of the amplifier. If the flicker noise is not considered, it is assumed that the thermal noise in band and each folded side band noise contribution are equal. The total thermal folded noise is expressed in Equation 4.33.

$$\overline{v_{TH}} = \sqrt{\overline{v_{TH}^2}(\pi \cdot \frac{f_{UGBW}}{f_S}) \cdot f_{SBW}} \quad (4.33)$$

Substituting the result 9.0305E-20 square voltage per hertz into Equation 4.33, the complete amplifier folded thermal noise is

$$\overline{v_{TH}} = 158.9nV \quad (4.34)$$

Slew rate is an important high frequency parameter of SC amplifiers. Slew rate is the maximum rate at which the output changes when input signals are large. For the integrator design in this research, it was desirable to achieve the fastest sample clock rate possible to improve system noise. Secondly, due to the input voltage pulse on the beam the output voltage steps are

quite large. For a two stage amplifier with a Miller compensation capacitor, the slew rate can be approximated by the first stage's tail current divided by the compensation capacitor as show in Equation 4.35.

$$SR = \frac{I_{DMN1}}{C_C} = \frac{2mA}{2pF} = 1000\,V/\mu s \tag{4.35}$$

Given that the unity gain bandwidth and noise were important design parameters requiring a large amount of current, the slew rate performance was not compromised.

4.4 Amplifier Common Mode Feedback

Although the magnitude and percent mismatch of parasitic capacitance has a considerable effect on the performance of the modulator, a ten percent difference should not cause the modulator to saturate. It was determined that the saturation in the initial design was due to the amplifier's common-mode feedback (CMFB). The CMFB produced a large common mode output ripple. The ripple is considered to be the output swing of the integrator when no input signal or parasitic mismatch is present. Together a parasitic mismatch error term and a large CM output ripple can easily saturate the modulator even for small input parasitic mismatch. The CMFB produced a large ripple because of the following four reasons. First, the switches found in the CMFB SC circuit were too large, creating charge injection problems on the output voltage. Second, the averaging capacitors, Ca as presented in Figure 4.7, in the SC CMFB circuit were too small, allowing the output to leak. Third, the averaging and biasing capacitors, Cs, have a ratio of one half, which aggressively pulls on the output. Last, the CMFB would update in phases when the output is not valid.

The averaging capacitors of the CMFB were increased, in order to reduce the leakage at the output. With larger averaging capacitors, the ratio between the averaging and biasing capacitors has been reduced from one-half to one-tenth. This will lower the effect of the biasing capacitor on the output. The clocking of the CMFB has been changed to adjust the output common-mode while the output is valid.

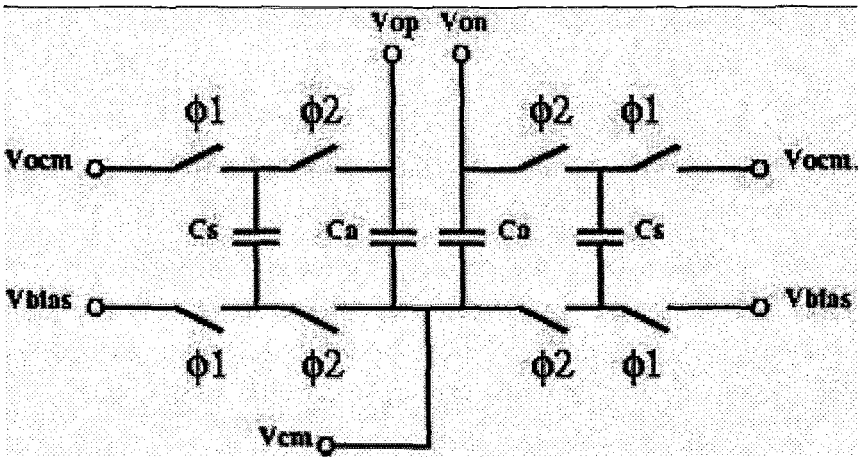

Figure 4.7 Amplifier common mode feedback structure.

4.5 Integrator Switch Design Implications

The improved chip uses minimum sized switches throughout the CDS integrator and SC CMFB circuits. The switch sizes are as small as possible in order to reduce charge injection. As stated, a large switch will experience more charge injection than a smaller switch. Another switch design consideration is the parasitic gate capacitance. The larger the capacitance the more clock and signal feed through is experienced [7]. However, there is a limit to the amount of reduction possible to the switches. The switch resistance increases with the reduction in switch size and gm. This increase in resistance has an RC filtering effect with the capacitors within a switch capacitor network limiting the sampling frequency of the integrator. The initial and re-design switch resistances are provided in Figures 4.8 through 4.11. The initial design CMOS and NMOS switch resistance are provided as the drain and source voltages are swept in Figures 4.8 and 4.9. The CMOS switch is used when large swing signals need to pass through the switch. Since a PMOS device can pass Vdd and an NMOS device can pass ground potentials without requiring a threshold voltage drop. The switches at the amplifier input are NMOS. Since the voltage swings are minimal, the switch is always biased properly. The maximum CMOS switch resistance is less than 1.4kΩ, and NMOS switch resistances for a drain voltage of 2.5V is around 700Ω.

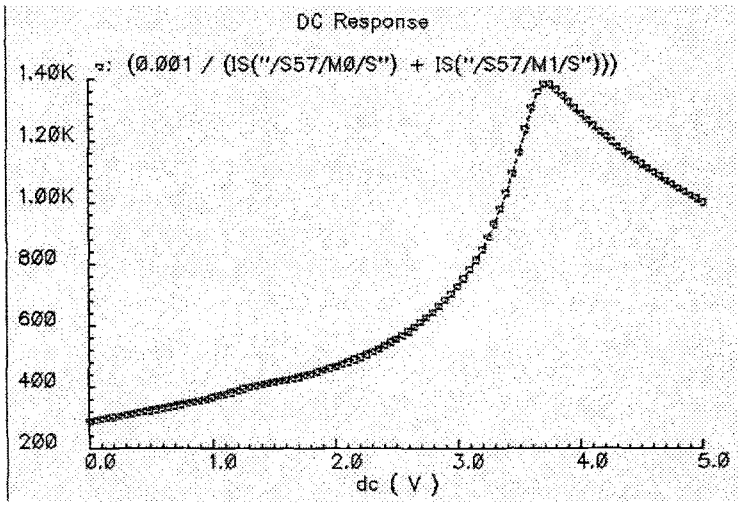

Figure 4.8 DC sweep resistance simulated for the CMOS initial design switch.

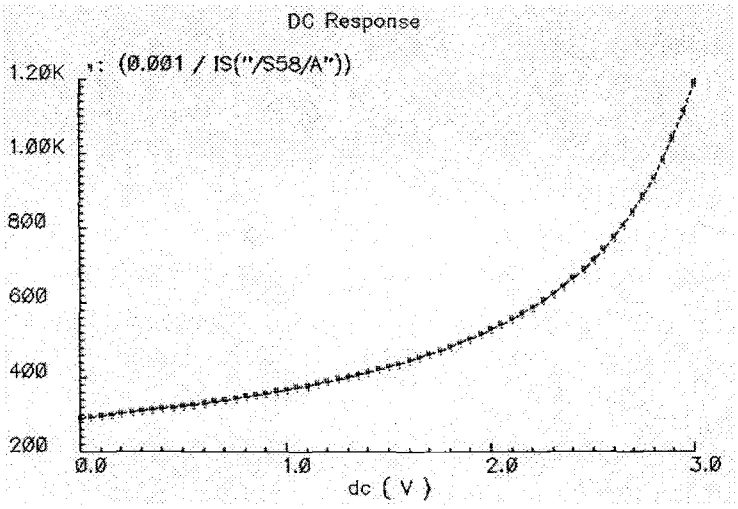

Figure 4.9 DC sweep resistance simulated for the NMOS initial design switch.

The second design CMOS and NMOS switch resistance are provided as the drain and source voltages are swept in Figures 4.10 and 4.11. The maximum CMOS switch resistance is almost 40kΩ, and NMOS switch resistances for a drain voltage of 2.5 is around 12kΩ.

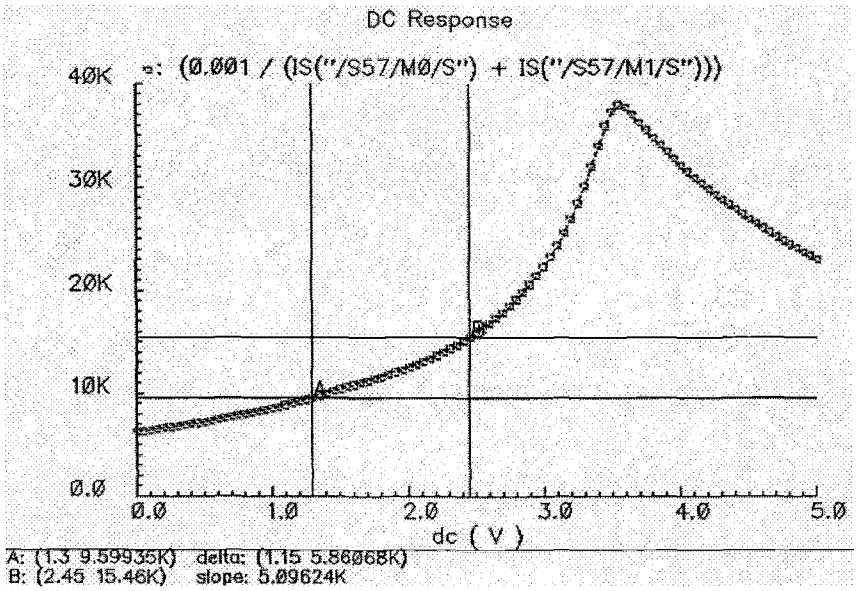

Figure 4.10 DC sweep resistance simulated for the CMOS re-design switch.

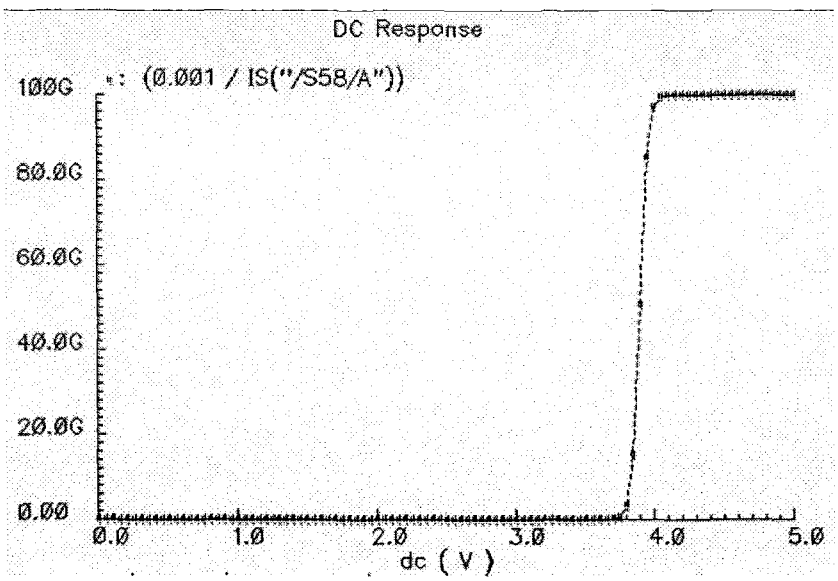

Figure 4.11 DC sweep resistance simulated for the NMOS re-design switch.

As a rule of thumb the RC effect of a switch resistance and sampling or integrating capacitor need to be five times larger than the second pole of the integrator's amplifier [16]. Equations 4.36 and 4.37 show the limiting settling frequency of the sampling and integrating capacitor due to the switch resistance.

$$f_{switch} = \frac{1}{2\pi R_{switch} C_{IN}} = \frac{1}{2\pi \cdot 12k\Omega \cdot 100fF} = 132MHz \quad (4.36)$$

$$f_{switch} = \frac{1}{2\pi R_{switch} C_{INT}} = \frac{1}{2\pi \cdot 12k\Omega \cdot 200fF} = 66.3MHz \quad (4.37)$$

The second pole of the amplifier is beyond 270MHz.

These switches were also used in the inner loop feedback DAC design presented in Figure 3.10. The NMOS switches were use to select +VREF or –VREF to the reference sampling capacitor depending on the quantization output. Recall from Figure 4.11, that the on resistance is extremely high especially with drain voltages greater than 3.8V. Above a 3.8 drain voltage, the switch is open. The gate to source voltage across the NMOS device is not larger than the drain voltage by the device threshold voltage needed for saturation. As a result the maximum reference that can be applied in the feedback is limited due to the NMOS threshold voltage. Therefore, the maximum reference voltage that can be feedback due to the switch biasing limitation is a differential 6V. The +VREF and –VREF are equal to 3V and 0V respectively. The differential reference voltage is shown in Equation 4.38.

$$VREF_{DIFF} = (+VREF - -VREF) - (-VREF - +VREF) = (3-0) - (0-3) = 6V \quad (4.38)$$

In order to have the full differential reference tune available for the re-design, CMOS switches should have been used. The second implication on the reference design is that the intended reference centered about input CM would reduce the maximum available reference even further due to the –VREF voltage being higher than 0V.

4.6 Correlated Double Sampling

The integrator used in the implementation of the interface circuit is a new correlated double sampling scheme proposed by Tetsuya Kajita [17]. This novel architecture is intended to improve the performance of an integrator with large parasitic capacitance at the input of an amplifier for applications similar to this research. These improvements include a reduction in flicker noise and DC offset voltage of the amplifier and KT/C noise of the parasitic capacitance. The basic concept of Correlated Double Sampling (CDS) is to sample unwanted noise and offset, and then subtract it from the contaminated signal either at the input or the output of the amplifier [18].

By following three rules, the negative effects of a large input parasitic capacitance can be minimized [17]. First, the two-chip interconnect parasitic capacitance at the input of the amplifier must not be reset in any clock phase. If this capacitor were reset, a large charge would be integrated since the input VCM is not an exact potential. This error charge would contain sampled amplifier flicker and thermal noise, signal voltages due to finite amplifier gain, and KT/C noise. The second rule is to remove any switches between the parasitic capacitance and the input of the amplifier. An increase in KT/C noise would result from adding this switch. Finally, the front-end block must be an integrator and not a gain stage. With an integrator implementation, noise shaping can be used to reduce the signal band noise significantly.

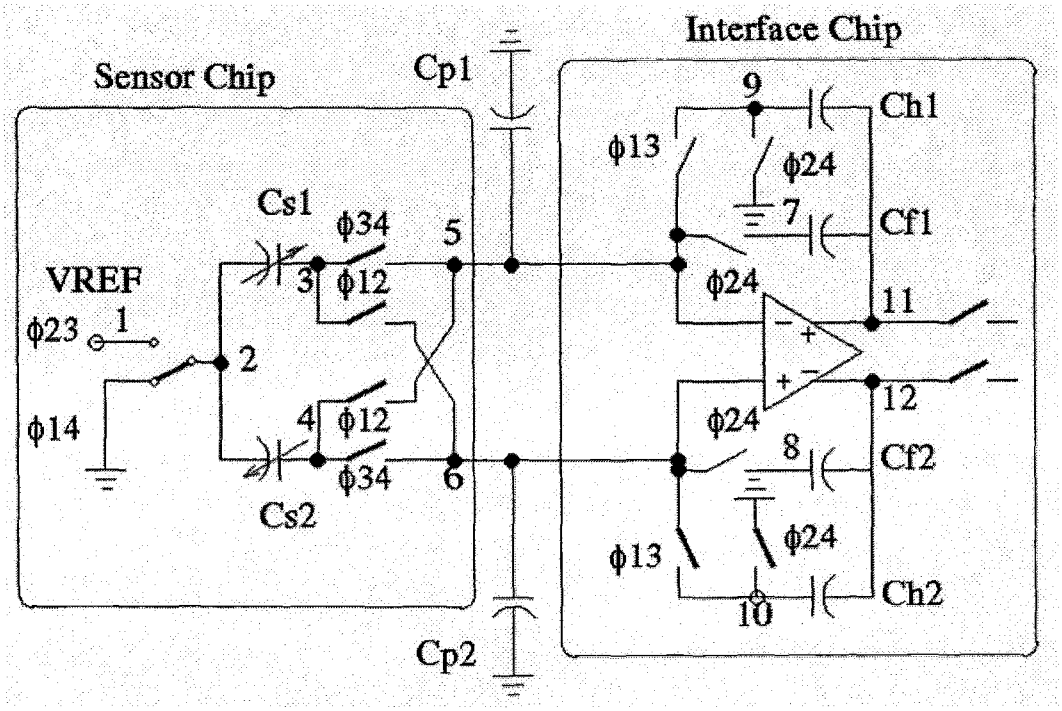

Figure 4.12 Schematic of the switch capacitor, CDS network.

In order to verify the attenuation in amplifier offset and 1/f noise, the charge equations from phase Φ1 to Φ2 are derived. The charge equations will be similar from Φ3 to Φ4, but with the input cross coupled. Node voltages that reflect Φ1 will have a superscript A and voltages present in Φ2 will have a superscript B. A node voltage during Φ4 is also needed and will be indicated by a superscript D. To simplify the derivation only the inverting side of the differential integrator will be considered. The charge equations for each capacitor during Φ1 are found in Equations 4.39

through 4.40. The voltage across capacitor C_{h1} does not change from Φ1 to Φ2. Therefore, the change in charge is zero and will be excluded from the Φ1 to Φ2 derivation.

$$QC_{S2} = (V_5^A - 0)C_{S2} \tag{4.39}$$

$$QC_{f1} = (V_5^D - V_{11}^A)C_{f1} \tag{4.40}$$

During Φ2 the charge equations are as follows:

$$QC_{S2} = (V_5^B - V_{REF})C_{S2} \tag{4.41}$$

$$QC_{f1} = (V_5^B - V_{11}^B)C_{f1} \tag{4.42}$$

Equations 4.43 through 4.44 show the change in charge for each capacitor from Φ1 to Φ2.

$$\Delta QC_{S2} = (V_5^B - V_5^A - V_{REF})C_{S2} \tag{4.43}$$

$$\Delta QC_{f1} = (V_5^B - V_5^D + V_{11}^A - V_{11}^B)C_{f1} \tag{4.44}$$

The change in charge on C_{S2} is integrated through C_{f1}. The holding capacitor C_{h1} is switched to the signal ground and is not involved in integrating the charge sampled by C_{S2}. Summing the charge contributions so that charge is conserved and maintaining the inverting property of the integrator, Equation 4.45 is determined.

$$\Delta QC_{S2} + \Delta QC_{f1} = 0 \tag{4.45}$$

Equation 4.46 shows the delta charge equations for C_{S2} and C_{f1} substituted into Equation 4.45.

$$(V_5^B - V_5^A - V_{REF})C_{S2} + (V_5^B - V_5^D + V_{11}^A - V_{11}^B)C_{f1} = 0 \tag{4.46}$$

The integrating and holding capacitors have the same capacitance. Therefore, capacitor, $C_{fb,}$ is substituted into Equation 4.46 for C_{f1}.

$$(V_5^B - V_5^A - V_{REF})\frac{C_{S2}}{C_{fb}} + (V_5^B - V_5^D + V_{11}^A - V_{11}^B) = 0 \tag{4.47}$$

The following substitutions were made to Equation 4.47. V_{sgnd} for simplicity is equal to zero. V_{REF} is the input signal V_{IN}. V_{OS} is the amplifier offset voltage which will be shown to be attenuated through this CDS implementation.

$$\mu = \frac{1}{A_{GAIN}} \tag{4.48}$$

$$V_5^A = -\mu V_{11}^A + V_{OS} \tag{4.49}$$

$$V_5^B = -\mu V_{11}^B + V_{OS} \tag{4.50}$$

$$V_5^D = -\mu V_{11}^D + V_{OS} \tag{4.51}$$

$$(-\mu V_{11}^B + \mu V_{11}^A - V_{IN})\frac{C_{S2}}{C_{fb}} + (-\mu V_{11}^B + \mu V_{11}^D + V_{11}^A - V_{11}^B) = 0 \tag{4.52}$$

$$V_{11}^B \cdot (1 + \mu \cdot (1 + \frac{C_{S2}}{C_{fb}})) = -V_{IN} \cdot \frac{C_{S2}}{C_{fb}} + V_{11}^A \cdot (1 + \mu \cdot \frac{C_{S2}}{C_{fb}}) + \mu V_{11}^D \tag{4.53}$$

To finish Equation 4.53, the voltage at node 11 during Φ4 needs to be expressed in terms of offset and Φ1 or Φ2 voltages. Continuing with the analysis, the charge equations for the previous phase Φ4 to Φ1 are derived. During Φ4, C_{S1} is connected to the inverting input of the amplifier. The voltage across capacitor C_{fl} does not change from Φ4 to Φ1. Therefore, the change in charge is zero and will be excluded from the Φ4 to Φ1 derivation.

$$QC_{S1} = (V_5^D - 0)C_{S1} \tag{4.54}$$

$$QC_{h1} = (V_{sgnd} - V_{11}^D)C_{h1} \tag{4.55}$$

During Φ1 the charge equations are presented in Equations 4.56 and 4.57. Note that C_{S2} is now connected to the inverting input of the amplifier.

$$QC_{S2} = (V_5^A - 0)C_{S2} \tag{4.56}$$

$$QC_{h1} = (V_5^A - V_{11}^A)C_{h1} \tag{4.57}$$

Equations 4.58 through 4.59 show the change in charge for each capacitor from Φ4 to Φ1.

$$\Delta QC_{S2} = (V_5^A - V_5^D)C_{S2} \tag{4.58}$$

$$\Delta QC_{h1} = (V_5^A + V_{11}^D - V_{sgnd} - V_{11}^A)C_{h1} \tag{4.59}$$

The change in charge on C_{S2} is integrated through C_{h1}. Summing the charge contributions so that charge is conserved and maintaining the inverting property of the integrator, Equation 4.60 is determined.

$$\Delta QC_{S2} + \Delta QC_{h1} = 0 \tag{4.60}$$

Equation 4.61 shows the delta charges equations for C_{S2} and C_{h1} substituted into Equation 4.60.

$$(V_5^A - V_5^D)C_{S2} + (V_5^A + V_{11}^D - V_{sgnd} - V_{11}^A)C_{h1} = 0 \tag{4.61}$$

The integrating and holding capacitors have the same capacitance. Capacitor C_{fb} is substituted into Equation 4.61 for C_{h1}. Remember, V_{sgnd} is equal to zero.

$$(-\mu V_{11}^{A} + \mu V_{11}^{D})\frac{C_{S2}}{C_{fb}} + (-\mu V_{11}^{A} + V_{OS} + V_{11}^{D} - V_{11}^{A}) \tag{4.62}$$

The voltage at node 11 during Φ4 is solved in Equation 4.63.

$$V_{11}^{D} = \frac{V_{11}^{A} \cdot (1 + \mu \cdot (1 + \frac{C_{S2}}{C_{fb}})) - V_{OS}}{(1 + \mu \cdot \frac{C_{S2}}{C_{fb}})} \cong V_{11}^{A} - V_{OS} \tag{4.63}$$

The gain from Φ1 to Φ2 is determined by substituting Equation 4.63 into 4.53 and V_{OUT} for $V_{11}^{B} - V_{11}^{A}$. Equation 4.64 shows that the offset voltage is attenuated by the DC gain of the amplifier.

$$V_{OUT} \cdot (1 + \mu \cdot (1 + \frac{C_{S2}}{C_{fb}})) = -V_{IN}\frac{C_{S2}}{C_{fb}} + \mu V_{OS} \tag{4.64}$$

4.7 Interface Integrator Gain Error

Another effect of the parasitic capacitance is the percent mismatch between the differential inputs of the amplifier. The integrator error terms derived in Equations 4.65 and 4.66 represent the charge equations of the differential integrator output from phase Φ1 to Φ2. Voltages relating to Φ1 and Φ2 are indicated by an A and B superscript respectively.

$$V_{11}^{B} - V_{12}^{B} = \frac{1}{C_{df}}\left[V_{REF}(C_{S2} - C_{S1}) + C_{S1}(V_5^{B} - V_5^{A}) - C_{S2}(V_6^{B} - V_6^{A}) + C_{P1}(V_5^{B} - V_5^{A}) - C_{P2}(V_6^{B} - V_6^{A})\right] \tag{4.65}$$

$$error = \frac{1}{C_{df}}\left[C_{S1}(V_5^{B} - V_5^{A}) - C_{S2}(V_6^{B} - V_6^{A}) + C_{P1}(V_5^{B} - V_5^{A}) - C_{P2}(V_6^{B} - V_6^{A})\right] \tag{4.66}$$

The error is amplified by the ratio of the parasitic capacitance mismatch to the integrator's feedback capacitance. These equations indicate that the closer the amplifier inputs remain to each other from phase to phase, as well as, the mismatch between the sensor sampling and parasitic capacitors, the smaller the error term becomes. When the feedback factor is decreased by an increase in parasitic capacitance magnitude, the loop gain is reduced. When the loop gain of the integrator is reduced, the integrator becomes more sensitive to percent mismatch. Since, it becomes harder for the amplifier to hold the two differential inputs at the same potential. Therefore, there is a limit to the increase in performance by adding capacitance to improve the parasitic matching.

4.8 KT/C and Thermal Noise

In switch capacitor integrators, sampled KT/C and amplifier thermal noise are important design considerations. An increase in noise will degrade the resolution of the system. The signal to noise ratio (SNR) will decrease with increases in noise and reduce the amount of detectable signal. The following discussion will compute the estimated integrator input referred noise. The noise from the SC feedback network is not considered in this analysis.

KT/C is a noise power, and the V_{RMS} is determined by taking the square root. If you multiply the V_{RMS} noise voltage by the applicable capacitance, the result is RMS charge, q_{RMS}. Figure 4.13 shows the single-ended block diagram of the integrator in terms of charge [19]. From this diagram, the input referred noise will be determined. The charge noise sources that have been included in the diagram are the KT/C noise for the sampling and reference capacitors, the thermal noise for the amplifier, and the feedback reference thermal noise. The KT/C noise represented in charge is expressed in Equation 4.67.

$$\overline{q_C} = C \cdot \overline{V_N} = C \cdot \sqrt{\frac{KT}{C}} = \sqrt{KTC} \tag{4.67}$$

In over sampled systems, the KT/C noise is reduced by a factor of the over sampling ratio (OSR) shown in Equation 4.69. OSR is the sample frequency divided by the twice the signal bandwidth of interest.

$$OSR = \frac{f_S}{2 \cdot f_{SBW}} \tag{4.68}$$

$$\overline{q_C} = \sqrt{\frac{KTC}{OSR}} \tag{4.69}$$

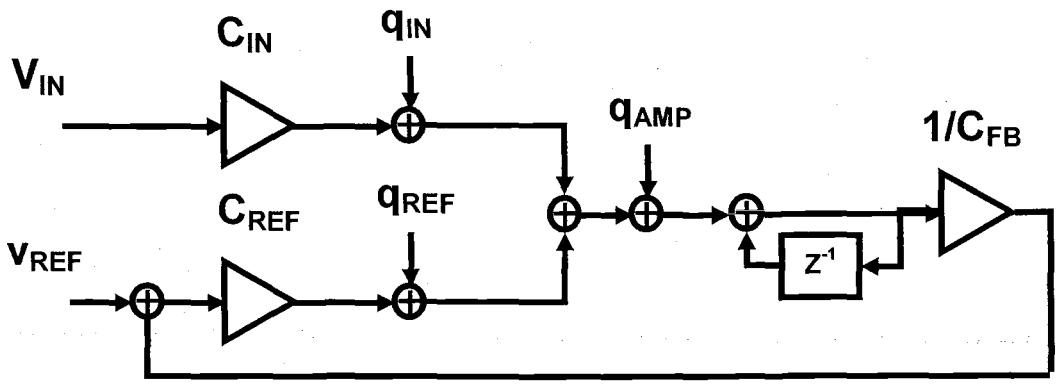

Figure 4.13 Integrator block diagram for noise analysis.

The noise of the amplifier is sampled onto the input sampling and reference capacitors. This noise is correlated between the capacitors and shown in Equation 4.70.

$$\overline{q_{AMP}} = \sqrt{\overline{V_{TH}^2} \cdot (C_{IN} + C_{REF})^2} \tag{4.70}$$

The block diagram in Figure 4.13 is re-arranged using Equations 4.69 and 4.70 and shown in Figure 4.14. This figure simplifies the task of computing the input referred thermal noise and signal to noise ratio (SNR). Adding the charge noise contributions at q_{Total} node in Figure 4.14 equates to Equation 4.71.

$$\overline{q_{Total}} = \sqrt{\frac{KT(C_{IN} + C_{REF})}{OSR} + \overline{V_{AMP}^2} \cdot (C_{IN} + C_{REF})^2 + \sqrt{\overline{V_{REF}^2} \cdot C_{REF}^2}} \tag{4.71}$$

Moving the charge noise to voltage noise at the summing node in the block diagram is shown in Equation 4.72.

$$\overline{V_{Total}} = \frac{1}{C_{REF}} \cdot \sqrt{\frac{KT(C_{IN} + C_{REF})}{OSR} + \overline{V_{AMP}^2} \cdot (C_{IN}^2 + C_{REF}^2) + \overline{V_{REF}^2} \cdot C_{REF}^2} \tag{4.72}$$

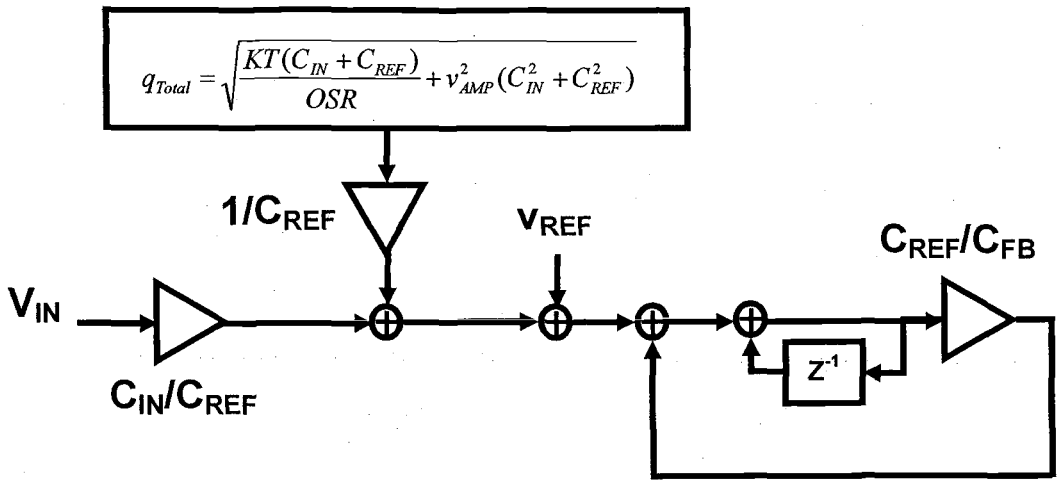

Figure 4.14 Modified integrator block diagram for noise analysis.

The signal to noise ratio at the summing node of the integrator block diagram is computed in Equation 4.74. Therefore, the noise of the integrator is found in Equation 4.75.

$$SNR = \frac{V_{IN} \cdot \frac{C_{IN}}{C_{REF}}}{\frac{1}{C_{REF}} \cdot \sqrt{\frac{KT(C_{IN}+C_{REF})}{OSR} + \overline{V_{AMP}^2} \cdot (C_{IN}+C_{REF})^2 + \overline{V_{REF}^2} \cdot C_{REF}^2}} \tag{4.73}$$

$$SNR = \frac{V_{IN}}{\sqrt{\frac{KT(C_{IN}+C_{REF})}{OSR \cdot C_{IN}^2} + \overline{V_{AMP}^2} \cdot (1+\frac{C_{REF}}{C_{IN}})^2 + \overline{V_{REF}^2} \cdot \frac{C_{REF}^2}{C_{IN}^2}}} \tag{4.74}$$

$$\overline{V_{Total}^2} = \sqrt{\frac{KT(C_{IN}+C_{REF})}{OSR \cdot C_{IN}^2} + \overline{V_{AMP}^2} \cdot (1+\frac{C_{REF}}{C_{IN}})^2 + \overline{V_{REF}^2} \cdot \frac{C_{REF}^2}{C_{IN}^2}} \tag{4.75}$$

The previous equations represent a single-ended integrator. Having two sampling and reference capacitors a factor of two needs to be added to Equation 4.75.

$$\overline{V_{Total}^2} = \sqrt{\frac{2 \cdot KT(C_{IN}+C_{REF})}{OSR \cdot C_{IN}^2} + 2 \cdot \overline{V_{AMP}^2} \cdot (1+\frac{C_{REF}}{C_{IN}})^2 + 2 \cdot \overline{V_{REF}^2} \cdot \frac{C_{REF}^2}{C_{IN}^2}} \tag{4.76}$$

In the three-axis micro-machined accelerometer paper, Mark Lemkin and Bernhard Boser warn that if the parasitic capacitance becomes larger than the sense and integrating capacitors, C_{IN} and C_{FB}, the output noise increases significantly [2]. Equation 4.77 adds the effects of the parasitic capacitor, C_P.

$$\overline{V_{Total}^2} = \sqrt{\frac{2 \cdot KT(C_{IN} + C_P + C_{REF})}{OSR \cdot C_{IN}^2} + 2 \cdot \overline{V_{AMP}^2} \cdot (1 + \frac{C_P}{C_{IN}} + \frac{C_{REF}}{C_{IN}})^2 + 2 \cdot \overline{V_{REF}^2} \cdot \frac{C_{REF}^2}{C_{IN}^2}} \quad (4.77)$$

From this equation, it is shown that if the parasitic capacitor sampled the amplifier noise and assuming a capacitance of 10pF, the amplifier noise contribution would increase by a factor of ten thousand. The noise increases from -126.95dB to -92.8dB with a 10pF parasitic capacitance. For a 20pF parasitic capacitance, the noise increases to -86.86dB.

Tetsuya Kajita states that if the parasitic capacitance is not reset the amplifier noise is not sampled and therefore, Equation 4.76 holds for the integrator design [17]. Tetsuya Kajita is missing one fundamental concept that Bernhard Boser points out in his paper [2]. Due to the voltage pulse on the beam of the capacitive sensor, large voltage fluctuation are present at the amplifier input causing charge to flow onto the integrating capacitors and the amplifier noise to be amplified. This voltage fluctuation described by Bernhard Boser is shown in Figure 4.15. The transient response of the amplifier input fluctuations are shown to be 46mV with matched parasitic capacitance of 10pF. Given Boser's observations and analysis and the experimental results of this research, it is concluded that the noise equation shown Equation 4.77 is correct.

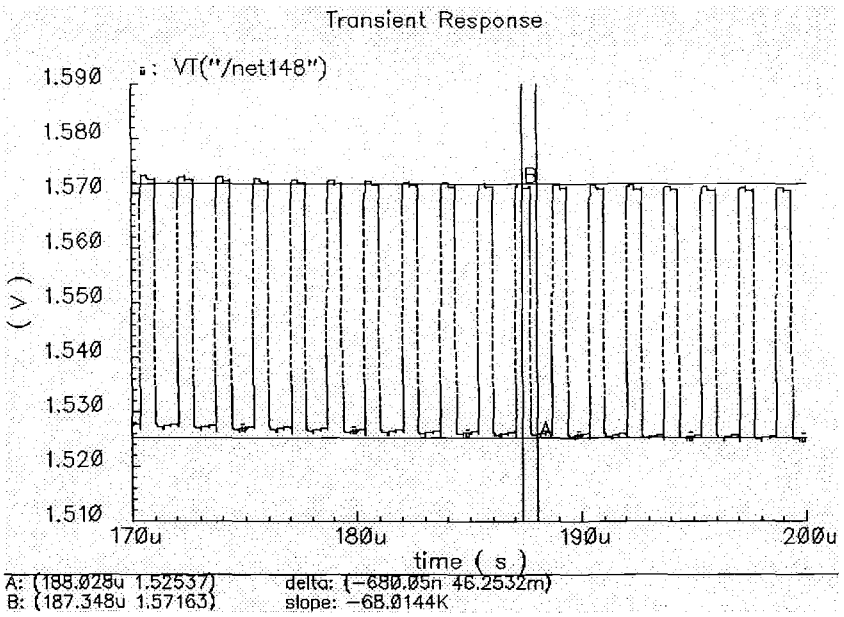

Figure 4.15 Amplifier input fluctuations due to voltage pulse on sensor beam.

Chapter 5.

TEST STRUCTURES AND METHODOLOGY

5.1 Interface On-Chip Test Structures

Two test structures were placed on the interface chip. One allows capacitors to be connected to the inputs of the amplifier in order to improve the parasitic capacitance mismatch as shown in Figure 5.1. The maximum amount of available on-chip parasitic matching capacitance with all four capacitors connected in parallel is 3.75pF. The tune ability is shown in the schematic with four various capacitors available. Lowering the parasitic mismatch between the inputs of the amplifier will make a significant improvement in the performance of the DS modulator. These improvements include a reduction in noise, gain error, offset, increased SNDR, and input dynamic range. This test structure serves two important functions. If the performance of the integrator is improved by adjusting the amount of capacitance connected to the amplifier inputs, it is proven that the integrator is in fact sensitive to the parasitic mismatch capacitance. If sensitive, this structure is available to improve the capacitive mismatch between the inputs.

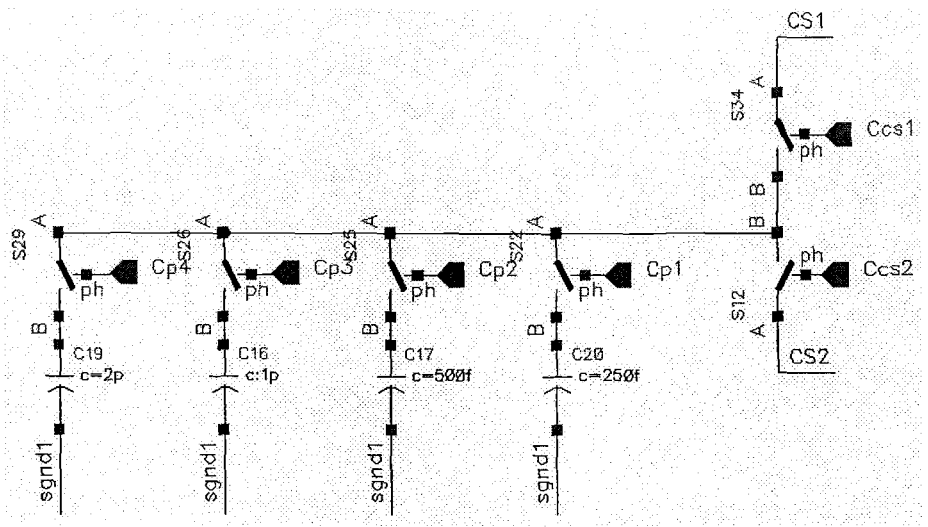

Figure 5.1 Parasitic capacitance matching test structure.

The second structure is used to replicate the sensor SC network on the interface chip shown in Figure 5.2. In addition to the on chip accelerometer model, the ability to switch in extra sampling capacitance to either CS1 or CS2 gives the model the ability to simulate DC applied acceleration. One or two 5fF capacitors can be added to each sampling capacitor. This equates to about 125Gs (gravity) per 5fF capacitance. Given process limitations and the fact that high thermal noise was observed on the initial design, 5fF seemed reasonable.

The connection between the on-chip sensor SC network and the interface is made at the package pins. Therefore, interconnect parasitic capacitance is still considered in the test structure but more controlled. Package pins that have matched parasitics were used for the interconnection between the sampling capacitor and the amplifier inputs reducing the parasitics as much as possible.

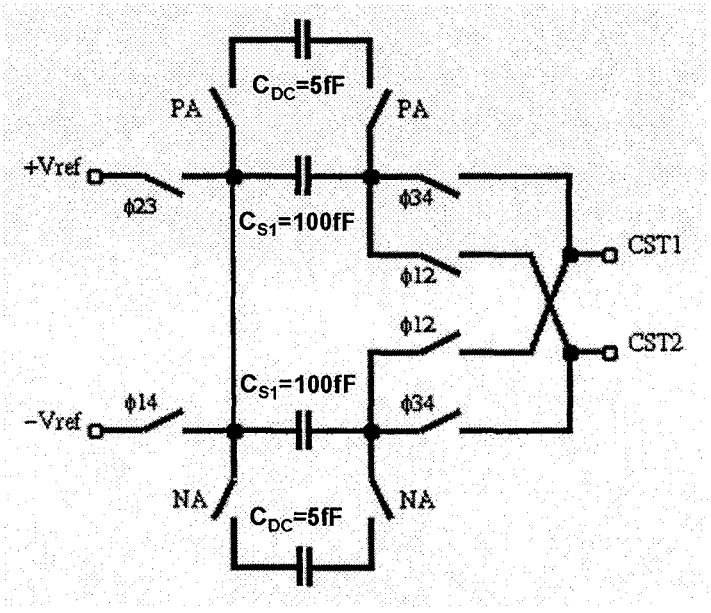

Figure 5.2 Capacitive Sensor model on the interface chip to simulate a constant DC acceleration.

5.2 Fist Order Integrator Test Method

To validate the design, the inner loop of the DS modulator was tested. The inner loop must perform properly in order for the complete system to work. In order to test the inner loop, the on-chip sensor SC network shown in Figure 5.2 is connected to the interface. By testing the inner loop, the first-order, noise-shaping integrator is validated. The circuitry that is validated includes the correlated double sampling (CDS) switched capacitor integrator, amplifier, quantizer,

and DAC feedback. Initial design measurements indicated that the inner loop was not modulating while Spectre simulations showed that the first-order system should function properly. It was discovered that parasitic capacitance mismatch at the amplifier input would cause the modulator to saturate. Several tests and simulations were performed to correlate this behavior between silicon and simulations. Another important measurement that can be performed with this test structure is to float terminals $+V_{REF}$ and $-V_{REF}$ and include dither for noise shaping. If the noise floor is reduced, it confirms that the voltage fluctuations at the amplifier input cause charge containing thermal noise to be integrated.

One important consideration when using the on-chip, sensor model is the noise present at the amplifier input is not shaped by the first order integrator. The dither and quantization noise are shaped since these noise sources are within the loop.

This test method is the first step in evaluating the system performance. If the integrator is performing as intended, then the complete third order accelerometer architecture can be tested. The next phase in testing would be to tilt the test board on its side and verify that the system can detect one G of constant DC acceleration. If each of the testing milestones is successful, the accelerometer is attached to a shaker table excited by a sinusoidal input signal.

Chapter 6.

EXPERIMENTAL RESULTS

6.1 Initial Design IO Pad Problem

A new layout of the Noise-Shaping Accelerometer Interface Circuit was sent for fabrication due to a MOSIS IO pad layout design problem. This pad design problem had prevented the analog circuitry from being biased appropriately. MOSIS agreed to pay for the fabrication costs of the resubmitted initial design.

The problem arose when using their IO pads in a mixed signal application. Bypassing the tri-state and buffering logic created a lateral zener-type diode that breaks down when reverse-biased at a relatively low voltage. The pad was used to supply the reference current to the current bias circuitry. The desired voltage on the pad was around one NMOS threshold voltage. At this voltage, there is a short from the pad to substrate through the diode preventing any current from being mirrored to the bias current. The pad layout was revised to remove all digital logic, ESD protection, and buffering. This eliminated any risks associated with the pads. However, precautions needed to be taken with the absence of electro-static discharge protection in the pads.

6.2 Reference Feedback DAC and Input VCM

The supply voltage, sgnd1 equal to 1.55V, is the desired input common mode voltage (VCM) of the amplifier. The input nodes of the interface amplifier are VCMN and VCMP shown in Figure 6.1. This voltage is the signal ground of the feedback SC DAC discussed previously in Figure 6.2.

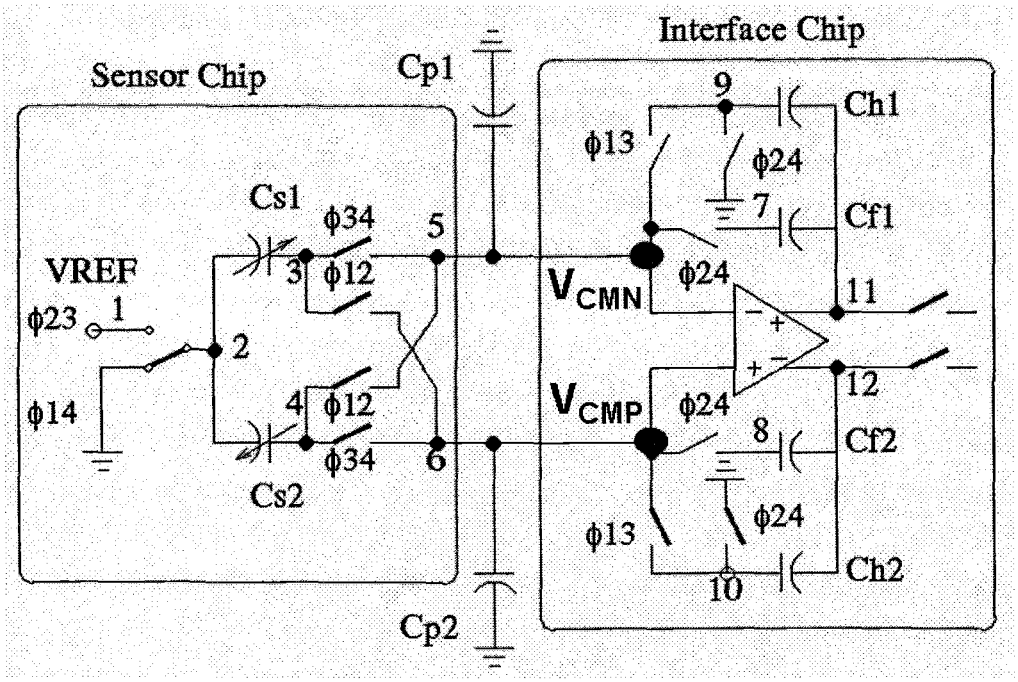

Figure 6.1 Schematic of the switch capacitor, CDS network.

The input common mode voltage is set by the DAC feedback. During clock phase Φ1, sgnd1 is sampled on the top plate of the 100fF, reference capacitor. During clock phase Φ2, this charge is shared with nodes VCMN and VCMP holding the input VCM to sgnd1. This charge will leak due to parasitics resulting in a VCM reduction. If the leakage is too great or the clock rate at which the feedback DAC is charging the VCM is infrequent, the VCM will drop. In implementations of high leakage currents on the VCM, the system clock rate must be increased to help hold the input common mode at the desired voltage.

The input common mode is set only by the feedback DAC. The sampling SC network of the CDS integrator does not set the input common mode. The stationary plate of the sense capacitor is not reset to sgnd1. The DAC reference is applied on Φ2. Therefore, the DAC updates the input CM once every integration cycle or five master clock periods. The input CM voltages were measured with a DC probe on nodes VCMN and VCMP. The measurement results are presented in Table 6.1. For all of the input VCM measurements, reference sgnd1 equals 1.674V. This reference voltage is increased from the desired signal ground of 1.55 to 1.674 in order to compensate for the large amount of leakage current present at the amplifier input. From Table 6.1, the dependence of the master clock, Fs, on VCM is clearly shown. Both of these observations

strongly suggest that there is a significant parasitic leakage path from the interface amplifier inputs. The table, also, indicates a different voltage between the two input nodes. Difference in input CM voltage is the result of parasitic mismatch. In terms of performance, this mismatch will translate into increased gain error, DC offset, and noise. The FFT measurements in this chapter are taken with an Fs equal to 3MHz.

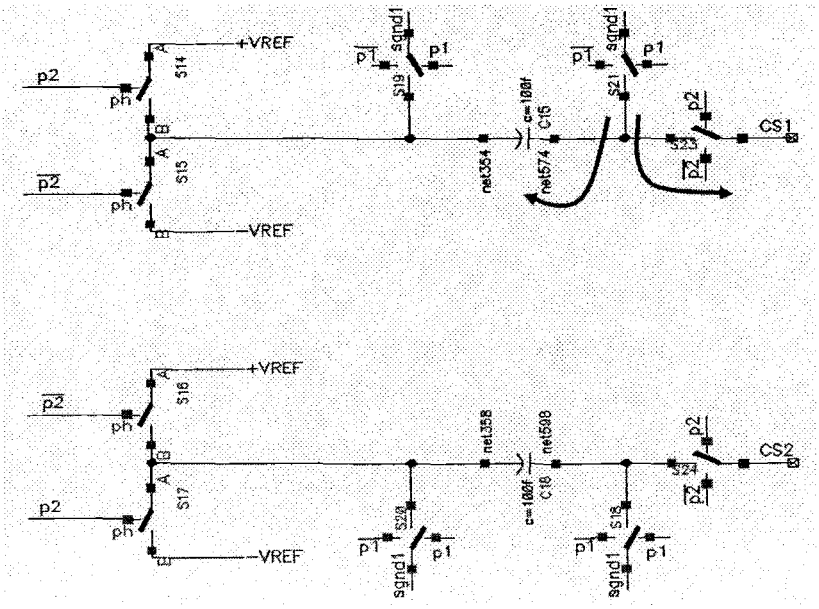

Figure 6.2 DAC schematic implementing the k4 feedback.

Table 6.1 Input CM voltages for various sample frequencies.

Fs	3MHz	1.5MHz	754kHz
FReference	600kHz	300kHz	150kHz
VCMP	1.587V	1.489V	1.265V
VCMN	1.543V	1.452V	1.25V

Using the following capacitor equation for changes in current, the total current leakage can be estimated.

$$I(t) = C \cdot \frac{dV(t)}{dt} \tag{6.1}$$

The C is dominated by the parasitic capacitance. For this discussion, let's assume the parasitic capacitance is 10pF. The change in voltage is estimated to be the adjusted sgnd1 voltage of

1.674V and the measured 1.587V. This assumes the DAC is able to charge VCMN and VCMP to 1.674V and by the end of the integrating cycle, 1.667μs, later the input has discharged to 1.587V. This is a worst case approximation.

$$\frac{dV(t)}{dt} = \frac{V_{sgnd1} - V_{CMP}}{period} = \frac{1.674 - 1.587}{1.667\mu s} = 5.22e4(V/\mu s) \tag{6.2}$$

Estimated worst case current leakage is

$$I(t) = C \cdot \frac{dV(t)}{dt} = 10pF \cdot 5.22e4(V/\mu s) = 522nA \tag{6.3}$$

6.3 First Order Test Structure Performance

Figure 6.3 shows the FFT response for the baseline test setup configuration. The baseline configuration refers to the default settings for the supplies and test structures. The on-chip accelerometer model, sgnd1 equal to 1.674V due to the parasitic leakage, and the maximum possible reference +VREF equal to 3V and –VREF equal to 0V are used and considered default settings. When using the on-chip accelerometer model, the system noise is first order noise shaped at 20dB per decade. With this sgnd1 voltage, the input VCM is near the implemented 1.55V. Dither and internal, parasitic capacitance matching are not used in the baseline configuration. Both modeled sampling capacitors are default. Therefore, no extra capacitance was switched in parallel with one of the sampling capacitors to create a DC signal. Performance FFT measurements were normalized to 0dB with a Hanning window.

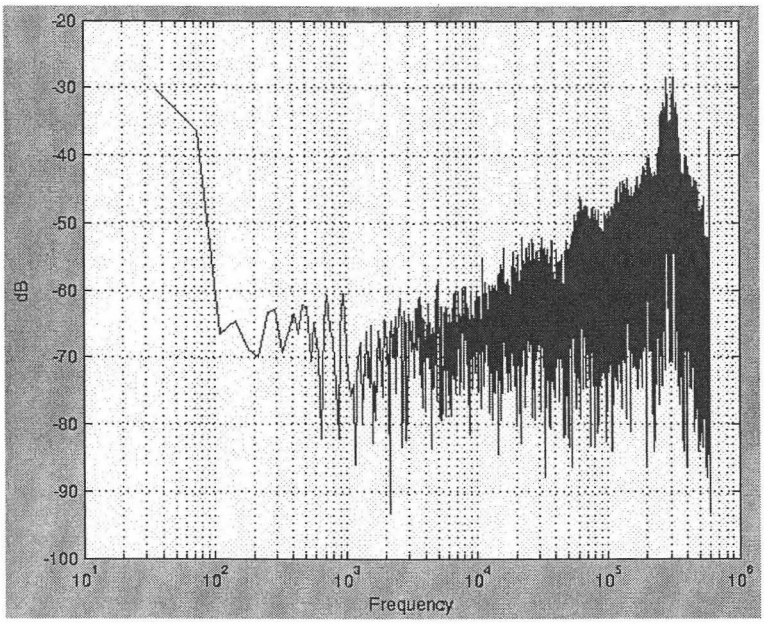

Figure 6.3 Baseline configuration test structure measurement.

This FFT reveals several aspects of the integrator performance. The first is the large DC signal indicating a significant offset in the integrator. The noise floor of the integrator is extremely high which questions the functionality of the integrator. The fact that the noise shaping appears to be around 10dB per decade and not 20dB, also raises the question that integrator is not functioning properly. The best explanation is that the parasitic capacitance mismatch has overloaded the integrator. Recall from the Simulink simulations that the differential reference need was 0.25V. For the measurements presented in this chapter, the reference is set to the maximum possible 6V differential. This is strong evidence that a huge gain error and offset exist in the implementation of the integrator.

The next configuration referred to as parasitic matching had the same setup as the baseline configuration with the following modification. All 3.75pF of the on-chip parasitic matching capacitance available was connected to the negative input of the differential amplifier. This is the input of the amplifier that has the lowest droop, VCMN = 1.543V, as presented in Table 6.1. Figure 6.4 shows the FFT response of the parasitic matching configuration. From the FFT response, you can see a significant improvement in the noise floor and noise shaping of the first order test structure. In Figure 6.5, the improvements are more apparent when comparing the FFTs from the two configurations. This comparison also identifies a small improvement in the

DC offset. From Table 6.2, the VCMP and VCMN difference for both the baseline and parasitic matching configurations are nearly identical with 44mV difference.

Table 6.2 Input CM voltages with capacitor matching.

Fs	3MHz
FReference	600kHz
VCMP	1.5106V
VCMN	1.5554V

By improving the parasitic matching between VCMN and VCMP, it is observed that that the parasitic leakage has not been balanced between the inputs.

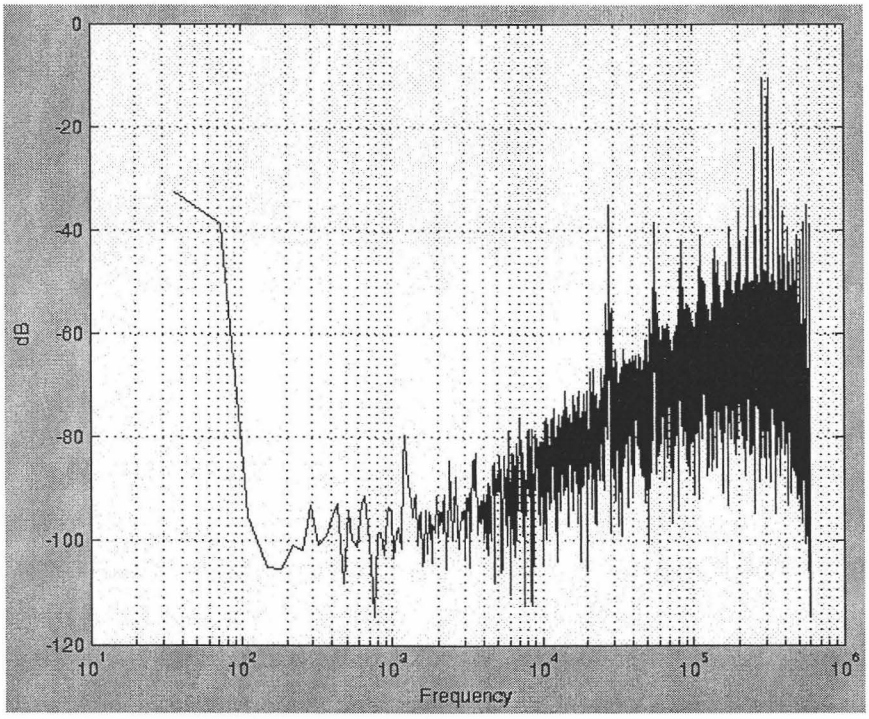

Figure 6.4 Test structure with parasitic matching measurement.

Through the parasitic capacitance, matching, test structure, the performance of the integrator has significantly improved. The noise floor has reduced over 30dB. More importantly, the noise shaping is now 20dB per decade indicating the integrator is function properly. Tones are present in the spectrum. However, this is expected for a first order modulator without dither.

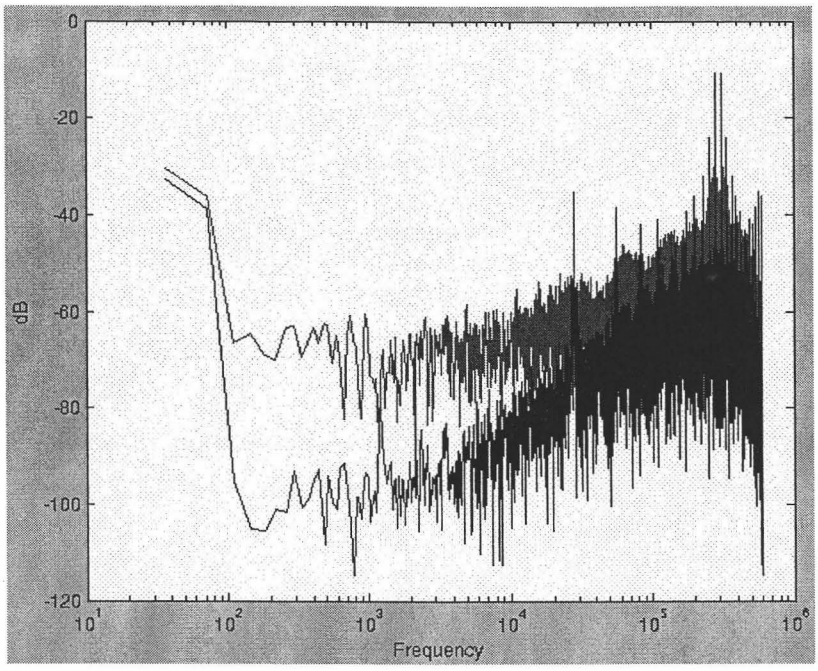

Figure 6.5 Test structure with parasitic matching verse baseline configuration measurement.

Figure 6.5 shows improving the parasitic matching between the amplifier inputs reduces the offset. With the reference set to its maximum possible voltage, it is concluded that a large offset is present in the implementation.

The last investigated test configuration uses the parasitic matching configuration with a few additional modifications. The first modification is that the beam of the accelerometer model is floating. In other words, node 2 in Figure 6.1 is floating. The implementation of this floating node is not to drive the references to V_{REF} and ground. This removes sampled KT/C and amplifier thermal noise on the sampling and parasitic capacitance due to the removal of the voltage pulse at the beam and corresponding fluctuations at the amplifier input. Dither was added to the system in order to create noise to be shaped by the Delta Sigma Modulator. The test board RNG is used which is the same implementation as the on-chip RNG. The dither voltage is grounded. This is the least amount of noise injected into the system possible preventing the system from further overloading. The expected result is confirmed in Figure 6.6. There is a significant improvement in the noise floor of the FFT. Figure 6.7 shows the FFT response comparison of the parasitic matching and this floating beam test configuration. An additional DC offset reduction is observed between the two test configurations. As shown earlier, the VCMP and VCMN difference between the baseline and parasitic matching configurations are nearly identical with a 44mV difference.

The VCMP and VCMN difference for the floating beam configuration is 6mV. This is a considerable reduction in input DC offset. The 6mV difference VCMP and VCMN is presented in Table 6.3.

Table 6.3 Input CM voltages with capacitor matching and floating beam.

Fs	3MHz
FReference	600kHz
VCMP	1.4944V
VCMN	1.4884V

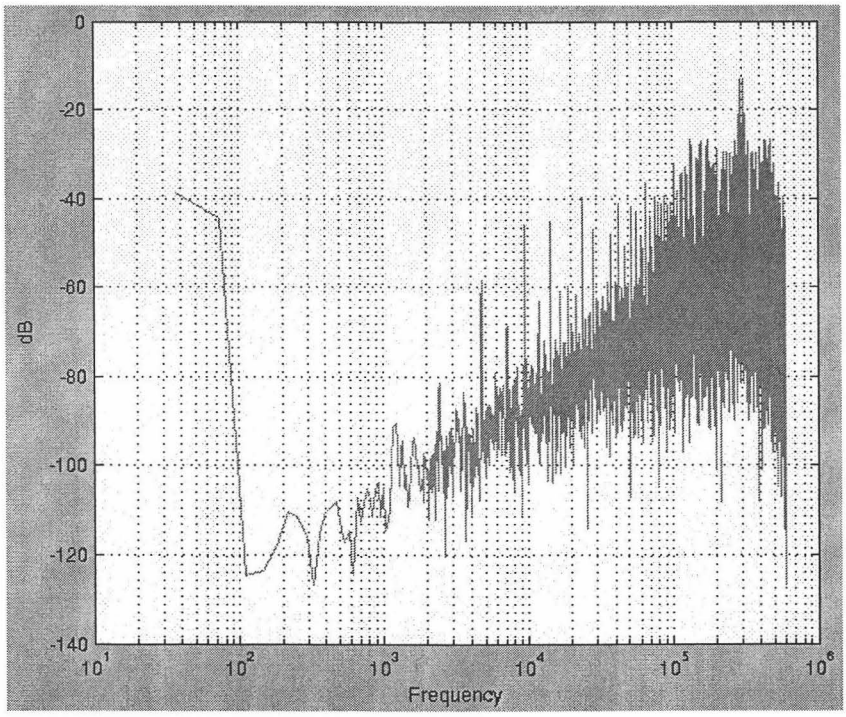

Figure 6.6 Test structure with parasitic matching, floating beam, and dither measurement.

Figure 6.6 shows that the noise floor has been reduced significantly confirming that the voltage fluctuations at the amplifier input does contribute to the noise by integrating sampled KT/C and amplifier thermal noise. Given the resolution of the FFT, the noise floor is not evident. The integrator is functioning properly as shown by the 20dB per decade noise shaping.

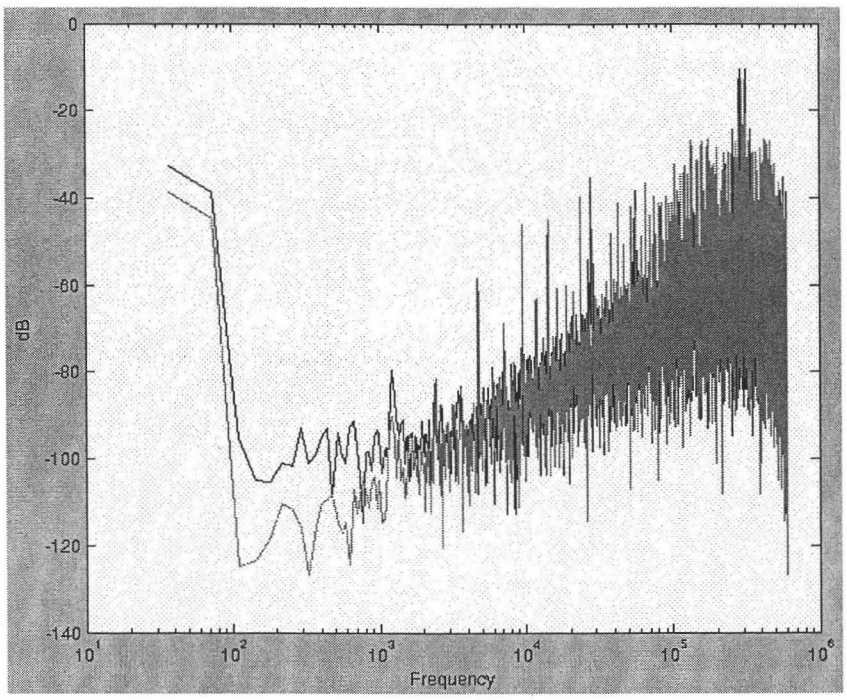

Figure 6.7 Test structure with parasitic matching verse floating beam configuration measurement.

Not only is the noise floor reduced by removing the voltage pulse at the beam, but the offset is also reduced as shown in Figure 6.7.

The complete two-chip system was connected and measured. Again parasitic mismatch was an issue for stability. External capacitors created from twisting wires together to produce small capacitances were needed to compensate for the capacitive mismatch. Once stability is maintained, the one G DC acceleration test was unable to be performed due to the dominating DC offset. With is large offset and the reference being 12 times larger than intended for the architecture, it is impossible to detect accelerations from 1-50Gs whether DC or sinusoidal.

Chapter 7.

CONCLUSION

The desired resolution of the noise-shaping accelerometer interface circuit for two-chip implementation was not achieved. Through the investigation of this research it is shown that the magnitude of the parasitic capacitance and its mismatch between the amplifier inputs has significant negative effects on the integrator. The detrimental effects include instability, a large DC offset and gain error, and increased noise.

The instability due to parasitic capacitance mismatch at the amplifier inputs limits the available applications. Applications with a large interconnect parasitic capacitance will experience more input fluctuations due to a decrease in the feedback factor and therefore, the closed loop gain of the amplifier. Parasitic mismatch trimming circuitry is mandatory for two-chip applications.

Offset and gain error are a result of large parasitic capacitance and amplifier input fluctuations from phase to phase and between the differential inputs. The affect again relates to the magnitude and mismatch of the parasitic capacitance. The offset and gain error was not significantly reduced by matching the parasitic capacitance or removing the large fluctuations from the voltage pulse on the beam. This suggests that the offset is due to interconnect parasitic capacitance and not mismatch or input amplifier fluctuations.

The last significant finding in this investigation is that the integrator architecture does experience more noise due to the presence of parasitic capacitance. This specific application experiences noise from the parasitic capacitance despite following Tetsuya's three suggested rules [17]. Voltage pulses on the beam create amplifier input voltage fluctuations that integrate sampled KT/C and amplifier thermal noise. By removing the input voltage pulses on the beam, the noise floor is significantly reduced

The interconnect parasitics for a two-chip implementation with a surface-machined capacitive sensor are even too much for Tetsuya's CDS integrator architecture. Moving forward, I

believe this integrator has potential in a two-chip implementation with a bulk-machined capacitive sensor. Where the sense capacitors are quite large, reducing the affects of interconnect parasitic capacitance on gain error and noise. Another selling point of this integrator interfaced with bulk sensor is that the interface circuitry can not be integrated on bulk-machined process.

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