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A method and apparatus are presented for generating suppressed carrier digital clock signals. These clock signals have the advantage of being broad band in nature and thus exhibiting lower power spectral density. Structures or systems utilizing such clock signals would be less likely to create electromagnetic noise of sufficient intensity to interfere with radio frequency systems and services.

The apparatus requires only digital logic devices, rather than the analog devices required for frequency- or phase-modulated spread spectrum clock generators. The method provides the opportunity to synchronously demodulate the clock, thus restoring the original narrow band clock signal where required.

The apparatus was implemented in a programmable gate array using 20 MHz and 33.33 MHz fundamental clocks. Measurements of the resulting electronic spectra and clock jitter are reported.

Digital Clocks Based upon Dual Side Band Suppressed Carrier Modulation

by

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1. Introduction

Electronic devices become more reliable and efficient as engineers design them to operate within an appropriate set of environmental conditions. Electromagnetic noise is a significant environmental constraint for many products and systems, and could cause many devices to malfunction unless the levels of man-made electromagnetic noise were controlled. Stray noise can impact communications, navigation, and other critical radio services. Fortunately, there are technologies and standards that enable engineers to reduce the electromagnetic noise generated by their designs. The work described in this thesis is an additional technology - a tool - for controlling the emissions from digital systems into the electromagnetic environment.

1.1 Electromagnetic Interference

Electromagnetic interference (EMI) occurs when radio noise from one electronic system disrupts the function of another system. Many countries have enacted laws that limit the strength of radio emissions from various classes of products. Some companies and military organizations have additional standards. These standards are all directed to achieving the objective defined in the European EMC Directive (European Council, 1989):

> The apparatus ... shall be so constructed that:
> a. the electromagnetic disturbance it generates does not exceed a level allowing radio and telecommunications equipment and other apparatus to operate as intended;
> b. the apparatus has an adequate level of intrinsic immunity to electromagnetic disturbance to enable it to operate as intended.

Interference requires three components: a noise source, a noise receptor, and a coupling path (Ott, 1988). A noise source can be any device that creates electromagnetic fields. A noise receptor is a device that responds to those fields in an unintended manner. The coupling path comes in many forms, and may include signal cables, power cables, or free space. The coupling path determines how much radio power from the noise source will impinge upon the receptor. By eliminating or modifying any of these three components, one can prevent troublesome interference effects. The condition in which interference effects are sufficiently controlled is called Electromagnetic Compatibility, or EMC.

1.2 Radio Systems

Many cases of electromagnetic interference involve radio systems. Radio transmitters intentionally create strong electromagnetic fields, thereby acting as the noise source. A well-known example is the HERO problem, which deals with the Hazards of Electromagnetic Radiation to Ordnance. It is a standard practice on many military ships to keep missiles and explosives away from radar dishes, because the strong radio pulses from such dishes can overload the propellant igniters or explosive initiators.

Radio receivers also are involved in many cases of interference, because they are intentionally designed to respond to radio waves. They can act as noise receptors. A well-publicized example of this arises from the use of personal electronic devices aboard airplanes. Many airlines restrict the types of electronic devices that passengers can use in flight, especially during the approach and departure phases of flight. These restrictions were established because cell phones, electronic toys, and other devices that seem safe can actually interfere with navigational radio systems.

Radio receivers typically contain very selective narrow band filters. For interference to occur, a noise source must emit significant radio power within the input band of the tuned receiver or its intermediate tuner stages.

1.3 High Speed Digital Systems

High speed digital systems are a very common source of electromagnetic noise, and often cause interference to other devices and systems. This happens mainly due to system clocks that are repetitive square wave signals. Interference may also occur on occasion as a result of data interactions, which are synchronous to the system clocks. The characteristics of these clock and data signals that allow them to cause interference are their high frequencies, their high harmonic content, and their narrow bandwidths which may be only a few hundred Hertz wide or less. The high frequency has functional value in that it permits faster data manipulation. The high harmonic content is necessary to provide clean signal edges. The narrow bandwidth is not always necessary; it is present as a result of the crystal oscillators used to generate reliable high frequency timing.

1.4 Spread Spectrum Clocks within Digital Systems

The manner in which a clock signal is used in high speed digital systems can generally be grouped into one of three categories: for direct drive of digital systems; as a frequency reference for phase locked loop (PLL) frequency synthesis; and as a timing reference for PLL synchronized data interchange. Each usage category responds differently to broad band clocks.

A fast digital clock is commonly used to indicate when data is valid on a bus, but sometimes data is simply synchronized to phase-locked loops at the data source and destination. The PLLs are synchronized using a slower clock or intermittent strobe. Narrow band clocks are critical for PLL synchronized data interchange. Systems that use this method include x86-class microprocessors, and the low-voltage differential signaling system (LVDS) used on many flat panel displays. Even the analog color system used in color television relies on PLL synchronized data interchange. Variations in the clock

operation, in the form of cycle-to-cycle jitter or frequency hopping, can cause data loss in such systems.

A clock used as a reference frequency for PLL synthesis can accommodate more jitter and frequency drift, though there are limits at which the synthesis becomes unstable (Hardin et al., 1997). PLL synthesis is used in many microprocessor systems, as well as digitally tuned radio and television sets, to generate a stable, digitally-selectable high frequency signal from a low frequency oscillator.

In the end, almost every digital clock is used to drive logic gates, such as NAND gates, latches and flip-flops. Clocks used to drive circuitry directly can withstand jitter and frequency variation without any difficulty, so long as the design meets the minimum values for clock period, data setup time, and data hold time. These minimum timing values are violated when the high period or the low period of the clock is shortened beyond an acceptable limit.

Spread spectrum clocks reduce interference to radio systems by spreading the electromagnetic emissions across a wider band of frequencies. Narrow bandwidth radio tuners are less likely to experience interference from digital systems using broad band clocks, because their own receiver filters tend to reject most of the noise power. Exchanging a narrow band clock for a spread spectrum clock will not generally decrease the power in an emission; rather, it decreases the power spectral density. This modification to the noise source can resolve many interference problems.

The application of a spread spectrum clock to a circuit or system must be done with an understanding of how that system uses the clock: for direct drive, synthesis, or synchronization. The cycle-to-cycle jitter and frequency drift characteristics of the spread spectrum clock must meet the requirements of the system.

1.5 Existing Spread Spectrum Technologies

Spread spectrum methods are increasingly popular in radio communications. These include methods of digitally double-modulating a radio carrier to improve efficient use of the communication channels. The second digital modulation is done with an encryption key, and several transmitters broadcast into overlapping frequency channels. The various keys used in a channel are mathematically orthogonal so the individual information streams in the channel can be recovered and discriminated.

Digital systems that use spread spectrum clocks for control of electromagnetic interference are not nearly so elegant. There are two basic methods in use: random phase or frequency variations, or controlled frequency modulation (FM).

The random methods are quick, cheap, and dirty: a disturbance signal is injected somewhere within the clock generation circuit. This disturbance signal causes the phase or frequency to shift from the oscillator's steady state conditions. The clock circuit recovers and establishes a new steady state condition. The disturbance signal changes again and again, forcing more recovery processes and steady state conditions. The resulting clock signal has spread spectrum characteristics. A clock with these random variations is called a dithered clock. The signal may also include significant levels of jitter or frequency drift, making these generally useful only for direct drive circuitry.
Due to the random nature of these dithering methods, the clock period may be lengthened or shortened while trying to restore steady state conditions. This can impact the timing margin in the digital design, and so the designer must take this effect into account. The effective clock rate or effective frequency of a signal is the number of low-to-high transitions per second. A circuit designer who uses random dithering must make the effective clock rate low enough so that the minimum timing requirements of the logic gates are not violated during the system's randomized timing variations, as shown in the

upper graph of Figure 1.1. The random variation method is not useful in circuits involving phase locked loops, or in high performance systems where the effective clock frequency must be near the minimum cycle time limit, defined by either the logic gate technology or the overall system design.

The FM method of spread spectrum clock generation is best described in work done by engineers at Lexmark, Inc. Their method uses a narrow band reference clock to create a frequency modulated output clock. The modulation is performed with a patented modulation wave, optimized to result in a flat frequency spectrum over the modulation band (Hardin et al., 1994). The frequency deviation of the fundamental may be set to provide the desired power spectral density. The deviation is multiplied for harmonics, such that higher harmonics have a wider spectral spread.

This FM method tends to work quite well in direct drive systems. With appropriate modulation rates, it works well in frequency synthesis systems, though the PLL loop filter within the synthesis circuit may alter the flatness of the emission spectrum. It is less useful in synchronization applications, though it can provide acceptable results. The major drawback of this method is that it requires phase locked loops, or similar analog devices, to establish low-jitter clocking. This makes the technique difficult to implement on a silicon process which is optimized for high speed digital operation. The effective clock rate depends on the modulation wave shape. Generally, the effective clock rate is set below the maximum permissible clock rate by the amount of the FM deviation, as shown in the middle graph of Figure 1.1.

1.6 A Dual Side Band Supressed Carrier Spread Spectrum Clock

This work presents a different method and system for generating a spread spectrum digital clock based upon dual side band suppressed carrier amplitude modulation, which is useful for most digital clock applications. The system is entirely digital, and is compatible with existing digital technology. The method does not create

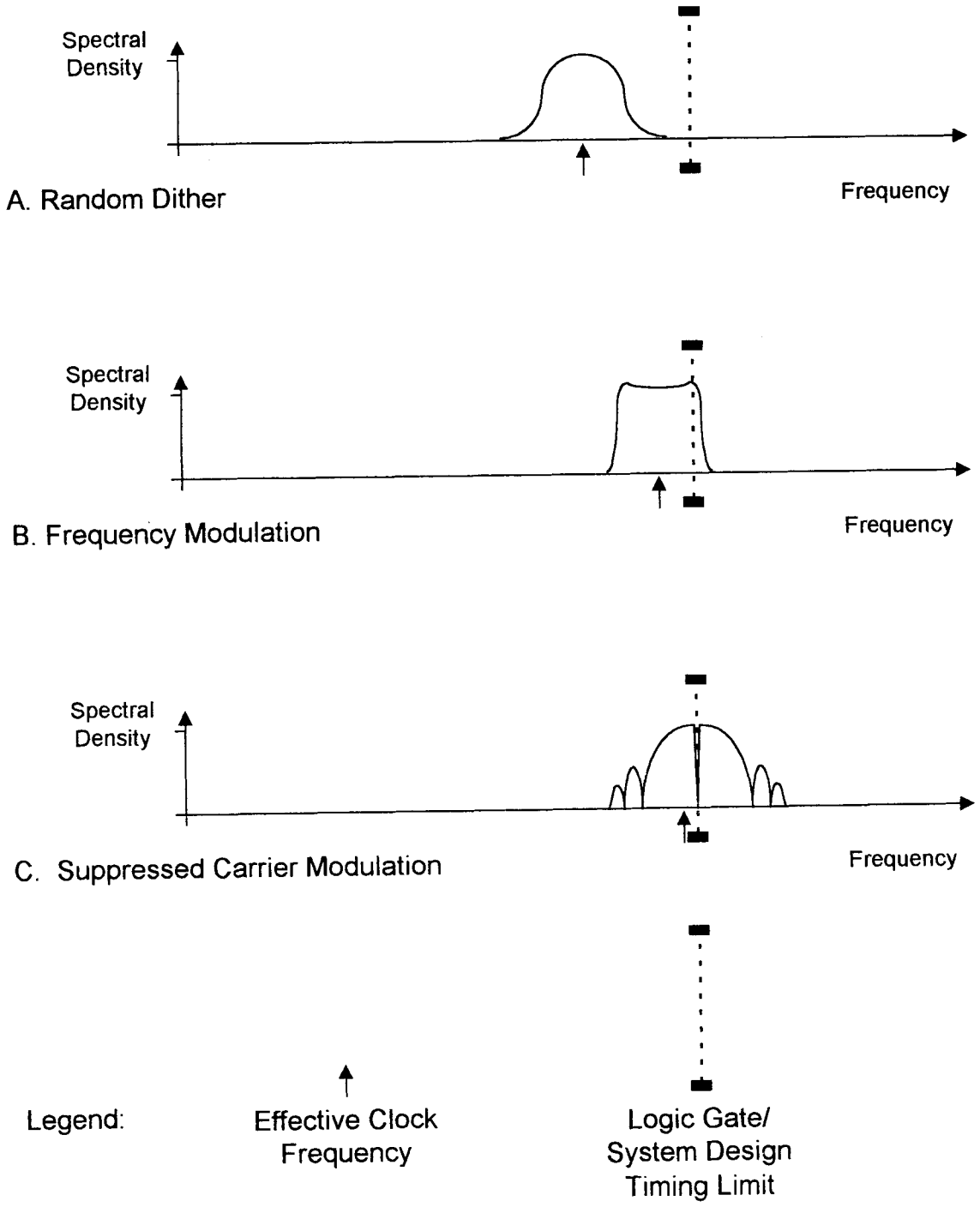


Figure 1.1: Spread Spectrum Technology Comparisons.

random short pulses that might violate minimum timing specifications, but allows the designer to achieve an effective clock rate that is closer to the maximal clock rate of the circuit, as suggested in the lower graph of Figure 1.1.

2. Technology Overview

Existing spread spectrum technologies modulate the phase or frequency of a wave to achieve broadband signal characteristics. The method described here uses amplitude modulation to create a broadband signal. A dual side band suppressed carrier clock can replace the narrow band square wave clock used in digital electronics.

A square wave clock changes between a logical 1 and a logical 0 at regular intervals. One could look at it as a bit pattern: 10101010101010101010101010. In the new scheme, transitions will be omitted from time to time, to make a bit pattern more like this: 10101101010101010010101. This modification to the pattern could be viewed as a phase delay; however, it is more useful to think in terms of repeatedly changing the polarity of the signal.

By changing the polarity of the signal, bits tend to cancel each other in the frequency domain. In fact, the signal energy moves into the side bands commonly discussed in AM modulation theory. The end result is that the modulation pattern - the template which determines how often the bit polarity will be inverted - will completely determine the shape of the side bands. Spectral reductions of greater than 20 decibels are noted in this thesis.

Many digital devices can use this clock as their timing reference. Others can use this clock only when distributing signals across cables or between chassis. This method has the capability of demodulating the signal so that the original square wave clock is recovered at the receiving circuit.

The proposed method uses only logic gates. It does not require the use of analog devices -such as phase locked loops - in digital designs.

3. Theory and Analysis

3.1 Phase Inversion and Spectral Cancellation

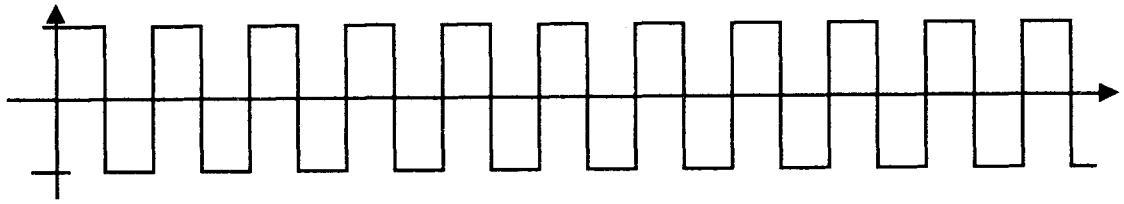
Consider the waves shown in Figure 3.1. The first wave, (a), represents a standard square wave moving between the binary values +1 and -1. The second, (b), is a sinusoidal wave with the same fundamental frequency as the square wave. Fourier analysis of the square wave would show a peak in the frequency spectrum at the frequency of the sinusoidal wave.

The Fourier transformation, $G(\omega)$, of a function, $g(t)$, is generated by comparing $g(t)$ with a sinusoidal wave (or, $e^{-j\omega t}$ in general) at every frequency, ω. The function $g(t)$ and the sinusoidal wave are compared by multiplying them together, and their product is integrated over a time period, such as $-\infty$ to ∞. For any value of ω, the transformed function, $G(\omega)$, will have some value corresponding to the power spectral density of the original function, $g(t)$, at frequency ω.

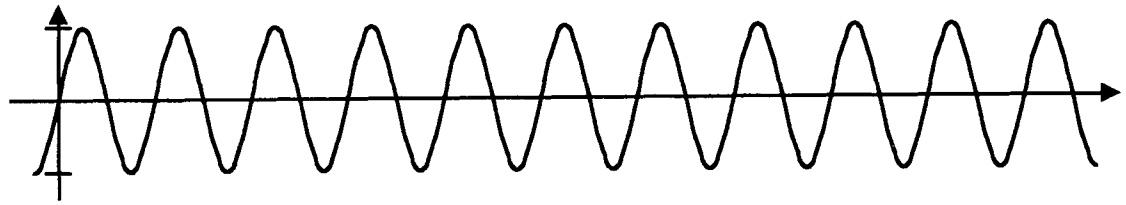
If the first two functions of Figure 3.1 were multiplied, as shown in part (c), the resulting function would always be positive: when the sine wave is positive, the square wave is positive, yielding a positive product; when the square wave is negative, the sine wave is negative, and the result is again positive. Since wave (c) is always positive, its average value of is also positive. The Fourier transform of the square wave has a peak at the frequency of the sinusoidal wave, indicating that the wave has power at the frequency of the sine wave. This power implies a possibility of interfering with a radio receiver tuned to the frequency of the sine wave.

Figure 3.1 includes an ordered set of numbers, (d), representing the square wave as a binary pattern of +1 and -1 values. Figure 3.1 also includes (e), a Fast Fourier Transform of that digital pattern. Only the integer part of the magnitude of the Fast

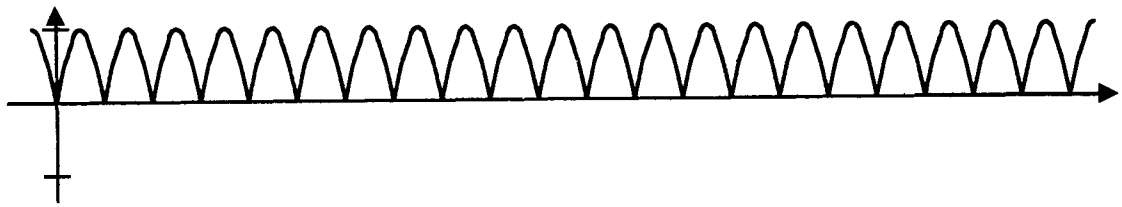
a. Square wave



b. Sine wave



c. Product function



d. Numeric pattern representing the square wave

[+1 -1 +1 -1 +1 -1 +1 -1 +1 -1 +1 -1 +1 -1 +1 -1]

e. Fast Fourier Transform of the numeric square wave pattern

< 0 0 0 0 0 0 0 0 16 0 0 0 0 0 0 0 >

Figure 3.1: Spectral analysis of pure square waves by graphic and numeric processes. Parts a, b, and c demonstrate the graphic process; parts d and e represent the numeric process.

Fourier results will be shown, though the values are often complex numbers. The Fast Fourier Transform identifies repetitions in a signal, and each entry in the transformed number set corresponds to a different repetition rate or frequency. The peak value of 16 located at position 9 in the transformed pattern corresponds to the fundamental frequency of the square wave.

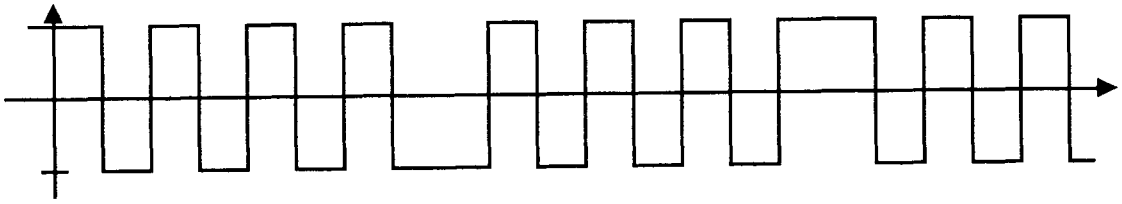
Compare these results to those in Figure 3.2. The first wave, (a), is like the square wave in Figure 3.1, except that the magnitude is inverted every four cycles. This is a suppressed carrier modulated square wave, and its spectral properties form the basis of this work. When the modulated wave, (a), and the sine wave, (b), are multiplied, their product function, (c), is sometimes positive and sometimes negative. The average value of this product function is exactly zero. A Fourier analysis would show no energy peak at the frequency of the sine wave. A radio receiver tuned to the frequency of the sine wave would not experience interference from this square wave.

Figure 3.2 also includes a binary representation of the wave with inversion, (d), and a Fast Fourier Transform of that binary pattern, (e). This transform shows two immediately significant properties. The first is that element 9, corresponding to the frequency of the sine wave, is zero. Note that other elements in the transformed pattern are nonzero, suggesting that the energy in such a wave would be distributed across many frequencies. The second significant property is that the highest value in Figure 3.1(e) was 16, but the peak lowered to a value of 10 in Figure 3.2(e).

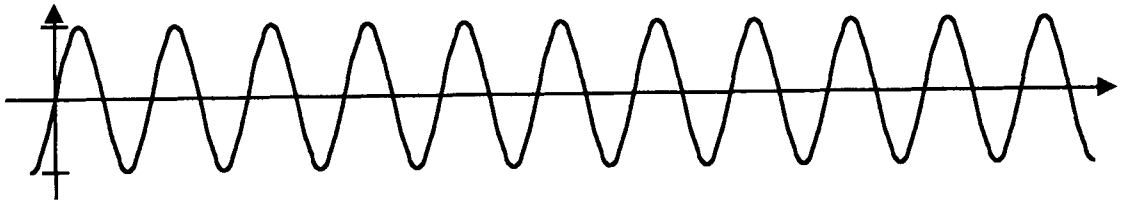
3.2 Suppressed Carrier Modulation

Suppressed carrier modulation can be considered mathematically from several different viewpoints. Starting with a binary pattern **C** which represents a clock or square wave, and a binary modulation pattern **M**, the modulated binary pattern **S** can be generated in either of two equivalent processes.

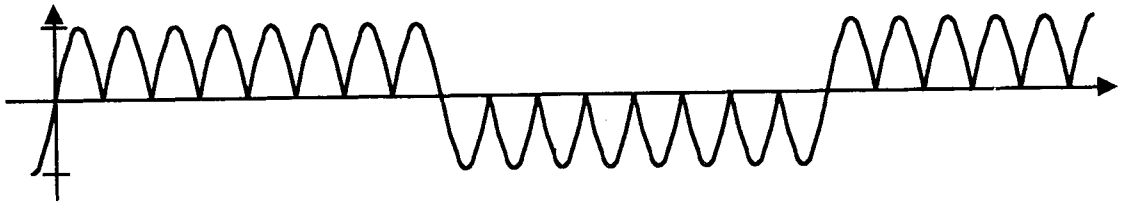
a. Modulated square wave



b. Sine wave



c. Product function



d. Numeric pattern representing the modulated square wave

[+1 -1 +1 -1 +1 -1 +1 -1 -1 +1 -1 +1 -1 +1 -1 +1]

e. Fast Fourier Transform of the numeric modulated square wave pattern

< 0 2 0 2 0 4 0 10 0 10 0 4 0 2 0 2 >

Figure 3.2: Spectral analysis of modulated square waves by graphic and numeric processes. Parts a, b, and c demonstrate the graphic process; parts d and e represent the numeric process.

The first process is an element-by-element multiplication process:

$$\mathbf{S}_j = A\,\mathbf{C}_j\,\mathbf{M}_j + B \quad \text{for } j = 1 \text{ to } n \qquad \text{Eq. 3.1}$$

$$\mathbf{C}_j \in \{ -1 +1 \}$$

$$\mathbf{M}_j \in \{ -1 +1 \}$$

Where **C**, **M** and **S** are binary patterns of length n. The scalar constants A and B are selected so that $\mathbf{S}_j$ maps into the same binary space as $\mathbf{C}_j$ and $\mathbf{M}_j$. For binary values in the set {-1 +1}, A = ±1 and B = 0.

Equation 3.1 defines an amplitude modulation process. Standard amplitude modulation is based upon the equation

$$f(t) = A \sin(2\pi f_c t)\,[1 + m(t)] \qquad \text{Eq. 3.2}$$

$$-1 < m(t) < 1$$

where f(t) is the modulated signal, f_c is the carrier frequency, and m(t) is the modulation signal. Since the quantity [1 + m(t)] is assured to be positive, there is always some spectral energy at the frequency f_c.

Suppressed carrier amplitude modulation, by contrast, has little or no energy at the carrier frequency f_c. It is based upon the equation

$$f(t) = A \sin(2\pi f_c t)\, m(t) \qquad \text{Eq. 3.3}$$

This modulation is similar to that described in Equation 3.1. The relationship exists more clearly between Equation 3.1 and Equation 3.3 when: **C** is the binary pattern of a square wave with a fundamental frequency fc; the variable A in Equation 3.3 takes the value one, with A and B in equation 3.1 set to +1 and 0 respectively; and **M** is a binary-valued substitute for m(t).

The second equivalent process for generating the modulated pattern **S** from **C** and **M** is to represent the patterns as logical values and perform a bit-by-bit exclusive-OR operation. The mapping of the logical space (0 1) into the binary space {-1 +1} is not unique. For mathematical purposes in this chapter, the logical state 0 will map to the

binary value +1, and the logical state 1 will map to the binary value -1. The mapping will be different in later chapters of this thesis, to better suit the mappings commonly used in electrical engineering. Once a mapping relationship is established, any binary-valued pattern **P** will uniquely map to a logical pattern P, and vice versa.

Let the binary patterns **S**, **C**, and **M** map into the logical patterns S, C, and M. The process of Equation 3.1 may be equivalently written as

$$S_j = C_j \oplus M_j \quad \text{for } j = 1 \text{ to } n \qquad \text{Eq. 3.4}$$

Table 3.1 demonstrates how **C**, **M**, **S**, C, M, and S relate under these mappings and modulation processes. Suppressed carrier modulation can be implemented in a binary system by using Equation 3.1, or in a logical system by using Equation 3.4. Binary patterns in brackets [], and logical patterns in braces {} will be used interchangeably in the remainder of this text.

Table 3.1: Binary Patterns and Logical Patterns.

Binary Patterns		Logical Patterns	
C	[-1 +1 -1 +1 -1 +1]	C	{1 0 1 0 1 0}
M	[-1 -1 +1 +1 -1 +1]	M	{1 1 0 0 1 0}
$\mathbf{S_j = C_j M_j}$	[+1 -1 -1 +1 +1 +1]	$S_j = C_j \oplus M_j$	{0 1 1 0 0 0}

3.3 Side Bands from Narrow Band Suppressed Carrier Modulation

Analog communication theory predicts that an amplitude modulation process will produce side bands equally spaced above and below the carrier frequency. The side bands are related in frequency and amplitude to the carrier frequency and the spectral content of the modulation signal. The Fast Fourier Transform pattern of Figure 3.2e showed spectral content equally spaced above and below position 9 in the pattern, where position 9 corresponded to the carrier frequency before modulation. This suggests that the side bands predicted in analog communication theory also appear as a result of the digital processes detailed above in Section 3.2.

3.4 Simulation and Analysis of Side Bands

This prediction is tested by analysis of several 32-element modulation patterns. In all cases, the carrier *C* is composed of alternating logic states { 0 1 0 1 0 1 ... 0 1 0 1 }. The Fast Fourier Transform of the binary modulation signal **M** is shown as Fm, and that of the binary modulated signal **S** is shown as Fs. As before, the Fast Fourier results will be shown in angled brackets <>, and only the integer portion of the magnitude will be shown. The transformations will be performed on binary patterns, as before, though logical patterns will be shown. This work was carried out using the Fast Fourier Transform, vector, and list manipulation functions of the HP48G calculator. The Reverse Polish LISP programs and algorithms are detailed in Appendix A.

For reference, the first system analyzed will be an unmodulated signal.

M = {0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 . 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0} Eq. 3.5a

Fm = <32 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 . 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0> Eq. 3.5b

S = {0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 . 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1} Eq. 3.5c

Fs = <0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 . 32 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0> Eq. 3.5d

The initial value of 32 in Fm indicates that the average value of **M** is not zero. The reader will recall that each binary value $\mathbf{M}_j$ is +1 for all j, because of the mapping between logic and binary spaces defined previously. Thus, Equation 3.5b is not the Fast Fourrier Transform of Equation 3.5a. Logical *M* is converted to binary **M**, and then transformed, and then magnitudes of the transformed values are rounded to the nearest integer for simpler presentation. Fs shows that the peak of 32 occurs at position 17, corresponding to the fundamental frequency of the carrier **C**.

The second system to be considered uses a square wave modulation signal of one-sixteenth the carrier frequency:

M = {0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 . 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1} Eq. 3.6a

Fm = <0 20 0 7 0 4 0 3 0 3 0 2 0 2 0 2 . 0 2 0 2 0 2 0 3 0 3 0 4 0 7 0 20> Eq. 3.6b

S = {0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 . 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0} Eq. 3.6c

Fs = <0 2 0 2 0 2 0 3 0 3 0 4 0 7 0 20 . 0 20 0 7 0 4 0 3 0 3 0 2 0 2 0 2> Eq. 3.6d

The first half of Fm shows a peak value in position 2, with decreasing values in even-numbered positions. This corresponds to a low frequency square wave and its decreasing spectral content at even-multiple harmonics. The second half of Fm is a reversal of the first half. This is a spectral wrap-around effect of the Fast Fourier Transform.

The first half of Fs is a reverse image of the first half of Fm, and the second half of Fs is a copy of the first half of Fm. These are the upper and lower side bands expected from modulation theory. As expected, the value at position 17 of Fs is zero. This indicates a suppressed carrier modulated square wave.

The next system to be analyzed uses a square wave modulation signal at one-quarter of the carrier frequency:

M = {0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 . 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1} Eq. 3.7a

Fm = <0 0 0 0 21 0 0 0 0 0 0 0 9 0 0 0 . 0 0 0 0 9 0 0 0 0 0 0 0 21 0 0 0> Eq. 3.7b

S = {0 1 0 1 1 0 1 0 0 1 0 1 1 0 1 0 . 0 1 0 1 1 0 1 0 0 1 0 1 1 0 1 0} Eq. 3.7c

Fs = <0 0 0 0 9 0 0 0 0 0 0 0 21 0 0 0 . 0 0 0 0 21 0 0 0 0 0 0 0 9 0 0 0> Eq. 3.7d

As in Equation 3.6, Fm shows harmonics of a square wave in the first half of the spectrum, which are repeated as upper and lower side bands in Fs.

It is useful to note the locations of the side bands between Fs in Equation 3.6 and Fs in Equation 3.7. In Equation 3.6, the largest elements are in positions 16 and 18. In Equation 3.7, the magnitudes of these largest elements have changed little, but they have been relocated to positions 13 and 21. A slower modulation signal can compact the side bands more closely together without necessarily changing the side band magnitude.

Another feature to note at this point is the total number of 0 to 1 or 1 to 0 transitions in S, compared to those in M and C. The effective clock rate or effective

frequency of a signal is the number of low-to-high transitions per second. Careful comparison will show that the number of transitions in S plus the number in M will equal the number in C. This arises because each transition in the modulation signal creates a phase inversion at the same time the carrier phase was expected to change. Therefore S has fewer transitions than C, and the difference is directly attributed to M. For application of this technique to the clocks of digital systems, that trade-off between the number of edges in the modulation signal and the resulting effective clock rate (as measured by the number of transitions in S) will become a major design consideration.

The next few systems will have random modulation signals.

$M = \{1001\ 1100\ 0011\ 0110.1011\ 1000\ 0001\ 1110\}$ Eq. 3.8a

Fm = <0 1 8 4 11 3 4 6 2 2 6 2 8 4 6 3 . 4 3 6 4 8 2 6 2 2 6 4 3 11 4 8 1> Eq. 3.8b

$S = \{1100\ 1001\ 0110\ 0011.1110\ 1101\ 0100\ 1011\}$ Eq. 3.8c

Fs = <4 3 6 4 8 2 6 2 2 6 4 3 11 4 8 1 . 0 1 8 4 11 3 4 6 2 2 6 2 8 4 6 3> Eq. 3.8d

Again, the number pattern in the first half of Fm is repeated as side bands in Fs. The peaks in Fm, and therefore in Fs, were lower with this randomly generated modulation signal. However, the number of transitions in M was large, resulting in a lower effective clock rate in S.

Equations 3.9 and 3.10 will examine the effect of doubling each entry in the previous random modulating signal, M. The first half of M from Equation 3.8 will be used in Equation 3.9, and the second half will be used in Equation 3.10.

$M = \{1100\ 0011\ 1111\ 0000.0000\ 1111\ 0011\ 1100\}$ Eq. 3.9a

Fm = <0 4 11 10 0 9 9 3 0 3 6 5 0 3 2 0 . 0 0 2 3 0 5 6 3 0 3 9 9 0 10 11 4> Eq. 3.9b

$S = \{1001\ 0110\ 1010\ 0101.0101\ 1010\ 0110\ 1001\}$ Eq. 3.9c

Fs = <0 0 2 3 0 5 6 3 0 3 9 9 0 10 11 4 . 0 4 11 10 0 9 9 3 0 3 6 5 0 3 2 0> Eq. 3.9d

M = {1 1 0 0 1 1 1 1 1 1 0 0 0 0 0 0 . 0 0 0 0 0 0 1 1 1 1 1 1 1 0 0} Eq. 3.10a

Fm = <0 12 13 5 5 2 4 7 6 6 3 1 2 2 2 1 . 0 1 2 2 2 1 3 6 6 7 4 2 5 5 13 12> Eq. 3.10b

S = {1 0 0 1 1 0 1 0 1 0 0 1 0 1 0 1 . 0 1 0 1 0 1 1 0 1 0 1 0 1 0 0 1} Eq. 3.10c

Fs = <0 1 2 2 2 1 3 6 6 7 4 2 5 5 13 12 . 0 12 13 5 5 2 4 7 6 6 3 1 2 2 2 1> Eq. 3.10d

The peak in Equation 3.8 was a value of 11. The peaks in Equations 3.9 and 3.10 were 11 and 13 respectively. The effective clock rate improved from a value of 9 cycles in Equation 3.8 to values of 12 cycles and 13 cycles in the later equations. In some cases, the effective clock rate can be increased without a significant impact on peak noise levels.

By comparison, the peak values found using square wave modulation in Equations 3.6 and 3.7 were relatively constant, with values of 20 and 21. The effective clock rates were quite different, with rates of 15 cycles in Equation 3.6 and 12 cycles in Equation 3.7. Again, effective clock rate and peak emission levels can be somewhat independent. However, the randomly modulated signals seem to have much lower peak spectral values that the square-wave modulated signals.

3.5 Prediction of Side Band Peak Frequencies and Intensities

The foregoing analysis suggests that the side band characteristics predicted by AM modulation theory will apply directly in the analysis of the spectra that result when two digital waves are modulated through an exclusive-OR operation. The basic analysis for side band peak locations arises by replacing m(t) in Equation 3.3 with a sine wave:

$$f(t) = A \sin(2\pi f_c t) \sin(2\pi f_m t) \quad \text{Eq. 3.11}$$

$$f(t) = 0.5\ A \{ \sin[2\pi (f_c + f_m) t] + \sin[2\pi (f_c - f_m) t] \} \quad \text{Eq. 3.12}$$

Two peaks of equal amplitude result, located at frequencies that are the sum and difference of the initial frequencies. A few clarifications are necessary when predicting the digital suppressed carrier modulation results, to account for the fact that the modulation occurs in logic space.

If the modulating signal is not a sine wave, it will be composed of a spectrum of frequencies. When the sine wave of Equation 3.11 is replaced with a series expansion of m(t), the spectrally-rich nature of side bands becomes apparent:

$$m(t) = \Sigma_j B_j \sin(2\pi f_j t + \phi_j) \qquad \text{Eq. 3.13}$$

$$f(t) = A \sin(2\pi f_c t) \Sigma_j B_j \sin(2\pi f_j t + \phi_j) \qquad \text{Eq. 3.14}$$

$$f(t) = 0.5A \Sigma_j B_j \{ \sin[2\pi(f_c + f_j)t+\phi_j] + \sin[2\pi(f_c - f_j)t-\phi_j] \} \qquad \text{Eq. 3.15}$$

where Σ_j denotes summation over j, B_j and ϕ_j are constants, and the f_j are the constituent frequencies which make up m(t).

In the present case, the carrier wave is not a sine wave, either. It is a square wave, c(t), which is composed of a harmonic spectrum of signals. The modulation process and harmonic products are defined by the following equations.

$$f(t) = c(t)\, m(t) \qquad \text{Eq. 3.16}$$

$$c(t) = \Sigma_k A_k \sin(2\pi k f_c t) \qquad \text{Eq. 3.17}$$

$$f(t) = \Sigma_k A_k \sin(2\pi k f_c t) \Sigma_j B_j \sin(2\pi f_j t + \phi_j) \qquad \text{Eq. 3.18}$$

$$f(t) = 0.5 \Sigma_k \Sigma_j A_k B_j \{ \sin [2\pi (k f_c + f_j) t +\phi_j] + \sin [2\pi (k f_c - f_j) t - \phi_j] \} \qquad \text{Eq. 3.19}$$

This is a long way of saying that the shape of the side bands will match the shape of the modulating signal in relative frequency and relative amplitude. However, the shape of the side band becomes more complicated as the side bands of adjacent harmonics begin to overlap.

When predicting the actual spectral content at a given frequency, one must account for the possibility that two modulation products may contribute to a single peak, and that contribution may be constructive or destructive based upon phase angle. For example, a first signal with spectral content at 20 kHz and 40 kHz is modulated with a second signal having spectral content at 5 kHz and 15 kHz. The spectral content at 25 kHz would include the modulation contribution from (20 kHz + 5 kHz) and the contribution from (40

kHz - 15 kHz). Similarly, the spectral content at 35 kHz would include content from the (20 kHz + 15 kHz) and (40 kHz - 5 kHz) modulation products.

3.6 Demodulation

When demodulation is discussed in the realm of communication theory, it is presented with the goal of recovering the modulation signal. Synchronous demodulation of an analog suppressed carrier signal is accomplished through a process of: (1) replicating or retrieving the original carrier signal; (2) modulating the suppressed carrier signal, f(t), with the replicated carrier, to produce g(t); and (3) passing g(t) through a low-pass filter to recover m(t), the modulation signal. Mathematically,

$$g(t) = D \sin(2\pi f_c t) f(t) \qquad \text{Eq. 3.20}$$

Recalling Equation 3.3 which generated the modulated signal,

$$f(t) = A \sin(2\pi f_c t) m(t) \qquad \text{(Eq. 3.3)}$$

it is clear from Equation 3.20 that

$$g(t) = A D \sin(2\pi f_c t) \sin(2\pi f_c t) m(t) \qquad \text{Eq. 3.21}$$

$$g(t) = 0.5 A D [m(t) - \cos(4\pi f_c t) m(t)] \qquad \text{Eq. 3.22}$$

from which m(t) can be retrieved using a low-pass filter. These equations assume there is no phase error introduced, or that the replicated carrier is phase locked to the original carrier. If there is time or phase delay introduced in the transmission of the suppressed carrier signal from modulator to demodulator, the same delays must be present in the replicated carrier.

In the present context where the carrier or clock is the significant signal and the modulation is of little functional value, there is great value in demodulating the suppressed carrier signal to retrieve the clock. This could be accomplished using a second exclusive OR gate and an exact copy of the logical modulation pattern *M*. Recalling Equation 3.4,

$$Sj = Cj \oplus Mj \quad \text{for } j = 1 \text{ to } n \qquad \text{(Eq. 3.4)}$$

this demodulation would create a pattern *T*, such that

$$T_j = S_j \oplus M_j$$
$$= C_j \oplus M_j \oplus M_j$$
$$= C_j \qquad \text{for } j = 1 \text{ to } n \qquad \text{Eq. 3.23}$$

In this manner, demodulation recovers the original clock signal. As with analog synchronous demodulation of suppressed carrier signals, the time delays introduced in transmission from the modulator to the demodulator must be present in the modulated signal and the modulating signal equally.

3.7 Application and Summary

The objective of a spread spectrum technology is to reduce the electromagnetic interference attributable to high speed electronic systems while creating minimal degradation to the performance of the systems. This chapter proposes and predicts that the peak spectral density in a clock signal can be reduced through use of suppressed carrier amplitude modulation. Significant points from this analysis include:

A. This modulation may be achieved in a logic system using the XOR logic gate function.

B. The original clock may be recovered by routing the modulating signal and the modulated signal to an XOR gate demodulator.

C. The side bands of the modulated wave will take the spectral shape of the modulation signal.

D. The effective clock rate after modulation will decrease as the edge rate of the modulating signal increases.

E. Decreasing the modulation wave frequency has the effect of compacting the side bands of the modulated signal. This compaction can improve the effective clock rate of the modulated signal with only a small impact upon peak spectral density.

F. Modulation with complex or random waves will produce lower peaks in the modulated signal spectrum.

There are practical limits to how compact the modulation spectrum can be. Power spectral density is measured with a device having a finite input bandwidth. Most devices that are susceptible to electromagnetic interference are susceptible over a small bandwidth. Any adjacent peaks in the modulation signal will be added together if they are separated by less than the critical input bandwidth of the measuring equipment or the susceptible device. International standards require the electromagnetic radiation from digital devices at frequencies below 1 GHz to be measured with a 120 kHz input bandwidth (IEC, 1993).

Assuming that adjacent peaks do not fall within the critical bandwidth, discrete spectral analysis predicts that a narrow band modulation signal applied to a square wave voltage clock could reduce the emissions from a relative linear level of 32 to a level of 20. A broad band modulation signal could decrease the emissions further – to a level of 11, for example.

4. Circuit Implementation

4.1 A Simple Modulator - Demodulator Pair

Figure 4.1 shows a simple modulator and synchronous demodulator, as suggested by the discussion of the previous chapter:

$$Sj = Cj \oplus Mj \quad \text{for } j = 1 \text{ to } n \qquad \text{(Eq. 3.4)}$$

The modulator would be located at a source circuit or system, and the demodulator would be located at the destination circuit. The traces or cables that connect the two circuits would not carry any narrow band signals. This feature tends to reduce the peak spectral emissions from the circuit or cable that would otherwise carry a narrow band clock.

In practice, this circuit would not perform well in a high speed digital system. The first problem lies in the nature of the exclusive-OR gate. If the Input Clock changes its logical state when the Modulating Signal changes state, the Modulated Clock may glitch. The glitch is a normal result when both inputs change at the same time, or at nearly the same time. In transition between input values of 11 and 00, the output should remain 0. In practice, the logic may attempt to output a transient value of 1, which is the proper result of a 01 or 10 input pattern. Thus the output of the XOR gate would start at $1 \oplus 1 = 0$, begin a transition to an intermediate state such as $1 \oplus 0 = 1$, and then revert to the desired $0 \oplus 0 = 0$ condition. A similar glitch could occur in the Output Clock signal if the Input Clock is stable when the Modulating Signal changes state. The Modulated Clock would change logical states, but its change would involve a time delay relative to the Modulation Signal. The Output Clock would change state in response to the Modulation Signal, and then change back due to the delayed transition of the Modulated Clock.

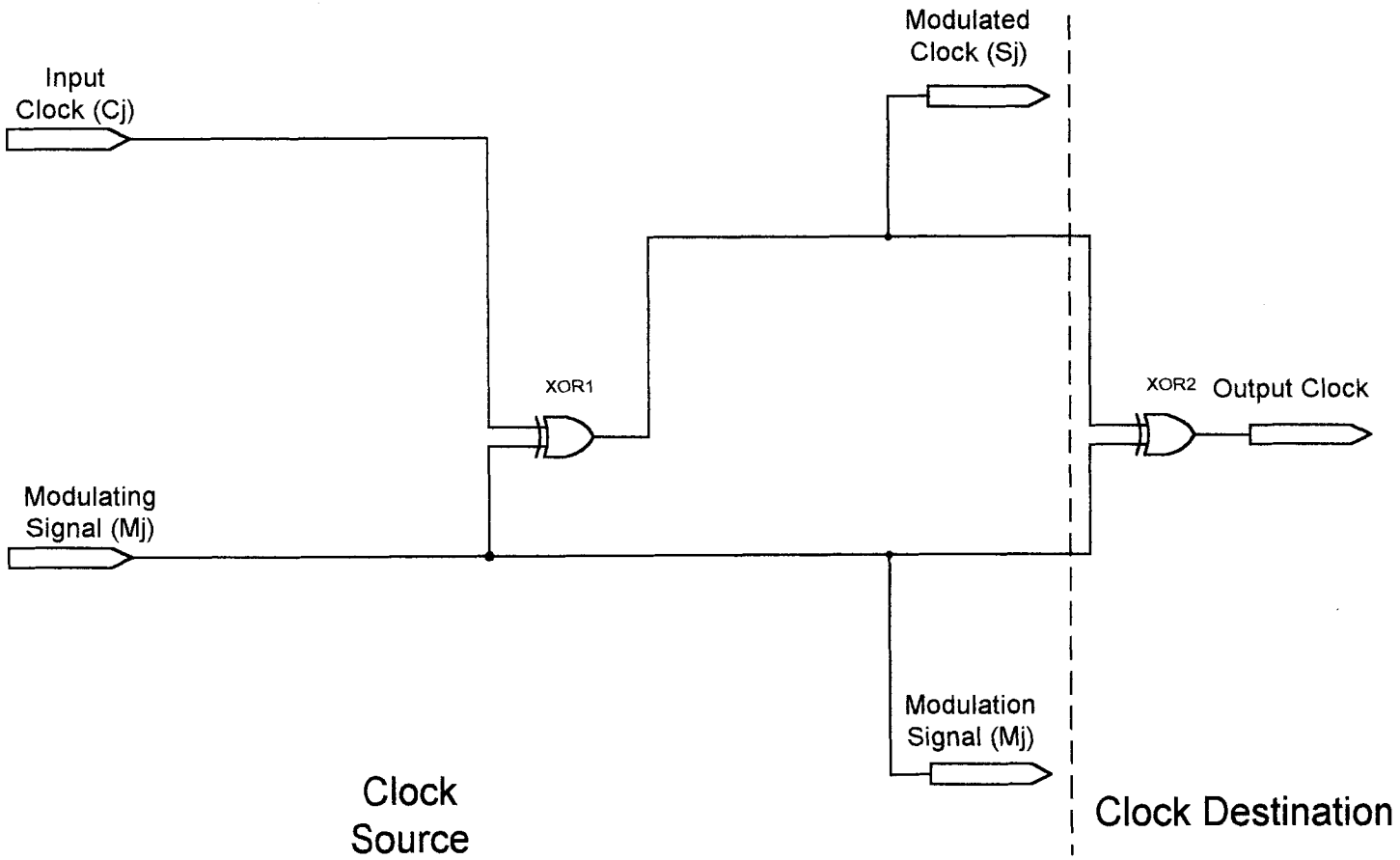


Figure 4.1: A simple modulator-demodulator pair.

To avoid such glitches, the circuitry surrounding an XOR gate should be arranged such that either (1) only one input switches at a time, or (2) glitches in the output are functionally acceptable.

A second problem with the simple circuit of Figure 4.1 is that the Input Clock and Modulating Signal are not necessarily synchronous. Their timing transitions could be separated by arbitrarily short intervals, leading to a condition where the Modulated Clock could have pulses of very short duration. These pulses would probably violate the minimum low or high periods of logic gates attached to the Modulated Clock line, including XOR2.

4.2 A Better Modulator - Demodulator Pair

These issues are addressed by the circuit design of Figure 4.2. Within the system architecture, the final XOR gate would be located at the destination circuit, and the remainder of the circuit elements would be located at the source circuit.

This design requires a reference clock (Clock x2) operating at twice the desired output clock frequency. Flip-flop 1 is arranged as a divide-by-two counter, to create the Input Clock for the modulator. This Input Clock changes state on the rising edge of Clock x2. Modulating Signal I is latched by a flip-flop to create Modulating Signal II, which also changes state on the rising edge of Clock x2. The XOR1 gate receives these two signals as input, and so the output of XOR1 will have glitches only at the rising edge of Clock x2.

A second stage of latches is clocked on the falling edge of Clock x2. At the falling edge of Clock x2, Modulating Signal II and the output of the first XOR gate are both stable. The Modulated Clock and Modulation Signal will both transition in sync with the falling edge of Clock x2.

Figure 4.3 is a timing diagram of the circuit in Figure 4.2. As this figure shows, either the Modulated Clock or the Modulation Signal will change on every falling edge

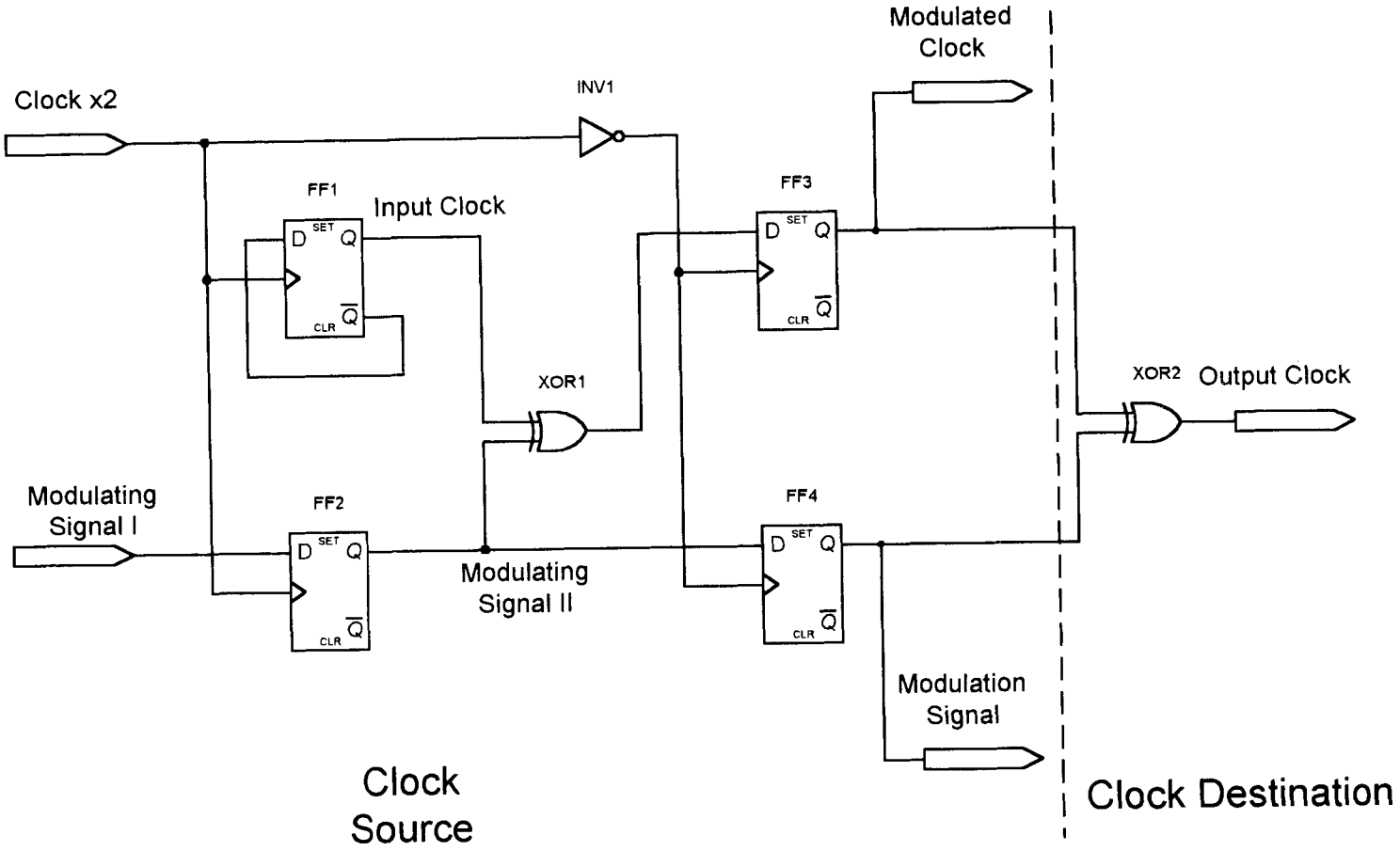


Figure 4.2: A buffered modulator-demodulator pair.

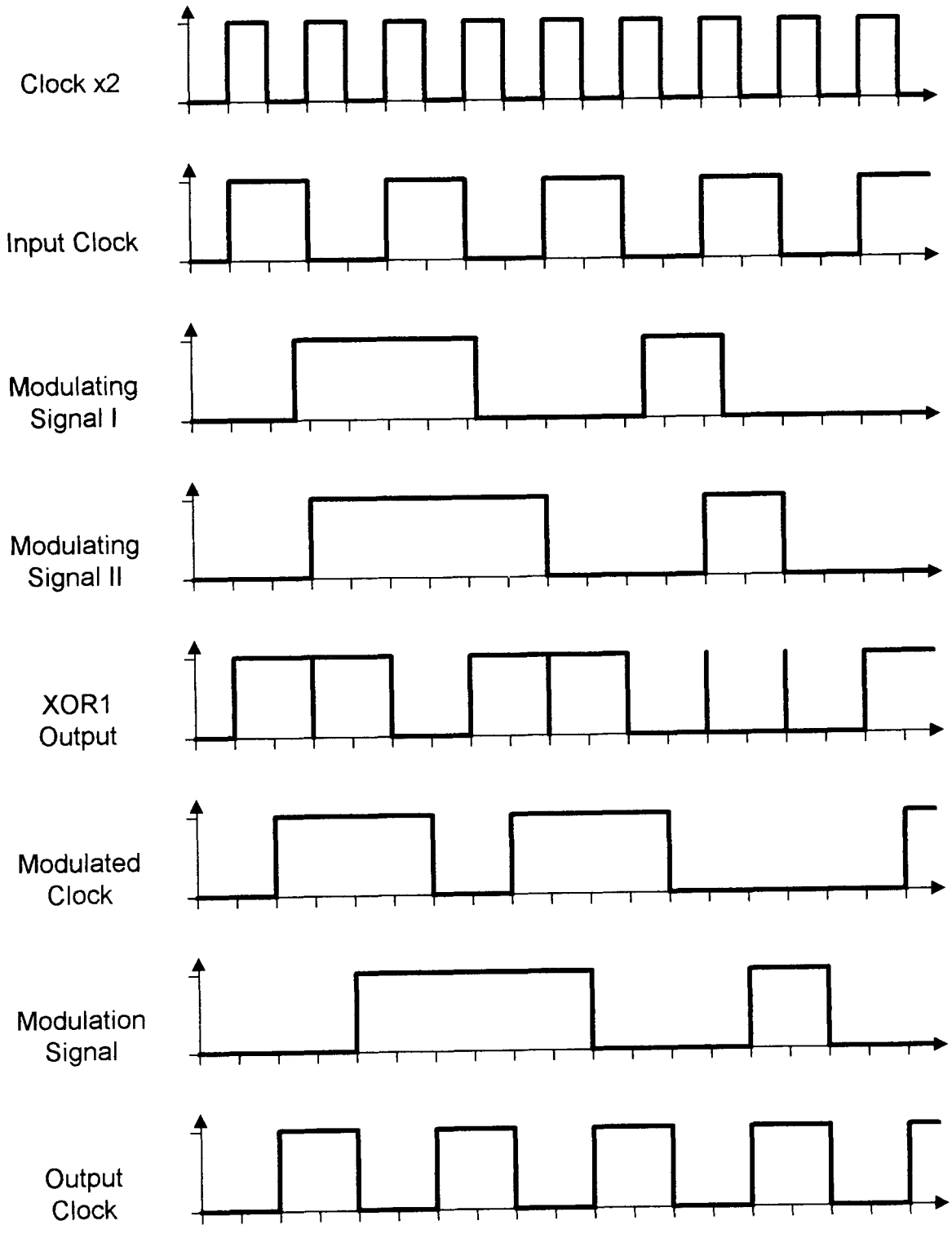


Figure 4.3: Timing Diagram.

of Clock x2, but never will both change at the same time. The Output Clock will not suffer from glitches. Note that the Output Clock is synchronous with the falling edge of Clock x2, not the Input Clock. This is an important design consideration.

4.3 Backward Compatibility

The modulator and the demodulator would typically be included in separate integrated circuits or system modules. The question arises how this method might be used on a standardized or generic device when other parts of the system may not be fully designed for suppressed carrier modulation.

If the modulator circuit or module were to drive a destination circuit incapable of utilizing a modulated clock, the Modulating Signal I input would simply be grounded. The output of the modulator will be a stable, unmodulated clock.

Suppose the destination system is built to accommodate a modulated clock, but a source module is chosen that does not include the modulator. Simply ground the Modulation Signal input at the destination circuit. In this way, the unmodulated clock will be received and utilized appropriately.

With these options in mind, the modulator and demodulator could be implemented in existing systems for use when connected to an appropriate mating circuit. Systems with these circuits added are backward compatible with narrow band systems.

4.4 A Stand-Alone Modulator

The circuit design of Figure 4.2 is sufficient to transmit a narrow band clock from one circuit or system to another without routing any narrow band signals across circuit boards or through cables. However, there are many direct-drive circuits that will operate effectively from a broad band clock having the characteristics described in Chapter 1. Specifically, the clock must meet the minimal high, low, setup, and hold requirements specified for logic gates. A state machine is an example of a direct drive circuit that can

operate on a clock that occasionally provides a longer clock phase than typical. A modulated clock can be used to drive such circuits without providing a demodulator.

The circuit of Figure 4.4 is appropriate for such a direct-drive circuit. The only changes are removal of the demodulating XOR gate, and the flip-flop used to create the Modulation Signal.

4.5 Modulation Sources

The design of broad-spectrum noise sources is related to, but distinct from, the present subject matter. The theory of suppressed carrier clock modulation predicts that the measured emission levels from a device using suppressed carrier clocks will depend heavily upon the modulating spectrum. The implication is that a spectrally broad modulation source may be desirable.

Every real suppressed carrier clock modulator must have such a noise source, including those that are to be used in the next chapter of this work, and so the topic will be discussed briefly at this point.

The simplest modulation waveform is a square wave with a frequency set below the input clock frequency, perhaps using a divide-by-n counter from the input clock. Such waveforms were used in the previous chapter (refer to Equation 3.7). A more complex waveform would be a random signal approximating white noise.

Another useful waveform is the pseudo-random pattern. It has good spectral smoothness, yet the hardware implementation of the pattern generator is simple and straightforward. The details of this pattern generator will not be covered in this present text. In future chapters, references to the pseudo-random signal will mention an order number (defining the size of the state machine used to generate the signal) and the effective clock rate (which is the average number of low-to-high transitions per second).

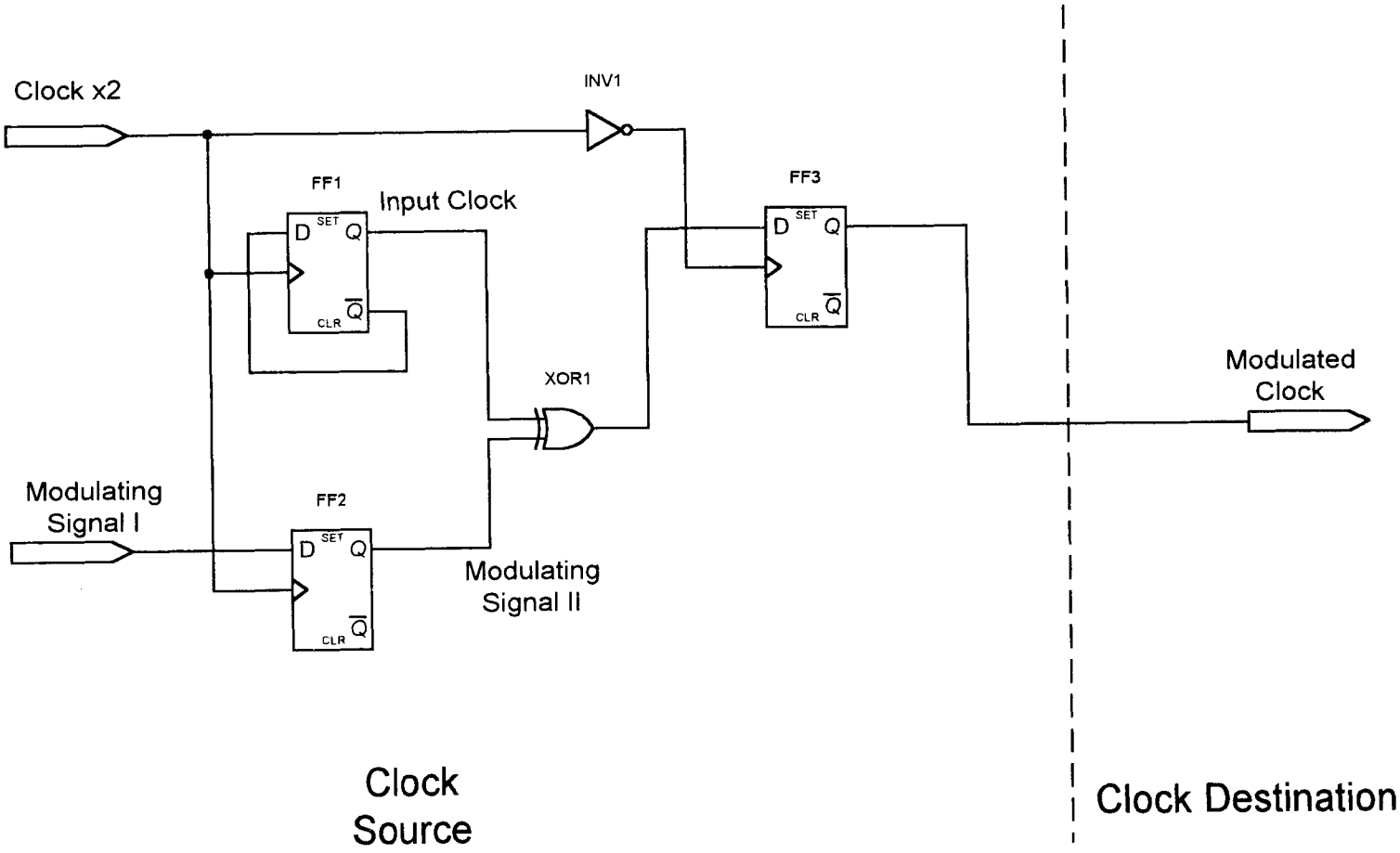


Figure 4.4: A stand-alone buffered modulator.

4.6 Construction

The suppressed carrier clock generator was assembled using a piece of 1.5 mm thick fiberglass circuit board plated on one side with copper, as shown in Figures 4.5 and 4.6. Traces and land patterns in the copper were created by carving out unwanted metal with a hobby knife, due to budget and schedule. Most interconnections are made with narrow gauge wire. The circuit includes a 5V power supply, a number of single-pole single-throw switches in Dual Inline Package (DIP) arrays, a connector for the serial programming interface, and a programmable gate array containing all the logic circuits. The circuit board was mounted inside a sheet metal box on half-inch standoffs. Four terminals are provided on the side of the box for accessing 5V power and ground rails, plus the two output signals (Modulated Clock and Modulation Signal). A hole in the end of the box permits insertion of the 12 V power input, as shown in Figure 4.7.

The gate array used is an Altera EPM7064S-7ES, which contains 64 macrocells, and has a maximum operational speed well above 140 MHz. A gate array macrocell can be thought of as a flip-flop with support gates. The output of each macrocell can be connected to the input nodes of other macrocells. This gate array can be reprogrammed in place using a serial interface from a computer. The array is in a 44-pin J-lead package.

The design has only five high-speed signals external to the gate array: 66.66 MHz and 40.00 MHz primary clocks, a Modulated Clock output, a Modulation Signal output, and a demodulated clock output. The primary clocks originate from crystal oscillators soldered on the circuit board, and attached to the gate array using narrow gauge wire. The outputs are routed on the non-plated side of the board using copper tape with an adhesive backing.

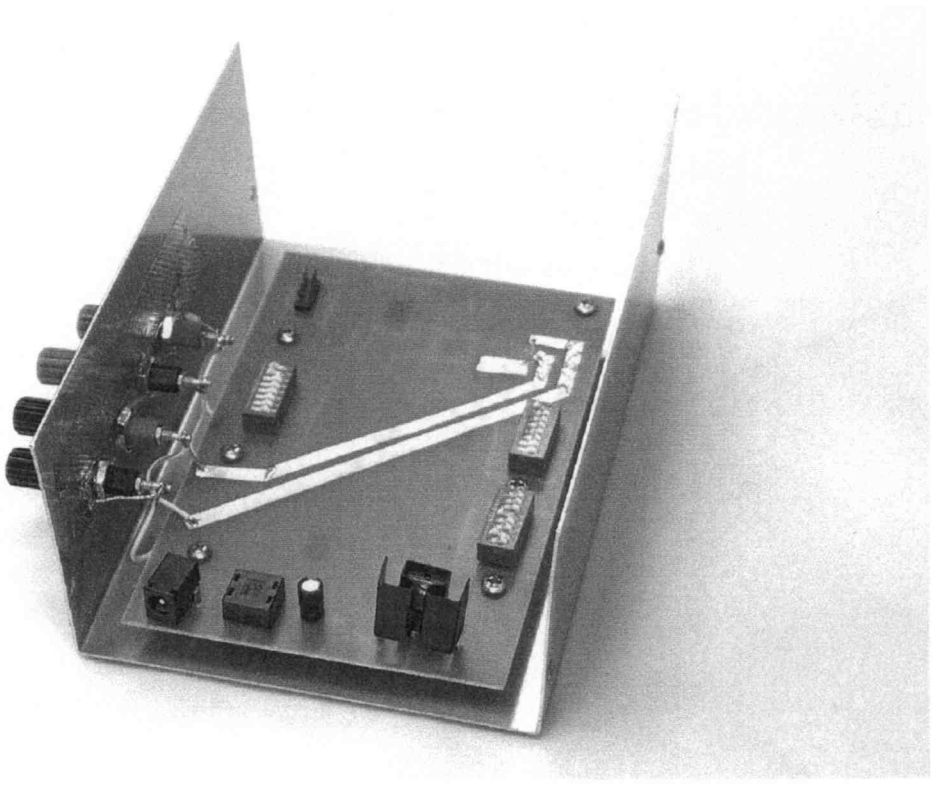


Figure 4.5: Top side of circuit board.

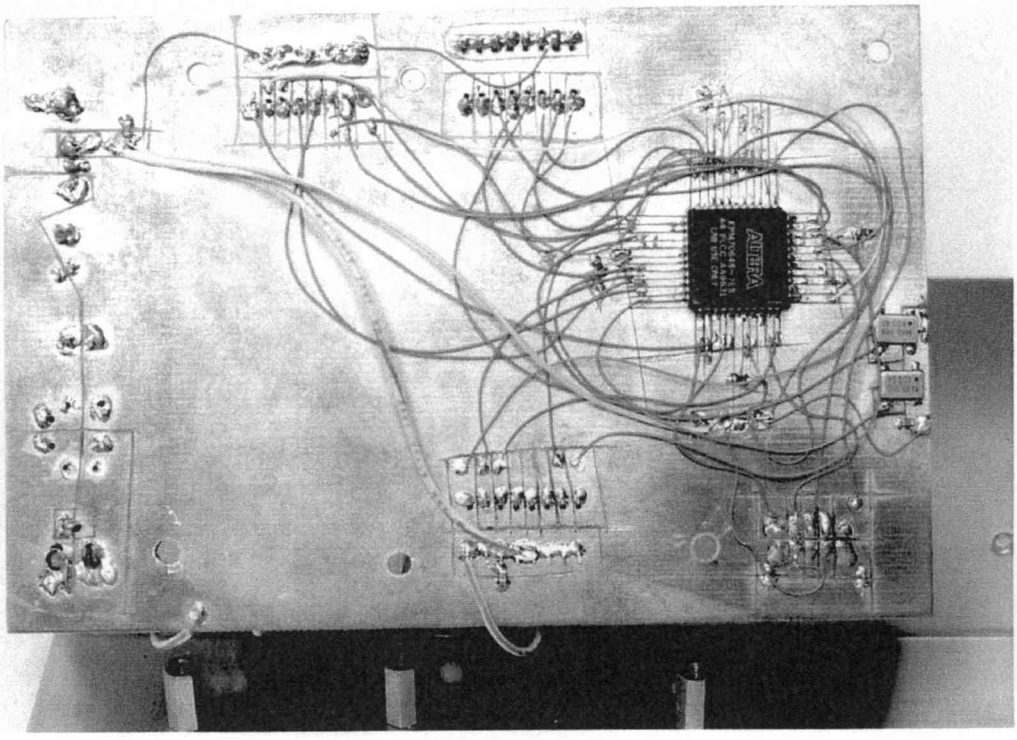


Figure 4.6: Bottom side of circuit board.

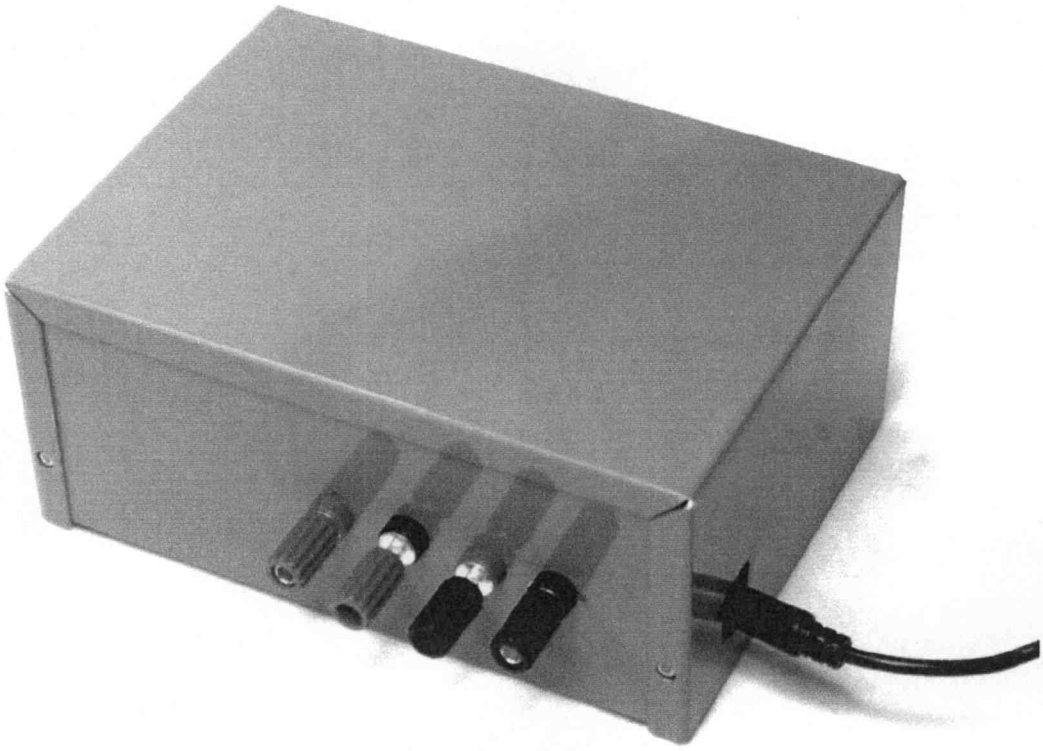


Figure 4.7: External view of test assembly.

The characteristic impedance of a microstrip structure can be approximated using Equations 4.1 and 4.2 (Pozar, 1990). The fiberglass thickness, d, is 1.5 mm. Its relative permittivity, ε_r, is 4.

$$\varepsilon_e = (\varepsilon_r + 1)/2 + [(\varepsilon_r - 1)/2\sqrt{(1 + 12d/W)}] \quad \text{Eq. 4.1}$$

$$Zo = 120\pi / \sqrt{(\varepsilon_e)}\,[W/d + 1.393 + 0.667 \ln(W/d + 1.444)] \quad \text{Eq. 4.2}$$

In the original arrangement this tape width, W, was approximately 4 mm, and contained no filter or termination elements. This would make the trace characteristic impedance about 45Ω. At a later stage of the measurement process, the trace width was narrowed to about 0.75 mm, as shown in Figure 4.8. This change produced a characteristic impedance near 100Ω.

There are, in fact, two demodulators in the system. The first demodulator receives the Modulated Clock and Modulation Signal before they exit the gate array. Its output is provided as a means of verifying that the system is running correctly. This demodulator was present throughout testing, and was referred to as Demod. At a later stage of the experimental work, when the trace impedances were increased to 100Ω, additional circuitry was provided to return the signals to gate array inputs and then demodulate the signals, resulting in the Xclk signal.

The Modulated Clock and Modulation Signals ran from the gate array outputs through 100Ω microstrip transmission lines to the terminal posts. The power and ground connections previously provided at these posts were removed. The signals were connected to a five-inch length of 300Ω television antenna twin-lead. After the twin-lead, the signals were routed back across the circuit board to the gate array, at the inputs of the second demodulator. The output of this second demodulator is called Xclk, because it demodulates signals that have been routed external to the gate array and circuit board. Measurements on Xclk permitted evaluation of the effects of signal filtering.

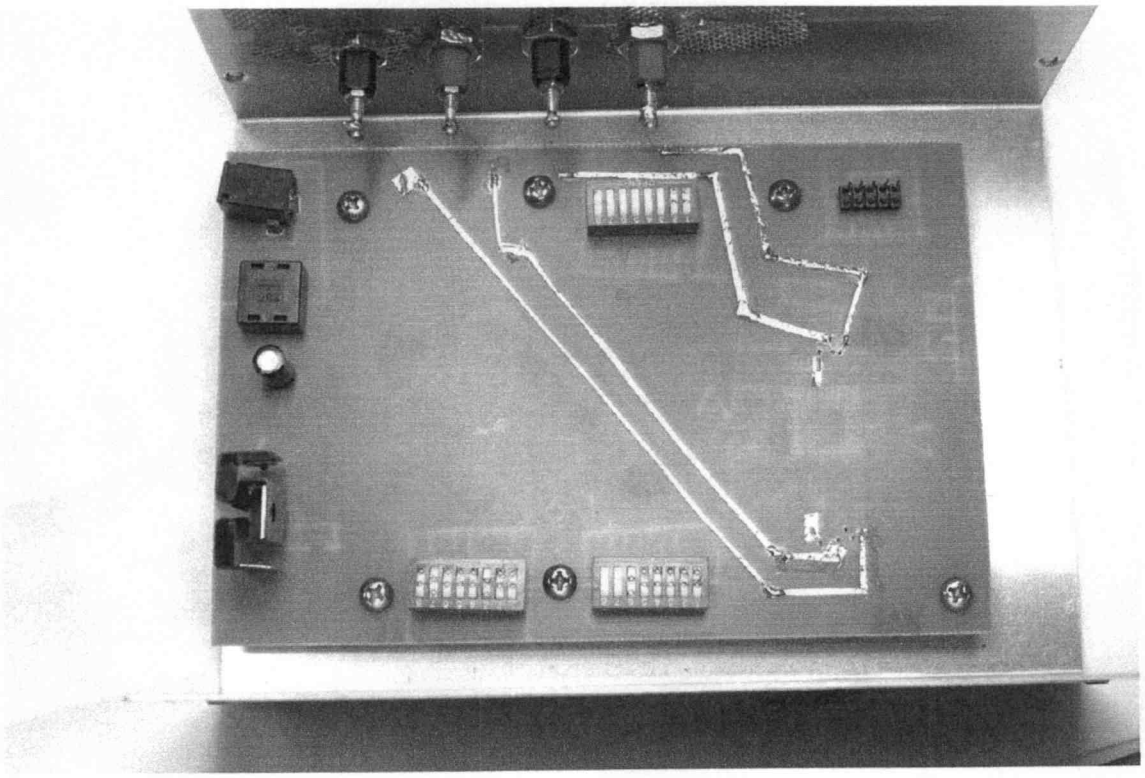


Figure 4.8: Circuit board with redesigned transmission lines.

Signal flow within the gate array is controlled using a number of digital inputs, set using the DIP switches. These are DC signals, and are routed with narrow gauge wire. The function of each switch is discussed in further detail in Appendix C.

The serial programming interface is also attached in one corner of the board. During normal circuit operation, these programming signals are idle.

The power supply is designed for quick assembly and quiet operation, rather than efficiency. The AC to DC converter is an HP F1044B AC adapter which converts power from the building mains to regulated 12V DC. This DC current enters the circuit board through a mating connector, and passes through a common mode choke to a 47 μF filter capacitor. The 12V power is converted to 5V using a 7805 voltage regulator chip set in an appropriate heat sink. This 5V power is supplied to the various elements of the system, with 0.1 μF decoupling capacitors added at the power input terminals of most devices on the board, and to the power terminal on the side of the box.

5. Measurement Configurations

Before providing the experimental data, it may be useful to describe the equipment used for various measurements.

5.1 Bench Top Spectral Measurements

The spectral content of a signal is linearly related to the far-field radio measurement used in most EMC testing, but predicting the scaling factor is a difficult task. That factor includes the effects of the spatial relationship between the measurement antenna and the electronics device creating the radio emissions. The measured strength of a radio emission will also depend upon the radiation efficiency of the mechanical structures that make up the source device. Measurement of the relative amplitudes in a signal spectrum on a laboratory bench is a convenient technique for evaluating variations in signal content, which will have a direct effect on far-field radio emissions.

During spectral measurements made on the laboratory bench, the clock generator is assembled as described in Chapter 4, except that the cover of the metal box is removed to permit frequency measurements. Spectral measurements are made at the terminal lugs outside the box, unless stated otherwise.

Measurement equipment includes an HP8594EM Spectrum Analyzer, an HP85024A High Frequency Probe with an HP11881A 10:1 Divider tip in place, and an XY Plotter controlled by the Spectrum Analyzer through an HPIB channel.

Spectrum analyzer measurements are made using a 120 kHz IF Bandwidth, as is typically used in regulatory emissions testing. Where possible, this bandwidth is also used when measuring spectra at frequencies below the lower regulatory limit of 30 MHz. The

analyzer readings are presented in dBμV without any additional calibration factors included to account for the response of the high frequency probe.

The frequency response of the probe and tip are assumed to be fairly flat over the measurement range. Most of the comparisons in the data analysis will involve comparing data at a single frequency or nearby frequencies from two different experiments. Therefore, the relative magnitudes of the various signals can be compared, and probe calibration effects will cancel out in the comparison. These probe calibration effects, if any, are small compared to the larger issues of antenna orientation and the radiating structure efficiency which must be considered in relating bench top tests to radiated field measurements.

The original measurements contain data measured with the peak detector and with the quasi-peak detector of the spectrum analyzer. For stable, narrow band spectral peaks, the two detectors will produce the same value. When measuring signals in which the in-band power level varies faster than 10 kHz, the Quasi-Peak detector will register more like an Average detector. Unless stated otherwise, spectral measurements discussed in this thesis are peak detector values and are equivalent to quasi-peak readings within 0.3 dB.

5.2 Effective Frequency Measurements

The effective clock rate or effective frequency of a signal is the number of low-to-high transitions per second. This parameter is important in understanding how a modulation technique will affect the operational throughput of a digital system that is directly driven by a modulated clock. This parameter is irrelevant in discussing the operation of systems using demodulated clocks.

The equipment set used to determine the effective clock edge rates of digital signals includes a Universal Counter, and a 10:1 voltage probe. The universal counter, often called a frequency counter, is adjusted to read a stable value of the effective frequency.

5.3 Clock Parameter Measurements

Hewlett-Packard makes a Time Interval Analyzer, the HP E1725A. This device makes very fast measurements of timing signals, and will report various characteristics of a clock signal, such a cycle-to-cycle jitter, or minimum and maximum pulse widths. The test device uses standard 1 MΩ 10:1 voltage probes as would be used on an oscilloscope. It has a graphic interface, based upon a windowed operating system, for control of the high-speed instrument. This instrument was used to measure jitter.

6. Experimental Results

6.1 Experimental Approach

The objectives of these experiments are: (1) to verify that the spectra generated by the modulator fit the theory presented in Chapter 3, especially the specific points detailed in Section 3.7; (2) to measure the timing parameters of digital clocks generated or distributed by the techniques described herein; and (3) to note, investigate, and characterize anomalous or unexpected results.

6.2 Baseline Clock Spectra

Before attempting to measure or discuss the complex spectra of modulated clocks, it is reasonable to present and discuss a few baseline spectra. The baseline spectra are an unmodulated 20 MHz clock, and unmodulated 33.33 MHz clock, and a signal held at the low logic level. The measurements of the unmodulated clocks will serve as a standard of comparison for determining how much noise reduction can be achieved with modulation. The data from the signal held low will indicate the noise levels measured by the test setup that come from sources other than the signals under study.

These initial measurements are made from 0 Hz to 100 MHz. This range is deemed sufficient to capture the expected effects without losing detail.

The 20 MHz clock is shown in Figure 6.1. This figure shows the electrical power present in the signal measured, as a function of frequency. The horizontal scale is the frequency axis. In this case, the frequency runs from 0 Hz (DC) to 100 MHz. The vertical scale is signal amplitude, measured on a logarithmic scale. The top line is 107 dBμV, and each division is a 10 dB separation. Four harmonics peaks were measured. The readings appear in Table 6.1.

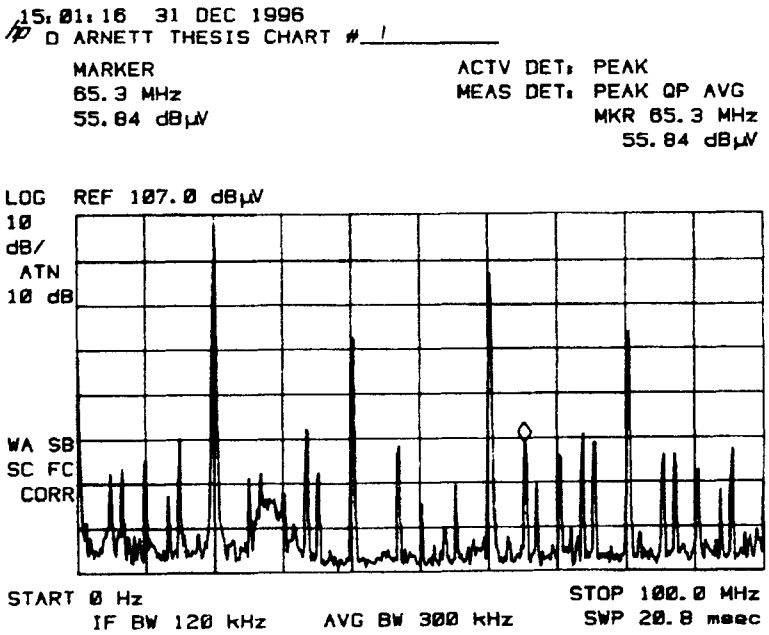


Figure 6.1: 20 MHz Baseline.

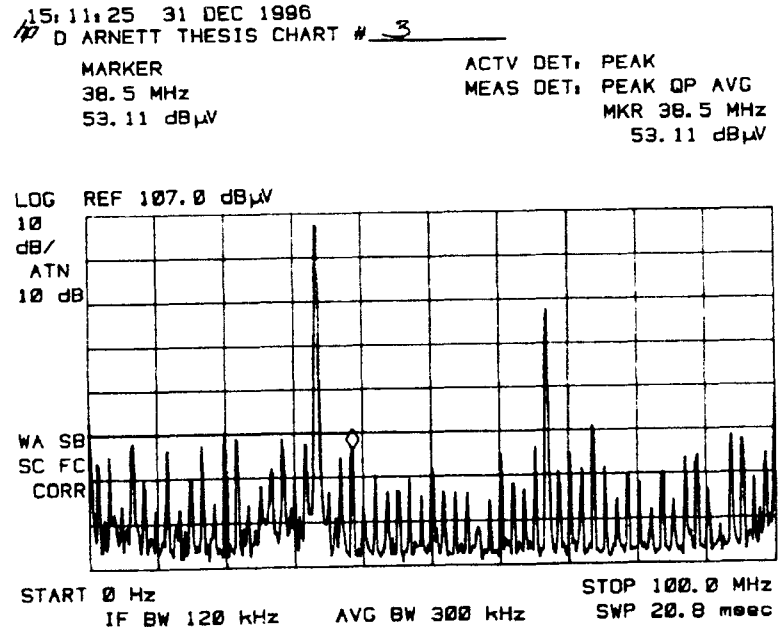


Figure 6.2: 33.33 MHz Baseline.

Table 6.1: 20 MHz Baseline Data.

Frequency MHz	Signal Level dBμV
20.0	105.1
40.0	79.8
60.0	94.2
80.0	81.2

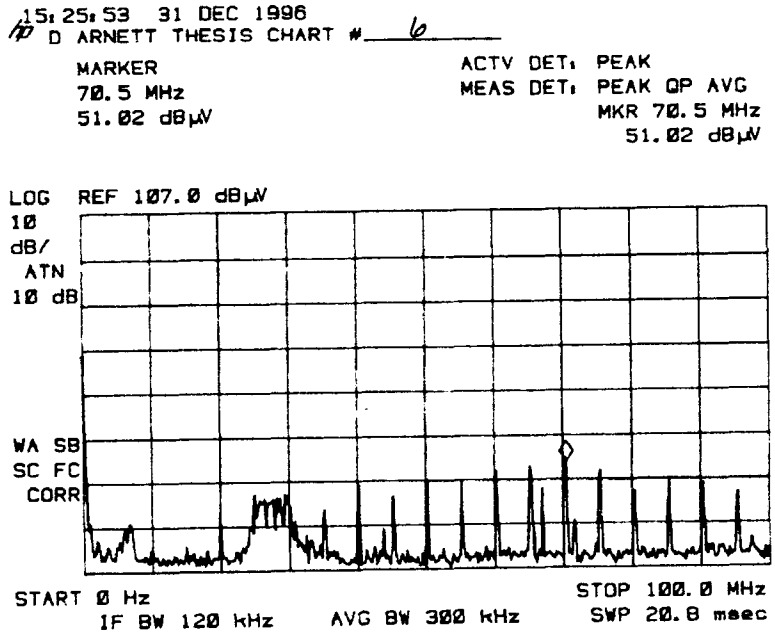
The 33.33 MHz clock is shown in Figure 6.2. Two harmonic peaks were measured, and those readings appear in Table 6.2.

Table 6.2: 33.33 MHz Baseline Data.

Frequency MHz	Signal Level dBμV
33.3	104.7
66.6	85.0

The null experiment data is shown in Figure 6.3. The diamond-shaped marker is placed on the highest data point in the spectrum. The notation in the upper right corner of the data plot indicates that the marker is at 70.5 MHz, and the signal amplitude at that frequency is 51.02 dBμV on the Modulated Clock line and 50.71 dBμV on the Modulation Signal line. This suggests that data above 60 dBμV is related to intentional signals rather than extraneous noise.

The signal readings reported, as with the 20 MHz and 33 MHz baseline data shown above, are made using a measure-at-maximum function of the HP8594EM Spectrum Analyzer. This function will repeatedly narrow the measurement range about a spectral peak, to find the local maximum very precisely. The function then makes Peak, Quasi-Peak, and Average detector measurements. The data measured in this way reflects the signal amplitude with better accuracy than the marker function.



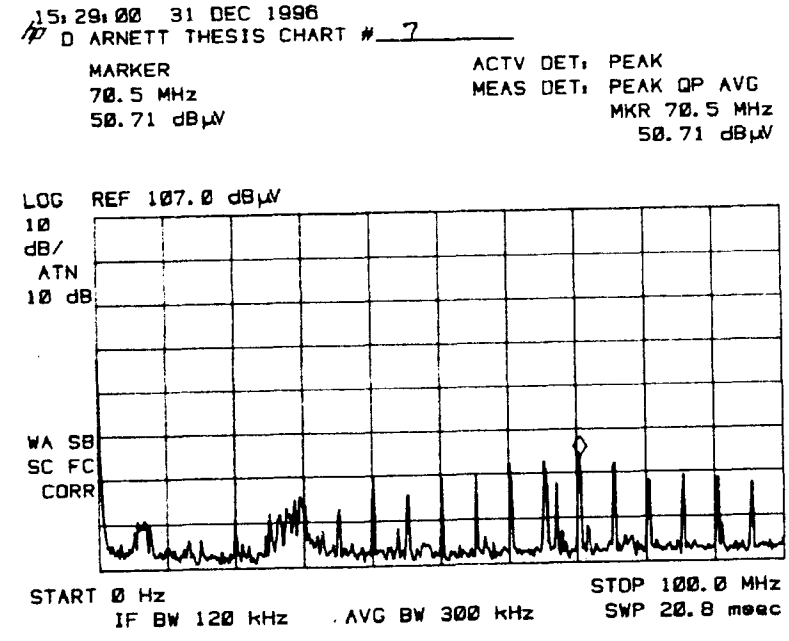


Figure 6.3: Null Experiment.
Above, Modulated Clock. Below, Modulation Signal.

6.3 Does an Exclusive-OR Modulator Generate a Suppressed Carrier Signal?

The data in Figure 6.4 shows the spectrum measured when a 20 MHz clock is modulated with a 2.5 MHz square wave. The unmodulated clock spectrum is also shown for comparison. The signal amplitude at 20 MHz is above the 60 dBμV background noise level, and so there is true spectral content measured there. However, 20 MHz has clearly been suppressed, and the energy has moved to other frequencies in the spectrum.

The clock harmonic at 60 MHz also is suppressed. However, the harmonics at 40 MHz and 80 MHz are not suppressed. This is an unexpected result, and will be discussed further in Section 6.9.

Similarly, Figure 6.5 shows the spectrum observed when a 33.33 MHz clock is modulated with a 2.083 MHz square wave. The signal at 33.33 MHz is suppressed; the signal at 66.67 MHz is not suppressed.

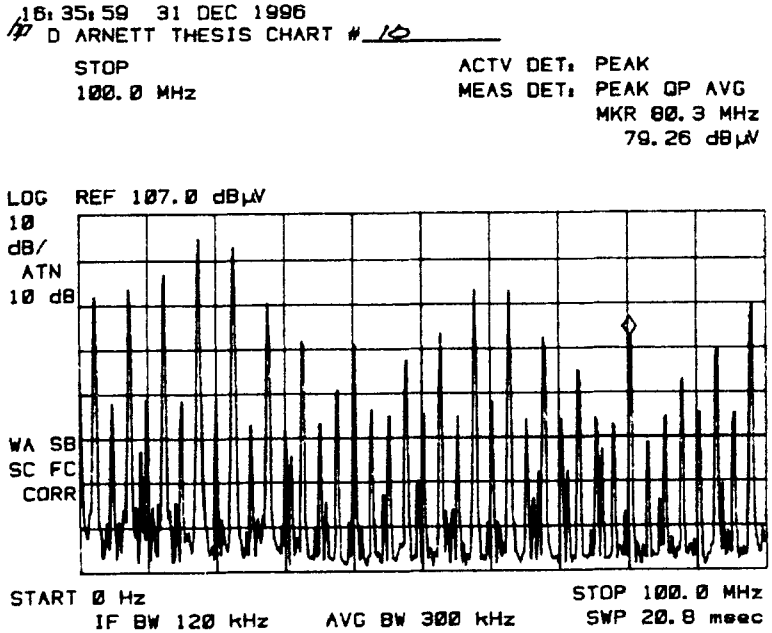
The buffered exclusive-OR modulator does create a suppressed-carrier signal. However, this suppression does not appear to benefit even-multiple harmonics.

6.4 Can Synchronous Demodulation Recover the Original Clock?

In each of the dozens of modulation profiles tested, the Demod signal was measured using the Universal Counter. Without fail, it reported the correct frequency. The signal timing was also quite good, as will be discussed in Section 6.10. Synchronous demodulation appears to function as expected.

6.5 Does the shape of the side band match the modulation spectrum?

To address this, we return to the measurements of the 20 MHz clock that has been modulated by a 2.5 MHz square wave. Figure 6.6 shows the spectrum observed at the



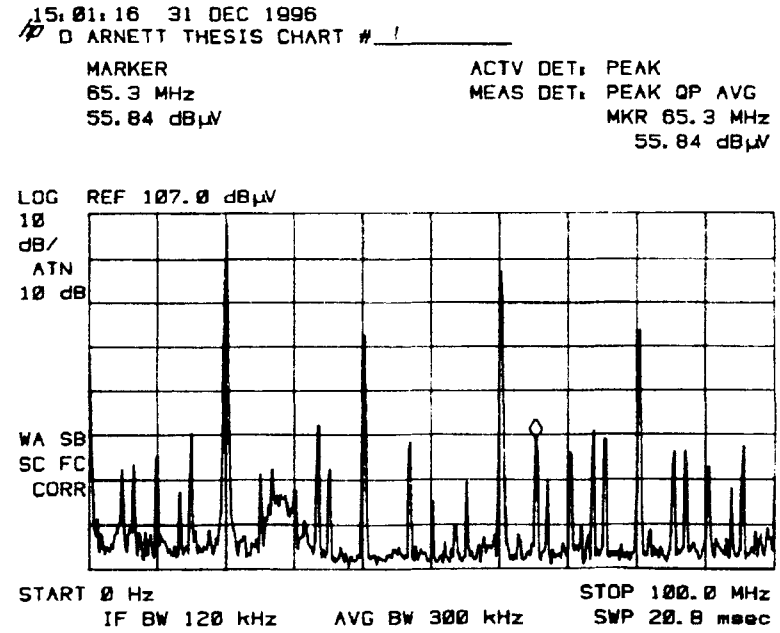


Figure 6.4: 20 MHz Clock with 2.5 MHz Square Wave Modulation.
Above, Modulated Clock. Below, Narrow Band Clock.

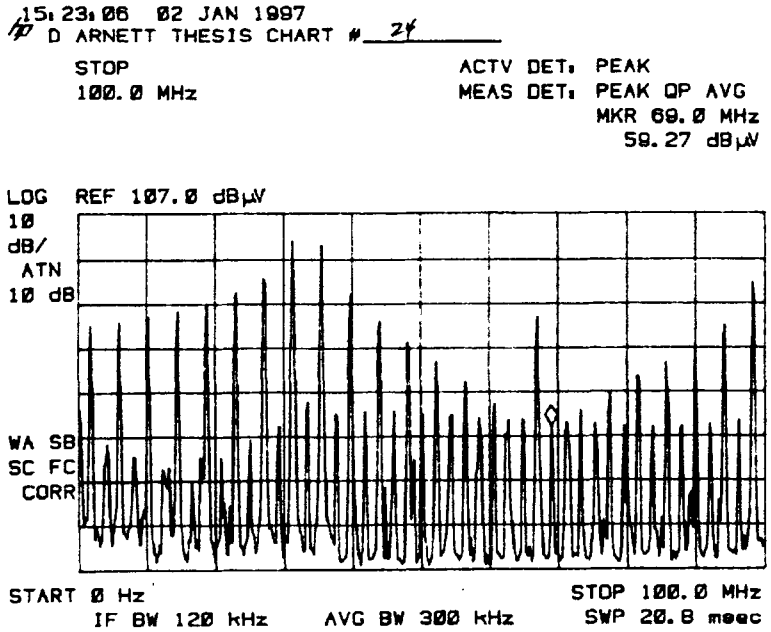


Figure 6.5: 33.33 MHz Clock with 2.083 MHz Square Wave Modulation. Above, Modulated Clock. Below, Narrow Band Clock.

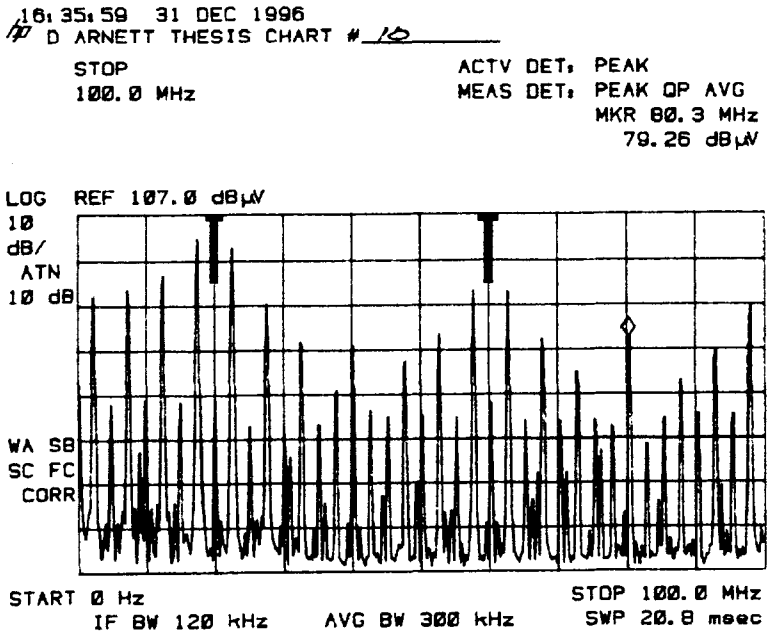


Figure 6.6: 20 MHz Clock with 2.5 MHz Square Wave Modulation and Marks. Above, Modulated Clock. Below, Modulation Signal.

Modulated Clock output, and the spectrum of the Modulation Signal. A dark line has been added to the upper plot to mark 20 MHz and 60 MHz, for easier identification of the side bands, which fall off monotonically with peaks every 5 MHz. The Modulation Signal spectrum has its highest content at 2.5 MHz. Peaks appear every 5 MHz, falling off monotonically. Thus, the side bands replicate the spectrum of the Modulation Signal.

The recorded spectrum of the Modulation Signal appears in Table 6.3 below. The first two columns are the recorded frequency and signal amplitudes. The third column shows the signal strength normalized to the 2.5 MHz signal level.

Table 6.3: 2.5 MHz Modulation Spectrum.

Frequency MHz	Signal Level dBμV	Normalized Level dB
2.5	102.8	0.0
7.5	93.8	-9.0
12.5	90.2	-12.6
17.5	87.6	-15.2

The spectrum of the Modulated Clock appears in Table 6.4. The third column shows the frequency offset from 20 or 60 MHz, as appropriate. The fourth column shows the level of the side band spectrum normalized to the level of the first side band peak at 20 MHz or 60 MHz, as appropriate. The predicted levels in column five came from Table 6.3.

The frequency offsets were as expected: 2.5, 7.5, and 12.5 MHz from the carrier harmonics. The normalized levels were predicted to be 0, -9, and -12.6 dB. The actual side band levels varied from those values, sometimes rather significantly, though the general trend of a decaying side band was as expected.

The spectra in Figure 6.7 were generated by modulating a 33.33 MHz clock with a 4^{th} order pseudo-random signal. The order number indicates the size of the state machine

Table 6.4: 20 MHz Clock with 2.5 MHz Square Wave Modulation.

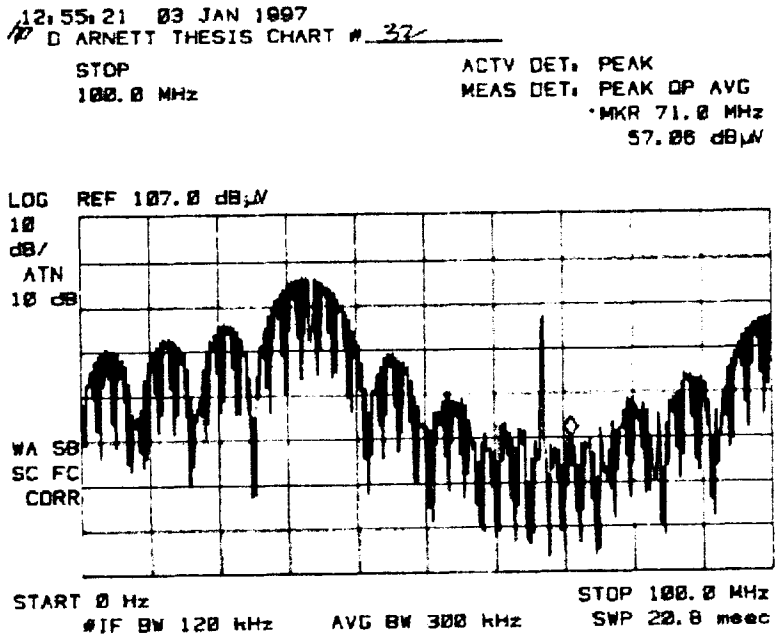
Frequency MHz	Signal Level dBμV	Frequency Offset MHz	Normalized Level dB	Predicted Level dB
7.5	90.7	12.5	-11.3	-12.6
12.5	94.0	7.5	-8.0	-9.0
17.5	102.0	2.5	0.0	0.0
20.0	66.7	0.0	NA	NA
22.5	100.2	2.5	0.0	0.0
27.5	87.3	7.5	-12.9	-9.0
32.5	79.0	12.5	-21.2	-12.6
40.0	78.5	NA	NA	NA
47.5	74.9	12.5	-15.4	-12.6
52.5	80.8	7.5	-9.5	-9.0
57.5	90.3	2.5	0.0	0.0
60.0	65.1	0.0	NA	NA
62.5	90.0	2.5	0.0	0.0
67.5	79.6	7.5	-10.4	-9.0

used to generate the modulation pattern. The effective clock rate of this Modulation Signal was 2.222 MHz. Note that the Modulated Clock spectrum still bears a null at 33.33 MHz. It appears as a notch in the curvature of the spectrum.

The spectral peaks of the Modulation Signal were measured. These are tabulated and normalized in Table 6.5. The peak is taken to be the highest spectral line in a group of lines. This peak can be more difficult to identify both in frequency and magnitude.

Table 6.5: 4th Order 2.222 MHz Pseudo-Random Modulation.

Frequency MHz	Signal Level dBμV	Normalized Level dB
0.0	96.6	0.0
11.7	83.7	-12.9
21.1	79.6	-17.0
29.4	76.7	-19.9



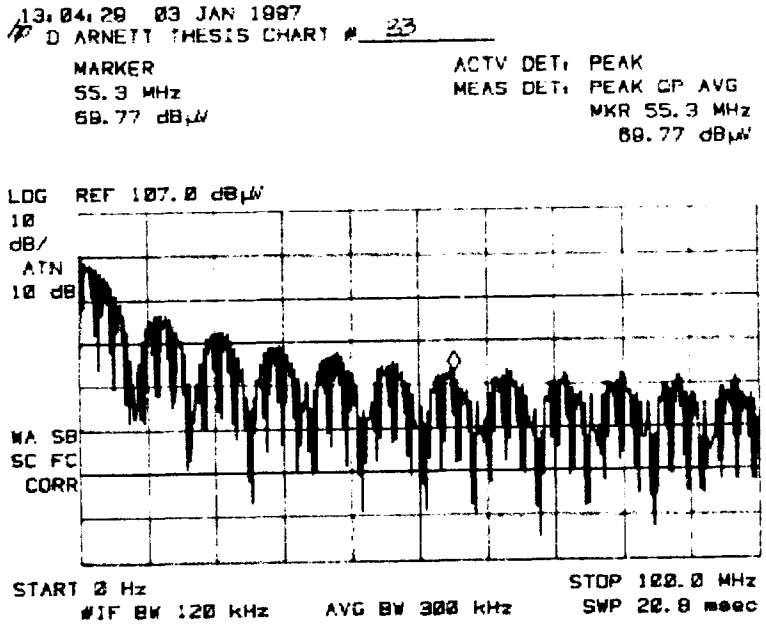


Figure 6.7: 33.33 MHz Clock with 4th Order Pseudo-Random Modulation. Above, Modulated Clock. Below, Modulation Signal.

The peak levels of the Modulated Clock are presented in Table 6.6. Calculating offsets and normalized signal levels is made difficult by the slight asymmetry of the spectrum about the 33.33 MHz carrier frequency, but the results are helpful.

Table 6.6: 33.33 MHz Clock with 4th Order 2.222 MHz Pseudo-Random Modulation.

Frequency MHz	Signal Level dBμV	Frequency Offset MHz	Normalized Level dB	Predicted Level dB
3.9	78.1	29.5	-15.3	-19.9
12.8	80.4	20.6	-13.0	-17.0
21.1	83.5	12.2	-9.9	-12.9
32.2	93.4	1.1	0.0	0.0
45.0	76.8	11.6	-16.6	-12.9
53.3	68.5	20.0	-24.9	-17.0
66.7	84.4	NA	NA	NA
78.9	66.3	21.1	-18.1	-17.0
87.8	71.6	12.2	-12.8	-12.9
100.5	84.4	0.5	0.0	0.0

In this case, the uncertainty in identifying peak locations disturbs the frequency offsets slightly from the predicted offsets of 0, 11.7, 21.1, and 29.4 MHz. As in the previous test case, the signal amplitudes also varied from the expected normalized values of 12.9, 17.0 and 19.9 dB.

It is significant to note that, in both cases, the upper side band of the fundamental fell away more quickly than expected, while the lower side band fell away more slowly. This trend was observed in many of the spectra studied.

In general, the side bands of the modulated clocks did bear a strong resemblance to the spectra of the modulating signals, as predicted by theory.

6.6 What is the relationship between the various effective frequencies?

The effective clock rate or effective frequency of a signal is the number of low-to-high transitions per second. These effective frequencies were measured for many combinations of input clock and modulation profile. A sampling is provided in Table 6.7. Note that the original clocks and demodulated clocks have the same frequencies, and that these frequencies could be calculated as the sums of the Modulated Clock effective rate and the Modulation Signal effective rate.

Table 6.7: Measured Effective Frequencies.

Original Clock Effective Rate MHz	Modulation Signal Effective Rate MHz	Modulated Clock Effective Rate MHz	Demod. Clock Effective Rate MHz
20.00	2.50	17.50	20.00
20.00	5.00	15.00	20.00
20.00	4.17	15.83	20.00
33.33	8.33	25.00	33.33
33.33	2.08	31.25	33.33
33.33	1.11	32.22	33.33
33.33	4.44	28.89	33.33

Clearly, raising the effective frequency of the Modulating Signal directly lowers the effective clock rate of the Modulated Clock.

6.7 How does the spread of the side bands affect side band amplitudes?

In this area, there were some unexpected results. With square wave modulation, the modulation rate seemed to have little effect on the magnitudes of the spectral

measurements. The results with broadband sources were different. In this section, all measurements are made at the highest peak in the side bands around 33.33 MHz.

Figures 6.8, 6.9, and 6.10 show the spectra measured when a 33.33 MHz clock is modulated by 2.1, 4.2, and 8.3 MHz square waves. The side bands are fairly compact with 2.1 MHz modulation, and rather broad with 8.3 MHz modulation. Yet, the peak amplitude of the Modulated Clock is not greatly affected, as demonstrated in Table 6.8.

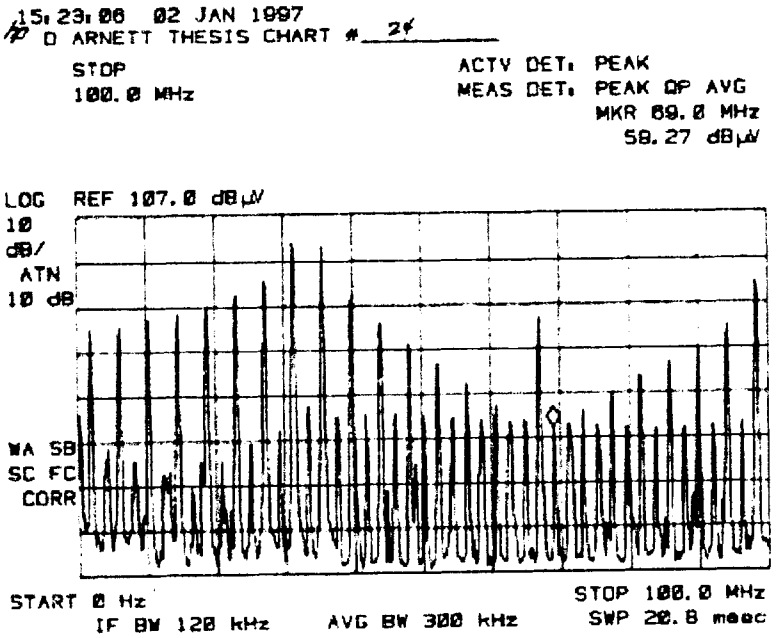
Table 6.8: Side Band Amplitudes with Various Narrow Band Modulation Profiles.

Modulation Frequency MHz	Modulated Clock Effective Rate MHz	Peak Amplitude dBμV
2.08	31.25	101.2
4.17	29.17	101.8
8.33	25.00	103.1

Since the effective clock rate is so much better with the 2.1 MHz modulation, one might suggest that slow modulation is always best. However, the pseudo-random modulation data suggests there is a limit to that line of thought.

A series of data points appears in Table 6.9 below. These were measured while modulating a 33.33 MHz clock with various 6th order pseudo-random signals. The quasi-peak detector function was used, rather than the peak detector, because results from the two varied significantly at some points in the measurement series. The results for the fastest and slowest modulation rates are higher than for those in the middle.

Further analysis of the signals indicated that the result is related to the separation between the fine detail in the spectra. These pseudo-random signals are composed of a series of individual spectral lines, which are closely spaced at regular intervals, and are of similar amplitudes. Compacting or expanding the side bands changes the separation between these fine spectral lines. In this case, with a 4.23 MHz effective modulation rate,



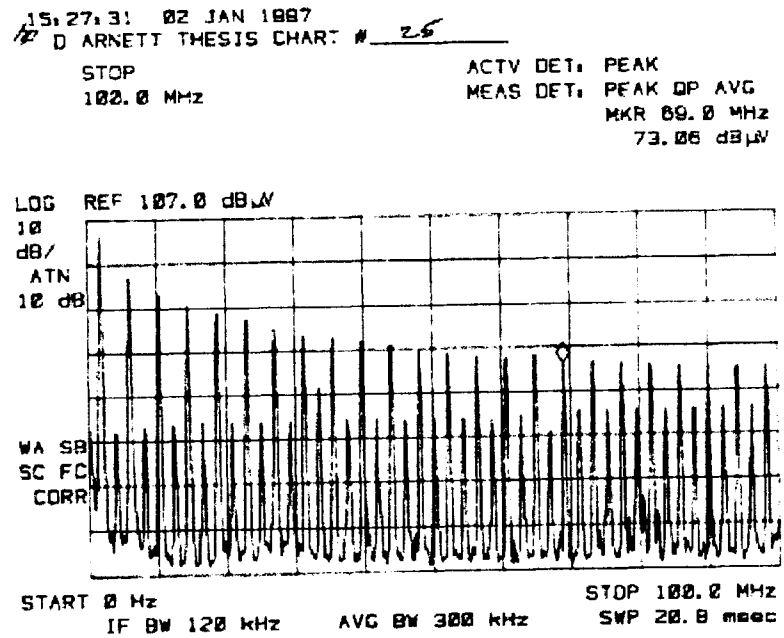
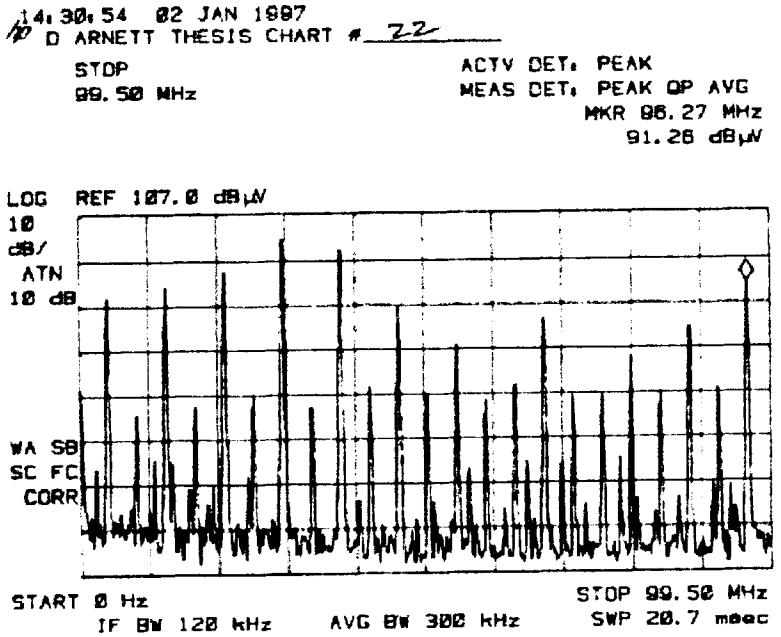


Figure 6.8: 33.33 MHz Clock with 2.1 MHz Square Wave Modulation. Above, Modulated Clock. Below, Modulation Signal.



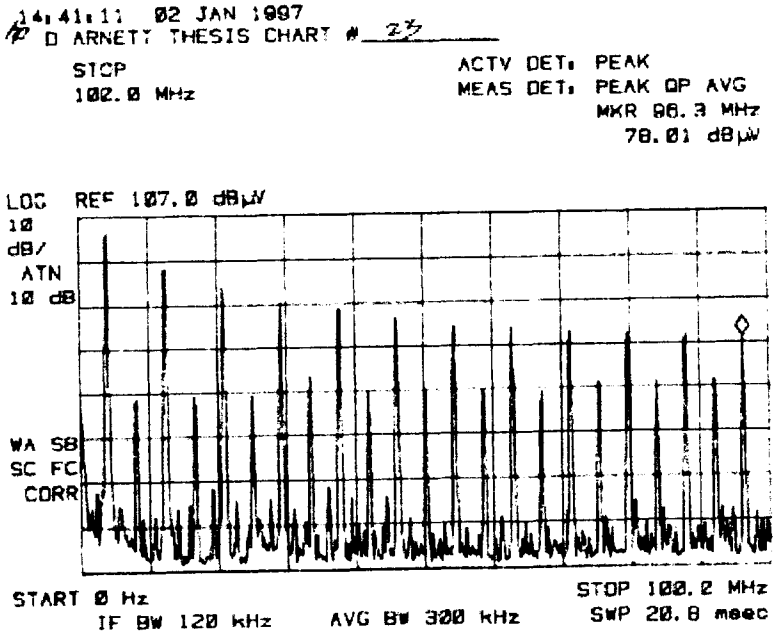
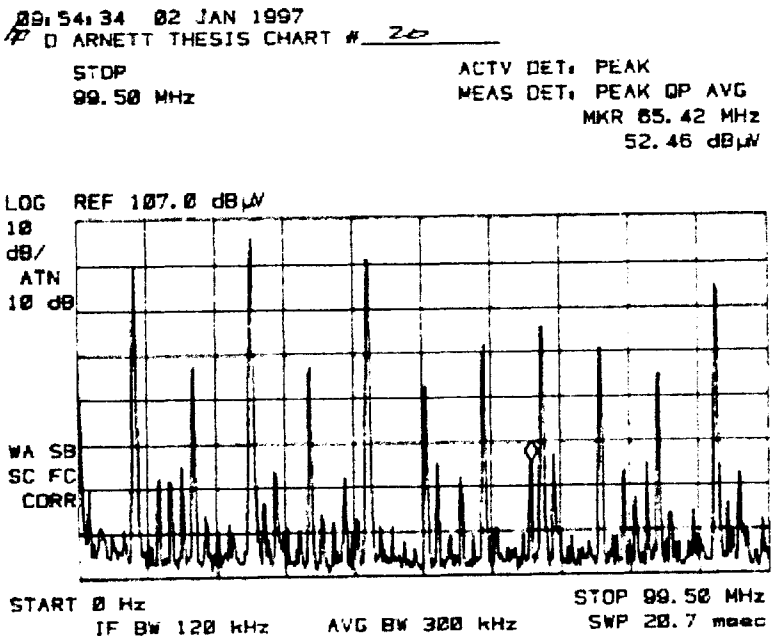


Figure 6.9: 33.33 MHz Clock with 4.2 MHz Square Wave Modulation. Above, Modulated Clock. Below, Modulation Signal.



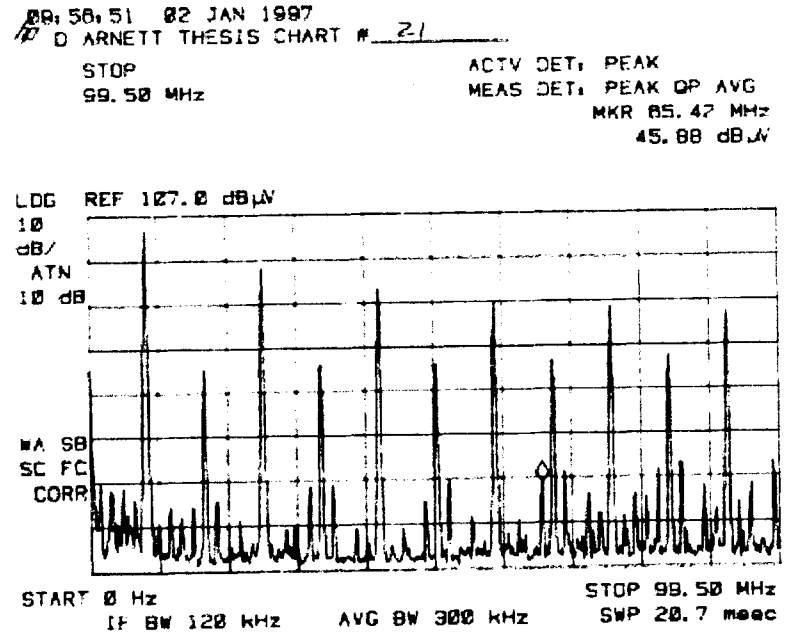


Figure 6.10: 33.33 MHz Clock with 8.3 MHz Square Wave Modulation. Above, Modulated Clock. Below, Modulation Signal.

Table 6.9: Side Band Amplitudes with Various Broadband Modulation Profiles.

Modulation Signal Effective Rate MHz	Modulated Clock Effective Rate MHz	Highest Amplitude (Quasi-Peak) dBμV
0.53	32.80	95.7
1.06	32.28	91.8
2.12	31.22	87.9
4.23	29.10	87.6
8.45	24.89	88.8
16.93	16.40	90.7

the separation between spectral lines was found to be 158 kHz. This would place adjacent spectral lines beyond the 120 kHz input bandwidth of the spectrum analyzer. Further side band compaction causes the spectrum analyzer to add together the power in adjacent spectral lines.

The spread of the side bands does not have a large effect upon the amplitude of the highest spectral peaks. The design is optimized by using a modulation profile in which the spacing between fine spectral details is near the input bandwidth of the measurement device or of the susceptible equipment.

6.8 How does narrow band modulation compare to broadband modulation?

The data used in the last section is useful here as well. In Section 6.2, the baseline measurements for the 33.33 MHz unmodulated clock showed that the amplitude of the fundamental was 104.7 dBμV. Table 6.10 demonstrates the degree to which the spectral amplitude around 33.33 MHz changes with modulation. Broadband and narrow band modulation signals will be compared based upon having nearly equivalent effective frequencies. The amplitude measurements for square wave signals were made with both peak and quasi-peak detectors, and were found to be the same, within tenths of a decibel.

Table 6.10: Amplitude Reductions in the Spectra of 33.33 MHz Clocks with Square-Wave and Pseudo-Random Modulation Signals having Comparable Effective Frequencies.

	Square Wave Signal		Pseudo-Random Signal	
Effective Modulation Frequency MHz	Peak Amplitude dBμV	Amplitude Change dB	Peak Amplitude (Quasi-Peak) dBμV	Amplitude Change dB
2.1	101.2	-3.5	87.9	-16.8
4.2	101.8	-2.9	87.6	-17.1
8.3	103.1	-1.6	88.8	-15.9

The broadband pseudo-random signals demonstrate a greater ability to reduce measurable emissions than do narrow band square wave signals.

6.9 Why are even-multiple harmonics not suppressed?

Experimentation often opens the way to new questions. The data reported in Section 6.3 showed that even-multiple harmonics were not diminished by modulation, but instead continued as narrow band peaks. These peaks are present in all of the spectra, and the amplitudes are consistent no matter what modulation profile was applied.

A pure square wave will not have even-multiple harmonics. In practice, there are two primary sources of even-multiple harmonics in the noise spectra radiated from digital devices: the first deals with power supply switching; the second deals with the structure of CMOS drivers.

In many digital circuits, some gates will change state on the rising edge of the system clock or strobe, and some will change state on the falling edge. There will be a current inrush at the power pins on both edges of the system clock. This is a spike function occurring at twice the clock frequency. This is sometimes called ΔI-noise (Costa et al., 1996). Using a suppressed carrier clock to drive a digital circuit typically causes a

small fraction of these clock edges to be omitted. Only a few power supply current spikes will be omitted. The net effect of this change is small, and is not expected to cause benefit in systems where the primary noise emission source is ΔI-noise.

The second source of even-multiple harmonics is related to the structure of CMOS output pads. These are the circuits that drive the output pins of digital ICs. The pin is connected to the positive voltage supply by a p-channel field effect transistor (FET), and to ground by an n-channel FET. Only one transistor conducts at a time, so that the output pin is driven either high (by the P-FET pull-up transistor) or low (by the N-FET pull-down transistor). P-FETs typically have a higher channel resistance than N-FETs, and so the rising edge of a signal pulse will be slower than the falling edge. This difference between rising- and falling-edge rates will introduce even-multiple harmonics into a signal that should ideally have none.

In this scenario, the even multiple harmonics are not affected by the modulation, because they are injected into the signal after the modulator.

The pull-up and pull-down resistances can be measured by allowing the output circuit to drive known loads. In this manner, the output resistances of the Altera gate array are determined to be 44.1Ω for the pull-up, and 10.9Ω for the pull-down. The ratio of pull-up to pull-down resistances is greater than 4. One way to determine whether this mechanism is the source of the even-harmonic content is to use series termination.

The trace characteristic impedances on the circuit board were changed to about 100Ω, and the secondary Xclk demodulator was added to the gate array program, as discussed in Section 4.6. The spectrum of Figure 6.11 was measured in this configuration. The 100Ω traces were severed near the gate array, and 120Ω resistors inserted in series with the transmission line. This change makes the pull-up resistance 164.1Ω, and the pull-down resistance 130.9Ω, for a ratio near 1.25. The spectrum of Figure 6.12 was measured in this configuration.

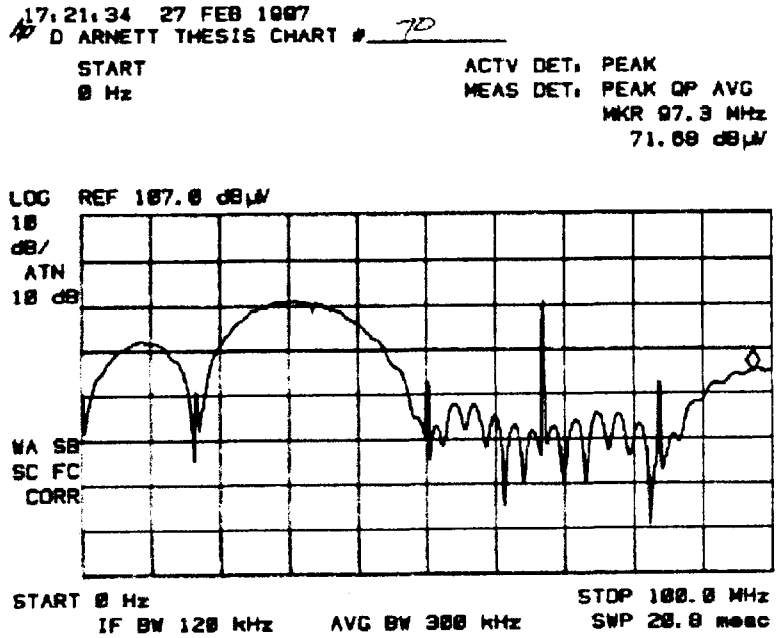


Figure 6.11: Modulated 33.33 MHz Clock Without Source Termination.

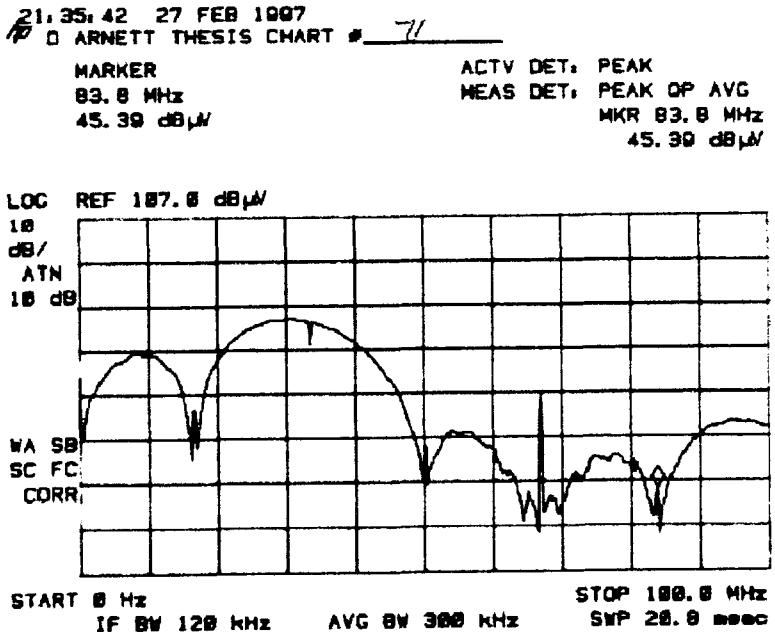


Figure 6.12: Modulated 33.33 MHz Clock With Source Termination Added.

Adding the series resistors to the two signal lines lowered the amplitude of the entire spectrum. At 30 MHz, the signal level dropped by 3.4 dB, which would be expected. At 66.7 MHz, the signal level dropped by 14.6 dB. This large change in the level of the 66.7 MHz harmonic supports the possibility that this signal is generated due to the asymmetry of the output driver.

6.10 How does signal filtering affect recovery of the original clock?

Signal filtering is a common technique for suppressing radio emissions. Filtering changes the shape of clock edges in ways that might harm the stability of the demodulated clock signal. Since filtering is so widely used, any degradation that arises from filtering should be understood. Degradation will be evaluated primarily by monitoring cycle-to-cycle jitter.

The 66.67 MHz oscillator feeding the gate array exhibited 27 psec of jitter. With no modulation, source termination, or filtering, the gate array put out a 33.33 MHz clock with 37 psec of jitter at the Xclk demodulator output. After modulation and demodulation, the same system exhibited 89 psec of jitter. One popular microprocessor that uses PLL synchronized data interchange requires less than 200 psec of jitter on system clocks.

When 120Ω source terminators were added to the gate array outputs, the jitter of the demodulated clock did not change. Strong filtering was added, in the form of Murata BLM21B201S surface mount ferrite beads. These were placed in series with the 120Ω resistors. Jitter increased to 101 psec.

To push the envelope, the BLM21B201S ferrite beads were replaced with BLM21B751S beads. These beads add well over 100Ω of reactance at 33 MHz. The square edges of the Modulated Clock wave were so heavily damped that the wave form

was more like a triangle wave, and fell well short of the power and ground voltages. In this extreme case, the jitter in the demodulator output was only 302 psec.

This method of modulation and demodulation appears capable of recreating clean clock waves when used in concert with source termination and signal filtering.

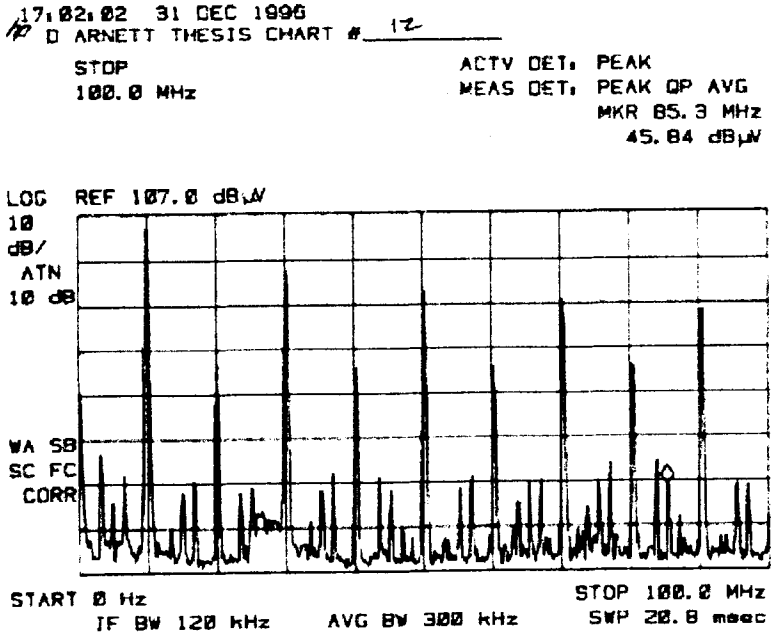
Synchronous demodulation assumes that the Modulated Clock and the Modulation Signal have been treated in a similar manner from the output of the modulator to the demodulator. There was no attempt to quantify the issues that can arise if the two signal lines are filtered differently.

6.11 Why are the side bands not symmetrical in many cases?

Side band asymmetry was not expected, but it should not be surprising. One reason for asymmetry was discussed in Section 3.5: there is band overlap. The intermodulation products of signals that are already spectrally rich can reinforce or cancel each other. The extreme case of side band asymmetry occurs when the Modulation Signal is a square wave at half the frequency of the original clock, as shown in Figure 6.13. Here, the 20 MHz square wave is modulated by a 10 MHz square wave. The combinations of wave harmonics adding and subtracting with other wave harmonics produce a Modulated Clock spectrum that closely resembles the Modulation Signal spectrum. In fact, they are the same. Modulating a 20 MHz square wave with a 10 MHz square wave creates a 10 MHz square wave which is 90° out of phase with the Modulation Signal.

6.12 Summary

The data verifies that the spectra generated by the suppressed carrier modulator fits the theory of Chapter 3. The timing parameters are within the range expected in digital devices, and are well enough understood to permit system designers to make appropriate trade-offs. Three areas of unexpected results were investigated: asymmetry in



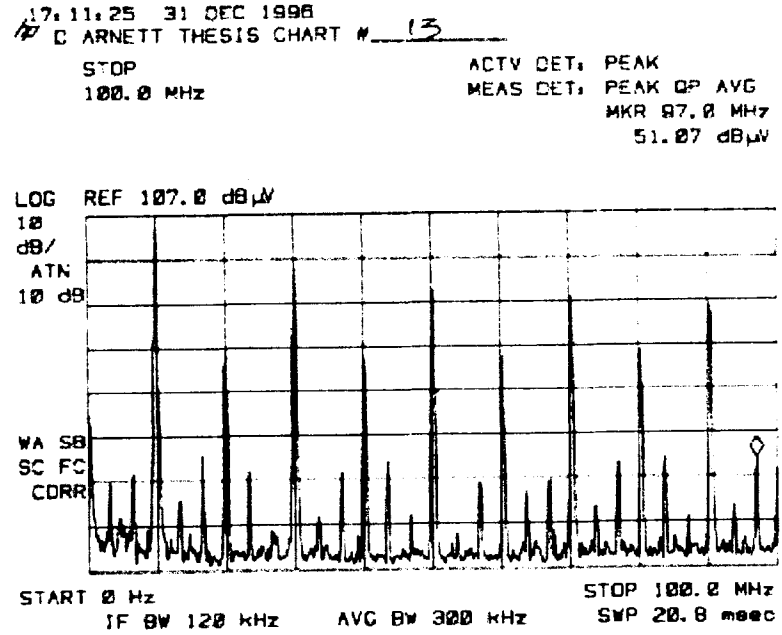


Figure 6.13: Extreme Side Band Asymmetry of Modulated 20 MHz Clock. Above, Modulated Clock. Below, Modulation Signal.

the side bands of the Modulated Clock; the presence of narrow band even-multiple harmonics in Modulated Clock spectra; and the rising of signal levels when the Modulation Signal has fine spectral lines spaced closer than the measurement bandwidth.

7. Design Scenarios

7.1 Design Constraints and Baseline

Two design scenarios will be presented. In the first scenario, the Modulated Clock will be used without demodulation. The second scenario will include demodulation.

Both scenarios are based upon 33.33 MHz clocks. Both will use 120Ω resistors and Murata BLM21B201S ferrite beads in series with the 5V TTL output driver pins. The signals will be routed through the five inch length of 300Ω television twin-lead on their way to the receiver chip.

Figure 7.1 is a plot of the spectrum measured without any modulation present. The range measured is from 30 MHz to 250 MHz, since the legal limits for radiated electromagnetic emissions start at 30 MHz, and many systems have their major emission issues below 250 MHz due to a 7 dB relaxation of the RF emission limits at 230 MHz.

7.2 Design Scenario #1

In this scenario, a high effective clock rate is required so that the system will have adequate data throughput. To achieve this throughput, the Modulation Signal will be a 4^{th} order pseudo-random signal with a 555 kHz effective frequency. The 33.33 MHz clock will be slowed 1.7% to 32.8 MHz.

Figure 7.2 shows the spectrum measured on the Modulated Clock signal trace. The peaks are summarized in Table 7.1 below, and are compared to the baseline measurements.

The odd-multiple harmonics that this technique is designed to resolve were decreased 9.5 to 11.7 dB. The even-multiple harmonics changed by 2.3 dB or less.

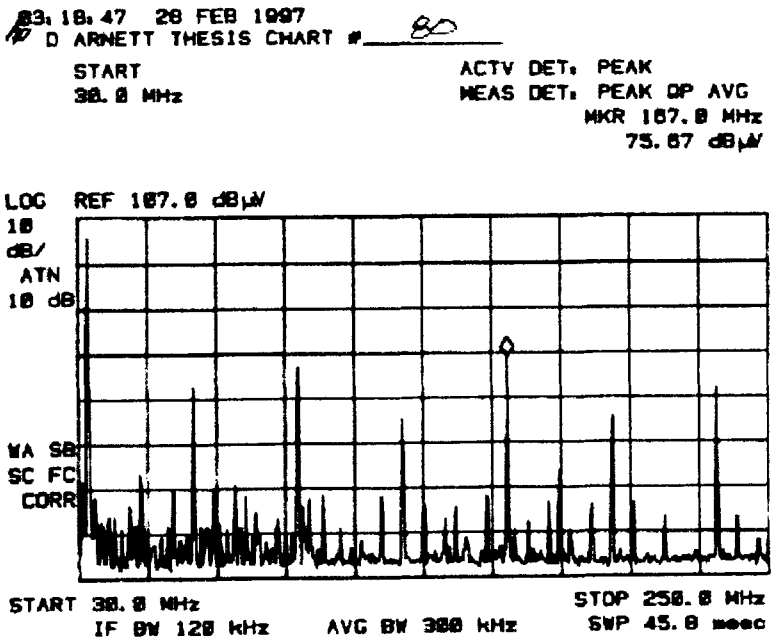


Figure 7.1: 33.33 MHz Design Baseline.

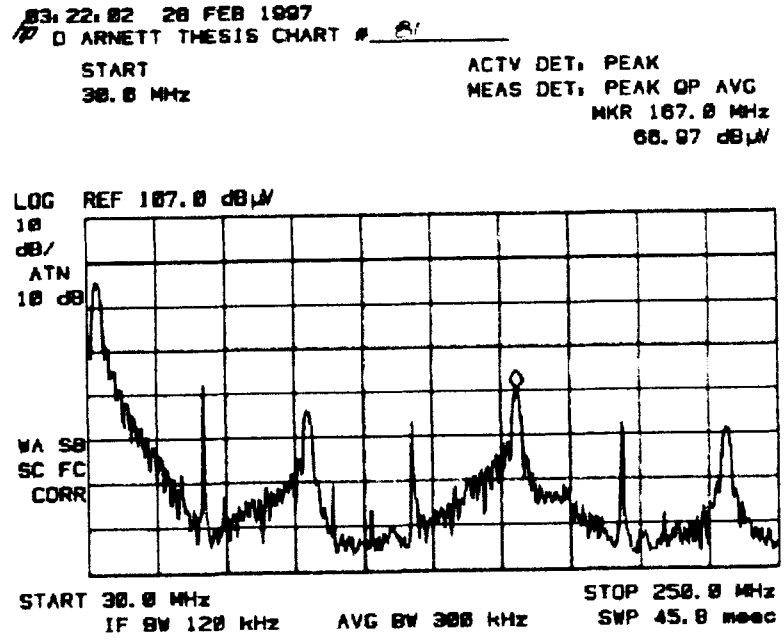


Figure 7.2: Design Scenario #1.

Table 7.1: Amplitude Reductions due to the Design Scenario #1 Modulation Profile.

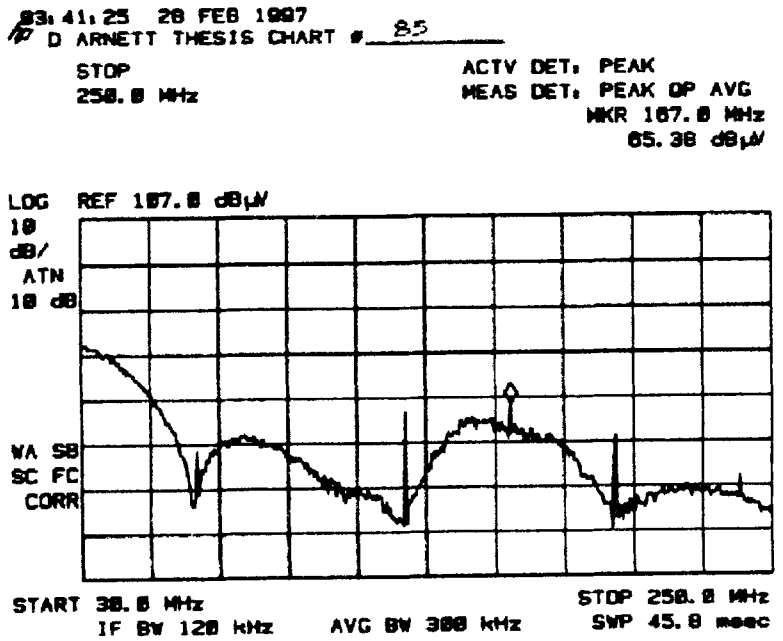
Baseline Frequency MHz	Baseline Amplitude (Quasi-Peak) dBμV	Modulated Amplitude (Quasi-Peak) dBμV	Amplitude Change dB
33.33	102.90	91.60	-11.30
66.67	70.00	69.70	-0.30
100.00	74.10	62.70	-11.40
133.33	63.00	60.70	-2.30
166.66	76.20	66.70	-9.50
200.00	63.00	60.90	-2.10
233.33	69.20	57.50	-11.70

7.3 Design Scenario #2

In this scenario, a high effective clock rate is not required because the system will operate on a full 33.33 MHz demodulated clock. In practice any modulation profile could be used which met the emission requirements. In this instance, the Modulating Signal will be a 10^{th} order pseudo-random signal with a 16.683 MHz effective frequency. With this modulation pattern, the Modulation Signal and Modulated Clock have almost the same effective frequencies.

Figure 7.3 shows the spectrum measured on both signals. The peak amplitudes are summarized in Tables 7.2 and 7.3. The peak frequencies in the pseudo-random spectra are so different from the baseline peak frequencies that direct comparison becomes difficult. The peaks closest to each other in the baseline and modulated tests will be compared as seems most reasonable. There is also no attempt to predict how actual emissions radiated from the two signals would combine at a radio receiver.

The spectral peaks that this technique is designed to resolve were decreased 8.8 to 24.7 dB. With this modulation, and fairly strong filtering, the Xclk demodulated clock



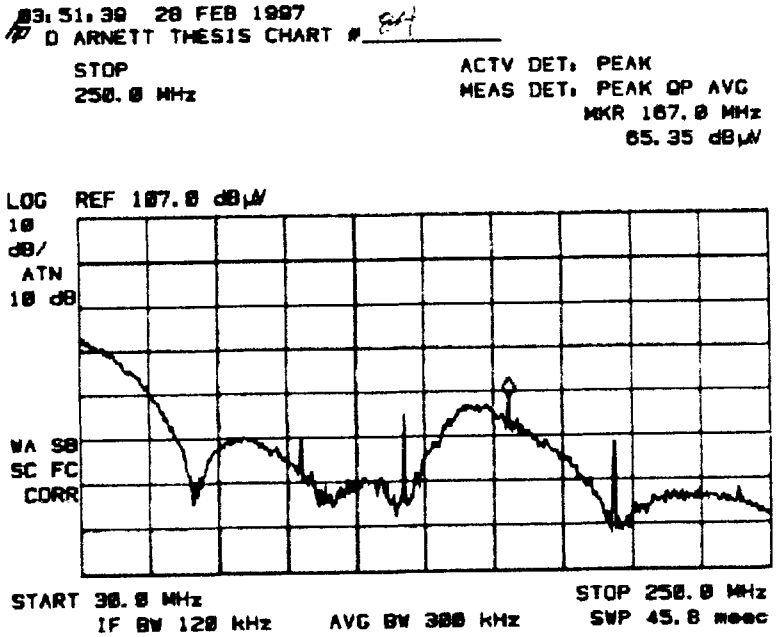


Figure 7.3: Design Scenario #2.
Above, Modulated Clock. Below, Modulation Signal.

Table 7.2: Amplitude Reductions Measured on the Modulated Clock Signal due to the Design Scenario #2 Modulation Profile.

Baseline Frequency MHz	Baseline Amplitude (Quasi-Peak) dBμV	Modulated Clock Frequency MHz	Modulated Clock Amplitude (Quasi-Peak) dBμV	Amplitude Change dB
33.3	102.9	32.5	78.2	-24.7
66.7	70.0	66.7	56.0	-14.0
100.0	74.1	80.0	58.5	-15.6
133.3	63.0	133.3	63.7	0.7
166.7	76.2	166.6	65.2	-11.0
200.0	63.0	200.0	58.2	-4.8
233.3	69.2	240.0	49.2	-20.0

Table 7.3: Amplitude Reductions Measured on the Modulation Signal due to the Design Scenario #2 Modulation Profile.

Baseline Frequency MHz	Baseline Amplitude (Quasi-Peak) dBμV	Modulation Signal Frequency MHz	Modulation Signal Amplitude (Quasi-Peak) dBμV	Amplitude Change dB
33.3	102.9	30.5	78.8	-24.1
66.7	70.0	NA	NA	NA
100.0	74.1	82.0	55.7	-18.4
133.3	63.0	133.3	62.4	-0.6
166.7	76.2	166.6	67.4	-8.8
200.0	63.0	200.0	57.7	-5.3
233.3	69.2	240.0	46.2	-23.0

output was a 33.33 MHz square wave signal having a maximum cycle-to-cycle jitter of 101 psec.

7.4 Other Design Considerations

A discussion of spread spectrum clocks used for reducing radio interference should include some indication of common pitfalls related to the techniques. Perhaps the comments that follow are not academically germane to the fundamental thesis issues, but they may turn out useful to those who read this document in the future.

It is good engineering practice to resolve basic EMI issues, so far as possible, with all spread spectrum techniques deactivated. Spread spectrum clocks are not a replacement for fundamentally solid design work.

The spectrum should be broadened only as much as necessary to achieve EMI design objectives. 'More' is not always 'better.' If the product's mechanical structure has resonances, spread spectrum clocks will find them. If the product will be used near other devices having narrow band susceptibilities, broad band emissions will find them.

EMI test technicians should be informed when spread spectrum clocks are in use. The task of identifying broadband emissions can be more difficult than finding narrow band emissions. Some test labs will need to develop new processes for measuring these signals. Make sure the test lab learns how to find all of the emissions during product development. Do not delay their learning curve until the start of production audits.

Frequency modulation and amplitude modulation are not mutually exclusive. Both techniques have value in resolving specific issues, and some designers may choose to use both. To use both techniques, frequency modulate first, then amplitude modulate. If synchronous demodulation is required, the recovered clock signal will be an FM clock.

8. Conclusions

This method of generating a spread spectrum clock can significantly reduce the power available to interfere with a narrow band radio receiver or other susceptible narrow band devices. The technique has strengths and weaknesses evident from the measured data.

One significant weakness is its inability to control noise from even-multiple harmonics. These harmonics do cause radio interference because of the imperfections in logic IC drivers and ΔI-noise.

Suppressed carrier clocks can have a fairly flat response at higher harmonics, as shown in Table 7.1. This may be seen as a disadvantage in comparison to frequency modulation techniques, where the higher harmonics of the modulated clock have higher total frequency deviation, and therefore have lower peaks. The other side to this issue is that suppressed carrier clocks achieve their full potency at the fundamental, which is not true of the FM methods.

The data demonstrates several advantages of the suppressed carrier method. Suppressed carrier modulation reduced several signal peaks more than 15 dB, and in some cases more than 20 dB. These levels of amplitude reduction are rare with other spread spectrum techniques.

With demodulation, the suppressed carrier method produces clocks with very low cycle-to-cycle jitter.

The shape of the spectrum after modulation is somewhat arbitrary, which could be exploited by a clever designer who needs to target a specific frequency range as a quiet zone. The final modulated clock spectrum can be selected by designing and tailoring the spectral content of the Modulating Signal.

As one good idea sometimes leads to another, so a research project, when complete, may suggest additional areas for investigation. Additional areas of study related to this work might address the following questions:

What modulation spectra are possible with this scheme, and how deftly could a design engineer tailor the final spectrum? Referring to Figure 4.2, Modulating Signal II must be synchronous with the rising edge of Clock x2, and so the actual modulation profile is constrained. Could digital filter theories help define the range of spectra possible with this method?

How does this apparatus impact over-all system design? A clock signal is usually synchronous with some data signal, and that data signal would be generated by reference to a master clock running at half the frequency of Clock x2 . Are there architectural issues related to digital IC design that must be addressed in new ways for this system to function?

In systems requiring signal line filtering and synchronous demodulation, how much filter asymmetry is acceptable? In Section 6.10, there was no attempt to quantify the timing issues that can arise if the two signal lines are filtered differently.

9. Summary

Spread spectrum technologies are used in the field of electromagnetic compatibility design today. These techniques are powerful in their ability to reduce the power spectral density of radio emissions that could otherwise interfere with radio communications, radio navigation, or other legitimate uses of the radio spectrum.

The generation of suppressed carrier clocks stands as a useful spread spectrum technique - a tool in the EMC engineer's toolbox. Like any tool, it has its strengths and weaknesses. There are jobs for which this tool works well, such as reducing the effect of emissions from a cable interconnecting two circuits or systems. There are jobs better suited to other tools, such as reducing emissions due to ΔI-noise. Suppressed carrier clocks may be used along with other design techniques, and are compatible with common EMI reduction methods.

Suppressed carrier clocks are applicable to a wide variety of design applications. These signals offer an all-digital solution with high functional throughput, large reductions to spectral peaks, and significant design flexibility. Suppressed carrier clocks also provide the option of demodulation, to restore the original, unmodulated clock signal where needed.

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APPENDICES

Appendix A. Analysis Programs

The following objects and programs will generate the numerical results presented in Section 3.4. These programs operate under the Reverse Polish LISP (RPL) operating system of the HP48 Calculator, release K or later.

To use the programs, enter each object and store it under the object name provided. Enter a 32-bit modulation pattern of 0s and 1s as a column vector, then execute the program object RUNMODS. The four objects returned to the stack will match the four item equations shown in Section 3.4. *M* will be at stack level 4, Fm at Stack level 3, *S* at stack level 2, and Fs at level 1. These objects are best viewed in the Matrix Writer format with complex numbers shown in polar format, and the numeric display mode set to 0 FIX.

In the object descriptions, or program comments, Binary form refers to objects made of -1 and +1 values, while Logic form refers to objects made up of 0 and 1 values.

Object Name: C **Object Type:** Column vector

Purpose: 32-bit carrier signal in Binary form.

[1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1 1 -1]

Object Name: L→B **Object Type:** Program

Purpose: Convert 32-bit column vector on Level 1 from Logic form to Binary form.

```
<<
OBJ→ DROP 32 →LIST          Change vector to list
-2 * 1 ADD                  Map {1 0} to {-1 +1}
OBJ→ DROP {32} →ARRY        Change list to vector
>>
```

Object Name: B→L **Object Type:** Program

Purpose: Convert 32-bit column vector on Level 1 from Binary form to Logic form.

```
<<
OBJ→ DROP 32 →LIST          Change vector to list
-1 ADD -0.5 *               Map {-1 +1} to {1 0}
OBJ→ DROP {32} →ARRY        Change list to vector
>>
```

Object Name: BMOD **Object Type:** Program

Purpose: Modulate two Binary column vectors located on Levels 1 and 2, returning in a Binary column vector on Level 1.

```
<<
OBJ→ DROP 32 →LIST SWAP     Change vector to list
OBJ→ DROP 32 →LIST          Change vector to list
*                           Modulate
OBJ→ DROP {32} →ARRY        Change list to vector
>>
```

Object Name: RUNMODS **Object Type:** Program

Purpose: Given a column vector *M* on Level 1, return *M*, Fm, *S* and Fs on Levels 4 through 1.

```
<<
DUP                    Save copy of M
L→B FFT                Create Fm
2 PICK L→B             Obtain M
C BMOD DUP B→L         Create S
SWAP FFT               Create Fs
>>
```

Appendix B. Terms and Acronyms

Terminology and acronyms change frequently in current technology, and some have such narrow usage as to be considered jargon. Many of the acronyms and terms used in this thesis are listed here, for reference. Acronyms will be alphabetized as if they were common words.

AC - Alternating current. Electrical currents (or voltages associated with such currents) that flow in both directions in a conductor. In circuit operation, the magnitude of the current (or voltage) will typically change to positive and negative values in a repetitive, and often symmetric, pattern.

Altera - an integrated circuit manufacturer. An Altera gate array was used to implement the test circuit described in this thesis.

AM - Amplitude Modulation. A method of encoding information into a radio signal or other carrier in which the signal frequency remains relatively constant, but the wave amplitude is adjusted.

CMOS - Complementary metal-oxide semiconductor. An integrated circuit design method which uses both n-channel and p-channel field-effect transistors in each functional device.

DC - Direct current. Electrical currents (or voltages associated with such currents) that flow in only one direction in a conductor. In circuit operation, the magnitude of the current (or voltage) may change to any non-negative value.

dB - decibel. A unit of measure for logarithmic comparison of ratios. In comparing power measurements, the decibel value is ten times the base ten logarithm of the power ratio.

dBμV - decibels referenced to a microvolt. A logarithmic unit of measure for the expression of voltages. Any voltage can be expressed in units of dBμV by dividing the voltage magnitude by one microvolt, taking the base ten logarithm of the ratio, and multiplying by twenty.

DIP - Dual Inline Package. A method of arranging the terminals of a device for ease of assembly. The device terminals are arranged in two parallel rows of pins, with a well-defined spacing between adjacent pins. A matching pattern of holes is created in a printed circuit board. The pins of the DIP part pass through the holes in the circuit board, and are electrically and mechanically bonded to the circuit board with solder.

EMC - Electromagnetic Compatibility. A situation in which the radio emissions from a circuit or system are controlled such that the do not interrupt the function of another circuit or system. Antonym of EMI.

EMI - Electromagnetic Interference. A situation in which the radio emissions from a circuit or system interrupt the function of another circuit or system. Antonym of EMC.

Exclusive-OR - a standard logic gate. The output is driven to a logic 1 level unless both inputs are at the same logic level.

FET - Field effect transistor.

Flip-flop - a standard logic gate. When the Clock input of a flip-flop transitions from logic level 0 to logic level 1, the data present at the D input is transferred to the Q output. Flip-flops may include an output that is the inverse of Q, and may include preset and clear inputs. Some flip-flops use J-K inputs instead of a D input. Since these J-K flip-flops are not used in the present work, their function will not be discussed here.

FM - Frequency Modulation. A method of encoding information into a radio signal or other carrier in which the signal amplitude remains relatively constant, but the wave period is adjusted.

Glitch - a momentary error condition.

HERO - Hazards of Electromagnetic Radiation to Ordnance. A topic in the field of EMC dealing with the ability of radio waves to ignite explosive devices.

Hold - a timing parameter of flip-flops and latches. Hold time indicates the minimum time over which data at the D input must be stable to assure it will be properly transferred to the Q output. This hold time is specified from either the rising edge of the Clock input or the falling edge of the Gate input until the time D changes to a new logic level.

HP - Hewlett-Packard Company.

HPIB - Hewlett-Packard Interface Bus. A communication interconnect and signaling system used to interface a wide variety of equipment. HPIB is used mainly on scientific test and measurement products, and is similar to GPIB - the General Purpose Interface Bus.

IC - Integrated Circuit. A complex circuit implemented in a batched process on a single material substrate. The substrate is usually a semiconductor, and the process usually involves multiple photo-lithographic steps. Other materials may be added to the substrate during the process, such as dopants, conductive metals, and oxides. The term IC usually includes a package that envelopes the finished substrate in a mechanically robust manner, and provides electrical and thermal interconnect points.

IEC - The International Electrotechnical Commission.

IEEE - The Institute of Electrical and Electronic Engineers.

IF - Intermediate frequency. Many radio systems operate by translating a modulated signal from the carrier frequency down to a lower frequency. This frequency

translation is called heterodyning, and permits better frequency selectivity in the receiver. The lower frequency is called the intermediate frequency.

Jitter - variations in the periodicity of a repetitive signal. Jitter is usually defined as the difference between the period of one wave and the period of the following wave.

J-lead - a type of connection lead for electronic parts which are to surface-mounted to a circuit board. The J-lead extends from the package body toward the board surface. At a specified distance, the lead then bends back toward the package body, forming a J shape. The base of the J is soldered to a metal pad on the board surface.

Latch - a standard logic gate. Data on the D input of a latch is transferred to the Q output during any period of time that the Gate input is asserted. When the Gate input is de-asserted, the Q output of the latch remains at the same level as was present at the D input when the Gate signal changed. Latches may include an output that is the inverse of Q, and may include preset and clear inputs.

LVDS - Low Voltage Differential Signaling. A communication protocol used to transfer data to flat panel displays, especially in notebook computers. The voltage levels used to communicate clock and data signals are typically less than a half volt, and are driven as differential signal pairs, rather than as a signal relative to system ground. The clock signal is typically no faster than one-seventh the data rate, and is actually a synchronization signal. At the receiver end, a phase-locked loop operates at the actual data rate, and is synchronized to the slow clock signal. The output of the phase-locked loop is used to clock data bits off of the high-speed serialized data bus.

Macrocell - a block of logic gates within a programmable gate array.

NAND gate - a standard logic gate. The output is driven to a logic 1 level unless both inputs are at logic 1 levels.

N-FET - an n-channel field effect transistor.

P-FET - a p-channel field effect transistor.

PLL - Phase-locked loop. A circuit containing a controllable oscillator, feedback loop filter, and phase comparator. The PLL may also included digital divide circuits. When operating properly, the phase and frequency of the controllable oscillator will have a known relationship to the phase and frequency of a reference signal. Thus, the feedback control system allows the oscillator and reference signal to be phase-locked.

RF - Radio Frequency. This term is also used to refer to signals on wires or waves propagating through space which oscillate at radio frquencies. Radio frequencies begin at a few kilohertz, and end well below the frequency of infrared light. The upper limit for frequencies included in the term RF changes as the technologies for intentionally generating high-frequency radio waves improve.

RPL - Reverse-Polish LISP. The operating system used in the Hewlett-Packard series 28 and 48 calculators. RPL uses many of the list-processing features of the LISP computer language, but operates in a reverse-polish, or post fix, math syntax.

Setup - a timing parameter of flip-flops and latches. Setup time indicates the minimum time over which data at the D input must be stable to assure it will be properly transferred to the Q output. This setup time is specified from the time D changes state until either the rising edge of the Clock input or the falling edge of the Gate input.

TTL - Transistor-transistor logic. TTL refers directly to a family of logic functions that use transistors for input and for output. The term TTL is often used in reference to the mapping between logic states and voltage levels used by TTL logic gates. 5V TTL levels typically map input voltages between -0.3 V and 0.8 V to logic level 0, and input voltages between 2.0 V and 5.3 V to logic level 1. At the circuit outputs, a logic level 1 maps to a voltage between 2.4 V and 5.3 V, while a logic level 0 maps to a voltage between 0 and 0.4 V.

Twin-lead - a low-cost transmission line used to connect television receivers to aerials (receive antennas) before coaxial cable became popular in homes. Twin-lead is a flat cable made with two stranded conductors spaced to create a nominal 300Ω characteristic impedance. The conductors are molded into weather-resistant plastic. Twin-lead is not shielded.

x86 - A broad class of microprocessors based upon the 8086 microprocessor, including the 80186, 80286, 80386, 80486, and Pentium™ processors. Intel Corporation manufactured these processors, and holds the trademark as noted. The term x86 is also used to refer to similar microprocessors built my other microchip manufacturers, such as Cyrix.

XOR - see Exclusive-OR.

Appendix C. Control Switches

The system provided three banks of single-pole single-throw DIP switches, for setting the machine state. Each DIP switch contains eight individual switches. The meaning of each bit is shown in the following lists. The name shown after the bit number is the input control bit name shown on the system schematics. In practice, exactly one pseudo-random generator chain length and one divide-by-n assignment should be selected at any time. The output of the divide-by-n counter can be used as a modulation source directly, and also sets the clock rate of the pseudo-random noise generator. The prime 66.66 and 40 MHz clocks originate from separate crystal oscillators, and therefore there is no phase correlation between them.

The switches may be identified in Figure 4.5. The bits are numbered with the high order bit toward the top of the picture and low order bits toward the bottom of the picture. When the right side of an individual switch is pressed down, the bit is designated to be at the logic 1 or true state. Switch bank 1 is furthest left in the picture. Of the two switch banks on the right of the picture, the upper is switch bank 2, and the lower is switch bank 3.

Switch Bank 1: Input Control.

Bit 7: Master33. When true, the main clock will run at 33.333 MHz. When false, the main clock speed is 20 MHz.

Bit 6: Noise66. When true, the input to the divide-by-n counter is a 66.666 MHz clock wave. When false, the input is a 40 MHz clock wave.

Bit 5: Unused.

Bit 4: Unused.

Bit 3: Unused.

Bit 2: Use External. When set true, the signal from an external pin is selected as the Modulation Signal. When false, the output of the divide-by-n counter is selected. The setting of Switch Bank 3 bit 1 (UseWide) overrides this setting.

Bit 1: NZ Clear. This switch resets an error state indicator within the pseudo-random noise generator. It does not affect any other system operation and is provided for diagnostics only.

Bit 0: Disable outputs. When true, the second pair of flip-flops within the modulator are held in a reset state, but all other high-speed switching within the system continues. This is used to distinguish noise emissions on the output pins from other noise within the system.

Switch Bank 2: Divisor Settings.

Bit 7: Take1. When true, the divisor output frequency is the same as the input frequency.

Bit 6: Take2. When true, the divisor output frequency is one half of the input frequency.

Bit 5: Take4. When true, the divisor output frequency is one quarter of the input frequency.

Bit 4: Take8. When true, the divisor output frequency is one eighth of the input frequency.

Bit 3: Take16. When true, the divisor output frequency is one sixteenth of the input frequency.

Bit 2: Take32. When true, the divisor output frequency is one thirty-second of the input frequency.

Bit 1: Unused.

Bit 0: Unused.

Switch Bank 3: Pseudo-Random Signal Generator Settings

Bit 7: N3. Sets pseudo-random generator for a 3 bit chain.

Bit 6: N4. Sets pseudo-random generator for a 4 bit chain.

Bit 5: N6. Sets pseudo-random generator for a 6 bit chain.

Bit 4: N10. Sets pseudo-random generator for a 10 bit chain.

Bit 3: N15. Sets pseudo-random generator for a 15 bit chain.

Bit 2: N20. Sets pseudo-random generator for a 20 bit chain.

Bit 1: UseWide. When true, the Modulating Signal is taken from the pseudo-random noise generator. When false, the Modulating Signal will be taken from either the external modulation input or the divide-by-n counter output, as determined by Switch Bank 1 bit 2.

Bit 0: Unmodulate. When true, the modulation source selected by other switch settings is overridden, and a low state is applied to the Modulating Signal input of the modulator.

Referring again to the photograph in Figure 4.5: Switch Bank 1 has bits 7 and 6 set true; Switch Bank 2 has bit 7 set true, and Switch Bank 3 has bits 4 and 1 set true. These settings would create a 33.33 MHz clock with pseudo-random modulation. The pseudo-random signal generator would be running at the 66.67 MHz rate, using a 10-bit chain. This switch setting was used to create the spectral data reported in Section 7.3, Design Scenario #2.