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Title: FABRICATION AND CHARACTERIZATION OF MODULATION DOPED FIELD EFFECT TRANSISTORS FOR QUANTUM WAVEGUIDE STRUCTURES.

Abstract approved: Redacted for Privacy
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Split and normal gate AlGaAs/GaAs MODFETs were fabricated along with the ohmic test structures and the Hall bar geometries. The DC characteristics of normal gate transistors were evaluated at room temperature and at 77K and the threshold voltages were extracted from the measurements and compared to the theoretical results. The performance of normal gate transistors was reasonable. The sheet carrier density and the mobility extracted from Hall measurements using the Hall bar geometry showed increase of carrier density with increasing gate voltage and an increase of mobility with increasing carrier density. The contact resistance obtained from the ohmic test structure was high and not uniform within the sample.

Fabrication and Characterization of Modulation Doped Field Effect Transistors for Quantum Waveguide Structures

by

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FABRICATION AND CHARACTERIZATION OF MODULATION DOPED FIELD EFFECT TRANSISTORS FOR QUANTUM WAVEGUIDE STRUCTURES

1. INTRODUCTION

1.1 The Modulation Doped Field Effect Transistor

The modulation doped field effect transistor (MODFET); also the called the selectively doped heterojunction transistor (SDHT), the high electron mobility transistor (HEMT), and the two dimensional electron gas field effect transistor (TEGFET), is a heterojunction device which utilizes the high mobility and high velocity of a two-dimensional electron gas (2DEG) formed at a heterointerface, for example between $Al_xGa_{1-x}As$ and GaAs.

It was Anderson (1960)[1] who first predicted the accumulation layer of carriers at the interface of a heterojunction. Later, Esaki and Tsu (1969)[2] suggested the spatial separation of impurities from the interface to enhance the mobility of the 2DEG at the heterointerface. The first observation of enhanced electron mobility of the 2DEG was made by Dingle et al. (1978)[3] and later Mimura and coworkers (1980)[4] fabricated the first heterojunction field effect transistor utilizing the mobility enhancement of the 2DEG. Since then, considerable progress has been achieved in improving the performance and increasing the integration scale for MODFETs.

1.2 Structure of the MODFET

MODFET structures with enhanced mobility may be grown in several ways; liquid phase epitaxy (LPE), metal organic chemical vapor deposition (MOCVD), and molecular beam epitaxy (MBE). The basic MODFET structure, illustrated in figure 1.1, has four important layers, starting from the top:

A. The GaAs cap layer which passivates the $Al_xGa_{1-x}As$ surface and is heavily doped to reduce the parasitic resistances and facilitate ohmic contact to the 2DEG.

B. The doped $Al_xGa_{1-x}As$ or donor later which supplies electrons for channel conduction and acts as a high quality dielectric material between the gate and the channel.

C. The undoped $Al_xGa_{1-x}As$ or the spacer which separates the channel electrons from the impurities in the donor layer.

D. The unintentionally doped GaAs buffer layer which is the active layer in which the 2DEG resides.

Source and drain contacts are typically formed by deposition and alloying of the Ni/Au/Ge layers. A gate region is formed by a thick film of Au for a Schottky-gate metalization.

1.3 Quantum Waveguides

Recently there has been considerable research in nanometer scale semiconductor devices in which the wave nature of electrons is fundamental to the device performance. Quantum effects become more pronounced as the device dimensions are reduced, since the associated quantized energy level separations are

increased. Transistor structures based on quantum interference phenomena have been proposed (Sols et al. 1989)[5] as well as structures exhibiting negative differential resistance effects (Weisshaar et al. 1990)[6]. The MODFET structure is well suited for fabricating quantum effect devices because elastic scattering is minimized due to the separation of electrons from the ionized donors through modulation doping. Furthermore, the energy levels are already quantized in one direction due to vertical confinement. Thus electrons at the interface are able to move merely along the xy-plane (Figure 1.1). With an ultra-small structure (Figure 1.2) patterned at the surface, the depletion region due to the electrostatic gate potential confines carriers to move in only one direction.

1.4 Present Goal

The objectives of this study were to design and fabricate the split-gate MODFET structures at the Oregon State University facilities for fabrication of quantum interference devices using the electron beam lithography system at University of Oregon. The steps performed in this study included designing of mask set, developing the compatible process steps of MODFET technology, fabricating MODFET structures with and without split gate, and characterizing the normal gate MODFETs by evaluating the DC characteristics and the contact resistance, and determining the mobility and the sheet carrier concentration. The detail of these activities is discussed in chapter 3. Fabrication of quantum waveguide structures and testing which are still on-going procedures are conducted at University of Oregon.

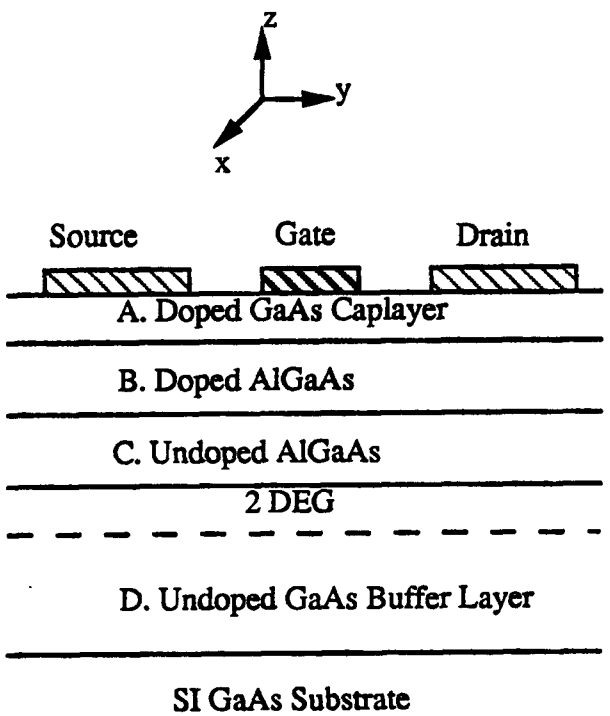


Figure 1.1 Cross section of a typical modulation doped structure.

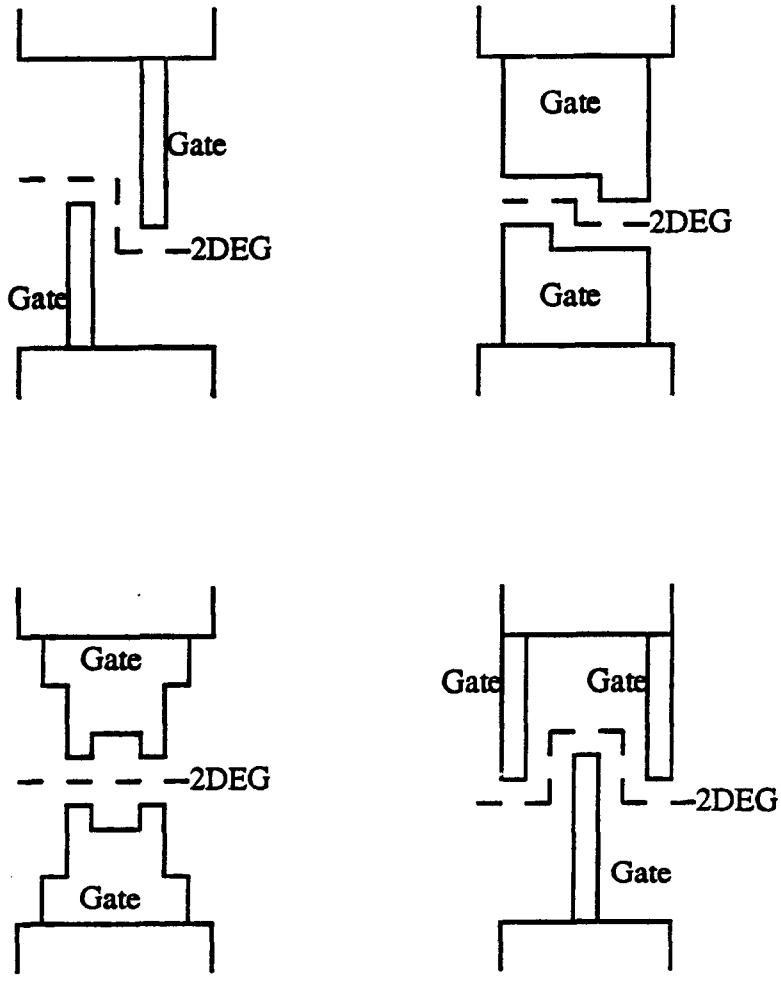


Figure 1.2 Examples of quantum waveguide structure.

2. THEORY

Since the current-voltage (I-V) relationship and the transconductance are the main characteristics of the transistors in this study, the derivation of the I-V characteristics of the MODFET is discussed briefly, starting from the band diagram of the heterojunction.

2.1 Energy Band Diagram

A heterojunction is a junction formed between two dissimilar semiconductors. When a high bandgap semiconductor ($Al_xGa_{1-x}As$) is grown on a lower bandgap semiconductor (GaAs), the difference of the two bandgaps (ΔEg) appears at the conduction band edge (67% of ΔEg) and at the valence band edge (33% of ΔEg) (Kuech et al., 1987)[7] as ΔEc and ΔEv, respectively (Fig 2.1). The conduction band offset is ideally given by the difference between the electron affinities of the two materials (Anderson, 1960)[1]. However, this model gives the conduction bandgap difference (ΔEc) of 88% because it does not include the effect of the dipole layer, caused by the surface states at the interface, which also contributes to the discontinuity in the conduction band (Tersoff, 1984)[8].

Due to the difference in the conduction band minima, a transfer of electrons from the doped to the undoped side occurs so as to align the Fermi level in equilibrium. This transfer causes the accumulation of electrons in the GaAs which forms a 2DEG at the interface due to quantum mechanical size quantization. Carrier confinement occurs over width on the order of a few tens of $\mathring{A}$ resulting in the formation of discrete energy levels in the direction perpendicular to the surface

called subbands. The 2DEG in the high purity GaAs and the ionized donors in the $Al_xGa_{1-x}As$ create a strong internal electric field which in turn produces pronounced band bending, resulting in a so called quantum well in the GaAs, as shown in Figure 2.2 for a single period modulation doped AlGaAs/GaAs heterojunction.

An incomplete electron transfer to the quantum well channel occurs when the doped AlGaAs layer is not fully depleted. In MODFETs, this effect is referred to as the parasitic MESFET effect because of the similarity to the MESFET when its channel becomes undepleted. In MODFETs, electron states in both the channel and the barrier will be occupied. Thus the conductivity will consist of both parallel conduction in the channel and barrier which degrades device performance for large gate biases, due to the relatively low mobility of doped $Al_xGa_{1-x}As$; typically <1000 cm^2/v-sec (Chand et al., 1984)[9].

2.2 Current-Voltage Relationship

In order to derive the current-voltage relationship, the interface carrier density should be determined. For the AlGaAs/GaAs heterojunction, the two lowest subbands accounts for 80-90% of sheet charge density (Yoshida, 1986)[10], and the charge accumulated in the potential well (n_s) can be found as follows:

$$n_s = \frac{DkT}{q} \ln\{(1 + \exp[\frac{q(E_{Fi} - E_0)}{kT}])(1 + \exp[\frac{q(E_{Fi} - E_1)}{kT}])\} \qquad (2.1)$$

where D = density of available energy states

E_0 = energy level of the first subband

E_1 = energy level of the second subband

E_{Fi} = Fermi energy level at the interface relative to the conduction band edge

With a Schottky gate on the $Al_xGa_{1-x}As$ (Figure 2.3), the expression relating n_s to the applied gate bias is derived using the linearization of the Fermi level; $\frac{E_{Fi}}{q} = \frac{\Delta E_{F0}(T)}{q} + an_s$ where $a = 0.125 \times 10^{-16}$ Vm^2 and $\Delta E_{F0} = 0$ at 300 K and $\Delta E_{F0} = 0.025$ at 77K and below (Drummond et al, 1981)[11] , and recognizing the variation of Fermi level with n_s. This assumption results in the charge control model

$$Q_s = qn_s = \frac{\varepsilon_2}{(d+\Delta d)}(V_G - V_{off}) \tag{2.2}$$

where $d = d_d + d_i$

$\Delta d = \varepsilon_2 a / q$ = 2DEG channel width

V_G = applied gate voltage

$$V_{off} = \Phi_b - \Delta E_c - V_{P2} + \frac{\Delta E_{F0}(T)}{q} \tag{2.3}$$

d_d is the donor layer thickness, d_i is the spacer thickness, ε_2 is the dielectric constant of the $Al_xGa_{1-x}As$, V_{off} is the threshold voltage of the 2DEG, Φ_b is the Schottky barrier height, and $V_{P2} = (qN_d d_d^2)/(2\varepsilon_2)$ is the doped $Al_xGa_{1-x}As$ pinch off voltage.

From the charge control model, the current-voltage relation may be obtained using a two-piece model. Assuming normal operating condition; the $Al_xGa_{1-x}As$ layer is completely depleted and the electrons are confined to the interface. The drain voltage is applied in addition to the gate voltage causing the potential distribution to vary from zero at the source to V_D' at the drain (Figure 2.4). Assuming the gradual channel approximation, the charge is given by

$$Q_s(x) = \frac{\varepsilon_2}{(d+\Delta d)} (V_G - V_c(x) - V_{off}) \tag{2.4}$$

where $V_c(x)$ is potential varying with distance from the drain to the source. From the total charge given, the drain current can be derived as follows.

$$I_D = Q_s(x)\, Z\, v(x) \tag{2.5}$$

where Z = the gate width

$v(x)$ = electron drift velocity

From the two-piece model and the integration at the drain voltages less than the saturation voltage, the current-voltage characteristic and the linear transconductance are given by

$$I_D = \frac{\varepsilon_2 \mu Z}{(d+\Delta d)L} \left\{ (V_G - V_{off})V_D - \frac{V_D^2}{2} \right\} \tag{2.6}$$

$$Gm = \frac{dI_D}{dV_G} = \frac{\varepsilon_2 \mu Z V_D}{(d+\Delta d)L} \tag{2.7}$$

where μ is the mobility and L is channel length. If saturation occurs by pinchoff, V_G - Voff - V_D = 0, and the saturation current and transconductance are

$$I_D = \frac{\varepsilon_2 \mu Z}{2(d+\Delta d)L}(V_G - V_{off})^2 \tag{2.8}$$

$$Gm = \frac{dI_D}{dV_G} = \frac{\varepsilon_2 \mu Z}{(d+\Delta d)L}(V_G - V_{off}) \tag{2.9}$$

If saturation is due to velocity saturation, the transconductance is given by (Shur, 1987)[12].

$$Gm = \frac{dI_D}{dV_G} = \frac{\beta V_G'}{\sqrt{1+\left[\frac{V_G'}{(V_s L/\mu)}\right]^2}} \tag{2.10}$$

where $\beta = \frac{\varepsilon_2 \mu Z}{(d+\Delta d)L}$

$V_G' = V_G$ - Voff

V_s = velocity saturation

which reduces to equation 2.9 as L --> ∞. In deriving equations (2.6), (2.7), (2.8), (2.9), and (2.10) the series resistance is omitted. With the series resistance included, the current voltage relationship and the transconductance equations are more complex (Shur, 1987)[12].

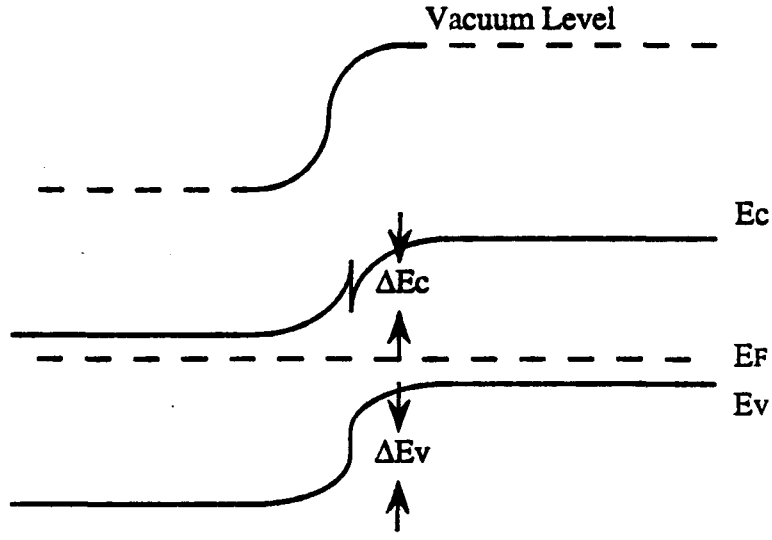


Figure 2.1 Band diagram of n-type AlGaAs and p-type GaAs heterojunction.

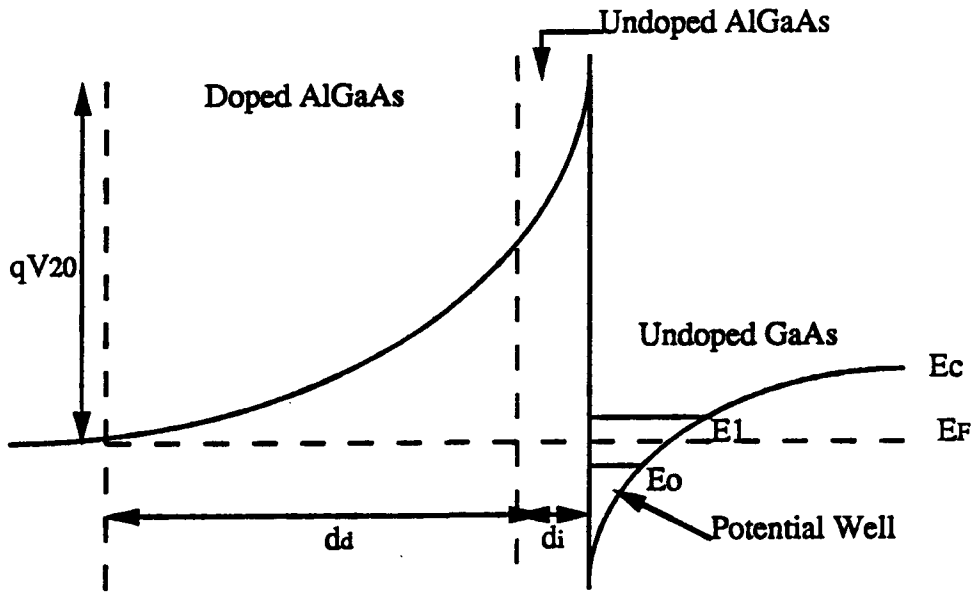


Figure 2.2 Band bending of the AlGaAs/GaAs heterojunction.

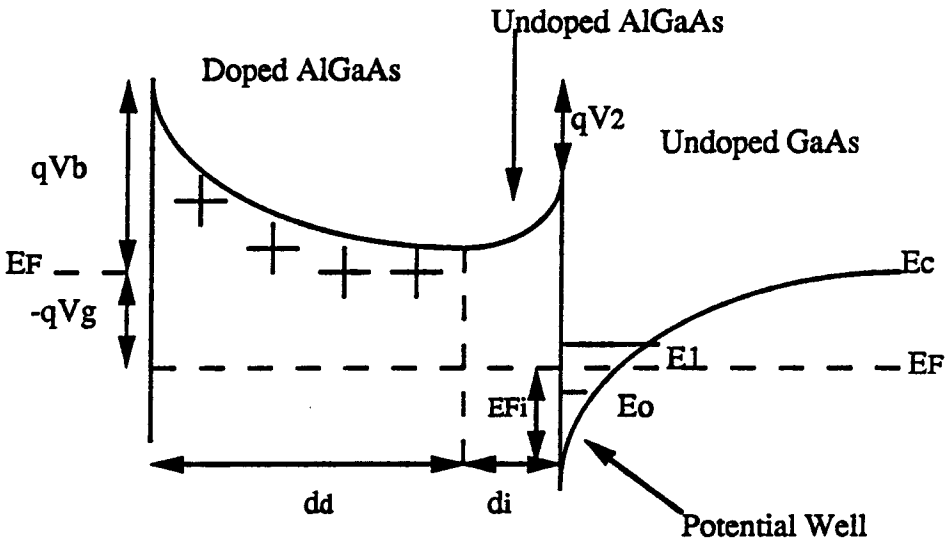


Figure 2.3 Conduction band edge diagram of a singleperiod modulation doped structure with a Schottky barrier deposited on the AlGaAs layer.

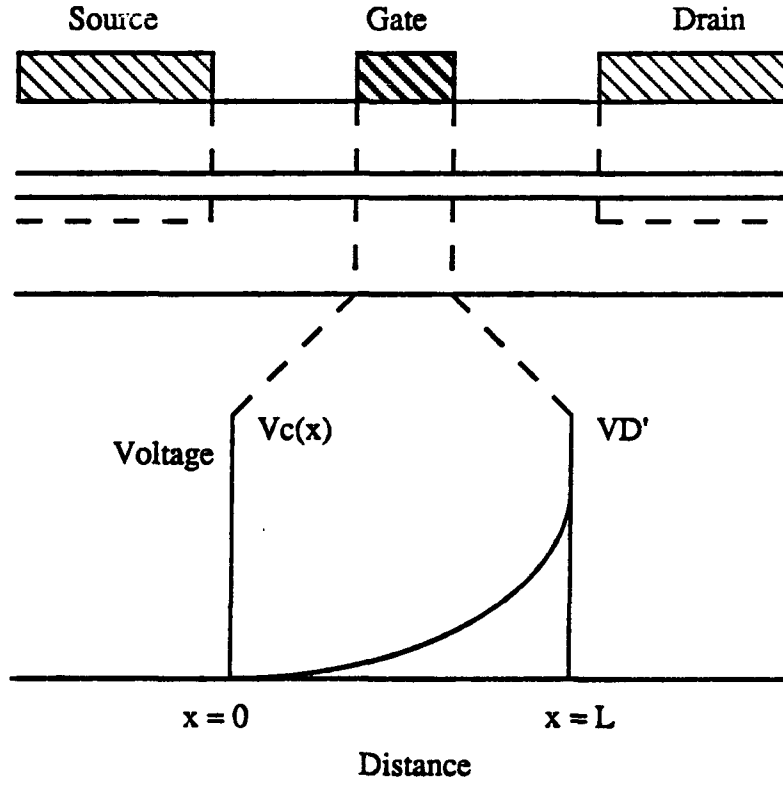


Figure 2.4 Channel potential vs distance along the gate for a MODFET.

3. DEVICE FABRICATION AND CHARACTERIZATION

Since the MODFET structures with split gate were intended for fabricating quantum effect devices, the structures should exhibit extremely low elastic scattering rate, and high carrier density at the interface. These qualities can be accomplished by means of sample growth as explained in the following section.

3.1 Layer Growth

Most samples used in the present study were grown, on <100> oriented SI GaAs substrates, in the OSU solid state laboratory by Jennifer Lary and Don Schulte using the molecular beam epitaxy (MBE) facility, while some were obtained from George Pubanz of Tektronix Laboratories, in Beaverton, Oregon. The substrate temperature during growth was 585°C. The structure (Figure 3.1) consists of one micron of unintentionally doped GaAs buffer layer which was grown for 60 minutes. With the Ga flux reduced to 0.73 monolayer/sec, the Al flux kept at 0.27 monolayer/sec, the undoped $Al_xGa_{1-x}As$ (x=0.27) was grown for 0.9 minute to create approximately 150 Å thick spacer layer. Thick spacer was required in this study so as to effectively separate the ionized impurity donors from the electrons in the channel, thus minimized the elastic scattering rate. Then a 400 Å thick of Si doped $Al_xGa_{1-x}As$ (x=0.27) was grown for 2.4 minutes with a high doping concentration of $1x10^{18}$ cm^{-3} to obtain high carrier density at the interface. Finally, the surface was covered with a 150 Å of GaAs cap layer which was Si doped with a concentration of $1.4x10^{18}$ cm^{-3}.

3.2 Mask Set

Four mask levels, containing the patterns of windows which are transferred to the surface of the sample, were designed for mesa isolation, ohmic contact deposition, oxide passivation, and metalization. First, the masks were designed using the Mentor Graphics tools on the APOLLO system. The minimum feature size used in the design was 5 microns in order to facilitate the limitation of the mask aligner which has resolution of 2 microns when fully optimized. The pattern consisted of four types of devices. The first two types are split gate and normal gate transistors (Figure 3.2) with gate lengths and widths of 10 and 50 microns, respectively, and a spacing of 10 microns for the split gate transistors. The size of source/drain is 50x50 microns. Electrical characterization was performed primarily on the normal gate transistors as discussed in the next section. The split gate device will be used for quantum waveguide studies in which the ultra-small structures (Figure 1.2) are patterned onto the spacing between gates by means of electron beam lithography (conducted at the Department of Physics, University of Oregon, Eugene). The third type of device included in the mask set was the ohmic test structure which was used to determine the quality of the ohmic contacts by evaluating the contact resistance. This structure was composed of six contacts as shown in Figure 3.3, each with a width and length of 100 and 50 microns, respectively, and the spacing between adjacent contacts were 5, 10, 15, 20, and 25 microns. The last device was Hall bar geometry (Figure 3.4), used to determine the mobility and the sheet carrier density, with source/drain contacts of 40x40 microns, gate length and width of 570 and 50 microns, respectively, the total length

of 750 microns, and a distance of 200 microns between the centers of the two adjacent arms. Devices were arranged on the sample as shown in Figure 3.5.

Each level designed on the APOLLO computer was then transferred onto the rubylith sheets, using the Hewlett-Packard 7586B plotter,with a magnification of 100X. This enlargement allowed an easy peeling of the ruby sheets especially when the 5 micron minimum feature size was realized. The rubylith pattern was then reduced by 2X onto the mylars at the reprographic center, CH_2M Hill. Then the patterns on mylars were transferred onto the glassplates with further reduction of 25X. The mask aligner at this laboratory has reduction of 2X, thus the pattern on a glassplate was marked onto the sample with the original size as initially designed on the computer.

3.3 Processing Procedures

The processing procedures used for the various mask steps above are as follows. Initially, the samples were cleaned in Trichloroethylene (TCE), followed by Acetone, Methanol, DI water, and blown dry with N_2 gas.

3.3.1 Mesa Isolation

The devices were isolated from one another by a mesa etch technique in which a wet chemical etch was used to remove the top surface through to the buffer layer. The process flow that was used follows:

1 Spin HMDS *(Hexamethyldisilazane) then positive photoresist (PR) at 3000 rpm for 20 seconds.

2 Soft bake at 60°C for 5 minutes**.

3 Expose to UV light with the light integrator (LI) set at 9.5.

4 Develop using KODAK developer : DI water (1 : 3.5), then rinse with DI water and N_2 gas blow dry.

5 Hard bake at 120°C for 5 minutes***.

6 Etch using H_3PO_4 : H_2O_2 : DI H_2O (3 : 1 : 25) for 40 seconds to remove approximate 800 Å .

7 Strip off the PR and clean using Acetone, Methanol, DI water, and blow dry.

* HMDS provides better attachment of PR to the sample surface.

** Soft bake is used to improve adhesion and remove solvent from the PR.

*** Hard bake is to harden the PR and improve adhesion to the substrate.

3.3.2 Ohmic Contact Deposition

The ohmic source/drain contacts were formed by vacuum deposition of Au-Ge/Au (Au-Ge is the eutectic composition with 88% wt. Au and 12% wt. Ge) using a lift-off technique:

1 Spin HMDS and positive PR at 3000 rpm for 20 seconds.

2 Soft bake at 60°C for 5 minutes.

3 Soak in Chlorobenzene* for 4 minutes and rinse with DI water then blow dry.

4 Expose to UV light (LI = 9.5).

5 Develop using summa developer (SDP-11)**, and rinse with DI water and blow dry.

6 Drop HCL*** on the sample for 30 seconds, rinse with DI water and blow dry.

7 Evaporate Au-Ge/Au (Au-Ge first and follow with Au). The thickness of Au-Ge and Au are approximately 1200 and 1400 Å, respectively.

8 Soak in Acetone to lift off the unwanted Au until the pattern is complete, then rinse with DI water and blow dry.

9 Alloy at 450°C for 5 minutes in a forming gas environment.

* Chlorobenzene helps to create a lip at the edge of the PR (Figure 3.6) after developing thus providing better lift-off of metal.

** SDP-11 also cleans the surface of the sample thus it is used whenever metal deposition is followed.

*** HCL removes the native oxide on the surface, thus this improves the quality of the ohmic contact.

3.3.3 Oxide Etch

After alloying, the samples were cleaned with Acetone, Methanol, DI water and then blown dry. Approximately 1000 Å of SiO_2 was deposited on the sample using the VEECO Sputter system with a quarts target. The oxide was then etched at the device windows using the same procedure as the mesa etch except replacing the etchant with Buffered HF and etching for 30 seconds.

3.3.4 Metalization

A lift-off technique was again utilized for this step. The procedure was the same as for the ohmic contact deposition with the exception that the HCL procedure was omitted, and Ti (0.05 gm.) and Au (0.25 gm.) were used in the evaporation process. The thicknesses of Ti and Au were approximately 80 and 1900 Å, respectively.

3.4 Characterization

3.4.1 MODFETs

The DC characteristics including current-voltage relationship (I-V), transconductance (Gm), and saturation current were measured using the HP 4145B parameter analyzer. The measurements were conducted at room temperature and at 77K in the absence of light.

3.4.2 Ohmic Test Structure

In this structure, the resistances between each two adjacent contacts for different spacing lengths were measured using also the HP 4145B analyzer. The measurements were performed in the dark at room temperature.

3.4.3 Hall Bar Geometry

A Hall effect technique was used for this structure. The diagram of measurement system is shown in Figure 3.7. A constant current was applied between source and drain (A1-A2), and the magnetic field was applied in the direction perpendicular to the device (x-direction). For each applied gate voltage, the voltages V_X^+ (B1-D1) and V_H^+ (C1-C2) for the magnetic field in the +x-direction, and V_X^-(B1-D1) and V_H^-(C1-C2) for the magnetic field in the -x-direction were measured. V_H was obtained from $(V_H^+ - V_H^-)/2$ to eliminate the offset voltage due to misalignment between C1 and C2, and V_X was the average of the V_X^+ and V_X^-.

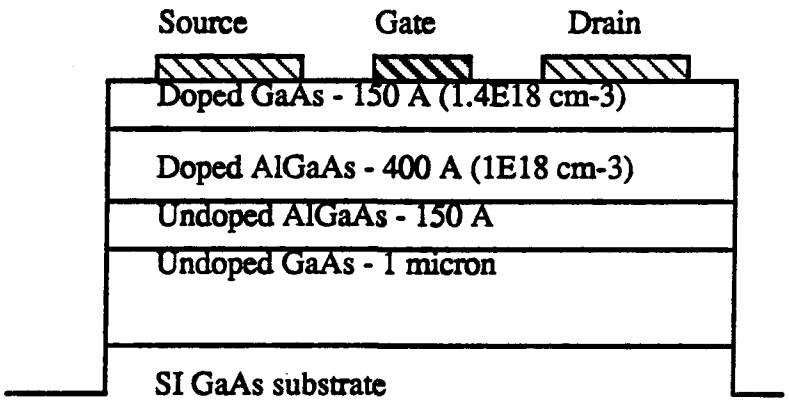


Figure 3.1 Structure of modulation doped layer in this study.

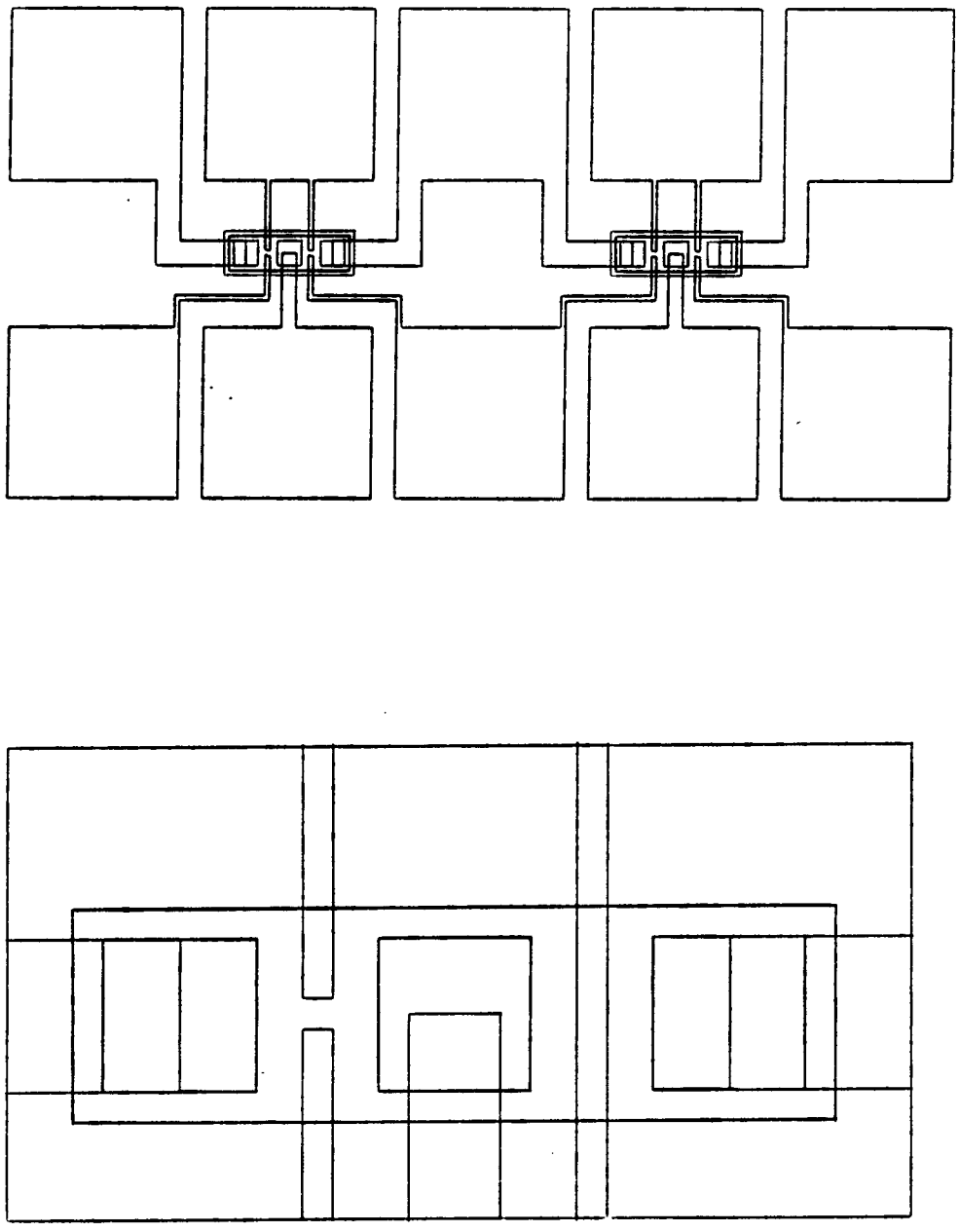


Figure 3.2 Diagram of split and normal gate transistors.

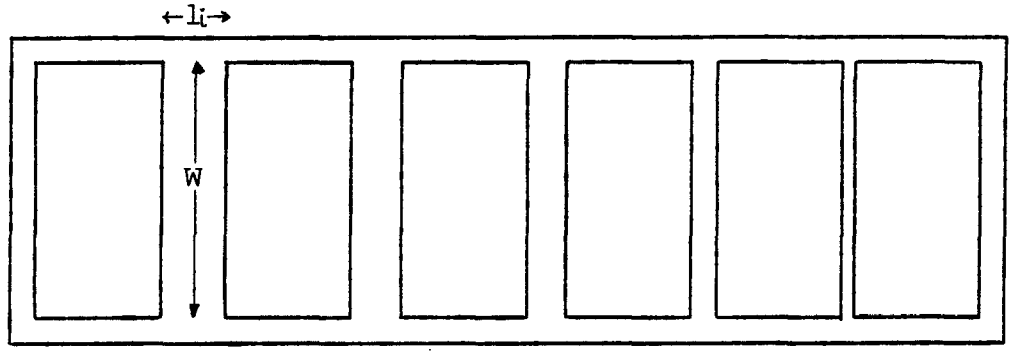


Figure 3.3 Diagram of ohmic test structure.

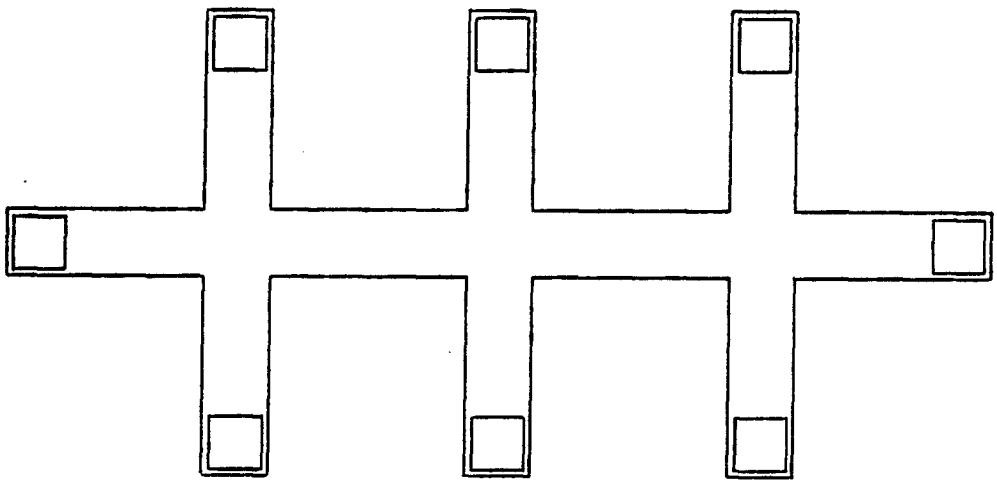


Figure 3.4 Diagram of Hall bar geometry.

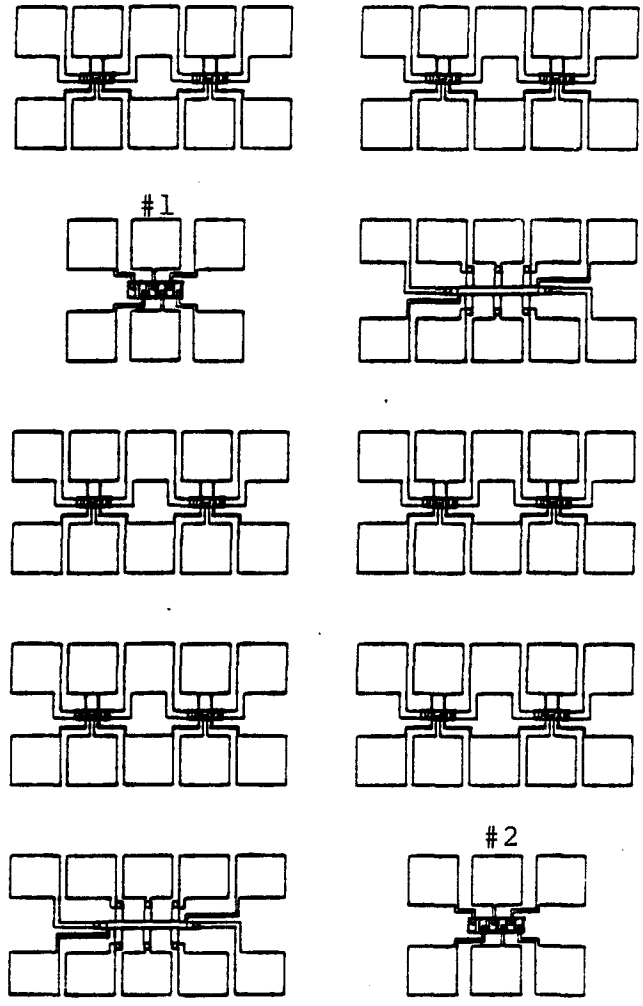


Figure 3.5 Diagram of device arrangement on the sample.

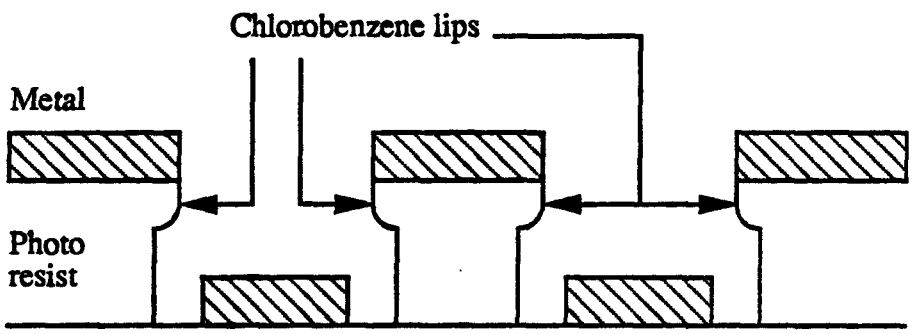


Figure 3.6 Chlorobenzene treated resist profile with lip extending beyond base of resist for good lift-off.

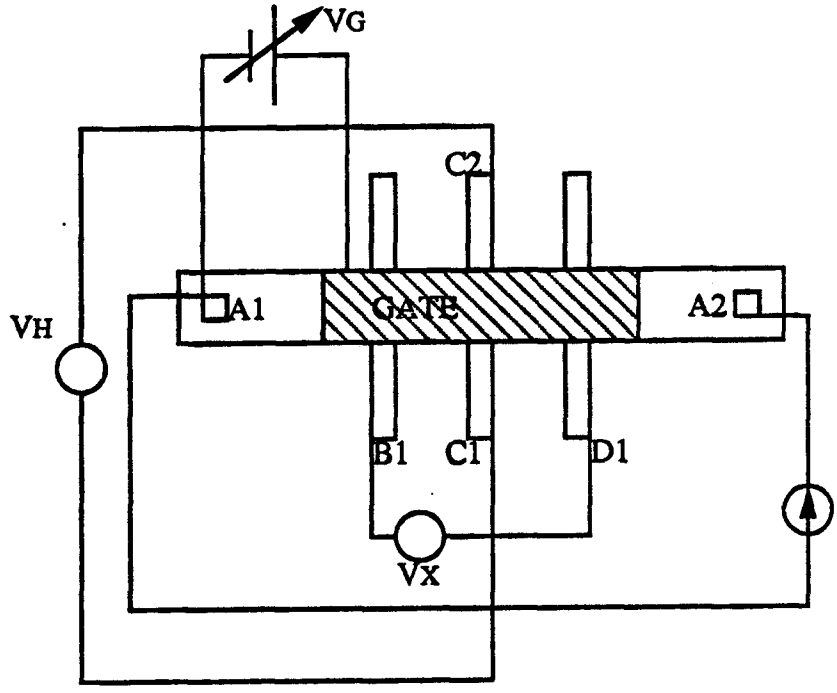


Figure 3.7 Diagram of Hall measurement system

4. RESULTS

4.1 Interface Carrier Density (n_s) and Mobility (μ)

From the Hall effect measurement, the interface carrier densities (N_S) and mobilities (μ) are calculated as follows (Smith, 1968)[13]:

$$n_s = \frac{IBr}{qV_H} \tag{4.1}$$

$$\mu = \frac{L_x V_H}{WV_X Br} \tag{4.2}$$

where I is the constant current applied which was selected to be 2μA to assure operation in the linear region, B is the magnetic field (0.32 T), r is the numerical factor depending on type of scattering and it is equal to 1 at 77K, L_x is the distance across which V_X was measured (400 microns), W is the width of the gate (50 microns), and V_H and V_X were calculated as mention previously in chapter 3.4.3.

The plot of sheet carrier density (N_S) versus gate voltage (V_G) is shown in Figure 4.1. n_s increased with increasing gate voltage for both room temperature and at 77K except the curve leveled off at high gate voltages at 77K. The theoretical results (Figure 4.2) of a self consistent solution to Schroedingers and Poisson's equations (Lary, 1990)[14] are quite different from Hall measurement results. First, the rate of the increase of n_s with increasing V_G from the experiment is not as steep as obtained from the theory. Furthermore, n_s at 77K was higher than that at room temperature. This is also contradictory to the results from the experiment by Hirakawa and Sakaki (1986)[15]. Due to the difficulty encountered when measuring with the negative gate voltages applied, most results were obtained

from the measurement in the positive gate voltage region. Thus one possible explanation is that the doped $Al_xGa_{1-x}As$ layer was partially undepleted, resulting in the existent of carriers in the $Al_xGa_{1-x}As$ region (3DEG). A qualitative sketch of the interface carrier density in a MODFET as a function of the gate voltage is shown in Figure 4.3. The parasitic MESFET is formed by the gate and the doped $Al_xGa_{1-x}As$ layer when the gate voltage is larger than (Shur, 1987)[12]

$$V_{t3} = V_{off} + (V_{PO})_{2D} \tag{4.3}$$

where

$$(V_{PO})_{2D} = \frac{qN_{so}(d+\Delta d)}{\varepsilon_2} \tag{4.4}$$

is the pinchoff voltage of the 2DEG and N_{so} is the maximum equilibrium 2DEG concentration given by the relationship in eq. 2.1. If the gate voltages are larger than the threshold voltage (V_{t3}) for the turn on of the parasitic MESFET, the carrier concentration obtained from Hall measurement will represent a combination of the 2DEG and the 3DEG which in a two layer model is given by (Ziman, 1979)[16]

$$n_{eff} = \frac{(\mu_{2D}n_{2D}+\mu_{3D}n_{3D})^2}{\mu_{2D}^2 n_{2D}+\mu_{3D}^2 n_{3D}} \tag{4.5}$$

The plot of mobility (μ) versus n_s is shown in Figures 4.4 for both room temperature and 77K. In both cases, μ increased with increasing n_s due to the screening effect of the electrons in the channel. The results showed that μ at 77K (range 38,000-66,000 cm^2/v-sec.) was higher than that at room temperature (range 6,900-8,500 cm^2/v-sec.). This is due to the dominance of ionized impurity scattering at low temperature. However, this effect was minimized due to

separation of ionized impurity donors from carriers by the spacer layer, thus higher mobility at low temperature was obtained.

4.2 Contact Resistance

Initially, alloying was done at 420°C for 5 minutes and the contacts showed non-ohmic characteristic (Figure 4.5a). After the alloy temperature was raised to 450°C, ohmic characteristic (Figure 4.5b) was constantly reproducible. This indicates the importance of temperature on the alloying process.

The measurements from five ohmic test structures from three samples are shown in Table 4.1. For each li, the measured resistances from five structures was averaged and then used to extracted the contact resistance which is defined by

$$R_i = 2\frac{R_c}{w} + \frac{R_s}{w} l_i \qquad (4.6)$$

where R_i is the resistance between the two contacts separated by l_i, R_s is the sheet resistance, and w is the width of the contact. By applying linear regression method to the data (average values) in Table 4.1, R_c and R_s were found to be 1.42 and 1.98×10^3 ohm.cm, respectively. Compared to the contact resistance of 0.05 ohm.cm obtained from the MODFETs fabricated by Triquint Inc (Beaverton, OR) (Chang, 1989)[17], the R_c obtained in this study was somewhat high.

A sample contained two ohmic test structures designed identically except for their placement on the chip; Structure #1 and #2 are shown in Figure 3.3. Linear regression was applied individually to data from structure #1 and #2 for sample A and B (Table 4.1) and R_c was found to be 1.14 and 1.98 ohm.cm for structure #1 and #2, respectively, for sample A. For sample B, R_c was 0.95 and 1.93 ohm.cm

for structure #1 and #2, respectively. These results show a non-uniform contact resistance within a sample and between samples.

The variation of the contact resistance may be due to several factors. First, since structure #1 from both sample A and B showed less R_C, it is possible that the distance which the sample was placed from the metal boats in the vacuum evaporator during ohmic contact deposition could effect the contact resistance because during evaporation, the sample was constantly oriented such that the structure #1 was closer to the metal boats. The closer the structure to the metal sources, the more the metal; in this case Au-Ge, deposited onto the structure and this probably resulted in better R_C. The other factor may be due to systematic variation in the l_i distances due to mask or photolithography variation.

4.3 Transistor Performance

4.3.1 Drain Current (I_D)

The I-V curves are shown in Figures 4.6 and 4.7 for room temperature and 77K, respectively. The gate voltage was swept from -1 to 1 volt. Since the transistor turns on at the negative gate voltage, this device is a depletion mode device which is desirable for quantum effect devices in order to be able to easily control the lateral dimension of the waveguide structures. The drain current obtained at 77K was higher than that measured at room temperature due to the dependence of the current on mobility (eq. 2.6 and 2.8) which is higher at 77K as shown by the results from Hall measurement.

4.3.2 Transconductance (Gm)

The linear transconductance (Gm) versus the applied gate voltage (V_G) at a fixed drain voltage (V_D) of 0.1 volts is presented in Figures 4.8 and 4.9 for room temperature and 77K, respectively. The maximum transconductance at room temperature was 13.2 ms and it increased to 80 ms at 77K. The saturation transconductance is shown in Figures 4.10 and 4.11 with the peak of 97 and 273 ms for room temperature and 77K, respectively. The peak of the transconductance occurs when the parasitic MESFET in the doped $Al_xGa_{1-x}As$ is turned on. For the structure used in this study, $(V_{PO})_{2D}$ was found to be 0.27 volt. $(V_{PO})_{2D}$ obtained from the measured linear transconductance characteristics (Figures 4.8 and 4.9) were close to the theoretical values.

4.3.3 Saturation Current

The saturation current ($\sqrt{I_D}$) characteristics for various gate voltages at a constant drain voltage of 4 volts are shown in Figures 4.12 and 4.13 for the measurement at room temperature and at 77K, respectively. Since the gate length used for the transistors in this study was quite long, the saturation current was due to the pinchoff not velocity saturation.

4.4 Device Characteristics

The DC device characteristics were used to determine the parameter; the threshold voltage (Voff) which was then compared to the theoretical value. The measured threshold voltages in this experiment were -0.76 and -0.31 volt at room temperature and at 77K, respectively. From eq. 2.3, the threshold voltage depends

on the Schottky barrier height, the conduction band discontinuity, and the doping concentration and the thickness of the doped $Al_xGa_{1-x}As$ layer. From experimental measurements, the Au-Schottky barrier height varies with AlAs mole fraction (x) in the doped $Al_xGa_{1-x}As$ layer and it is approximately 1.19 eV for x=0.27 (Odekirk, 1987)[18]. The conduction band discontinuity which also varies with AlAs mole fraction is estimated to be 0.226 volt for $Al_{.27}Ga_{.73}As$/GaAs interface assuming 67% of the band gap difference on the conduction band. With the doping concentration and the thickness of the doped $Al_xGa_{1-x}As$ layer given in Figure 3.1, Voff were calculated to be -0.21 and -0.18 volt , for room temperature and 77K, respectively, which were in a close agreement with the theoretical values of the self consistent solution to the Schroedingers and Poisson's equations (Lary, 1990)[14] which were -0.21 and -0.13 volt for room temperature and 77K, respectively. The discrepancy between the experimental and the theoretical values may be due to the inaccuracy of the estimated value of the Schottky barrier height, and the conduction band discontinuity.

The measured threshold voltages between the normal and the split gate (with quantum waveguide structure) transistors were compared (Figure 4.14). The threshold voltage of the split gate transistor was more negative. This is because it has to be turned off both vertically and laterally, thus it is more difficult to turn off.

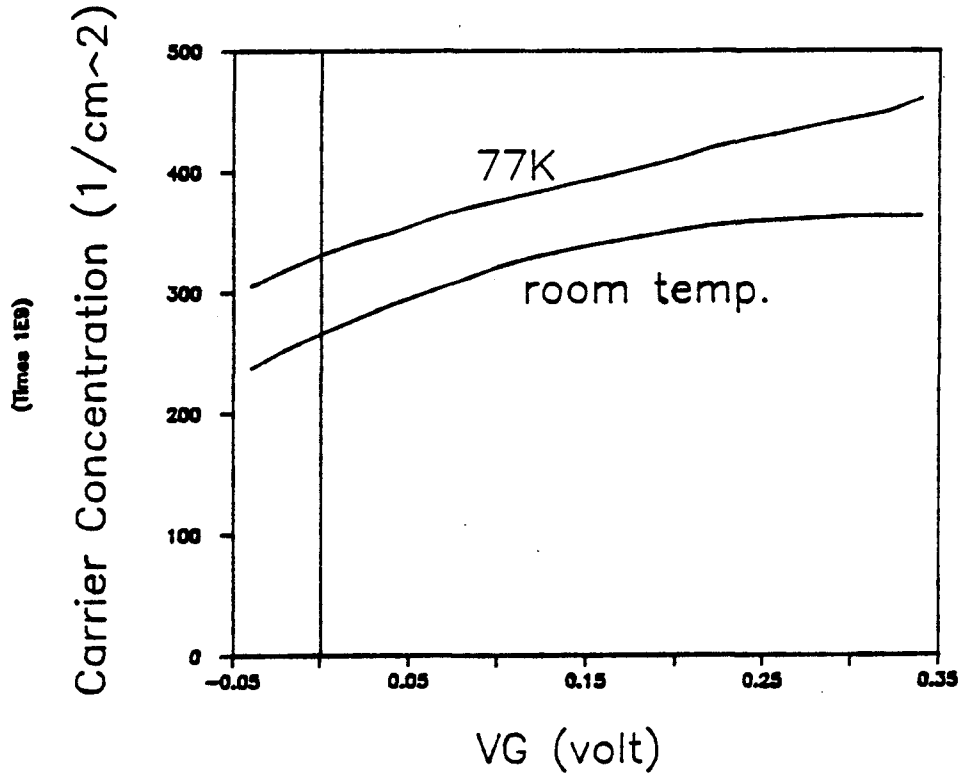


Figure 4.1 Sheet carrier density (n_S) vs gate voltage (V_G) from Hall measurement at room temperature and at 77K.

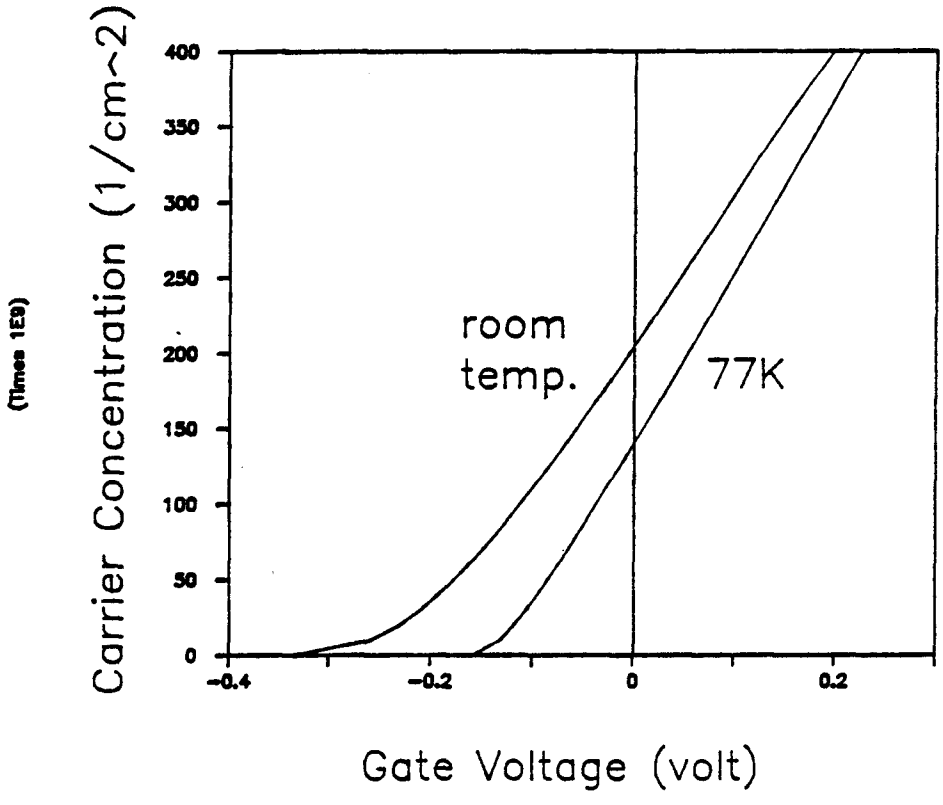


Figure 4.2 Sheet carrier density (n_s) vs gate voltage (V_G) from self consisteent solution to Schroedingers and Poisson's equations.

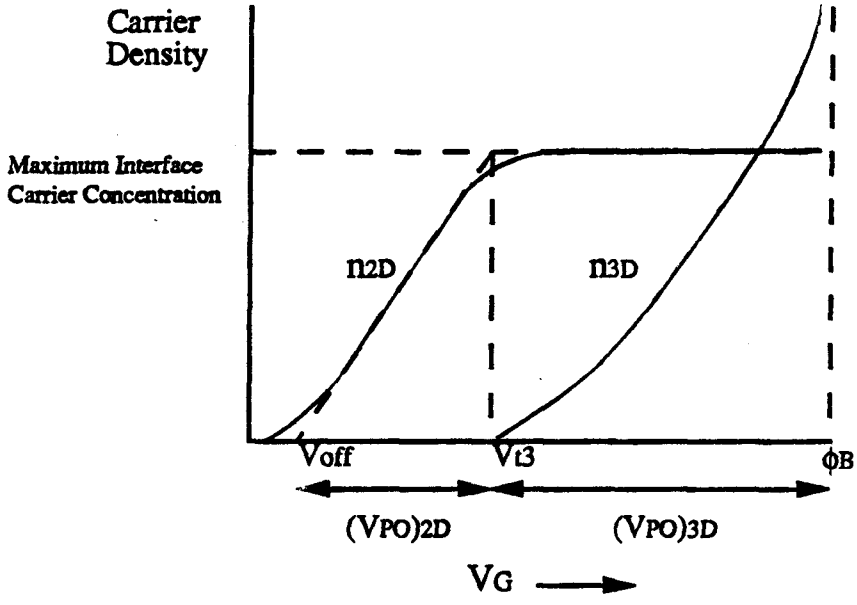


Figure 4.3 Qualitative sketch of interface (n_{2D}) and parasitic MESFET (n_{3D}) carrier density in a MODFET (Shur, 1987)

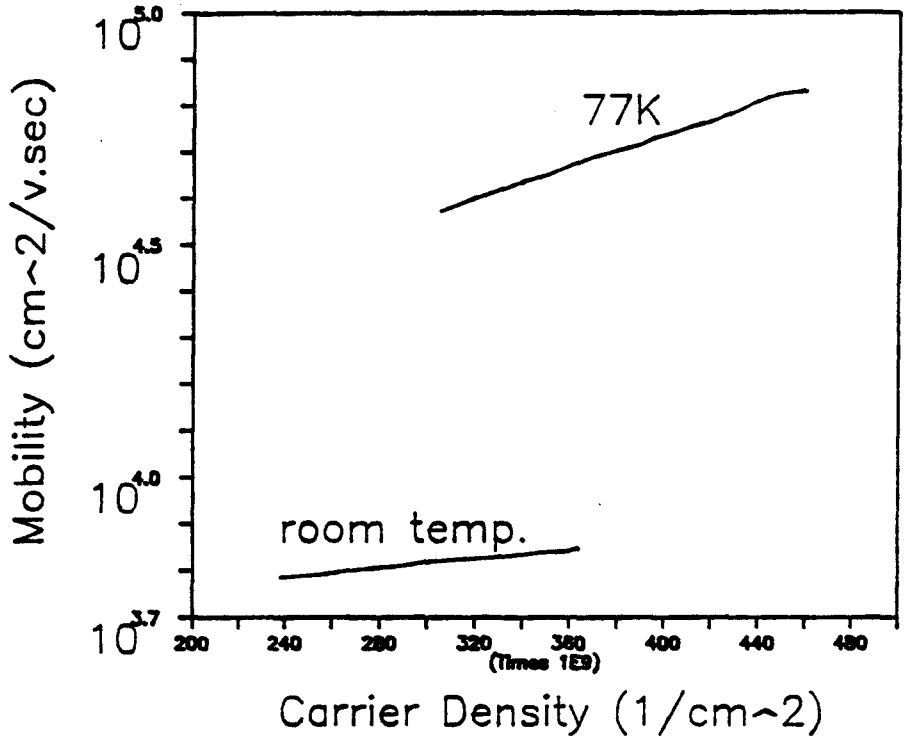
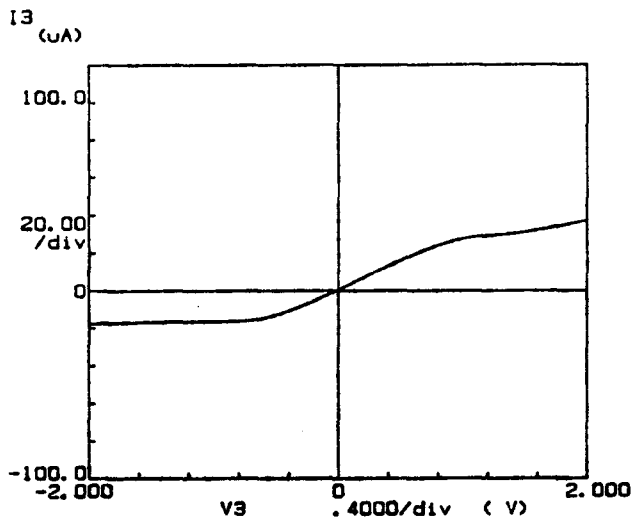
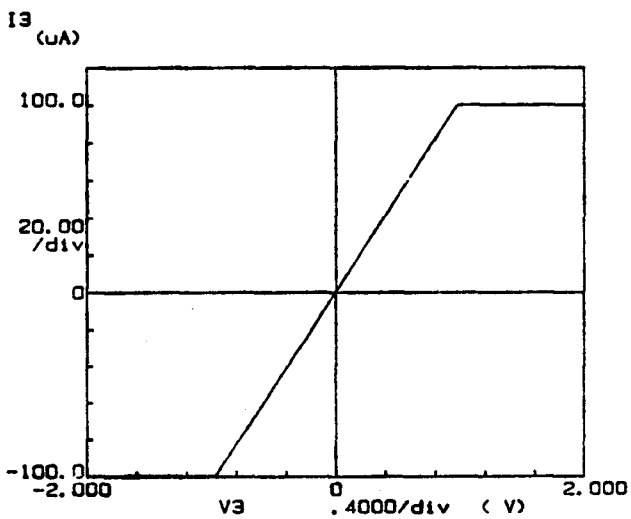


Figure 4.4 Mobility (μ) vs sheet carrier density (n_s) from Hall measurement at room temperature and at 77K.



(a)



(b)

Figure 4.5 A non-ohmic characteristic (a), an ohmic characteristic (b)

Samples	A		B		C*	
Structures	#1	#2	#1	#2	#2	
l_i (microns)	R_i (ohms)	R_i (ohms)	R_i (ohms)	R_i (ohms)	R_i (ohms)	Avg (R_i)
25	870	727	1100	803	559	**811.8**
20	700	700	727	685	475	**657.4**
15	648	565	529	592	407	**548.2**
10	503	500	514	535	380	**486.4**
5	332	488	427	488	270	**401.0**
R_c (ohm.cm)	**1.14**	**1.98**	**0.95**	**1.93**	**1.08**	**1.4±0.2**

* Data from structure #1 not available

Table 4.1 The results from ohmic test structure measurements.

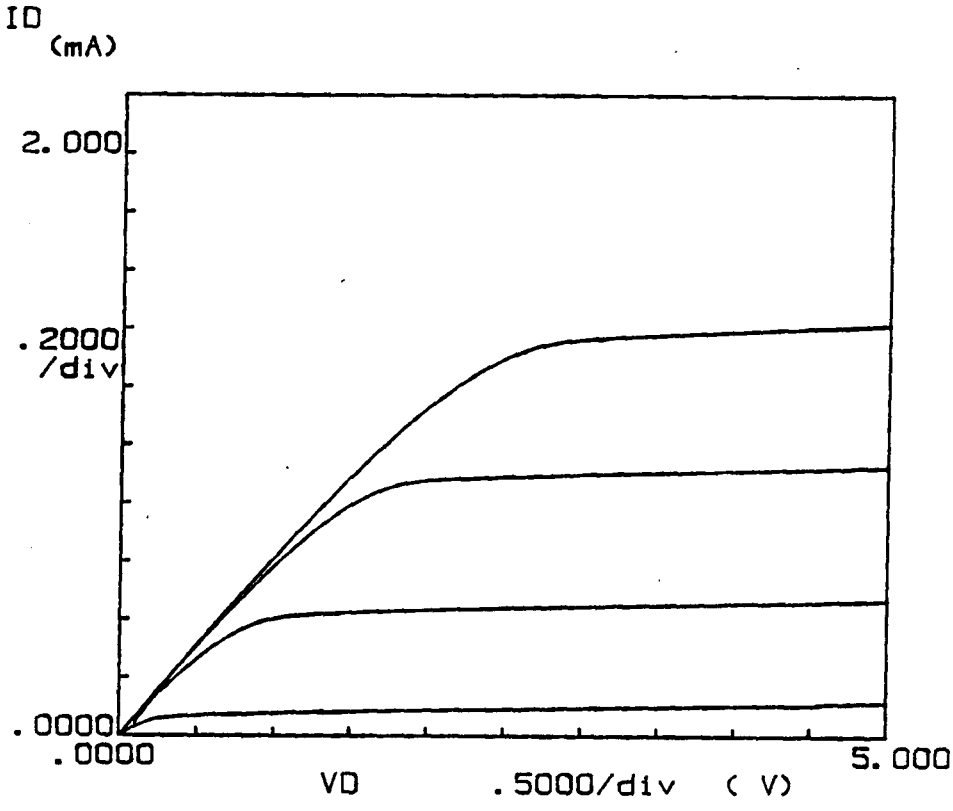


Figure 4.6 I-V characteristic of the normal gate transistor at room temperature.

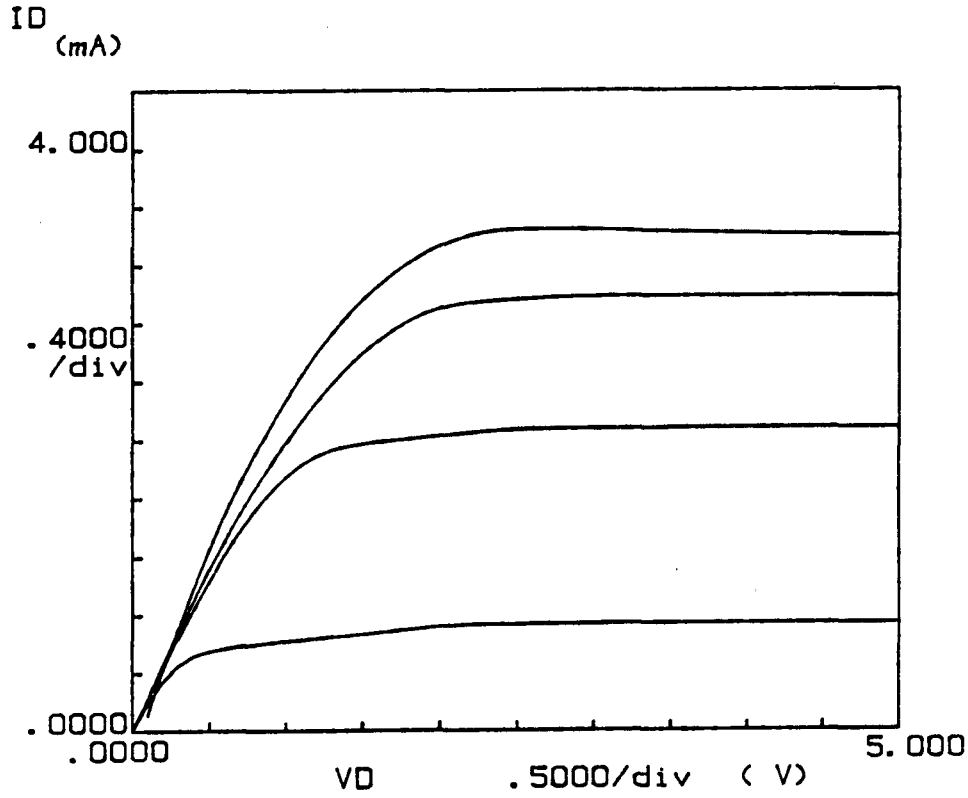


Figure 4.7 I-V characteristic of the normal gate transistor at 77K.

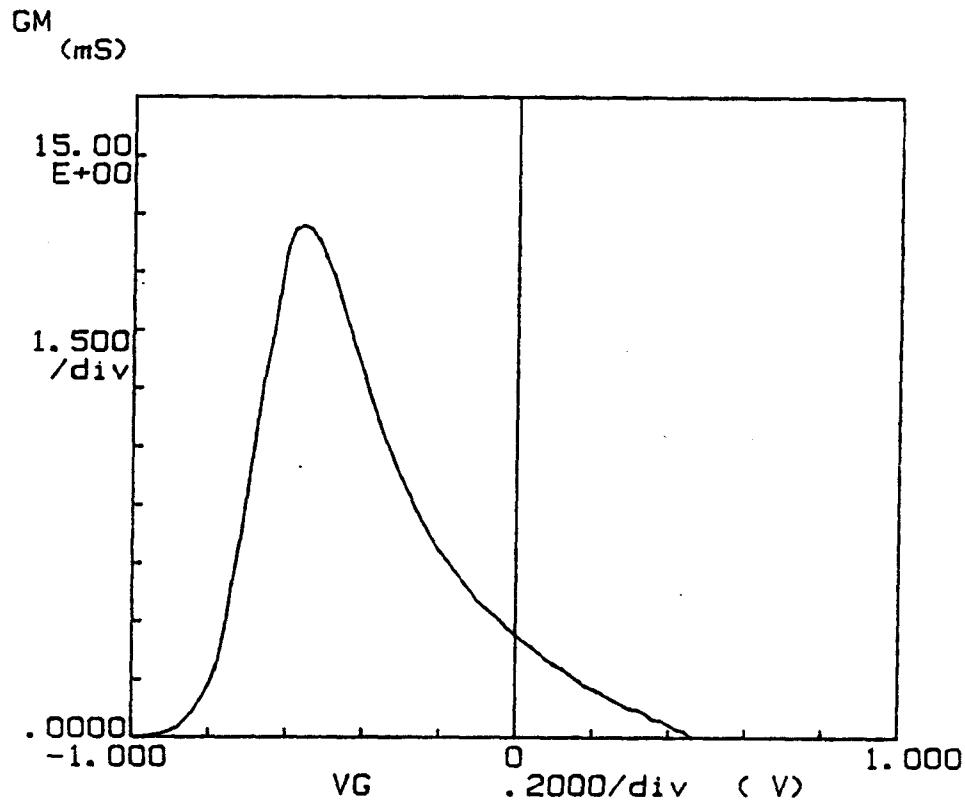


Figure 4.8 Linear transconductance of the normal gate transistor at room temperature.

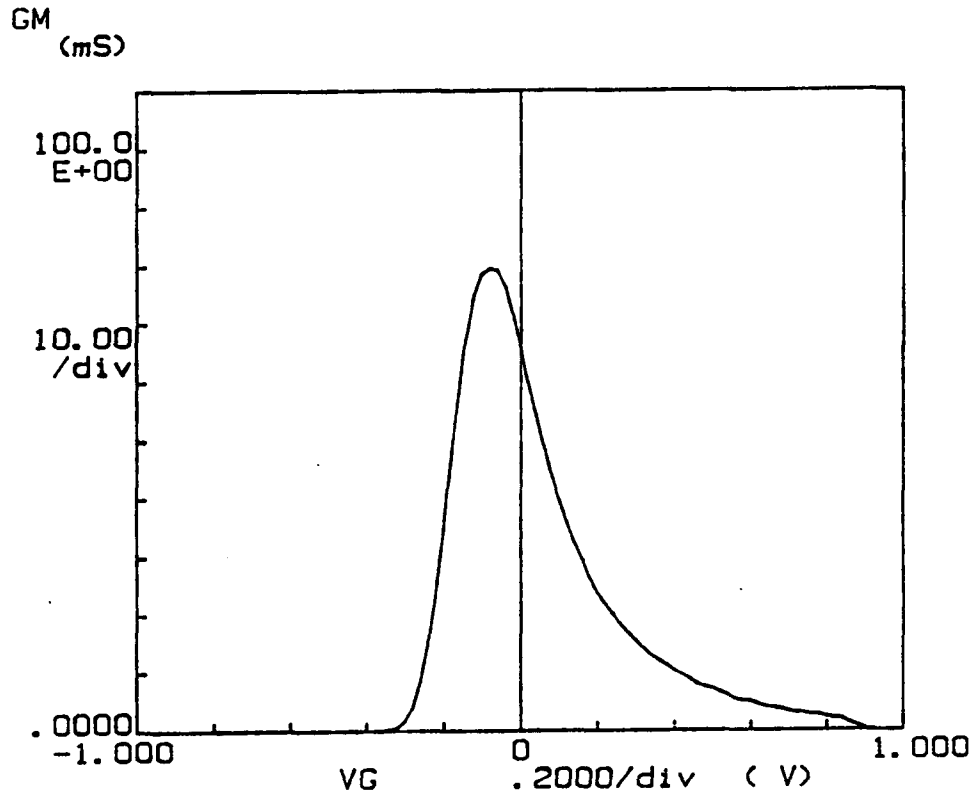


Figure 4.9 Linear transconductance of the normal gate transistorat 77K.

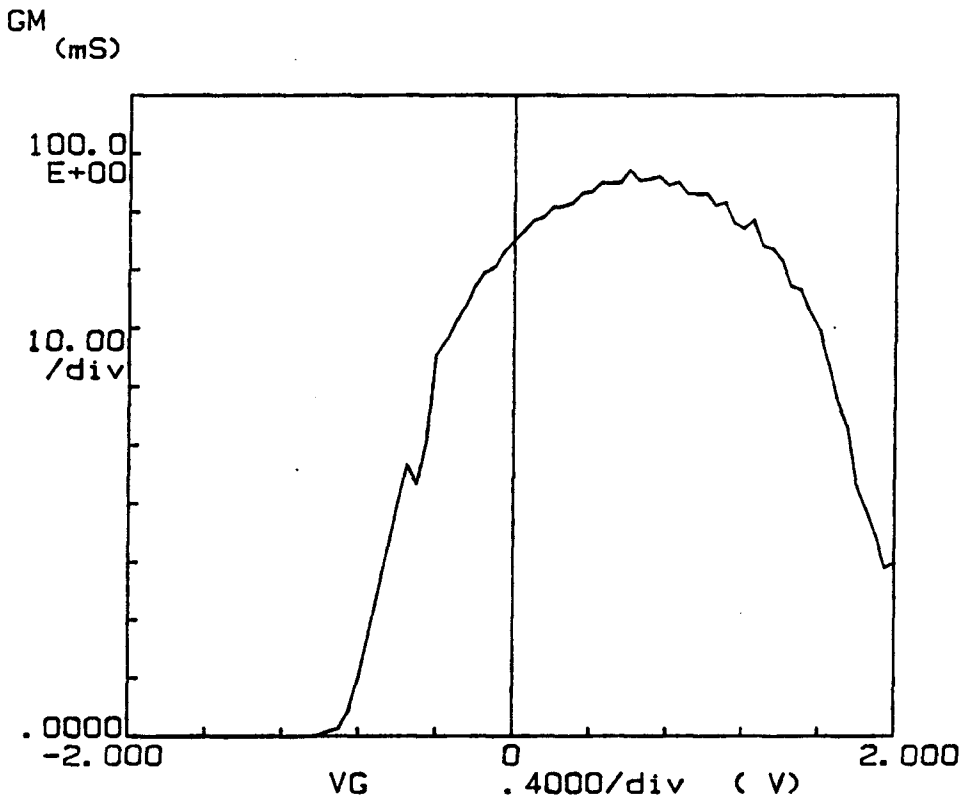


Figure 4.10 Saturation transconductance of the normal gate transistor at room temperature.

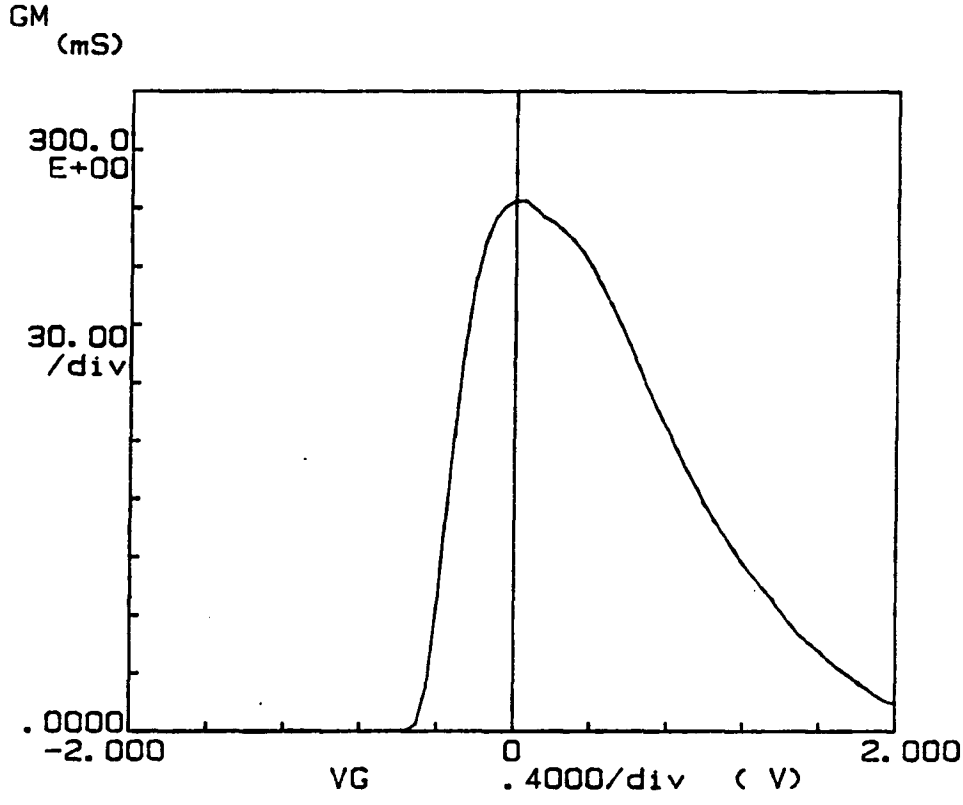


Figure 4.11 Saturation transconductance of the normal gate transistor at 77K.

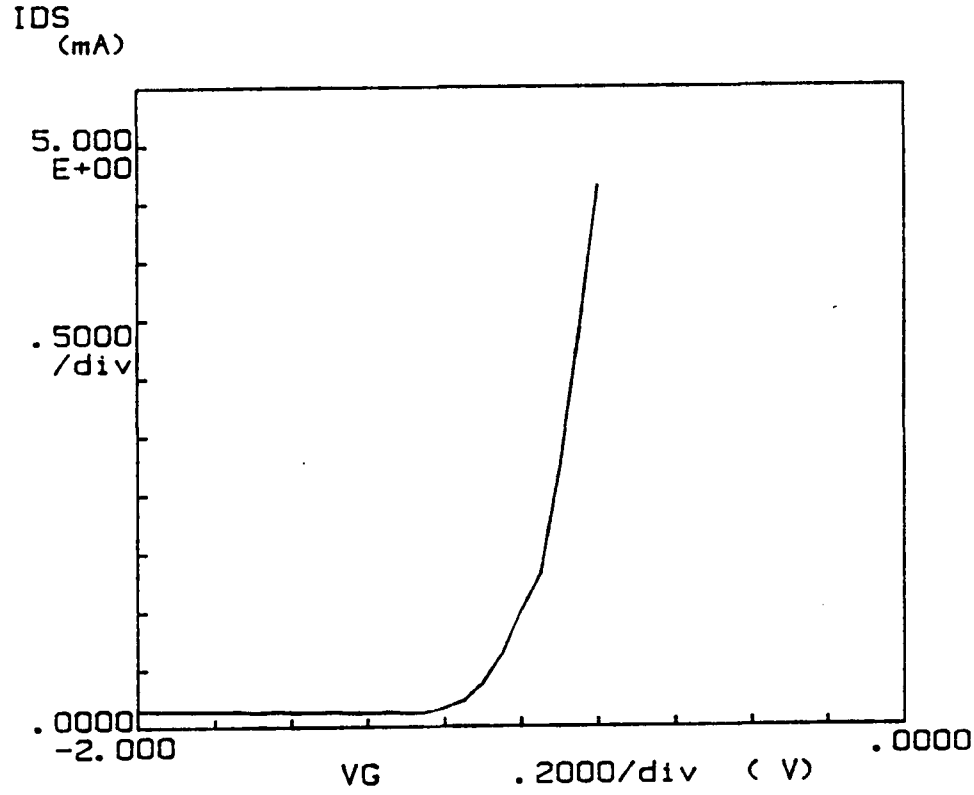


Figure 4.12 Saturation current of the normal gate transistor at room temperature.

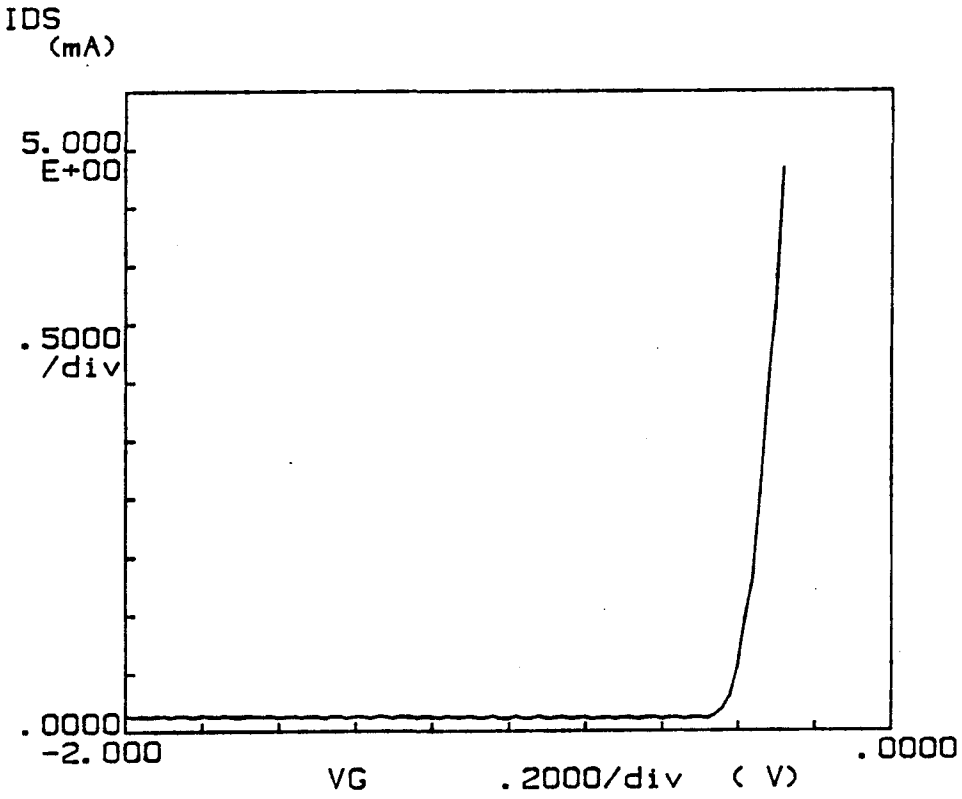


Figure 4.13 Saturation current of the normal gate transistor at 77K.

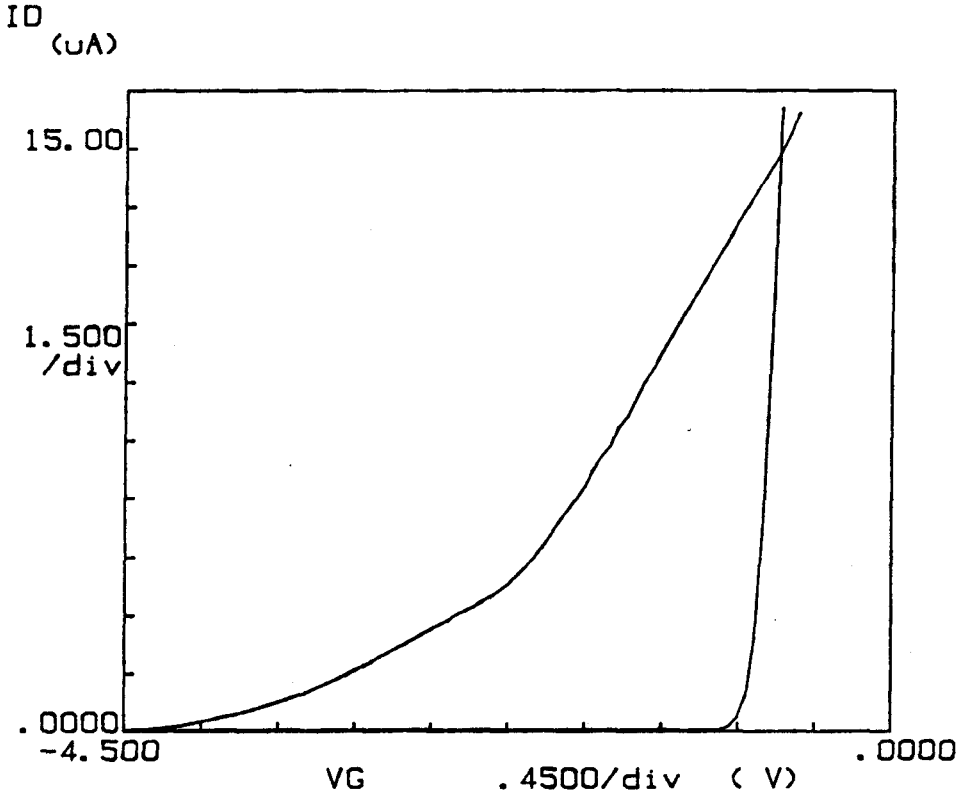


Figure 4.14 Threshold voltages of split and normal gate transistors.

5. CONCLUSION

The normal gate transistors performed reasonably well although there was discrepancy between V_{off} from the measurement and from calculation. All parameters extracted from the measurements are summarized in Table 5.1. The results from Hall measurements showed the increase of carrier density with the increasing gate voltage and the increase of mobility with the increase of carrier density. The mobility at 77K was higher than that at room temperature. However, the carrier density at 77K was higher than that at room temperature. This result was not expected and it was suspected to be caused by the parasitic MESFET because measurements were conducted mostly in a high gate voltage region. The contact resistance was found to be rather high. Furthermore, it was non-uniform within the sample and this was probably due to systematic variation.

Since the results have shown the low quality ohmic contacts due to high contact resistance, this could limit the device performance. The variation of contact resistance could cause the inconsistency of the device behavior as seen from the Hall measurement where the result was not obtainable when the negative voltages were applied. For future studies, it would be proper to develop an appropriate procedure for ohmic contact deposition to obtain better quality contacts. In addition, a consistent and controllable environment in terms of equipments need to be maintained to assure a reproducible result.

Parameters	Room Temperature	77K
Voff (volts)	-0.76	-0.31
Gm (Linear Region) (ms)	13.2	80
Gm (Saturation) (ms)	97	273

Table 5.1 Parameters extracted from experimental measurements.

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