AN ABSTRACT OF THE THESIS OF

Fredrick D. Whitwer for the degree of Master of Science in Electrical and Computer Engineering presented on June 27, 1986.

Title: DLTS Characterization of Precipitation Induced Microdefects

Redacted for privacy

Abstract approved: ______________________
Leonard Forbes

The electrical properties of microdefects in both n- and p-type silicon has been investigated. Oxygen rich Czochralski grown silicon wafers were subjected to a two step heat treatment to nucleate and grow oxide precipitates. The growth of the precipitates in turn induces other microdefects such as dislocation complexes and stacking faults to be formed. Aluminium Schottky barrier diodes were then fabricated on the wafer surfaces. These diodes were used as the test structures for the Deep Level Transient Spectroscopy (DLTS) characterization.

The results indicate that for n-type silicon a mid-bandgap deep level exists. This majority carrier trap could act as an effective generation-recombination center. But the trap concentrations measured (10^{12} cm^{-3}) suggest any detrimental effects due to these traps would be negligible. The results for p-type show not one deep level energy but a band of allowed energies in the lower half of the bandgap. The concentrations measured for this majority carrier trap are approximately 10^{13} cm^{-3}. At slightly reduced concentrations the same band of energies is detected in as grown or non-heat treated samples.

DLTS CHARACTERIZATION
OF PRECIPITATION INDUCED MICRODEFECTS

by

Fredrick D. Whitwer

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Completed June 27, 1986
Commencement June 1987

APPROVED:

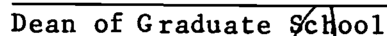
Redacted for privacy

Professor of Electrical and Computer Engineering in charge of major

Redacted for privacy

Head of Department of Electrical and Computer Engineering

Redacted for privacy



Dean of Graduate School

Date thesis is presented June 27, 1986

CONTRIBUTION OF AUTHORS

J. D. Peng was the industrial collaborator who provided the silicon samples necessary for the project.

H. Haddad was a more junior student who assisted with the electrical measurements.

TABLE OF CONTENTS

INTRODUCTION	1
Transient Analysis	2
DLTS Technique	4
OXYGEN PRECIPITATION IN CMOS WAFERS	9
Abstract	9
Introduction	9
Influence of Ambients on Oxygen Precipitation	10
Electrical Characteristics of Secondary Microdefects	12
Conclusions	17
References	18
DLTS CHARACTERIZATION OF PRECIPITATION INDUCED MICRODEFECTS	19
Abstract	19
Introduction	19
Experimental Procedure	20
Results	21
Models and Conclusions	26
Acknowledgements	27
References	28
CURRENT PROBLEMS AND FUTURE DIRECTIONS	29
Additional Observations on Microdefect Related Deep Levels	29
Suggestions for Further Work	33
CONCLUSIONS	34
BIBLIOGRAPHY	37

LIST OF FIGURES

FIGURE		PAGE
1.	Schematic diagram of the DLTS system used for this study	6
2.	Band diagram of a Schottky barrier with a deep level trap	8
3.	Influence of ambients on oxygen precipitation	11
4.	Time required for start of precipitation	13
5.	Schottky diodes used for DLTS measurements	14
6.	Time constant or reciprocal emission rate versus 1000/T	16
7.	Electrical activity or concentration of the mid-gap level	17
8.	Activation energies for precipitated n-type silicon	22
9.	DLTS spectra from precipitated p-type silicon	24
10.	Activation energies for etched p-type silicon	25
11.	Trap and BSF density profile	26
12.	Trap density and bulk stacking fault density profiles for p-type silicon	31

DLTS CHARACTERIZATION OF PRECIPITATION INDUCED MICRODEFECTS

INTRODUCTION

The characterization of deep levels in silicon is important because any mid-gap levels that may exist will act as efficient generation-recombination centers. It is well known that the heat treatment of oxygen rich silicon can cause the precipitation of oxygen which in turn induce the formation of microdefects. One of the questions to be answered is whether or not these microdefects introduce any mid-bandgap energy levels which in turn would have a detrimental effect on minority carrier lifetime The minority carrier lifetime is an important parameter for all types of solid state devices but is especially critical for Metal-Oxide-Semiconductor (MOS) capacitors used extensively in VLSI dynamic RAMs. The retention time of MOS capacitors can be severely degraded by the presence of generation-recombination centers close to or in the depletion region.

To investigate the electrical properties of precipitation induced microdefects Deep Level Transient Spectroscopy (DLTS) measurements were undertaken. Two of the more important quantities obtained from DLTS measurements are; 1) activation energy or energy level position in the bandgap and 2) trapping center concentration. The DLTS technique is applicable to any device having a depletion region such as pn junction diodes, Schottky barrier diodes and even MOS capacitors. One advantage of the Schottky barrier diode is that it requires no high temperature processing steps of the substrate material which could alter the structure of the microdefects. This fact coupled with the ease of fabrication resulted in the use of Schottky barrier diodes for this

study. Reference has been made above to both generation-recombination (G-R) centers and to traps. A distinction can be made between the two types of deep levels by considering the rate of carrier capture [1]. A G-R center has large capture rates for both electrons and holes. The kinetics of this kind of center can be explained using Schockly-Read-Hall (SRH) recombination theory [2]. For a trapping center one of the capture rates will usually dominate. But in the space charge region of a semiconductor the electron and hole concentrations are essentially zero, hence both the capture rates are zero also. For this situation all deep levels act as traps since recombination cannot occur. Thus the deep levels detected using DLTS are usually refered to as traps. To help better understand the results of this characterization, a description of the DLTS technique and of the more general topic of transient analysis will be given.

TRANSIENT ANALYSIS

Departures from the regular silicon crystal lattice structure can be caused by intentionally introduced dopant impurities and unintentionally introduced impurities such as oxygen and carbon. Microdefects such as oxygen precipitates and bulk stacking faults also alter the silicon lattice structure. These alterations in the periodicity of the silicon lattice result in the formation of potential wells which can cause current carriers to be bound to the defects. The emission of these trapped carriers procedes at a rate (e) determined by Boltzmann statistics and is a function of lattice temperature (T) and activation energy ($\triangle E$). Or,

$$e = C\exp(-\triangle E/kT) \qquad (1)$$

where k is Boltzmanns constant and C is a pre-expontial dependent on T^2. From a plot of the emission rate versus reciprocal temperature one can determine the difference in energy between the deep level and the band to which the carrier is emitted to, i.e. the activation energy. The inverse process of emission is capture with its associated capture rate (c). The capture rate can be written,

$$c = svn \quad (2)$$

where s is the carrier capture cross-section, v is the carrier average thermal velocity and n is the carrier concentration. An expression for the rate of change of electrons at a trapping center (dn_t/dt) can be written using the emission and capture rates [3],

$$dn_t/dt = c_n n p_t - e_n n_t + e_p p_t - c_p p n_t \quad (3)$$

where the subscripts n and p refer to electrons and holes respectively. The quantities n_t and p_t refer to concentration of electrons and holes respectively at the trapping center. Note that $n_t + p_t = N_{tt}$ or the total trap density. The remaining quantities n and p are the carrier densities in the conduction and valence bands respectively. In a depletion or space charge region both n and p are zero. Hence we can rewrite Eq. 3 and then solve for n_t assuming all the traps are initially filled,

$$n_t(t) = N_{tt} t_c [e_p + e_n \exp(-t/t_c)] \quad (4)$$

where $t_c = 1/(e_n + e_p)$ is the time constant of the trap. Since t_c is not dependent on N_{tt} the small signal error due to low trap concentrations is reduced. As seen in Eq. 4 the electron concentration at the trap is a decreasing function of time. The electrons emitted from the trap to the conduction band are immediately swept out of the depletion region by the electric field. As this happens the width of the

depletion region gradually relaxes back to the steady state depletion width with a corresponding increase in depletion capacitance. The capacitance increases at an exponential rate which has a time constant equal to that of the trapping center. The important point is that this time constant which is the reciprocal emission rate is a strong function of the temperature. The above analysis of electron emission in n-type material can be extended to hole emission in n-type with appropriate changes in initial conditions. The major difference being that the depletion region relaxes so that the capacitance decreases, again with a time constant highly dependent on temperature. The result of this transient analysis is that by measuring macroscopic parameters such as capacitance and temperature the microscopic properties of a trapping center such as $\triangle E$ and N_{tt} can be determined. The DLTS technique allows rapid determination of these microscopic properties.

DLTS TECHNIQUE

The exponential capacitance transient described in the previous section can be analyzed in many ways to determine its time constant. One of the most common ways is with use of a boxcar integrator. This method samples the transient at two different times t_1 and t_2. The normalized difference in capacitance at these two times is given by [4],

$$S = [C(t_1) - C(t_2)] / \triangle C(0) \qquad (5)$$

where $\triangle C(0)$ is the capacitance change at the beginning of the transient. For a true exponential transient $S=\exp(-t_1/t_c)-\exp(-t_2/t_c)$. From this expression the time constant (t_c) can be determined by finding the value where the output S is maximum. By setting $dS/dt_c=0$ we obtain,

$$t_c = (t_2 - t_1) / \log(t_2/t_1) \qquad (6)$$

Since t_1 and t_2 are fixed parameters of the boxcar integrator there is only one value of t_c that satisfies Eq. 6. From the previous section we know that t_c or reciprocal emission rate is a function of the temperature (T). Hence a peak in the plot $C(t_1)-C(t_2)$ versus T will reveal the temperature at which the traps time constant equals the boxcar time constant. Also from the plot of $C(t_1)-C(t_2)$ versus T the trap density N_{tt} can be determined. This is done by determining the magnitude of the peak and dividing this value by S_{max},

$$S_{max} = \exp[-t_1 \ln(t_2/t_1)/(t_2-t_1)] - \exp[-t_2 \ln(t_2/t_1)/(t_2-t_1)] \quad (7)$$

This results in a value for $\triangle C(0)$, which will be shown later to be proportional to N_{tt}.

The efficiency of the DLTS technique is due to the repeated filling and emptying of deep level traps by varying the reverse bias of a depletion region. The bias is supplied by a pulse generator which in addition triggers the boxcar averager. The boxcar averager allows the capacitance transient to be sampled repeatedly and then signal averaged. Now, if the temperature is scanned while the transient is monitored one obtains a continious plot of $C(t_1) - C(t_2)$ versus T. A schematic diagram of the DLTS system used in this study is shown in Figure 1. The boxcar integrator shown is a PAR model 162. The capacitance meter used is a Boonton model 72B which has a 1 ms response time. And the pulse generator used for most of this study is a Leader model LFG-1300S. The steady state reverse bias applied to the diode must be small enough to avoid avalanche breakdown. Additionally at large reverse biases there is the problem of leakage currents that adversely affect the accuracy of the capacitance measurement.

By changing the boxcar time constant and doing several thermal

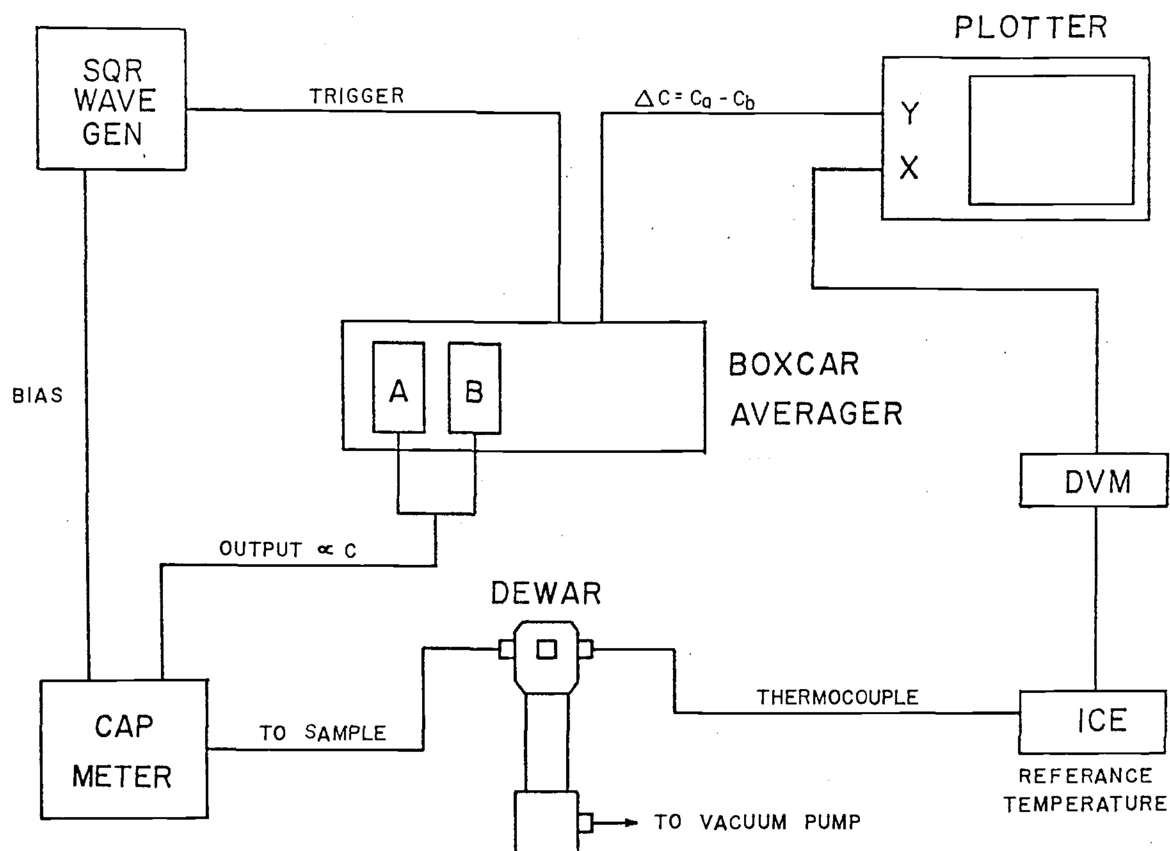


Fig 1. Schematic diagram of the DLTS system used for this study

scans the trap activation energy can be determined. In changing the time constant the ratio t_2/t_1 is usually kept constant to maintain the symmetry of the peak from plot to plot. Using Eq. 1 the activation energy can be calculated from the slope of a semi-log plot of e^{-1} ($=t_c$) versus 1000/T.

$$\triangle E = 0.2\triangle(\log_{10} t_c)/\triangle(1000/T) \quad (8)$$

The trap concentration as mentioned previously, can be determined from the $C(t_1) - C(t_2)$ peak height. Once $\triangle C(0)$ is found using Eq. 5, the trap concentration can be found using,

$$N_{tt} = 2(|N_a - N_d|)(\triangle C/C) \quad (9)$$

where C is the steady state reverse bias capacitance at the temperature at which the peak occurs. This equation is derived from the relation for depletion region capacitance with $|N_a-N_d|$ replaced by $|N_a-N_d| - N_{tt}\exp(-t/t_c)$, for majority carrier trapping. Or in other words, that the depletion region capacitance is less than the capacitance in the absence of traps. Two points must be made about Eq. 9. The first is that the ratio $N_{tt}/|N_a-N_d|$ must be less than about 1/3 for the equation to be valid [1]. The second point is that not all the traps within the depletion region eventually become ionized. As shown in Figure 2, there is an edge region (Y) where the trapping level lies below the Fermi energy. The result is an underestimate of the trap density which is largest when using low reverse bias voltages. For details on how to correct for this effect see Ref. 4.

The series of thermal scans that give activation energy data can also give information as to the donor or acceptor nature of the trap. If Poole-Frenkle barrier lowering [5] is considered, one notes that as the space charge field is increased the emission rate of trapped carriers

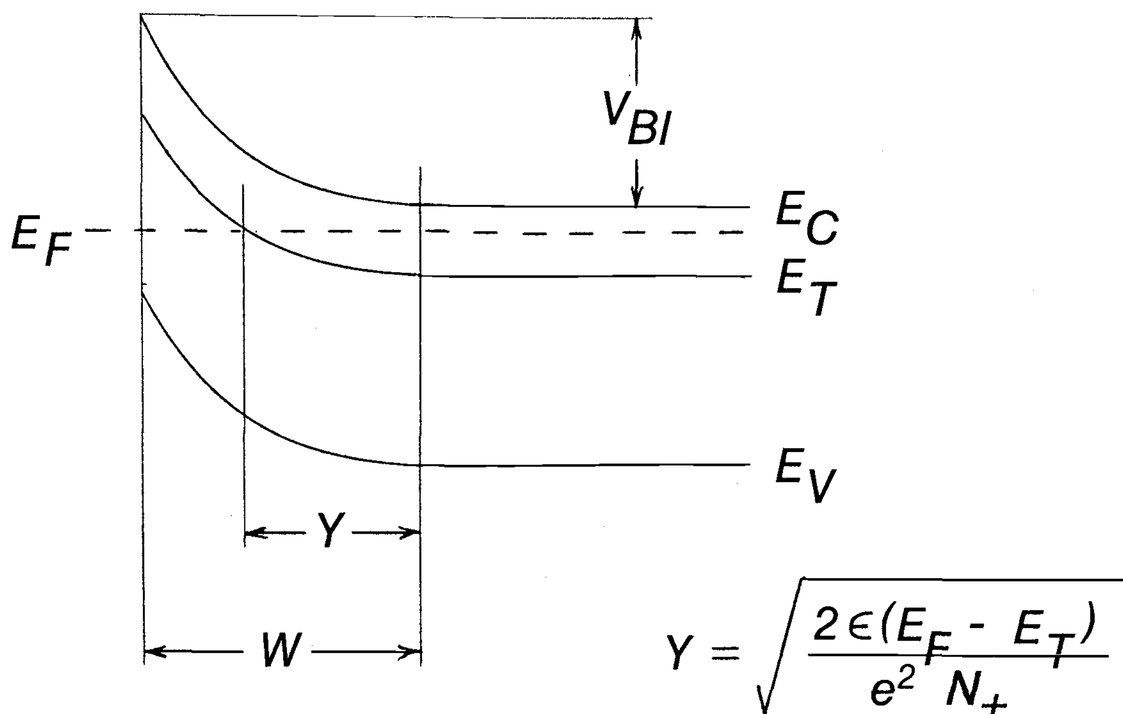


Fig 2. Band diagram of a Schottky barrier with a deep level trap

also increases. This means that less thermal energy is required to ionize the defect state. So in terms of the DLTS thermal scans the peaks move to lower temperatures as the steady state reverse bias is increased. Barrier lowering only occurs for defect states that are charged when empty. This corresponds to a donor type impurity. If, on the other hand, the defect is acceptor like, the charge state is neutral when empty. So for an acceptor like defect no shift in the peak temperature is seen as the reverse bias is increased.

OXYGEN PRECIPITATION IN CMOS WAFERS

F.D. Whitwer*, L. Forbes* and J.D. Peng**
*Dept. of Elect. Engr., Oregon State University, Corvallis, OR 97331
**Silicon Materials Division, Fairchild, Healdsburg, CA 95448

ABSTRACT

The application of denuding, nucleation, and intrinsic gettering in CMOS integrated circuit processes is described. Specifically, it will be demonstrated that an initial oxidizing step, as many manufacturers are using, seriously retards the effectiveness of any subsequent nucleation step or procedure. The results of a large number of one-step, two-step, and three-step heat treatments are summarized and design criteria for controlled oxygen precipitation in integrated circuit fabrication are described. Two-step heat treatments, without denuding and with the nucleation step first, have been used to induce precipitates close to the surface of CMOS wafers and DLTS measurements made to deduce the effectiveness of intrinsic gettering and the electrical characteristics of precipitation induced microdefects.

INTRODUCTION

Several attempts have been made to employ denuding, nucleation, and intrinsic gettering [6] effectively in p-well CMOS and high density n-channel MOS processes with varying degrees of success. The industrial adaptations of these basic sequences usually involve a high temperature oxygen out diffusion of 1100 C for 2 or 4 hours, a nucleation step between 600 C to 750 C for four hours, and the subsequent oxygen precipitation and intrinsic gettering to occur during the standard CMOS or n-channel MOS device processing sequence. The CMOS process in

particular may involve extended times at high temperatures associated with the p-well drive-in and diffusion during which significant oxygen precipitation should or could occur. Unfortunately, however, there are a number of subtle differences between the basic studies as reported in the literature [6] and the actual implementation of these in industrial applications. This report specifically seeks to address these issues and their consequences. Firstly we have done an exhaustive study of the influence of ambients in the first step of three step sequences on oxygen precipitation in silicon and then DLTS investigations of the electrical characteristics of secondary microdefects induced by oxygen precipitation in CZ silicon.

INFLUENCE OF AMBIENTS ON OXYGEN PRECIPITATION

S.M. Hu [7] was among the first to notice and report in a consistent manner ambient effects on oxygen precipitation in silicon. As shown in Fig. 3, we have found the ambient used in the first step of a three-step sequence to have a drastic effect on subsequent nucleation and precipitation. We have used a so-called "V-graph" representation which shows the change in interstitial oxygen concentration versus the initial, and final, interstitial oxygen concentrations. The intercept of the "V" on the abscissa is the "critical oxygen concentration"; if the initial value is lower than this value, no significant oxygen precipitation will occur. For the sequences shown in Fig. 3, if the initial step is a neutral ambient, as was used in the basic investigations, then this critical value is about 21pmA. On the other hand, however, if the first step is an oxidation, then the critical value is 27ppmA.

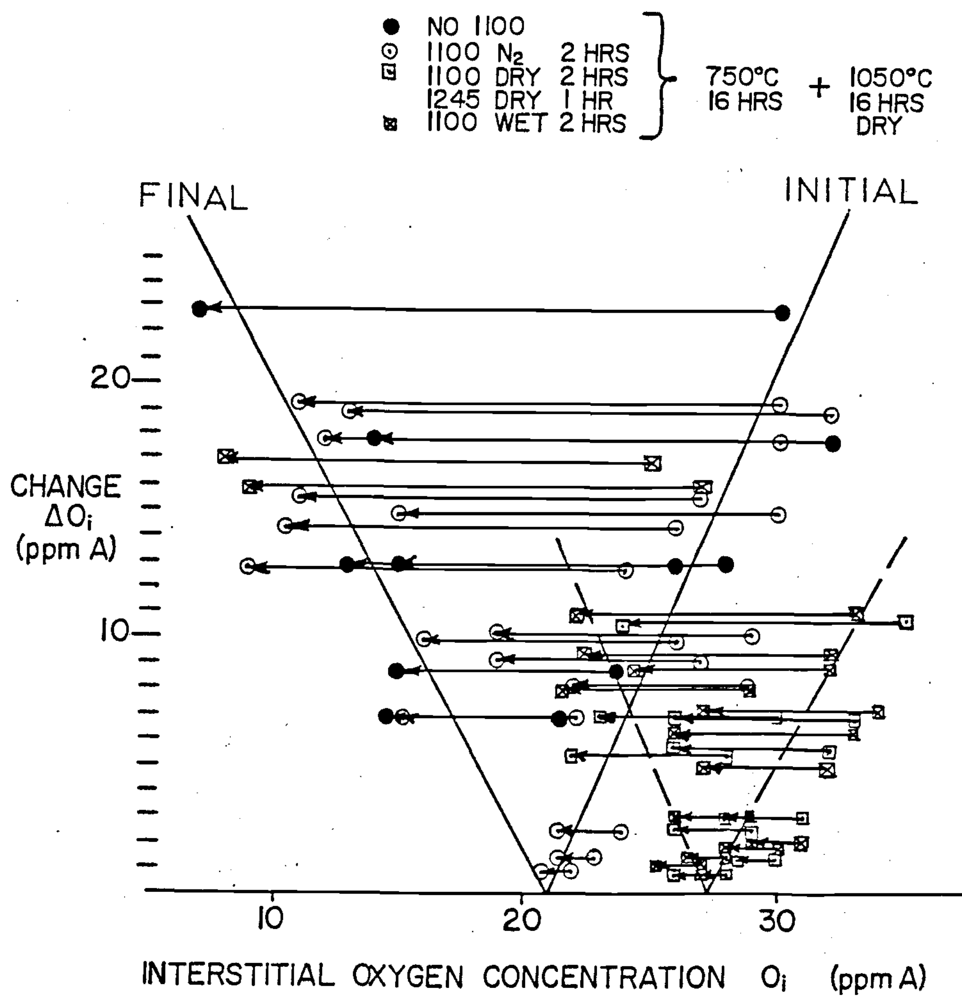


Fig 3. Influence of ambients on oxygen precipitation

Moreover, when the results of a large number of single step, double step, and three-step heat treatment are summarized as has been done in Fig. 4, the effect of an initial oxidation in the three-step sequence becomes clearer. Specifically, it renders any subsequent attemp at nucleation at 750 C ineffective. In other words, the amount of precipitation occurring in a three-step sequence with an initial oxidation and final 1050 C for 16 hours is the same as a single step heat treatment of 1050 C for 16 hours. Both have the same "critical oxygen concentration" of about 27ppmA.

Fig. 4 is a master design curve which can be used to deduce approximately the "critical oxygen concentration" for a variety of conditions. A three-step sequence with an initial neutral ambient is the same as a two-step sequence, to achieve a "critical oxygen concentration" of 27ppmA, less than 8 hours at 750 C and less than 8 hours at 1050 C would be sufficient, or only about one half the time before at high temperatures.

Unfortunately, neutral ambients as a first step are unacceptable in industrial processes due to "haze" and surface pitting. Some variations on this process have been to try to use only vary thin initial oxides, however, we have found that even 400A is sufficient to render subsequent nucleation ineffective. Presumably this is due to oxidation producing fast diffusing interstitials [8] which subsequently suppress low temperature nucleation of oxygen precipitation.

ELECTRICAL CHARACTERISTICS OF SECONDARY MICRODEFECTS

Many CMOS processes and most n-channel MOS processes are employed in low leakage current applications or dynamic memories. As such, there

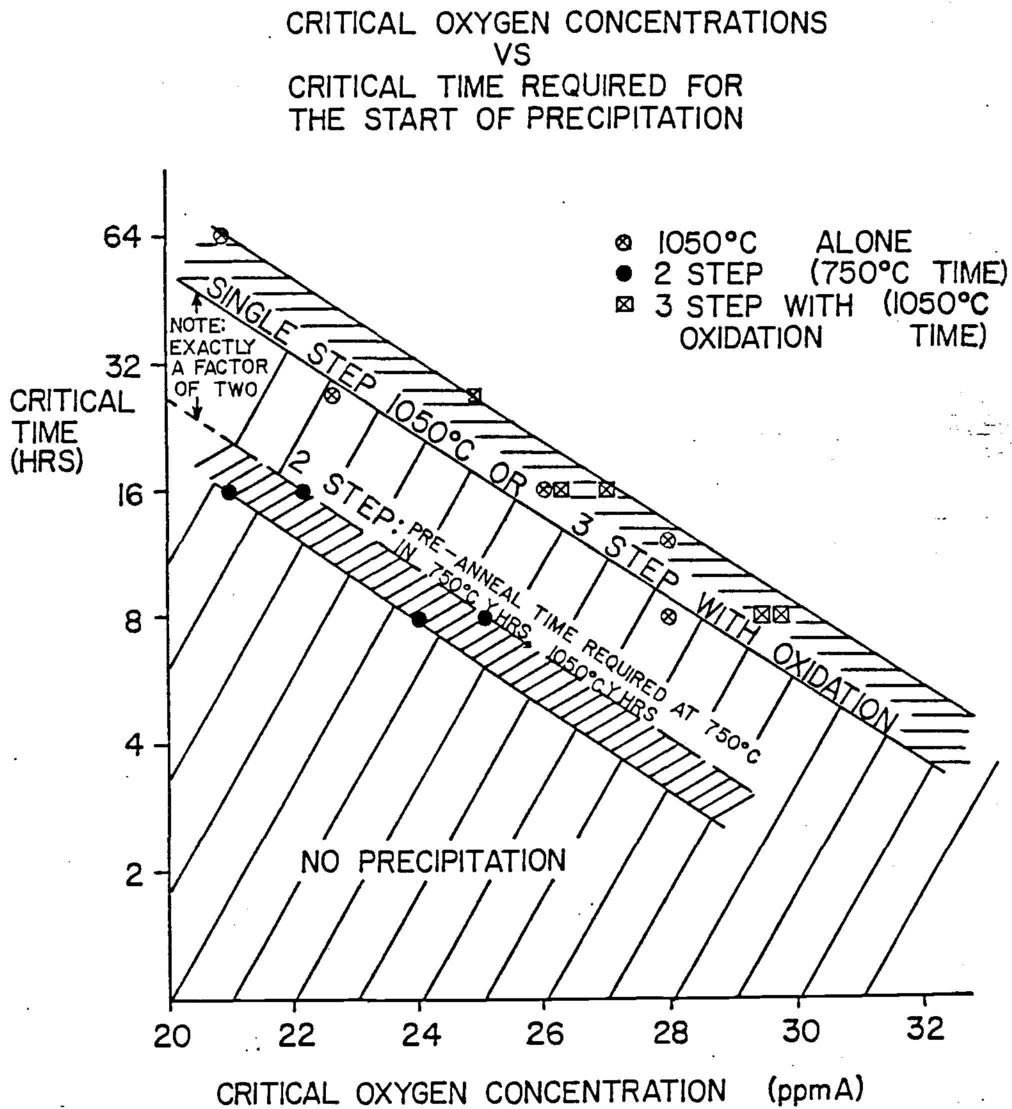


Fig 4. Time required for start of precipitation

might be some considerable concern about the electrical characteristics of the precipitates themselves or secondary microdefects induced by precipitation, particularly any residual defects which might occur in the denuded zone near the surface. While there have been some reports [8] on the electrical characteristics of microdefects these have been primarily done in oxygen free float zone silicon (FZ) rather than Czochralski (CZ) silicon.

To address this concern we have fabricated Schottky diodes and have done capacitance DLTS measurements to identify any mid-gap defect level which might act as a source leakage currents. Fig. 5 shows the basic device structure used, in this particular process we have used a low temperature nucleation at 750 C first in order to try and induce, near the surface, as many precipitates and secondary microdefects as

CMOS WAFERS
n-type
3-6 Ω-CM
DEPLETION REGION
AL-SCHOTTKY BARRIER
PRECIPITATED BY
12 hrs 750°C
16 hrs 1100°C
OR
4 hrs 750°C
16hrs {400Å 1100°C, 1100°C N_2}

Fig 5. Schottky diodes used for DLTS measurements

possible, or in other words, have tried to minimize oxygen outdiffusion and the formation of a denuded zone near the surface. Figs. 6 and 7 show the results in terms first of the reciprocal electron emission rate of the mid-gap level identified and then the relative concentration versus the amount of oxygen precipitation.

In the Arrhenius plot of Fig. 6 the mid-gap level appears to be close to both that of the gold acceptor level in silicon [10] or defects induced by thermal quenching [11], or in other words, nearly as close as possible to the center of the silicon band-gap. As such it should be an effective generation center or leakage current source. Fig. 7 shows however that the relative concentration is low, or the electrical activity is low, $\Delta C/C$ being only a few time 10^{-3} so that the equivalent concentration of defect centers is on the average only a few times $10^{+12}/cm^3$.

When Wright's etched the sample with a large amount of precipitation,ΔO_i=16ppmA, showed a very high density of bulk stacking faults and dislocations at 3 microns from the surface. The sample with a lesser amount of precipitation, ΔO_i=9ppmA, shows very few defects, less than $100/cm^2$, at 3 microns and a significant number only after a 25 micron etch. The precipitates and secondary microdefects do not seem to be very effective in introducing mid-gap levels and leakage current generation centers near the surface in CZ silicon. On the average then, and over large areas, precipitates and secondary microdefects near the surface should not contribute significant mid-gap defect level and leakage in CMOS processes.

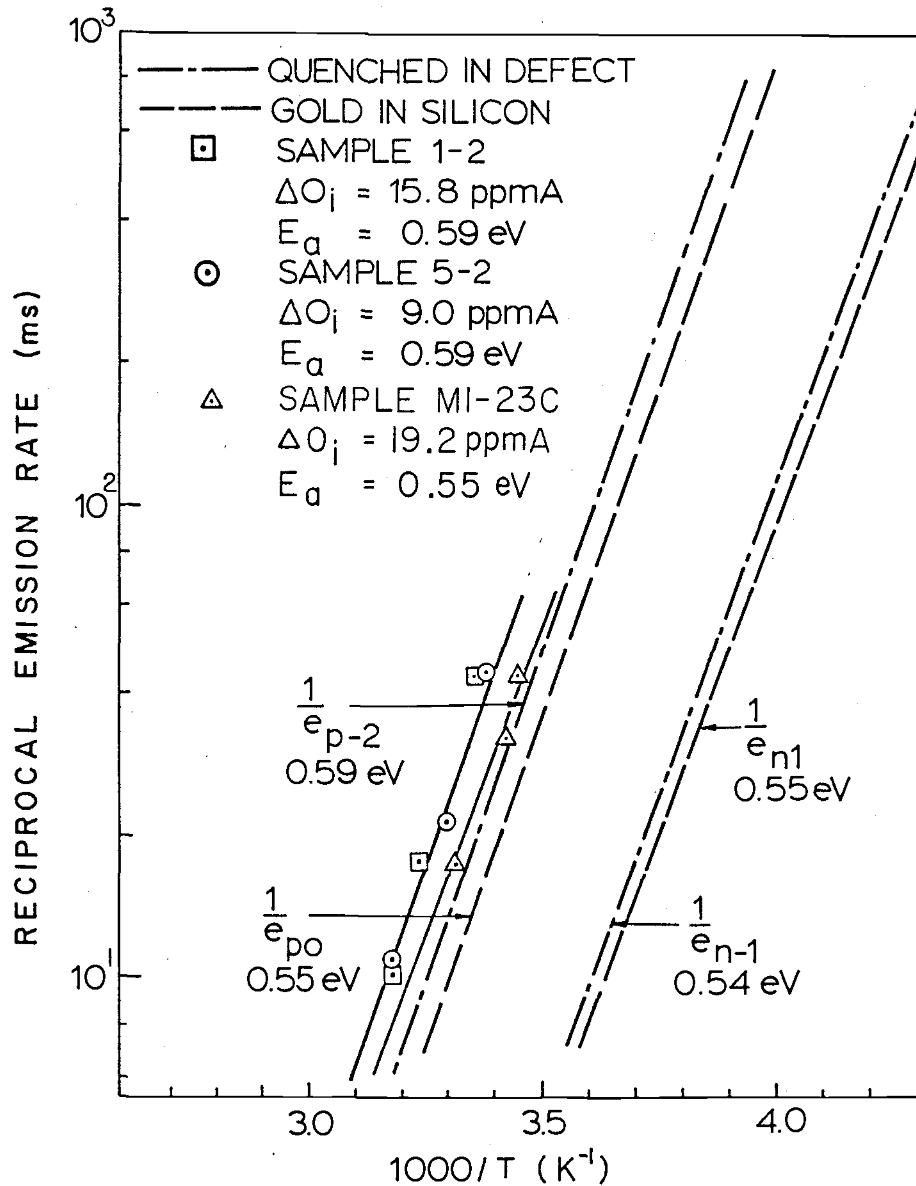


Fig 6. Time constant or reciprocal emission rate versus 1000/T

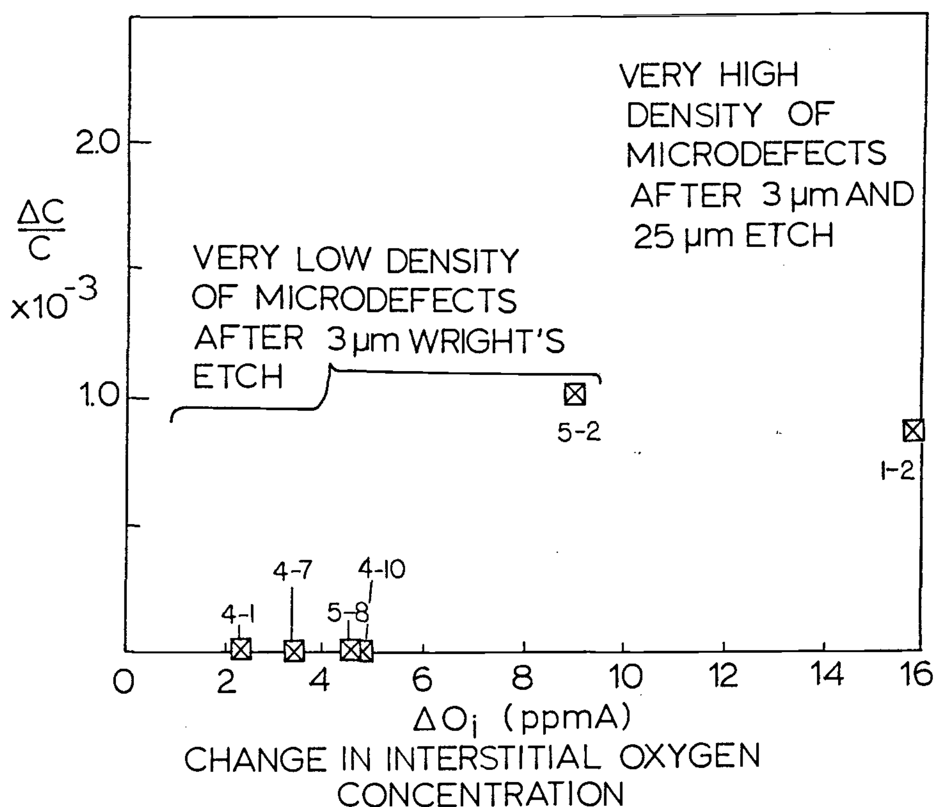


Fig 7. Electrical activity or concentration of the mid-gap level

CONCLUSIONS

In view of the influence of ambients on oxygen precipitation in industrially acceptable heat treatment schemes, little advantage seems to be gained from oxygen outdiffusion and nucleation prior to device fabrication. The same degree of control over denuded zones and amount of oxygen precipitation can be accomplished by entering the device

fabrication process with a controlled range of initial interstitial oxygen concentrations.

In addition, we have found the electrical activity of precipitates and secondary microdefects, in terms of mid-gap generation levels, to be low. As long as an upper limit is placed on the amount of oxygen precipitation which is allowed, and it is constrained to moderate levels, there should be little concern about excessive leakage over large areas such as a chip power supply bus due to mid-gap levels introduced by precipitation and secondary microdefects. There might, however, still be some concern about leakage in small isolated areas, as a dynamic memory cell, due to residual precipitates and secondary microdefects near the surface.

These results are particularly applicable to any low leakage current CMOS process or MOS dynamic memory application which does not employ epitaxial materials.

REFERENCES

[6] J. Andrews, in Defects in Silicon, Ed. by W.M. Bullis and L.C. Kimerling (Electrochmical Scociety, Pennington, NJ, 1983) p. 133.

[7] S.M. Hu, Appl. Phys. Lett., 36, 561 (1980).

[8] J.R. Patel, in Semiconductor Silicon 1981, Ed. by H.R. Huff, R.J. Kriegler, and Y. Takeishi (Electrochemical Society, Pennington, NJ, (1981) p. 189.

[9] T.Y. Tan, in Defects in Silicon, Ed. by W.M. Bullis and L.C. Kimerling (Electrochemical Society, Pennington, NJ, 1983) P. 325.

[10] C.T. Sah, L. Forbes, L.L. Rosier, A.F. Tasch and A.B. Tole, Appl. Phys. Lett., 15, 161 (1969).

[11] L.D. Yau and C.T. Sah, Solid-State Elect., 17, 193 (1974).

DLTS CHARACTERIZATION OF PRECIPITATION INDUCED MICRODEFECTS

F.D. Whitwer*, H. Haddad** and L. Forbes*
*Dept. of Electrical Engineering, Oregon State University
Corvallis, OR 97331
**Hewlett-Packard, NID, Corvallis, OR 97330

ABSTRACT

Capacitance DLTS measurements have been performed on heavily precipitated n- and p-type silicon wafers. The results indicate heavy metal gettering with a mid-bandgap deep level (0.55eV) for n-type silicon. The results for p-type silicon show a band of states present in the lower half of the bandgap. This band of states correlates well to the band of allowed energies found in heavily dislocated p-type silicon.

INTRODUCTION

The characterization of deep levels in silicon is important because any mid-bandgap levels that exist may act as efficient generation-recombination centers. It is well known that oxygen rich silicon that has been precipitated introduces microdefects into the silicon lattice. The question to be answered is whether or not these microdefects introduce any mid-bandgap energy levels that would have a detrimental effect on minority carrier lifetime. In an attempt to answer this question we have carried out capacitance Deep Level Transient Spectroscopy (DLTS) measurements on Czochralski silicon that had been heavily precipitated. A two step heat treatment described priviously [12] was used to precipitate both n- and p-type wafers. The two step heat treatment is the last two steps of a high-low-high anneal sequence

commonly used to getter CMOS silicon wafers intrinsically. After a discussion of the experimental procedure, the DLTS results for both the n- and p-type silicon will be presented. Finally, comparison of these results with other current research will be given.

EXPERIMENTAL PROCEDURE

The test structures for the DLTS measurements were aluminium Schottky barrier diodes that were fabricated on freshly etched surfaces. The evaporation of aluminium to form these diodes requires no high temperature processing but the usefulness of these diodes is limited in the fact that they conduct only majority carrier current.

The starting n-type material was 5-7 ohm-cm phosphorus doped CZ silicon with (100) orientation. The initial interstitial oxygen concentration for this lot was 31.3 $\pm$ 0.9 ppma. The p-type material was boron doped CZ silicon with (100) orientation and 14-22 ohm-cm resistivity. The initial interstitial oxygen for this set of wafers was 27.3 $\pm$ 0.6 ppma. The two step high-low heat treatment was used to induce precipitates as close to the surface of the wafer as possible. The n- type silicon was annealed for 16 hours at 750 C in flowing N_2 followed by 1 hour in O_2 at 1050 C then 15 hours in N_2 at 1050 C. The p-type silicon was similarily annealed 16 hours at 750 C in N_2 then 16 hours at 1050 C in O_2. The final interstitial oxygen concentrations were; n-type 11.3 $\pm$ 0.4 ppma and p-type 9.0 $\pm$ 0.4 ppma. The next step in the process was to use a mixture of HF, nitric and acetic acids to slowly etch the silicon while leaving a suitably polished surface. This step exposed precipitation induced microdefects that could in turn be probed by Schottky barrier diodes. The diodes were fabricated by

evaporation of aluminium through a metal mask at 10^{-5} torr. The resulting low leakage diodes had diameters of 0.8 mm. The DLTS system used was the dual channel boxcar integrator type with a liquid nigrogen dewar. The diodes were scanned in temperature from 100 K to 380 K and the capacitance DLTS spectra were obtained. Reverse bias voltages applied to the diodes varied from 1 to 3 volts. To delineate any microdefects present on the surface, Wright each was used for three minutes.

RESULTS

The DLTS spectra showed that traps with different characteristics exist for the n- and p-type materials. Previous results [12] for heat treated n-type silicon showed majority carrier trap activation energies close to mid-bandgap (0.55 eV) and capture cross sections close to that of substitutional gold in silicon [13]. Figure 8 is an Arrhenius plot comparing the results for n-type to that of the acceptor state due to gold in silicon and quenched in defects [11]. The numbers associated with the electron and hole emission rates refer to the defects' initial charge state. For further information see Refs. [13,11]. The spectra also revealed that the trap concentration increased in regions further from the surface of the wafer. However the largest concentrations measured were only a few times 10^{12} /cm^{3}. Subsequent preferential etching of the silicon in Wright each revealed bulk stacking faults (BSF) with densities that increased to 10^{5} /cm^{2} at 25 microns from the surface. It is presumed then that heavy metal gettering is occuring at the stacking faults or possibly at the precipitation dislocation complexes (PDC). The result is the formation

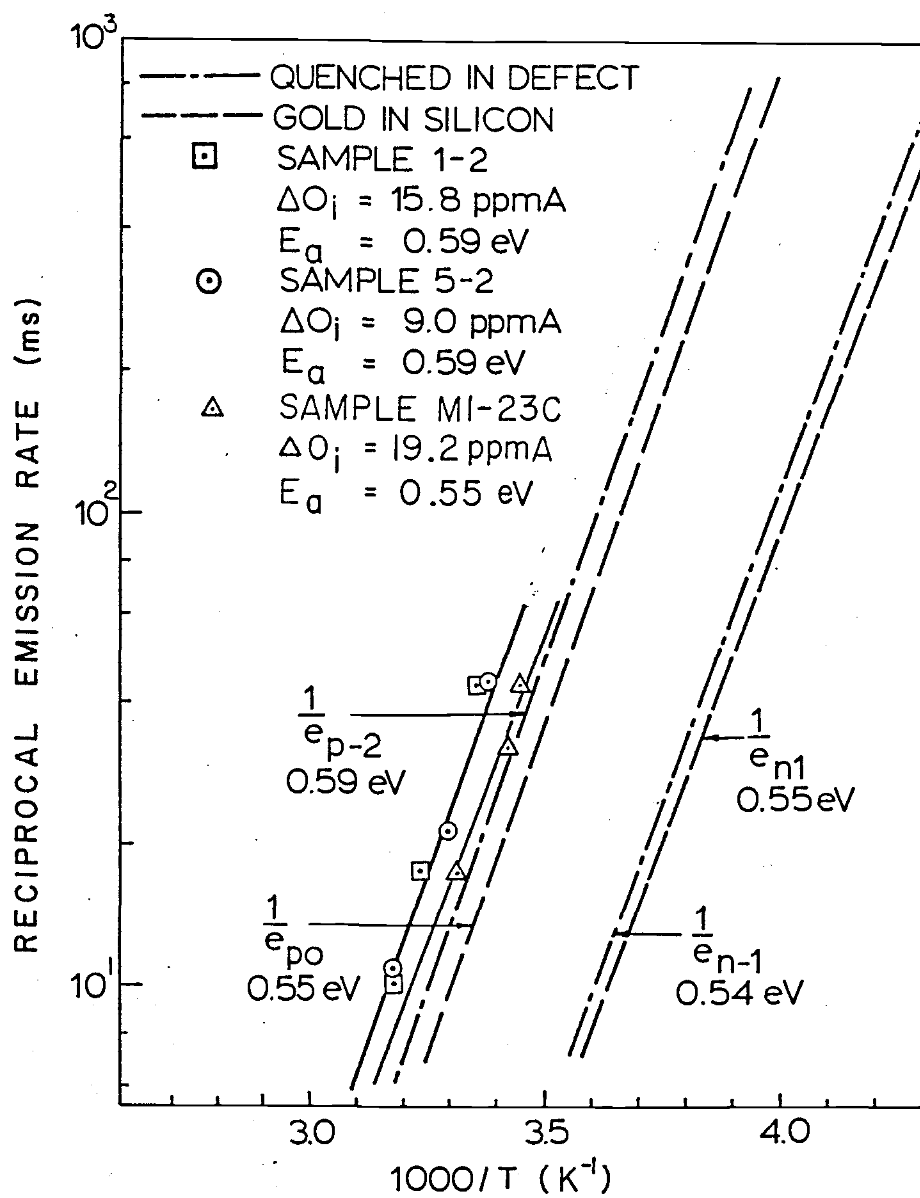


Fig 8. Activation energies for precipitated n-type silicon

of localized states that give rise to mid-bandgap activation energies, such as for gold in silicon.

Traps in the p-type material show a different behavior. First of all the activation energies for these majority carrier traps range from 0.2 to 0.5 eV. Secondly the capture cross sections show no uniformity. Two adjacent diodes from the same sample can show different energy levels and different capture cross sections. Figure 9 shows two typical scans from samples that had been etched different amounts. These data were obtained with one volt reverse bias applied to the diode. The activation energy results for one particular wafer are shown in Figure 10; here the parameter is the amount of silicon removed from the surface. These results are compared with gold in silicon and the results of similar work done by S. Chan et al. [14]. It is seen from this figure that the range of energies observed in our study in no way correspond to the accepted energy levels of gold in silicon, but our results are comparable to other results obtained from precipitated p-type silicon [14]. The test structures used in Ref.14 were diffused pn junction diodes. It was noticed that the activation energy changed slightly with changes in reverse bias and that irrespective of the amount of etch the diodes showed the same reverse bias dependance. As the reverse bias was increased the activation energy was seen to decrease. This is understandable if one assumes a Poole-Frenkel type barrier lowering. Wright etching of the sample again revealed large number of bulk stacking faults. The density of the first 5 microns was essentially zero, indicating a denuded zone, increasing to 10^5 at 25 microns from the surface. A comparison of the bulk stacking fault density with $\Delta C/C$ is shown in Figure 11 for p-type silicon. As can be seen there is a

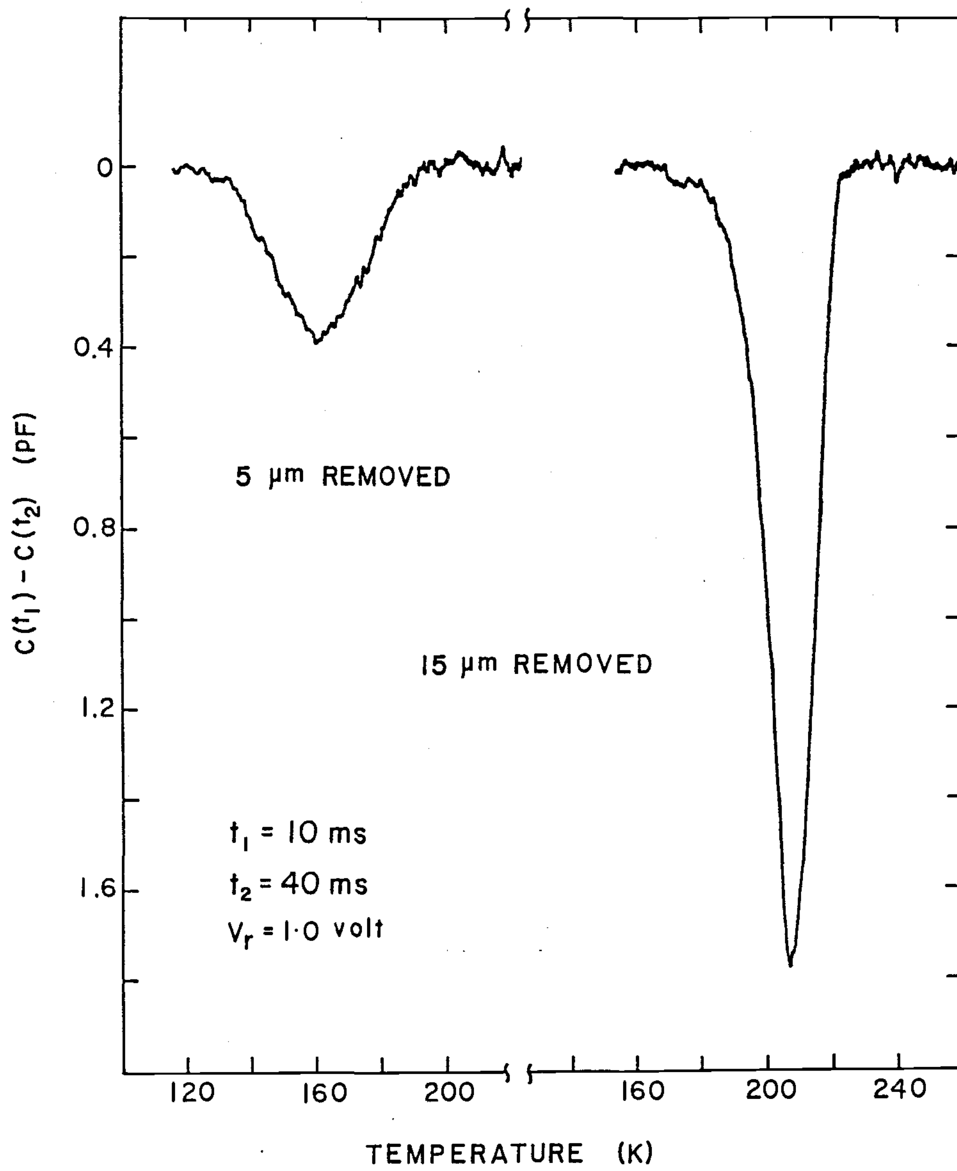


Fig 9. DLTS spectra from precipitated p-type silicon

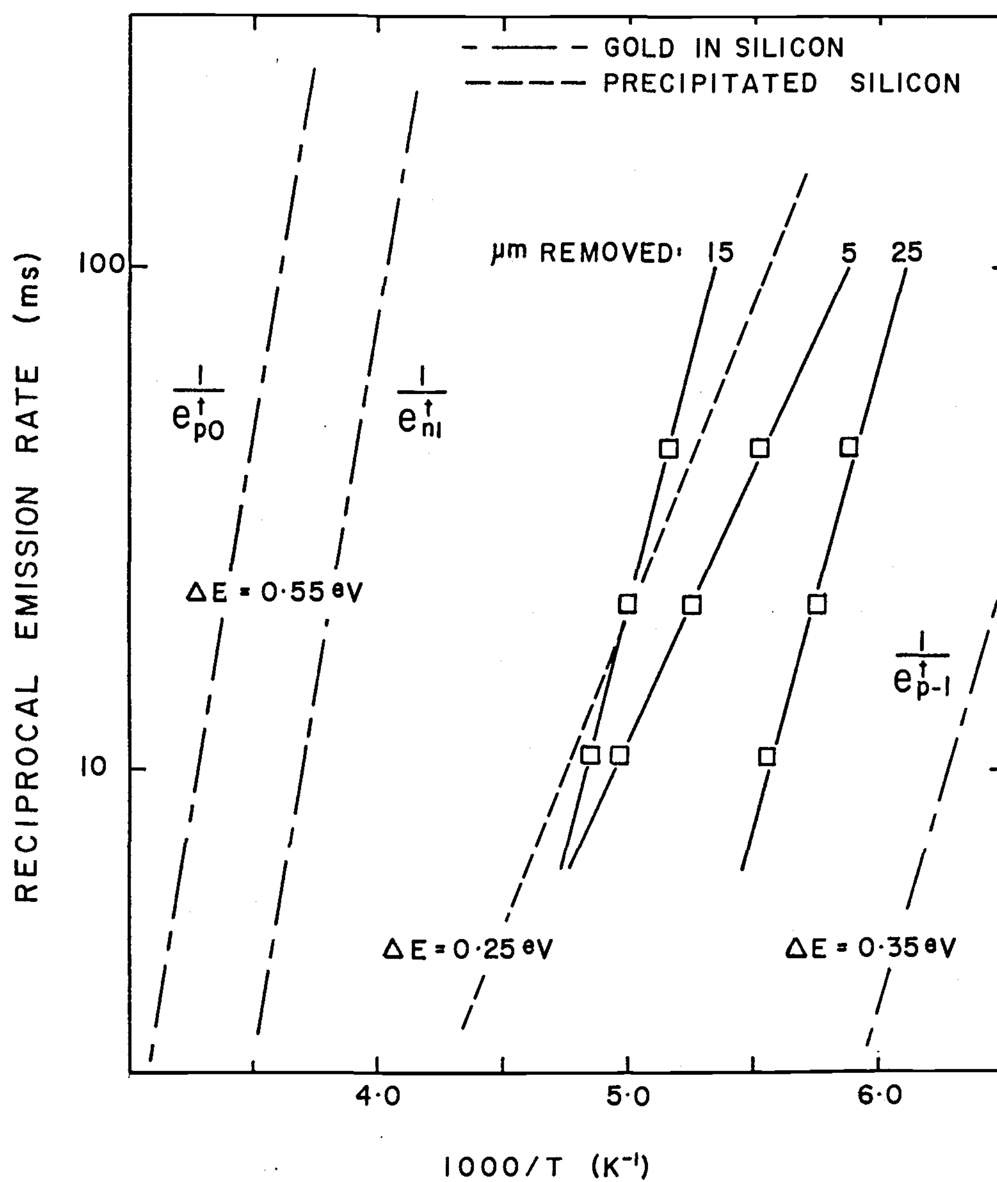


Fig 10. Activation energies for etched p-type silicon

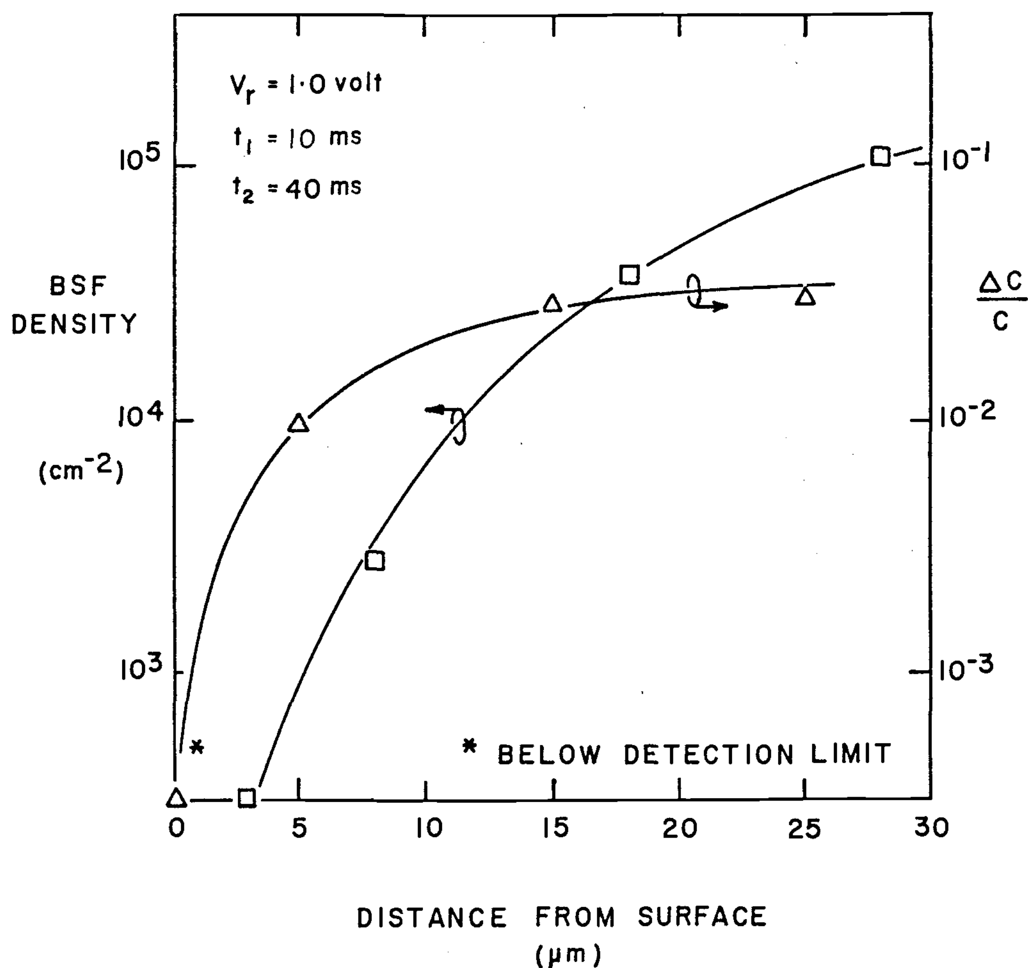


Fig 11. Trap and BSF density profile

general trend for the trap density to increase with increasing stacking fault density. But as the figure shows, trap density at say 5 microns greatly exceeds BSF density. It is assumed then that the deep level traps are not directly associated with bulk stacking faults.

MODELS AND CONCLUSIONS

It has been proposed that the minority carrier trapping observed in p-type silicon [14] is due to precipitation dislocation complexes (PDC). This conclusion was reached because, it was said, the activation energy of the minority carrier trap was identical to that found in heavily

dislocated n-type silicon. It was not stated as to whether PDC were responsible for the observed majority carrier trapping. Previous work done to characterize bandgap energy levels in heavily dislocated p-type silicon [15,16] has revealed a band of allowed energies in the lower half of the bandgap. In particular, DLTS spectra obtained from deformed p-type silicon show a broad peak centered at 0.35 eV above the valence band [15]. This band of states is reportedly due to reconstruction of the dislocation core. Photoconductivity measurements have shown a band of energies from 0.26 to 0.52 eV from the valence band [16]. The center of the band at 0.39 eV corresponds to the energy of the neutral dislocation.

In summary, energy levels observed in heat treated n-type silicon correspond quite closely to levels associated with substitutional gold impurity. Hence we are probably detecting the gettering of heavy metal impurities which are acting as trapping sites. The band of energies seen with the p-type silicon are most likely due to PDC, since it is well known that the low-high heat treatment of silicon wafers with initially high interstitial oxygen induce large amounts of precipitates with dislocation loops. The exact mechanism of the trapping is unclear since the structure of the dislocation core is still unresolved [17].

ACKNOWLEDGMENTS

The assistance of W. Sze is gratefully acknowledged for his heat treatment of the silicon wafers. This work was supported in part by the Intel Research Council.

REFERENCES

[12] L. Forbes, F.D. Whitwer and J.D. Peng in Impurity Diffusion and Gettering in Silicon, Proceedings of the Materials Research Society, Vol.36, Edited by R.B. Fair, C.W. Pearce and J. Washburn (MRS, Pittsburgh, 1985), p.257.

[13] C.T. Sah, L. Forbes, L.I. Rosier, A.F. Tasch, Jr., and A.B. Tole, Appl. Phys. Lett. 15, 145(1969).

[11] L.D. Yau and C.T. Sah, Solid-St. Electron. 17, 193 (1974).

[14] S.S. Chan, C.J. Varker, J.D. Whitfield and R.W. Carpenter in Microscopic Identification of Electron Defects in Semiconductors, Proceedings of the Materials Research Society, Vol. 46, edited by N.M.Johnson, S.G. Bishop and G.D. Watkins, (MRS, Pittsburgh, 1985), p.281.

[15] L.C. Kimerling and J.R. Patel, Appl. Phys. Lett. 34, 73 (1979).

[16] J.J. Kos and D. Heubert, Phys. Stat. Sol. (a), 44, 259 (1977).

[17] H.J. Queisser in Defects in Semiconductors 2, Proceedings of the Materials Research Society, Vol. 14, edited by S. Mahajan and J.W. Corbett, (Elsevier Science Publishers, New York, 1983), p.323.

CURRENT PROBLEMS AND FUTURE DIRECTIONS

ADDITIONAL OBSERVATIONS ON MICRODEFECT RELATED DEEP LEVELS

At the time of writting of the last section the results of the characterization of p-type silicon were thought to be fairly clear [18]. Subsequent study of precipitated p-type silicon has revealed new data that needs to be considered. First of all, DLTS characterization on unetched samples has detected a majority carrier peak similar to that detected on etched samples. This would indicate that hole trapping is occuring up to within one or two microns from the wafer surface. Previously the high leakage currents measured on unetched samples made it very difficult to detect any deep level traps. Etching of the silicon surface prior to aluminium evaporation usually improved the current-voltage characteristics thus reducing the amount of reverse leakage current. To detect the majority carrier trap on etched or unetched samples it was necessary to slightly forward bias the diode in order to fill the trap centers. The usual forward bias voltage was 50-100 mV. It was noticed that as the amount of forward bias was increased the DLTS peak height also increased. This would indicate a larger number of traps were being populated as the forward bias was increased. Another fact that was noticed about the majority carrier trap was the non-exponential capacitance transient. The diode capacitance instead of increasing exponentially increased nearly linearly with time. This effect is seen in the non-symmetrical shape of the DLTS peak. See Figure 9.

Going one step further, Schottky diodes were fabricated on p-type silicon that had received no heat treatment. Again a deep level majority carrier trap was detected. Although in this case the trap density was

lower than any previously detected. Since these samples received no heat treatment the trapping activity must be due to as grown defects. As grown defects have been detected using DLTS in n-type silicon [19] but are unreported in p-type silicon. The level detected in n-type silicon is a shallow level donor ($E_c-E_t=0.13$ eV) that increases in concentration with heat treatment at 450 C. Thus there is reason to suspect that as grown type defects also occur in p-type silicon. A comparison of trap concentrations for as grown and heat treated samples is shown in Figure 12. The figure shows that the heat treated silicon has in general a higher density of traps both at the surface and in the bulk. If one attributes the trapping to oxide precipitates this result is understandable. The as grown silicon is partially precipitated as it cools from the melt. This results in relatively low density of precipitates and hence trapping centers. The amount of precipitation is inversely related to the interstitial oxygen concentration $[O_i]$, which is indicated in the figure. When the as grown samples receive the two step heat treatment described in the previous two chapters the density and the size of the precipitates increase still further. Thus a higher density of traps would be measured on the heat treated samples. The hole trapping mechanism at the precipitate is uncertain though. Assuming the precipitate is an SiO_x complex, there is then an associated positive charge. Thus the trapping of majority carrier holes would be due to capture by a repulsive center. Trapping by repulsive centers is known to exist and would explain the hole trapping that is observed.

An effect that was noticed when the p-type samples were annealed in forming gas was the disappearance of the deep level. Forming gas is 5 per cent hydrogen with the remainder being nitrogen. Hydrogen, as it

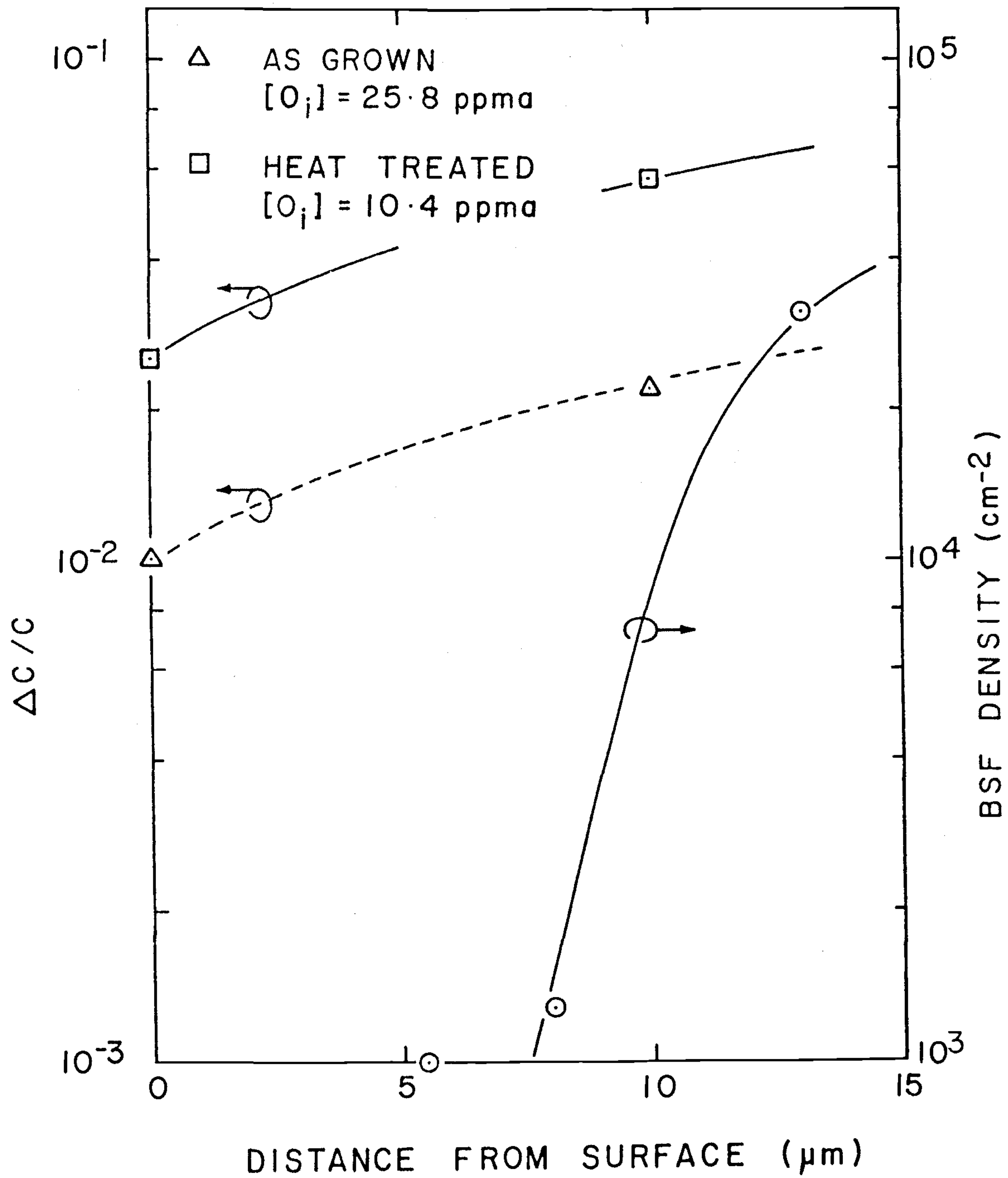


Fig 12. Trap density and bulk stacking fault density profiles for precipitated p-type silicon

diffuses into the silicon is known to neutralize interface states [20] and deep level donors [21] by bonding with a silicon dangling-bond. And since hydrogen diffuses very rapidly even at low temperatures this would account for the absence of any deep level traps after the 20 minute, 450 C anneal.

SUGGESTIONS FOR FURTHER WORK

Two main topics will need to be addressed in future work on p-type silicon. The first is a technological problem that needs to be overcome. That is, the backside contact on the Schottky barrier diodes needs to be ohmic in order to have near ideal current-voltage (I-V) characteristics. The fact that fairly high resistivity substrates are used will cause the I-V characteristics to be slightly non-ideal. The p-type diodes used in this study had less than ideal I-V characteristics in the forward direction. Also a matter of concern is the use of aluminium on p-type silicon for the formation of Schottky barrier diodes. The practical maximum barrier height is only 0.4 eV. A different kind of metal, one which provides a larger barrier height needs to be used. Samarium and Titanium are two metals that could be used for this purpose, both of which are in common use at the present.

The second topic of intrest for future work is a comprehensive model that explains the results for not only p-type but n-type silicon as well. Any model that attempts to explain the deep levels caused by precipitates and other microdefects, should be valid reguardless of the majority carrier type. In the next section a first attempt at such a model, along with its limitations, will be given. It should be noted that the silicon materials used in this study were obtained from different manufacturers at different times. So differences in trace impurities and thermal histories could lead to difficulties in interpreting results and drawing conclusions. Future work should try and concentrate on material from a single vendor.

CONCLUSIONS

The study that has been presented here has shown that the precipitation of oxygen in silicon does indeed change the electrical characteristics of the silicon. One of the most important result is the mid-bandgap level detected in n-type silicon. With an activation energy of approximately 0.55eV this deep level presents a potential problem for the development of high lifetime material. But it is important to note that the trap concentrations of this level are relatively small. The trapping mechanism for this level is not well understood though. The time constant of the trap detected with DLTS is comparable to that of the substitutional gold acceptor (about 1ms at room temperature). But to assume that the trapping is due to heavy metal (gold, copper, iron, nickel) gettering is a matter of debate. The crystaline structure around a defect (precipitate, BSF, etc.) is certain to be altered and hence the potential around a gettered metal atom is also certain to be altered. Of course the crystal structure around a subtitutional metal impurity will be altered too, but in a different way from that of a metal atom gettered at a defect. Also the different heavy metal atoms typically cause various deep levels to occur, not all of which have mid-bandgap energies. To help resolve this question it may be useful to introduce heavy metals into the silicon. The intention here is to test the ability of the defects to getter the metals. Then as the concentration is varied one could look for a correlation with trap density. There may be the problem of traps due to ungettered metals being present. But if the amounts of metal introduced are kept very small, this effect would probably be negligible.

A possible explaination for the trapping observed in n-type silicon

is provided by the positive charge associated with SiO_x complexes. The fixed positive charge would cause electrons to be bound by coulomb attraction to the precipitate [22]. Thus given the proper amount of fixed charge mid-bandgap levels could be possible. The work of Ref. 22 also supposes the existance of interface states between the oxide precipitate and the silicon. These states are analogous to those at the silicon-silicon dioxide interface which exhibit a continuous density of states increasing toward the band edge. Our results do not show the presence of these interface states. The explaination here is that the density is greatly reduced due to the high temperature heat treatment (1050 C for 16 hrs) that the wafers received. The discrete mid-bandgap level that is detected is probably due to bound coulombic states. A possible problem with this model is that it neglects the electrical activity of other microdefects such as bulk stacking faults. This may be a valid assumption though since nowhere in this study has the density of deep level traps been correlated to the bulk stacking fault density. For example, Figure 12 shows that for the heat treated sample at 10 microns from the surface the trap concentration is not substantially higher than at the surface. But at a depth of 10 microns the bulk stacking fault density is approximately 10^4 cm^{-2}, or about 100 stacking faults per diode. Whereas at the surface there are no stacking faults. In other words, bulk stacking faults may be electrically inactive.

The positively charged oxide precipitate model can also be used to explain the results obtained for p-type silicon. If a deep level state is assumed to exist within the precipitate that could trap a majority carrier hole this would explain the level detected by DLTS. The capture of holes by this center is dependent upon the field across the depletion

region of the diode. This is evidenced by the fact that zero bias or a slight forward bias is necessary to populate these trap centers. Then as the voltage is switched back to reverse bias the trapped holes are reemitted and give rise to the capacitance transient. The problem with the model in this case is that it presumes that holes traps exist in SiO_x precipitates. As an example, for SiO_2 the existance of deep level electron traps have been shown. But there is very little evidence as to the existance of hole traps or hole conduction in the literature.

BIBLIOGRAPHY

[1] G.L. Miller, D.V. Lang and L.C. Kimerling, Ann. Rev. Mater. Sci. 7, 377 (1977)

[2] C.T. Sah, R.N. Noyce and W. Shockley, Proc. IRE, 45, 1228, (1957)

[3] C.T. Sah, L. Forbes, L.L. Rosier and A.F. Tasch, Jr., Solid-State Electron., 13, 759, (1970)

[4] D.V. Lang, J. Appl. Phys., 45, 3023, (1974)
D.V. Lang in Thermally Stimulated Relaxation in Solids, Topics Appl. Phys. vol. 37, ed. by P. Braunlich, (Springer, Berlin, Heidelberg, New York, 1979) Chpt. 3

[5] J.L. Hartke, J. Appl. Phys., 39, 4871, (1968)

[6] J. Andrews, in Defects in Silicon, Ed. by W.M. Bullis and L.C. Kimerling (Electrochmical Scociety, Pennington, NJ, 1983) p. 133.

[7] S.M. Hu, Appl. Phys. Lett., 36, 561 (1980).

[8] J.R. Patel, in Semiconductor Silicon 1981, Ed. by H.R. Huff, R.J. Kriegler, and Y. Takeishi (Electrochemical Society, Pennington, NJ, (1981) p. 189.

[9] T.Y. Tan, in Defects in Silicon, Ed. by W.M. Bullis and L.C. Kimerling (Electrochemical Society, Pennington, NJ, 1983) P. 325.

[10] C.T. Sah, L. Forbes, L.L. Rosier, A.F. Tasch and A.B. Tole, Appl. Phys. Lett., 15, 161 (1969).

[11] L.D. Yau and C.T. Sah, Solid-State Elect., 17, 193 (1974).

[12] L. Forbes, F.D. Whitwer and J.D. Peng in Impurity Diffusion and Gettering in Silicon, Proceedings of the Materials Research Society, Vol.36, Edited by R.B. Fair, C.W. Pearce and J. Washburn (MRS, Pittsburgh, 1985), p.257.

[13] C.T. Sah, L. Forbes, L.I. Rosier, A.F. Tasch, Jr., and A.B. Tole, Appl. Phys. Lett. 15, 145(1969).

[14] S.S. Chan, C.J. Varker, J.D. Whitfield and R.W. Carpenter in Microscopic Identification of Electron Defects in Semiconductors, Proceedings of the Materials Research Society, Vol. 46, edited by N.M.Johnson, S.G. Bishop and G.D. Watkins, (MRS, Pittsburgh, 1985), p.281.

[15] L.C. Kimerling and J.R. Patel, Appl. Phys. Lett. 34, 73 (1979).

[16] J.J. Kos and D. Heubert, Phys. Stat. Sol. (a), 44, 259 (1977).

[17] H.J. Queisser in Defects in Semiconductors 2, Proceedings of the Materials Research Society, Vol. 14, edited by S. Mahajan and J.W. Corbett, (Elsevier Science Publishers, New York, 1983), p.323.

[18] F.D. Whitwer, H. Haddad and L. Forbes, presented at Spring 1986 meeting of the Materials Research Society, Symposium F, to be published.

[19] J.R. Patel in Semiconductor Silicon 1981, edited by H.R. Huff R.J. Kriegler and Y. Takeishi, (Electrochem. Soc. Inc., New Jersey 1981), p.189.

[20] N.M. Johnson, D.K. Biegelson and M.D. Moyer, J. Vac. Sci. Technol. 19, 390 (1981).

[21] N.M. Johnson and S.K. Hahn, to be published in Appl. Phys. Lett.

[22] K. Hoelzlein, G. Pensl, M. Schulz and N.M. Johnson, presented at Fall 1985 meeting of the Materials Research Society, Symposium K, to be published.