Problems with Hall devices for instructional use in undergraduate laboratories stimulated this investigation for development of rugged, easily constructed, inexpensive, electrically reproducible Hall devices with high output voltage. Silicon was chosen as the Hall-plate material on the basis of cost and availability. Advantages and disadvantages of various plate shapes, sizes, surface treatments, contact arrangements and types of contacts are discussed. Aluminum evaporation and electroless nickel plating were found to be satisfactory for making contact to the p- and n-type silicon plates, respectively. The final products chosen consisted of Hall plates of about 1.0 in x 0.235 in x 0.007 in which were placed on circuit board and connected by spring contact (phosphor-bronze wire) to the external circuitry. The effects of band structure, scattering mechanisms and plate geometry were considered in predictions of Hall voltage for two p-type and three n-type Hall plates. Agreement was obtained between theory and experiment to the author's satisfaction.
Hall-Effect Devices for Instructional Use

by

Gerald Frederick Dills

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TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>Chapter</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>I. INTRODUCTION</td>
<td>1</td>
</tr>
<tr>
<td>II. HALL-PLATE DESIGN--THEORETICAL CONSIDERATIONS</td>
<td>5</td>
</tr>
<tr>
<td>Plate Material and Shape</td>
<td>5</td>
</tr>
<tr>
<td>Differences in Lapped and Polished Silicon Surfaces</td>
<td>7</td>
</tr>
<tr>
<td>Important Methods for Making Electrical Contact to Silicon</td>
<td>8</td>
</tr>
<tr>
<td>p-Type Silicon</td>
<td>8</td>
</tr>
<tr>
<td>n-Type Silicon</td>
<td>10</td>
</tr>
<tr>
<td>Contact Arrangements</td>
<td>11</td>
</tr>
<tr>
<td>III. FACTORS AFFECTING DEVICE PERFORMANCE</td>
<td>24</td>
</tr>
<tr>
<td>Extrinsic p-Type Silicon Hall-Coefficient Factor</td>
<td>24</td>
</tr>
<tr>
<td>Extrinsic n-Type Silicon Hall-Coefficient Factor</td>
<td>28</td>
</tr>
<tr>
<td>The Seebeck Effect</td>
<td>29</td>
</tr>
<tr>
<td>The Peltier Effect</td>
<td>29</td>
</tr>
<tr>
<td>IV. EXPERIMENTS CONDUCTED</td>
<td>34</td>
</tr>
<tr>
<td>Investigation of Aluminum-Evaporated Contacts on Silicon</td>
<td>34</td>
</tr>
<tr>
<td>Investigation of Electroless Nickel Contacts</td>
<td>35</td>
</tr>
<tr>
<td>Plate-Shaping and Cleaning Processes</td>
<td>36</td>
</tr>
<tr>
<td>Hall Plate Construction and Testing</td>
<td>38</td>
</tr>
<tr>
<td>The p-Type Plates</td>
<td>39</td>
</tr>
<tr>
<td>The n-Type Plates</td>
<td>41</td>
</tr>
<tr>
<td>V. EXPERIMENTAL RESULTS</td>
<td>44</td>
</tr>
<tr>
<td>Aluminum Evaporated Contacts</td>
<td>44</td>
</tr>
<tr>
<td>Electroless Nickel Contacts</td>
<td>45</td>
</tr>
<tr>
<td>Two-Ohm-Cm, p-Type Silicon</td>
<td>45</td>
</tr>
<tr>
<td>One-Ohm-Cm, n-Type Silicon</td>
<td>45</td>
</tr>
<tr>
<td>Plate-Shaping Processes</td>
<td>46</td>
</tr>
<tr>
<td>Hall-Plate Resistivity and Hall-Voltage Measurements</td>
<td>46</td>
</tr>
<tr>
<td>Magneto-Resistance</td>
<td>53</td>
</tr>
<tr>
<td>Lapped-Edge and Polished Plates</td>
<td>53</td>
</tr>
<tr>
<td>VI. DISCUSSION OF RESULTS</td>
<td>54</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td>54</td>
</tr>
<tr>
<td>Plate-Shaping Process</td>
<td>54</td>
</tr>
</tbody>
</table>
Chapter
Plate Performances  54
      The p-Type Plates  54
      The n-Type Plates  55
Thermal Effects on Transverse Voltage  56
Plates with Lapped and Polished Surfaces  57

VII. CONCLUSIONS  58
      The p-Type Plates  58
      The n-Type Plates  59
      Objectives Revisited  59

BIBLIOGRAPHY  61
## LIST OF TABLES

<table>
<thead>
<tr>
<th>Table</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Approximate contact resistance of aluminum evaporated and alloyed contacts on one-ohm-cm, p-type, (111)-plane silicon.</td>
<td>44</td>
</tr>
<tr>
<td>2. Approximate contact resistance of electroless nickel on one-ohm-cm, n-type, (111)-plane silicon.</td>
<td>45</td>
</tr>
<tr>
<td>3. Comparison of observed and predicted transverse voltages for two two-ohm-cm, p-type silicon Hall plates of Plate (e) electrode configuration at $B = 4.8$ kG.</td>
<td>48</td>
</tr>
<tr>
<td>4. Comparison of observed and predicted transverse voltages for two ten-ohm-cm, n-type, silicon Hall plates of Plate (e) electrode configuration at $B = 4.8$ kG.</td>
<td>51</td>
</tr>
</tbody>
</table>
# LIST OF FIGURES

<table>
<thead>
<tr>
<th>Figure</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Schematic of circuitry for measurement of the Hall voltage.</td>
<td>4</td>
</tr>
<tr>
<td>2. Possible contact arrangements considered for rectangular Hall plates.</td>
<td>13</td>
</tr>
<tr>
<td>3. Schematic of circuitry used for Hall-voltage measurements with all voltage electrodes on one side of the Hall plate.</td>
<td>13</td>
</tr>
<tr>
<td>4. Equipotentials in a p-type Hall plate with no magnetic field applied.</td>
<td>15</td>
</tr>
<tr>
<td>5. Equipotentials in a p-type Hall plate with a magnetic field directed into the page.</td>
<td>15</td>
</tr>
<tr>
<td>6. Effect of current-contact shorting on Hall-voltage measurements using the bridge technique.</td>
<td>17</td>
</tr>
<tr>
<td>7. Shorting of the Hall voltage by transverse contacts.</td>
<td>22</td>
</tr>
<tr>
<td>8. Comparison of observed and predicted transverse voltages of two p-type silicon Hall plates.</td>
<td>49</td>
</tr>
<tr>
<td>9. Comparison of observed and predicted transverse voltages of two n-type silicon Hall plates.</td>
<td>52</td>
</tr>
</tbody>
</table>
HALL-EFFECT DEVICES FOR INSTRUCTIONAL USE

I. INTRODUCTION

Problems with Hall devices for instructional use in undergraduate laboratories stimulated this investigation for the development of rugged, high-output devices which are easily constructed, inexpensive and reproducible in electrical characteristics. Commercially available Hall devices may be fragile, expensive, not readily available or lacking in visually instructive qualities. Silicon is the most readily available and economical semiconductor for the Hall-plate material; however past efforts at making ohmic contacts of low resistance between Hall plates and the external circuitry have been unsatisfactory because of degradation of their electrical characteristics with time and their fragility. Breakage of the Hall plates during use in the undergraduate laboratories has also occurred. It was therefore desirable to develop Hall-effect devices which are breakage-resistant and have ohmic, low-resistance, long-lasting contacts. The fabrication processes should be simple enough so students can build the devices without much difficulty. Connections to the Hall plates should be visible so students can easily see how the Hall plates are connected to the external circuitry. In summary, the products desired are breakage-resistant, reproducible Hall devices with ohmic, low-resistance current contacts. In addition, ease of
fabrication, high output voltage and low cost are other important considerations in the choice of the final products. To find a desirable compromise among the above considerations is the purpose of the investigation described below.

Basically, the Hall effect is the production of a voltage across an electrically conductive medium, the voltage being transverse to current flowing through the medium and to an applied magnetic field. A schematic of an experimental arrangement for measurement of the Hall voltage is shown in Figure 1, where $B$, $I$, $L$, $w$ and $t$ are the applied magnetic field, the current flowing through the Hall plate, and the Hall plate length, width and thickness, respectively. As the current carriers flow along the length of the plate, they are slightly deflected by the Lorentz force, which is described by the equation

$$\vec{F} = q\vec{V} \times \vec{B}$$  \hspace{1cm} (1)

where $\vec{F}$ is the force on a current carrier of charge $q$ and velocity $\vec{V}$. According to Equation (1), the force experienced by the carriers is perpendicular to both the directions of carrier motion and the magnetic field. Since some of the carriers which experience the force are restricted by the walls of the Hall plate, charge builds up at the plate edges, causing an electric field which cancels the electric field associated with the Lorentz force within the Hall plate. These fields are related to the Hall voltage, the magnitude of which is given
by the equation (Putley, 1960, p. 99).

\[ V_H = \frac{R_H IB}{t} = \frac{rIB}{\text{net}} \]  

(2)

Here \( R_H \), \( n \), \( e \), and \( r \) are the Hall coefficient, the majority carrier concentration, the signed magnitude of the charge on each majority carrier and the Hall-coefficient factor, respectively. Note that the Hall coefficient for a semiconductor has the same sign as that of the majority carriers. The Hall-coefficient factor depends on a number of the characteristics of the Hall-plate material and on the conditions of measurement, to be elaborated on in Chapter III.
Figure 1. Schematic of circuitry for measurement of the Hall voltage.
HALL-PLATE DESIGN--THEORETICAL CONSIDERATIONS

Plate Material and Shape

The shape, size and type of material for the Hall plates were the first problems that arose in the design of the Hall devices. As mentioned above, silicon with both n- and p-type dopants is inexpensive and readily available. Silicon is about one-fifth the cost of germanium. It is desirable to have both n- and p-type Hall plates made of the same element so that students need not question whether the Hall-voltage polarity is different for the two types of plates because of some difference in the materials other than the type of impurity doping. The investigation therefore proceeded considering only silicon as the Hall-plate material, and was found to be acceptable. Hall-plate shape was the next subject of concern.

Isenberg, Russell and Green (1948) have shown that if the length-to-width ratio of a rectangular-parallelopiped-shaped Hall plate is less than four, the Hall voltage is reduced from the value obtained for a plate of length-to-width ratio four. This assumes that the plate has two contacts for the measurement of the Hall voltage placed halfway along its length, and that no electric field exists perpendicular to the length of the plate at the ends of the plate. This latter condition results in a shorting of the Hall voltage for L/w less than four. It will be shown below that two types of transverse-contact
shorting exist. The magnitude of one varies directly with the degree of spacing of the resistivity-measurement contacts from the middle of their plate edge, while that of the other varies with the percentage of the plate width traversed by the transverse contacts. Plates of length-to-width ratio four were chosen for experiments because of their higher output voltage.

In the above discussion, it has been assumed that the Hall plates are rectangular. This is the most desirable shape for several reasons. Hall measurements may be made on arbitrarily shaped samples, however related calculations are somewhat elaborate, and this technique is usually reserved for materials that cannot be easily shaped. Many Hall plates are rectangular parallelopipeds with enlarged ends for the current contacts and have two or three fingers extending from each edge for Hall-voltage measurements. Such shapes are cut by impact grinders. This cutting process may easily take over an hour for a plate of seven mils thickness and can easily result in breakage of some of the transverse fingers. A silicon wafer can be scribed and broken or cut with a diamond saw into a rectangular shape in a fraction of the time necessary for the grinding process. On the basis of speed of fabrication, scribing and breaking and diamond saw cutting were chosen for experimental investigation.
Differences in Lapped and Polished Silicon Surfaces

The surface treatments Hall plates undergo are important factors in determining the performances of high-resistivity Hall devices, as shown by Colman and Kendall (1969). Their apparent sample resistivities and mobilities varied drastically after dipping the samples in 48% hydrofluoric acid and subsequently in boiling, deionized water. The apparent mobilities and resistivities of the samples were also highly dependent on the length of time the samples were kept in the deionized water. Sandblasted samples of the same resistivity material illustrated, in general, much less dependence of the apparent mobilities and resistivities on the hydrofluoric acid and boiling, deionized water dips; however, the apparent mobility for high-resistivity, p-type silicon did undergo great variation. The authors also mention significant deviations in the apparent mobilities and resistivities of one-ohm-cm, polished silicon which has undergone the same treatment. This suggested to the author that the performances of one- or ten-ohm-cm Hall plates made of polished silicon might also be highly dependent on buffered, four-to-one hydrofluoric acid treatments. Since dipping silicon in buffered HF is a necessary step in low-resistence contact formation to silicon by aluminum evaporation or electroless nickel plating, this is an important consideration. These are two simple, effective methods of
making contact to silicon. It has also been found that electroless nickel does not adhere well to polished silicon.

**Important Methods for Making Electrical Contact to Silicon**

**p-Type Silicon**

One highly successful method for making ohmic, low-resistance contact to p-type silicon of low resistivity is by aluminum evaporation and alloying. Using this method, all contacts may be applied simultaneously. McNeil (1969) found that contacts consisting of aluminum evaporated onto silicon wafers that were alloyed in a nitrogen atmosphere for five minutes at 500°C resulted in the lowest contact resistance obtained to p-type silicon of $7 \times 10^{18}$ cm$^{-3}$ acceptor concentration. Information on lower acceptor concentrations was not found by the author. If a tungsten filament which has previously been wetted by aluminum is used, the evaporation is a simple process to carry out. The problem of making contact between the external circuitry and the aluminum contacts can be solved by making pressure contacts utilizing phosphor-bronze wire.

Electroless nickel was considered for making contact to p-type silicon. This process, like aluminum evaporation, allows for simultaneous contact formation. Teramoto, Hitoo and Tai (1968) have shown that low-resistance contacts to highly-doped silicon may be
obtained by depositing electroless nickel on the silicon, then alloying in a nitrogen atmosphere for 30 minutes at temperatures between 450° and 600°C. It was shown, however, that as the acceptor concentration decreased from $10^{19}$ cm$^{-3}$ to $10^{18}$ cm$^{-3}$, the contact resistance increases by a factor of 100. Sullivan and Eigler (1957) reported obtaining contact resistances of about 20 ohm-mm$^2$ for electroless nickel alloyed to 1.5 ohm-cm, p-type silicon at temperatures between 100°C and 500°C for a period of one hour. Contacts formed by electroless nickel plating have the advantage that they may be soldered to and the necessary equipment and procedure for making the contacts are very simple.

The ultrasonic bonding of aluminum wire was the last technique considered for making contact to p-type silicon. This method involves rubbing a fine aluminum wire against the silicon surface at a high (ultrasonic) frequency. The friction generates heat and causes a spot weld. The problem of how to connect the aluminum wire to the external circuitry arises, however. Also, the wire might easily break with continued usage in undergraduate laboratories, or the wires might be pulled off the silicon. The ultrasonic bonding process is difficult for a student to learn, compared to aluminum evaporation or electroless nickel plating. The bonding machine may require adjustment, and appreciable set-up time might be necessary for an undergraduate student trying to make such a bond. Also, degradation
of this type of contact with time has been observed in Hall devices built in our laboratories, possibly due to the formation of oxide beneath the aluminum wires.

**n-Type Silicon**

Sullivan and Eigler (1957) have shown that alloying electroless nickel contacts to one-ohm-cm, n-type silicon at a temperature of 700°C yields a contact resistance of about two ohm-mm². Basu, Paria and Nag (1968) obtained ohmic contact to five-ohm-cm, n-type silicon without alloying electroless nickel deposits on lapped surfaces.

The thermocompression-bonding technique (Anderson, Andreatch and Christensen, 1957; Hemment, 1966) is one in which the end of a fine, antimony-doped, gold wire is heated to form a small ball at the end of the wire, and the ball is pressed against the silicon (heated to about 320°C) where the bond is desired. The resulting contact is ohmic and has a resistance of about 1000 ohms on 900 ohm-cm, n-type silicon. Hemment (1966) notes that a rectifying contact may be formed using the procedure if any contamination exists on the gold ball. The process is also somewhat undesirable in that, as in the case of ultrasonic bonding, the bond cannot be made without some amount of time having been spent adjusting the bonder and practicing the bonding technique.

It is also possible to use aluminum evaporation to make ohmic
contact to n-type silicon by making a shallow \( n^+ \) diffusion, such that strongly n-type regions are created at the locations where the contacts are desired. Thus when aluminum is alloyed into the silicon, its acceptor behavior does not result in the formation of a p-n junction within the semiconductor, as would be the case if aluminum were allowed to diffuse into a lowly-doped n-type region of silicon. But this process has the disadvantage of requiring considerably more construction time than is necessary for making p-type silicon-aluminum contacts. Oxide must be grown and etched and a phosphorus diffusion must be performed prior to the evaporation.

On the basis of ease of device construction, expected device reliability and ruggedness, aluminum evaporation and electroless nickel plating were considered for experiments. The final choice of contact type was determined from the experimental results, described in Chapter V. Since the Hall plates are taken from silicon wafers of from six to nine mils thickness, it is most practical to attach all contacts to one side of the plate, thus allowing for the formation of all necessary contacts simultaneously. The next consideration made was the type of contact arrangement desired.

**Contact Arrangements**

Two types of contacts are necessary for operation of the Hall plates. The first type provides for the passage of electrical current
through the plate and the second for making plate resistivity and Hall voltage measurements. Some general types of contact arrangements considered for the Hall plates are shown in Figure 2. It is desired that students be able to measure the resistivities of the plate material. Since appreciable current passes through the end contacts of all the plates shown in Figure 2, the voltage measured between any two contacts in series along the plates would include the voltage across at least one of the current (end) contacts unless at least two transverse contacts are provided. Since this latter voltage is a characteristic of the type of contact and not of the Hall plate semiconductor, plates for which resistivity measurements must involve one of the current contacts are undesirable. Transverse contacts interconnected by a high-impedance voltmeter conduct very little current compared to the current contacts. Consequently, if two transverse contacts are used for resistivity measurements, the voltmeter will more accurately indicate the potential difference along the plate than if one or two current contacts are used because of the smaller potential drops across the transverse contacts. In order for transverse contacts to be used for resistivity measurements, at least two contacts must be on the same side of the plate. Thus Plates (a) and (c) are eliminated from consideration.

If Plate (b) is used, the Hall voltage must be measured as illustrated in Figure 3, and only one-half the Hall voltage is measured.
Figure 2. Possible contact arrangements considered for rectangular Hall plates.

Figure 3. Schematic of circuitry used for Hall-voltage measurements with all voltage electrodes on one side of the Hall plate.
This is because nulling the voltmeter reading effectively places the voltmeter lead which is connected to the potentiometer in the center of the plate, as indicated by the dashed line and \( x \) in Figure 3. This can be understood as follows. When current is flowing through the Hall plate and no magnetic field is applied, the equipotentials within the plate are approximately as illustrated in Figure 4. The potentiometer is taken to be adjusted such that the voltmeter reading is zero. Thus the potentials at Points A, B, C, and D are equal. Figure 5 shows the same circuit, only with a magnetic field applied perpendicular to the plane of the Hall plate. Point A is raised in potential by the same amount Point C is lowered. Thus only one-half of the Hall voltage is measured using Plates (a) and (b). These plates were therefore rejected in favor of the plates with transverse contacts on both sides of each plate, since these plates produce about twice as much transverse voltage as those with transverse contacts on only one side of the plate.

The number of desirable contact arrangements can be narrowed down further by applying boundary conditions resulting from the large-area current contacts on the ends of most of the Hall plates. As mentioned above, large-area current contacts which extend across the entire width of a Hall plate have the effect of reducing the observed transverse voltage to less than the calculated Hall voltage if the length-to-width ratio of the plate is less than four. This arises from
Figure 4. Equipotentials in a p-type Hall plate with no magnetic field applied.

Figure 5. Equipotentials in a p-type Hall plate with a magnetic field directed into the page.
the fact that the current contacts are of very low resistivity, and any transverse component of the current within the contacts results in a negligibly small transverse voltage. Thus the metal contacts can be considered equipotentials. The transverse voltage across a Hall plate reaches a maximum midway between the current contacts and decreases continuously to zero at the current contacts. Now consider the effect this has on attempted measurement of the Hall voltage by the bridge technique (illustrated in Figure 1) when the transverse contacts are far from the center of the plate, as illustrated in Plate (f) of Figure 2.

Part (a) of Figure 6 shows the bridge arrangement for measurement of the Hall voltage using Plate (f), the equipotentials being drawn for the case of no magnetic field applied and the potentiometer adjusted such that the voltmeter reading is zero. Thus the potentials at $P_2$, $P_3$, and $C_5$ are equal.

Part (b) of Figure 6 shows the same circuit with a magnetic field applied perpendicular to the plane of the plate. The settings of the circuit components have not been changed and the equipotentials have been drawn neglecting the current-contact shorting effect. As can be seen from Part (b), the potentials of $C_3$, $P_3$, $C_4$ and thus $P_2$ are all raised an equal amount since all the equipotential lines are parallel. Contact $C_5$ is lowered by the same amount $P_2$ is raised in electrical potential. Since the shorting effect of the current
Figure 6. Effect of current-contact shorting on Hall-voltage measurements using the bridge technique. Part (a) shows the Hall-voltage circuitry with plate equipotentials for no $B$ applied and the voltmeter nulled. Part (b) shows the resultant equipotentials with $B$ applied and the current-contact shorting effect neglected. In Part (c) the equipotentials are shown modified by the current contacts.
contacts is neglected in Part (b), the proper Hall voltage is indicated by the voltmeter.

In Part (c), the effect of current-contact shorting is illustrated. In this case (the physically real one) the changes in potential at \( C_3 \), \( C_4 \), and \( P_3 \) due to the application of the magnetic field are no longer equal. Of \( C_3 \), \( C_4 \) and \( P_3 \), the latter experiences the greatest increase in potential upon application of a magnetic field, since the shorting effect is minimal at the center of the plate, and can be taken as zero if the part of the plate not covered by the current contacts has a length-to-width ratio greater than or equal to four.

Assuming \( C_3 \) and \( C_4 \) are equidistant from the center of the plate, the potentials of \( C_3 \) and \( C_4 \) in Part (c) are lowered from their respective counterpart values in Part (b) by the same amount. Thus the amount of current flowing through the potentiometer in the voltmeter circuit does not change in going from the situation depicted in Part (b) to that in Part (c) of Figure 6. The potential differences between Point \( P_1 \) and Point \( P_2 \) in Parts (b) and (c) are thus identical. Therefore, since the potentials at \( P_1 \) and \( C_3 \) are equal within each part of Figure 6 and the potential at \( C_3 \) in Part (c) is lower than the potential at \( C_3 \) in Part (b), the potential of \( P_2 \) in Part (c) must be lower than the potential of \( P_2 \) in Part (b). The potentials of \( C_5 \) in Part (b) and \( C_5 \) in Part (c) are equal since the current-contact shorting effect is negligible midway between the
current contacts for a plate of length-to-width ratio greater than or equal to four. Thus the voltage indicated by the voltmeter in Part (c) is less than the Hall voltage. The magnitude of this effect depends on the distance of \( C_3 \) and \( C_4 \) from the center of the plate. The effect can therefore be minimized by moving the transverse voltage contacts closer together than in Plate (f), like those of Plate (e) in Figure 2. Plate (f) was therefore rejected in favor of Plate (e) because of the desire to maximize transverse voltage.

Plate (g) is inferior to Plate (e) in that the former requires slightly greater construction time and cost than the latter because of the extra wires necessary for the additional contact. Also, it is expected that the two contacts half-way along the length of Plate (g) would be slightly mis-aligned. This would necessitate taking averages of transverse voltage with the plate current in forward and reverse directions. Experimental results indicate that this is not necessary if the bridge technique is used, since the differences between transverse voltage measurements for the two current directions are less than the experimental error. Also, the current-contact shorting of the transverse voltage is greater for Plate (g) than for Plate (e). For these reasons, Plate (g) was rejected in favor of Plate (e).

Mis-alignment of center contacts could also present problems for Plate (d), for which the bridge technique is not applicable if the
lower voltage contact is mis-aligned away from the other voltage contacts. The plate has the advantages, however, that if the mis-alignment voltage is negligibly small for large current (say 20 ma) through the plate, the current-contact shorting effect is eliminated for a plate of length-to-width ratio four, and plate resistivity measurements can be made without using the current contacts. The Plate (d) contact arrangement was therefore tested to see if mis-alignment voltage could be a problem for this design (Chapters IV and V).

Making the current contacts as those of Plate (h) largely removes the boundary condition for current-contact shorting and should result in negligibility of the current-contact shorting for a plate of length-to-width ratio four or less. However in order for the current to reach the edges of the plate, it must produce ohmic drops across the width of the plate. This is clearly undesirable since one wants to measure transverse voltages produced by the Lorentz field only.

Plate (i) has the advantages that it minimizes current-contact resistance (as opposed to the Plate (d) design) and has no shorting of the Hall voltage by the current contacts. It has the disadvantage that greater length-to-width ratio plates must be narrower than the shorter ones in order that the same number of long plates can be taken from a wafer of given size. Assuming a single optimal size for the transverse contacts, transverse-contact shorting (discussed
below) is larger for the longer plates than the shorter plates. A plate of this type was built and tested (Chapters IV and V) to see if significant current contact shorting existed for several Type (e) plates that had already been constructed. Only one plate was made since the Type (e) deviation from theory was so large (about 60% of predicted transverse voltage). If current-contact shorting were responsible for the deviation, the author was sure the Type (i) plate would perform quite differently from the Type (e) plates.

Consider the effects of transverse voltage contacts in the middle of the Hall plate. The equipotentials in the plate are tilted from the vertical by a very small amount and would appear vertical if correctly drawn on the equipotential diagrams above. There exists, however, a shorting of the Hall voltage due to the transverse contacts, as illustrated in Figure 7. The potentials of the low-resistivity metal contacts are those of the respective equipotentials running through their centers. These equipotentials are closer together than those which determine the Hall voltage. Identifying a as the distance between a transverse-contact center and the nearest plate edge, the observed transverse voltage for the contact arrangement shown in Part (a) of Figure 7 is

\[ V_{2,3} = \frac{b-2a}{b} V_{1,4} \]
Figure 7. Shorting of the Hall voltage by transverse contacts. Part (a) shows the transverse contacts taking the potentials of the equipotentials passing through their geometric centers, i.e., $E_2$ and $E_5$. Part (b) shows the Hall voltage between Points 1 and 4 is greater than the voltage measured in Part (a).
where \( V_{2,3} \) is the voltage measured across the transverse contacts, \( V_{1,4} \) is the actual plate transverse voltage and \( b \) is the width of the plate. It is thus desirable to minimize the distance the transverse contacts extend across the width of the plate while making adequate area for easy contact formation.
III. FACTORS AFFECTING DEVICE PERFORMANCE

It is the purpose of this chapter to illustrate approximate calculations of the Hall-coefficient factors for p- and n-type silicon Hall plates of rectangular geometry, describe the Seebeck and Peltier effects, and present a calculation showing the importance of a Seebeck voltage on resistivity measurements.

**Extrinsic p-Type Silicon Hall-Coefficient Factor**

The Hall mobility $\mu_H$ is defined as the product of the conductivity $\sigma$ and the Hall coefficient $R_H$. The ratio of the Hall mobility to the conductivity mobility $\mu$ is the Hall-coefficient factor $r$. This is calculated for semiconductors by averaging $\mu_H/\mu$ over participating bands according to their carrier concentrations (Beer, 1963, pp. 184-185). It has been shown that deviation of the shape of the constant energy surface of a particular carrier band from sphericity is associated with a reduction of $\mu_H/\mu$ for that band from unity. Values of 0.979 and 0.749 are listed by Beer (1963, pp. 184, 198) for these ratios for the light- and heavy-mass bands of silicon, respectively. These values presume that the product of the carrier mobility and the magnetic field (in webers/cm$^2$) is much less than unity, a condition satisfied in the Hall-voltage experiments described in Chapter IV. Also, the carrier collision-relaxation times
are assumed to be energy independent.

On the energy band diagram of the valence band of silicon at
k = 0, the split-off band is separated from the junction of the heavy-
and light-hole bands by 0.04 ev (Beer, 1963, p. 210). The hole con-
centrations in each band are calculated from the formula (Beer, 1963,
p. 180)

\[ p_i = \frac{2a_i (2\pi m_i kT/h^2)^{3/2}}{e^{-(E_f - E_{vi})/kT}} \]

(4)

where \( m_i \) is the density-of-states effective mass for the holes, \( a_i \)
is an anisotropy factor and \( E_{vi} \) is the level of the top of the par-
ticular valence band at \( k = 0 \). From Equation (4), it is easily seen
that the ratio of the split-off to heavy-hole concentrations is given by

\[ \frac{p_1}{p_2} = \frac{a_1/a_2 (m_1/m_2)^{3/2}}{e^{-(E_f - E_{v1})/kT} - (E_{v2} - E_f)/kT} \]

(5)

where \( p_1 \) is the split-off-band hole concentration. Equation (5)
may be simplified to yield

\[ \frac{p_1}{p_2} = \frac{a_1/a_2 (m_1/m_2)^{3/2}}{e^{-(E_{v2} - E_{v1})/kT}} \]

(6)

The room-temperature value of \( kT \) is 0.0259 ev. The exponential
in Equation (6) is thus equal to about 0.213. The equation for the
split-off valence band of allowed energy states is given by
Dresselhaus, Kip and Kittel (1955, p. 380, 382) and Dexter, Zeiger and Lax (1956, p. 641) as

\[ E(k) = -0.04 - 2\hbar^2 k^2 / m_0 \]  

(7)

after substitution of the appropriate constants for silicon, \( m_0 \) being the free-electron rest mass. It is seen from Equation (7) that the constant-energy surface for the split-off band is spherical. The anisotropy factor \( a_1 \) is therefore unity (Beer, 1963, p. 180). The effective mass is defined as (Wang, 1966, p. 165).

\[ \frac{1}{m} = (\frac{1}{\hbar^2}) \frac{\partial^2 E(k)}{\partial k^2} \]  

(8)

for a band with a spherical constant-energy surface, where \( m \) is the effective mass. The effective mass for the split-off band may then be determined by substituting Equation (7) into Equation (8), which yields

\[ m_1 = 0.25m_0 \]  

(9)

where \( m_1 \) is the split-off band effective mass. Wang (1966, p. 186) gives the value for the average heavy-hole effective mass as \( 0.50m_0 \). The heavy-hole anisotropy factor is given by Beer (1963, p. 184) as 1.186. Using these in Equation (6) yields

\[ p_1/p_2 = (1/1.186)(0.25m_0 / 0.50m_0)^{3/2} (0.213) \]  

(10-a)
\[ \frac{p_1}{p_2} = (0.843)(0.353)(0.213) = 0.063 \]  (10-b)

In the same manner, the ratio of light- to heavy-hole concentrations may be calculated. This has been done by Beer (1963, p. 184) with the result
\[ \frac{p_3}{p_2} = 0.157. \]  (11)

The Hall-coefficient factor is calculated from the relation
\[ r_p = \frac{(\mu_{H1}/\mu_1)(p_1/p_2)+(\mu_{H2}/\mu_2)(p_2/p_2)+(\mu_{H3}/\mu_3)(p_3/p_2)}{p_1 + p_2 + p_3} \]  (12)

Dividing numerator and denominator by \( p_2 \) yields
\[ r_p = \frac{(\mu_{H1}/\mu_1)(p_1/p_2)+(\mu_{H2}/\mu_2)+(\mu_{H3}/\mu_3)(p_3/p_2)}{(p_1/p_2) + 1+(p_3/p_2)} \]  (13)

Using values from above in Equation (13) yields
\[ r_p = \frac{(1)(0.063)+(0.749)+(0.979)(0.157)}{0.063+1+0.157} \]  (14-a)
\[ r_p = \frac{(0.978)/(1.220) = 0.79} { } \]  (14-b)

Several points are of note concerning the above calculation. The values of effective masses used were measured at low temperatures. Effective masses exhibit some temperature dependence. The values used in the above calculation are, however, expected to be
accurate to within ten percent at the highest temperatures (Bagguley, Stradling and Whiting, 1961). It has been speculated by Beer (1963, p. 205) that the warping of the constant-energy surfaces may be greater than has been supposed. Also, the assumption that the collision-relaxation times for the three bands are constants is rather artificial, unless neutral-impurity scattering is of major importance (Conwell and Debye, 1954, p. 700). Assuming dominance of acoustical phonon scattering, one multiplies the Hall-coefficient factor calculated using the energy-independent relaxation time assumption by a factor of 1.18 to obtain a result of 0.93 (Beer, 1963, p. 124, 182-184, 198). This is the value used in the Hall-voltage calculations of Chapter IV for the p-type plates.

Extrinsic n-Type Silicon Hall-Coefficient Factor

Assuming dominance of acoustical phonon scattering, one may calculate the Hall-coefficient factor from the equation (Beer, 1963, p. 232)

$$r_n = \frac{3\pi}{8} \left[ \frac{(3K)(K+2)}{(2K+1)^2} \right]$$  \hspace{1cm} (15)

where K is the ratio of longitudinal to transverse effective masses divided by the ratio of the corresponding collision relaxation times. This formula applies to silicon as well as germanium, r being independent of the arrangement of the ellipsoids in k-space (Beer,
The important consideration is that the ellipsoids possess cubic symmetry. Values of $K$ have been determined by several investigators, the room-temperature values ranging around $K = 5$. Using this value in Equation (15) yields

$$r_n = \frac{3\pi}{8} \frac{(15)(7)}{(11)^2} = 1.02$$

(16)

This is the value used in the $n$-type Hall plate theoretical calculations of Chapter IV.

**The Seebeck Effect**

If a temperature gradient is set up within a semiconductor, a net diffusion of majority carriers from the region of higher temperature to the region of lower temperature occurs. The electric field associated with the charge distributions prohibits further net diffusion and an equilibrium situation is reached. Thus it is undesirable to have any large transverse temperature gradients present in the Hall plate while measuring the Hall voltage, or any large longitudinal temperature gradients while measuring resistivity.

**The Peltier Effect**

The Peltier effect, in conjunction with the Seebeck effect may introduce error in the measurement of plate conductivity. Consider a Hall plate with two metal contacts at the ends to promote current flow
through the plate. If the plate is then connected to a voltage source such that current flows through the plate, a longitudinal temperature gradient may be set up due to heat transfer from one metal-semiconductor interface to the other (Peltier effect). The temperature gradient would then be associated with an electric field which would contribute to the voltage measured across the transverse contacts (Seebeck effect). Thus resistivity measurements could be in error on this account (Putley, 1960). It is therefore of interest to calculate the magnitude of the Seebeck contribution to the resistivity-contact voltage for an estimated temperature gradient across the length of the plate. This is done below for both p- and n-type plates.

The thermo-electric powers for p- and n-type silicon can be calculated from the formulas (Wang, 1966, p. 235)

\[ Q_p = \frac{E_f - E_v + 2kT}{eT} \]  \hspace{1cm} (19-a)

\[ Q_n = \frac{E_f - E_c - 2kT}{eT} \]  \hspace{1cm} (19-b)

where \( Q_p \) and \( Q_n \) are the thermo-electric powers of p- and n-type silicon, respectively, \( E_c, E_v \) and \( E_f \) are energy levels of the conduction and valence band edges and the Fermi level, respectively. The energy separations in Equations (19-a) and (19-b) may be calculated from the formulas (Wang, 1966, p. 149)
\[
E_f - E_v = \frac{kT \ln(N_v/N_a)}{eT} \quad (20-a)
\]
\[
E_c - E_f = \frac{kT \ln(N_c/N_d)}{kT} \quad (20-b)
\]

where \( N_c = N_v = 2.5 \times 10^{19} \text{ cm}^{-3} \), \( N_a \) and \( N_d \) are the acceptor and donor densities. For the experiments conducted in this work, \( N_a \) and \( N_d \) were about \( 7 \times 10^{15} \text{ cm}^{-3} \) and \( 5 \times 10^{14} \text{ cm}^{-3} \), respectively. Using these values and a temperature of 300°K, one obtaines

\[
E_f - E_v = (0.0259) \ln\left(\frac{2.5 \times 10^{19}}{7 \times 10^{15}}\right)
\]
\[
E_f - E_v = 0.21 \text{ ev} \quad (21-a)
\]
\[
E_c - E_f = (0.0259) \ln\left(\frac{2.5 \times 10^{19}}{5 \times 10^{14}}\right)
\]
\[
E_c - E_f = 0.28 \text{ ev} \quad (21-b)
\]

Substituting these values in Equations (19-a) and (19-b) yields

\[
Q_p = \frac{(0.21 \text{ ev} + 0.052 \text{ ev})(1.6 \times 10^{-19} \text{ joule/ev})}{(1.6 \times 10^{-19} \text{ coul})(3 \times 10^{2} \text{°K})}
\]
\[
Q_p = 0.87 \text{ mv/°K} \quad (22-a)
\]
\[
Q_n = \frac{-(0.28 \text{ ev} + 0.052 \text{ ev})(1.6 \times 10^{-19} \text{ joule/ev})}{(1.6 \times 10^{-19} \text{ coul})(3 \times 10^{2} \text{°K})}
\]
\[
Q_n = 1.1 \text{ mv/°K} \quad (22-b)
\]

Consider first the result for p-type silicon. Suppose a 20°K
temperature difference is developed between the current contacts of a p-type plate when mounted on the circuit board while conducting a current of five milliamps. The Seebeck voltage between the contacts is given by (Wang, 1966, p. 235)

\[ V_s = Q_p(T_1 - T_2) \]  \hspace{1cm} (23-a)

\[ V_s = (0.87 \text{mv/°K})(20°\text{K}) \]

\[ V_s = 17 \text{ mv.} \]  \hspace{1cm} (23-b)

Since the distance between the resistivity contacts is only about one-ninth of the plate length between the current contacts, a small part of the 17 mv would appear across the resistivity contacts. Making the approximation that the temperature gradient is linear across the length of the plate, roughly one-ninth of the current-contact Seebeck voltage will appear across the transverse contacts. If one makes the approximations that two millivolts appears across the resistivity contacts when the plate is on the circuit board, then resistivity measurements for the plate could be in error by, at most, two millivolts. At five milliamps plate current, the average voltage that appears across the resistivity contacts is about 0.25 volt. Thus the rough estimation of the error is less than one percent of the contact voltage produced by current flow, and is thus not of concern to the author. The estimation would be about 1.5% for a 40°K temperature difference
between the current contacts. It is expected that the estimation of
20°K is much too large. It was desired, however, to calculate a sure
upper limit to the importance of the effect in question.

Although the thermoelectric power of the n-type silicon is
slightly higher than for the p-type silicon, the n-type plates experi-
mented with below have approximately five times the resistivity of
the p-type plates. Thus for a given current level, a given tempera-
ture gradient is between three and four times less important in the
n-type resistivity measurements than in the p-type measurements,
and is thus negligible.
IV. EXPERIMENTS CONDUCTED

Investigation of Aluminum-Evaporated Contacts on Silicon

The experiments described below were undertaken to find out whether aluminum-evaporated contacts have ohmic behavior or not excessively high resistance before or after alloying.

Two one-ohm-cm, p-type silicon wafers cut along (111) planes were scribed and broken into quarters, dipped in buffered hydrofluoric acid (4:1) for ten seconds, rinsed in deionized water, blown dry with nitrogen gas and placed on a hot-plate at 150°C for one minute. The quarter-wafers were then placed in the vacuum evaporator and aluminum was evaporated onto the dull sides of the pieces. The samples were then removed and alloyed for five minutes in a nitrogen atmosphere at 530°C. Next, 600-grit silicon carbide was used to finger-lap the polished sides of the pieces, which were subsequently cleaned by cotton swabbing with trichlorethylene, then placed in a teflon beaker containing trichlorethylene, and the beaker placed in the ultrasonic vibrator for 12 minutes. The samples were then dipped in buffered hydrofluoric acid for ten seconds, and, continuing with the procedure mentioned above, aluminum was evaporated onto the lapped surfaces. By applying the photoresist process, round dots of aluminum of about 0.7 mm diameter were left on the samples. Then, using the Fairchild 6200-B Curve Tracer, the approximate
resistances of several dots (each in series with the bulk semiconductor and the large-area current contact) were obtained by noting the slope of the display curve under forward and reverse bias. The resistance measurements were then repeated after the samples had been alloyed for five minutes in a nitrogen atmosphere at 530°C. Thus alloyed and unalloyed aluminum-silicon contacts could be roughly compared. In order to reduce the effects of fringing of the current lines due to the large rear contact, four dice, each having only one aluminum dot, were scribed and broken out of one of the alloyed samples, and one resistance measurement was made on each of these. These measurements were used in calculations of approximate contact resistance. The measured results were then divided by two to take into account the two contacts in series.

Investigation of Electroless Nickel Contacts

The purposes of these experiments were similar to the experiments described above for aluminum contacts. Quarter wafers were scribed and broken out of one-ohm-cm, n-type and two-ohm-cm, p-type silicon wafers cut along (111) planes. Alloyed aluminum contacts were applied to the unpolsished surfaces of the p-type pieces as described above. Some Brenner basic electroless nickel solution (Sullivan and Eigler, 1957) was poured in a pyrex beaker and the beaker placed on a Corning hot-plate. The samples, after undergoing
lapping, cleaning, and the hydrofluoric acid treatment used above, were placed in the heated plating solution (about 95° C) for about ten minutes. The photoresist process was then applied, leaving nickel dots 0.2 mm in diameter on the samples. The etch was a four-to-one by weight solution of tap water and ferric chloride at room temperature. This etching process was not well-behaved, however, and no future success with the process was obtained. Resistances were measured for various dots on the quarter-wafer samples as described above. A p-type quarter wafer was then alloyed at 530° C for two periods of 15 minutes. An n-type quarter wafer was alloyed at 930° C for 15 minutes. The above alloys were carried out in nitrogen atmospheres. Four dice were then taken from the n-type sample and one resistance measurement was made on each of these.

Plate-Shaping and Cleaning Processes

The methods attempted for shaping plates out of (111)-plane silicon wafers were scribing and breaking and diamond saw cutting. The latter is most easily accomplished by mounting the wafer to be cut on a glass microscope slide with wax. By making the outsides of the current contacts one inch apart and allowing 0.03 inch for the width of each current contact, and requiring that the part of the plate not covered by the current contacts has a length-to-width ratio of four, the width of the plate must be 0.235 inch. This size has the
advantage that three Hall plates can be cut out of one wafer of 1.25 inches in diameter. The size is wide enough to allow the transverse contacts to be a small percentage of the plate width (say 20%) while being large enough to allow easy contact to them with spring wire (described below). This would result in a transverse-contact shorting of the Hall voltage of slightly more than 10% for a plate like Type (e) of Figure 2.

After shaping, the plates were lapped using 600-grit silicon carbide. This was done by heating a metal lapping block on a hot-plate, melting wax onto a flat surface of the block, placing the plate on the melted wax and cooling the block with cold water. After lapping one side, the plate was cleaned by squiriting it with trichlor-ethylene and rubbing it with cotton swabs, and repeating until the swabs appeared clean. The block was then heated, the wax melted and the plate slid off the block, turned over and the process repeated. After removing the plate from the block with both faces lapped and cotton-swabbed, wax remaining on the plate was removed by squirting it with acetone.

Since leaving Hall-plate silicon past the current contacts has no important effect on device performance, three Hall plates can be cut or scribed and broken by making four parallel passes across a wafer. The silicon plates are thus not rectangular, however the electrical contact arrangements are as shown in Figure 2.
Hall Plate Construction and Testing

An explanatory note is appropriate here. After construction and testing of the first three p-type Hall plates, it was found that the plates put out only slightly more than 60% of the Hall voltage predicted by the simple formula given in Chapter I. The formula was expected to be accurate because of its repeated appearance in the literature in connection with silicon and germanium, and accompanying statements that it is a good approximation. Note, however, that the observed voltages would have to be increased by roughly 70% in order for the predictions to be correct. It was therefore felt that some factor or factors peculiar to the plates tested was associated with the large deviations from prediction. Due to a rigid time constraint, it was decided to conduct some preliminary experiments to seek out the most promising sources for the deviations from predicted voltages, then using statistics, conclude whether or not any positive results from the preliminary experiments were significant. It was expected that this procedure would greatly save on time spent taking measurements and constructing Hall plates. This turned out to be the case.

The construction of most of the plates was for the explicit purpose of uncovering the possible source or sources of the large deviations between theory and experiment observed for the p-type plates. In all such experiments, no promising results were obtained. At
this point, the author concluded that the large discrepancy was probably due largely or totally to bulk semiconductor characteristics not taken into account in the derivation of Equation (2) in Chapter I. The author therefore began a search for more detailed Hall voltage calculations which would yield agreement between theory and preliminary experiment, to the author's satisfaction. Such calculations were found and are presented in Chapter III. Since satisfactory agreement was obtained, and considering the results of the experiments conducted, it was concluded that the miscellaneous factors explored experimentally were not important contributors to device performance, and that no further investigation of these factors was warranted. As a result, the experiments described below are of a non-statistical nature.

The p-Type Plates

The first Hall plate built was of about 2.5 ohm-cm, p-type silicon and had the electrode configuration of Plate (d) in Figure 2. Aluminum evaporated and alloyed contacts were made as described above. The plate was mounted, as were all others, on copper-covered printed circuit board measuring about 3 in x 2 in. The latter was prepared by covering the part of the board on which it was desired to leave copper with black electrical tape. The board was then placed in a solution of 4:1 by weight tap water and ferric chloride at room
temperature for roughly five hours. The ferric chloride was not completely dissolved, however, as evidenced by the opaqueness of the solution. The electrical tape was then removed. Pieces of 30-gauge phosphor-bronze wire (springy) of about 0.5 inch length were cut and soldered to the five copper squares left on the circuit board, one wire for each of the five contacts. The areas were made large enough so that electrical lead wires could easily be soldered to the squares without disturbing or interconnecting solder used to secure the phosphor-bronze contact wires. After the phosphor-bronze and lead wires had been soldered to the copper areas, tweezers were used to bend the wires such that pressure contact was made between the unsoldered ends of the wires and the circuit board. The locations of these points of pressure contact were made to roughly correspond to the places where the Hall-plate contacts are when the latter is in place on the circuit board. The Hall plate was then slid onto the circuit board, lifting the phosphor-bronze wires one by one using tweezers, and placing them on the Hall plate. Connection between the wires and the Hall-plate electrodes was finally made by additional bending of the wires where necessary, using tweezers as before. Resistivity, mis-alignment and Hall voltage measurements were taken.

In a similar manner, other p-type plates with the electrode configurations of Plates (e), (h) and (i) were constructed, four like (e),
and one like (h). The transverse contacts on these plates and all others tested extended about 20% of the distance across the width of the plates.

**The n-Type Plates**

The n-type plates constructed had the electrode configurations of Plates (e) and (i), two like (e), one like (i). These were constructed by applying the plate-shaping process described above, using scribing and breaking. After the final cotton-swabbing, the ten-second dip in buffered hydrofluoric acid and deionized-water rinsing, photoresist was applied on one side of the plates and developed such that the photoresist was removed where the nickel contacts were desired. After waxing the plates down on a glass slide, a small amount of aluminum was scratched on small parts of the areas where the contacts were desired. The plates were removed from the slides, and the wax washed off the backs of the plates with acetone. This expedites the plating process. The plates were then placed in Brenner acid plating solution at about 95°C for 15 minutes. After removal from the solution, nickel plated on the back of the plate was lapped off using 600-grit silicon carbide.

It has been noted by Colman and Kendall (1969) that dipping silicon into 48% hydrofluoric acid can induce an n-type inversion layer on high-resistivity, p-type silicon. To remove most of the
possible effects of the buffered hydrofluoric acid treatment, the aluminum evaporation and the phosphoric acid solution used to etch the aluminum on transverse voltage, one p-type plate, after lapping and cleaning, was covered, front and back, with photoresist. The latter was removed where the contacts (in the arrangement of Plate (e) of Figure 2) were desired. After baking the photoresist for ten minutes, aluminum was evaporated and etched, then alloyed as before. Hall-voltage measurements for the plate were then taken, using a magnet of approximately 4800 gauss, a Hewlett-Packard Model 413A DC Voltmeter, a 100 megohm potentiometer and a 35 ma full-scale ammeter connected as shown in Figure 1. The same apparatus was used for all transverse voltage measurements.

Attempts to detect the magneto-resistance effect were also made. This was done for one n- and one p-type plate by leaving the voltage control on the power supply at a constant setting while moving the Hall plate attached to the circuit board in and out of the magnetic field and watching very closely for the slightest deflection of the ammeter reading (30 ma full-scale).

All of the plates used above had unlapped edges which had a somewhat shiny appearance. In order to reduce the mobilities of possible inversion-layer carriers, the edges of a p-type plate were lapped until the long edges appeared dull. The observed transverse voltage for the plate was measured and compared with the same plate's
performance before the lapping. A p-type plate was also constructed without lapping any faces or edges (polished surfaces). The plate's transverse voltage was then measured for several current levels.
V. EXPERIMENTAL RESULTS

Aluminum Evaporated Contacts

The resistances of the samples prior to alloying varied between 10.3 ohms and 17.8 ohms under forward bias, with about 65% of all resistances being between 11 and 13 ohms. In reverse bias, the resistances varied from 230 ohms to 2500 ohms. After five minutes of alloying, practically all the resistances measured yielded values of between 12 and 13 ohms, each dot yielding apparently identical resistance values in both the forward- and reverse-biased conditions. The resistance readings from the four small squares, along with the approximate areas of each, and the calculated contact resistances are shown in Table 1. The approximate areas of the squares were found by measurements using a scale one millimeter in length that is divided into one-hundred parts. The contact resistances were calculated by multiplying the sample resistances by the respective sample areas.

Table 1. Approximate contact resistance of aluminum evaporated and alloyed contacts on one-ohm-cm, p-type, (111)-plane silicon. Each R and A is the result of one experimental determination.

<table>
<thead>
<tr>
<th>Sample</th>
<th>R (ohms)</th>
<th>A (mm$^2$)</th>
<th>C (ohm-mm$^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4.0</td>
<td>0.3</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>5.5</td>
<td>0.3</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>7.5</td>
<td>0.3</td>
<td>2</td>
</tr>
<tr>
<td>4</td>
<td>7.0</td>
<td>0.3</td>
<td>2</td>
</tr>
</tbody>
</table>
Electroless Nickel Contacts

Two-Ohm-Cm, p-Type Silicon

The electroless nickel contacts to the two-ohm-cm, p-type wafer allowed no current to flow under reverse bias. After one alloy, for most of the dots about 2 ma current flowed for one volt reverse bias. After the second alloy, the characteristics were similar. The contacts were nonlinear and of high resistance under reverse bias.

One-Ohm-Cm, n-Type Silicon

Four small squares were also obtained from nickel-dotted wafers as described above for aluminum-dotted samples. The method of calculation of contact resistance was the same for the electroless nickel contacts (Table 2) as above for the aluminum evaporated contacts. The V-I characteristics were linear under forward and reverse bias.

Table 2. Approximate contact resistance of electroless nickel on one-ohm-cm, n-type, (111)-plane silicon. Each value is the result of one experimental determination.

<table>
<thead>
<tr>
<th>Sample</th>
<th>R (ohms)</th>
<th>A (mm²)</th>
<th>C (ohm-mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>30</td>
<td>0.2</td>
<td>6</td>
</tr>
<tr>
<td>2</td>
<td>30</td>
<td>0.1</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>20</td>
<td>0.2</td>
<td>4</td>
</tr>
<tr>
<td>4</td>
<td>20</td>
<td>0.2</td>
<td>4</td>
</tr>
</tbody>
</table>
Plate-Shaping Processes

It was found that diamond-saw cutting of Hall plates from (111) planes resulted in plates that were unlikely to break during the remainder of the plate processing. This cutting procedure, when applied to (100)-plane wafers resulted in, after finger lapping, extremely fragile plates. It was found, however, that the (100)-plane wafers could be scribed and broken easily, and resulted in plates that always withstood the remainder of the plate processing. The above (100) plates were block-lapped instead of finger-lapped. One lapped plate was dropped from a height of about four feet onto a hard floor and did not break.

Hall-Plate Resistivity and Hall-Voltage Measurements

The first Hall plate made, which had the electrode configuration of Plate (d) of Figure 2, had an appreciable mis-alignment voltage. Four-point-probe measurements indicated a plate resistivity of 2.5 ohm-cm; however plate probe measurements indicated a resistivity of 2.2 ohm-cm, the difference possibly being due to the roughness and microcracks on the surface of the plate. The Hall voltage was measured at about 60 mv at 50 ma current. Excessive heating was noted at this current level.

Four p-type plates with the electrode configuration of Plate (e),
and one like Plate (h) were constructed and tested. The various plate performances were highly reproducible, the plate electrode configurations having little or no noticeable effect on transverse voltage. Hall voltage data for two p-type plates using the electrode configuration of Plate (e) in Figure 2 are shown in Table 3 and in Figure 8.

It is believed that heating is the only important contributor to non-linearity of the plate V-I characteristics. Since heating was minimal for Plates II, III and IV, and since their V-I characteristics appeared close to linear as judged by the author, it was decided to use the least-squares method to obtain the experimental estimates of volts/amp-kG for these plates. These numbers were then compared with calculations using the theory presented in Chapter III. For Plate I, the current levels were not adjusted to zero between readings, as done for Plate II. The volts/amp-kG determination for this plate was found by making an eye judgement of the least squares line for current levels of 5, 10 and 15 ma. These values were chosen since the V-I curve is approximately linear for these points, and since heating is not large, nor is the error on the current reading.

The predicted values for all plates, p- and n-type were calculated from the formula

\[ V = \frac{(b-2a)}{b} \left( \frac{rIB}{\text{net}} \right) \quad (17) \]
Table 3. Comparison of observed and predicted transverse voltages for two two-ohm-cm, p-type silicon Hall plates of Plate (e) electrode configuration at $B = 4.8$ kG. Tolerances (in millivolts) on observed values are 2% of full-scale deflection. Tolerances on all predicted and calculated values in this thesis were obtained in a manner suggested by Baird (1962, p. 49-59). All tolerances are subjectively estimated by the author as 80% to 90% confidence limits on the quantities for which measurement or calculation is attempted; they are not standard deviations unless specifically identified as such.

<table>
<thead>
<tr>
<th>Plate</th>
<th>I (ma)</th>
<th>Transverse Voltage (mv)</th>
<th>Agree Within Error</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Observed</td>
<td>Predicted</td>
</tr>
<tr>
<td>I</td>
<td>2.0 ± 0.7</td>
<td>3.2 ± 0.2</td>
<td>4 ± 1</td>
</tr>
<tr>
<td></td>
<td>5.0 ± 0.7</td>
<td>8.5 ± 0.2</td>
<td>9 ± 2</td>
</tr>
<tr>
<td></td>
<td>10.0 ± 0.7</td>
<td>17.4 ± 0.6</td>
<td>19 ± 3</td>
</tr>
<tr>
<td></td>
<td>15.0 ± 0.7</td>
<td>24.3 ± 0.6</td>
<td>28 ± 4</td>
</tr>
<tr>
<td></td>
<td>20.0 ± 0.7</td>
<td>28.0 ± 0.6</td>
<td>37 ± 6</td>
</tr>
<tr>
<td></td>
<td>25.0 ± 0.7</td>
<td>34 ± 2</td>
<td>47 ± 7</td>
</tr>
<tr>
<td>II</td>
<td>5.0 ± 0.7</td>
<td>10.0 ± 0.2</td>
<td>11 ± 2</td>
</tr>
<tr>
<td></td>
<td>10.0 ± 0.7</td>
<td>20.0 ± 0.6</td>
<td>23 ± 4</td>
</tr>
<tr>
<td></td>
<td>15.0 ± 0.7</td>
<td>29.0 ± 0.6</td>
<td>34 ± 5</td>
</tr>
<tr>
<td></td>
<td>20.0 ± 0.7</td>
<td>39 ± 2</td>
<td>45 ± 7</td>
</tr>
<tr>
<td></td>
<td>25.0 ± 0.7</td>
<td>50 ± 2</td>
<td>57 ± 9</td>
</tr>
</tbody>
</table>

Plate Characteristics

<table>
<thead>
<tr>
<th>$\rho$ (ohm-cm)</th>
<th>$t$ (mils)</th>
<th>Observed Output (volts/amp-kG)</th>
<th>Predicted Output (volts/amp-kG)</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>2.1 ± 0.2</td>
<td>7.3 ± 0.1</td>
<td>$0.33^a$ ± 0.02 0.39 ± 0.07</td>
</tr>
<tr>
<td>II</td>
<td>2.2 ± 0.2</td>
<td>6.2 ± 0.1</td>
<td>$0.41^b$ ± 0.01 0.48 ± 0.09</td>
</tr>
</tbody>
</table>

$a$ Calculated from observed voltages at 5, 10 and 15 ma (see text).

$b$ Least-squares determination; tolerance is a standard deviation calculated from five V-I readings.
Figure 8. Comparison of observed and predicted transverse voltages of two p-type silicon Hall plates (data from Table 3).
where the factor \((b-2a)/b\) (defined in Chapter II) is due to transverse contact shorting. For all plates, this factor is taken as \(0.90 \pm 0.05\). For Plate I,

\[
\frac{0.90 \rho B}{n_1 e t_1} = \frac{(0.90)(0.93)(4.75 \times 10^{-5})}{(7.14 \times 10^{15})(1.6 \times 10^{-19})(1.85 \times 10^{-2})} \quad (18-a)
\]

\[
\frac{0.9 \rho B}{n_1 e t_1} = \frac{3.97 \times 10^{-5}}{2.1 \times 10^{-5}} = 1.87 \text{ mv/ma} \quad (18-b)
\]

Since all transverse voltage measurements were taken using a magnet of 4.8 kG \(\pm 0.1\), the predicted transverse voltage for Plate I from Equation (18-b) may be expressed as \(0.39\) volts/amp-kG \(\pm 0.07\).

The value of the impurity concentration \(n\) was obtained from a graph of resistivity vs. impurity concentration (Fordemwalt and Warner, 1965, p. 29). Carrying out the above procedure for Plate II yields a value of \(0.48\) volts/amp-kG \(\pm 0.09\), taking the Hall coefficient factor as exactly 0.93. The far sides of the current contacts were spaced one inch apart. The plate widths were 0.235 inch \(\pm 0.005\), and resistivity contacts were 0.10 inch apart, center to center, as on all plates. The special p-type plate that was protected with photoresist performed the same as the other plates with regard to transverse voltage.

Two n-type Hall plates with the electrode configuration of
Plate (e) (Plates III and IV) and one of Plate (i) were constructed and tested. Data for Plates III and IV are shown in Table 4 and Figure 9. The n-type plate resistivities were all between nine and ten ohm-cm. The long plate had a length-to-width ratio of about 5.2 and a resistivity of about 9.5 ohm-cm. Its performance was similar to those of Plates III and IV.

Table 4. Comparison of observed and predicted transverse voltages for two ten-ohm-cm, n-type, silicon Hall plates of Plate (e) electrode configuration at B = 4.8 kG. Tolerances (in millivolts) on observed values are 2% of full-scale deflection. See heading, Table 3.

<table>
<thead>
<tr>
<th>Plate</th>
<th>I (ma)</th>
<th>Transverse Voltage (mv)</th>
<th>Agree Within Error</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Observed</td>
<td>Predicted</td>
</tr>
<tr>
<td>III</td>
<td>2.0 ± 0.7</td>
<td>67 ± 2</td>
<td>65 ± 10</td>
</tr>
<tr>
<td></td>
<td>4.0 ± 0.7</td>
<td>142 ± 6</td>
<td>130 ± 20</td>
</tr>
<tr>
<td></td>
<td>5.0 ± 0.7</td>
<td>178 ± 6</td>
<td>160 ± 20</td>
</tr>
<tr>
<td></td>
<td>7.0 ± 0.7</td>
<td>249 ± 6</td>
<td>230 ± 30</td>
</tr>
<tr>
<td>IV</td>
<td>2.0 ± 0.7</td>
<td>68 ± 2</td>
<td>72 ± 11</td>
</tr>
<tr>
<td></td>
<td>4.0 ± 0.7</td>
<td>147 ± 6</td>
<td>140 ± 20</td>
</tr>
<tr>
<td></td>
<td>6.0 ± 0.7</td>
<td>227 ± 6</td>
<td>220 ± 30</td>
</tr>
<tr>
<td></td>
<td>10.0 ± 0.7</td>
<td>380 ± 20</td>
<td>360 ± 50</td>
</tr>
</tbody>
</table>

| Plate Characteristics |
|-------------------------|-----------------|-----------------|
| p (ohm-cm) | t (mils) | Observed Output (volts/amp-kG) | Predicted Output (volts/amp-kG) |
| III | 9.0 ± 0.9 | 6.5 ± 0.1 | 7.4* ± 0.1 | 6.8 ± 0.9 |
| IV | 10.2 ± 0.9 | 6.6 ± 0.1 | 8.0* ± 0.1 | 7.5 ± 0.9 |

*Least squares determinations; tolerances are standard deviations calculated from four V-I readings each.
Figure 9. Comparison of observed and predicted transverse voltages of two n-type silicon Hall plates (data from Table 3).
Magneto-Resistance

No magneto-resistance effect was observed, within the limit of accuracy of the current meter (35 ma full-scale). No movement of the current meter needle was observed.

Lapped-Edge and Polished Plates

These plates' performances were very similar to that of the other p-type plates.
VI. DISCUSSION OF RESULTS

Contact Resistance

The contact resistance determinations were meant to be only rough approximations, the purpose of which was to illustrate any high resistances that might be present in the Hall-plate circuits. Since the results indicated very small resistances would result for one- and two-ohm-cm silicon, it was decided to proceed with Hall-plate construction without further investigation of contact resistances on silicon of other resistivities.

Plate-Shaping Process

The scribing and breaking of (100)-plane wafers was chosen above diamond saw cutting of (111)-plane wafers because the former was much easier and faster. Using this procedure with block lapping resulted in greatly reduced fragility of the plates from the case of diamond saw cutting and finger lapping, as the vibrational stress incurred by the plates during sawing is eliminated.

Plate Performances

The p-Type Plates

Since the Hall plate with the electrode configuration of Plate (d)
in Figure 2 had an appreciable mis-alignment voltage, this contact arrangement was rejected.

As can be seen from Table 3, the observed and predicted values for volts/amp-kG for Plates I and II overlap, however the experimental values fall considerably below the predicted values for both plates. The predicted values were calculated using a Hall-coefficient factor of 0.93. The observed Hall-coefficient factors for both Plates I and II are about 0.79. Thus the experimental values are roughly 85% of the predicted values. Simple theory assuming spherical constant-energy surfaces and acoustical phonon scattering predicts a Hall-coefficient factor of 1.18 while the experimental results of Morin and Maita (1954, p. 34, 35) indicate one of 0.72 for boron-doped silicon at room temperature. They account for their results by warped constant-energy surfaces and low-quality crystals.

The n-Type Plates

These plates displayed the opposite tendency in performance relative to prediction as they performed at consistently higher transverse voltage. The Hall-coefficient factor calculated in Chapter III is 1.02, while those observed for Plates III and IV are about 1.11 and 1.09, respectively, or about 108% of the predicted value.
Thermal Effects on Transverse Voltage

As mentioned above, it is strongly expected that the rather pronounced deviation of the observed transverse voltage from the predicted voltage for Plate I (Figure 8) is associated with heating. The voltameter needle (indicating the plate transverse voltage) would begin a slow descent after reaching a peak, the amount of descent being positively correlated with the current level. If the current level was rapidly returned to zero, then up to a high level (say 20 ma) the reading would remain low. If a minute or so elapsed after the current was shut off, then the current level adjusted to its former value, the slow descent was also observed. Heating was noticeable by putting the hand near the plate after about 20 ma was run through the plate for a minute or so.

One or more of four factors might account for the decrease in transverse voltage for a given current level with increasing temperature.

1. The velocity dependence of the collision relaxation time depends partly on the percentage of lattice scattering accountable to optical phonons. Since this velocity dependence also effects the value of the Hall-coefficient factor, and since optical phonon density increases with temperature, the Hall-coefficient factor would decrease with increasing
temperature on this account.

2. Increasing warping of the constant energy surfaces of the heavy- and light-hole bands with increasing temperature would also result in a negative temperature dependence of the Hall-coefficient factor (see Chapter III).

3. Changes in the effective masses of carriers in the three bands with temperature increases might help produce the observed dependence.

4. An increase in hole concentration with increasing temperature would increase the denominator in Equation (17), thereby reducing V/I.

**Plates with Lapped and Polished Surfaces**

Plates with lapped surfaces have in addition to the roughness, microcracks in the surfaces. These characteristics have the effect of impeding surface carriers. Thus if inversion-layer carriers were present in a large number, their effect on the Hall voltage should be much different in the cases of polished and lapped surfaces of Hall plates. The Lorentz fields for inversion-layer electrons are much different for much different carrier mobilities under a given current-contact voltage. Therefore inversion-layer carriers do not exist in sufficient quantity to effect Hall voltage output of the p-type plates.
VII. CONCLUSIONS

The p-Type Plates

The p-type plate behavior is difficult to predict. All factors deemed important and many minor factors in the literature have been considered in the Hall-coefficient factor calculation for the p-type plates in Chapter III. All methods of calculation found by the author that seem to accurately represent the silicon yield values for the Hall-coefficient factor in the vicinity of unity. Based on previous experimental results of Morin and Maita (1954, p. 34) and on the experiments and theoretical calculations contained in this thesis, the author has concluded that the difference between the theoretical Hall-coefficient factor calculated in Chapter III (0.93) and those observed for Plates I and II (0.79) is not due to any peculiarities of the Hall-plate design. Other experiments (Morin and Maita, 1954, p. 31) have also illustrated the negative temperature dependence of the Hall-coefficient at room temperature, mentioned above as a reason for the shape of the observed V-I curve for Plate I.

These plates may be constructed by simply scribing and breaking them from (100)-plane silicon wafers (lapping and cleaning optional) evaporating an aluminum film on one side, applying the photoresist process to leave the contacts in the arrangement of Plate (e), then performing a five-minute alloy in a nitrogen atmosphere
The n-Type Plates

Agreement between theory and experiment here meets the author's satisfaction. A 10% tolerance has been placed on the carrier concentration readings from the graph of resistivity vs. carrier concentration used earlier for the Hall voltage calculations. Thus agreement within 8% is pleasing.

These plates may be made by scribing and breaking, lapping one side and cleaning, photoresisting and electroless nickel plating, lapping nickel off the back of the plate and alloying for five minutes at 530°C in a nitrogen atmosphere. It is necessary to have one side of the plate lapped before photoresist is applied since an aluminum scratch is necessary on each contact area to initiate the plating process. The aluminum will not scratch on a polished silicon surface. The lapping also aids the adhesion of the nickel to the silicon surface.

Objectives Revisited

It is felt by the author that all of the requirements for the devices set forth at the outset of this work have been fulfilled to satisfactory degrees. Previous devices built in our laboratories have had maximum Hall voltages of around one millivolt. The n- and p-type products of this investigation put out about 400 and 20
millivolts, respectively. When on the circuit boards, Hall plates may be dropped without breaking. All the processes for making the completed devices are simple and reliable. Performance characteristics have been reproducible. Silicon is the lowest-cost semiconductor Hall-plate material available. No claim is made that this is the most optimal design, however its advantages are apparent from the work above. It is felt by the author that the objectives have thus been accomplished.
BIBLIOGRAPHY


