

AN ABSTRACT OF THE THESIS OF

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(Name) (Degree)

in Electrical and Electronics Engineering  
(Major)

presented on 12 - 16 - 70  
(Date)

Title: VACUUM-DEPOSITED ALUMINUM-OXIDE MOS TRANSISTORS

Abstract approved: *Redacted for Privacy*

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The properties of evaporated aluminum-oxide films were investigated. The characteristics of MOS devices made with single-layer aluminum-oxide films and double-layer films which were made by evaporating aluminum oxide over thermally-grown silicon dioxide as gate insulation have been investigated. Vacuum-evaporated aluminum oxide has features which are suitable for fabricating MOS devices. Both MOS capacitors and transistors were fabricated on one ohm-cm n-type (111) silicon wafers. Automatic display and plotting equipment were used to measure the capacitance-voltage (C-V) characteristics. Bias-temperature tests were performed on the MOS capacitors. The characteristics of the MOS transistors were measured and the drain current-voltage (I-V) characteristics, threshold voltages, transconductances, effective hole mobilities, and drain diode breakdown voltages of the

MOS transistors were obtained. Both MOS capacitors and transistors with double-layer films as gate insulation revealed the best characteristics. The MOS devices with single-layer aluminum oxide as a gate dielectric exhibited unstable characteristics.

VACUUM-DEPOSITED ALUMINUM-OXIDE MOS TRANSISTORS

by

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A THESIS

submitted to

Oregon State University

in partial fulfillment of  
the requirements for the  
degree of

Master of Science

June 1971

APPROVED:

*Redacted for Privacy*

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Date thesis is presented 12-16-70

Typed by Erma McClanathan for Yun-Sheng Hwang

## ACKNOWLEDGMENTS

The author would like to express his deep appreciation to Professor James C. Looney for his guidance and assistance during the course of this study.

Special acknowledgment is made to my parents for their encouragement and help in making this study here in the United States possible.

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# VACUUM-DEPOSITED ALUMINUM-OXIDE MOS TRANSISTORS

## I. INTRODUCTION

In the past few years, the metal-oxide-semiconductor (MOS) devices have been developed extensively. The gate insulator of the MOS device is an active, integral part of the device, and device operation and characteristics are very sensitive to its properties. Until the advent of the MOS device, the effects of passivating insulator films used on the surface of silicon bipolar transistors and other devices were only minimally understood. Various dielectric materials have been used in the fabrication of the MOS devices. The most commonly used dielectric is thermally-grown silicon dioxide ( $\text{SiO}_2$ ). The silicon-silicon dioxide system has become a very well characterized interface. Insulators other than silicon dioxide have been examined and have been considered a replacement for it. Recently, the use of aluminum oxide ( $\text{Al}_2\text{O}_3$ ) for passivation of devices and for fabrication of MOS transistors (17) and thin film transistors has attracted interest. Aluminum oxide has some features which are more desirable than silicon dioxide such as: higher dielectric constant, greater density (7), and better radiation resistance (17). Table I is the comparison of the properties of aluminum oxide and silicon dioxide (7,16,8).

This thesis project is to investigate the properties

of aluminum-oxide films which were deposited on silicon substrates by electron bombardment evaporation of sapphire source material, and to investigate the characteristics of MOS devices (capacitors and transistors) with aluminum-oxide films and aluminum oxide-silicon dioxide sandwich films as the gate insulation, and to compare the results with the MOS devices fabricated with the thermally-grown silicon dioxide gate.

Table I. Comparison of  $\text{Al}_2\text{O}_3$  and  $\text{SiO}_2$ .

	Breakdown Strength, V/cm	Density $\text{g/cm}^3$	Volume per g atom O, $\text{cm}^3$	Dielectric Constant
$\text{SiO}_2$	$\sim 6 \times 10^6$	2.20	13.7	3.8
$\text{Al}_2\text{O}_3$	$2-7 \times 10^6$	3.5-4.0	8.5-9.7	$\sim 7.5$

### MOS Theory

An MOS structure consists of a semiconductor substrate covered by an insulator layer upon which a metal electrode (gate) is deposited. A brief discussion of the theory and operation of the MOS devices will follow, from which the effects of the insulator properties on the characteristics of the MOS devices can be shown.

### The MOS Capacitor

A schematic representation of the MOS capacitor is

shown in Figure 1. In the absence of work-function differences between metal and semiconductor, charges in the insulator, and surface states (the ideal MOS structure), the

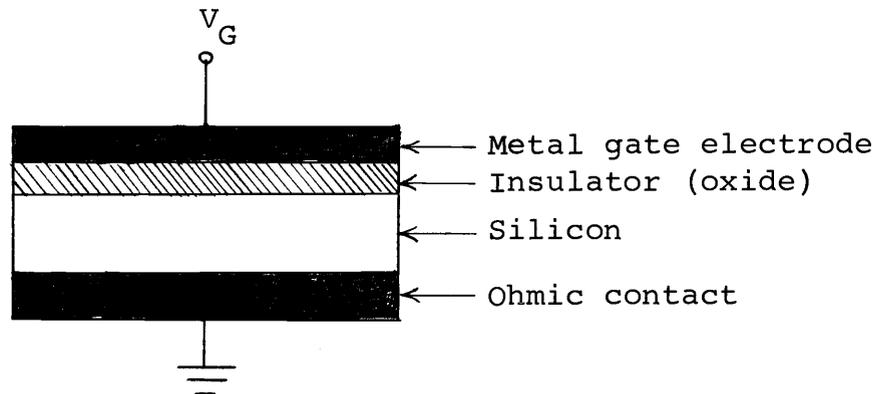


Figure 1. Schematic representation of an MOS capacitor.

capacitance of the device is given by the series combination of the capacitance per unit area of the oxide layer,  $C_o$ , and the capacitance per unit area of the surface space-charge region in the semiconductor,  $C_s$ .

$$C = \frac{C_o C_s}{C_o + C_s}$$

The capacitance of the oxide layer per unit area is:

$$C_o = \frac{K_o \epsilon_o}{x_o}$$

where  $K_o$  = dielectric constant of the oxide

$\epsilon_o$  = permittivity of free space ( $8.86 \times 10^{-14}$  f/cm)

$x_o$  = oxide (insulator) thickness.

And the capacitance of the surface space-charge region in

the semiconductor per unit area is:

$$C_s = \frac{K_s \epsilon_0}{x_d}$$

where  $K_s$  = dielectric constant of semiconductor

$x_d$  = width of surface space-charge region.

While the surface is being depleted the formula for the capacitance of the MOS structure (n-type substrate) is (8, p. 272):

$$\frac{C}{C_0} = \frac{1}{\sqrt{1 - \frac{2K_s^2 \epsilon_0 V_G}{q N_D K_s x_0^2}}}$$

where  $V_G$  = gate voltage

$q$  = magnitude of electronic charge,  $1.6 \times 10^{-19}$  coulomb

$N_D$  = concentration of donor impurities.

When the gate voltage is zero or positive, no depletion region exists. The above formula loses its meaning. The capacitance can be readily obtained by considering that when the surface is accumulated. Thus it will be simply  $C_0$ . And when strong inversion sets in, the width of the depletion region will not increase with further increase in gate voltage magnitude. This will take place as the gate voltage is equal to turn-on voltage,  $V_T$  (8, p. 273).

$$V_T = -\frac{Q_B}{C_0} + \phi_s(\text{inv.}) = -\frac{Q_B}{C_0} + 2\phi_F$$

where  $Q_B$  = charge per unit area contained within the

surface depletion region at and after the onset of strong inversion

$\phi_s$  = surface potential

$\phi_F$  = Fermi potential.

Thus the capacitance will level off and remain constant at a value given by the above equation for  $V_G = V_T$ . A typical capacitance-voltage (C-V) curve for the ideal MOS capacitor is shown in Figure 2. The illustration is for

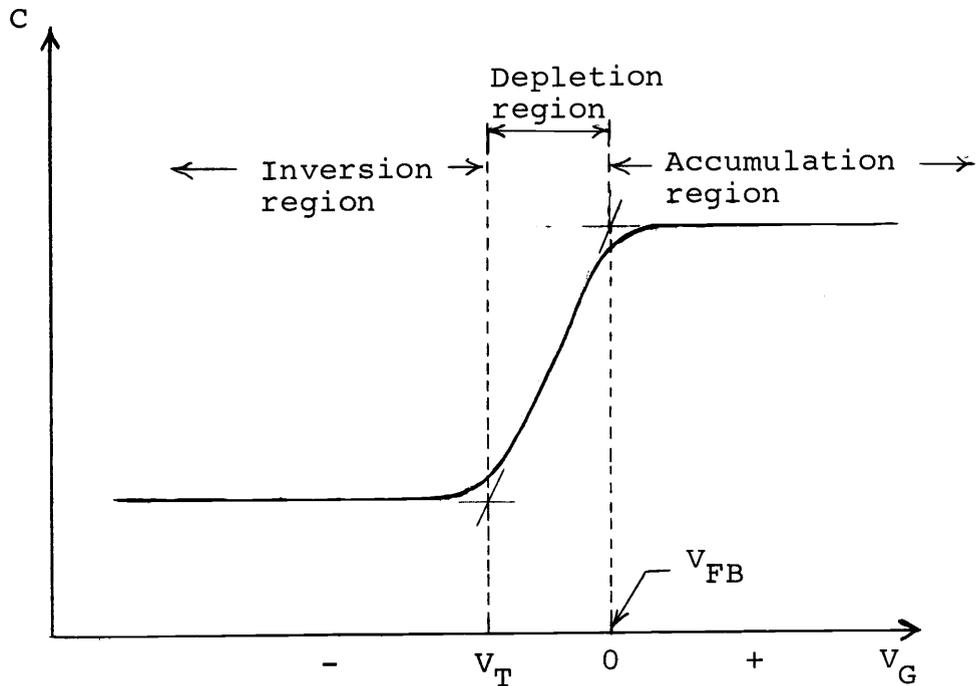


Figure 2. Typical capacitance-voltage characteristics of an ideal MOS capacitor. N-type substrate.

n-type silicon substrate. In laboratory fabricated MOS capacitors, the insulators are not ideal and the surface of the silicon is not perfect. Thus, space charge or

interface charge in the insulator, silicon surface states, and the metal-semiconductor work-function difference will lead to a translation of the flat-band point (8, p. 278) from  $V_G = 0$  along the voltage axis. The total translation of the flat-band voltage,  $V_{FB}$ , or of any other well defined point on the capacitance-voltage characteristics will then be given by (8, p. 281):

$$V_{FB} = \Phi_{MS} - \frac{Q_{SS}}{C_O} - \frac{1}{C_O} \int_0^{x_O} \frac{x}{x_O} \rho(x) dx$$

where  $\Phi_{MS}$  = metal-semiconductor work-function difference

$Q_{SS}$  = surface-state charge density per unit area

$\rho$  = space-charge density

$C_O$  = oxide capacitance per unit area

$x_O$  = oxide thickness.

The flat-band voltage for the double-oxide structure is given by (1):

$$V_{FB} = V_O - \frac{1}{K_1 \epsilon_O} \int_0^{x_1} x \rho_1(x) dx - \frac{1}{K_2 \epsilon_O} \int_{x_1}^{x_1+x_2} \left( \frac{K_2}{K_1} x_1 + (x-x_1) \right) \rho_2(x) dx$$

where  $V_O$  = includes all terms except the oxide charge

$K_1$  = dielectric constant of the outer oxide

$K_2$  = dielectric constant of the inner oxide

$x_1$  = the outer oxide thickness

$x_2$  = the inner oxide thickness

$x$  = the coordinate measured from the metal-oxide interface.

The comparison of the ideal theoretical and practical MOS capacitance-voltage characteristics is shown in Figure 3.

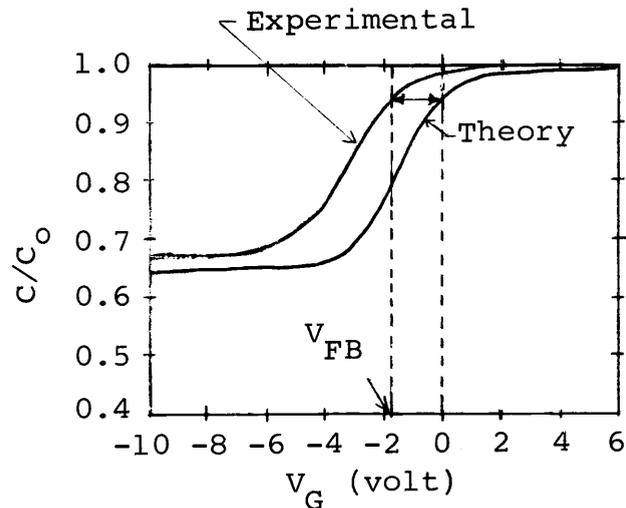


Figure 3. Comparison of ideal theoretical and practical MOS capacitor characteristics (9).

### The MOS Transistor

A schematic representation of the MOS transistor is shown in Figure 4. In this illustration, an n-type silicon substrate is used. Two heavily doped p-type regions, the source and the drain, are diffused into this n-type silicon substrate. A thin insulating material, usually the oxide, is placed over the surface of the silicon between the source and the drain, forming the gate dielectric material. The channel, the region at the substrate surface between the source and the drain, is under the

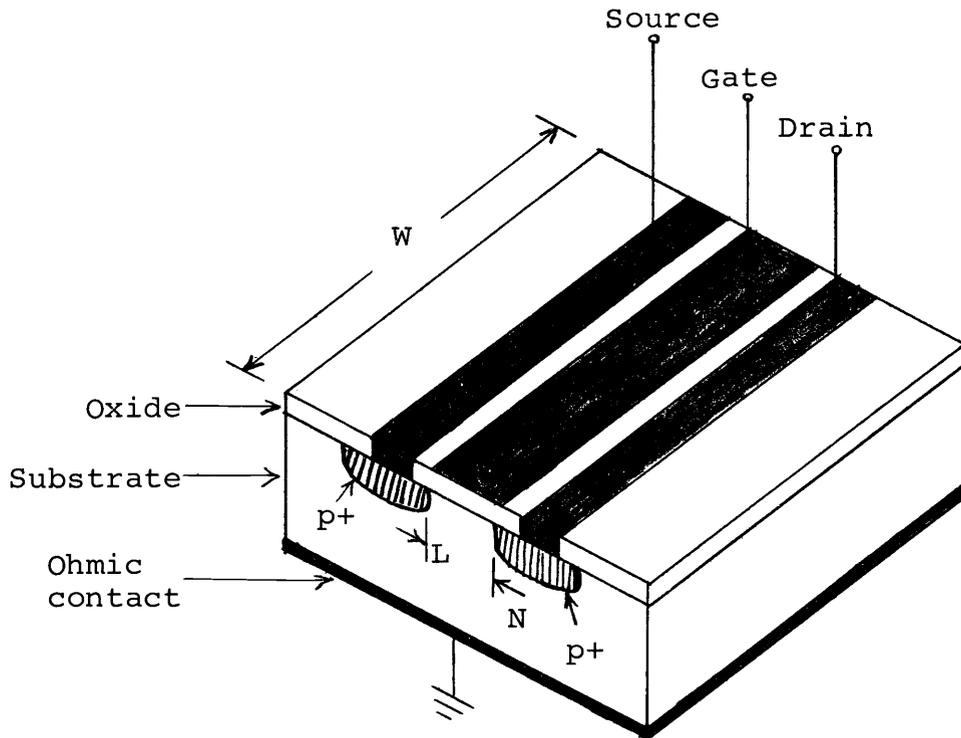


Figure 4. Schematic representation of an MOS transistor.

influence of a metal field plate or gate which is deposited on the insulator. The conductance of the channel is varied by means of a voltage applied between the gate and channel. For a p-type channel, the application of a negative voltage to the gate results in an increase in the number of holes in the channel and a corresponding increase in the channel conductance. A positive gate voltage repels holes from the channel giving a decrease in the channel conductance. These two modes of operation are known as the enhancement mode and the depletion mode. In this project, only enhancement mode transistors will be considered.

Typical current-voltage (I-V) characteristics of the MOS transistor are shown in Figure 5. The illustration is for a p-channel enhancement-type transistor. For a given

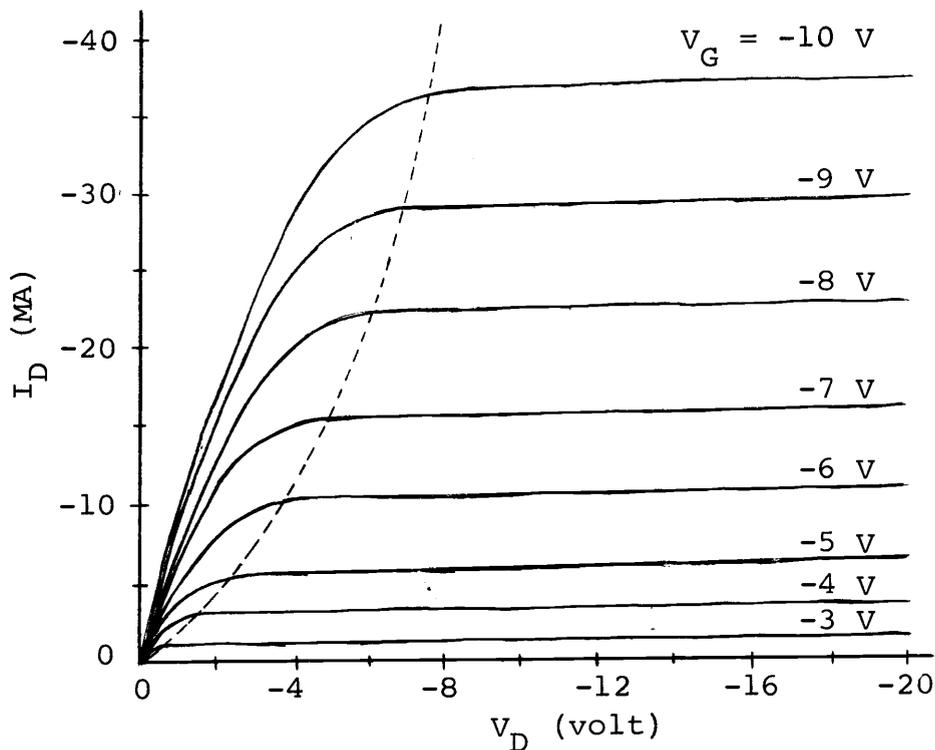


Figure 5. Typical current-voltage characteristics of the MOS transistor. P-channel enhancement type transistor.

gate voltage such that  $|V_G| > |V_{th}|$ , as the drain voltage is increased in magnitude from zero volts, the drain current increases linearly at first, then slows down, and finally tends to level out as  $V_D$  is made large. Thus we can distinguish two regions, linear region and saturation region, of operation of the MOS field-effect transistor. The turn-on or the threshold voltage,  $V_{th}$ , is the minimum

gate voltage necessary to initiate conduction. It is given by (8, p. 324):

$$V_{th} = V_{FB} + 2\phi_{Fn} - \frac{Q_{B,o}}{C_o}$$

where  $V_{FB}$  = the flat-band voltage

$\phi_{Fn}$  = Fermi potential, n-region

$Q_{B,o}$  = charge per unit area within the surface depletion region at the onset of strong inversion, in equilibrium

$C_o$  = capacitance per unit area of oxide layer.

The current-voltage relationships for the drain current are given by (11):

$$I_D = -\frac{W}{L}\mu_p C_o \left\{ (V_G - V_{th}) V_D - 1/2 V_D^2 \right\}$$

for linear (triode) region, defined by  $|V_D| \leq |V_G - V_{th}|$

and 
$$I_D = -\frac{W}{2L}\mu_p C_o (V_G - V_{th})^2$$

for saturation region, defined by  $|V_D| \geq |V_G - V_{th}| = |V_{Dsat}|$ .

The transconductance  $g_m$  of the transistor is defined by (8, p. 326):

$$g_m = \left. \frac{\partial I_D}{\partial V_G} \right|_{V_D = \text{constant.}}$$

Thus the transconductance is given by (11):

$$g_m = -\frac{W}{L}\mu_p C_o V_D$$

for  $|V_D| \leq |V_{Dsat}|$

and 
$$g_m = - \frac{W}{L} \mu_p C_o (V_G - V_{th})$$

for  $|V_D| \geq |V_{Dsat}|$ .

The cut-off frequency  $f_c$  of the transistor is defined by (4, p. 72):

$$f_c = \frac{g_m}{2\pi C_G}$$

where  $g_m/C_G$ , the figure of merit of the transistor, is (10, p. 345):

$$\frac{g_m}{C_G} = - \frac{\mu_p}{L^2} (V_G - V_{th}).$$

Thus 
$$f_c = - \frac{\mu_p}{2\pi L^2} (V_G - V_{th}).$$

## II. EQUIPMENT AND PROCEDURE FOR DEPOSITION

### Sapphire Preparation

The aluminum oxide source material used in this project was high-purity (99.98%) white synthetic sapphire. The half-inch diameter sapphire rod was cut into quarter-inch sections by using a diamond saw. These sections were ultrasonically washed in trichlorethylene and acetone. The sections were etched in a 4:1 solution of buffered HF (eight parts by weight of  $\text{NH}_4\text{F}$  to 15 parts by weight of deionized water was the buffering  $\text{NH}_4\text{F}$  solution; HF added to this solution in the volume of 4:1  $\text{NH}_4\text{F}:\text{HF}$ ) for a few minutes. The sections were then boiled in deionized water, rinsed in deionized water, and dried with dry nitrogen. The sections were then baked in nitrogen at  $530^\circ\text{C}$  in the furnace prior to evaporation.

### Varian Vacuum System

The equipment used for the vacuum deposition of aluminum-oxide films in this project was a Varian vacuum system. The main components of the system are bell jar, base plate, mechanical roughing pump, VacIon pump, titanium sublimation pump, valves, substrate heater, deposit thickness monitor, Varian e-Gun evaporation source, gauges, associated control units, and the mechanical hardware installed within the chamber. The relative positions

of the various components of the system are illustrated in Figure 6.

The vacuum chamber consisted of a standard 18-inch diameter by 30-inch high Pyrex bell jar and a stainless steel staging platform.

The roughing system is used to reduce pressure in the vacuum system from atmosphere to below ten millitorr (one millitorr = one micron  $H_g$ ). A 17.7 CFM Edwards mechanical pump is used. A molecular sieve trap, located between the pump and the chamber, minimizes back-streaming of oil and aids in pumping water vapor.

The VacIon pump provides completely clean, vibration-free pumping. It removes gases by gettering chemically active gases, ion burial of heavy noble gases, cracking and gettering of complex molecules, and by diffusion of hydrogen and helium into the titanium cathode plates. It can be completely isolated before the system is opened to air.

The titanium sublimation pump removes gas by "gettering." Titanium is sublimed from heated filaments and deposited on the lower walls of the baseplate. Active gases are permanently pumped when they combine chemically with this film to form stable compounds. This pump is used throughout the pressure range from 15 millitorr to  $10^{-11}$  torr (one torr = one mm  $H_g$ ).

The Varian e-Gun source is a completely clean

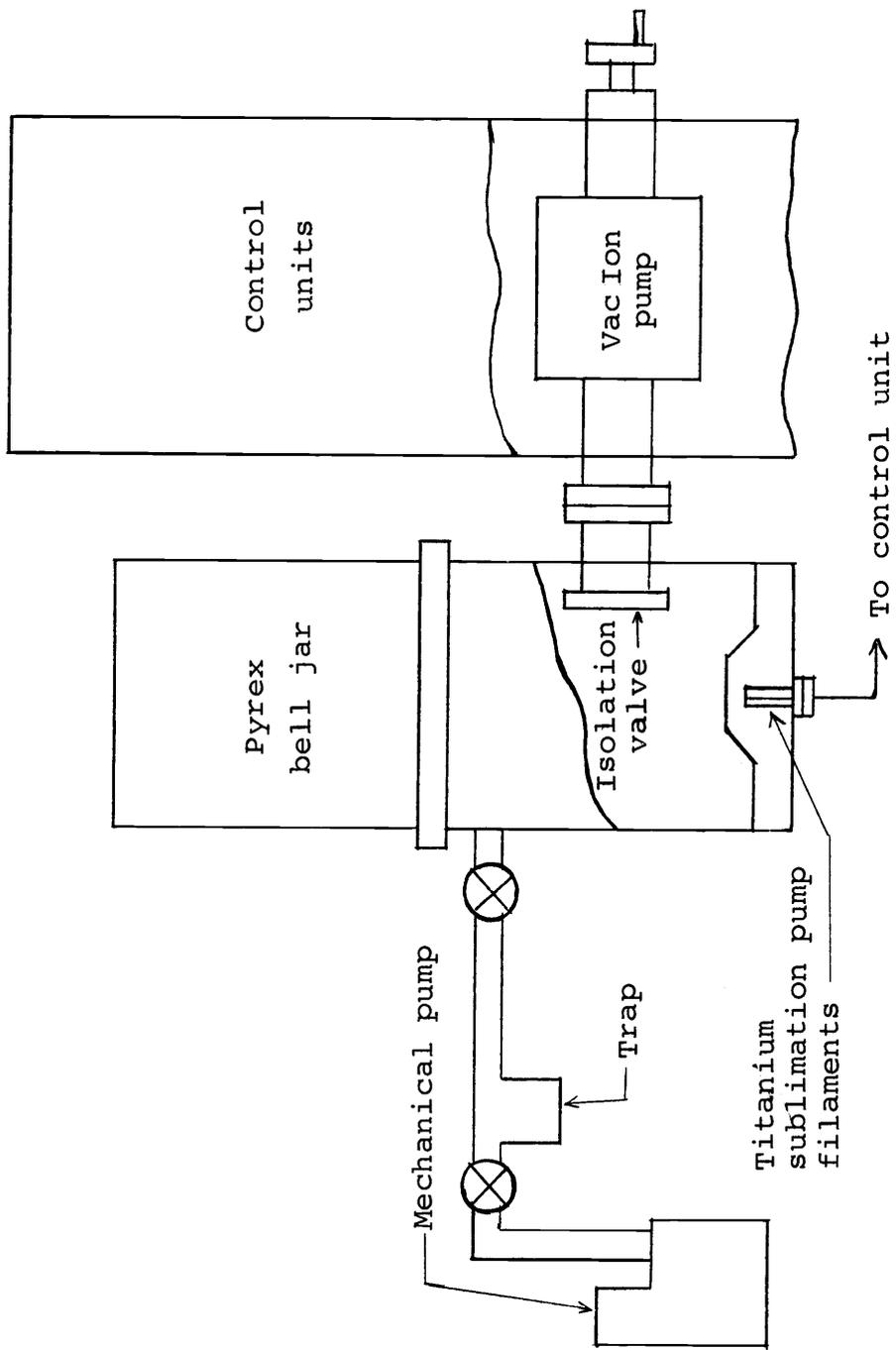


Figure 6. Schematic diagram of Varian vacuum system.

electron bombardment evaporation source. It consists of a filament (source of electrons), focusing magnet, and a water-cooled three crucible block (target). The focused electron beam from the filament strikes the evaporant material placed in the center of the water-cooled crucible. The 2000-watt maximum power of the beam is sufficient to evaporate refractory and dielectric materials as well as the more common conductive and semiconductor materials. The e-Gun source control unit provides convenient single-knob control of evaporation. It also provides the connection of a water-flow interlock, a pressure interlock, and a thickness monitor.

The substrate heater used in this project consisted of a ceramic disk heater. It was put directly on the upper face of the substrate holder. A thermocouple was attached to the face of the heater and was calibrated to read the actual temperature of the substrate.

The Sloan Instruments deposit thickness monitor (Model DTM-3) was used for monitoring and control of thickness of the deposited aluminum-oxide films. The mass of the deposit was measured by evaluating the change in frequency of an oscillating quartz crystal inside the vacuum system as a deposit built up on its surface.

#### E-Gun Evaporation Procedure

In a typical e-Gun deposition experiment, the

prepared substrate was mounted on the substrate holder. The substrate and its holder was then placed in the vacuum system. An appropriate section of sapphire, which had been prepared prior to evaporation, was then placed in the e-Gun crucible in the vacuum system. The shutter was closed over the evaporation port. The bell jar was lowered and the mechanical roughing pump was applied by opening the appropriate valve. When the chamber pressure decreased to 15 millitorr, the titanium sublimation pump was turned on, and when the pressure decreased to ten millitorr, the mechanical roughing pump was disconnected by closing the appropriate valve. The isolation valve of the VacIon pump was slowly opened. Both the titanium sublimation pump and the VacIon pump continued to evacuate the system until the chamber pressure decreased to  $10^{-7}$  torr. (It took several hours.)

Next, the deposition monitor and substrate heater were turned on. After a few minutes, the substrate temperature reached  $300^{\circ}$  C. Then the water valve to the e-Gun water-cooling system was turned on. The main power to the e-Gun was turned on and the beam current was increased to ten milliamperes. After 15 minutes, the evaporation source (sapphire) was heated up. Then the beam current was slowly increased until the sapphire began to evaporate (the beam current was usually about 50 milliamperes). The shutter was now opened and the frequency of the deposition

monitor was set in an appropriate position corresponding to the desired film thickness. The aluminum-oxide film was deposited on the substrate and the deposition monitor exhibited the frequency shift. When the aluminum-oxide film reached the required thickness, the relay in the deposit thickness monitor shut the e-Gun power supply off. Then the shutter was closed and the deposition monitor, the substrate heater, and the titanium sublimation pump were turned off. The pressure in the vacuum system during the e-Gun deposition was usually below  $2 \times 10^{-5}$  torr.

The substrate and the vacuum system were then allowed to cool for more than one hour before removing the substrate. After the cooling period, the water supply was shut off and the isolation valve of the VacIon pump was closed. Dry nitrogen (99.99%) was connected to the system to bring it up to atmospheric pressure. The nitrogen was then disconnected and the bell jar was raised. The substrate was removed from the vacuum system for further processing.

#### Measurement of Aluminum-Oxide Film Thickness

Several methods for measuring aluminum-oxide film thickness are available. In this project the multiple-beam interference method was used (3). The sample with a uniform aluminum oxide step, fabricated using e-Gun evaporation, was metallized by depositing a thin film of

aluminum on the surface with a vacuum evaporator. One surface of a glass piece was silvered to be approximately 80% reflecting. The silvered surface of the glass piece was placed directly in contact with the metallized surface of the sample. The combination was examined with a Unitron metallurgical microscope equipped with a monochromatic light source (sodium light,  $\lambda = 5893 \text{ \AA}$ , was used for this project). Light entering the combination underwent a series of multiple reflections giving rise to narrow sharp fringes. The silvered surface of the glass piece acted as a reference plane, and the fringes displayed the irregularities associated with the surface of the sample. The film thickness was calculated by (3):

$$d = p \frac{\lambda}{2}$$

where  $d$  = the aluminum-oxide film thickness

$p$  = the fringe displacement

$\lambda$  = the wavelength of the monochromatic light.

The accuracy of measurement was estimated to be 0.02 fringe, corresponding to  $\pm 59 \text{ \AA}$ .

#### Aluminum-Oxide Film Thickness versus Deposition

##### Monitor Frequency Change

The deposit thickness monitor was calibrated for aluminum-oxide films and for the vacuum system which was used throughout the project. It was calibrated by

evaporating various thicknesses of aluminum-oxide films onto clean silicon substrates and recording the corresponding change in deposition monitor frequency. While the evaporation was being done, the pressure was below  $2 \times 10^{-5}$  torr, the e-Gun beam current was 50 milliamperes, and the substrate temperature was  $300^{\circ}$  C. The distance between the e-Gun evaporation source and the substrate was eight inches. These evaporation conditions were typical of the values used for evaporation of aluminum oxide on the MOS devices which will be considered later. The actual thickness of the deposited films on silicon substrates were then measured using the multiple-beam interference method as described in the previous section. The mean values of aluminum-oxide film thickness versus deposition monitor frequency change is shown in Figure 7. The mean film thickness is the arithmetic mean of samples. The 95% confidence interval was calculated using a Student's t distribution. It is evident that the deposit thickness monitor frequency shift is directly proportional to the aluminum oxide thickness.

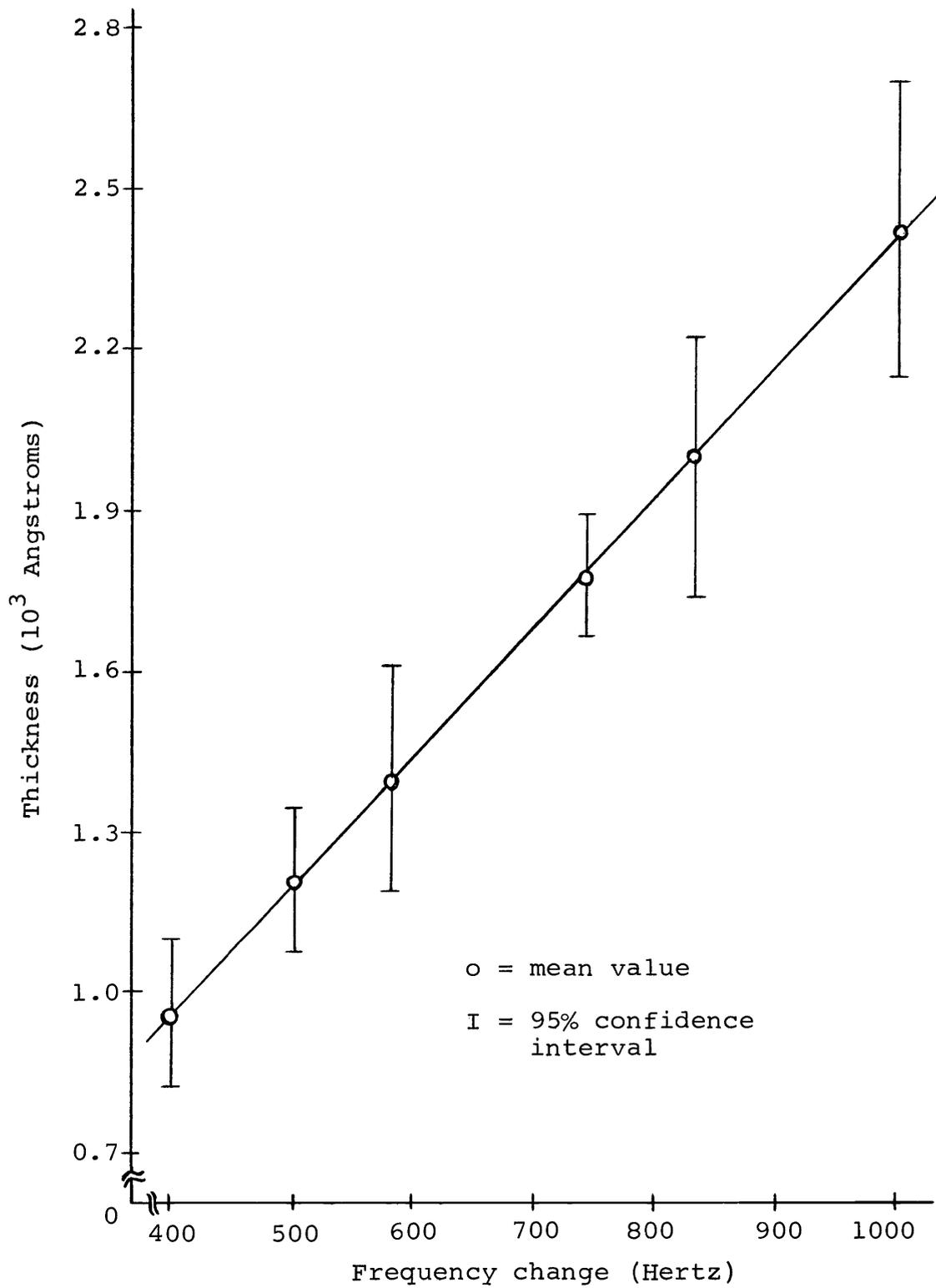


Figure 7. Deposited aluminum oxide thickness versus deposition monitor frequency change.

### III. PROPERTIES OF VACUUM-DEPOSITED ALUMINUM OXIDE

Before fabricating MOS devices with e-Gun evaporated aluminum-oxide films, some properties of the aluminum-oxide films were investigated. These properties may affect the characteristics of MOS devices or have effects on the procedures of fabricating the devices.

The aluminum-oxide films were deposited on the silicon substrates under the conditions outlined in the previous chapter. The aluminum-oxide films were assumed to be amorphous (6, p. 39). Various other properties were also investigated.

#### Density and Index of Refraction

The density and the index of refraction of aluminum-oxide films were measured by Delzer (6, p. 53). Delzer has reported that the density is about  $3-5 \text{ g/cm}^3$  and the refractive index is 1.66-1.79. Zaininger and Wang (16) have reported that the index of refraction is 1.6-1.7 for thin aluminum-oxide films. For the bulk material, the density and the index of refraction are  $3.5-4.0 \text{ g/cm}^3$  (7) and 1.665-1.680 or 1.63-1.65 (14, p. E219) respectively.

#### Number of Pinholes and Adhesion

The aluminum-oxide films were inspected for pinholes using a high power Unitron metallurgical microscope. There

were very few pinholes observable.

An important characteristic of the film is its adhesion to the silicon substrate. The Scotch tape test was used to examine the adhesion of the deposited aluminum-oxide films. A strip of Scotch tape was applied to the film and firmly rubbed in place. It was then lifted off. The film could withstand this test.

### Dielectric Strength and Dielectric Constant

To measure the electrical properties of the film, the MOS capacitors were employed. The aluminum-oxide films of 2000 Å thickness were evaporated on n-type silicon substrates (one ohm-cm) at the previously described deposition conditions. The films were then annealed in dry nitrogen for ten minutes at 1100° C. Aluminum dots,  $4 \times 10^{-4} \text{ cm}^2$  in area and 5000 Å thick, were evaporated on the aluminum-oxide films through a metal mask. A copper plating solution (five parts saturated  $\text{Cu}_2\text{SO}_4$  to one part 48% HF to six parts deionized water) was used to make an ohmic copper contact on the back side of the silicon substrates. These MOS capacitors were used to measure the dielectric properties.

Dielectric strength (breakdown strength) is computed from the breakdown voltages measurement. The breakdown voltages were measured using a Fairchild curve tracer Model 6200-B. It must be measured with the silicon

positive with respect to the metal (aluminum) electrode. The measured dielectric strength of the aluminum-oxide films is about  $6.2 \times 10^6$  V/cm. It has been reported by Delzer that the breakdown strength of aluminum-oxide films is about  $10^7$  V/cm (6, p. 62). It has also been reported by Zaininger and Wang (16) that the breakdown strength of thin aluminum-oxide films is in the  $2-7 \times 10^6$  V/cm range.

Dielectric constant (relative permittivity) is computed from the capacitance measurement. From the known area of the aluminum dot and the thickness of the oxide, the dielectric constant is calculated by

$$K_o = \frac{x_o C_o}{\epsilon_o A}$$

where  $K_o$  = dielectric constant of the oxide

$x_o$  = oxide thickness

$C_o$  = measured oxide capacitance

$\epsilon_o$  = permittivity of free space,  $8.86 \times 10^{-14}$  f/cm

A = area of the capacitor.

The measured dielectric constant of the aluminum-oxide film is about 8.3. Delzer reported it was from about 8.3 to 8.8 (6, p. 54). Zaininger and Wang reported that the dielectric constant for thin aluminum-oxide film is 7.6 (16). The dielectric constant of the silicon dioxide is 3.9 (8, p. 102). The value of the dielectric constant of aluminum oxide is about twice that of silicon dioxide.

### Etching Properties

In order to facilitate the processes in fabricating MOS transistors, etching tests were made on the aluminum-oxide films. The etchants were buffered HF, phosphoric acid ( $H_3PO_4$ ), and aluminum etch. Buffered HF, which is usually used for silicon dioxide etching, has been described in the previous chapter. Aluminum etch solution, which is usually employed for aluminum etching, is made by mixing 80 parts of  $H_3PO_4$  (concentration 85%) to 16 parts of deionized water to five parts of  $HNO_3$  (concentration 70%).

The unannealed aluminum oxide can be etched by using buffered HF, hot phosphoric acid ( $H_3PO_4$ ), or hot aluminum etch. The etch rate in hot phosphoric acid (about  $200^\circ C$ ) or hot aluminum etch (about  $80^\circ C$ ) is greater than in buffered HF. For a  $1000 \text{ \AA}$  thick aluminum-oxide film, it only took about one minute to etch off in hot phosphoric acid or in hot aluminum etch. After a heat treatment in dry nitrogen at  $1100^\circ C$  for ten minutes, the aluminum oxide is hard to etch off using buffered HF or hot aluminum etch. Only the hot phosphoric acid can still etch the annealed aluminum oxide though the etch rate decreases drastically. It took about three minutes to etch  $2000 \text{ \AA}$  thickness of annealed aluminum-oxide film in hot  $H_3PO_4$ .

The hot aluminum etch solution etches the

unannealed aluminum oxide. And the photo-resist AZ-1350 can withstand the hot aluminum etch solution. Thus the aluminum etch can be used to etch the aluminum oxide in fabricating MOS transistors.

#### Diffusion Masking Properties

The diffusion masking properties of the e-Gun evaporated aluminum-oxide films have been tested by Delzer (6). It has been concluded that the  $\text{Al}_2\text{O}_3$  films were better diffusion masks because they were more impervious to the diffusion of impurities (6, p. 126). In this project no experiment was made to test the diffusion masking properties.

#### IV. FABRICATION AND PROPERTIES OF MOS CAPACITORS

The capacitance versus bias behavior of MOS device is sensitive to the physical properties of the insulator-semiconductor interface. Thus MOS capacitors are the most frequently employed structures for evaluating insulator properties and insulator-semiconductor interface properties (9,12,5,2). The MOS theory has been discussed in Chapter I. In this project three kinds of MOS capacitors were fabricated. They were MOS capacitors with (1) single-layer silicon dioxide, (2) single-layer aluminum oxide, and (3) double-layer silicon dioxide-aluminum oxide films as gate insulation. Then the structures were evaluated by MOS capacitance-voltage (C-V) measurements.

##### Fabrication of MOS Capacitors

All of the MOS capacitors were fabricated on one ohm-cm ( $N_D = 5.3 \times 10^{15} \text{ cm}^{-3}$ ) n-type silicon wafers with (111) crystal orientation. Initially, the silicon wafers were cleaned using trichlorethylene, acetone, 4:1 buffered HF, and deionized water. The surface contamination and residual silicon dioxide were thereby removed.

For the single-layer silicon-dioxide films, the silicon substrates were oxidized in wet oxygen (0.4 cfh oxygen bubbled through 95° C deionized water) at 1100° C for six minutes in the oxidation furnace. The substrates were

then transferred to the phosphorus deposition furnace where the phosphorus compensation was made for 15 minutes. The films were then annealed in dry nitrogen at 1100° C for six and a half minutes. For the single-layer aluminum-oxide films, the silicon substrates were placed in the vacuum system. Aluminum-oxide films of about 1500 Å thick were evaporated on the heated substrates (300° C). The films were then annealed in dry nitrogen at 1100° C for 12 minutes. For the double-layer films, the silicon substrates were first oxidized in wet oxygen (0.4 cfh) at 1100° C for 30 seconds in the oxidation furnace to grow 500 Å of silicon dioxide; then aluminum-oxide films of 1000 Å thickness were deposited on the thermally grown SiO<sub>2</sub>. The double-layer films were then annealed in dry nitrogen at 1100° C for 12 minutes.

The substrates were placed in a small vacuum system where 5000 Å of aluminum was filament evaporated over the oxide films. The aluminum films were alloyed at 530° C with 2.0 cfh nitrogen flow rate for five minutes and were then annealed in nitrogen at 400° C for 30 minutes. Using the photo-resist, appropriate mask, and aluminum etch solution, the aluminum was etched off the substrates except the desired capacitor pattern (5 mils X 5 mils). The copper ohmic contacts were then plated on the back side of the wafers, using a copper plating solution. The MOS capacitors were ready for testing.

### Equipment for C-V Measurement

In this project a large number of capacitors had to be measured. An automatic and rapid method of measurement of the continuous MOS capacitance versus bias was used. It is better than the capacitance bridge method which is extremely time-consuming. The equipment arrangement for automatically measuring MOS C-V characteristics is shown in Figure 8. A Tektronix type 3C66 carrier amplifier (25 KHz carrier) and a type 67 time base plugged into a Tektronix type 564 storage oscilloscope were actually used. The capacitance range of this equipment is from one pf/DIV to 1000 pf/DIV. The C-V characteristics were displayed on the storage scope and permanent copies can be obtained by means of a Polaroid camera. In this project a Houston Instrument HR-93 X-Y recorder was used to record the C-V characteristics on graph paper.

MOS capacitors were measured immediately after their fabrication on the silicon wafers in air, and the bias-temperature tests were made after measuring the initial C-V characteristics.

### MOS Capacitor Tests

The fabricated MOS capacitors were measured using the automatic display and plotting equipment described in the previous section. First the capacitance versus bias (C-V)

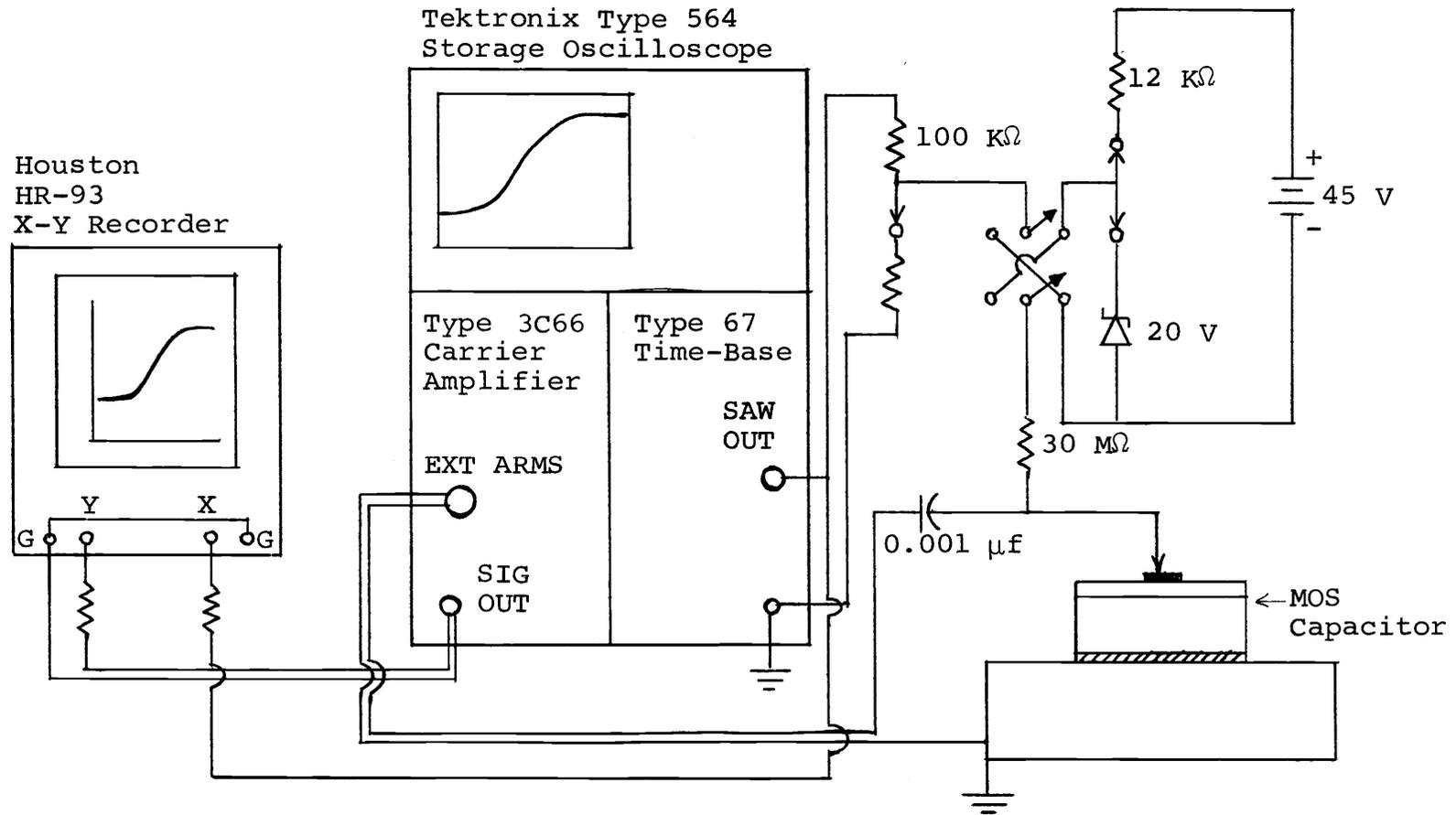


Figure 8. Schematic diagram of equipment for automatic display and record of MOS capacitance versus bias characteristics.

characteristics of capacitors were taken at room temperature. Then the bias-temperature (B-T) tests were performed. The capacitors were heated to 250° C with a bias of -20 volts (or -34 volts) on the gate electrode. This bias was allowed to remain on the heated capacitors for ten minutes, and then the capacitors were cooled rapidly to the room temperature. The C-V characteristics were again measured for the capacitors. Then, the capacitors were again heated to 250° C with a bias of +20 volts (or +34 volts) on the gate electrode. This bias was also allowed to remain on the heated capacitors for ten minutes, and then the capacitors were cooled rapidly to room temperature. The C-V characteristics were again measured. The bias-temperature tests were repeatedly taken with alternative bias polarity. The measured and normalized C-V characteristics for each type of gate dielectric are given in Figures 9, 10, and 11. In these figures the abscissa shows the gate bias voltage while the ordinate shows the normalized capacitance. In these figures, curve 1 was the initial C-V curve made on the devices. Curve 2 was measured after -20 volts (or -34 volts) bias at 250° C for ten minutes. Curve 3 was measured after +20 volts (or +34 volts) bias at 250° C for ten minutes. Curve 4 was measured after -20 volts (or -34 volts) bias at 250° C for ten minutes. Curve 5 was measured after +20 volts (or +34 volts) bias at 250° C for ten minutes. And

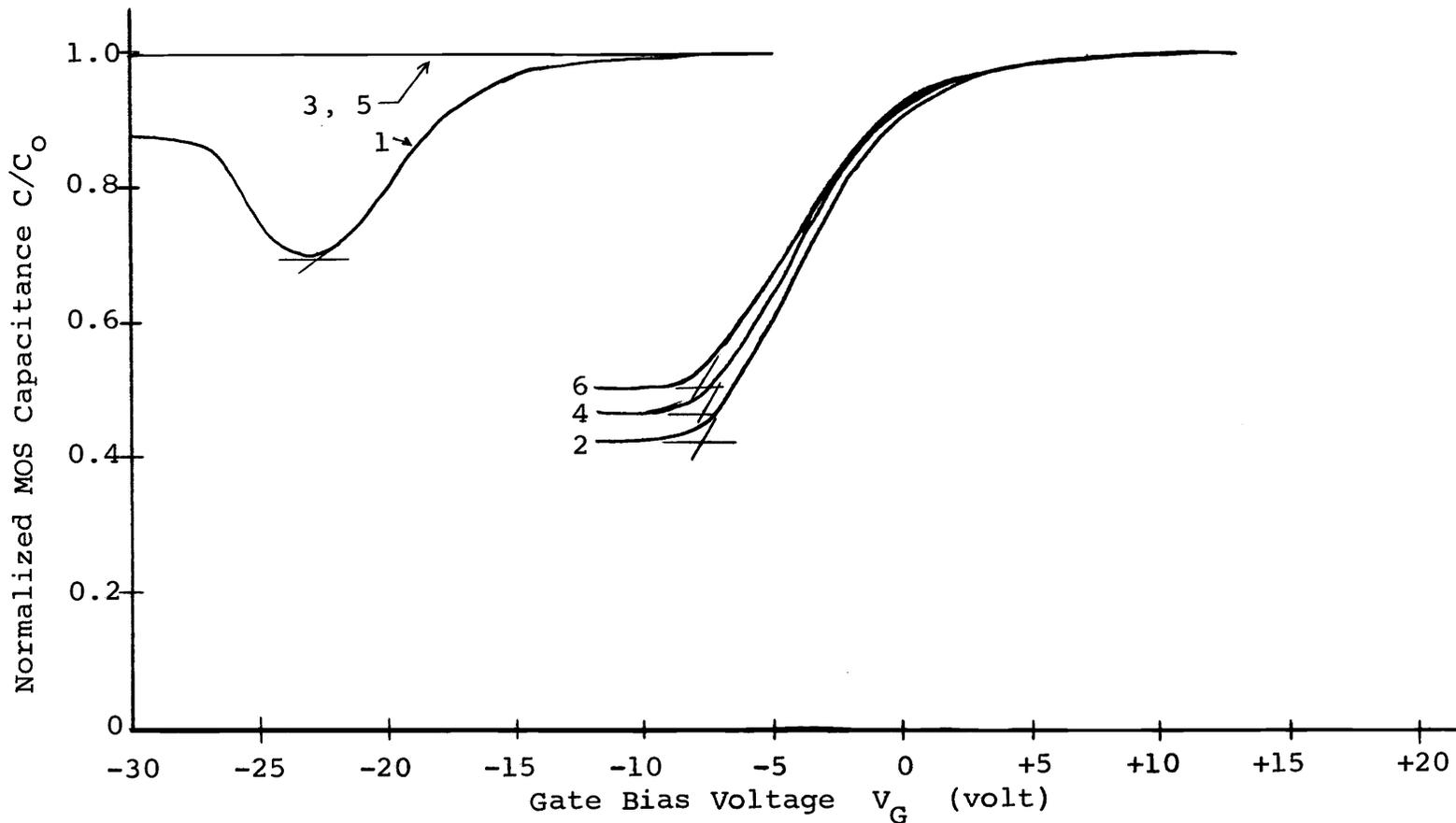


Figure 9. Single-layer silicon dioxide MOS capacitor C-V characteristics and bias-temperature tests.

1. Initial characteristic.
2. After 10 minutes at -34 V, 250° C.
3. After 10 minutes at +34 V, 250° C.
4. After 10 minutes at -34 V, 250° C.
5. After 10 minutes at +34 V, 250° C.
6. After 10 minutes at -34 V, 250° C.

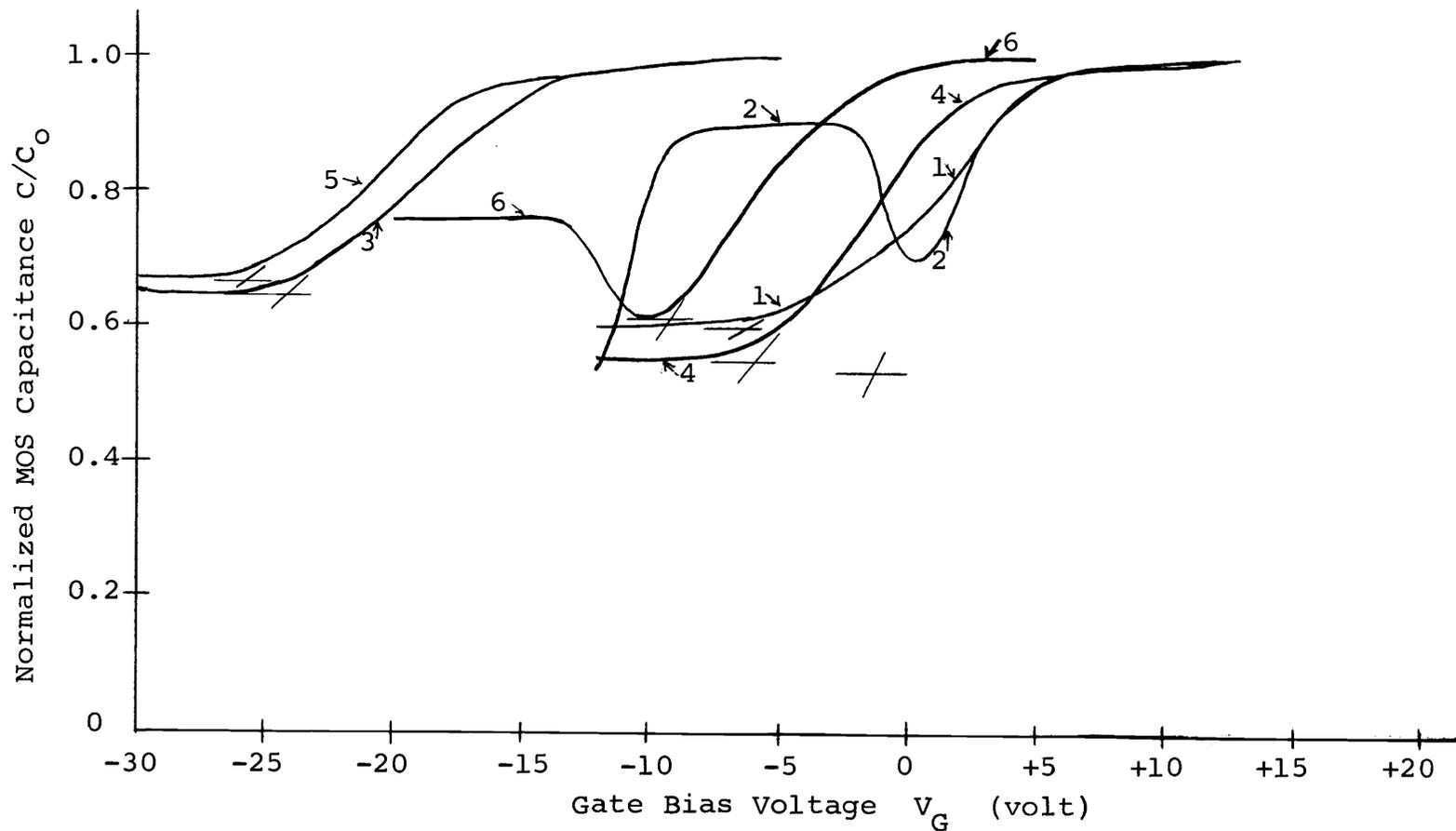


Figure 10. Single-layer aluminum oxide MOS capacitor C-V characteristics and bias-temperature tests.

1. Initial characteristic.
2. After 10 minutes at -20 V, 250° C.
3. After 10 minutes at +20 V, 250° C.
4. After 10 minutes at -20 V, 250° C.
5. After 10 minutes at +20 V, 250° C.
6. After 10 minutes at -20 V, 250° C.

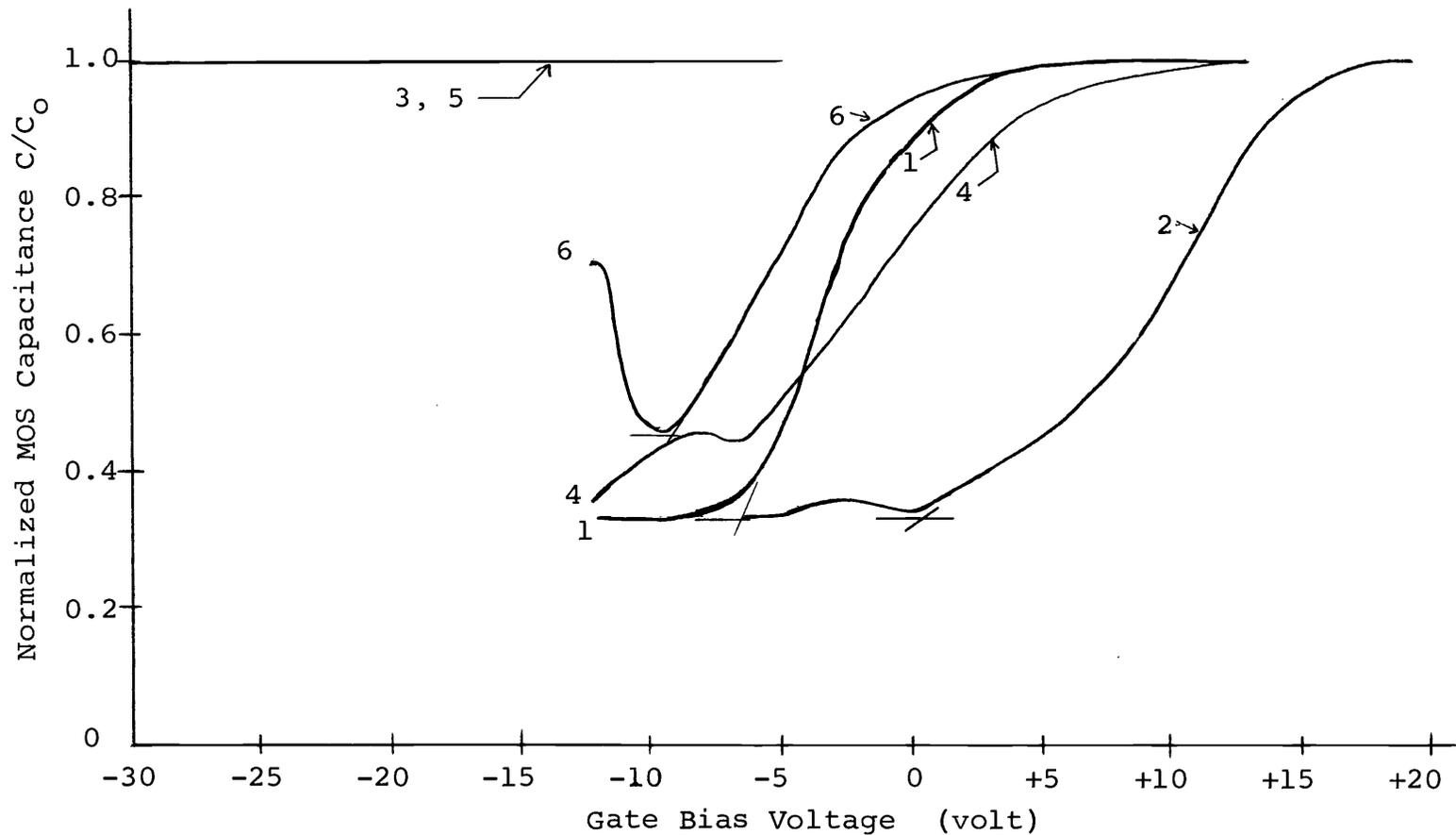


Figure 11. Double-layer silicon dioxide-aluminum oxide MOS capacitor C-V characteristics and bias-temperature tests.

1. Initial characteristic.
2. After 10 minutes at -20 V, 250° C.
3. After 10 minutes at +20 V, 250° C.
4. After 10 minutes at -20 V, 250° C.
5. After 10 minutes at +20 V, 250° C.
6. After 10 minutes at -20 V, 250° C.

curve 6 was measured after -20 volts (or -34 volts) bias at 250° C for ten minutes.

Figure 9 shows the C-V characteristics and bias-temperature tests for the MOS capacitor with single-layer silicon dioxide as the gate insulator. The threshold voltages or turn-on voltages of the curves are listed in Table II. The flat-band voltages exhibited very large

Table II. Threshold voltages of the MOS capacitors with single-layer silicon dioxide (Figure 9), single-layer aluminum oxide (Figure 10), and double-layer oxide (Figure 11) as gate insulation.

Curve No.	Figure 9	Figure 10	Figure 11
1	-23 V	-6 V	-6.5 V
2	-7.3 V	-1.5 V	+0.5 V
3	<-30 V	-24.5 V	<-30 V
4	-7.5 V	-6 V	-8 V
5	<-30 V	-26 V	<-30 V
6	-7.5 V	-9.5 V	-9.5 V

drifts after the bias-temperature tests. It can be attributed to the ionic charges within the silicon-dioxide film. From the shift directions of the flat-band voltages relating to the bias voltage polarities, it revealed there was positive ionic contamination within the silicon dioxide. This may be attributed to the sodium ionic contamination (12). After +34 volts bias at 250° C for ten minutes,

there were no threshold voltages shown on curves 3 and 5. The threshold voltages were greater than -40 volts (the negative magnitudes were more than 40 volts). It means that the space charge density is more than  $3.5 \times 10^{12} \text{ cm}^{-2}$ . After the bias-temperature tests the C-V curves were almost recoverable.

Figure 10 shows the C-V characteristics and bias-temperature tests for the MOS capacitor with single-layer aluminum oxide as gate dielectric. The threshold voltages or turn-on voltages of the curves are listed in Table II. The flat-band voltages also exhibited very large drifts after the bias-temperature tests, which also can be attributed to the sodium ionic contamination within the aluminum oxide. From curves 2 and 3, the space charge density can be calculated and it is about  $4.9 \times 10^{12} \text{ cm}^{-2}$ . In the figure, the C-V curves which were measured after the bias-temperature tests were not simply horizontal displacement of the initial curve. Also, the C-V characteristics and the threshold voltages were not the same even when measured after the same bias conditions. It may be interpreted that these distorted and irrecoverable curves were due to nonuniform space charge distribution and the sodium ions were less mobile in aluminum oxide, thus they must take longer than ten minutes for rearrangement under the bias-temperature conditions.

Figure 11 shows the C-V characteristics and

bias-temperature tests for the MOS capacitor with double-layer film as the gate insulation. The threshold voltages or turn-on voltages of the curves are listed in Table II. The flat-band voltages also exhibited very large drifts after the bias-temperature tests, which also can be attributed to the sodium ionic contamination within the gate dielectric. After +20 volts bias at 250° C for ten minutes, there were no threshold voltages shown on curves 3 and 5. The threshold voltages were greater than -40 volts (the negative magnitudes were more than 40 volts), indicating that the space charge density was more than  $7.2 \times 10^{12} \text{ cm}^{-2}$ . The C-V characteristic curves also revealed the different curve shapes and after the bias-temperature tests they had the tendency to shift to the more negative direction. It also may be assumed that they were due to nonuniform space charge distribution and the sodium ions were less mobile in the double-layer films.

In these three figures, the initial C-V characteristics revealed all the MOS capacitors had large threshold voltages. They had much sodium contamination within their gate insulation. This contamination may be introduced in the processes used in fabrication of the devices since these capacitors were made with the same procedure used for fabricating the MOS transistors. Though they all had large threshold voltages, the capacitors with single-layer aluminum oxide as gate dielectric had the smallest

threshold voltages. Both the capacitors with single-layer aluminum oxide and double-layer films had less threshold voltages than the capacitors with single-layer silicon-dioxide films. And in the bias-temperature tests, there sometimes was conduction phenomena in the aluminum oxide films, indicating that the aluminum-oxide films had a greater tendency toward conduction than silicon-dioxide films. It has also been observed by Duffy and Revesz (7) for the aluminum-oxide films obtained by thermal decomposition of aluminum-isopropoxide. For the purpose of investigating the interface properties with less contamination in oxide, further tests were performed which are discussed in Chapter VI.

## V. FABRICATION AND PROPERTIES OF MOS TRANSISTORS

The theory of MOS field-effect transistors has been discussed in Chapter I. In this project MOS transistors with single-layer aluminum-oxide films and double-layer silicon dioxide-aluminum oxide films as the gate insulation were fabricated. Also, the MOS transistors with single-layer silicon-dioxide films as gate insulation were fabricated. The characteristics of these transistors were measured.

### MOS Transistors Fabrication

All of the MOS transistors were fabricated using one ohm-cm ( $N_D = 5.3 \times 10^{15} \text{ cm}^{-3}$ ) n-type silicon wafers with (111) crystal orientation. Only enhancement mode transistors were fabricated and considered. These MOS transistors had winding channels with channel width  $W = 75$  mils and channel length  $L = 0.625$  mils. The geometry of the MOS transistor is shown in Figure 12.

Initially, the silicon wafers were cleaned using trichlorethylene, acetone, 4:1 buffered HF, and deionized water to remove any surface contamination and residual silicon dioxide. Then the substrates were oxidized in wet oxygen (0.4 cfh oxygen bubbled through 95° C deionized water) for two hours at 1100° C in an oxidation furnace. The silicon dioxide masking layer of 8600 Å thickness was

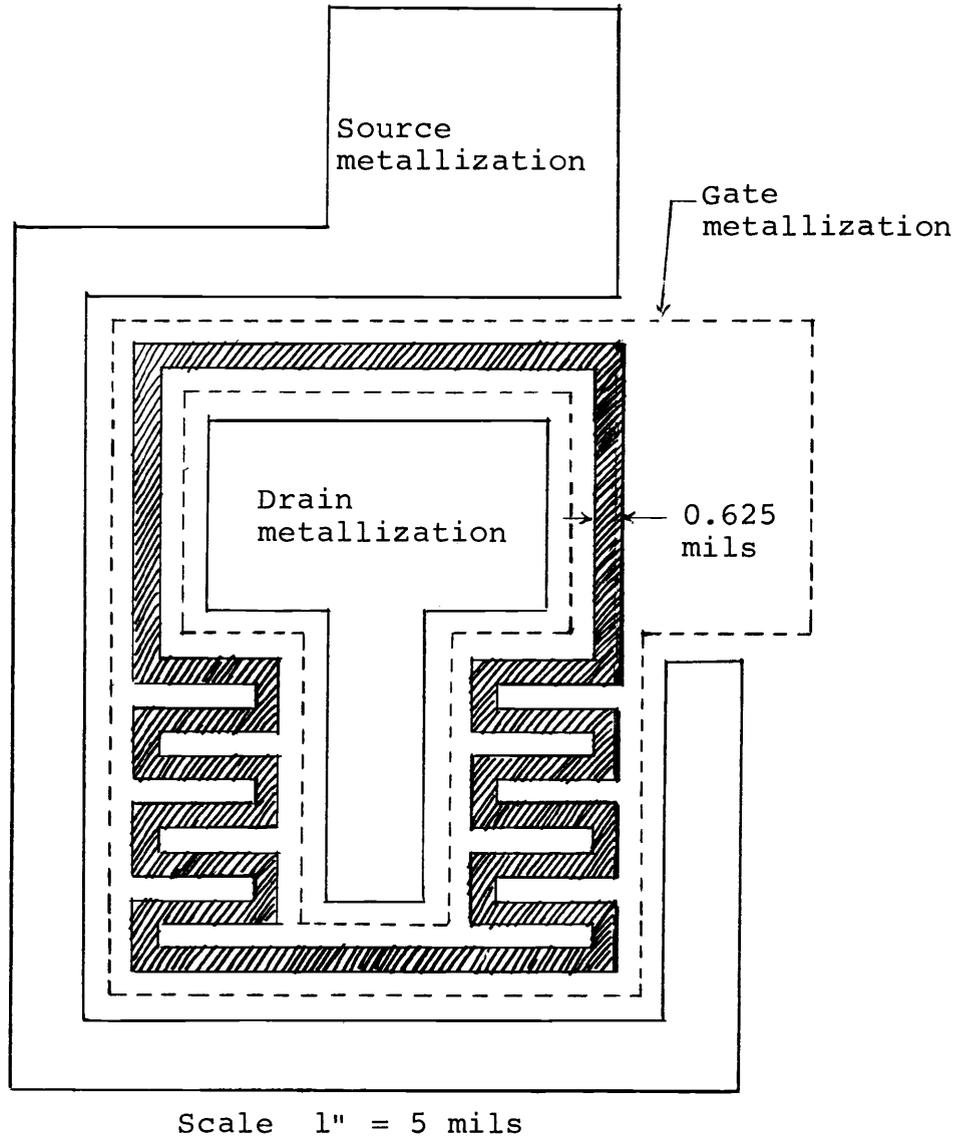


Figure 12. The fabricated MOS transistor geometry.

$W = 75$  mils,  $L = 0.625$  mils

grown on the silicon surface. The substrates with oxide films were annealed in dry nitrogen for 30 minutes at 1100° C. Next, using an appropriate photographic glass mask, AZ-1350 positive photoresist, and 4:1 buffered HF, the source-drain windows were cut through the masking oxide. After etching, the remaining photoresist was removed, leaving the silicon dioxide masking window pattern.

The wafers were coated with borofilm (a solution of boron containing polymers in water) and were baked on hot plate (150° C) for three minutes. Then the substrates were placed in the diffusion furnace. Boron was soaked into the source-drain regions of the substrates at 1100° C in air for 15 minutes. After boron deposition, the substrates were removed from the furnace. They were boiled in deionized water for 30 minutes and etched in 4:1 buffered HF for one minute to remove the boron film grown during deposition.

Then, using an appropriate glass mask, photoresist and 4:1 buffered HF, the silicon dioxide on gate area was etched away. After etching, the remaining photoresist was removed by using acetone. The sheet resistances were measured. They were about 15-20 ohms/square. The substrates were boiled for 15 minutes in deionized water, rinsed in deionized water, and dried using dry nitrogen.

For single-layer silicon-dioxide films, the silicon substrates were oxidized for five and a half minutes in wet oxygen (0.4 cfh oxygen bubbled through 95° C deionized

water) at  $1100^{\circ}$  C in an oxidation furnace. The silicon dioxide of  $1500 \text{ \AA}$  thickness was grown on the gate area. Then the substrates were transferred to the phosphorus deposition furnace where the phosphorus compensation was made for 15 minutes. The substrates were then moved back to the oxidation furnace where the films were annealed in dry nitrogen for six and a half minutes at  $1100^{\circ}$  C. For single-layer aluminum-oxide gate dielectrics, the substrates were placed in the vacuum system. Aluminum-oxide films of about  $1500 \text{ \AA}$  thickness were evaporated onto the heated substrates ( $300^{\circ}$  C). For the double-layer dielectric films, the substrates were first placed in the oxidation furnace for 30 seconds to grow  $500 \text{ \AA}$  of silicon dioxide in wet oxygen and then they were placed in the vacuum system where about  $1000 \text{ \AA}$  of aluminum oxide were evaporated over the silicon dioxide.

The source-drain contact holes were cut through the dielectrics using an appropriate glass mask, photoresist, and etching solution. For single-layer silicon-dioxide films 4:1 buffered HF was used. For single-layer aluminum-oxide films the aluminum etch, described in Chapter III, was used. For double-layer oxide films the aluminum etch was used for etching aluminum oxide, then the 4:1 buffered HF was used for etching silicon dioxide. After etching, the photoresist was removed, using acetone. The substrates were rinsed in deionized water and dried with nitrogen.

The substrates containing single-layer aluminum-oxide films and double-layer films were placed in the furnace and then annealed in dry nitrogen for 12 minutes at 1100° C.

Then the wafers were placed in a small vacuum system and an aluminum layer about 5000 Å in thickness was evaporated over the surface of the wafers. The aluminum films were alloyed in the furnace at 530° C for six minutes in dry nitrogen (2.0 cfh) and annealed at 400° C for 30 minutes in dry nitrogen. The unwanted metal was then etched away, using an appropriate mask, photoresist, and aluminum etch solution. After etching, the photoresist was removed, using acetone. The substrates were rinsed in deionized water and dried using dry nitrogen. Copper was plated on the back side of the wafers to insure good ohmic contacts to the substrates. The MOS transistors were thus completed and ready for testing.

### MOS Transistor Tests

MOS transistors were measured after their fabrication in the silicon wafer. The wafer was mounted on the holder and the micromanipulators were used as wire contacts. A Fairchild 6200-B curve tracer was used. The drain current-voltage (I-V) characteristics; threshold voltages,  $V_{th}$ ; transconductance,  $g_m$ ; effective hole mobility,  $\mu_p$ ; and drain diode breakdown voltage,  $BV_{DSS}$  were obtained. These are the important characteristics for evaluating the

device capabilities. Both the experimental and theoretical characteristics are listed in Table III.

The measured typical I-V characteristics of the MOS transistors are shown in Figures 13, 14 and 15. In these figures, the vertical axes represent the drain current and the horizontal axes represent the drain voltage. The source and the substrate were grounded. Figure 13 shows the I-V characteristics of the MOS transistor with single-layer silicon dioxide as gate insulation. During I-V measurement, the drain currents shifted at the room temperature. Figure 14 shows the I-V characteristics of the MOS transistor with single-layer aluminum oxide as gate insulation. During the I-V measurement, the drain currents shifted drastically even at the room temperature. The transistors revealed very unstable characteristics. Figure 15 shows the I-V characteristics of the MOS transistor using double-layer film as gate insulation. During the I-V measurement the drain currents shifted slightly at room temperature. All of the fabricated MOS transistors with different gate insulation revealed unstable I-V characteristics. This can be attributed to the ionic contamination in the gate oxide. It was the same factor that caused the C-V characteristics of the MOS capacitors to drift as seen in the previous chapter. Though all of the MOS transistors had unstable characteristics, the transistors with double-layer gate dielectrics exhibited the most stable ones.

Table III. Experimental and theoretical characteristics of MOS transistors using various dielectrics.

Type of dielectric	Single-layer SiO <sub>2</sub>	Single-layer Al <sub>2</sub> O <sub>3</sub>	Double-layer SiO <sub>2</sub> -Al <sub>2</sub> O <sub>3</sub>
Measured V <sub>th</sub> (volts)	-9.2— -12.3	-1.6— -5.2	-3.2— -4
Measured μ <sub>p</sub> (cm <sup>2</sup> /V-sec)	185—215	165—200	240—275
Calculated μ <sub>p</sub>	200—210 for V <sub>G</sub> = -12 V, V <sub>th</sub> = -5 V		
Measured g <sub>m</sub> (μmhos)	2900—3300 V <sub>G</sub> = -20 V	4500—5000 V <sub>G</sub> = -12 V	4800—5400 V <sub>G</sub> = -12 V
Calculated g <sub>m</sub> (μmhos)	4750—5040 V <sub>G</sub> = -20 V V <sub>th</sub> = -5 V	4720—4950 V <sub>G</sub> = -12 V V <sub>th</sub> = -5 V	4850—5100 V <sub>G</sub> = -12 V V <sub>th</sub> = -5 V
Measured BV <sub>DSS</sub> (volts)	-34— -40	-20— -25	-26— -30
Calculated BV <sub>DSS</sub>	about -45 volts, assume junction radius = 1.5 μ.		

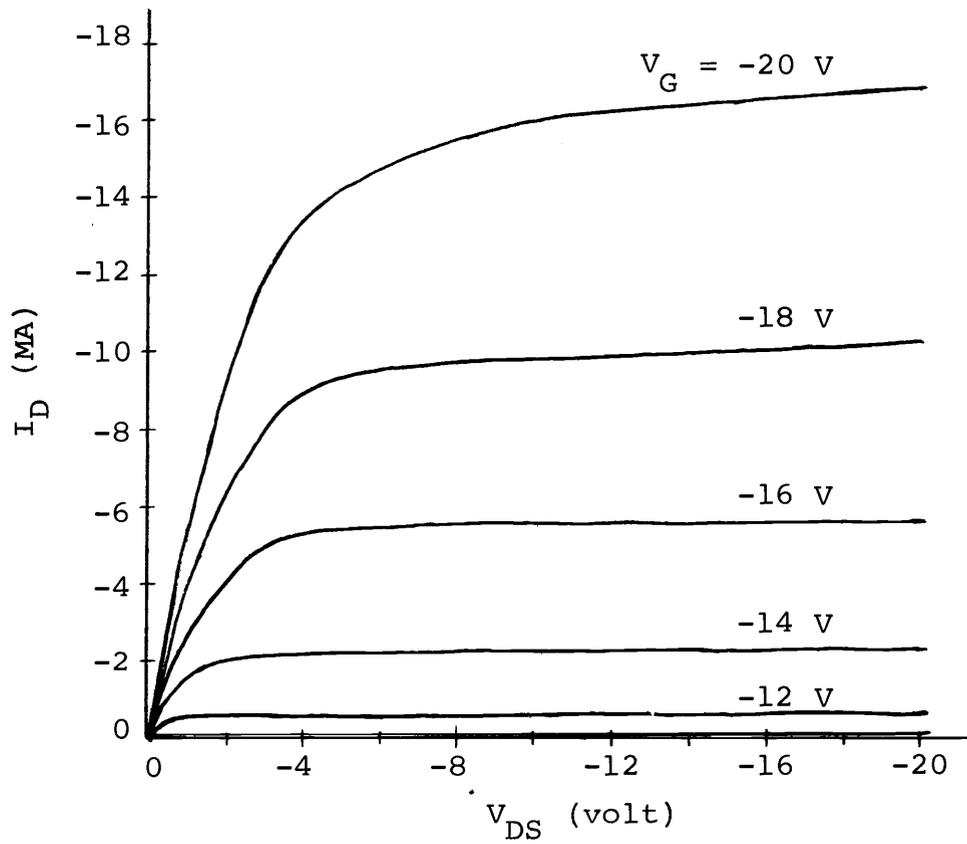


Figure 13. Typical I-V characteristic for p-channel MOS transistor with single-layer silicon dioxide as gate insulation.

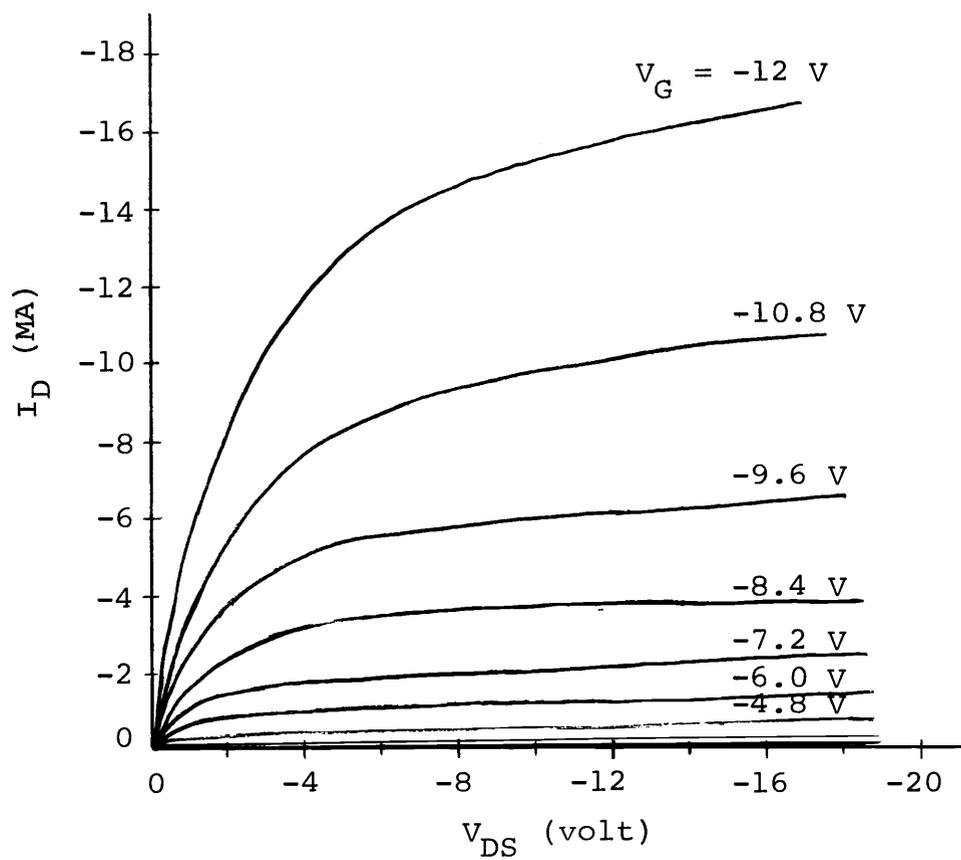


Figure 14. Typical I-V characteristic for p-channel MOS transistor with single-layer aluminum oxide as gate insulation.

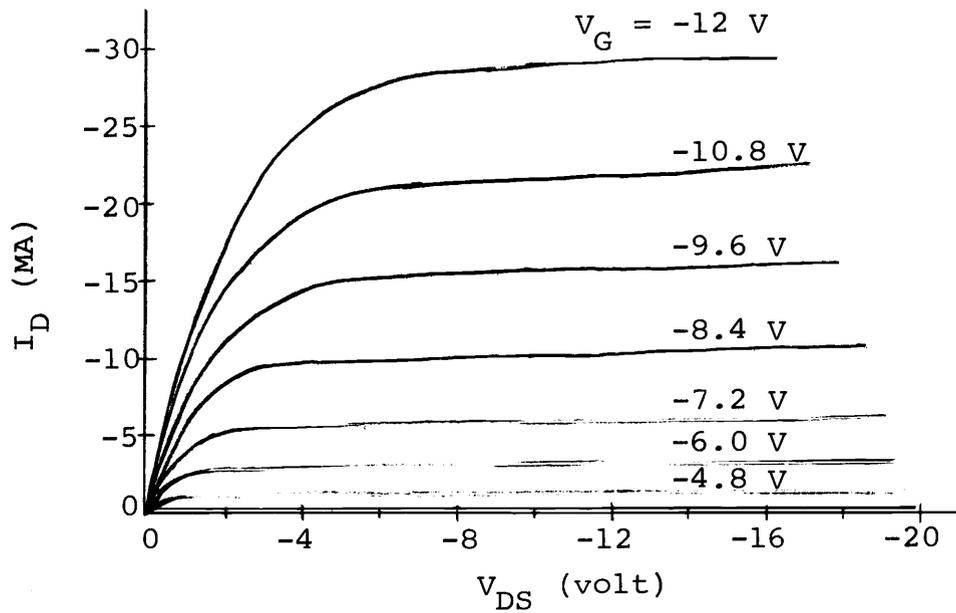


Figure 15. Typical I-V characteristic for p-channel MOS transistor with double-layer silicon dioxide-aluminum oxide film as gate insulation.

The threshold voltage,  $V_{th}$ , was measured as the gate voltage at a drain current of ten microamperes. The measured threshold voltages of various MOS transistors are: from -9.2 to -12.3 volts for single-layer silicon dioxide gate insulation, from -1.6 to -5.2 volts for single-layer aluminum oxide gate insulation, and from -3.2 to -4 volts for double-layer films gate insulation. Although there was contamination in the gate insulators, the MOS transistors with single-layer aluminum-oxide films or double-layer films as gate insulation still had reasonable threshold voltages. If there had been less contamination in their gate insulation, the threshold voltages might be reduced to a smaller value. However, the transistors using silicon dioxide as gate dielectric revealed unreasonable threshold voltages. In general, MOS transistors built on 1-2 ohm-cm n-type (111) silicon substrates have threshold voltages of about -4 to -6 volts (15).

In the saturation region, the drain current is given by:

$$I_D = -\frac{W}{2L}\mu_p C_o (V_G - V_{th})^2.$$

The effective hole mobility,  $\mu_p$ , can be obtained using this equation. In the experiment, the saturated drain currents,  $I_D$ , corresponding to each gate voltage,  $V_G$ , were measured. Then the curve of  $\sqrt{-I_D}$  versus  $V_G$  was plotted and the slope of the curve was measured. The ratio of the channel width,  $W$ , to the channel length,  $L$ , was 120

for the fabricated transistors. The capacitance per unit area of oxide layer,  $C_o$ , was measured. Then the effective hole mobility is

$$\mu_p = \frac{2L}{WC_o} (\text{the slope of } \sqrt{I_D} \text{ versus } V_G \text{ curve})^2.$$

The measured effective hole mobilities were about 185-215  $\text{cm}^2/\text{V-sec}$ , 165-200  $\text{cm}^2/\text{V-sec}$ , and 240-275  $\text{cm}^2/\text{V-sec}$  for transistors with single-layer silicon dioxide, single-layer aluminum oxide, and double-layer films as gate insulation, respectively. If the equation given by Crawford (4, p. 68) is used, the calculated mobility is about 200-210  $\text{cm}^2/\text{V-sec}$  for  $V_G = -12$  volts and  $V_{th} = -5$  volts. The measured mobilities are approximately equal to or greater than this value.

The transconductance,  $g_m$ , of the transistor is defined by

$$g_m = \left. \frac{\partial I_D}{\partial V_G} \right|_{V_D = \text{constant}}.$$

In the experiment, from the transistor I-V characteristics the incremental drain current,  $\partial I_D$ , corresponding to the incremental gate voltage,  $\partial V_G$ , at some gate voltage was measured. Then the transconductance of the transistor at that gate voltage was obtained. Or the transconductance can be calculated by using the equation

$$g_m = \frac{W}{L} \mu_p C_o (V_G - V_{th}).$$

The measured transconductances were about 2900-3300  $\mu\text{mhos}$  at  $V_G = -20$  volts and  $V_D = -16$  volts for the transistors with single-layer silicon dioxide gate insulation. The measured transconductances were about 4500-5000  $\mu\text{mhos}$  and 4800-5400  $\mu\text{mhos}$  at  $V_G = -12$  volts and  $V_D = -16$  volts for the transistors with single-layer aluminum oxide and double-layer gate insulation respectively. If the equation is used, the calculated transconductances are about 4750-5040  $\mu\text{mhos}$ , 4720-4950  $\mu\text{mhos}$ , and 4850-5100  $\mu\text{mhos}$  for the transistors with single-layer silicon dioxide, single-layer aluminum oxide, and double-layer films as gate insulations, respectively (assume  $\mu_p = 200-210 \text{ cm}^2/\text{V-sec}$ ,  $V_{th} = -5$  volts,  $V_G =$  as mentioned above).

The drain diode breakdown voltage was measured when the gate electrode was biased to the negative voltage and the source and substrate were grounded. The measured drain diode breakdown voltages of the fabricated MOS transistors were -34 to -40 volts for the single-layer silicon dioxide gate insulation, -20 to -25 volts for the single-layer aluminum oxide gate insulation, and -26 to -30 volts for the double-layer gate insulation. Theoretical drain diode breakdown voltage may be estimated from the figure given by Hofstein (13, p. 133). If the space charge curvature of  $1.5 \mu$  near the surface is used the drain diode breakdown voltage is about -45 volts.

It has been reported by Zaininger and Waxman (17)

that the MOS devices employing a gate insulator obtained by plasma anodization of evaporated aluminum possess remarkable radiation resistance. In this project the radiation effects were not tested. Since the dielectric constant of aluminum oxide is about twice as large as that of silicon dioxide, an identical change in the surface charge, as due to irradiation, gives rise to only half the shift in the flat-band voltage. Thus silicon-aluminum oxide structures are more resistant to high energy electron radiation than MOS devices using silicon dioxide as insulator.

From the characteristics of the fabricated MOS transistors, it can be seen that the transistors using silicon dioxide-aluminum oxide double-layer films as gate insulation are the best ones. And in every run of fabrication three wafers were used for various dielectrics -- single-layer  $\text{SiO}_2$ , single-layer  $\text{Al}_2\text{O}_3$ , and  $\text{SiO}_2$ - $\text{Al}_2\text{O}_3$  double-layer films. This always showed that the transistors using double-layer films as gate insulation were more stable and better than the others.

## VI. FURTHER EVALUATION OF MOS CAPACITORS

The MOS capacitors described previously were fabricated at the same time as MOS transistors were fabricated. The processes were more complicated than just fabricating MOS capacitors only and the gate dielectrics were severely contaminated because of the extra processing. For the purpose of investigating the aluminum oxide-silicon interface and aluminum oxide-silicon dioxide-silicon interface properties more thoroughly, MOS capacitors were fabricated by using a simpler process. Then these MOS capacitors were evaluated by C-V measurement.

### MOS Capacitor Fabrication

The MOS capacitors were fabricated on one ohm-cm ( $N_D = 5.3 \times 10^{15} \text{ cm}^{-3}$ ) n-type silicon wafers with (111) crystal orientation. Initially, the silicon wafers were cleaned using trichlorethylene, acetone, 4:1 buffered HF, and deionized water. Then the wafers were blown dry with nitrogen and baked at 150° C for five minutes.

For single-layer aluminum-oxide films, the silicon substrates were placed in the vacuum system. Aluminum-oxide films of about 2000 Å thickness were evaporated on the heated substrates (300° C). For the double-layer films, the silicon substrates were first oxidized in wet oxygen (0.4 cfh oxygen bubbled through 95° C deionized

water) at 1100° C for 30 seconds in the oxidation furnace to grow 500 Å of silicon dioxide; and then aluminum-oxide films of about 1500 Å thickness were evaporated on the thermally grown SiO<sub>2</sub> in the vacuum system. For single-layer silicon-dioxide films, the silicon substrates were oxidized in wet oxygen (0.4 cfh) at 1100° C for five and a half minutes in the oxidation furnace. The SiO<sub>2</sub> films of about 1500 Å thickness were grown. Before the substrates were put in the furnace, the furnace was flushed with steam for 30 minutes.

The copper ohmic contacts were plated on the back side of the wafers using a copper plating solution. A mercury probe was used as the gate electrode. The MOS capacitors were thus ready for testing.

#### MOS Capacitor Tests

The equipment for C-V measurement which were described in Chapter IV were used except a mercury (H<sub>g</sub>) probe was used in these tests. The bias-temperature tests were also performed.

For the capacitor with single-layer silicon dioxide as gate insulation, the measured and normalized C-V characteristics are shown in Figure 16. Curve 1 was measured when the silicon dioxide film had been grown. After the SiO<sub>2</sub> film was annealed in dry nitrogen at 1100° C for 15 minutes the C-V characteristic was measured and as shown

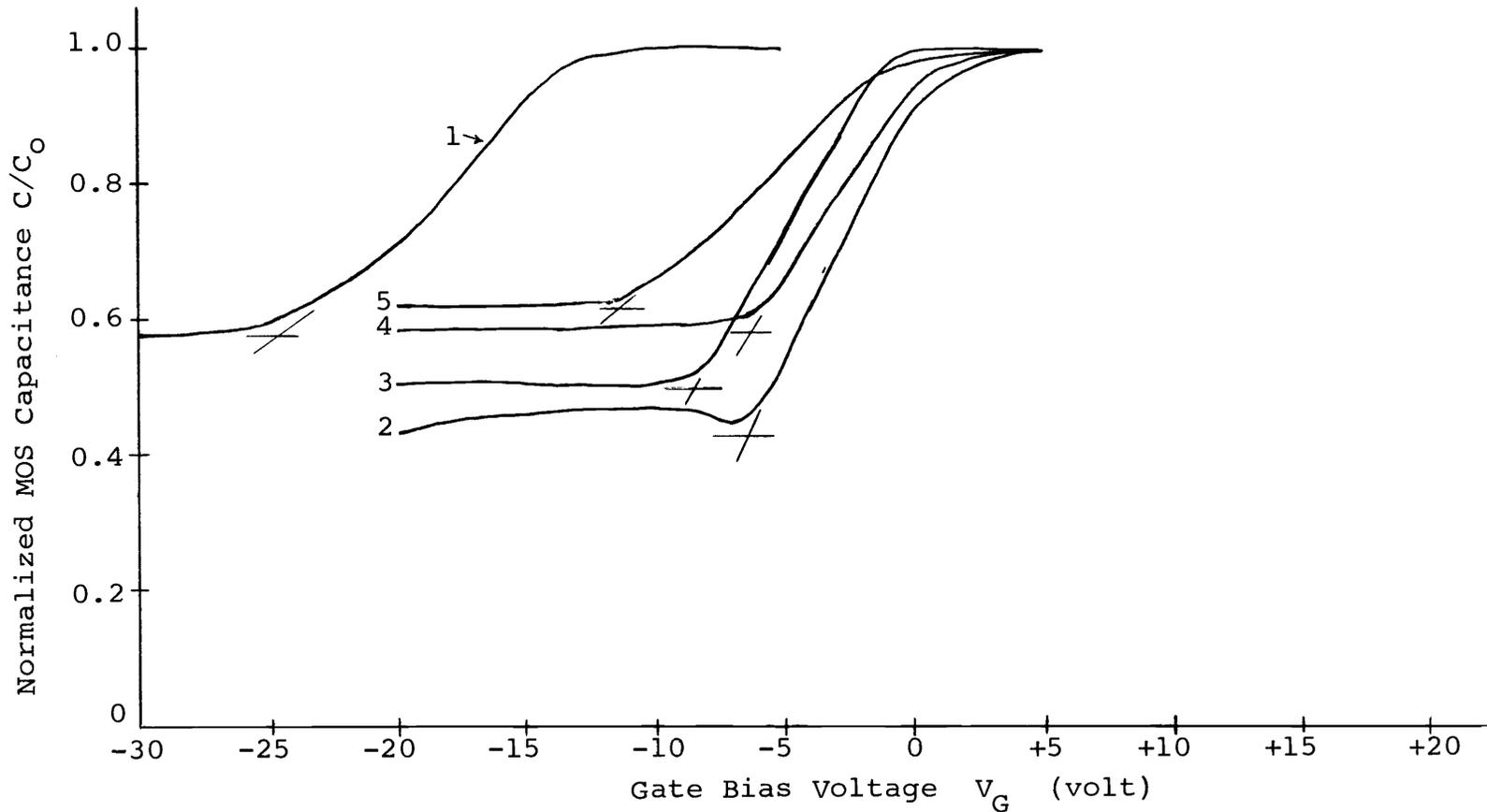


Figure 16. Single-layer silicon dioxide MOS capacitor C-V characteristics.

1. Initial curve.
2. After annealing in nitrogen at 1100° C for 15 minutes.
3. After holding at room temperature for 3000 hours.
4. After -20 V bias at 250° C for 10 minutes.
5. After +20 V bias at 250° C for 10 minutes.

by curve 2. The wafer was put in a plastic petri dish and held at room temperature for 3000 hours. Then the C-V characteristic was again measured and as shown by curve 3. Curve 4 was measured after -20 volts bias at 250° C for ten minutes. Curve 5 was measured after +20 volts bias at 250° C for ten minutes. The threshold voltages or turn-on voltages of these curves are listed in Table IV. In this figure the C-V curves show that for the silicon dioxide film the high temperature annealing resulted in shifting the flat-band voltage to the more positive direction. The bias-temperature tests show there had been some positive ionic charges in the SiO<sub>2</sub> film, which may be attributed to sodium ion contamination.

For the capacitor with single-layer aluminum oxide as a gate dielectric, the measured and normalized C-V characteristics are shown in Figure 17. Curve 1 was measured when aluminum oxide had been just deposited on the substrate. Then the Al<sub>2</sub>O<sub>3</sub> film was annealed in dry nitrogen at 1100° C for 15 minutes. After annealing, the C-V characteristic was measured and shown as curve 2. The wafer was then put in a plastic petri dish and held at room temperature for 3000 hours. The C-V characteristic was again measured and shown as curve 3. Curve 4 was measured after -20 volts bias at 250° C for ten minutes. After the +20 volts bias at 250° C was applied for ten minutes, the dielectric had conduction phenomena and

Table IV. Threshold voltages of the MOS capacitors with single-layer silicon dioxide (Figure 16), single-layer aluminum oxide (Figure 17), and double-layer oxide (Figures 18 and 19) as gate insulation.

Curve No.	Figure 16	Figure 17	Figure 18	Figure 19
1	-25 V	-1.5 V	-7.8 V	-3.7 V
2	-6.5 V	-2 V	-3.7 V	-3.4 V
3	-8.5 V	-4 V	-0.5 V	-4 V
4	-6.5 V	-4 V	-2.7 V	
5	-11.5 V			

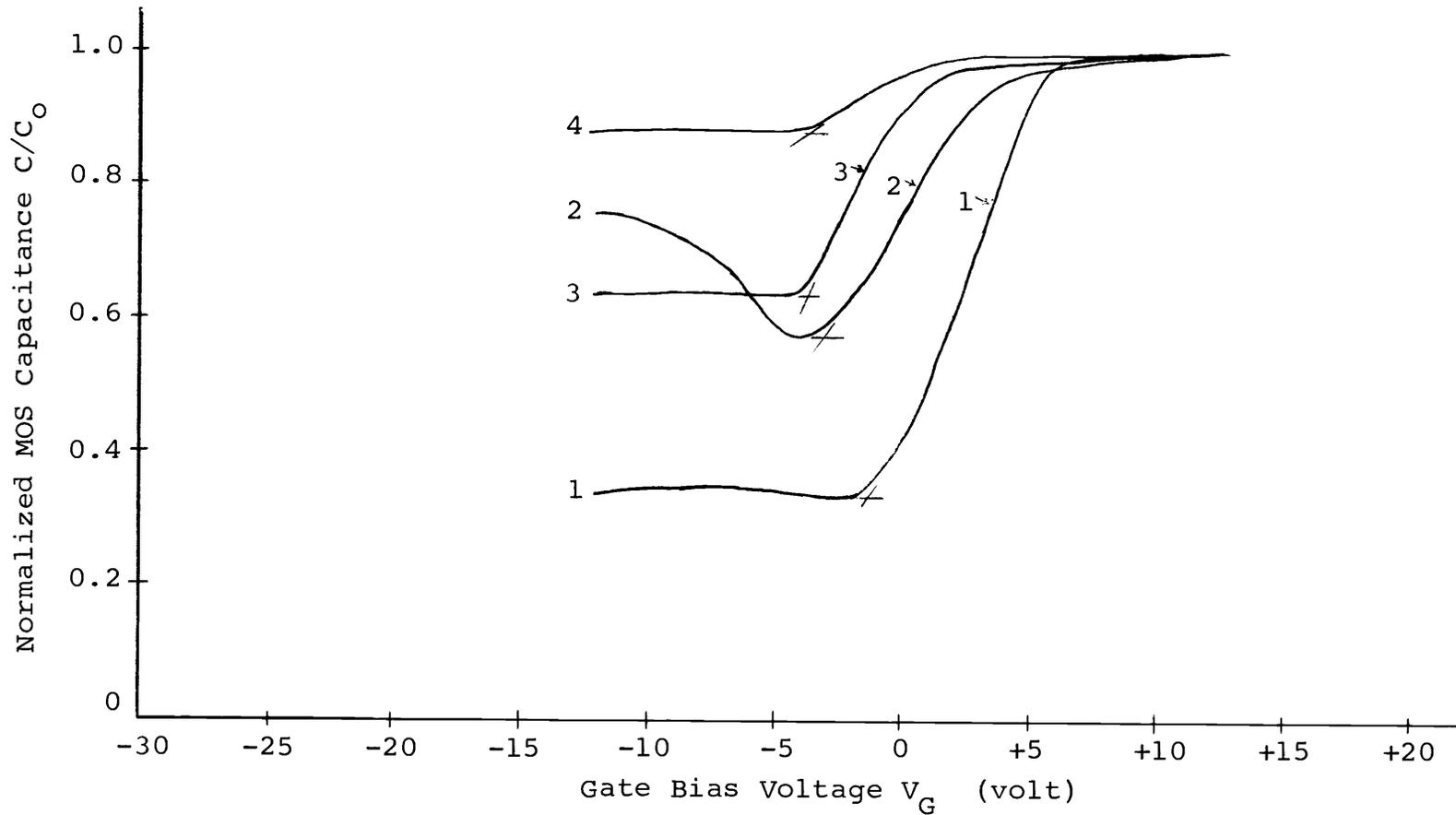


Figure 17. Single-layer aluminum oxide MOS capacitor C-V characteristics.

1. Initial curve.
2. After annealing in nitrogen at 1100° C for 15 minutes.
3. After holding at room temperature for 3000 hours.
4. After -20 V bias at 250° C for 10 minutes.

no C-V curve could be obtained. The threshold voltages or turn-on voltages of these curves are listed in Table IV. These curves show that the flat-band voltages shifted a few volts only. From curve 1 and curve 2 they show the high temperature annealing resulted in shifting the flat-band voltage to the more negative direction. It means that annealing in high temperature introduced some fast surface states (1).

For the capacitor with double-layer film as gate dielectric, the measured and normalized C-V characteristics are shown in Figures 18 and 19. In Figure 18, curve 1 was measured when the silicon dioxide had thermally grown. Then the  $\text{SiO}_2$  film was annealed in dry nitrogen at  $1100^\circ\text{C}$  for 15 minutes. After annealing, the C-V characteristic was measured and shown as curve 2. Aluminum oxide was then evaporated on the silicon-dioxide film. Curve 3 shows the C-V characteristic measured after the aluminum oxide had been deposited. Then the  $\text{Al}_2\text{O}_3$  film was annealed in dry nitrogen at  $1100^\circ\text{C}$  for 15 minutes. After annealing, the C-V characteristic was again measured and shown as curve 4. In Figure 19, curve 1 was measured after the wafer had been put in a plastic petri dish and held at room temperature for 3000 hours. Curve 2 was measured after -20 volts bias at  $250^\circ\text{C}$  for ten minutes. Curve 3 was measured after +20 volts bias at  $250^\circ\text{C}$  for ten minutes. The threshold voltages or turn-on voltages

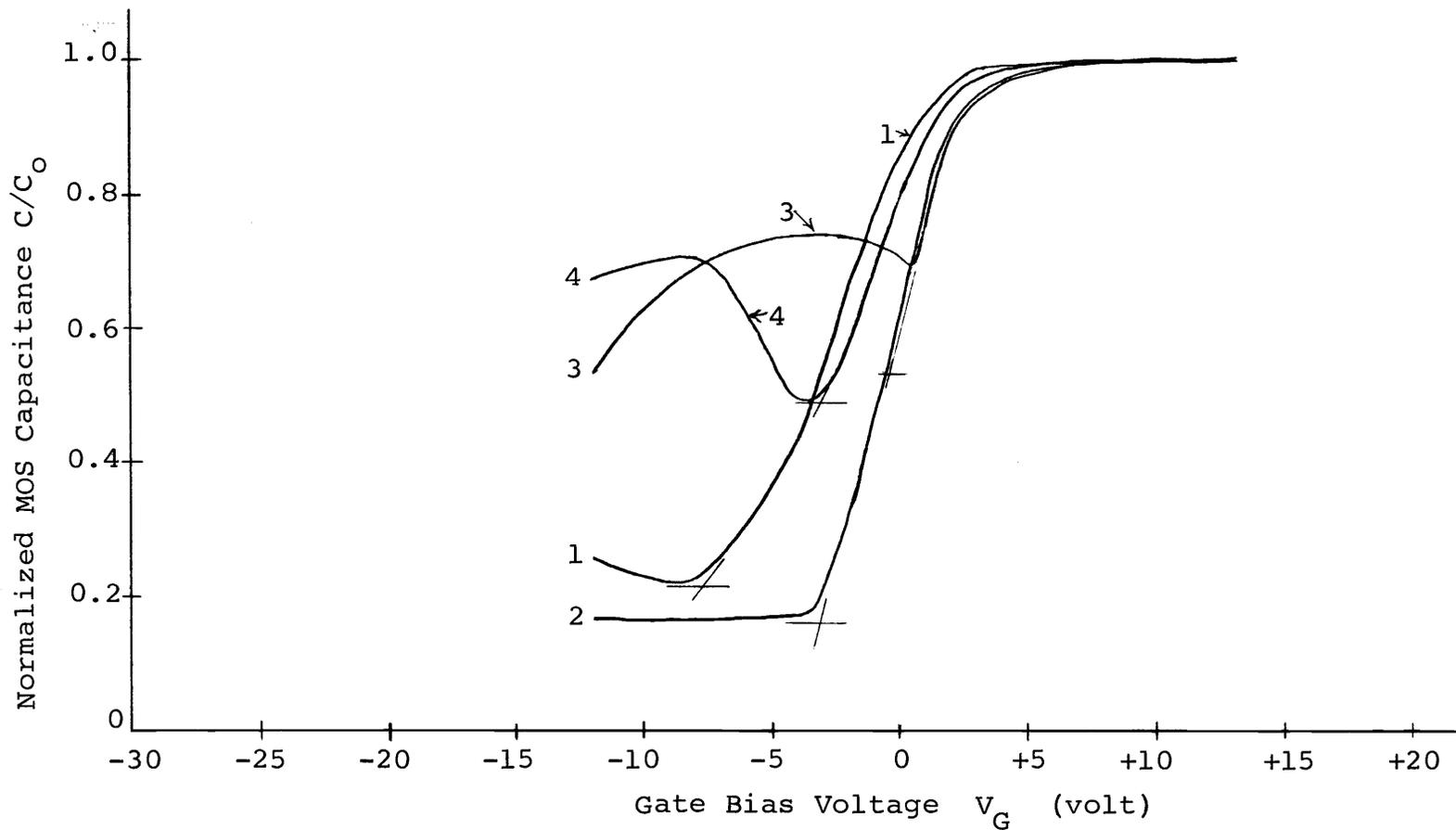


Figure 18. Silicon dioxide-aluminum oxide double-layer dielectric MOS capacitor C-V characteristics.

1. C-V characteristic of silicon dioxide capacitor.
2. After annealing in nitrogen at 1100° C for 15 minutes.
3. After aluminum oxide deposited on silicon dioxide.
4. After annealing in nitrogen at 1100° C for 15 minutes.

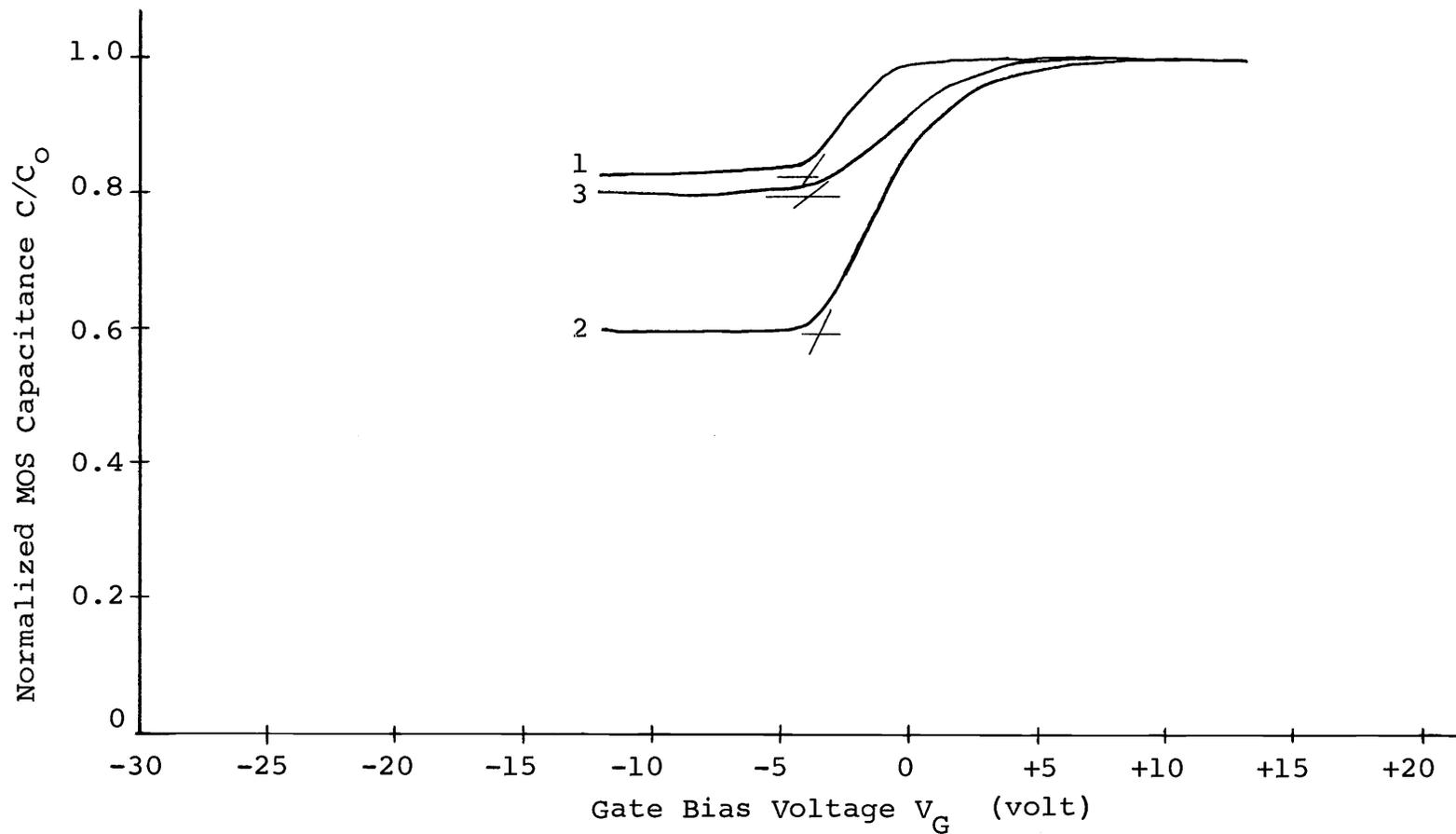


Figure 19. Silicon dioxide-aluminum oxide double-layer dielectric MOS capacitor C-V characteristics.

1. After holding at room temperature for 3000 hours.
2. After -20 V bias at 250° C for 10 minutes.
3. After +20 V bias at 250° C for 10 minutes.

of these curves are listed in Table IV. In the C-V curves of Figure 18, they also show that for aluminum-oxide films the high temperature annealing shifted the flat-band voltage to the more negative direction, while for silicon-dioxide films the high temperature annealing shifted the flat-band voltage to the more positive direction. In Figure 19, these curves show that the double-layer film had very stable characteristics.

In these tests, the MOS capacitor with double-layer films as gate insulation revealed the least flat-band voltage drift after being stored at room temperature for a long period (3000 hours), and in the bias-temperature tests it also revealed the most stable characteristics. It is possible that the drifting impurities were trapped at the oxide-oxide interface and must overcome a substantial barrier before they could penetrate into the underlying silicon dioxide. Thus the ions could not easily penetrate the oxide-oxide interface in either forward or the reverse direction (1). The MOS capacitor with single-layer aluminum oxide as gate insulation revealed lower threshold voltage and less contamination than capacitor with single-layer silicon dioxide as gate insulation. Aluminum-oxide film is good barrier to ionic migration. But after the bias-temperature test, the aluminum-oxide film had a tendency to conduct. To use double-layer films for the gate dielectrics of the MOS devices is better than

to use single-layer silicon dioxide or single-layer aluminum oxide alone.

In these tests, all of the MOS capacitors exhibited less contamination than those discussed in Chapter IV. In the previous tests, the MOS capacitors were fabricated by a more complicated process. Thus the main contaminants, sodium and other alkali ions, might come from several sources, including photoresist, cleaning agent, furnace wall, or impure metallization.

## VII. CONCLUSIONS

The characteristics of MOS devices are very sensitive to their gate dielectric properties. The vacuum deposited aluminum-oxide films had good adhesion to the silicon substrates, few pinholes observable, high breakdown field strength (about  $6.2 \times 10^6$  V/cm), and higher dielectric constant (about 8.3) than silicon dioxide. The films can easily be etched off by using hot aluminum etch solution before annealing. It appears that suitable aluminum-oxide films can be obtained by vacuum deposition. Thus it is feasible and advantageous to use the e-Gun deposited aluminum-oxide films to fabricate MOS devices.

For the MOS capacitors fabricated by a complicated process, the capacitors using single-layer aluminum-oxide films and double-layer silicon dioxide-aluminum oxide films as gate insulation revealed less mobile ion contamination than the capacitors using single-layer silicon-dioxide films as gate insulation. Single-layer aluminum oxide and double-layer films were more impervious to the diffusion of impurities, but single-layer aluminum-oxide films had a tendency to conduct. For the MOS capacitors fabricated both by a complicated or a simpler process, the capacitors using double-layer films as gate insulation exhibited the most stable characteristics under various tests.

The fabricated MOS transistors always revealed high

ionic contamination in their gate dielectrics. These contaminants, sodium and other alkali ions, might come from photoresist, cleaning agent, furnace wall, or metallization. The MOS transistors with single-layer aluminum-oxide films or double-layer films as gate insulation had high effective hole mobilities and they had lower threshold voltages and higher transconductances than the transistors with single-layer silicon-dioxide films as gate insulation. The MOS transistors using double-layer films as gate insulation also revealed the most stable characteristics. Thus double-layer films are better than single-layer silicon-dioxide films or single-layer aluminum-oxide films for fabricating MOS devices. The MOS transistors with single-layer aluminum oxide as gate insulation revealed very unstable characteristics. After gate voltages were applied for a while, they sometimes even had positive threshold voltages (p-channel MOS transistors). Thus the MOS transistors with single-layer aluminum oxide as gate insulation are not suitable for general use.

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