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ABSTRACT

Reliability of sub-micron analog circuits is directly related to impact ionization and the subsequent changes in threshold voltage and drain current of n-MOSFET devices. This thesis presents theory of the hot-electron effects on the device characteristics and circuit performance, explores several approaches to improve performance at both the device and circuit level, and finally shows a new composite n-MOSFET device which significantly suppresses substrate current - an indication of hot-electron degradation. By using the composite device in the output gain stage of a CMOS differential amplifier with 1μm technology, the normalized substrate current of the n-channel device is reduced by eight orders of magnitude for a sloping input waveform. The reduction in device substrate current is achieved at the cost of increased area and reduced frequency response.

Replacing conventional n-channel devices with composite n-MOSFETs provides a simple way to improve device and circuit reliability without modification of the device structure and/or fabrication process.

Reliability and Hot-Electron Effects in Analog and Mixed-Mode Circuits

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Reliability and Hot-Electron Effects in Analog and Mixed-Mode Circuits

1. Introduction

Higher density and faster propagation speed have become a trend for the future development of VLSI technology. Figure 1 shows the trend in CMOS technology in terms of reduction in both device channel length and gate oxide thickness. It was first published in 1991 International Device Reliability Symposium. Many of the leading edge commercial products are using 0.8μm technology in the field of digital circuits and 1μm devices in the field of analog circuits. Technology using 0.6μm devices is ready to be implemented in the digital circuit. Intel's new generation Pentium CPU chip is using 0.6μm technology. Technology of 0.3μm devices will be implemented in 1995; and further development is under way.

As we further reduce the channel length and the oxide thickness, a high electric field between drain and source, and between drain and substrate can be introduced in the channel resulting from the reduction in the device's physical dimensions without decreasing the power supply voltage. The high electric field is the main cause of impact ionization.

The reliability of sub-micron analog and mixed-mode circuits is directly related to impact ionization and the subsequent changes in threshold voltage and drain current of n-MOSFETs. The hot-electron effects resulting from high drain electric fields cause the device degradation and thus often lead to the circuit's failure. The device degradation is monitored by measuring the substrate currents. Long channel devices generally have low substrate current. For devices with

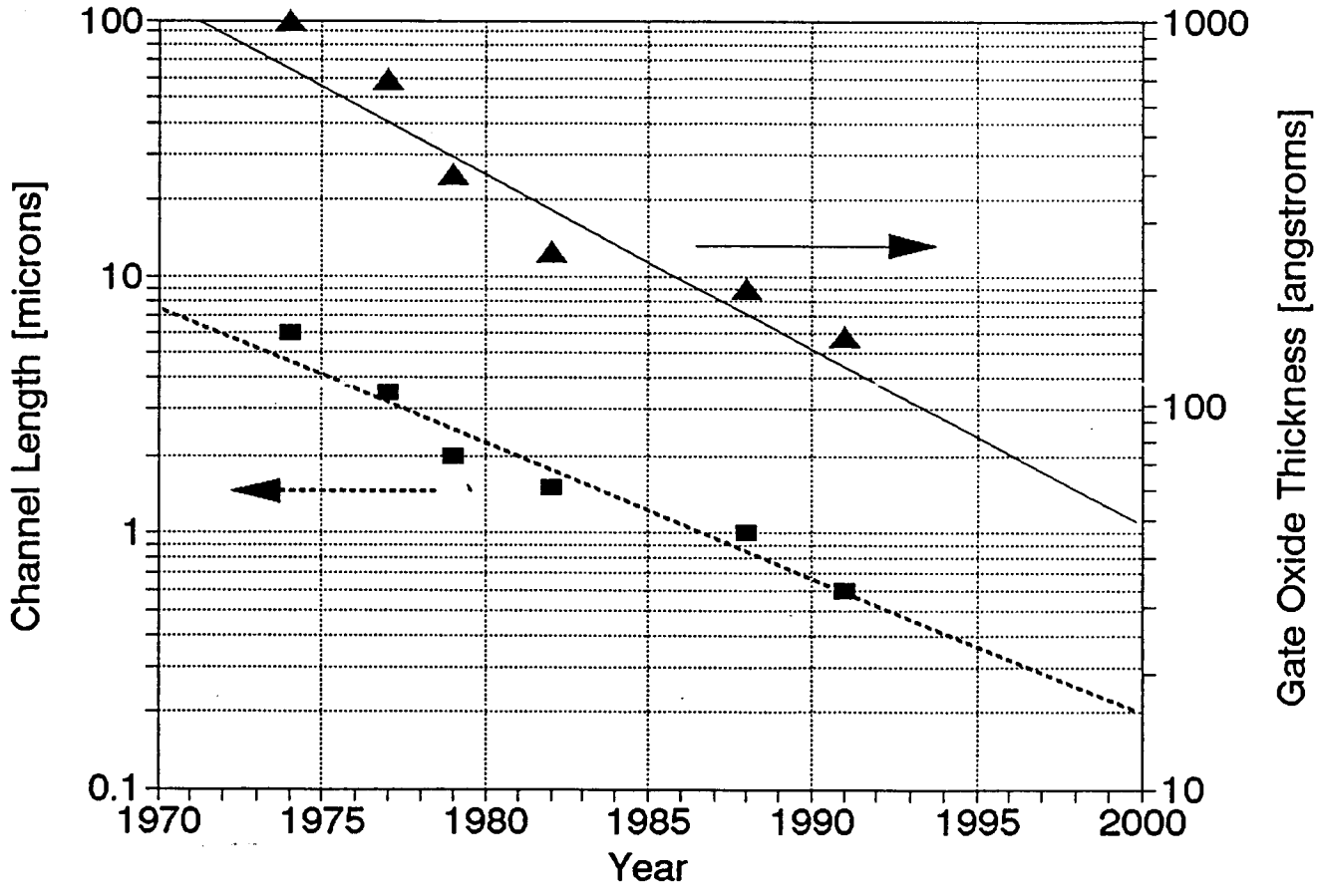


Figure 1 CMOS Technology Trend

channel length longer than 5μm, hot-electron degradation is not the concern because of the low electric field between the drain and the source.

In this study, the primary subject is the reliability and matching consideration of the 1μm n-substrate metal-oxide semiconductor field effect transistor, MOSFET, in analog and mixed mode circuits.

In chapter 2, background knowledge of hot electron degradation is reviewed. Several mechanisms responsible for degradation are studied. The relationship between the substrate current and drain electric field is established, and variations of several device parameters, such as threshold voltage, transconductance, and drain current under hot-electron stress are observed.

The effect of hot electron degradation in circuits is studied in chapter 3. Many analog and mixed-mode circuits require matching in terms of device parameters and physical dimensions in order to operate properly. Most problems caused by degradation exist in circuits where matching is required, such as differential amplifiers, and where high voltages appear across drain and source of n-type MOSFET, such as output drivers. The amount of circuit performance degradation is determined by comparing the performance of a particular circuit using fresh devices with the one using after-stress devices. The professional version of the simulator Pspice is employed in this part of the study, and the 1μm technology device Pspice parameters are provided by Hewlett Packard.

Chapter 4 covers the improvement from the past to present on both device processing and circuit designing levels. A composite n-type MOSFET is the result of our work. It improves the device lifetime under operating conditions by about 8 orders of magnitude.

The implication of hot-electron degradation in analog and mixed-mode circuits is discussed in chapter 5. There are three different types of circuit selected

2. Device Reliability

2.1 Hot-Electron Injection

In the VLSI technology, long term instability of device characteristics due to hot-electron injection has become a major problem as devices scaling down from the long channel devices of a few years ago to sub-micron short channel MOSFETs. The degree of degradation strongly depends on the VLSI technology involving process quality, device structure, and circuit-system complexity.

Several hot-electron injection mechanisms have been proposed for hot-electron-carrier injection based on both gate current and substrate current generation. They are shown in Figure 2.1.

a) Channel Hot-Electron Injection (CHE) [1]. The injection is caused by some electrons gaining significant energy and overcoming the Si-SiO_2 barrier without losing energy by colliding into other particles in the channel, as explained by the "lucky electrons" model.

This mechanism is dominant when the voltage across the drain and source is the same as the one across the gate and source. The injected electrons create a significant gate current. The model for the current due to CHE is shown below [2] [3]:

$$I_g \propto \exp(-\frac{\Phi_e}{E_m \lambda}) \qquad (2.1)$$

where

ϕ_e is the electron energy barrier at the Si-SiO_2 interface;

E_m is the channel electric field at the drain end ;

λ is the scattering mean free path of hot electrons.

b) Drain Avalanche Hot-Carrier (DAHC) Injection. This injection is caused by impact ionization of channel current near the drain. As electrons approach the drain, they gain a significant amount of energy so that the avalanche multiplication of holes and electrons occurs in the depletion region near the drain. At room temperature, both holes and hot-electrons are injected into the gate oxide as well as into the substrate, which causes the most severe degradation on the device [4]. This mechanism is dominant at $V_{gs} = \frac{1}{2} V_{ds}$.

Hot electrons and holes generated by impact ionization can be monitored in terms of the substrate current. Then the gate current due to DAHC can be written as below [5]:

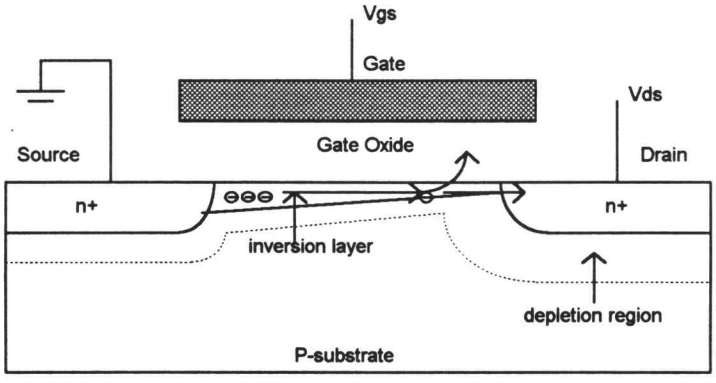
$$I_{ge} = \xi_e (E_x, E_y) I_{sub} \qquad \text{for electrons} \qquad (2.2)$$

$$I_{gh} = \xi_h (E_x, E_y) I_{sub} \qquad \text{for holes} \qquad (2.3)$$

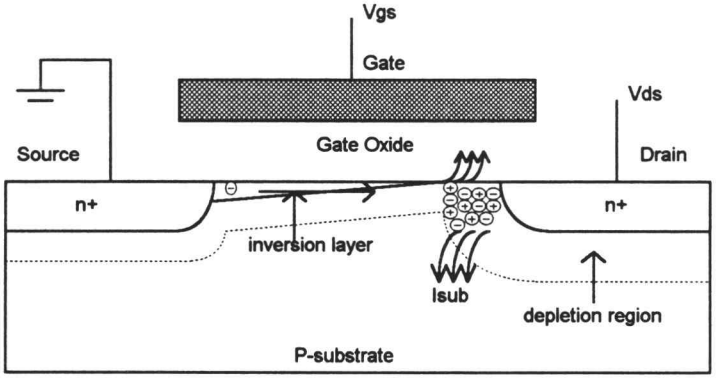
where $\xi (E_x, E_y)$ is the intrinsic injection ratio.

c) Substrate Hot-Electron (SHE) Injection. In this case, hot-electrons are thermally, or optically generated or injected from the forward-biased p-n junction into the substrate high field region.

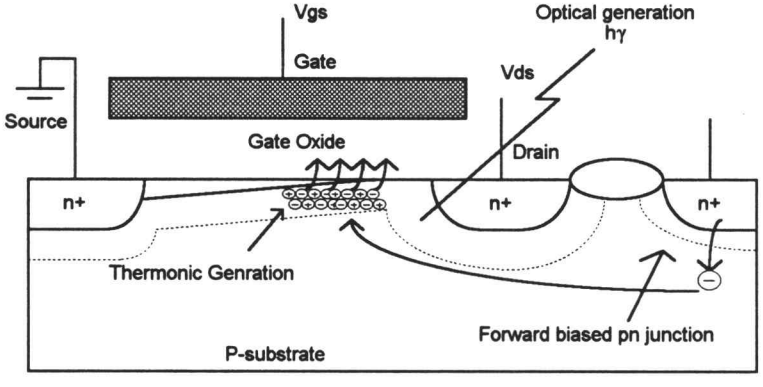
For most sub-micron devices, all the factors described above may be taken into account at the same time, depending upon various conditions.



a) Channel Hot-Electron Injection Model



b) Drain Avalanche Hot-Electron Injection Mechanism



c) Substrate Hot-Electron Injection Mechanism

Figure 2.1 Schematic Diagrams for Hot-Electron Injection Mechanisms

2.2 Substrate Current

The easy-to-measure substrate current is a key factor to determine the population of hot-electron generated in the drain high electric field region, which leads to device degradation.

In a short n-channel MOSFET, the impact ionization generated holes are responsible for the substrate current; while the hot electrons injected into the gate oxide cause the flow of gate current. The electric field at the drain end of the channel is sometimes so high that it induces significant impact ionization and avalanche multiplication current in the drain depletion region.

The relationship between the substrate current and drain electric field is shown below [6]:

$$I_{sub} = C_1 I_d e^{-\beta i/Em} \tag{2.4}$$

C_1 is a very weak function of E_m and device parameters; β_i is the distance that an electron must travel in the electric field in order to gain energy, β_i is a function of energy and I_d is the drain current [6].

$$\beta_i = \frac{\varphi_i}{q\lambda} \tag{2.5}$$

where φ_i is the minimum energy that a hot-electron must have in order to create an impact ionization.

This model shows that the substrate current has an exponential dependence on the impact ionization coefficient $1/E_m$.

Substituting equation (2.5) into (2.4), we get the substrate current due to hot electrons possess higher energy than φ_i [7].

Similar relationships hold for the gate current.

$$I_g = C_2 I_d \, e^{\frac{-\varphi_b}{q\lambda E_m}} \tag{2.6}$$

where φ_b is the barrier energy at the Si-SiO_2 interface, and $C_2 \cong 2\times10^{-3}$ for Vg>Vd [2].

Figure 2.2 shows a normalized substrate current curve for a 50μm width n-channel device. The substrate currents start at a very low value for small gate to source voltage, peak around 2V, and gradually decrease as the gate-source voltage increases. A model proposed by T.Y. Chan in 1984 provides a simple and accurate way of predicting the substrate current of a device [9].

$$I_{sub} = \frac{\alpha}{A\beta} E_m I_D \exp[-\frac{\beta}{E_m}] \tag{2.7}$$

2.3 Change in Device Characteristics

MOSFET hot-electron degradation shows up in three major areas: shift in threshold voltage [10], shift in transconductance in the linear region and shift in the transconductance in the saturation region [11].

Figure 2.3 shows the changes in threshold voltage, $V_{th,}$ over a one day time period for both n and p MOSFETs. The threshold voltage can be measured from the I_{ds} versus V_{gs} curve at V_{ds}=0.1V. First, the transconductance is measured. From the g_m versus V_{gs} curve, we can determine V_{gs} where g_m is the maximum. Then, we select five points surrounding the determined V_{gs} value, and draw a line connecting these five points. The interception of the line and the V_{gs} axis is the threshold voltage. The width and length ratio for both devices are 50:1, and the oxide thickness is 200nm. The stressing conditions are:

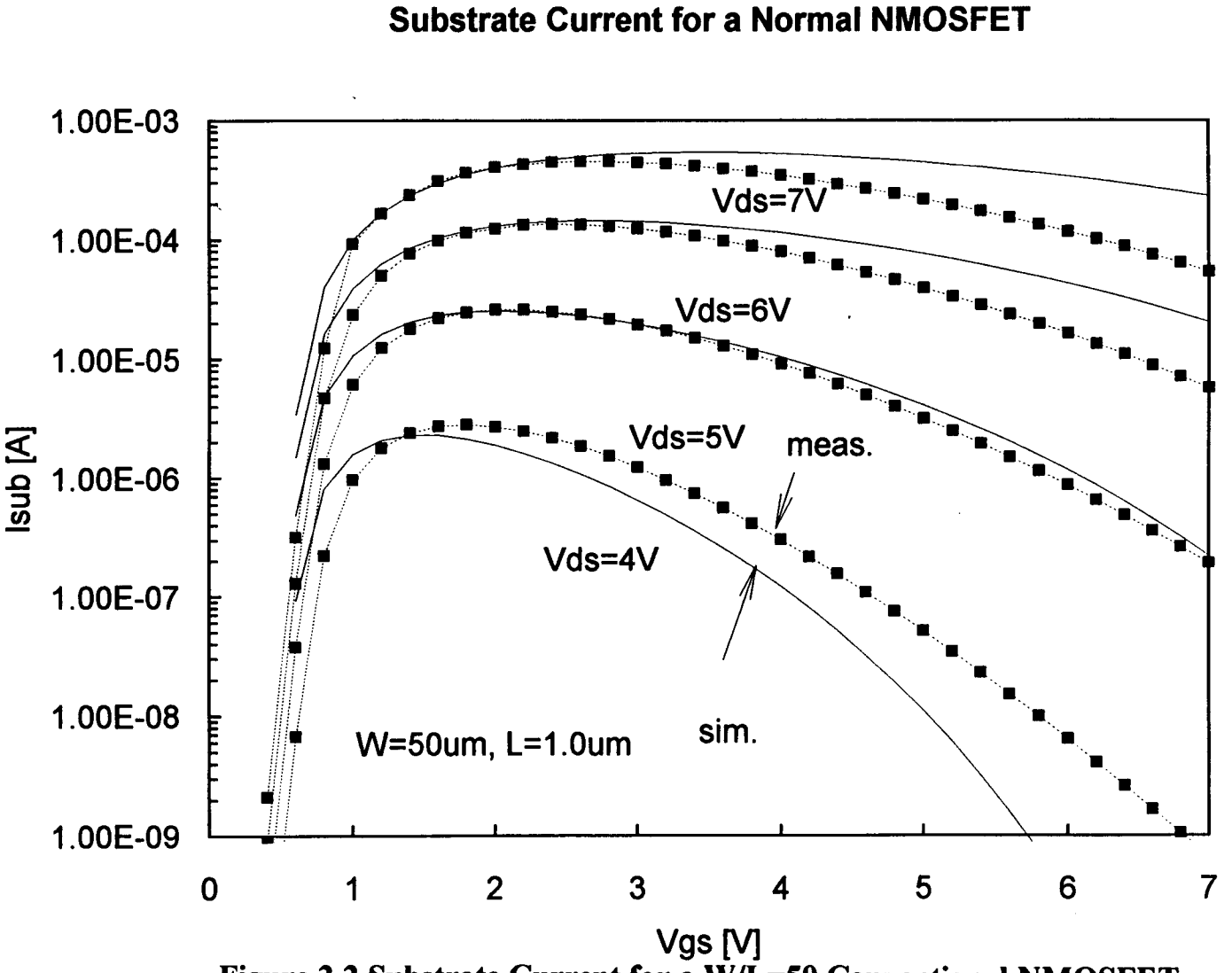


Figure 2.2 Substrate Current for a W/L=50 Conventional NMOSFET

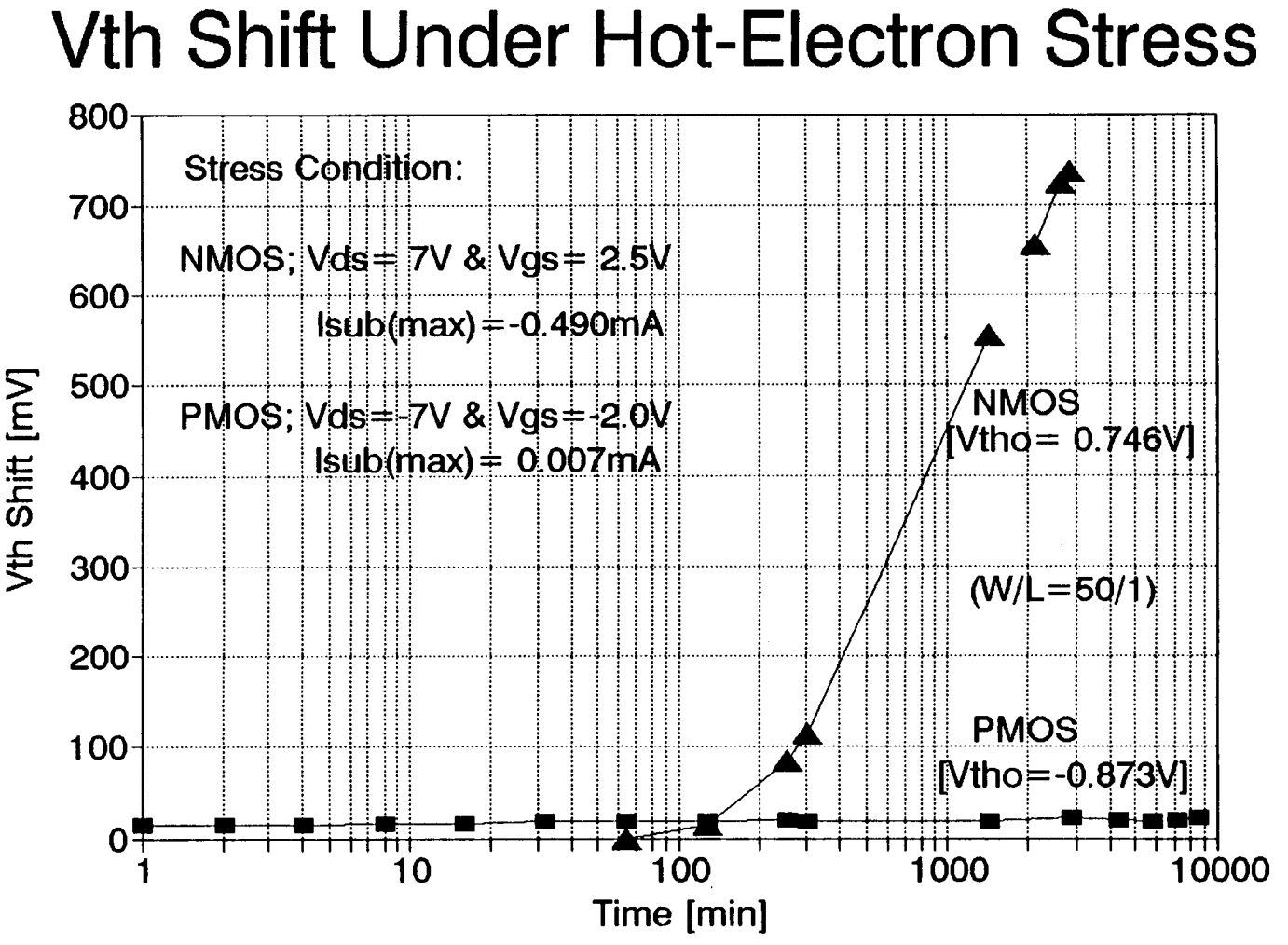


Figure 2.3 NMOSFET Threshold Voltage Shift under Hot-Electron Stress

NMOSFET	PMOSFET
V_{ds} = 7V	V_{ds} = 7V
V_{gs} = 2.5V	V_{gs} = 2V

After one day stress (1440 minutes), the n-MOSFET has shifted nearly 800mV, while the p-MOSFET has no observable shifting.

The time variance of I_{ds}(sat) is shown in Figure 2.4. I_{ds}(sat) is measured at V_{ds} = 6.5V and V_{gs} = 5.5V. The stressing conditions are listed as below:

	n-MOSFET	p-MOSFET
V_{ds} (Volts)	7	-7
V_{gs} (Volts)	2.5	-2
I_{sub}(max) (mA)	-0.49	0.007

After one day stress, I_{ds}(sat) of n-MOSFET has changed 11%, while p-MOSFET only has a 3% shift. This current is measured in the saturation region since in digital and mixed-mode applications, the device is often operating in either "on" or "off". While it is "on", it is eventually operating in the saturation region. Therefore any change in drain current in this region due to hot-electron effect will certainly affect the circuit performance.

The drain conductance is another significant parameter relating to analog and digital circuit performance. The gain of a single stage amplifier is inversely proportional to g_d. As g_d varies, so does the gain of the amplifier. In digital

Idss Shift Under Hot-Electron Stress

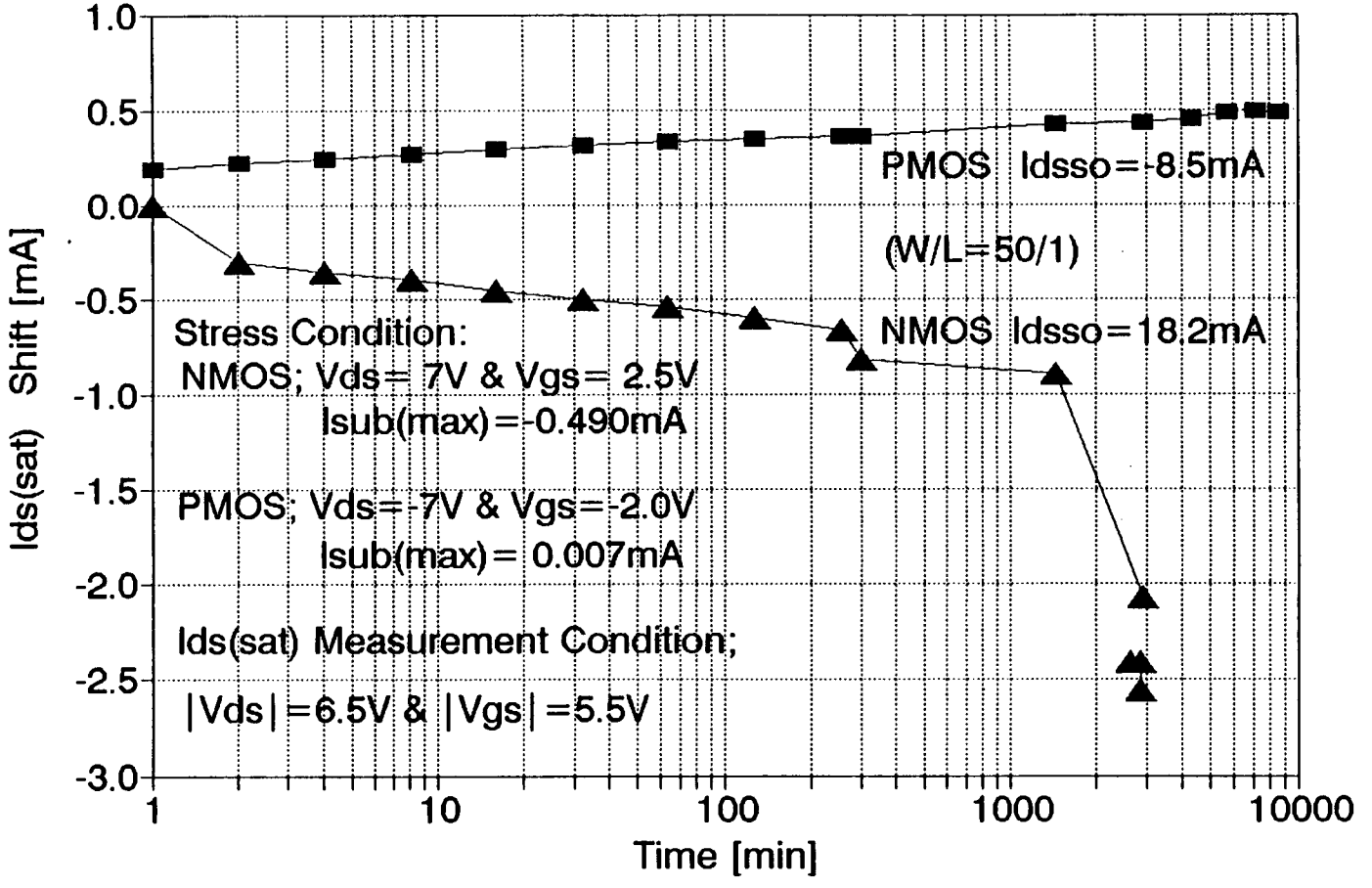


Figure 2.4 NMOSFET Drain Current in Saturation Region under Hot-Electron Stress

circuits, n-MOSFET provides a path to sink the current when it is turned on. However, the path is not a short circuit. The drain resistance, or inverse of drain conductance, g_d, is present in the device. Any shifting in drain conductance will have a similar effect on digital circuit as drain current does in terms of speed and data holding time.

To determine the drain conductance variation, we stress an n-MOSFET with width of 50μm under dc conditions at V_{gs}=2.5V, and V_{ds}=7.0V for one day. Then we measure g_d at V_{ds}=V_{gs}=5V condition. Figure 2.5 shows the change of drain conductance under dc stress. From the graph, we observe that there is a greater change for the short channel device than the long channel one. For the 1μm device, g_d is nearly 3 times larger after stressing.

After studying the physical mechanisms of hot-electron injection, we focus the next chapter on examining how the change of device parameters affects the circuit performance.

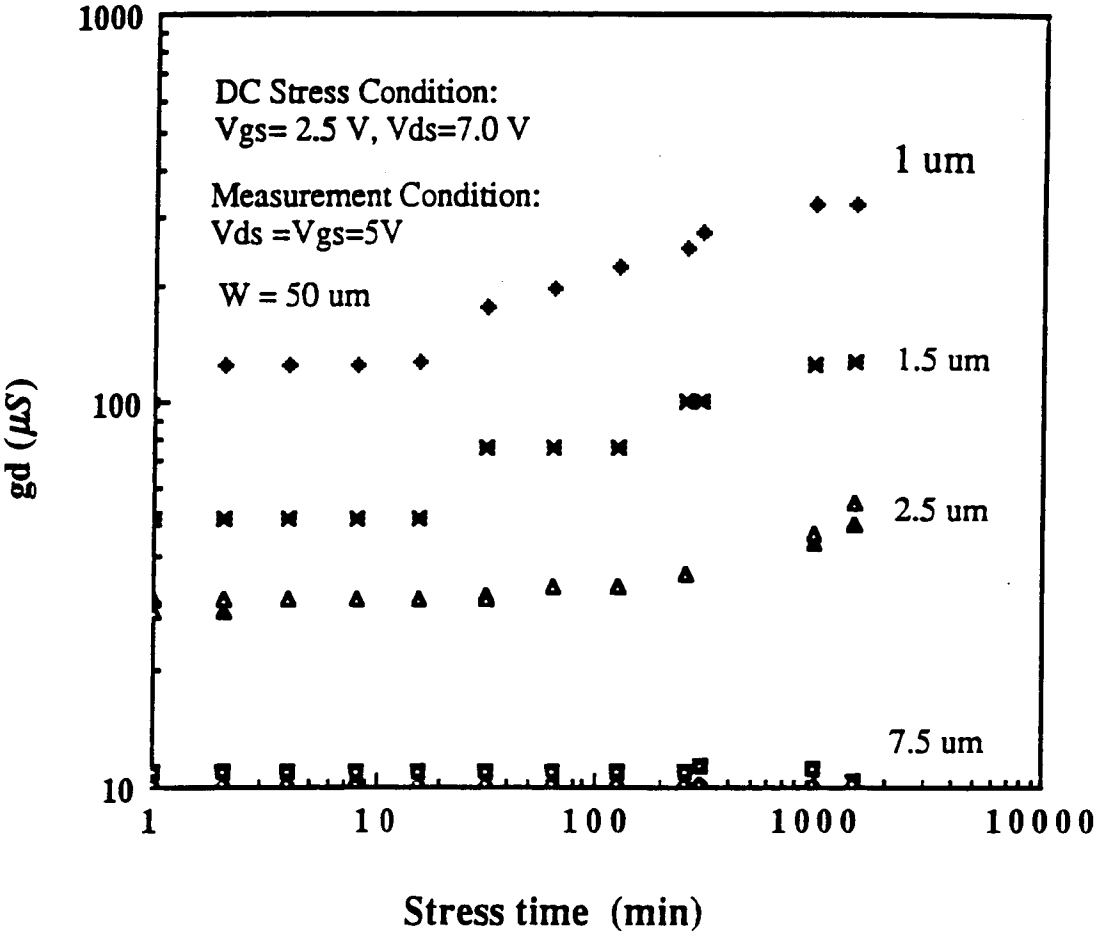


Figure 2.5 Drain Conductance Changes under DC Stress

3. Effects of Device Reliability in Analog and Mixed-Mode Circuits

3.1 Lifetime Definition

The lifetime of circuits is defined as the tolerance of the practical circuits to the variations in DC output voltages and the changes in gain. It defines the duration of time for a circuit operating under normal conditions until the change of some parameters causes the circuit to fail under a pre-defined failure condition. To determine the life of a device due to hot electron degradation, the normalized substrate current has been identified as an indicator. Then the lifetime can be expressed as [2]

$$\tau \propto (\frac{I_{sub}}{W})^{-2.9} \tag{3.1}$$

where W is the device width.

3.2 Effects of Drain Current Shift on Amplifier Circuits

In order to explore the effects of device parameter changes on the circuit performance, a basic differential amplifier is simulated using the Pspice circuit simulation program. As shown in Figure 3.1

A differential amplifier is one of the fundamental circuits in both the digital and analog circuit families. A Mosis level one model is used in the simulation for simplicity. To examine the effect of the drain current, I_{ds}, on the circuit performance, we must vary I_{ds}. Then results of the circuit simulation will show the change of performance. Unfortunately, there is no I_{ds} parameter in the level one device parameter which one can modify. Therefore, other parameters must be modified in order to examine the effects of the change in Ids. After looking into

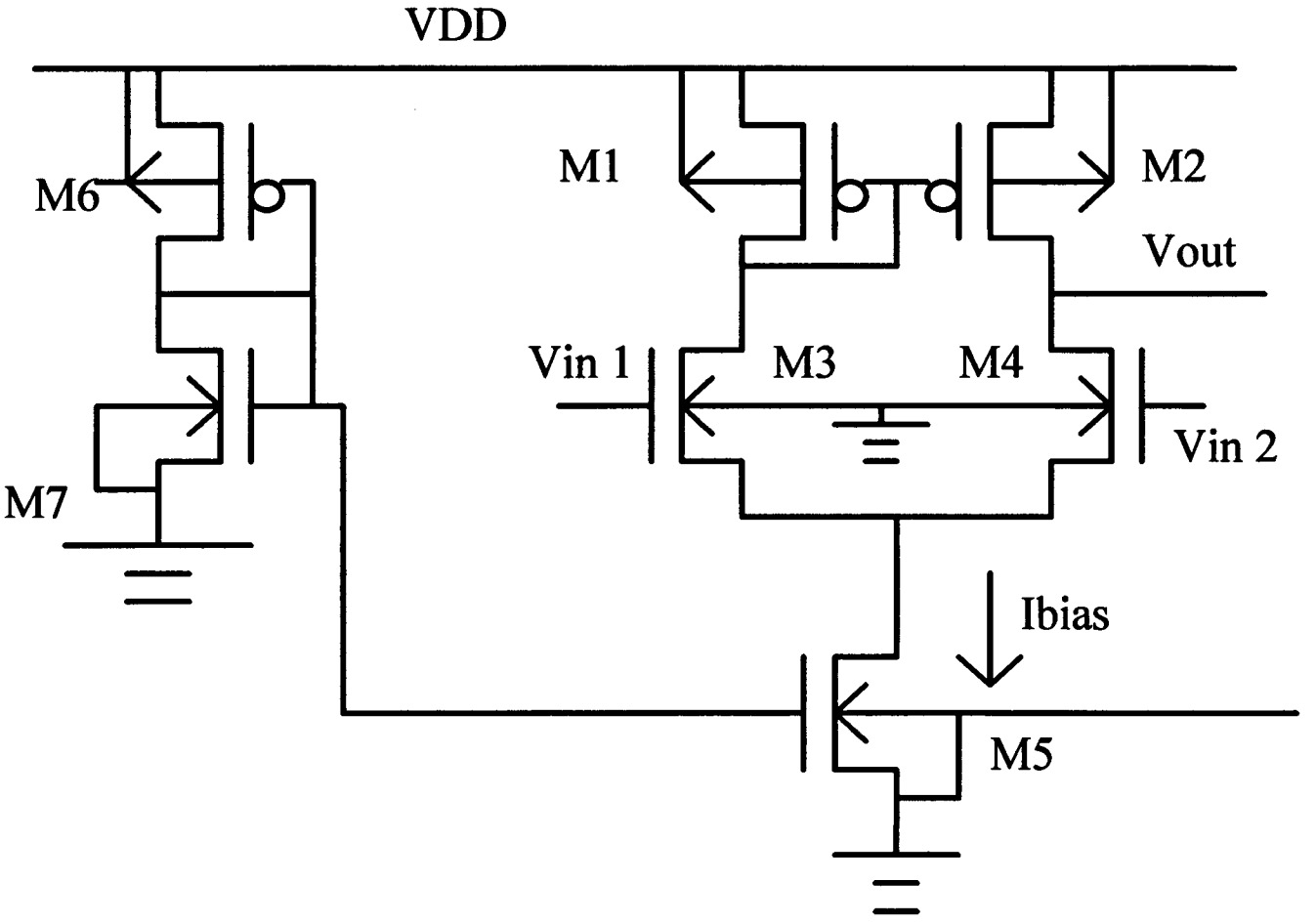


Figure 3.1 A Simple Differential Amplifier

the level one model equations, we find the relationship between V_{th} and I_{ds}, given below:

$$I_{ds} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs}-V_t)^2(1+\lambda V_{ds}) \tag{3.2}$$

In the case of V_{ds}= V_{gs} = 5V, and I_{dss} = I_{ds}, the change of I_{ds} can be related to the change of V_{th} as below:

$$\frac{\Delta I_{dss}}{I_{dss}} \propto \frac{2\Delta V_t}{(V_{gs}-V_t)} \tag{3.3}$$

Knowing the relationship between the change of I_{ds} and the change of the threshold voltage, we can easily vary the value of the threshold voltage in the level one Mosis device model. For the device size of 50μm/1μm, width/length, 2.5% I_{dss} variation reflects a 50mV change in threshold voltage.

$$\frac{\Delta I_{ds}}{I_{ds}} = -\frac{2\Delta V_t}{(V_{gd}-V_t)} \tag{3.4}$$

The lifetime for the drain current is now defined as

$$\frac{\Delta I_{ds}}{I_{ds}} = 2.5\% \qquad where \quad I_{dss} = I_{ds} \tag{3.5}$$

From the simulation of a basic differential amplifier, we find that a 50mV change in threshold voltage of the input NMOSFET, M3, will result in a 1V output DC voltage level shift at the drain. The device model file is listed in Appendix A.

After knowing the dc bias condition, we calculate that the product of g_m/g_d is about 20. Therefore, for a 50mV variation in the input, there will be a 1 volt swing at the output. In the analog circuits, 1 voltage of dc bias shift could cause circuit failure since the bias condition is extremely important in analog circuits.

3.3 Effects of Drain Conductance Shift on Mixed-Mode Circuits

The variation of transconductance of a device has a significant effect on the gain of the amplifier. First of all, the change of g_{ds} will change the gain of the circuit, since the total gain of an amplifier is directly related to the product of g_m and $1/g_{ds}$.

$$Gain \propto g_m r_o = \frac{g_m}{g_d} \tag{3.6}$$

Second of all, g_{ds} variation affects the dc bias condition of the circuit, which is extremely important for analog circuits. Without proper biasing, an amplifier will have no gain, let alone amplify signals.

Again, a differential amplifier is employed to examine the effects of g_{ds} on the gain of the circuit. Mosis level one model is sufficient for this purpose. Lambda is varied to emulate the variation of g_{ds}. The relationship between lambda and g_{ds} is shown below:

$$I_{ds} = \frac{\mu C_{ox}}{2} \times \frac{W}{L} (V_{gs} - V_t)^2 (1 + \lambda V_{ds}) \tag{3.7}$$

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} = \frac{\mu C_{ox}}{2} \times \frac{W}{L} (V_{gs} - V_t)^2 \lambda \tag{3.8}$$

From equation 3.8, one realizes that the drain conductance is proportional to λ. For the circuit shown in Figure 3.2, a 5% variation in lambda has significantly affected both the dc bias and the gain of the circuit. The nominal gain for this particular amplifier is 4500 and the output dc voltage is near zero, Figure 3.3. However, a 5% variation of lambda causes the gain to fumble down to 100 while shifting the output dc bias voltage to 4V. In other words, the amplifier is no longer functioning properly. As the lambda of M2 increases, the voltage at node 6 shifts down to 2.50V, which drives M8 into the linear region. The output voltage shifts from zero to near 4V. In the case of decreasing lambda by 5%, the voltage at the drain of M2 moves up to 2.77V, which moves M9 into linear region. It results in a negative 3.7V voltage at the output node. In both cases, the gain of the amplifier is dramatically reduced.

In conclusion, a 5% change in drain conductance can affect the gain of the amplifier dramatically. Mixed-mode and digital circuits have much better drain conductance tolerance since they are insensitive to dc biasing conditions.

3.4 Process Variations

During the process, it is impossible to make the parameters of all device exactly the same way. There is always some uncertainty and unknown sources of error involved in the processing and manufacturing areas. Therefore, the processing variation of the device parameters is unavoidable. In CMOS processes, there are two key device parameters often being monitored, threshold voltage, V_{th}, and drain and source current, I_{ds}. Threshold voltage is a function of gate oxide thickness. As the gate oxide get thinner, it is very difficult to acquire the same amount of oxide thickness throughout the wafer due to the temperature gradient

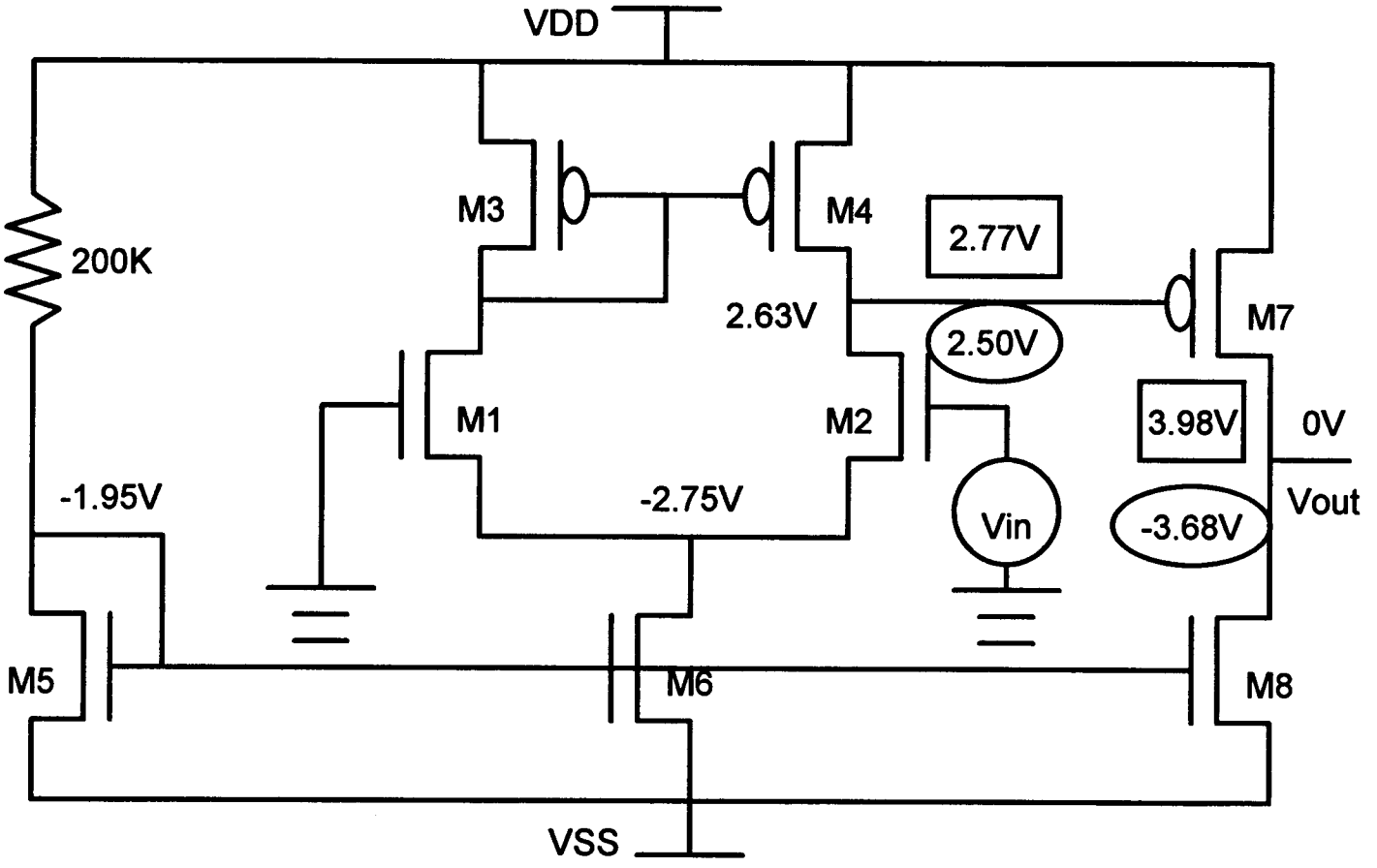


Figure 3.2 A Simple Differential Amplifier with an Output Stage

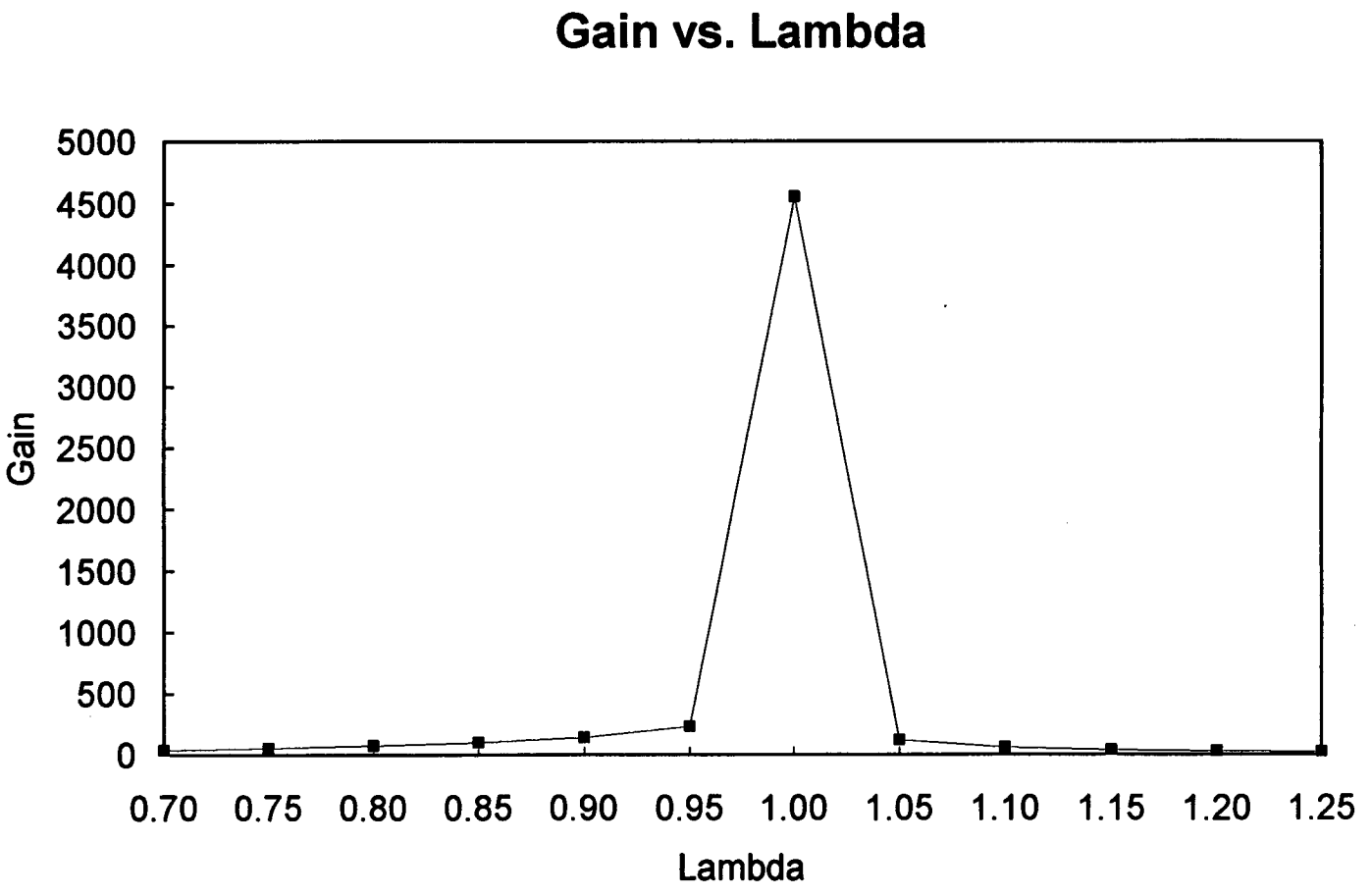


Figure 3.3 Gain vs Lambda Variation in a Differential Amplifier

and the direction of heat flow. Also, during production, there is a threshold adjustment step which employs ion implantation techniques to adjust the threshold voltage to a desired value. In this process, a thin oxide layer is used as a mask to selectively allow ions to be implanted into certain areas. An unevenly distributed oxide layer will affect the ion implantation process, and thus causes large threshold voltage variation.

Device size varies due to over or under-etching. The variation of geometry may not effect the circuit performance for large devices such as 50μm in length and/or width. However, it certainly causes problems in circuits composed of small devices. For example, a 0.2μm variation in channel length may not mean much (0.4%) in a 50μm device, yet contributes to 20% variation in a 1μm device. This is called the short channel effect. Short-channel effects are another cause of parameter variations.

Drain current in both the linear and saturation regions is an important parameter in monitoring process variation, since it is related to the carrier mobility, the oxide thickness and the physical dimensions.

In chapter 4, a composite n-MOSFET is proposed for replacing conventional n-type MOSFET in circuits where high drain-source voltages exist.

4. Improvement in Lifetime

4.1 Literature Review

Currently, there are two approaches to attack the reliability problem in sub-micron circuits. One is on the device processing level while another is on the circuit design level.

Several processing approaches to the reliability problem have been used, principally the LDD, or lightly doped drain, structure; however, consideration also has been given to doping the structures with germanium, fluorine, chlorine and carbon. Ge impurities implanted in the channel creates scattering to reduce the probability of generating hot-carriers [13]. A small amount of fluorine diffused in SiO_2 can suppress the generation of interface traps significantly [14]. A carbon doped substrate not only reduces the density of hot-electron generated interface sites, but also the concentration of hot carrier trapping sites.

4.2 Composite N-MOSFET

Several circuit tricks have been proposed in many publications [15,16]. In digital circuits, an extra transistor can be added to a NAND gate to reduce the substrate current during the switching transient [15]. By inserting a self-bootstrapping n-MOSFET in a conventional NAND logic circuit, the source potential of the upper n-MOSFET is temporarily increased. Therefore, we reduce the voltage across the drain-source of the upper n-MOSFET during the transient time, resulting in the reduction of the impact ionization effects.

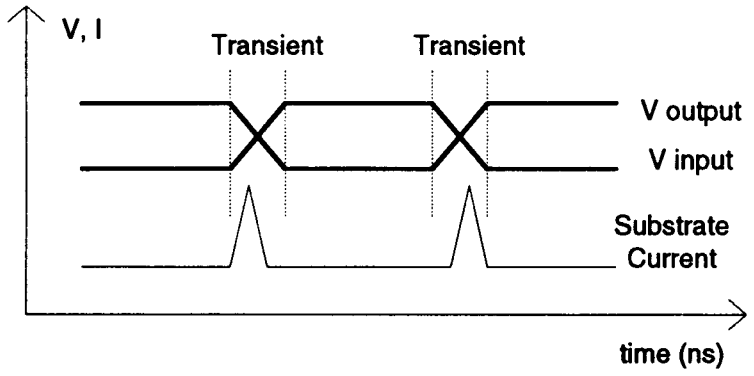


Figure 4.1 Generation of the Substate Current during the Transient Time

In analog circuits, a shield or extra device has been introduced to limit the maximum voltage across the n-MOS device [16]. By inserting a shielding device in series with the n-MOSFET in a conventional CMOS gain stage, we observe that the shielding device goes into saturation to reduce the drain-source voltage across the n-channel device by one half during the positive voltage swing. It has no significant effect during the negative voltage swing since it operates in the triode mode. Power supply voltage reduction from 5V to 3.3V is another simple way to reduce hot-electron degradation.

Here, a composite n-MOS transistor is proposed for use in analog and mixed-mode circuits. This consists of an n-MOSFET transistor and two p-MOSFET devices, as shown in Figure 4.2, where the voltage and/or current across the n-MOS is kept low by employing voltage and current divider techniques.

4.3 I-V Characteristics of the Composite Device

The composite device circuit has three-terminal characteristics similar to a conventional n-channel device. Yet most of the current and/or voltage is absorbed by the output p-MOSFET transistor, which has a large W/L ratio. By inserting a p-MOSFET in series with an n-MOSFET, the drain-source voltage of the n-

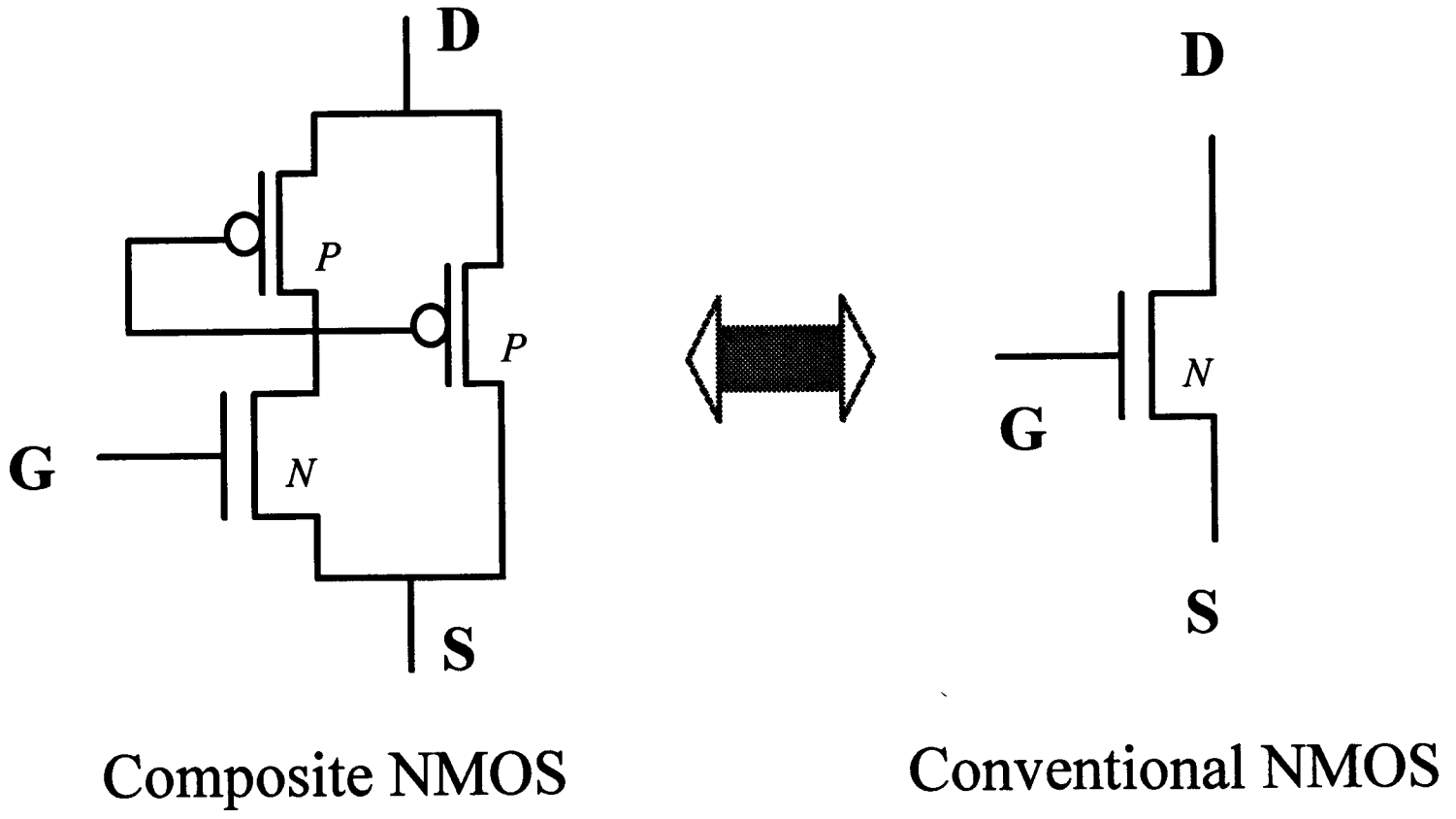


Figure 4.2 Schematic Diagram of the Composite n-MOSFET

channel device is reduced dramatically. Therefore, the substrate current is suppressed.

Figure 4.3 shows a comparison of I-V characteristic curves between normal n-channel and composite NMOS devices.

By observing the I-V characteristic curves of two types of devices, It shows that these two curves are comparable in some applications, such as an output driver. In the case of the output driver, it often has large voltage across the drain-source of the n-channel device. When the gate voltage is at 2.5V and the drain-source voltage is at 5V where the substrate current is the highest. Under the DC operating conditions, $V_{gs} \cong 2.5V$, $V_{ds} \cong 5V$, the I-V curve matches reasonably well.

4.4 Using the Composite Device in Analog and Mixed-Mode Circuits

Device characteristic comparison is one aspect, while the circuit performance is a more important aspect. The real value of a device is determined by its performance in circuits, therefore, a single-ended differential amplifier is selected to determine the performance of both conventional and composite devices. Figure 4.4 is the schematic diagram of the amplifier circuit with an output stage. M12 is the n-MOSFET where the performance comparison is made.

The computer simulation results show that by using the composite device instead of the conventional n-MOSFET in the output gain stage of the CMOS differential amplifier, the substrate current per unit gate width in the n-channel device is suppressed by a factor of 120 in peak value for a sloping input waveform. However, the reduction of the substrate current is at the cost of increased device area and a factor of 2 decreased frequency wave response, as shown in Figure 4.5 and 4.6.

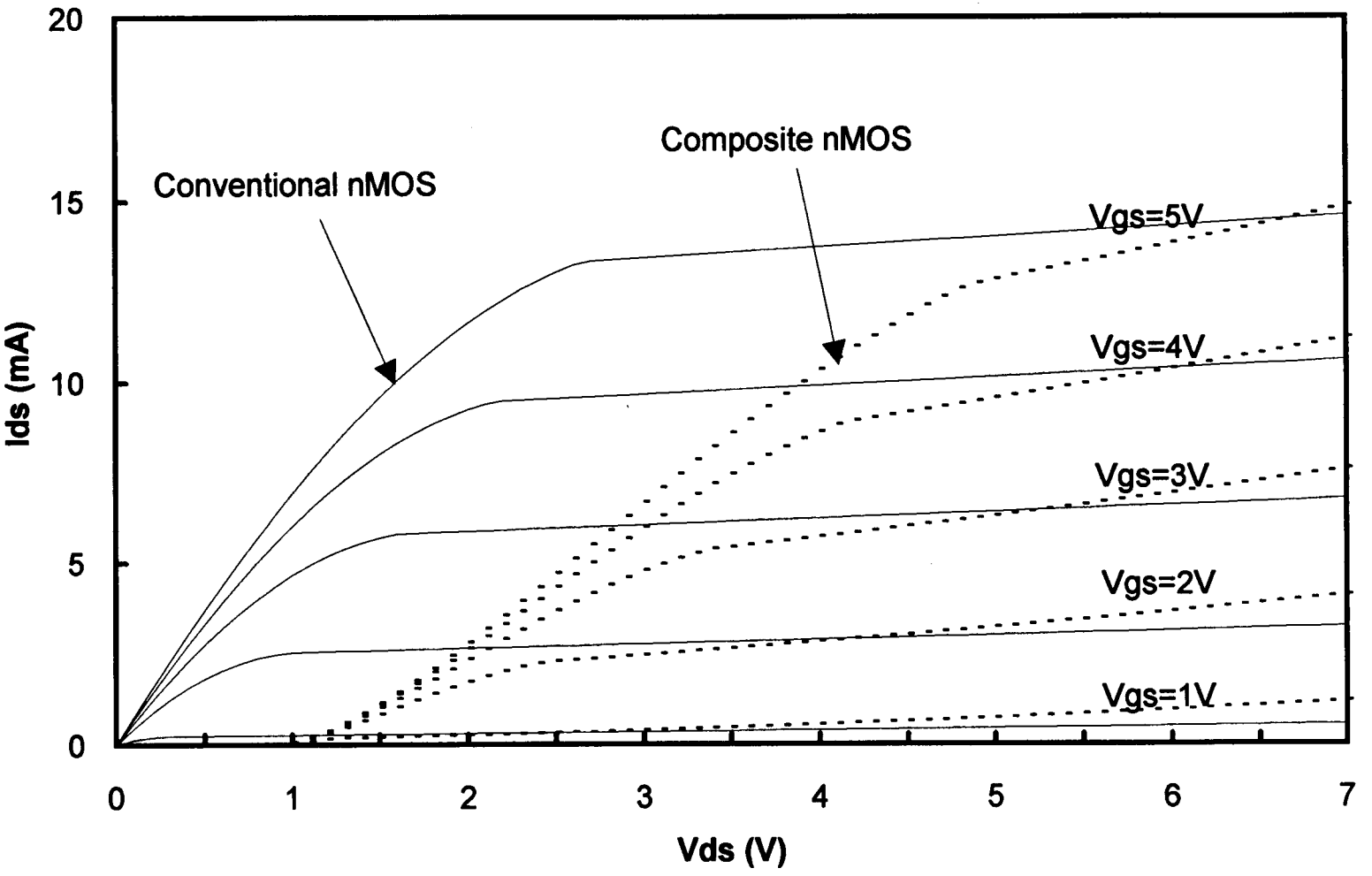


Figure 4.3 I-V Characteristic Curves of Conventional and Composite n-MOSFETs

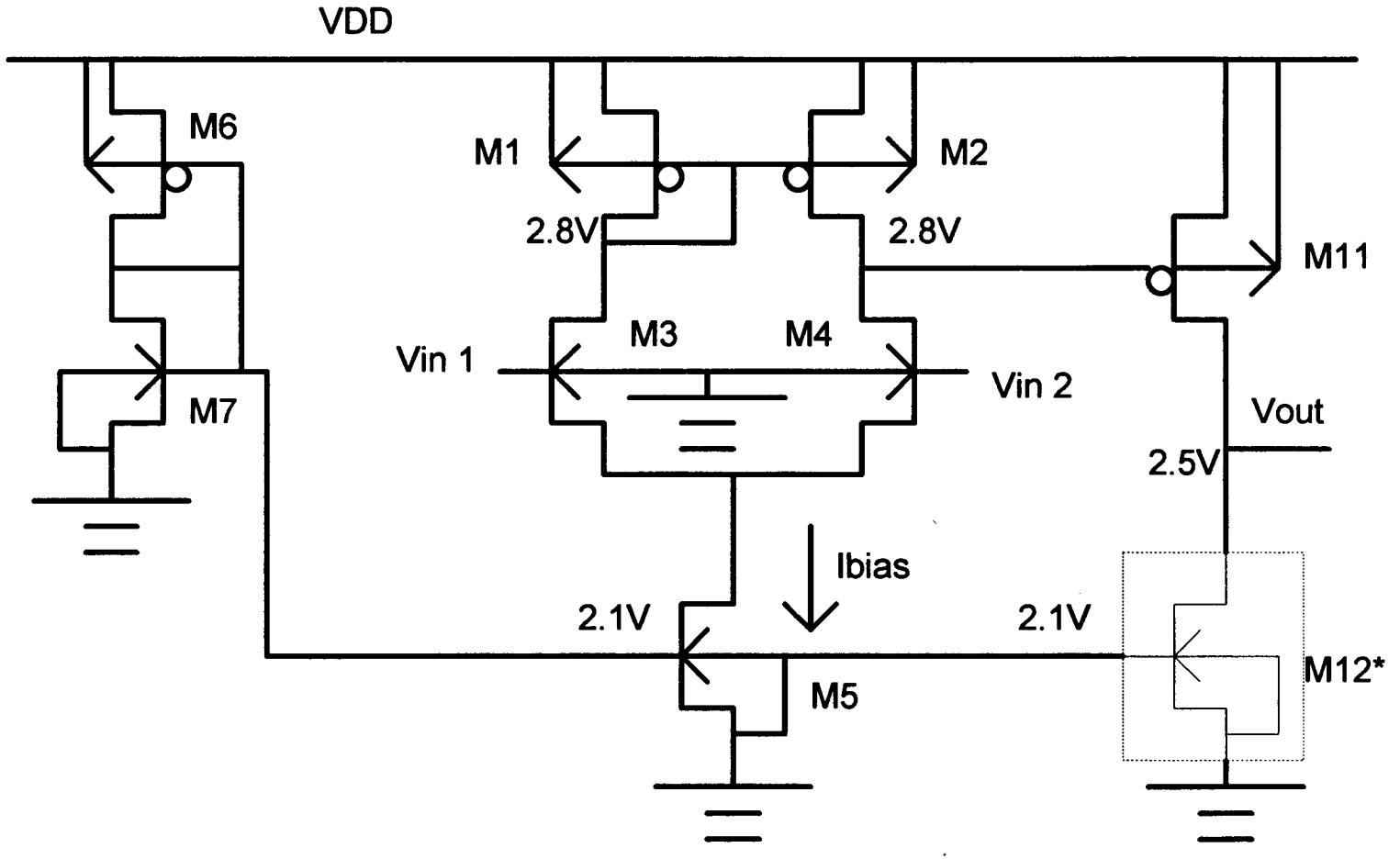


Figure 4.4 CMOS Single-Ended Output Differential Amplifier

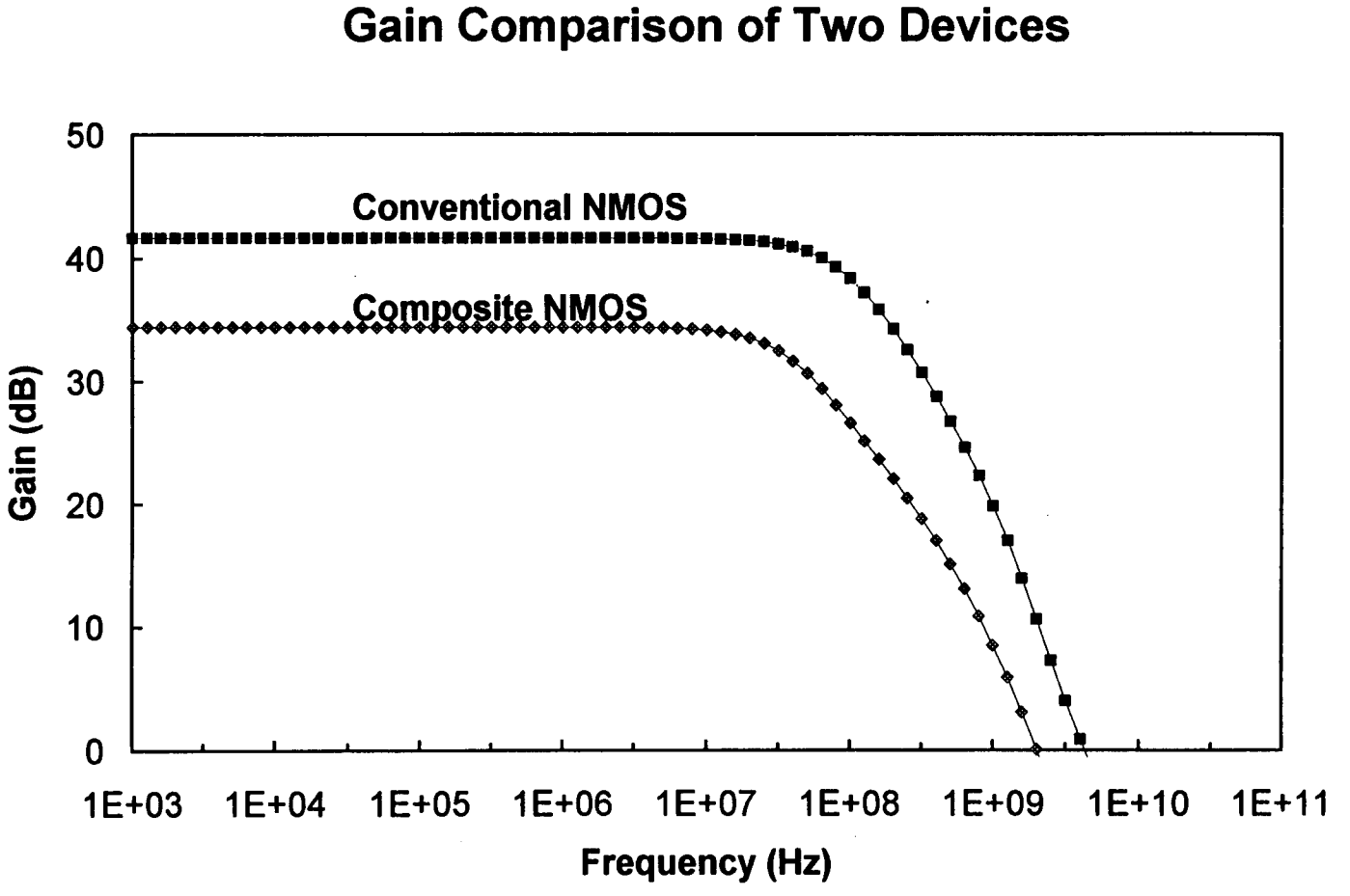


Figure 4.5 Frequency Response of the Amplifier using Conventional and Composite n-MOSFETs

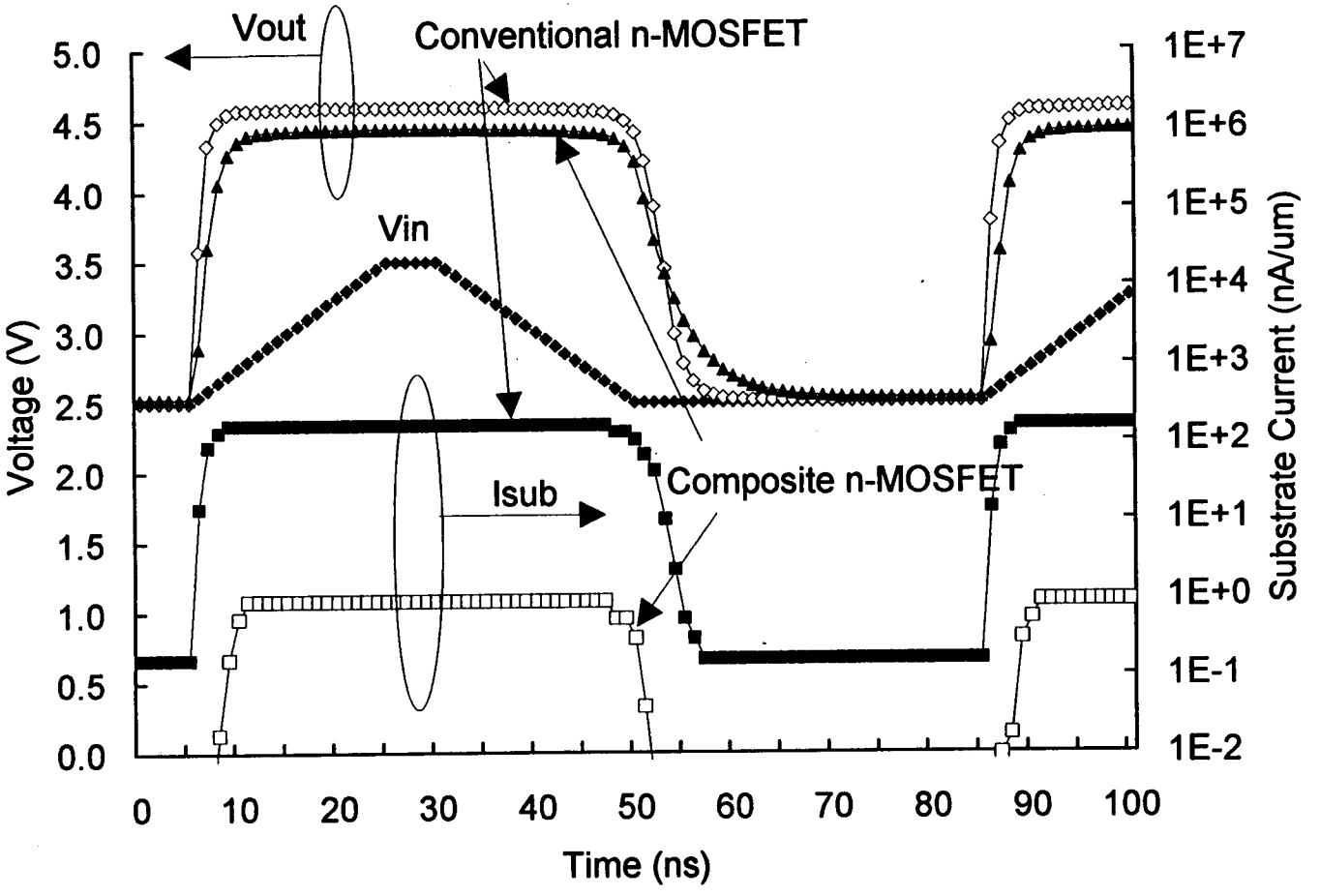


Figure 4.6 Output and Substrate Current Waveforms of the Differential Amplifier

A longer channel length device is less effected by the substrate current and thus has a longer lifetime. To compare the improvement between the 1μm composite and the long channel length device, one uses a 2μm device since it is easy to implement in terms of design, layout and manufacture. The results from the Pspice simulation show that by using the 2μm device at the output stage the amplifier lifetime doubles. The 1μm composite device, however, has an improvement of nearly six orders of magnitude. It seems that the composite device has the potential to improve the lifetime of 0.8μm device circuits more. Since there is no substrate current data available for the 0.8μm channel length device, we have to estimate its substrate current according to Figure 4.7, I_{sub} vs. L_{eff} from the existing device. It shows the substrate currents of 1.0, 1.5 and 2μm devices. Figure 4.8 shows both the measured and projected lifetimes of 0.8, 1, 2μm conventional n-channel devices as well as that of 0.8, 1μm composite devices. From the curves, one can show that by using a 0.8μm composite device the lifetime of the circuit has improved magnitude of eight orders.

Replacing conventional n-channel devices with composite n-MOS devices improves circuit reliability and extends device lifetime dramatically. It provides a simple way to improve device and circuit reliability of sub-micron technology without any modification of device structures and/or fabrication processes.

After proposing possible improvements, chapter 5 is mainly to discuss the importance of hot-electron effect in analog and mixed-mode circuits. There are several different types of circuit families investigated for hot-electron effects, notably, switched-capacitor, sense amplifier and source-coupled logic inverter.

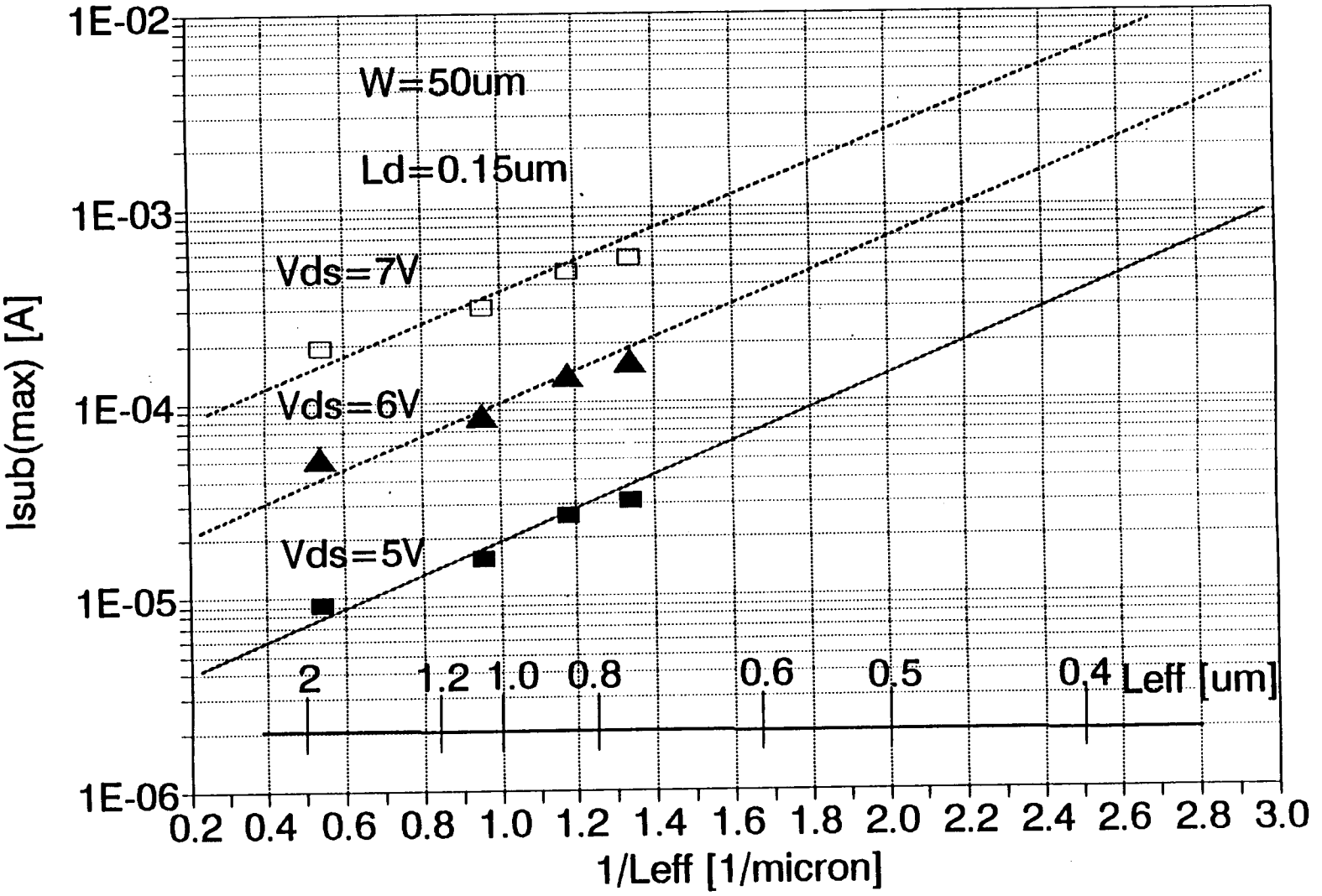


Figure 4.7 The Relationship Between I_{sub} and L_{eff}

Lifetime Projection of the Amplifier

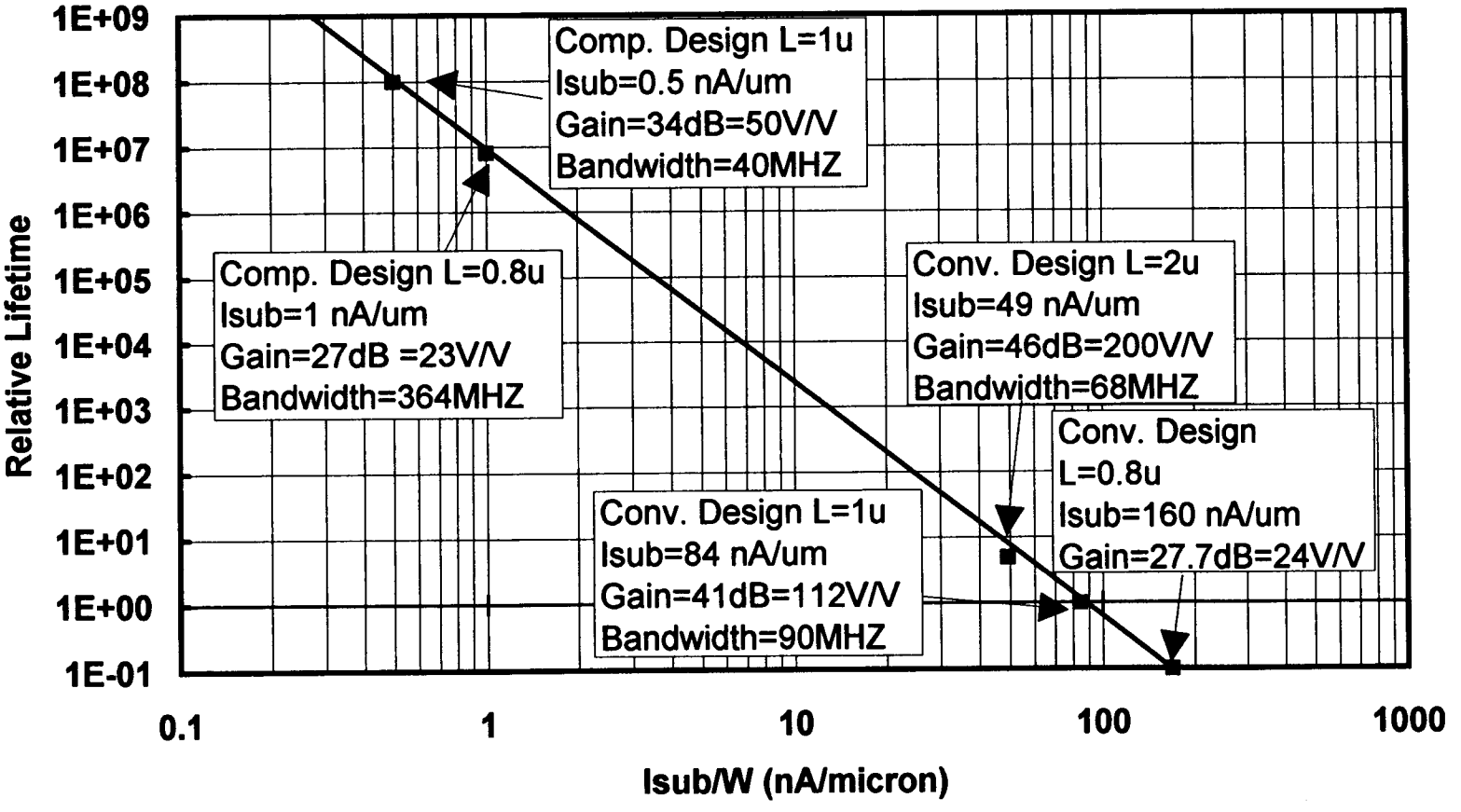


Figure 4.8 The Lifetime Projection

5. Implications of Hot Electron Effects in Analog and Digital Circuits

5.1 Switched-Capacitor Integrator

The differential amplifier is one of the fundamental circuits in both analog and mixed-mode circuits families. One of the commonly used circuits in the analog world to perform the frequency-domain filtering of signals is the switched-capacitor circuit. A switched-capacitor filter consists of op-amps and capacitors instead of conventional passive devices involving resistors, inductors and capacitors. In integrated circuits, it is often difficult to implement resistors and inductors in silicon since the process variation of resistors is very different from that of capacitors. Inductors often introduce interference noise into the IC circuits. Therefore, a new concept was introduced by Fried [11] in the United States in 1972.

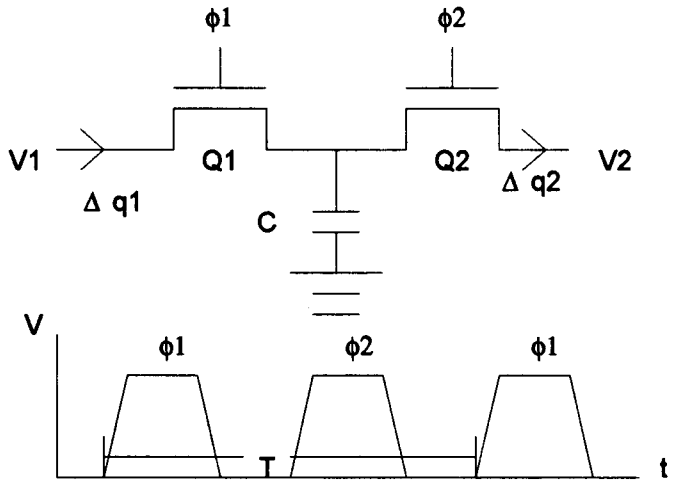


Figure 5.1 Simulated Resistor using Switched Capacitors

As $\phi 1$ rises to high, the charge Δq_1 enters the capacitor from the input V_1. Assuming C is previously charged to V_2, now it is charged to V_1. Therefore the total charge can be calculated as :

$$\Delta q_1 = C(V_1 - V_2) \tag{5.1}$$

Then as $\phi 1$ goes down to low, the capacitor holds its voltage at V_1 before $\phi 2$ goes to high. When $\phi 2$ goes to high, the capacitor is recharged to V_2 through Q_2. Hereby, Δq_1 is equal to Δq_2 during the clock period, T.

We now can define the average current flowing from the input to the output as below:

$$i \equiv \frac{\Delta q_1}{T} = \frac{\Delta q_2}{T} = \frac{C}{T}(V_1 - V_2) \tag{5.2}$$

The I-V characteristic of a resistor can be expressed as below:

$$i = \frac{1}{R}(V_1 - V_2) \tag{5.3}$$

By comparing equations 5.2 and 5.3, we discover that these two equations are very similar in terms of I-V characteristic behavior. Therefore, we define as below:

$$R \equiv \frac{T}{C} \tag{5.4}$$

In other words, the physical behavior of a resistor can be simulated by using a capacitor and periodic clocks. The switched-capacitor integrator is one of the most basic circuits in SC circuits area. Its schematic is shown in Figure 5.2.

In this circuit, an offset voltage is induced due to the hot-electron degradation caused by mismatching, as explained in chapter 3. This offset voltage at the input will cause dc level shifting at the output, which may affect the dc bias condition of the next stage. By the same analysis as shown above for the resistors, the transfer function for the offset voltage of this particular circuit can be shown follows:

$$\Delta V_{out} = (1+\frac{C_1}{C_2})V_{offset} \tag{5.5}$$

The offset voltage can be amplified to the output of the integrator, depending upon the values of C_1 and C_2. Thus V_{off} may cause the dc bias condition of the next stage to be shifted unintentionally, especially in multiple stage circuits. The final result will be circuit failure. Corrective measures are required to eliminate the effect of the offset voltage caused by hot-electron degradation. [17] [18]

5.2 Sense Amplifier

The sense amplifier is one of the circuits commonly used in DRAM and some SRAM circuits. The core part of the sense amplifier is a cross-coupled latch activated during sensing by either a pull-down or a pull-up latching waveform to amplify and to restore a differential voltage signal. Parametric mismatch in threshold voltage and transconductance such as g_d and g_m, can cause logic errors

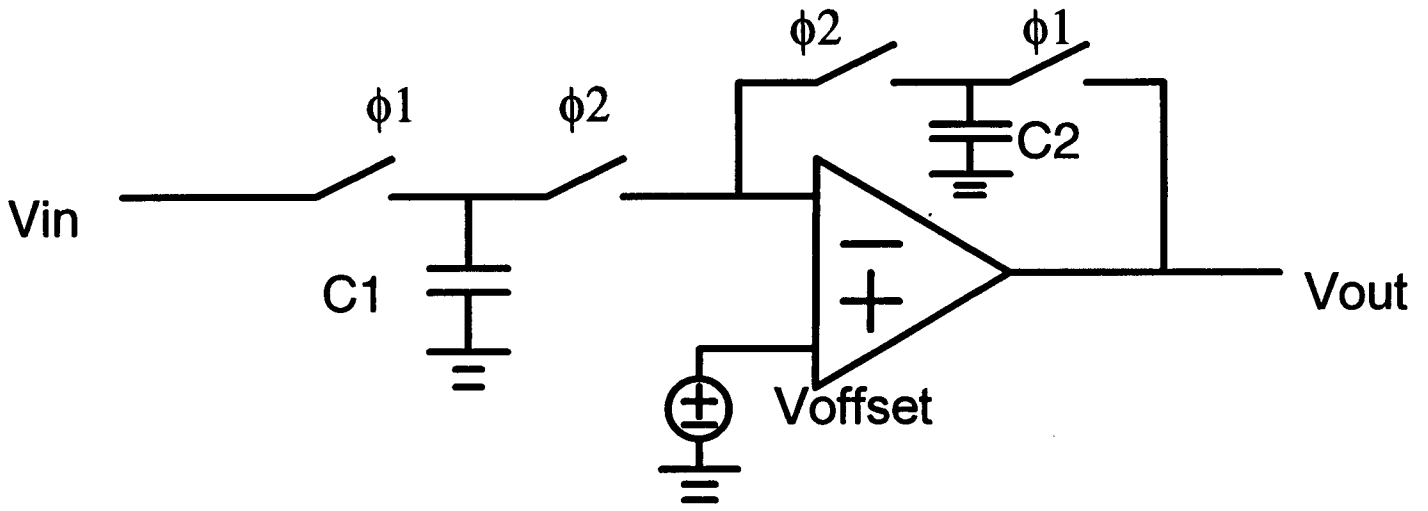


Figure 5.2 Switched-Capacitor Integrator

in the sense amplifier. It may amplify the differential input signal in the wrong direction. To determine the performance of the sense amplifier, a new terminology is introduced -sensitivity-. It is defined as the magnitude of the minimum differential input signal that can be correctly sensed. Figure 5.3 shows the cross-coupled CMOS sense amplifier [19].

V_p, V_s are the pre-charge and sink voltages, while V_1, V_2 are the differential input signals from the bit-lines of the memory. Fig. 5.4 shows the Pspice simulation results for the case of successful sensing for a linear latching and simultaneous activation sense amplifier. Under the perfectly balanced, or symmetrical condition, V_1 is amplified to nearly V_p, while V_2 is sunk down to V_s. V_1 is initially higher than V_2. Spice level 3 model is used for simulation. A case of unsuccessful sensing is shown in Fig. 5.5. Even though V_2 is higher than V_1, V_2 is still sunk down to V_s, while V_1 is charged up to V_p. In this case, the differential input voltage is 100mV, and the threshold voltage mismatch is 140mV. The sense amplifier circuit is vertically matched, or W/L's of NMOSFETs and PMOSFETs are ratioed, so that it has equal pull-up and pull-down capability.

Fig.5.6 shows that the sensitivity of the sense amplifier is linearly related to the change of I_{ds}, which is caused by threshold voltage shift due to hot-electron degradation. At the maximum allowed 2.5% I_{ds} mismatch before declaring circuit failure, the sensitivity of the sense amplifier degrades to 65mV from 2mV. The damage caused by degradation is rather severe. For a small I_{ds} variation, the sensitivity can be expressed as below:

$$Sensitivity \propto \Delta I_{ds} \propto \Delta V_{th} \qquad (5.6)$$

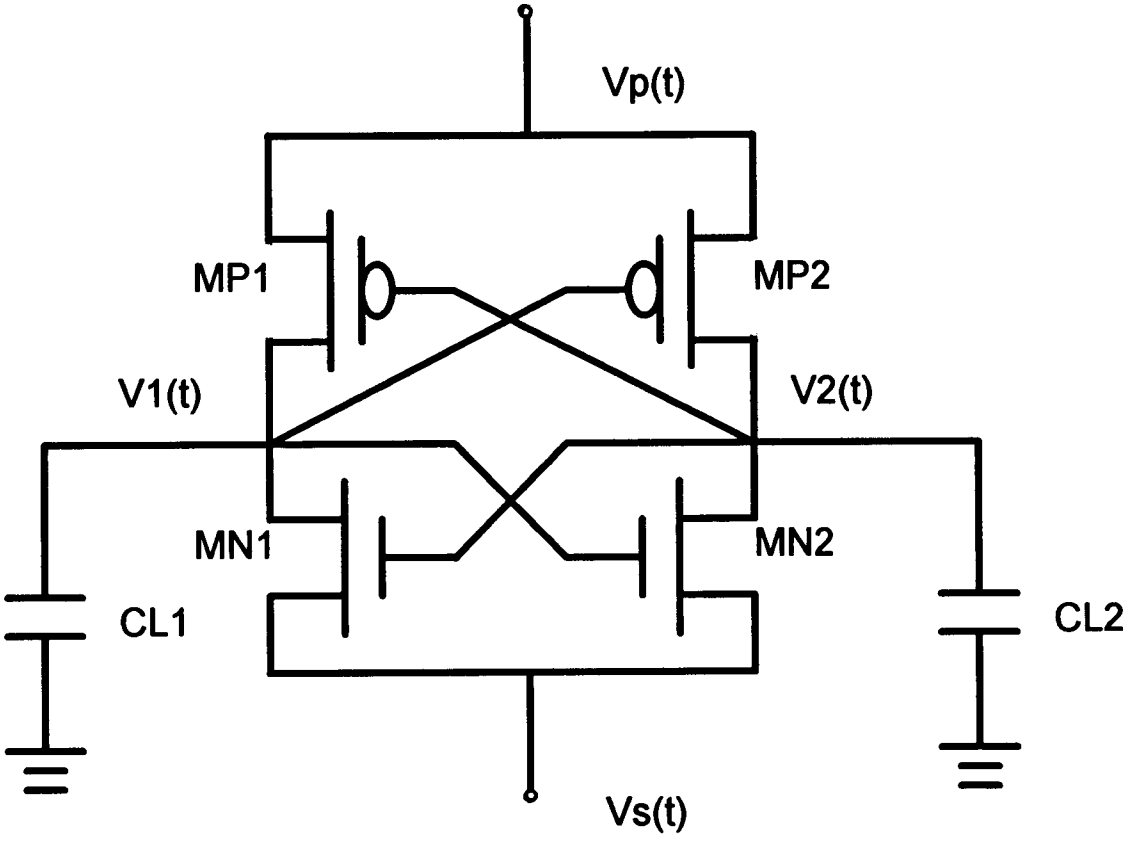


Figure 5.3 A Simple Sense Amplifier

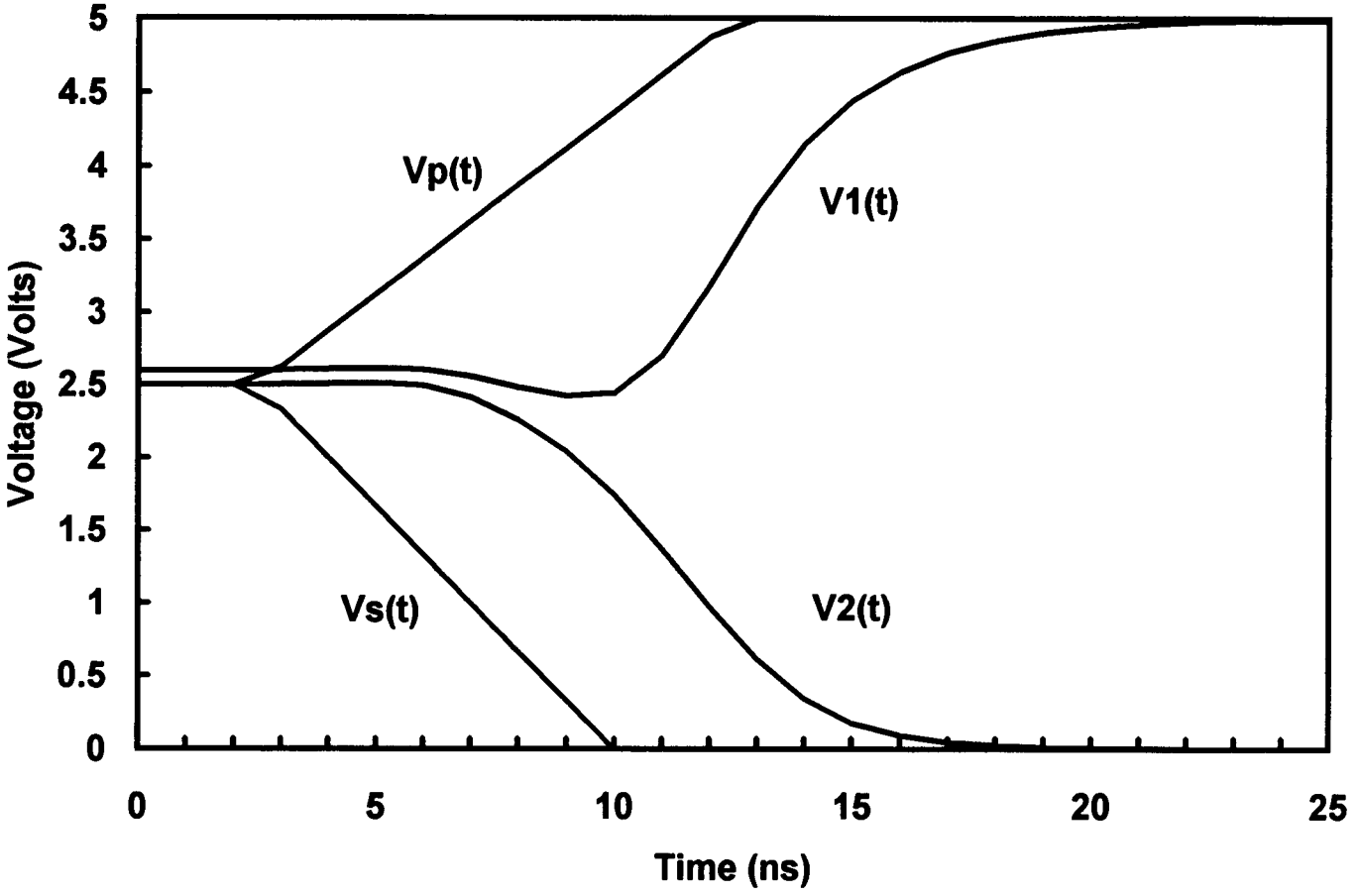


Figure 5.4 Successful Sensing of the Sense Amplifier

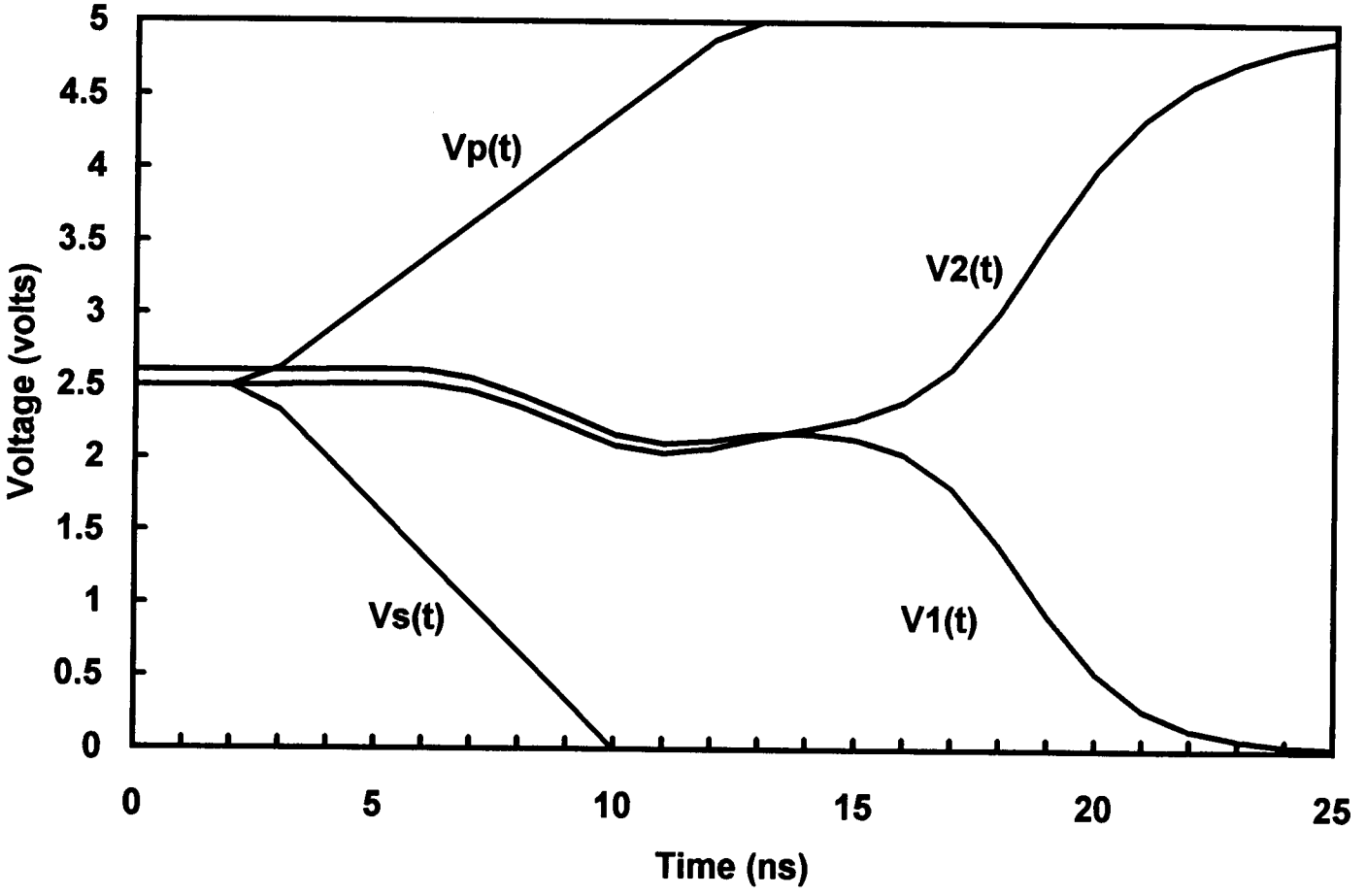


Figure 5.5 Unsuccessful Sensing of the Sense Amplifier

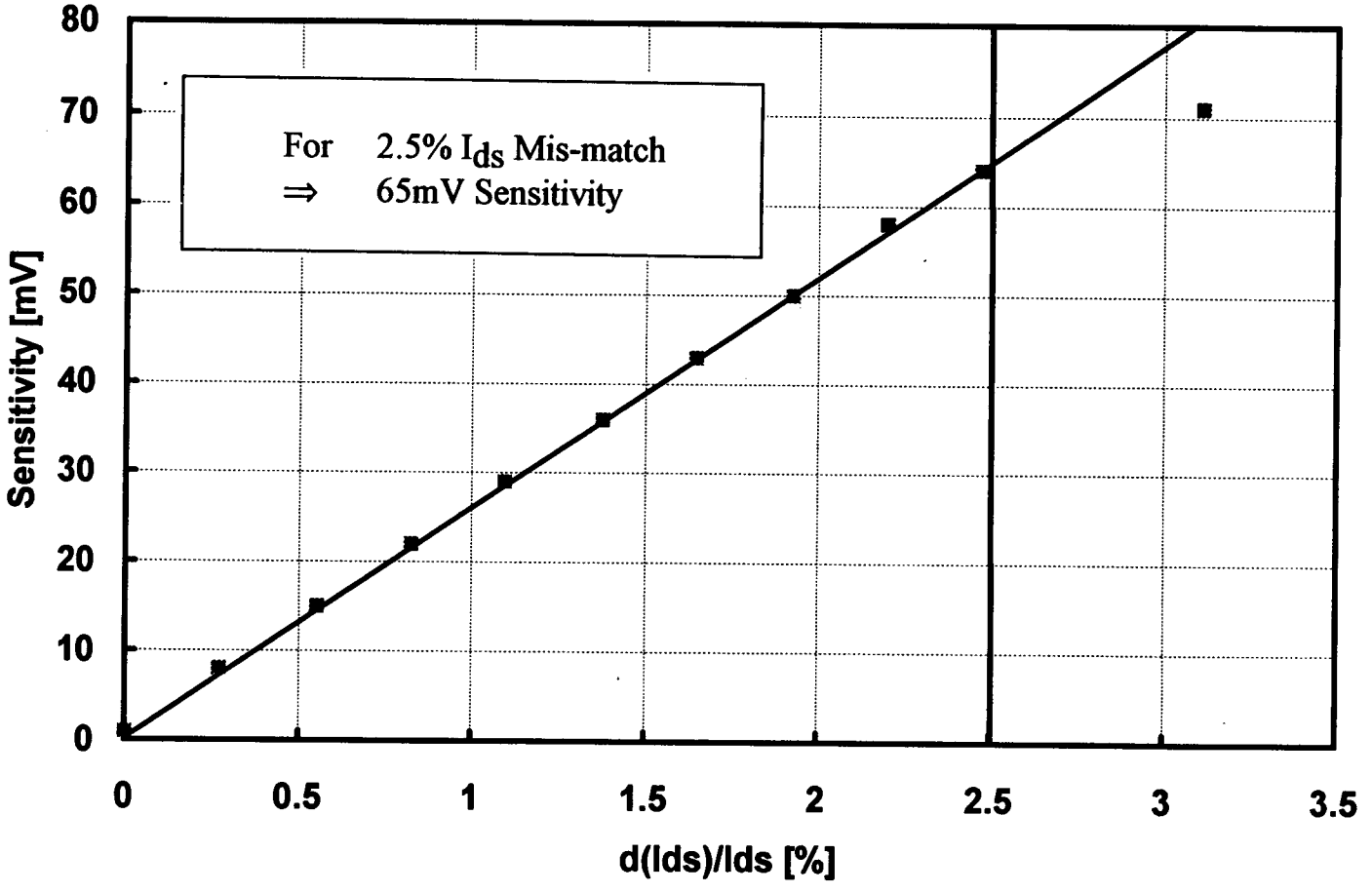


Figure 5.6 Effects of Drain Current Variation on Sense Amplifier Sensitivity

The transconductance dependence of sensitivity is shown in Fig.5.7 and 5.8. Fig.5.7 shows that the sensitivity is a linear function of g_{ds}. However, for 50% of g_{ds} variation, where the circuits will no longer be considered reliable, there is only a 3mV change in sensitivity. Therefore, one may conclude that the effect of g_{ds} on the sense amplifier is minimal. The negative sensitivity shifting can compensate for the positive shifting due to other parametric degradation.

A 10% degradation of g_m can cause nearly a 30mV sensitivity shift toward the positive direction. The g_m variation is achieved by varying the carrier mobility and threshold voltage simultaneously to isolate the effect of g_m without involving the effects of other parametric degradation.

From the simulation results shown above, the circuit performance degradation caused by hot-electron injection can be fairly severe if all parametric degradation occurs together in the worse case.

5.3 Source-Coupled Logic

One of the most important members of the digital logic family is the source-coupled logic(SCL). Its major advantage over conventional CMOS static logic is that the SCL circuit has much smaller switching noise while providing comparable, or better performance in terms of power dissipation, speed and accuracy [20].

A simple differential CMOS SCL inverter is shown in Fig.5.9. The basis of this circuit is an NMOS differential pair biased with a constant current source. The logic input is a differential input voltage which controls the current flowing only through one side of the differential pair. From the performance point of view, the SCL circuit does not produce the large switching noise since its operating mechanism determines the low overlap current spikes. From the reliability point of

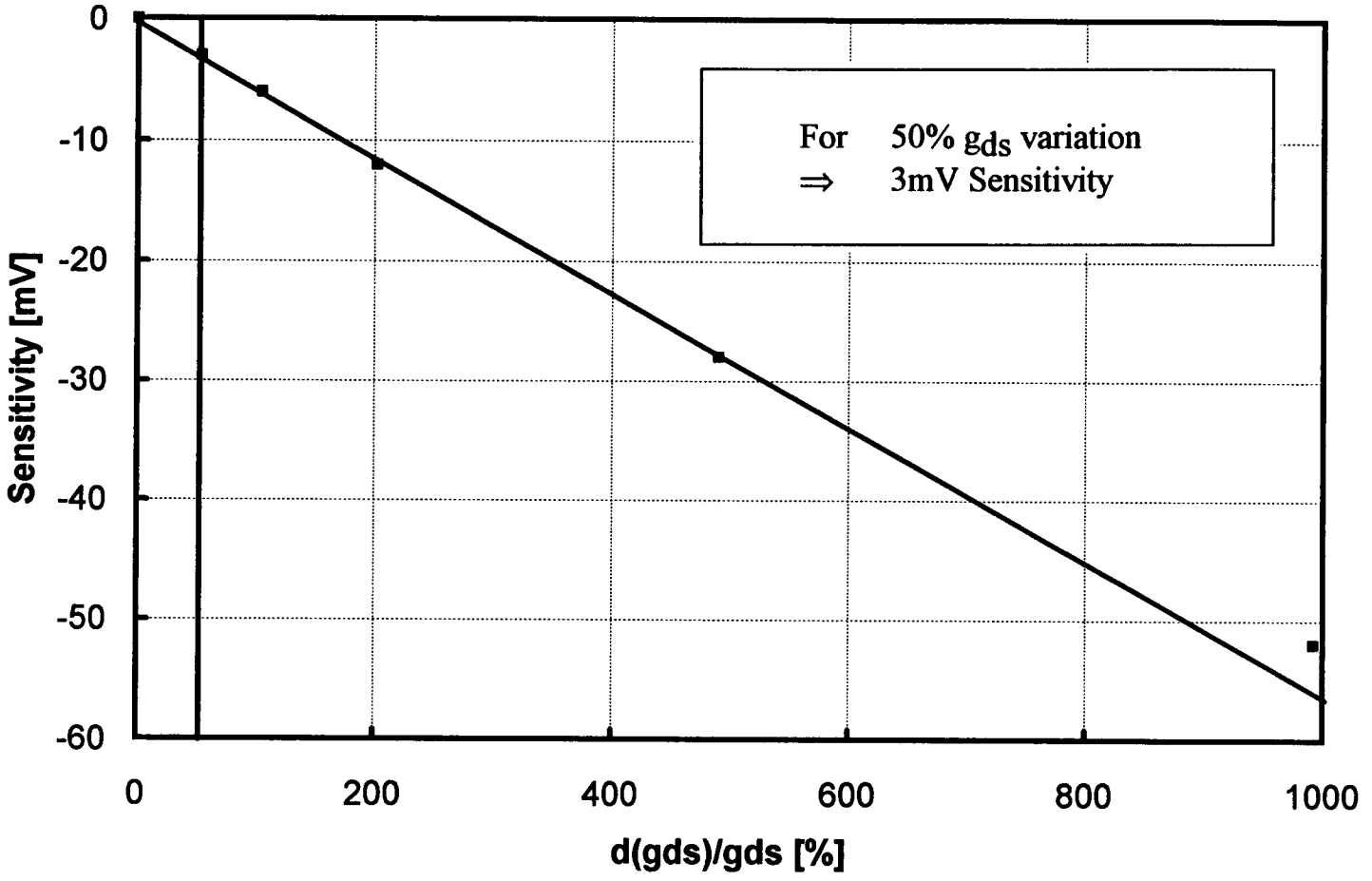


Figure 5.7 Effects of Drain Conductance Variation on Sense Amplifier Sensitivity

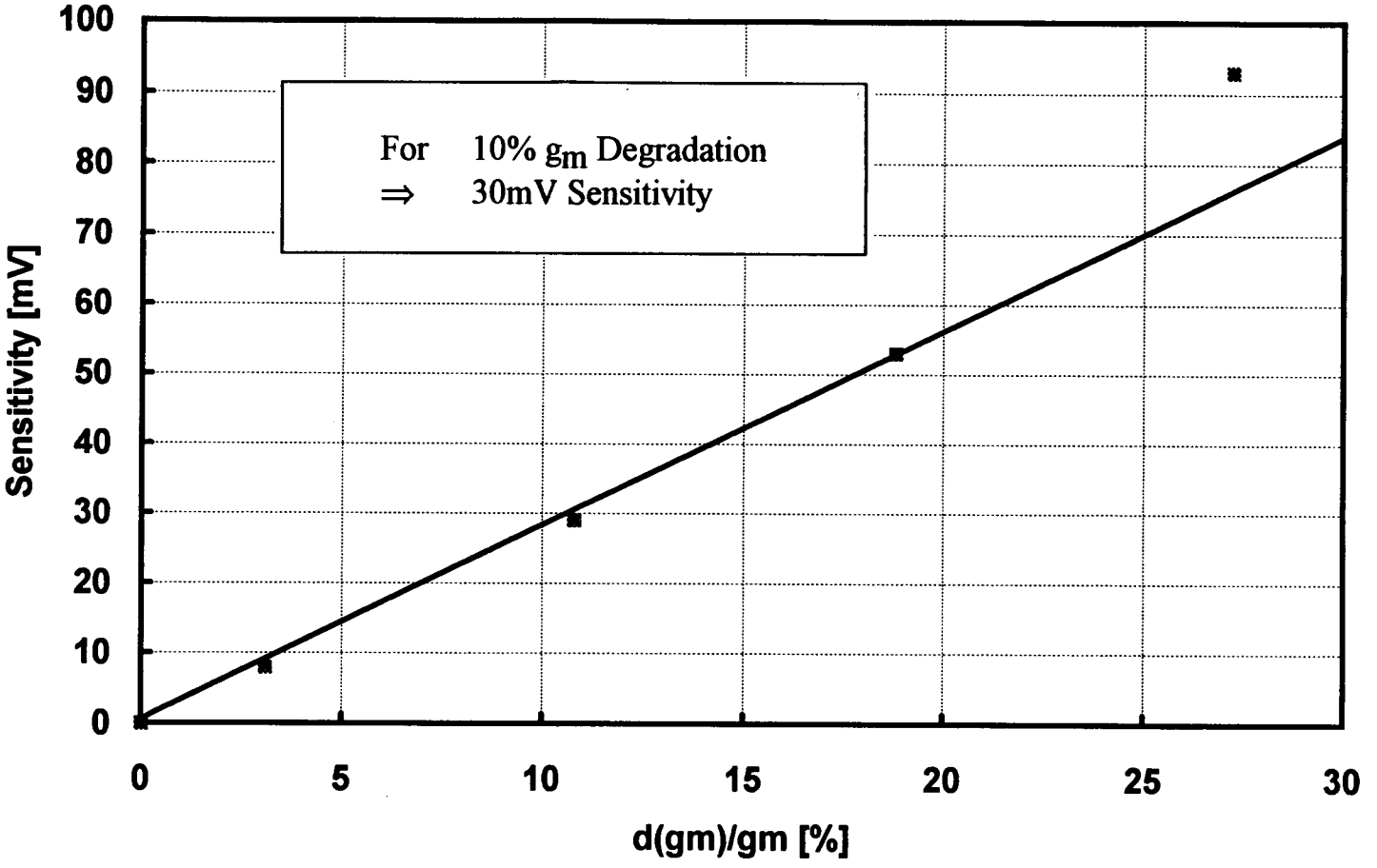


Figure 5.8 Effects of Transconductance Variation on Sense Amplifier Sensitivity

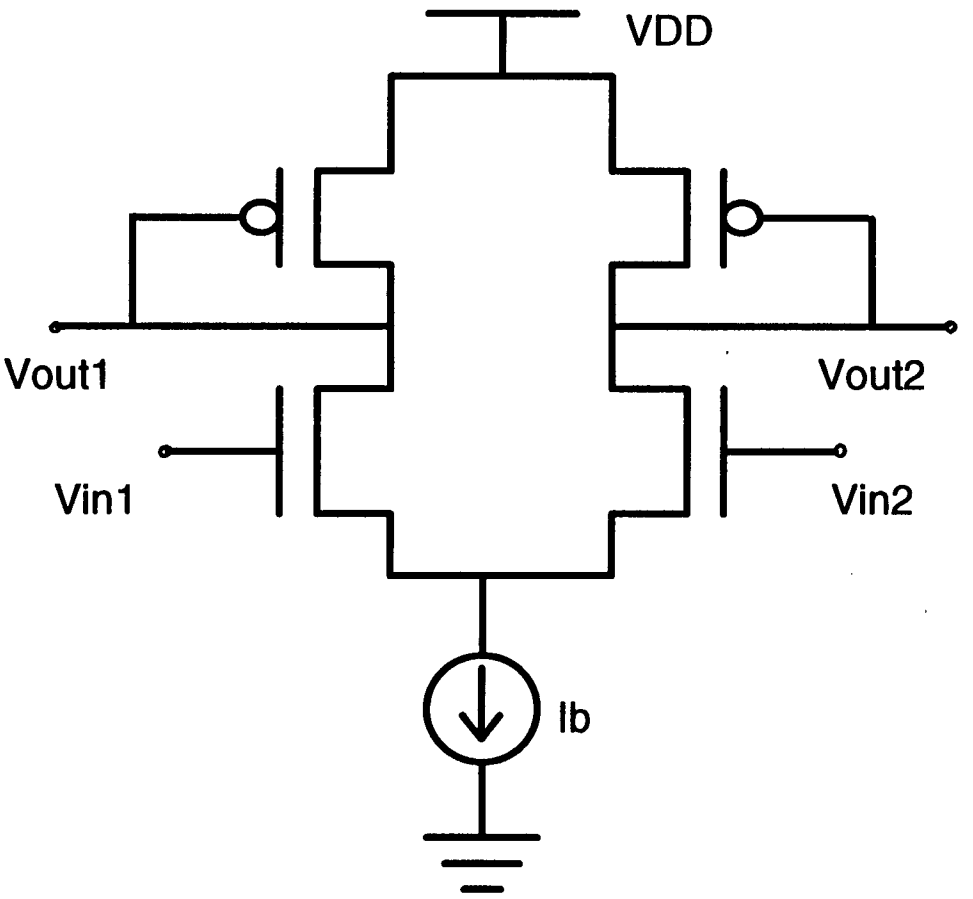


Figure 5.9 A Source-Coupled Logic Inverter

view, the differential pair mismatch has very little effect on the performance because it is a one-side operation only. However, the threshold voltage shift, drain conductance shift and drain current change will certainly affect the performance of the SCL inverter in terms of the speed.

6. Conclusion

The effect of hot-electron degradation on analog and mixed-mode circuits has been studied in this work. The major concentration of the reliability consideration is given to the matching requirements in analog and mixed-mode circuits. The first part of the work presents several mechanisms of hot-electron injection and identifies the substrate current as the key indicator for measuring hot-electron degradation, as well as the device lifetime. Several device parameters have been experimentally measured under dc stress condition. The degradation phenomenon has been observed in various measurements, including threshold voltage, transconductance, and drain current.

The effect of hot-electron degradation on analog and mixed-mode circuits is determined by simulating the differential amplifier performance in terms of gain and dc bias with parametric variations. The simulation results confirm that the hot-electron degradation has significant influence on circuit performance. The threshold voltage shift is amplified to the output of the differential amplifier. Thus it changes the dc bias condition at the output. The drain conductance variation ruins the originally optimized gain, from 4500 V/V down to 100V/V, of a differential amplifier circuit using one micron technology.

A composite MOSFET has been proposed to reduce the hot-electron effects by suppressing substrate current. It has three terminal characteristics similar to that of a conventional n-type MOSFET. By replacing a conventional n-MOSFET at the output stage with the composite n-MOSFET, the average substrate current is suppressed by nearly 90 times, while maintaining comparable circuit performance. Table 1 compares two devices in terms of device characteristics and circuit performance.

Table 1 Comparison of Device Characteristics and Circuit Performance of Conventional and Composite n-MOSF

Device Characteristics	Channel Length	Effective Width	Actual Area	Unity Gain Frequency
	micron	micron	um*um	GHz
Normal N-Channel Device	0.8	50	40	17.5
Composite NMOS	0.8	50	228	14.5
Normal N-Channel Device	1	50	50	13
Composite NMOS	1	50	345	11
Normal NMOS	2	50	100	3.3

Circuit Performance	DC Gain	Cutoff Frequency	Unity Gain Frequency	Substrate Current
	dB	MHz	GHz	nA/um (ave.)
Normal N-Channel Device(0.8u	27	442	5.7	160
Composite NMOS (0.8u)	28	364	5.2	1.1
Normal N-Channel Device(1u)	41	90	4.2	84
Composite NMOS (1u)	34	40	2.6	0.5
Normal N-Channel Device(2u)	46	68	3.26	48.8

Matching requirements in analog and mixed-mode circuits need to be taken into serious consideration because of the severe mismatch caused by hot-electron-induced degradation. Some mismatch can be corrected by using clever circuit design techniques, while others require process level improvement. The major advantage of the proposed composite n-MOSFET is that it can be applied to a designed circuit to improve device and circuit reliability without modification of device and/or fabrication process.

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APPENDICES

Appendix A.

1). Mosis level 1 Spice model

This model is used in the case study for the effects of threshold change on the gain of an 2μm operational amplifier.

**MODEL CARDS

```
MODEL NTYPE NMOS(LEVEL=1 VTO=1 KP=2.4E-5 LAMBDA=2.0E-2
+          CBD=2.0E-14 CBS=2.0E-14 PB=0.7
+          CGSO=3.3E-10 CGDO=3.3E-10 CGBO=1.5E-9 TOX=8E-8
+          FC=0.5)

.MODEL PTYPE PMOS(LEVEL=1 VTO=-1 KP=1.2E-5 LAMBDA=1E-2
+          CBD=2.0E-14 CBS=2.0E-14 PB=0.7
+          CGSO=3.3E-10 CGDO=3.3E-10 CGBO=1.5E-9 TOX=8E-8
+          FC=0.5)
```

2). Generic Level 3 Berkeley Device Model

This model is used to simulate the performance of a circuit under near reality condition.

**MODEL CARDS

```
.MODEL NM1 NMOS(LEVEL=3 LD=0.15U WD=0.3U VTO=0.73 TOX=200E-10
+ UO=520 NSUB=2.8E16 VMAX=1.35E5 ETA=0.02 THETA=0.07 KAPPA=0.1
+ DELTA=0.6 XJ=0.1U NFS=5E11 RSH=20 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=3.2E-4 CJSW=2.8E-10
+ MJ=0.95 MJSW=0.12 JS=1E-3 FC=0 PB=0.8)
* FOR W=50U SHEET RESISTANCE IS SCALED DOWN TO 1000/50=20

.MODEL PM1 PMOS(LEVEL=3 LD=0.0U WD=0.4U VTO=-0.9 TOX=200E-10
+ UO=180 NSUB=2.8E16 VMAX=1.9E5 ETA=0.09 THETA=0.13 KAPPA=3
+ DELTA=0.3 XJ=0.0U NFS=1E12 RSH=17.5 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=5.2E-4 CJSW=2.8E-10
```

```
+ MJ=0.5 MJSW=0.33 JS=1E-3 FC=0 PB=0.9)
*RSH IS SCALED DOWN TO 1400/80=17.5
```

Appendix B: CMOS Differential Amplifier Circuit Files

1). 2μm CMOS Amplifier using level 1 model

This circuit is used to determine the effect of Vth variation on gain (Chapter 3)

```
CMOS OPERATIONAL AMPLIFIER L=2μm
*THIS SIMULATION IS DONE FOR PROF. FORBES TO TEST THE EFFECTS
* OF Vth VARIATION IN A GENERAL CMOS AMPLIFIER USING
* 2 um TECHNOLOGY
*DATE 1-15-92

*POWER SUPPLY
VDD 4 0 DC 5
VSS 8 0 DC -5

*INPUT SIGNAL
VIN1 1 0 AC 1mV

**FIRST STAGE OF THE DIFFERENTIAL AMPLIFIER
M1 5 0 2 2 NTYPE  L=2U   W=10U
M2 6 1 2 2 NTYPE  L=2U   W=10U
M3 5 5 4 4 PTYPE  L=2U   W=34U
M4 6 5 4 4 PTYPE  L=2U   W=34U
M5 2 3 8 8 NTYPE  L=2U   W=18U

**SECOND & OUTPUT STAGE
M6 7  6 4 4 PTYPE L=2U  W=100U
M7 7  3 8 8 NTYPE L=2U  W=22U
M8 10 6 4 4 PTYPE L=2U  W=100U
M9 10 3 8 8 NTYPE L=2U  W=22U

**BIASING CIRCUIT
M12 3 3 8 8  NTYPE L=18U W=12U
R1  4 3          200K

**ANALYSIS
.TF V(10) VIN1
.OP
```

```
.AC DEC 10 0.01K 100MEG
.PROBE
.END
```

2) 0.8μm CMOS Differential Amplifier with Output Stage using all 0.8μm Device

This circuit is to determine the performance of the CMOS amplifier using all 0.8μm devices.

CMOS Differential Amplifier With Output Stage L=0.8U

```
VDD 1 0 DC 5V
*VIN2 3 0 PWL(0 2.5V 5NS 2.5V 25NS 3.5V 30NS 3.5V 50NS 2.5V 85NS 2.5V
*+ 105NS 3.5V)
*VIN2 3 0 PWL(0 2.51V 5NS 2.51V 5.01NS 2.49V 30NS 2.49V 30.01NS 2.51V
55NS
*+ 2.51V 55.01NS 2.49V 80NS 2.49V 80.01NS 2.51V 100NS 2.51V)
*VIN2 3 0 PWL(0 3.5V 5NS 3.5V 5.01NS 2.5V 30NS 2.5V 30.01NS 3.5V 55NS
*+ 3.5V 55.01NS 2.5V 80NS 2.5V 80.01NS 3.5V 100NS 3.5V)
VIN1 2 0 DC 2.5V
VIN2 3 0 DC 2.5V AC 1MV
*.DC VIN -5 5 0.1
*VIN 3 0

* AMPLIFIER CIRCUIT
M1 5 5 1 1 PM1 L=0.8U W=70U
M2 6 5 1 1 PM1 L=0.8U W=70U
M3 5 2 4 0 NM1 L=0.8U W=50U
M4 6 3 4 0 NM1 L=0.8U W=50U

* OUTPUT STAGE
M11 7 6 1 1 PM0 L=0.8U W=71U
M12 7 8 0 0 NM3 L=0.8U W=50U

*BIAS CIRCUIT
M5 4 8 0 0 NM2 L=0.8U W=100U
M6 8 8 1 1 PM2 L=0.8U W=25U
M7 8 8 0 0 NM1 L=0.8U W=50U

.MODEL NM1 NMOS(LEVEL=3 LD=0.15U WD=0.3U VTO=0.73 TOX=200E-10
+ UO=520 NSUB=2.8E16 VMAX=1.35E5 ETA=0.02 THETA=0.07 KAPPA=0.1
+ DELTA=0.6 XJ=0.1U NFS=5E11 RSH=20 RD=0 RS=0 RG=0 RB=0
```

```
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=3.2E-4 CJSW=2.8E-10
+ MJ=0.95 MJSW=0.12 JS=1E-3 FC=0 PB=0.8)
* FOR W=50U SHEET RESISTANCE IS SCALED DOWN TO 1000/50=20

.MODEL NM2 NMOS(LEVEL=3 LD=0.15U WD=0.3U VTO=0.73 TOX=200E-10
+ UO=520 NSUB=2.8E16 VMAX=1.35E5 ETA=0.02 THETA=0.07 KAPPA=0.1
+ DELTA=0.6 XJ=0.1U NFS=5E11 RSH=10 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=3.2E-4 CJSW=2.8E-10
+ MJ=0.95 MJSW=0.12 JS=1E-3 FC=0 PB=0.8)
* FOR W=50U SHEET RESISTANCE IS SCALED DOWN TO 1000/100=10

.MODEL NM3 NMOS(LEVEL=3 LD=0.15U WD=0.3U VTO=0.83 TOX=200E-10
+ UO=520 NSUB=2.8E16 VMAX=1.35E5 ETA=0.02 THETA=0.07 KAPPA=0.1
+ DELTA=0.6 XJ=0.1U NFS=5E11 RSH=20 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=3.2E-4 CJSW=2.8E-10
+ MJ=0.95 MJSW=0.12 JS=1E-3 FC=0 PB=0.8)
* FOR W=50U SHEET RESISTANCE IS SCALED DOWN TO 1000/50=20

.MODEL PM0 PMOS(LEVEL=3 LD=0.0U WD=0.4U VTO=-0.9 TOX=200E-10
+ UO=180 NSUB=2.8E16 VMAX=1.9E5 ETA=0.09 THETA=0.13 KAPPA=3
+ DELTA=0.3 XJ=0.0U NFS=1E12 RSH=19.7 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=5.2E-4 CJSW=2.8E-10
+ MJ=0.5 MJSW=0.33 JS=1E-3 FC=0 PB=0.9)
*RSH IS SCALED DOWN TO 1400/71=19.7

.MODEL PM1 PMOS(LEVEL=3 LD=0.0U WD=0.4U VTO=-0.9 TOX=200E-10
+ UO=180 NSUB=2.8E16 VMAX=1.9E5 ETA=0.09 THETA=0.13 KAPPA=3
+ DELTA=0.3 XJ=0.0U NFS=1E12 RSH=20 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=5.2E-4 CJSW=2.8E-10
+ MJ=0.5 MJSW=0.33 JS=1E-3 FC=0 PB=0.9)
*RSH IS SCALED DOWN TO 1400/70=20

.MODEL PM2 PMOS(LEVEL=3 LD=0.0U WD=0.4U VTO=-0.9 TOX=200E-10
+ UO=180 NSUB=2.8E16 VMAX=1.9E5 ETA=0.09 THETA=0.13 KAPPA=3
+ DELTA=0.3 XJ=0.0U NFS=1E12 RSH=56 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=5.2E-4 CJSW=2.8E-10
+ MJ=0.5 MJSW=0.33 JS=1E-3 FC=0 PB=0.9)
*RSH IS SCALED DOWN TO 1400/25=56

*ANALYSIS
*.OP
*.TF V(7) VIN2
.AC DEC 10 1K 100E9
*.TRAN 1NS 100NS
```

```
*.PRINT tran V(3) V(7)
.PROBE
.END
```

3) 0.8μm CMOS Differential Amplifier with Output Stage using Composite Device.

This circuit is to determine the performance of the 0.8μm CMOS amplifier using composite device at M12, output stage.

CMOS Differential Amplifier L=0.8μm With Output Stage Using Composite Device

```
* COMPOSITE  NMOS AT THE OUTPUT M12 (L=0.8U)

VDD 1 0 DC 5V
*VIN2 3 0 PWL(0 2.5V 5NS 2.5V 25NS 3.5V 30NS 3.5V 50NS 2.5V 85NS 2.5V
*+ 105NS 3.5V)
*VIN2 3 0 PWL(0 2.51V 5NS 2.51V 5.01NS 2.49V 30NS 2.49V 30.01NS 2.51V
55NS
*+ 2.51V 55.01NS 2.49V 80NS 2.49V 80.01NS 2.51V 100NS 2.51V)
*VIN2 3 0 PWL(0 3V 5NS 3V 5.01NS 2V 30NS 2V 30.01NS 3V 55NS
*+ 3V 55.01NS 2V 80NS 2V 80.01NS 3V 100NS 3V)
*.DC VIN -5 5 0.5V
VIN1 2 0 DC 2.5V
VIN2 3 0 DC 2.5V AC 1MV
*VIN 3 0

* AMPLIFIER CIRCUIT
M1 5 5 1 1 PM1 L=0.8U W=70U
M2 6 5 1 1 PM1 L=0.8U W=70U
M3 5 2 4 0 NM1 L=0.8U W=50U
M4 6 3 4 0 NM1 L=0.8U W=50U

* OUTPUT STAGE
M11 7 6 1 1 PM1 L=0.8U W=90U
M12 7 8 0 0 NM2 L=0.8U W=50U
*M121 124 8 0 0 NM0 L=0.8U W=5U
*M122 124 124 7 1 PM2 L=0.8U W=30U
*M123 0 124 7 1 PM0 L=0.8U W=250U

*BIAS CIRCUIT
M5 4 8 0 0 NM2 L=0.8U W=100U
M6 8 8 1 1 PM2 L=0.8U W=25U
M7 8 8 0 0 NM1 L=0.8U W=50U
```

```
.MODEL NM0 NMOS(LEVEL=3 LD=0.15U WD=0.3U VTO=0.73 TOX=200E-10
+ UO=520 NSUB=2.8E16 VMAX=1.35E5 ETA=0.02 THETA=0.07 KAPPA=0.1
+ DELTA=0.6 XJ=0.1U NFS=5E11 RSH=200 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=3.2E-4 CJSW=2.8E-10
+ MJ=0.95 MJSW=0.12 JS=1E-3 FC=0 PB=0.8)
* FOR W=50U SHEET RESISTANCE IS SCALED DOWN TO 1000/5=200

.MODEL NM1 NMOS(LEVEL=3 LD=0.15U WD=0.3U VTO=0.73 TOX=200E-10
+ UO=520 NSUB=2.8E16 VMAX=1.35E5 ETA=0.02 THETA=0.07 KAPPA=0.1
+ DELTA=0.6 XJ=0.1U NFS=5E11 RSH=20 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=3.2E-4 CJSW=2.8E-10
+ MJ=0.95 MJSW=0.12 JS=1E-3 FC=0 PB=0.8)
* FOR W=50U SHEET RESISTANCE IS SCALED DOWN TO 1000/50=20

.MODEL NM2 NMOS(LEVEL=3 LD=0.15U WD=0.3U VTO=0.73 TOX=200E-10
+ UO=520 NSUB=2.8E16 VMAX=1.35E5 ETA=0.02 THETA=0.07 KAPPA=0.1
+ DELTA=0.6 XJ=0.1U NFS=5E11 RSH=10 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=3.2E-4 CJSW=2.8E-10
+ MJ=0.95 MJSW=0.12 JS=1E-3 FC=0 PB=0.8)
* FOR W=50U SHEET RESISTANCE IS SCALED DOWN TO 1000/100=10

.MODEL PM0 PMOS(LEVEL=3 LD=0.0U WD=0.4U VTO=-0.9 TOX=200E-10
+ UO=180 NSUB=2.8E16 VMAX=1.9E5 ETA=0.09 THETA=0.13 KAPPA=3
+ DELTA=0.3 XJ=0.0U NFS=1E12 RSH=5.6 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=5.2E-4 CJSW=2.8E-10
+ MJ=0.5 MJSW=0.33 JS=1E-3 FC=0 PB=0.9)
*RSH IS SCALED DOWN TO 1400/250=5.6

.MODEL PM1 PMOS(LEVEL=3 LD=0.0U WD=0.4U VTO=-0.9 TOX=200E-10
+ UO=180 NSUB=2.8E16 VMAX=1.9E5 ETA=0.09 THETA=0.13 KAPPA=3
+ DELTA=0.3 XJ=0.0U NFS=1E12 RSH=20 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=5.2E-4 CJSW=2.8E-10
+ MJ=0.5 MJSW=0.33 JS=1E-3 FC=0 PB=0.9)
*RSH IS SCALED DOWN TO 1400/70=20

.MODEL PM2 PMOS(LEVEL=3 LD=0.0U WD=0.4U VTO=-0.9 TOX=200E-10
+ UO=180 NSUB=2.8E16 VMAX=1.9E5 ETA=0.09 THETA=0.13 KAPPA=3
+ DELTA=0.3 XJ=0.0U NFS=1E12 RSH=46.7 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=5.2E-4 CJSW=2.8E-10
+ MJ=0.5 MJSW=0.33 JS=1E-3 FC=0 PB=0.9)
*RSH IS SCALED DOWN TO 1400/30=46.7

*ANALYSIS
```

```
*.OP
*.TF V(7) VIN2
.AC DEC 10 1K 100E9
*.TRAN 1NS 100NS
*.PRINT tran V(7)
.PROBE
.END
```

4) 1μm CMOS Differential Amplifier with Output Stage

This circuit is to determine the performance of the CMOS amplifier using all 1μm devices.

CMOS Differential Amplifier With Output Stage L=1u @ Output Stage

```
*THIS CIRCUIT IS COMPOSED OF ALL 1μm DEVICES

VDD 1 0 DC 5V
VIN2 3 0 PWL(0 2.5V 5NS 2.5V 25NS 3.5V 30NS 3.5V 50NS 2.5V 85NS 2.5V
+ 105NS 3.5V)
*VIN2 3 0 PWL(0 2.51V 5NS 2.51V 5.01NS 2.49V 30NS 2.49V 30.01NS 2.51V
55NS
*+ 2.51V 55.01NS 2.49V 80NS 2.49V 80.01NS 2.51V 100NS 2.51V)
*VIN2 3 0 PWL(0 3.5V 5NS 3.5V 5.01NS 2.5V 30NS 2.5V 30.01NS 3.5V 55NS
*+ 3.5V 55.01NS 2.5V 80NS 2.5V 80.01NS 3.5V 100NS 3.5V)
VIN1 2 0 DC 2.5V
*VIN2 3 0 DC 2.5V AC 1MV
*.DC VIN -5 5 0.1
*VIN 3 0

* AMPLIFIER CIRCUIT
M1 5 5 1 1 PM1 L=1U W=80U
M2 6 5 1 1 PM1 L=1U W=80U
M3 5 2 4 0 NM1 L=1U W=50U
M4 6 3 4 0 NM1 L=1U W=50U

* OUTPUT STAGE
M11 7 6 1 1 PM0 L=1U W=72U
M12 7 8 0 0 NM3 L=1U W=50U

*BIAS CIRCUIT
M5 4 8 0 0 NM2 L=1U W=100U
M6 8 8 1 1 PM2 L=1U W=25U
```

```
M7 8 8 0 0 NM1 L=1U W=50U

.MODEL NM1 NMOS(LEVEL=3 LD=0.15U WD=0.3U VTO=0.73 TOX=200E-10
+ UO=520 NSUB=2.8E16 VMAX=1.35E5 ETA=0.02 THETA=0.07 KAPPA=0.1
+ DELTA=0.6 XJ=0.1U NFS=5E11 RSH=20 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=3.2E-4 CJSW=2.8E-10
+ MJ=0.95 MJSW=0.12 JS=1E-3 FC=0 PB=0.8)
* FOR W=50U SHEET RESISTANCE IS SCALED DOWN TO 1000/50=20

.MODEL NM2 NMOS(LEVEL=3 LD=0.15U WD=0.3U VTO=0.73 TOX=200E-10
+ UO=520 NSUB=2.8E16 VMAX=1.35E5 ETA=0.02 THETA=0.07 KAPPA=0.1
+ DELTA=0.6 XJ=0.1U NFS=5E11 RSH=10 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=3.2E-4 CJSW=2.8E-10
+ MJ=0.95 MJSW=0.12 JS=1E-3 FC=0 PB=0.8)
* FOR W=50U SHEET RESISTANCE IS SCALED DOWN TO 1000/100=10

.MODEL NM3 NMOS(LEVEL=3 LD=0.15U WD=0.3U VTO=0.83 TOX=200E-10
+ UO=520 NSUB=2.8E16 VMAX=1.35E5 ETA=0.02 THETA=0.07 KAPPA=0.1
+ DELTA=0.6 XJ=0.1U NFS=5E11 RSH=6.5359 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=3.2E-4 CJSW=2.8E-10
+ MJ=0.95 MJSW=0.12 JS=1E-3 FC=0 PB=0.8)
* FOR W=50U SHEET RESISTANCE IS SCALED DOWN TO 1000/153=6.5359

.MODEL PM0 PMOS(LEVEL=3 LD=0.0U WD=0.4U VTO=-0.9 TOX=200E-10
+ UO=180 NSUB=2.8E16 VMAX=1.9E5 ETA=0.09 THETA=0.13 KAPPA=3
+ DELTA=0.3 XJ=0.0U NFS=1E12 RSH=16.2 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=5.2E-4 CJSW=2.8E-10
+ MJ=0.5 MJSW=0.33 JS=1E-3 FC=0 PB=0.9)
*RSH IS SCALED DOWN TO 1400/86=16.2

.MODEL PM1 PMOS(LEVEL=3 LD=0.0U WD=0.4U VTO=-0.9 TOX=200E-10
+ UO=180 NSUB=2.8E16 VMAX=1.9E5 ETA=0.09 THETA=0.13 KAPPA=3
+ DELTA=0.3 XJ=0.0U NFS=1E12 RSH=17.5 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=5.2E-4 CJSW=2.8E-10
+ MJ=0.5 MJSW=0.33 JS=1E-3 FC=0 PB=0.9)
*RSH IS SCALED DOWN TO 1400/80=17.5

.MODEL PM2 PMOS(LEVEL=3 LD=0.0U WD=0.4U VTO=-0.9 TOX=200E-10
+ UO=180 NSUB=2.8E16 VMAX=1.9E5 ETA=0.09 THETA=0.13 KAPPA=3
+ DELTA=0.3 XJ=0.0U NFS=1E12 RSH=56 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=5.2E-4 CJSW=2.8E-10
+ MJ=0.5 MJSW=0.33 JS=1E-3 FC=0 PB=0.9)
*RSH IS SCALED DOWN TO 1400/25=56
```

```
*ANALYSIS
*.OP
*.TF V(7) VIN2
*.AC DEC 10 1K 100E9
.TRAN 1NS 100NS
.PRINT tran V(3) V(7)
.PROBE
.END
```

5) 1um CMOS Differential Amplifier using Composite Device

This circuit is to determine the performance of the CMOS amplifier using all 1μm devices except M12, which is replaced with composite device.

CMOS Differential Amplifier With Output Stage Using Composite NMOS

```
*ALL 1μm CONVENTIONAL NMOS EXCEPT M12 (COMPOSITE DEVICE)

VDD 1 0 DC 5V
VIN2 3 0 PWL(0 2.5V 5NS 2.5V 25NS 3.5V 30NS 3.5V 50NS 2.5V 85NS 2.5V
+ 105NS 3.5V)
*VIN2 3 0 PWL(0 2.51V 5NS 2.51V 5.01NS 2.49V 30NS 2.49V 30.01NS 2.51V
55NS
*+ 2.51V 55.01NS 2.49V 80NS 2.49V 80.01NS 2.51V 100NS 2.51V)
*VIN2 3 0 PWL(0 3V 5NS 3V 5.01NS 2V 30NS 2V 30.01NS 3V 55NS
*+ 3V 55.01NS 2V 80NS 2V 80.01NS 3V 100NS 3V)
*.DC VIN -5 5 0.5V
VIN1 2 0 DC 2.5V
*VIN2 3 0 DC 2.5V AC 1MV
*VIN 3 0

* AMPLIFIER CIRCUIT
M1 5 5 1 1 PM1 L=1U W=80U
M2 6 5 1 1 PM1 L=1U W=80U
M3 5 3 4 0 NM1 L=1U W=50U
M4 6 2 4 0 NM1 L=1U W=50U

* OUTPUT STAGE
M11 7 6 1 1 PM1 L=1U W=64U
*M12 7 8 0 0 NM2 L=1U W=50U
M121 124 8 0 0 NM0 L=1U W=5U
M122 124 124 7 1 PM1 L=1U W=40U
M123 0 124 7 1 PM0 L=1U W=300U
```

```
*BIAS CIRCUIT
M5 4 8 0 0 NM2 L=1U W=100U
M6 8 8 1 1 PM2 L=1U W=25U
M7 8 8 0 0 NM1 L=1U W=50U

.MODEL NM0 NMOS(LEVEL=3 LD=0.15U WD=0.3U VTO=0.73 TOX=200E-10
+ UO=520 NSUB=2.8E16 VMAX=1.35E5 ETA=0.02 THETA=0.07 KAPPA=0.1
+ DELTA=0.6 XJ=0.1U NFS=5E11 RSH=200 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=3.2E-4 CJSW=2.8E-10
+ MJ=0.95 MJSW=0.12 JS=1E-3 FC=0 PB=0.8)
* FOR W=50U SHEET RESISTANCE IS SCALED DOWN TO 1000/5=200

.MODEL NM1 NMOS(LEVEL=3 LD=0.15U WD=0.3U VTO=0.73 TOX=200E-10
+ UO=520 NSUB=2.8E16 VMAX=1.35E5 ETA=0.02 THETA=0.07 KAPPA=0.1
+ DELTA=0.6 XJ=0.1U NFS=5E11 RSH=20 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=3.2E-4 CJSW=2.8E-10
+ MJ=0.95 MJSW=0.12 JS=1E-3 FC=0 PB=0.8)
* FOR W=50U SHEET RESISTANCE IS SCALED DOWN TO 1000/50=20

.MODEL NM2 NMOS(LEVEL=3 LD=0.15U WD=0.3U VTO=0.73 TOX=200E-10
+ UO=520 NSUB=2.8E16 VMAX=1.35E5 ETA=0.02 THETA=0.07 KAPPA=0.1
+ DELTA=0.6 XJ=0.1U NFS=5E11 RSH=10 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=3.2E-4 CJSW=2.8E-10
+ MJ=0.95 MJSW=0.12 JS=1E-3 FC=0 PB=0.8)
* FOR W=50U SHEET RESISTANCE IS SCALED DOWN TO 1000/100=10

.MODEL PM0 PMOS(LEVEL=3 LD=0.0U WD=0.4U VTO=-0.9 TOX=200E-10
+ UO=180 NSUB=2.8E16 VMAX=1.9E5 ETA=0.09 THETA=0.13 KAPPA=3
+ DELTA=0.3 XJ=0.0U NFS=1E12 RSH=4.7 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=5.2E-4 CJSW=2.8E-10
+ MJ=0.5 MJSW=0.33 JS=1E-3 FC=0 PB=0.9)
*RSH IS SCALED DOWN TO 1400/300=4.7

.MODEL PM1 PMOS(LEVEL=3 LD=0.0U WD=0.4U VTO=-0.9 TOX=200E-10
+ UO=180 NSUB=2.8E16 VMAX=1.9E5 ETA=0.09 THETA=0.13 KAPPA=3
+ DELTA=0.3 XJ=0.0U NFS=1E12 RSH=17.5 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=5.2E-4 CJSW=2.8E-10
+ MJ=0.5 MJSW=0.33 JS=1E-3 FC=0 PB=0.9)
*RSH IS SCALED DOWN TO 1400/80=17.5

.MODEL PM2 PMOS(LEVEL=3 LD=0.0U WD=0.4U VTO=-0.9 TOX=200E-10
+ UO=180 NSUB=2.8E16 VMAX=1.9E5 ETA=0.09 THETA=0.13 KAPPA=3
+ DELTA=0.3 XJ=0.0U NFS=1E12 RSH=28 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=5.2E-4 CJSW=2.8E-10
```

```
+ MJ=0.5 MJSW=0.33 JS=1E-3 FC=0 PB=0.9)
*RSH IS SCALED DOWN TO 1400/50=28

*ANALYSIS
*.OP
*.TF V(7) VIN2
*.AC DEC 10 1K 100E9
.TRAN 1NS 100NS
.PRINT tran V(7)
.PROBE
.END
```

6) 1μm CMOS Differential Amplifier using 2μm Device at the Output Stage.

This circuit is to determine the performance of the CMOS amplifier using all 1μm devices except M12, which is replaces with a 2μm device.

CMOS Differential Amplifier With Output Stage L=2u @ Output Stage

```
* M12 of the Output Stage is Replaced with a L=2μm Device
VDD 1 0 DC 5V
VIN2 3 0 PWL(0 2.5V 5NS 2.5V 25NS 3.5V 30NS 3.5V 50NS 2.5V 85NS 2.5V
+ 105NS 3.5V)
*VIN2 3 0 PWL(0 2.51V 5NS 2.51V 5.01NS 2.49V 30NS 2.49V 30.01NS 2.51V
55NS
*+ 2.51V 55.01NS 2.49V 80NS 2.49V 80.01NS 2.51V 100NS 2.51V)
*VIN2 3 0 PWL(0 3.5V 5NS 3.5V 5.01NS 2.5V 30NS 2.5V 30.01NS 3.5V 55NS
*+ 3.5V 55.01NS 2.5V 80NS 2.5V 80.01NS 3.5V 100NS 3.5V)
VIN1 2 0 DC 2.5V
*VIN2 3 0 DC 2.5V AC 1MV
*.DC VIN -5 5 0.1
*VIN 3 0

* AMPLIFIER CIRCUIT
M1 5 5 1 1 PM1 L=1U W=80U
M2 6 5 1 1 PM1 L=1U W=80U
M3 5 2 4 0 NM1 L=1U W=50U
M4 6 3 4 0 NM1 L=1U W=50U

* OUTPUT STAGE
M11 7 6 1 1 PM0 L=1U W=86U
```

```
M12 7 8 0 0 NM3 L=2U W=153U

*BIAS CIRCUIT
M5 4 8 0 0 NM2 L=1U W=100U
M6 8 8 1 1 PM2 L=1U W=25U
M7 8 8 0 0 NM1 L=1U W=50U

.MODEL NM1 NMOS(LEVEL=3 LD=0.15U WD=0.3U VTO=0.73 TOX=200E-10
+ UO=520 NSUB=2.8E16 VMAX=1.35E5 ETA=0.02 THETA=0.07 KAPPA=0.1
+ DELTA=0.6 XJ=0.1U NFS=5E11 RSH=20 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=3.2E-4 CJSW=2.8E-10
+ MJ=0.95 MJSW=0.12 JS=1E-3 FC=0 PB=0.8)
* FOR W=50U SHEET RESISTANCE IS SCALED DOWN TO 1000/50=20

.MODEL NM2 NMOS(LEVEL=3 LD=0.15U WD=0.3U VTO=0.73 TOX=200E-10
+ UO=520 NSUB=2.8E16 VMAX=1.35E5 ETA=0.02 THETA=0.07 KAPPA=0.1
+ DELTA=0.6 XJ=0.1U NFS=5E11 RSH=10 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=3.2E-4 CJSW=2.8E-10
+ MJ=0.95 MJSW=0.12 JS=1E-3 FC=0 PB=0.8)
* FOR W=50U SHEET RESISTANCE IS SCALED DOWN TO 1000/100=10

.MODEL NM3 NMOS(LEVEL=3 LD=0.15U WD=0.3U VTO=0.83 TOX=200E-10
+ UO=520 NSUB=2.8E16 VMAX=1.35E5 ETA=0.02 THETA=0.07 KAPPA=0.1
+ DELTA=0.6 XJ=0.1U NFS=5E11 RSH=6.5359 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=3.2E-4 CJSW=2.8E-10
+ MJ=0.95 MJSW=0.12 JS=1E-3 FC=0 PB=0.8)
* FOR W=50U SHEET RESISTANCE IS SCALED DOWN TO 1000/153=6.5359

.MODEL PM0 PMOS(LEVEL=3 LD=0.0U WD=0.4U VTO=-0.9 TOX=200E-10
+ UO=180 NSUB=2.8E16 VMAX=1.9E5 ETA=0.09 THETA=0.13 KAPPA=3
+ DELTA=0.3 XJ=0.0U NFS=1E12 RSH=16.2 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=5.2E-4 CJSW=2.8E-10
+ MJ=0.5 MJSW=0.33 JS=1E-3 FC=0 PB=0.9)
*RSH IS SCALED DOWN TO 1400/86=16.2

.MODEL PM1 PMOS(LEVEL=3 LD=0.0U WD=0.4U VTO=-0.9 TOX=200E-10
+ UO=180 NSUB=2.8E16 VMAX=1.9E5 ETA=0.09 THETA=0.13 KAPPA=3
+ DELTA=0.3 XJ=0.0U NFS=1E12 RSH=17.5 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=5.2E-4 CJSW=2.8E-10
+ MJ=0.5 MJSW=0.33 JS=1E-3 FC=0 PB=0.9)
*RSH IS SCALED DOWN TO 1400/80=17.5

.MODEL PM2 PMOS(LEVEL=3 LD=0.0U WD=0.4U VTO=-0.9 TOX=200E-10
+ UO=180 NSUB=2.8E16 VMAX=1.9E5 ETA=0.09 THETA=0.13 KAPPA=3
```

```
+ DELTA=0.3 XJ=0.0U NFS=1E12 RSH=56 RD=0 RS=0 RG=0 RB=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=5.2E-4 CJSW=2.8E-10
+ MJ=0.5 MJSW=0.33 JS=1E-3 FC=0 PB=0.9)
*RSH IS SCALED DOWN TO 1400/25=56

*ANALYSIS
*.OP
*.TF V(7) VIN2
*.AC DEC 10 1K 100E9
.TRAN 1NS 100NS
.PRINT tran V(3) V(7)
.PROBE
.END
```