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Title A VOLTAGE-REGULATED SCR INVERTER UTILIZING CONDUCTION-ANGLE CONTROL

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This paper describes an inverter design which provides voltage regulation against variations in both the input voltage and load impedance. This design modifies the so-called parallel inverter, which consists of two silicon controlled rectifiers (SCRs) operating in a push-pull arrangement, to include a third regulating SCR. This regulating SCR is controlled by a small self-saturating magnetic amplifier which is driven by a low-voltage winding of the inverter output transformer. The regulating SCR reduces the conduction angle of each of the parallel-connected SCRs to something less than the normal 180° conduction angle in order to maintain the output voltage constant.

The regulating circuitry also reduces the harmonic distortion of the output waveform. Mathematical equations are given which relate the harmonic content of the output waveform to the conduction angle.

Circuitry is incorporated into the design to feed back reactive energy associated with the commutating elements to the dc source. This circuitry results in a considerable increase in efficiency, particularly under light load conditions.

Waveforms of the various circuit voltages and currents are plotted on the same time base to clarify the regulating mode. Curves are plotted of the output voltage, efficiency and percent harmonic distortion as a function of the load and the input voltage.

A VOLTAGE-REGULATED SCR INVERTER UTILIZING CONDUCTION-ANGLE CONTROL

by

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INTRODUCTION

The invention of the mercury vapor lamp by Hewitt shortly after the turn of the twentieth century presented the electrical industry with the first practical device for efficiently converting large blocks of electrical energy by non-mechanical means. The relatively low anode-to-cathode voltage drop together with the capability of heavy, unilateral current conduction suggested the application of the device for power rectification.

With the introduction of the third electrode, the control grid, the controlled rectifier came into being. It then became feasible to reverse the process of rectification and convert large blocks of dc energy to ac energy. Alexanderson, the man to whom the invention of the first electronic dc to ac scheme has been attributed, grouped the general family of energy conversion schemes under the title "electronic power converter" (2). It has become common practice in the recent literature to be more definitive; units of equipment used to convert dc power to dc power at a different voltage level have been termed converters; units of equipment used to convert dc power to ac power have been termed inverters. This paper will be concerned only with the inverter.

The first paper devoted to the inverter was written by Prince over forty years ago (12). As a natural consequence of his investigations of rectifying circuits using the controlled rectifier, he described the process whereby the rectification operation was "inverted" to yield the electronic inverter. This initial application utilized a dc generator to drive the static inverter, with a synchronous machine as the load.

Tompkins gave a qualitative analysis of the parallel inverter with resistance load in which an extensive number of oscillograms were displayed of the currents and voltages in the various branches of the inverter (18).

Wagner wrote two papers which have become classics in the inverter literature (23, 24). He gave a very complete analysis of the parallel inverter with resistance load in the first paper and with inductive load in the second paper. An important characteristic calculated by Wagner was the time available for turning off the controlled rectifiers. He developed relationships between this turn-off time and a group of parameters associated with the inverter circuit. These parameters included the frequency of operation, the magnitude and phase of the load impedance, and the value of the commutating capacitance. The relationships could be used to determine the value of commutating capacitance required for a given load and frequency of operation, in order to insure an adequate turn off time.

Little progress of consequence took place in inverter circuit development during the two decades following Wagner's papers, although the power-handling capability of inverters was increased considerably during this period with the invention of the ignitron by Ludwig (22). An excellent history of the early development of electronic power conversion equipment is given by Alexanderson in his paper which was written in 1944 (2).

The announcement of the silicon controlled rectifier in 1957 was probably the single most important improvement in inverter technology since the inception of the original parallel inverter design. Initially, the silicon controlled rectifier (SCR) was used in the circuits that had been designed previously for thyratrons and ignitrons. However, designs soon appeared which capitalized on the unique advantages of the SCR. One of the most significant design improvements was that presented and analyzed in great detail by McMurray and Shattuck (7). This design featured circuitry capable of feeding back reactive energy from the load circuit to the dc source. The basic idea involved had been presented some years earlier by Lee in a patent disclosure (6); however, the paper written by McMurray and Shattuck was the first to give a complete mathematical analysis of the circuitry. It was also the first to take advantage of the considerable reduction in the size of the commutating components which the feedback circuitry made possible. A description of this circuit will be given later.

Although many papers have appeared in the literature which describe schemes for utilizing the SCR in a variety of inverter configurations, comparatively few provide a means for regulating or actively filtering the output voltage. It is felt that those designs which do provide regulation and active filtering suffer serious shortcomings such as lack of efficiency, complexity or the need for special power supplies (8, 10, 14, 19, 20).

This paper describes an inverter design which provides voltage regulation against variations in both the input voltage and load impedance. This design modifies the so-called parallel inverter, to include a third regulating SCR. The regulating SCR reduces the conduction angle of each of the parallel-connected SCRs to something less than the normal 180° conduction angle to maintain the output voltage constant. The regulating SCR is controlled by a small self-saturating magnetic amplifier which is driven by a low-voltage winding of the inverter output transformer. The regulating circuitry also reduces the harmonic distortion of the output waveform.

TRIGGER CIRCUIT

SCR Characteristics

The characteristics of the SCR switching elements have been covered in great detail in the literature (1, 3, 17). The most important of these which the typical inverter design must take into account are:

a. With no signal applied to the gate circuit, the device is capable of sustaining a high forward or inverse voltage across its anode-to-cathode terminals with essentially no current conduction.

b. With the anode voltage more positive than that of the cathode, a gate trigger current of approximately 20 milliamperes sustained for several microseconds (depending on the nature of the load) will cause the SCR to turn ON; in this state it will conduct a current of many amperes with an anode-to-cathode voltage drop of approximately one volt.

c. Once triggered to the ON condition, the gate loses control. In order to turn the SCR OFF, the anode current must be reduced below a level defined as the holding current for an interval denoted as the turn-off time.

General Description

The trigger circuit is an adaptation of the magnetically-coupled multivibrator devised by Van Allen (21). In the hope of reducing the number of circuit components even more, an attempt was made to use the single transistor magnetically coupled oscillator reported by Chen and Schwiewe (4), but it was found too difficult to control the frequency and symmetry of the output waveform. The Van Allen circuit was found to be almost ideal as an inverter trigger oscillator. It provided square waves of output voltage, with a frequency of operation easily controlled by a low-level direct current. The symmetry of the square waves is a function of the core characteristics and the number of turns on the primary winding of the square-loop cores.

Matched Supermendur cores were used in the trigger oscillator. The extremely high saturation flux density of Supermendur allows a smaller size of core to be used for a given application and also results in fewer turns per volt in the winding design. The use of matched cores enhanced the symmetry of the oscillator square-wave output voltage.

Royer Multivibrator Circuit

Before describing the theory of operation of the Van Allen circuit, it will be helpful to consider the Royer magnetically-coupled multivibrator which is a bit simpler and hence more easily understood (13). The basic circuit is shown in Figure 1a and the square-loop core B-H curve which accounts for its novel characteristics in Figure 1b.

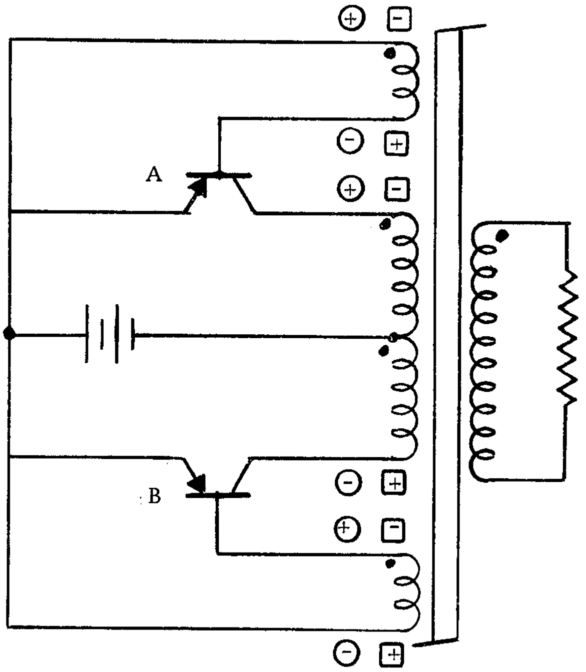


Figure 1a. The Royer Circuit

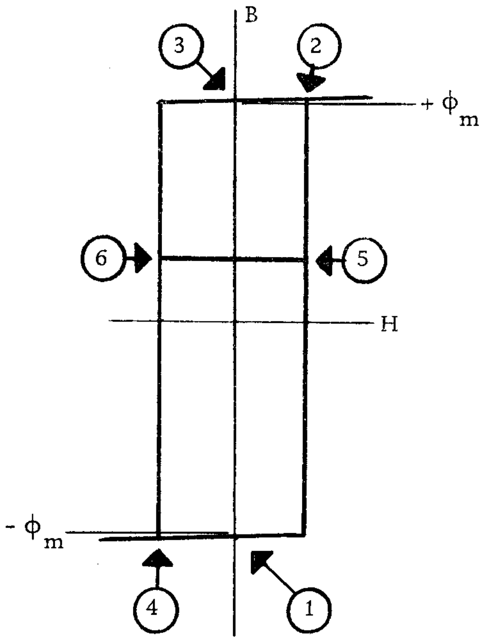


Figure 1b. B-H Loop

The transistors operate in the switching mode, being in either one of two states - saturation or cutoff. Assume that the core flux is in the state indicated by the number "1" in Figure 1b. Further assume that transistor A has just started to conduct so that the resultant magnetomotive force applied to the upper portion of the primary winding tends to move the flux to the right and upward along the B-H curve. By noting the dot phasing convention, it is apparent that the voltages in the circuit may then be described as indicated by the circled polarity marks in Figure 1a. It is also evident that the induced voltages in the base windings are such that transistor A is forward biased and transistor B reverse biased. Cumulative feedback between the collector and base windings of transistor A drives it rapidly into saturation. The operating point of the core flux then moves up the B-H curve and eventually attains the value noted by "2." At this point the rate of change of flux becomes so small that the induced voltage in the base winding of transistor A is insufficient to maintain heavy current. As the current through transistor A decreases, the flux drops back from point "2" to point "3" on the B-H curve. This represents a negative rate of change of flux which causes induced voltages in the transformer windings as indicated by the boxed-in polarity marks in Figure 1a. Under this condition, the cumulative feedback between the collector and base windings of transistor B drives it rapidly into saturation - with transistor A biased to cutoff. The magnetomotive force now causes the point of operation to move from point "3" to point "4." When the point "4" is reached, the rate of change of flux again becomes so small that the induced voltage in the base winding of transistor B is insufficient to maintain heavy current. The point of operation on the B-H curve drops back to point "1," and the entire cycle of operation continues indefinitely in a repetitive manner.

The period of oscillation of the circuit may be developed from the basic relationship involving the applied voltage, the number of primary turns and the flux:

$$e = N \frac{d\phi}{dt} \tag{1}$$

The time required for the flux to move from point "1" to point "2" on the B-H curve represents one half cycle of operation. Equation (1) may be put in the integral form as:

$$T_{\frac{1}{2}} = \Delta t = \frac{N_1}{E} \int_{-\phi_m}^{+\phi_m} d\phi = \frac{2N_1\phi_m}{E} \tag{2}$$

then $$T = 2T_{\frac{1}{2}} = \frac{4N_1\phi_m}{E} \tag{3}$$

and $$f = \frac{1}{T} = \frac{E}{4N_1\phi_m} \tag{4}$$

where f = frequency of operation

N_1 = number of primary turns

E = applied dc voltage

ϕ_m = flux value at saturation

Hence it is seen that the operating frequency is directly proportional to the applied voltage and inversely proportional to the number of primary turns and the value of flux at which saturation of the square-loop core occurs.

The Van Allen Circuit

The Van Allen circuit operates on the principle that the frequency of oscillation may be varied by controlling the flux excursion over a minor hysteresis loop. The circuit diagram of the complete trigger circuit is shown in Figure 2. It will be noted that two cores are employed in the Van Allen multivibrator circuit; it is this fact that accounts for the smooth frequency control characteristic.

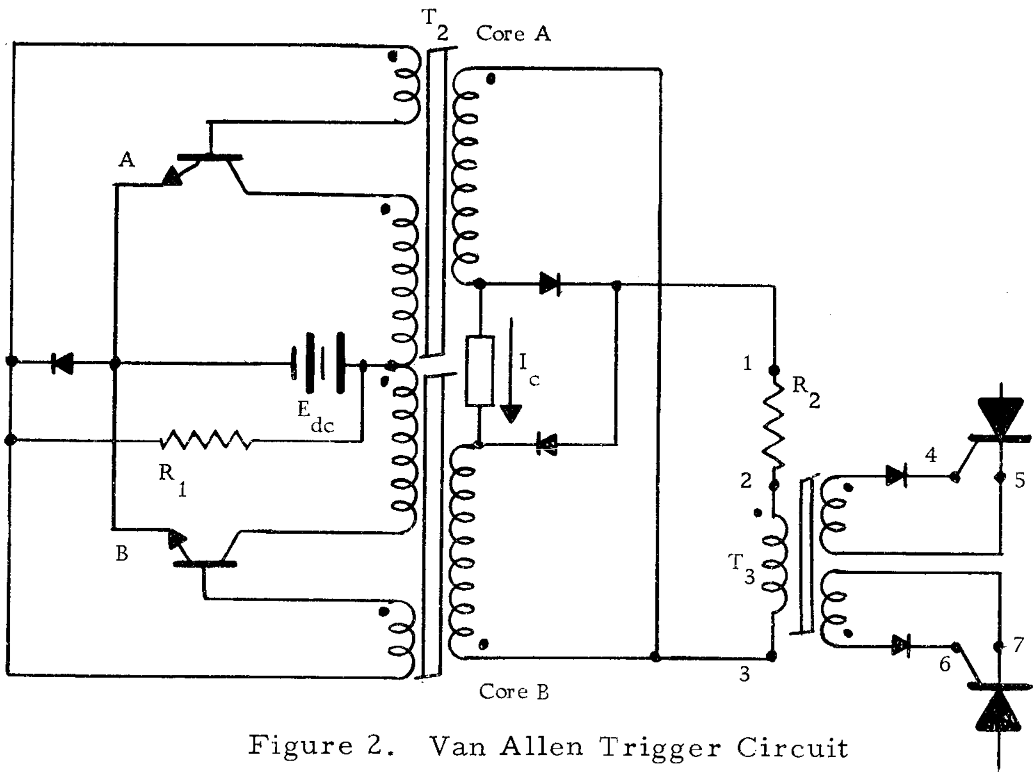


Figure 2. Van Allen Trigger Circuit

The mode of operation is similar to that of the Royer circuit, except that the flux values do not make the transition from $-\phi_m$ to $+\phi_m$. Rather, the operating point moves along a minor loop as indicated by the path 1-5-6-4-1 in Figure 1b. Further, while transistor A is in saturation, the control winding is operating on core B and resetting it to the appropriate level. Conversely, when transistor B is in saturation, the control winding is operating on core A and resetting it to the appropriate level.

It will be noted that the circuit provides for a control current path through the output windings. Using this mode of operation it is possible for energy from the transistor A - core A circuit to reset the core B during the half cycle that transistor B is cutoff. Conversely, the transistor B - core B circuit will supply energy to reset core A during the half cycle that transistor A is cutoff. However, if it is desired to have the control function independent of the load circuit, it is possible to have a primary winding for T_3, a diode and a resistance in series with the load winding of each of the cores. This method requires a more complex core winding design, but it does allow the use of a single isolated control winding to reset the two cores, independent of the load.

Pulse-forming Circuit

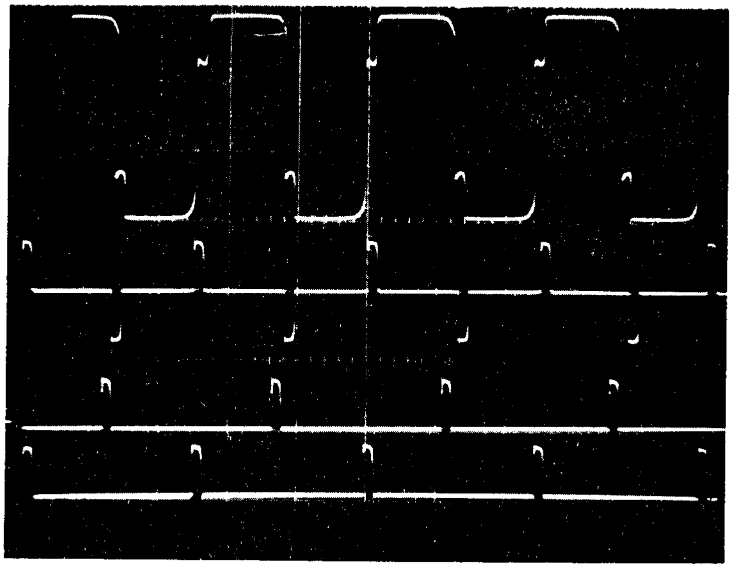
As mentioned in the discussion of triggering requirements for SCRs, it is only necessary to provide gate current pulses for a few microseconds duration to initiate conduction in the SCR anode-cathode circuit. For some inverter applications, such as the McMurray-Shattuck inverter to be described later, a square wave gate drive signal is desirable. However, for the inverter circuit developed by the writer, excessively long-duration gate currents are undesirable. Not only does the square-wave type of drive result in unnecessary temperature rise in the SCRs, but also such signals would be disastrous in a conduction-angle controlled inverter. This latter statement will be clarified in the section covering the inverter circuit.

The pulse-forming function is provided by transformer, T_3, in Figure 2. Transformer T_3 is actually a parallel-connected saturable reactor with a square-loop core characteristic as indicated in Figure 1b. When the square wave voltage from the Van Allen oscillator is first applied to the series combination of T_3 and R_2, the operating point of flux in the core of T_3 moves from point "1" to the right and upward along the vertical portion of the B-H curve. While in this mode, the law of equal ampere-turns is in effect, causing a current to be transformed into the gate circuit of the SCR. So long as R_2 is considerably greater than the dynamic impedance of the SCR gate-cathode junction as reflected into the primary circuit, the gate current is to a first approximation independent of the SCR gate-cathode impedance.

The duration of the current pulse is determined by the number of primary turns of T_3, the cross-sectional area of the core and the turns ratio of the saturable reactor. For the design described in this paper the pulse duration was chosen to be approximately 200 microseconds. The frequency of operation of the trigger circuit was

400 cycles per second.

Waveforms of the voltages between various points in the trigger circuit are shown in Figure 3. The double subscripts refer to the appropriate points in Figure 2.



V_{12} - 2 V/CM

V_{23} - 2 V/CM

V_{45} - 1 V/CM

V_{67} - 1 V/CM

Figure 3. Trigger Circuit Waveforms
(Sweep Speed - 1 MS/CM)

INVERTER CIRCUIT

The Basic Parallel Inverter

The basic power inversion circuit as described by Wagner is shown in Figure 4.

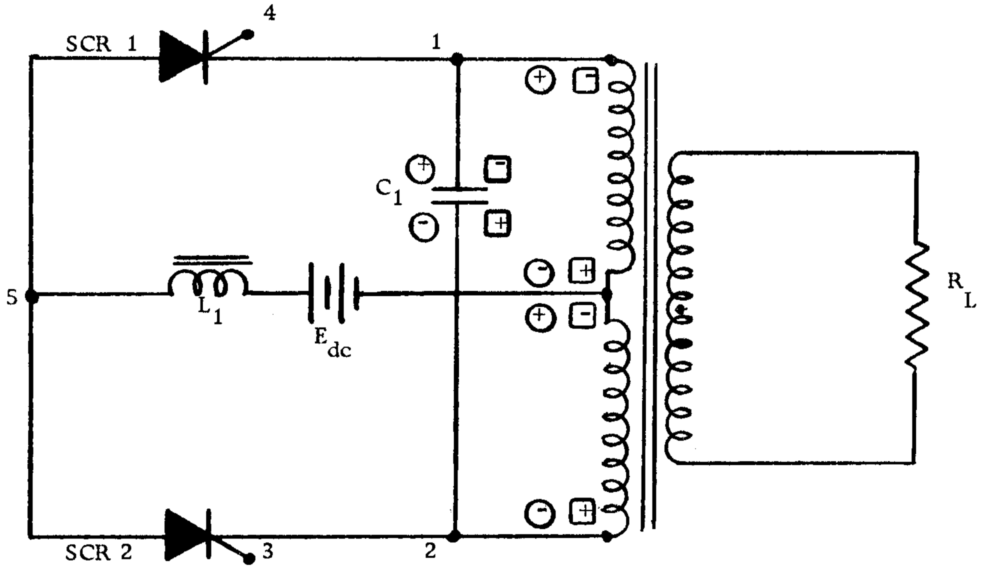


Figure 4. Basic Parallel Inverter Circuit

Capacitor C_1 is termed the commutating capacitance. Its primary purpose in the circuit is to provide a reverse bias voltage for the necessary turn-off time in order to insure that one SCR will be turned OFF when the other is triggered ON. Inductor L_1 is termed the ballast inductance. Its primary purpose is to maintain the current to the push-pull SCRs constant during the switching interval.

The commutating capacitance and the ballast inductance also provide some wave shaping of the output voltage. Although the output voltage of the basic inverter tends to approach a square waveform, Wagner has pointed out that by a suitable choice of elements L_1 and C_1 the output waveform more closely approximates a sinusoid (23).

Figure 5 illustrates typical waveforms of the voltages present in the basic inverter circuit. The voltages are shown to the same time scale and the double subscripts refer to the appropriate points in Figure 4. Reference to the waveforms shown will assist in understanding the circuit description which follows.

V_{12} - 20 V/CM

V_{51} - 20 V/CM

V_{41} - 1 V/CM

V_{52} - 20 V/CM

V_{32} - 1 V/CM

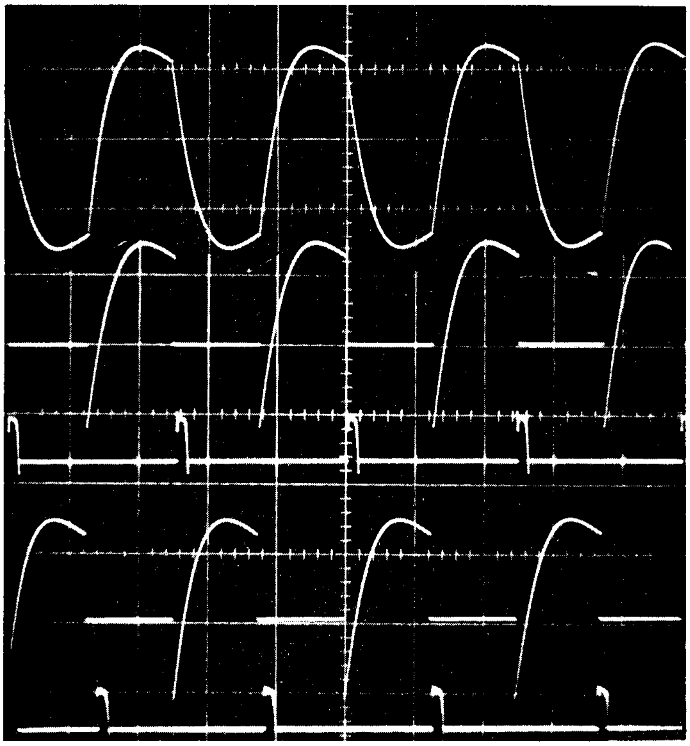


Figure 5. Inverter Voltage Waveforms

It will be assumed that trigger pulses of the proper frequency, polarity, magnitude and duration are available at the gate terminals of the two push-pull SCRs. When the trigger pulse is applied to the gate of SCR 1, it is turned ON and the voltage E is applied to terminals 1-2 of transformer T_1. By autotransformer action the voltage E is induced between terminals 2-3 of T_1 and the voltage across capacitor C_1 is 2E volts. The polarities of the appropriate voltages are indicated by the circled symbols in Figure 4.

If a trigger pulse is now applied to the gate of SCR 2, it will turn ON. Since the voltage across capacitor C_1 cannot change instantaneously, it will now reverse bias SCR 1 causing it to turn OFF. With SCR 2 turned ON the voltage E is applied to terminals 3-2 of T_1. Again by autotransformer action the voltage E is induced between terminals 2-1 of T_1, and again the voltage across the capacitor C_1 is 2E volts. The polarities of the appropriate voltages are now indicated by the boxed-in symbols of Figure 4.

When SCR 1 is again turned ON, C_1 reverse biases SCR 2 and turns it OFF, with SCR 1 again conducting fully. This sequence of operation continues repetitively so long as the proper trigger pulses are applied to the SCR gate terminals.

The McMurray-Shattuck Inverter

The parallel inverter circuit of Figure 4 suffers from the disadvantage that its commutating capacitance must be chosen large enough to insure adequate turn-off time under the worst load condition. An improved inverter circuit which eliminates the dependency of the required turn-off time upon the power factor of the load is shown in Figure 6. This circuit will hereafter be referred to as the McMurray inverter.

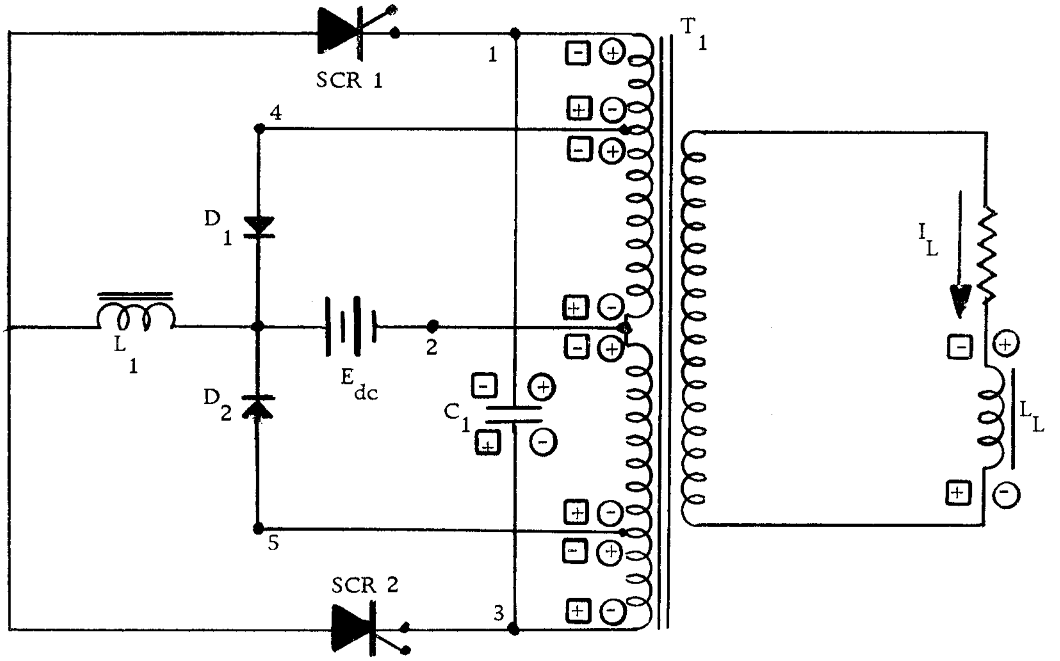


Figure 6. McMurray Parallel Inverter

It can be seen that the McMurray circuit differs from the basic inverter circuit only in that it includes feedback diodes connected from taps on the transformer primary to the dc source. This simple revision, however, completely alters the operation of the circuit. The diodes provide a path for the reactive load current and allow reactive energy to be returned to the dc source. The net results are that the circuit efficiency is considerably improved and that the necessary value of commutating capacitance is considerably reduced.

Assume that SCR 1 has been triggered ON, that the current direction through the load impedance is as shown and that the polarities of circuit voltages are as indicated by the encircled symbols.

When SCR 2 is triggered ON, the voltage across C_1, which cannot change instantaneously, reverse biases SCR 1 and turns it OFF. Since the energy stored in L_1 and L_L cannot change instantaneously, the currents in each of these elements must be maintained at the instant that the commutation operation takes place. When the current in the load impedance starts to decrease, a voltage will be induced in L_L which is proportional to the rate of change of load current. L_L, acting as a voltage source, establishes induced voltages in the inverter circuit as shown by the boxed-in symbols of Figure 6. The polarity of the induced voltage between terminals 2-5 of T_1 is such that if the voltage induced tends to exceed the value E_{dc}, diode D_2 will conduct and feed energy back to the voltage source E_{dc}. This action will clamp the voltage between terminals 2-5 of T_1 to E_{dc} volts. It can be seen that the magnitude of voltage between terminals 3-2 of T_1 will be greater than E_{dc} and of polarity which will reverse bias SCR 2. Thus SCR 1 and SCR 2 are both turned OFF; it is necessary to apply a trigger pulse to the gate of SCR 2 again at this time to turn it back ON and continue the inverter action. In practice, a square wave of voltage is maintained between the gate-to-cathode circuit of the SCRs at all times. The square-wave signal forward biases the gate during the half cycle it is to conduct, and reverse biases the gate during the half cycle it is to be OFF.

Although the McMurray circuit is an improvement upon the basic parallel inverter circuit, it still suffers two major disadvantages. The first is the fact that the inverter is not regulated and hence has an output voltage which varies greatly with variations in input voltage and load. The second and more serious drawback is the fact that the output waveform is essentially a square wave and requires extensive filtering to yield the sinusoidal waveform often required at the inverter output.

This explanation of the McMurray inverter has, admittedly, been brief; for additional details of the circuit operation which have been omitted, the reader is referred to the paper by McMurray and Shattuck (7).

An Improved Inverter

The inverter circuit which has been designed by the writer is shown in Figure 7.

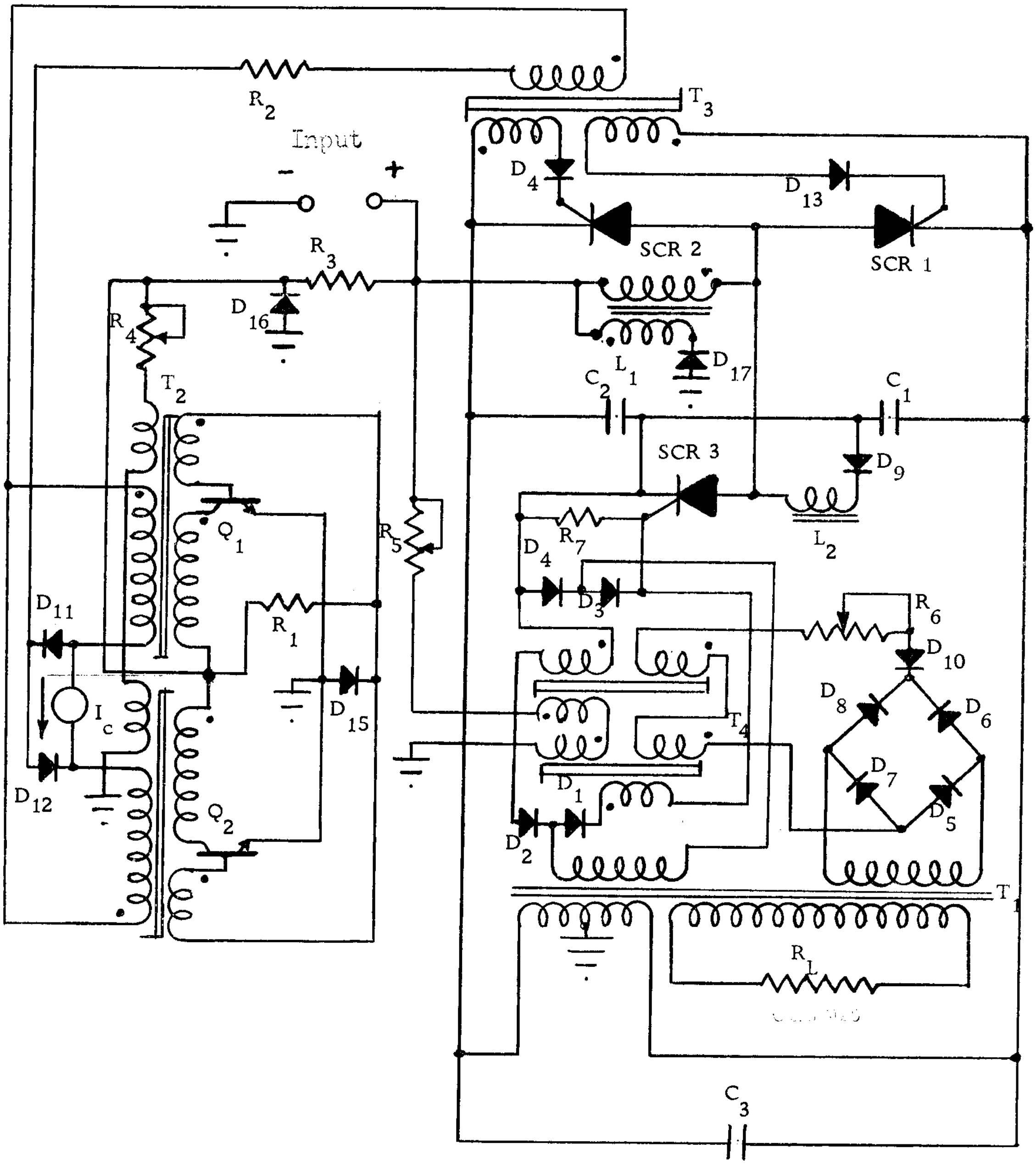


Figure 7. Voltage Regulated Inverter Circuit

The design is relatively simple. It contains a total of only two transistors and only three SCRs. The design is extremely flexible in that the same trigger and regulating circuits can be used with a variety of output power levels. Throughout the design advantage has been taken of recent advances in transformer core materials. Wherever possible high permeability, grain-oriented ferro-magnetic core materials have been used. The use of these materials, particularly in the trigger circuitry and the regulating circuitry, has resulted in a good compromise among the factors of size, reliability, efficiency and cost.

Magnetic Amplifier Control Circuitry

Before attempting to explain the complete regulated power inversion process, the self-saturating magnetic amplifier which controls the regulating operation will be discussed. The circuit diagram for such a magnetic amplifier is shown in Figure 8. The configuration offers a number of advantages as an SCR control device:

a. The firing angle may be conveniently controlled over the 180° half cycle.

b. The magnetic amplifier output waveform has a very steep leading edge.

c. Electrical isolation is easily attained.

d. The circuitry is simple, rugged and reliable.

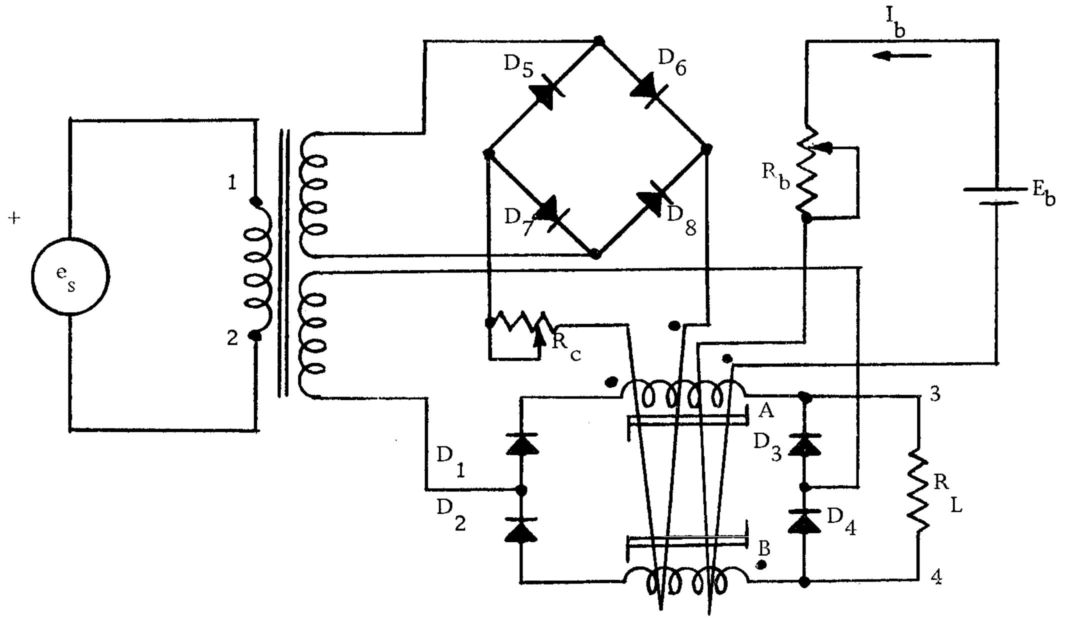


Figure 8. A Self-saturating Magnetic Amplifier

Cores A and B in Figure 8 are Deltamax tape wound toroidal cores, with B-H characteristics as shown in Figure 1b. The Deltamax material was selected because of its high saturation flux density, low coercive force and squareness of its hysteresis loop. The high saturation flux density results in fewer turns per volt for a given gate winding. The low coercive force results in higher gain (lower required control current) and greater efficiency. The squareness of the hysteresis loop results in a steeper leading edge on the output wave form.

The operation of the magnetic amplifier is dependent upon the same basic equation used for the trigger circuit (see Equation (1), Section II). With diodes D_1 and D_2 in series with each of the cores A and B, respectively, it can be seen that only positive half-cycles of e_s will be applied to core A and only negative half-cycles of e_s will be applied to core B. With the bias current and the control current equal to zero, so long as

$$\frac{e_s}{R_L} > I_x = \frac{H_c L}{N_1} \tag{5}$$

where e_s = the instantaneous value of the voltage

L = the mean length of the core

R_L = the load resistance

H_c = the coercive force for the core

N_1 = number of gate winding turns

then the flux in both cores A and B will be in the saturation state and the gate windings will sustain no voltage. If the signal voltage, e_s, is sinusoidal, the idealized output will be a full wave rectified waveform; this, of course, assumes that the current in the bias winding and the current in the control winding are zero (16).

If a dc voltage is applied to the bias winding with the phasing noted, the resulting current in the bias winding of the magnetic amplifier will have a resetting action on the flux in each of the cores; this resetting action takes place in each of the cores during the half cycle of applied voltage that is blocked by diodes D_1 and D_2, respectively. The resulting output voltage is inversely proportional to the value of the bias current; that is, when the bias current is zero, the output voltage is a maximum and when the bias current is of sufficient magnitude, the output voltage is zero. Figure 9 shows oscillograms of the output waveform for four different conditions of bias current.

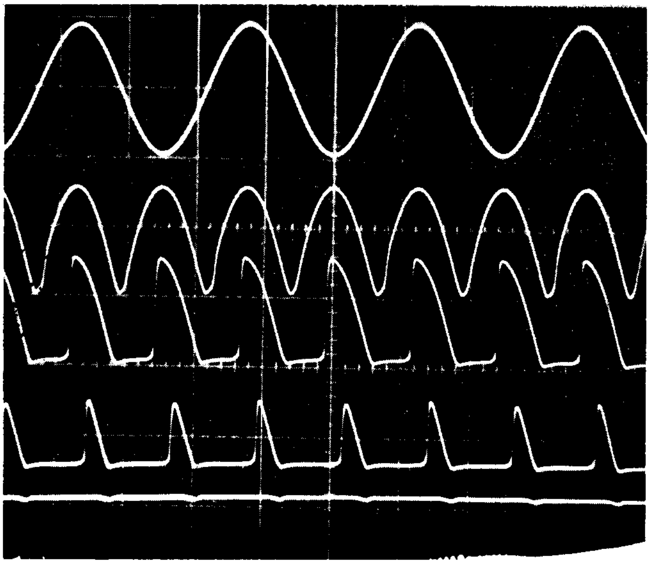


Figure 9. Magnetic Amplifier Waveforms
(Sweep Speed - 1 MS/CM)

Assume now that the bias current is set so that the magnetic amplifier conduction angle is approximately 25° with no control current. Further assume that it is desired to control the magnetic amplifier output so that the conduction angle is directly proportional to the ac input voltage; that is, if the ac input voltage rises, the conduction angle increases. The natural characteristic of the magnetic amplifier tends to accomplish this action even with no control current present. This is due to the fact that the volt-second area absorbed by the magnetic amplifier tends to be constant for a given bias and control current. If the ac input voltage should increase, the conduction angle of the output waveform must also increase since the volt second area of the absorbed voltage is constant. Unfortunately, this corrective action is insufficient for the regulating application.

The proper regulating action may be obtained by providing a control current which exhibits a large percentage increase for a small percentage increase in the voltage which drives the magnetic amplifier. A control current with this characteristic may be obtained by the bridge rectifier-zener diode circuit shown in Figure 8. It should be noted that the phasing of the control winding is such that the effect of the control current opposes the effect of the bias current; that is, an increase in the control current increases the conduction angle of the magnetic amplifier output voltage. By proper selection of the number of turns on the winding feeding the bridge rectifier and proper selection of the breakover voltage of zener diode D_9, the conduction angle of the magnetic amplifier can be smoothly controlled from essentially 25° to 180° for any reasonable change in the transformer output voltage.

The above mode of operation is typical of that used in the regulating circuit of the inverter. The control winding senses the magnitude of the inverter output voltage; the resulting control current varies the conduction angle of the magnetic amplifier output; and the magnetic amplifier output triggers the regulating SCR in such a manner that it cuts off SCR 1 and SCR 2 prematurely if the inverter output voltage tends to rise above a preselected level.

Power Conversion Circuit

A simplified schematic of the improved inverter circuit is shown in Figure 10. It can be seen that the major difference between this circuit and the basic parallel inverter circuit is in the use of the center-tapped commutating capacitance and the addition of the third SCR. These additions, however, alter the normal inversion process in a manner that allows the conduction angle of each of the push-pull SCRs to be easily controlled. The magnetic amplifier control circuitry, which has been previously described, has been replaced in the simplified circuit by the block termed the Output Sensing Circuit.

When the first trigger pulse is applied to the gate circuit of SCR 1, it is turned ON. The equivalent circuit during the interval that SCR 1 conducts consists of the ballast inductance connected in series with the parallel combination of the commutating capacitance and the load resistance referred to the primary of the transformer. The circuit elements are such that an under-damped condition exists so that the peak voltage applied between terminals 1-2 of T_1 is considerably greater than the dc supply voltage E_{dc}. This same voltage is transformed across the other windings of T_1 with the polarities as indicated by the encircled symbols of Figure 10.

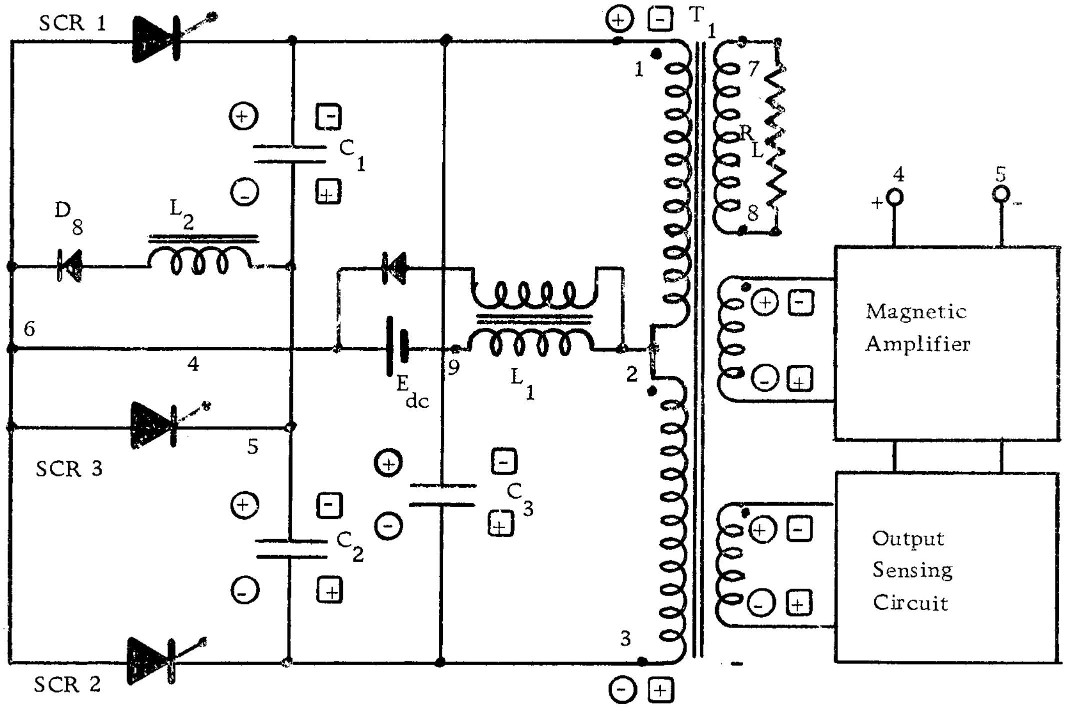


Figure 10. Simplified Inverter Schematic

If the output voltage is within the design tolerance, the Output Sensing Circuit will be inactive and no control current will flow. However, the bias current to the magnetic amplifier is set such that the magnetic amplifier will saturate after SCR 1 has conducted for approximately 155° of its possible 180° half cycle. The magnetic amplifier will then trigger SCR 3 to the ON condition. The voltage across C_1, which cannot change instantaneously, reverse biases SCR 1 and turns it OFF.

The equivalent circuit during the interval that SCR 3 conducts is different from that when SCR 1 conducts. The circuit consists of the series combination of the ballast inductance, the center-tapped commutating capacitance and the effective value of the load resistance as reflected into the primary circuit of the transformer. Qualitatively, it can be seen that the circuit is a series resonant circuit with a frequency of oscillation determined primarily by L_1 and C_1. The amount of damping, and the corresponding peak voltage rise across L_1 and C_1, are dependent on the value of load resistance R_L. This voltage rise is limited by the feedback winding on L_1 which clamps the secondary voltage on the feedback winding to the dc source voltage E_{dc} and feeds the energy stored in the ballast inductance L_1 back into E_{dc}. The action of the feedback winding of L_1 is similar to the diode feedback arrangement in the McMurray circuit. In the present case, however, the energy returned to the dc source is the reactive energy stored in the commutating elements rather than in the load as is the case in the McMurray circuit.

Since the values of L_1 and C_1 are chosen to yield a resonant frequency considerably higher than the inverter output frequency (400 cycles per second), capacitance C_1 is charged to its peak voltage in a small fraction of a complete cycle. When the current through SCR 3 approaches zero, SCR 3 cuts OFF. All three SCRs are now OFF.

The charge which had accumulated on C_1, C_2 and C_3 during the interval that SCR 1 had been conducting continues to discharge through the load resistance R_L. Before this discharge is completed, the trigger circuit feeds a positive pulse to the gate of SCR 2, turning it ON. If SCR 3 had not already been turned OFF by natural circuit action, it would now be turned OFF due to the reverse bias effect of the voltage on C_2. The equivalent circuit with SCR 2 conducting is the same as it had been with SCR 1 conducting. However, the polarities of voltages in the circuit with SCR 2 conducting are indicated by the boxed-in polarity symbols in Figure 10.

Assuming that the output voltage is still within design tolerance, the Output Sensing Circuit will be inactive and again no control current will flow. The bias current of the magnetic amplifier is again set such that the amplifier will saturate after SCR 2 has conducted for approximately 155° of its possible 180° half cycle. The magnetic amplifier will then trigger SCR 3 to the ON condition. The voltage across C_2, which cannot change instantaneously, reverse biases SCR 2 and turns it OFF. The equivalent circuit during the interval that SCR 3 conducts is the same as it had been when SCR 3 conducted in the previous half cycle; however, capacitance C_2 now assumes the role previously filled by capacitance C_1. Again the resonant charging action will charge C_2 rapidly, the feedback winding on L_1 will come into play, and the reactive energy in the ballast inductance will be returned to the dc source. All three SCRs will return to the

OFF condition. A positive pulse will again trigger SCR 1 ON and the entire sequence of events as described previously will continue repetitively so long as the output voltage of the inverter remains within the design tolerance.

Let it now be assumed that either the input voltage has been raised or that the load resistance has been increased - tending to cause an increase in the output voltage. With SCR 1 triggered ON the initial sequence of events will be the same as above. However, with the output voltage attempting to rise, the Output Sensing Circuit will feed a control current, proportional to the increase in the output voltage, to the magnetic amplifier which in turn increases the conduction angle of the amplifier output. This causes it to trigger SCR 3 ON sooner than previously. When SCR 3 is triggered ON it, in turn, causes whichever of the push-pull SCRs is conducting to turn OFF prematurely. This corrective action will tend to hold the output voltage constant. It can be seen qualitatively that the conduction angle of the push-pull SCRs is inversely proportional to the output voltage, once this output voltage has exceeded the upper limit of the design tolerance.

Nothing has been said as yet about L_2 and D_8 of Figure 10. The purpose of these elements is to eliminate the excess charge which accumulates at the junction of C_1 and C_2 due to the conduction of SCR 3. It will be remembered that the regulating action turns ON

SCR 3 and causes current to flow into C_1 and C_2 unilaterally. If no path is provided for this charge accumulation, it would become impossible to trigger SCR 3 to the ON condition and the regulating action would cease.

Let it be assumed that the inverter has been operated for some time and that SCR 1 has been conducting just prior to the interval of interest. The regulating action of the Output Sensing Circuit in conjunction with the magnetic amplifier will then cause SCR 3 to conduct. The polarities of the voltages in the circuit just prior to the time that SCR 3 begins to conduct are indicated by the circled polarity marks in Figure 10. When SCR 3 conducts, the dc current into the junction of C_1 and C_2 causes an accumulation of charge to be superimposed upon that already existing as noted by the circled polarity marks. However, when SCR 2 is triggered to the ON condition it can be seen that the polarity of C_2 is such as to cause a current from the junction of C_1 and C_2 through the loop consisting of elements L_2, D_8, SCR 2 and C_2. This dc component of current compensates for the dc component of current through SCR 3 which causes the accumulation of charge at the junction of C_1 and C_2.

In a similar manner, if SCR 2 has been conducting just prior to the interval of interest, the polarity of the voltages in the circuit will be as indicated by the boxed-in symbols of Figure 10. Again when SCR 3 conducts, the dc current into the junction of C_1 and C_2

causes an accumulation of charge to be superimposed on that already existing as noted by the boxed-in polarity marks. However, when SCR 1 is triggered ON it can be seen that the polarity of voltage on C_1 is such as to cause a current from the junction of C_1 and C_2 through the loop consisting of elements L_2, D_8, SCR 1 and C_1.

Since the energy involved is relatively small, L_2 is accordingly a very small inductance. For the inverter under investigation, its weight was less than 0.75 ounces. It should be pointed out, however, that with the dc component of current that flows through L_2 it is necessary to use either a gapped-core construction or a powdered-type core.

Harmonic Reduction

The method by which the regulating circuitry controls the conduction angle of the push-pull connected SCRs to maintain the inverter output voltage constant has been explained previously in this paper. In this section equations will be developed which show that the control of the conduction angle serves the further purpose of reducing the harmonic content of the output waveform.

It would be possible to determine the Fourier series for the actual inverter output waveform with any given load impedance. It can be seen that the output waveform always exhibits half-wave symmetry in the steady state and that a half period is composed of two exponential factors. However, this analysis would be somewhat complex in that the boundary conditions would change for each value of the conduction angle.

Since it is the purpose of this section to show the advantage of the active filtering of the regulating circuit, the development which follows will disregard the passive filtering action contributed by the ballast inductance and the commutating capacitance. It can be seen qualitatively that the ballast inductance and commutating capacitance will tend to prevent sudden changes in the leading and lagging edges of the output voltage waveform; hence the harmonic content of the actual output waveform will always be less than the value to be developed.

The idealized quasi-square waveform of a conduction-angle controlled inverter output is shown in Figure 11. With the zero time base reference as indicated, it is evident that the waveform is an odd function with half-wave symmetry. In conducting a Fourier analysis of the waveform it is evident that the series contains only odd harmonics, only sine terms and that to determine the Fourier coefficients it is only necessary to integrate from zero to $\frac{\pi}{2}$ and multiply by four (15).

Performing the Fourier analysis to determine the coefficients of the infinite series

$$b_n = \frac{4}{\pi} \int_0^{\frac{\pi}{2}} f(x) \sin nx \, dx \tag{6}$$

$$= \frac{4E}{\pi} \left[\int_0^{\theta} (0) \sin nx \, dx + \int_{\theta}^{\frac{\pi}{2}} \sin nx \, dx \right] \tag{7}$$

$$= \frac{4E}{n\pi} \left[- \cos nx \Big|_{\theta}^{\frac{\pi}{2}} \right] \tag{8}$$

$$= \frac{4E}{\pi n} \cos n\theta, \text{ for all odd n numbers} \tag{9}$$

The resulting Fourier series is

$$e_t = \frac{4E}{\pi} \left[\cos \theta \sin wt + \frac{\cos 3\theta}{3} \sin 3 wt + \frac{\cos 5\theta}{5} \sin 5wt + \frac{\cos 7\theta}{7} \sin 7wt + \ldots \right] \tag{10}$$

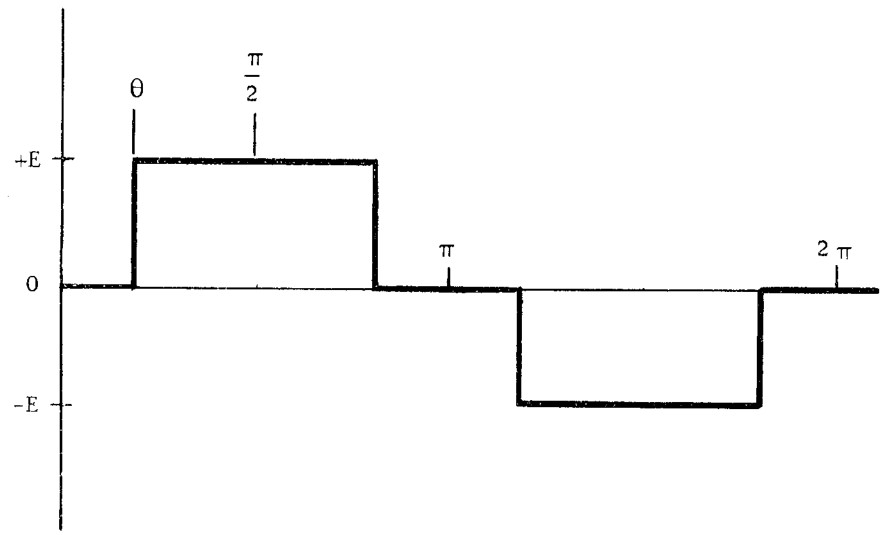


Figure 11. Idealized Quasi-square Waveform

It is evident that the root mean square (rms) value of the fundamental component can be made any value desired by a suitable choice of E and θ; however, to reduce the complexity of the additional filtering circuitry necessary to eliminate the predominant harmonics it would be desirable to select E and θ so as to reduce the predominant harmonics. For example, if one were to make θ equal 30°, the third and ninth harmonics would be eliminated and the fifth and seventh would be reduced by 13%. It can be shown that the total harmonic distortion is a minimum for value of θ approximately equal to 25°. However, since in the inverter application θ will vary as a function of both the input dc voltage and the load, the angle will be set equal to approximately 25° at full rated load and nominal input voltage and will be allowed to make whatever excursion is necessary to maintain the output voltage essentially constant as the input voltage and load are varied.

As a consequence of the active filtering covered above plus the passive filtering of the ballast inductance and the commutating capacitance, the total harmonic distortion of the output waveform may be held considerably below ten percent for an appreciable range of input dc voltage and load resistance. For applications requiring a value of harmonic distortion lower than five percent it will be necessary to provide additional passive filtering.

Ott has provided a filter design for a square-wave type inverter which provides excellent harmonic reduction with a four element filter (11). At the same time it provides regulation against variations in the load and, in addition, provides a filter input impedance that is capacitive over the normal range of load. Design equations for determining the values of the four elements which make up the Ott filter are provided in reference (5). These equations assume an input waveform that is a square wave. Consequently, the component values are much larger than necessary for an output such as that provided by the improved inverter described in the body of this paper. Although no attempt was made to use additional passive filtering, it is likely that a filter of the Ott type with reduced component sizes could be utilized to reduce the harmonic distortion well below five percent over the normal variation in input dc voltage and load impedance.

EXPERIMENTAL RESULTS

Instrumentation

In the sections which follow, oscillograms of the waveforms which appear in the improved inverter circuit are presented, along with graphs showing the regulation, efficiency and harmonic distortion as a function of the input voltage and load resistance.

The oscillograms were obtained by use of a Tektronix Model C-12 Camera in conjunction with a Tektronix Model 502 Dual Beam Oscilloscope.

A Heathkit Model IP-10 transistorized power supply was used to obtain the data on regulation, efficiency and harmonic distortion. Due to the power limitation of this supply it was only possible to operate the inverter at a power level of approximately 40 to 55 watts. The actual inverter design was capable of 100 watts output at an efficiency in excess of 80 percent. Although no data is provided in the paper at this power level, the inverter was operated at the 100 watt level using a Hyperion Model HY-Z1-32-5 Power Supply.

The output voltage and harmonic distortion were measured with a Hewlett Packard Model 400E Vacuum Tube Voltmeter and a Hewlett Packard Model 330D Harmonic Distortion Analyzer, respectively.

Inverter Waveforms

Waveforms of the voltages which occur in the various portions of the improved inverter circuitry are shown in Figures 12, 13 and 14 below. The oscillograms are taken with respect to the same time base and the double-subscript notation used with the voltages denotes the points in the inverter schematic of Figure 10 between which the oscillograms were recorded.

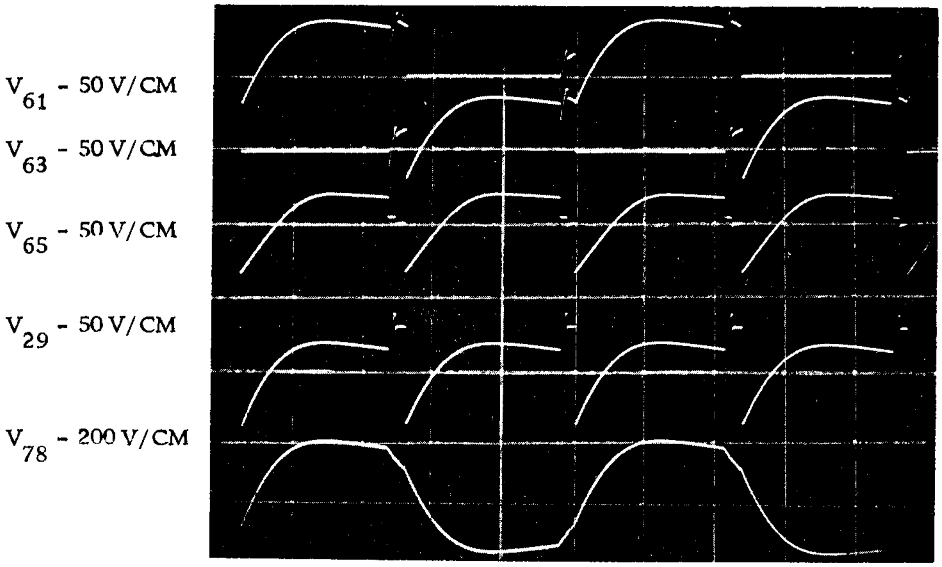


Figure 12. Voltage Waveforms - Full Load
(Sweep speed - 0.5 MS/CM)

V_{61} - 50 V/CM

V_{63} - 50 V/CM

V_{65} - 50 V/CM

V_{29} - 50 V/CM

V_{78} - 200 V/CM

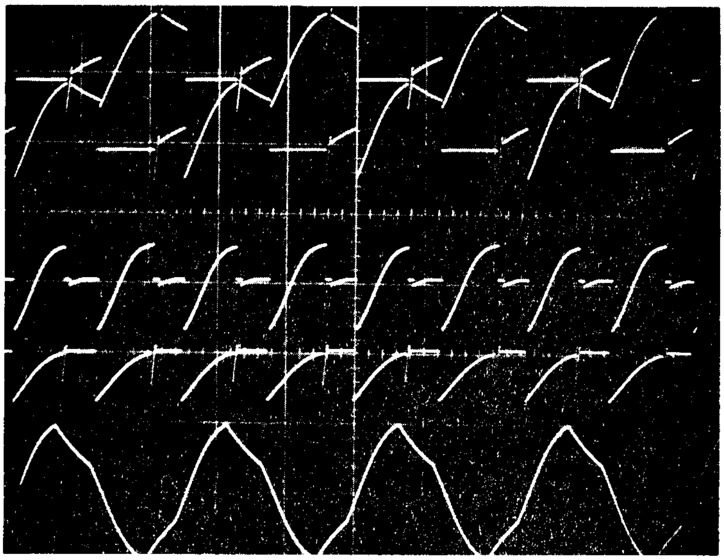


Figure 13. Voltage Waveforms - Half Load
(Sweep speed - 1 MS/CM)

V_{61} - 50 V/CM

V_{63} - 50 V/CM

V_{65} - 50 V/CM

V_{29} - 50 V/CM

V_{78} - 200 V/CM

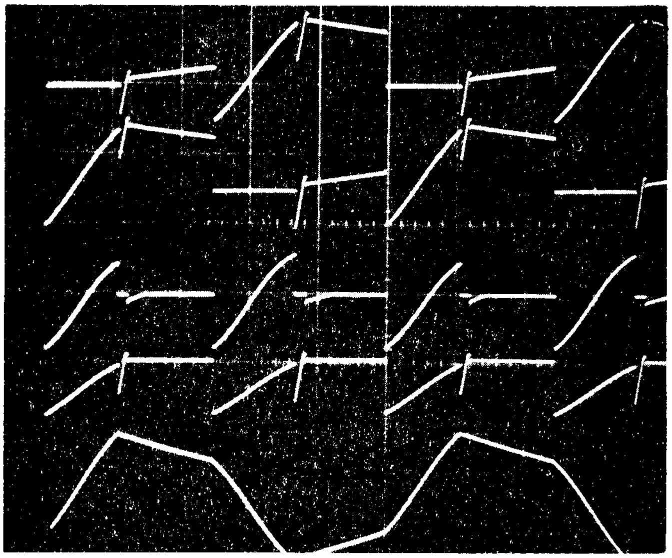


Figure 14. Voltage Waveforms - One Fourth Load
(Sweep speed - 0.5 MS/CM)

Regulation, Efficiency and Distortion

In the graphs which follow, the characteristics of the improved inverter will be compared with those of the basic parallel inverter under the same input voltage and load conditions, wherever possible. Data cannot be provided for the basic parallel inverter at the higher input voltages under light load conditions, because the transformer voltage becomes so large that saturation of its core would occur.

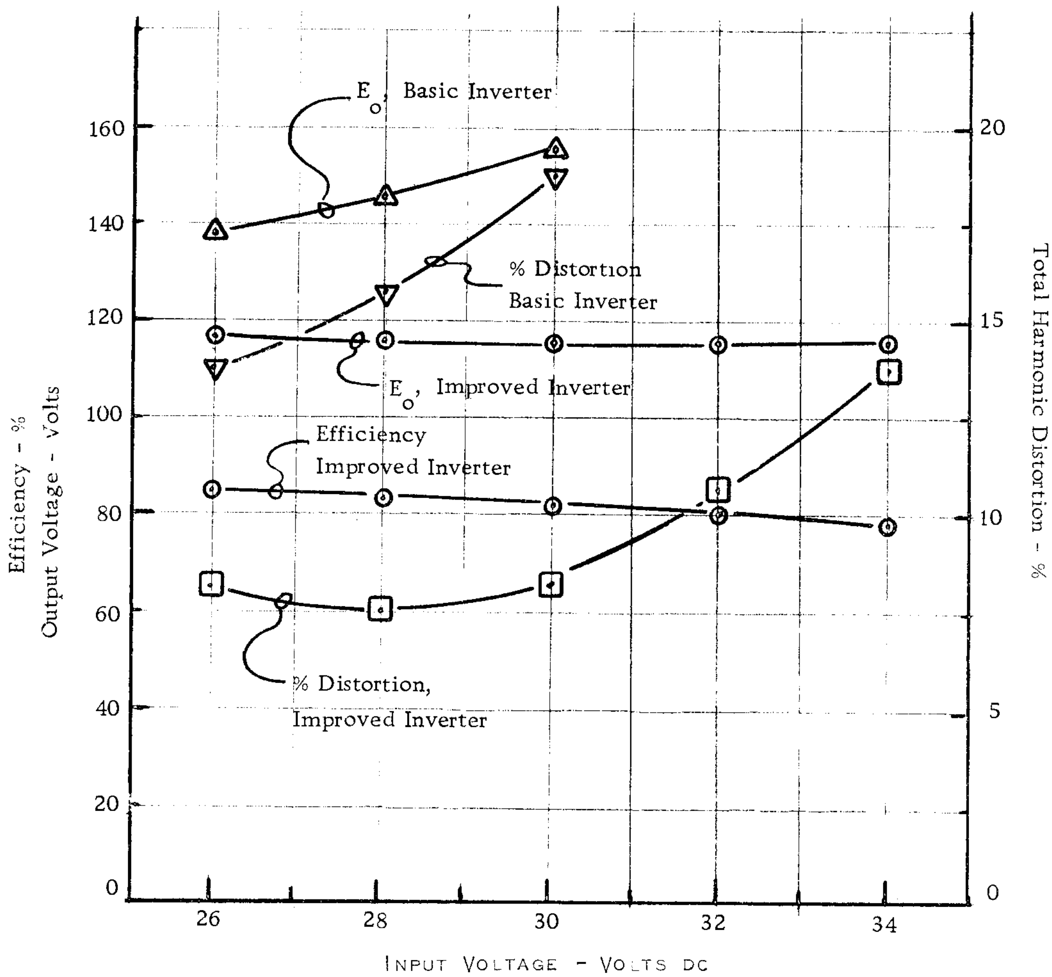


Figure 15. Regulation, Efficiency and Distortion Curves

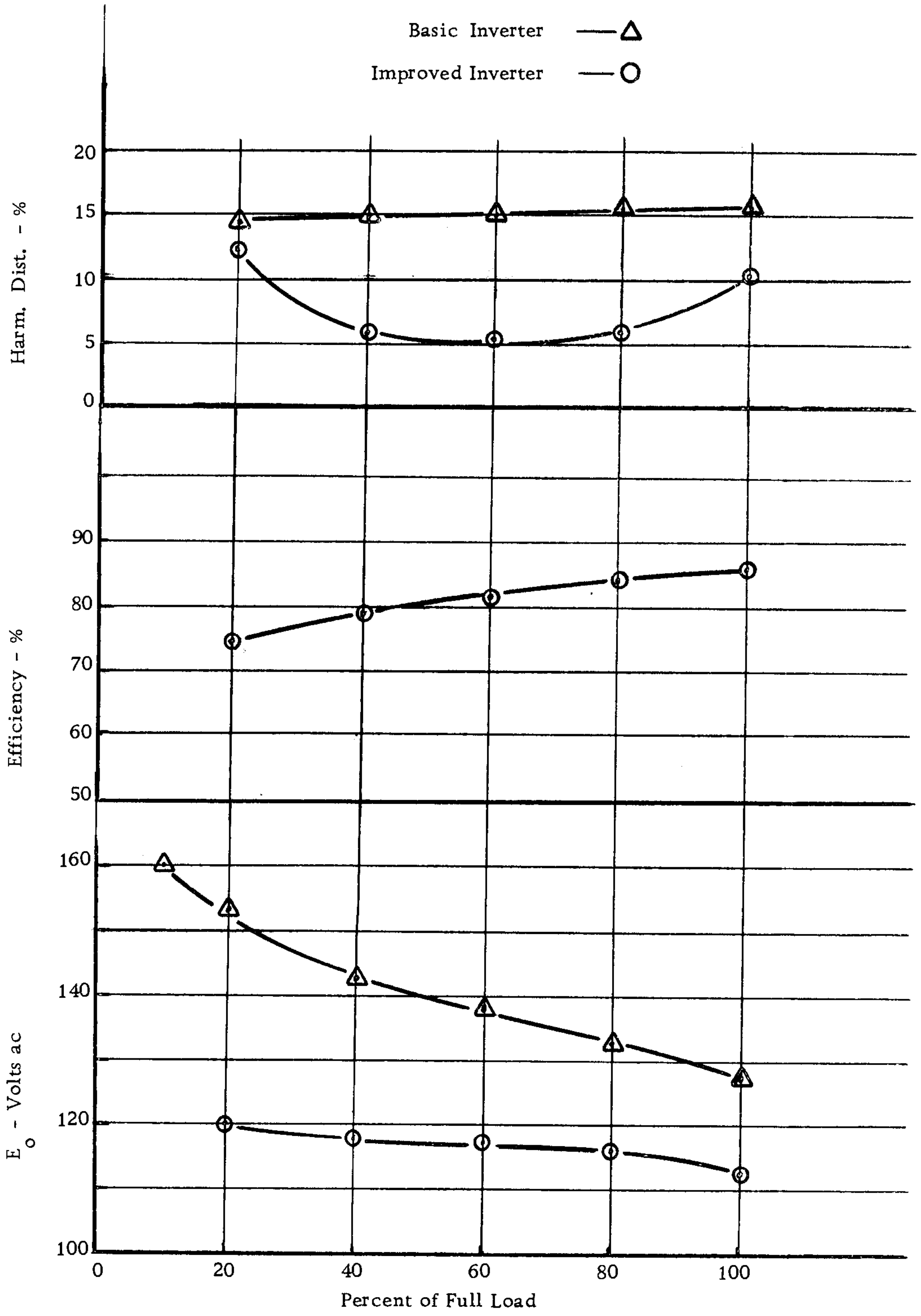


Figure 16. Output Voltage, Efficiency and Distortion (Input voltage - 26 volts dc)

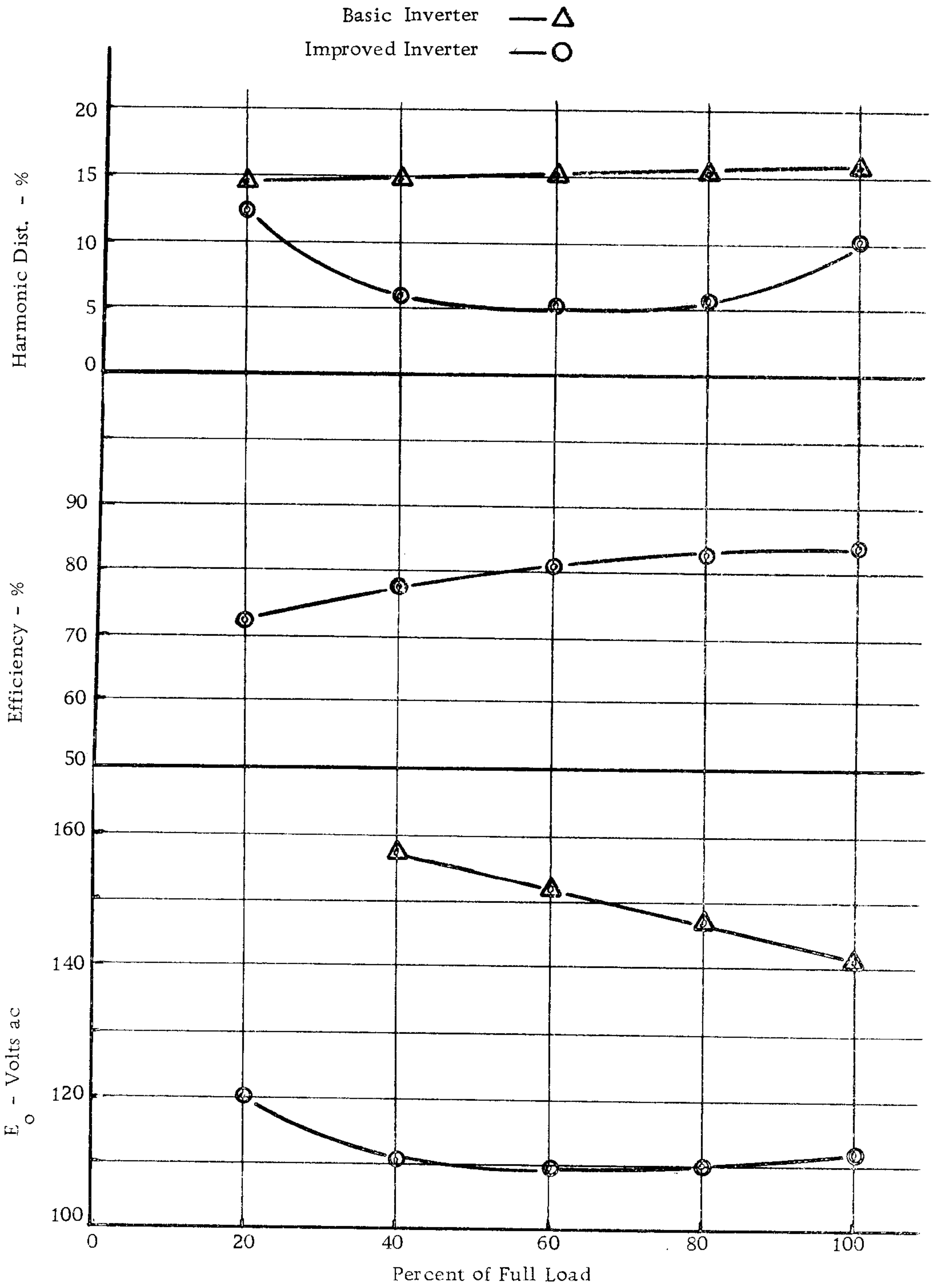


Figure 17. Output Voltage, Efficiency and Distortion
(Input voltage - 30 volts dc)

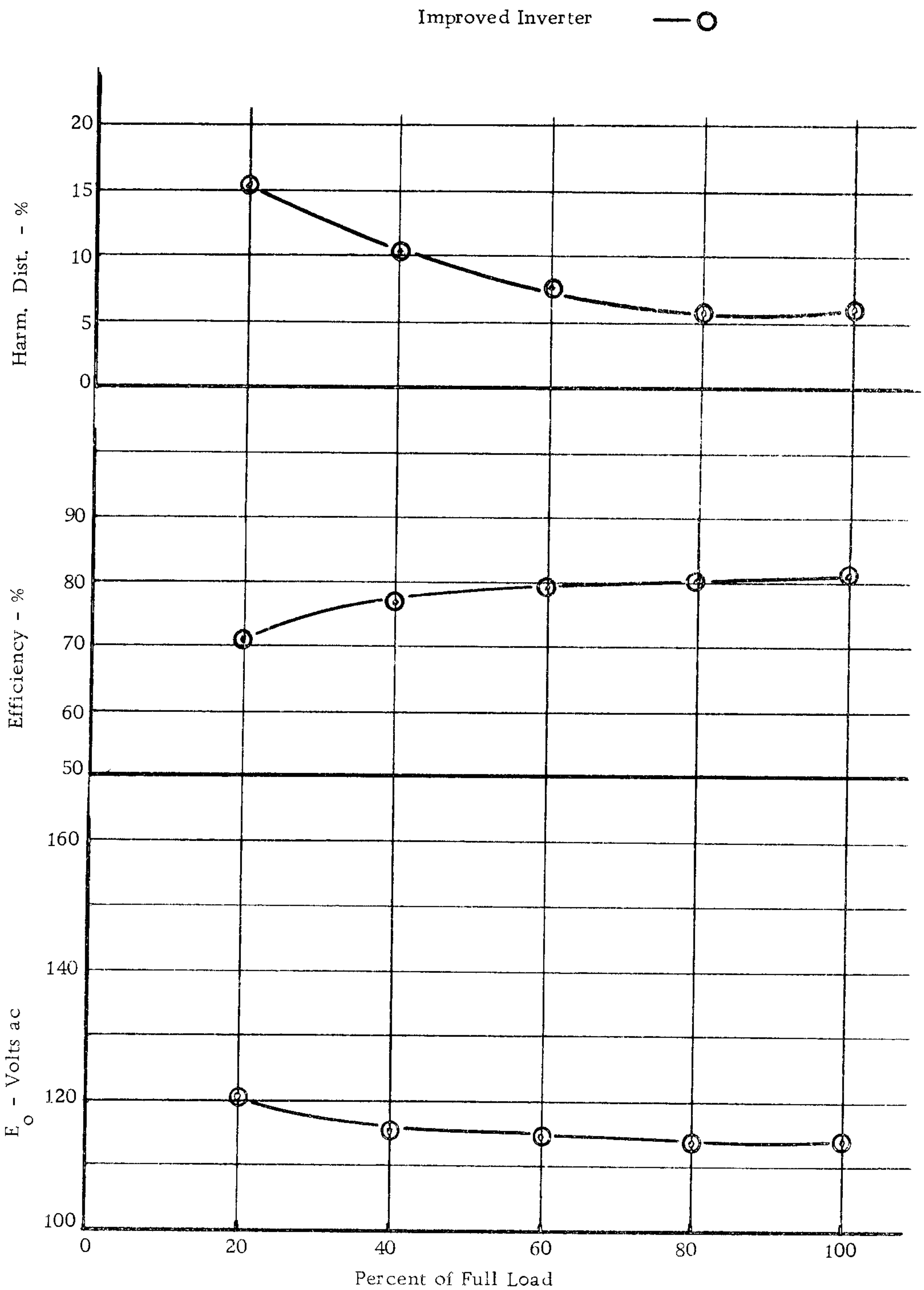


Figure 18. Output Voltage, Efficiency and Distortion
(Input voltage - 34 volts dc)

CONCLUSIONS

The principle of operation of an improved inverter has been explained and oscillograms and graphs indicating its characteristics have been shown. Particularly, the characteristics of the improved inverter have been compared with those of the basic parallel inverter previously described in the literature, to show the considerable improvement in most operating characteristics exhibited by the improved inverter.

There are several features of the improved inverter design, which have not been mentioned in this paper, but which it is believed are of some importance. There are also several areas in the inverter development which bear further investigation. Some of these will now be summarized.

The inverter would appear to be particularly well adapted for use in missile applications where remote ON-OFF cycling is likely. In the event of the loss of the trigger signal in the improved inverter, whether intentional or accidental, the power inversion circuit would shut down. Since the sequence of operation is such that SCR 3, which is self-extinguishing, is always the last SCR to conduct, the improved inverter is fail-safe against loss of trigger signal. It is this characteristic which makes it ideally suited for ON-OFF cycling.

In contrast, the basic parallel inverter and the McMurray inverter are extremely vulnerable to interruption of the trigger signal. If, for any reason, the trigger circuit of these inverters were to become inactivated for several cycles, the push-pull SCR which had been last turned ON would remain ON and would essentially short circuit the dc source across the low resistance ballast inductance and transformer primary.

To cycle either of the above two inverters ON and OFF it would be necessary to provide a relay or other power dissipating series-connected device which could interrupt the power to the inverter circuit proper. In contrast, in order to energize or de-energize the improved inverter circuit, it is only necessary to provide a control element in the milliwatt range to disable the trigger circuitry. The control power required in the other types of inverter require a power level many orders of magnitude larger.

The improved inverter is very adaptable to current-limiting operation. It has already been pointed out that the Output Sensing Circuit becomes active only when the output voltage rises above the design tolerance; a more proper name for this circuitry would probably be the Voltage Sensing Circuit. It will be remembered that this circuit reduced the conduction angle of the push-pull SCRs in the event of an over-voltage condition. In like manner it would appear that a current transformer in series with the load, and conceivably a portion of an output filter circuit, could be used to provide a dc control signal to the magnetic amplifier reducing the push-pull SCR conduction angle in the event of a current overload. This would appear to be an adjustable feature which would allow transition from constant voltage to constant current operating conditions.

It would appear that the Van Allen trigger circuit, utilizing the only two transistors required in the improved inverter, could be eliminated and the regulated inverter could operate in a self-oscillating mode. Moore, et al., have described a self-oscillating circuit that offers obvious advantages in weight, reliability and circuit simplicity (9). In like manner, the improved inverter should be operable in the self-oscillating mode with a relatively minor design change. It would be necessary to provide an initial trigger pulse to one of the push-pull SCRs by means of an R-C circuit. A low-voltage winding on the output transformer could then be used to drive a two-core square-loop circuit, not unlike the regulating circuit, the output of which would alternately trigger the push-pull SCRs. The ON-OFF cycling feature would not be lost because this two-core square-loop circuit could be controlled by a low-level dc current to absorb the full volt-second area of the low-voltage output winding, and hence stop the inversion process.

As was mentioned in the section of this paper which described the basic parallel inverter, the primary purpose of the ballast inductance is to ensure that the current from the dc source is maintained relatively constant during the switching interval. This was a necessary condition in order to avoid the possibility of currents flowing through the push-pull SCRs simultaneously in a manner which would cancel the self-inductance of the transformer primary winding. In the Moore inverter, the ballast inductance was eliminated since one of the push-pull SCRs turns OFF naturally before the other is turned ON. Since in the improved inverter, one push-pull SCR is OFF before the other is turned ON, the ballast inductance would appear to be unnecessary. An attempt was made to eliminate the ballast inductance in the improved inverter circuit; although the inverter did operate, the output could not be controlled in a stable manner. This mode of operation deserves additional study because of the improvement in efficiency promised. Such a design change would, of course, require considerably more filtering in the output circuit to obtain the same level of harmonic reduction enjoyed by the improved inverter described in the body of this paper.

Elimination of the ballast inductance would remove one very desirable, and unexpected, windfall that the tapped ballast inductance provides. It will be remembered that the reason for including the feedback winding was to return the energy stored in the inductance to the dc source; it also developed that the feedback circuitry enabled the improved inverter to operate at no load, even with the regulating circuit disconnected. Operation under no load conditions is not possible with the basic parallel inverter. (As a matter of fact, the basic parallel inverter becomes unstable under light load conditions. It is for this reason that data for the basic parallel inverter operated at light loads and high input voltage was not provided in the Experimental Results section). The action of the feedback winding on the ballast inductance is not unlike that of the feedback circuit in the McMurray inverter.

Finally, it should be pointed out that the inverter characteristics shown are by no means optimum. Considerable improvement in efficiency, weight and regulation characteristics could be made with additional effort. It has been shown, however, that a new method of regulation has provided an inverter design that shows promise of excellent reliability, efficiency and regulation characteristics.

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APPENDIX

APPENDIX

Parts List - Reference Figure 7

Commercial Components

$C_{1,2}$	- Capacitor, 1 microfarad, 200 VDC
C_3	- Capacitor, 4 microfarad, 200 VDC
$D_{9,17}$	- Diode, silicon junction, 1N253
D_{10}	- Diode, zener; 1N1314 (two reverse-biased emitter-base junctions of 2N3638 used in actual circuit)
D_{16}	- Diode, zener; 1N1316 (three reverse-biased emitter-base junctions of 2N3638 used in actual circuit)
$Q_{1,2}$	- Transistor, silicon; 2N3643
R_1	- Resistor, 47K ohm, 1/4 watt
R_2	- Resistor, 33 ohm, 1/4 watt
R_3	- Resistor, 100 ohm, 1/4 watt
$R_{4,5}$	- Resistor, variable, 2K ohm, 1 watt
R_6	- Resistor, variable, 200 ohm, 1 watt
SCR_{1-3}	- Silicon controlled rectifier, Motorola type MCR 1305-4

All diodes type IN 462 unless otherwise noted.

Fabricated Components

L_1 - Inductance:

Winding number one (1-2): 75 turns, No. 19 wire

Winding number two (3-4): 132 turns, No. 23 wire

Core: M6X - Arnold 3/4'' Silectron laminations - .010'' gap

L_2 - Inductance:

Winding: 300 turns, No. 32 wire

Core: Two (2) powdered iron cores, 3/8'' ID x 3/4'' OD x 1/4''

T_1 - Inverter transformer:

Primary winding: 240 turns, center-tapped, No. 20 wire, wound on each leg of core and paralleled

Output winding: 500 turns, No. 23 wire, wound on each leg of core and connected series-aiding

Feedback winding: 60 turns, No. 23 wire

Magnetic amplifier drive winding: 36 turns, No. 23 wire

Core: Carstedt No. CH-50, 4 mil, C type

T_2 - Van Allen oscillator transformer:

Collector winding: 500 turns, No. 38 wire

Base winding: 300 turns, No. 38 wire

Control winding: 200 turns, No. 38 wire

Core: Matched pair, Arnold type T6592 Supermendur cores; identical windings, each core

T_3 - Pulse-forming transformer:

Three windings: each, 100 turns, No. 38 wire

Core: Arnold type 3T5694-D1, Deltamax, 1 mil

T_4 - Magnetic amplifier:

Gate winding: 500 turns, No. 38 wire

Control winding: 230 turns, No. 38 wire

Bias winding: 100 turns, No. 38 wire

Core: Matched pair, Arnold type T5692 Deltamax cores; identical windings, each core