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Title: Discrete Trap Modeling of Thin-film Transistors.

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A discrete trap model is developed and employed for elucidation of thin-film transistor (TFT) device physics trends. An attractive feature of this model is that only two model parameters are required, the trap energy depth, E_T, and the trap density, N_T. The most relevant trends occur when E_T is above the Fermi level. For this case drain current – drain voltage simulations indicate that the drain current decreases with an increase in N_T and E_T. The threshold voltage, V_T, extracted from drain current – gate voltage ($I_D - V_{GS}$) simulations, is found to be composed of two parts, V_{TRAP}, the voltage required to fill all the traps and $V_{ELECTRON}$, the voltage associated with electrons populating the conduction band. V_T moves toward a more positive voltage as N_T and E_T increase. The inverse subthreshold voltage swing, S, extracted from a $\log(I_D) - V_{GS}$ curve, increases as N_T and E_T increase. Finally, incremental mobility and average mobility versus gate voltage simulations indicate that the channel mobility decreases with increasing N_T and E_T.

Discrete Trap Modeling of Thin-film Transistors

by

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I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Ganesh Chakravarthy Yerubandi, Author

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No words can express my debt to my family: my parents and my brother who have always put my interests before theirs. Whatever I am and wherever I shall be, I owe it all to them.

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1. INTRODUCTION

A thin-film transistor (TFT) with a micro-crystalline cadmium sulfide semi-conducting channel layer, an evaporated gate dielectric, and gold source, drain, and gate contacts was first reported by P. K. Weimer in 1962 [1]. TFT technology emerged as a prominent technology for active-matrix liquid-crystal displays with the advent of amorphous or poly-crystalline silicon as the semiconducting channel material.

Circuit-oriented SPICE models were subsequently developed in order to facilitate computer-aided design of complicated TFT circuits and electronic systems [2,3]. These models focus specifically on amorphous and polycrystalline silicon TFT modeling, concentrating on materials topics pertinent to such devices including band-tail & localized gap states; dispersive transport; threshold voltage metastability; and grain boundary trapping, passivation, & transport. However, as new TFT applications emerge, involving large-area, low-cost, printed, flexible, and/or transparent electronics, new material development is required. The models presented in references 2 and 3, even though they accurately account for TFT behavior, are not of much help in the development of new materials and devices for emerging applications. Thus, more generic device models should be developed in order to

provide insight regarding the electrical properties of a TFT from the perspective of the development of new materials and emerging applications.

The objective of this thesis is to present a device physics-based TFT model which includes the effects of a discrete trap. A derivation of the drain current (I_D) equation for this discrete trap TFT model is developed. A portion of this derivation was presented earlier by Sze [4]. The discrete trap model is employed in simulation in order to elucidate the primary device physics consequences of carrier trapping. The effects of trap depth and density on the drain current – drain voltage ($I_D - V_{DS}$) output characteristics and drain current – gate voltage ($I_D - V_{GS}$) transfer characteristics are studied. The degradation in incremental and average mobility of carriers in the TFT channel due to the presence of a discrete trap is discussed. Also, mechanisms associated with sub-threshold current in a TFT are considered within the perspective of the discrete trap model.

The organization of this thesis is as follows. Chapter 2 contains a review of the pertinent literature and background information relevant to the results discussed in the thesis. Chapter 3 presents the development of the discrete trap model and simulation results derived from this model. Non-idealities in TFT behavior such as sub-threshold current and channel mobility degradation are considered within the context of the discrete trap model. Finally, Chapter 4 presents conclusions and recommendations for future work.

2. LITERATURE REVIEW AND TECHNICAL BACKGROUND

The primary goal of this chapter is to present an overview of the structure and operation of TFTs and to review the ideal square-law model for the operation of an n-channel TFT. Basic aspects of traps and trap parameters are also discussed.

2.1. TFT Structures

A TFT is an insulated-gate field-effect transistor whose operation depends on the same basic principle as a metal oxide semiconductor field-effect transistor (MOSFET). However, there are significant differences between the structure of a TFT and a MOSFET. Figure 2.1 shows typical cross-sectional views of a TFT and a MOSFET.

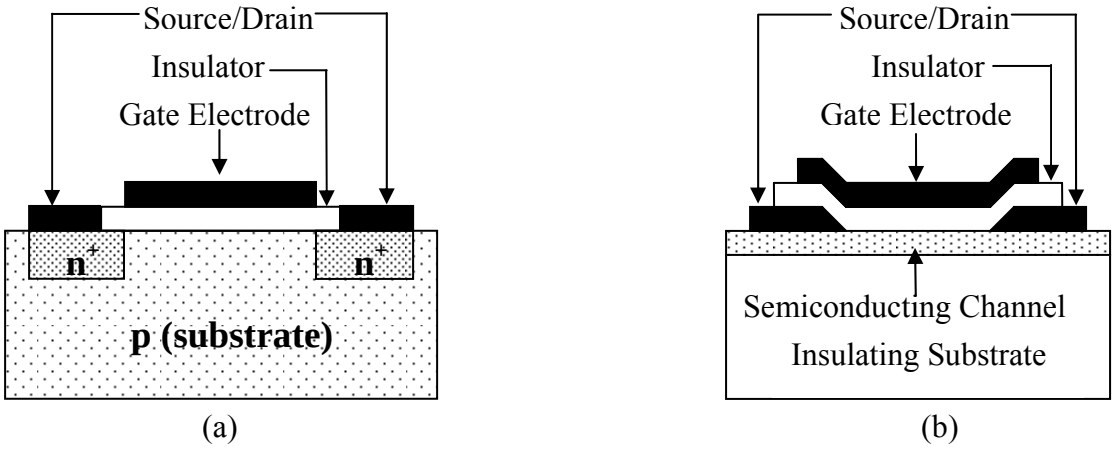


Figure 2.1: Cross-sectional schematic drawing of a (a) MOSFET and (b) TFT.

As evident from Fig. 2.1, the substrate of a TFT is an insulating material, whereas the substrate of a MOSFET is a semiconductor material (p-type) of opposite polarity as the source and drain diffusions (n-type). Source and drain contacts to the

semiconducting channel material are injecting contacts to the channel in a TFT structure, rather than ohmic contacts to a pn junction as in a MOSFET.

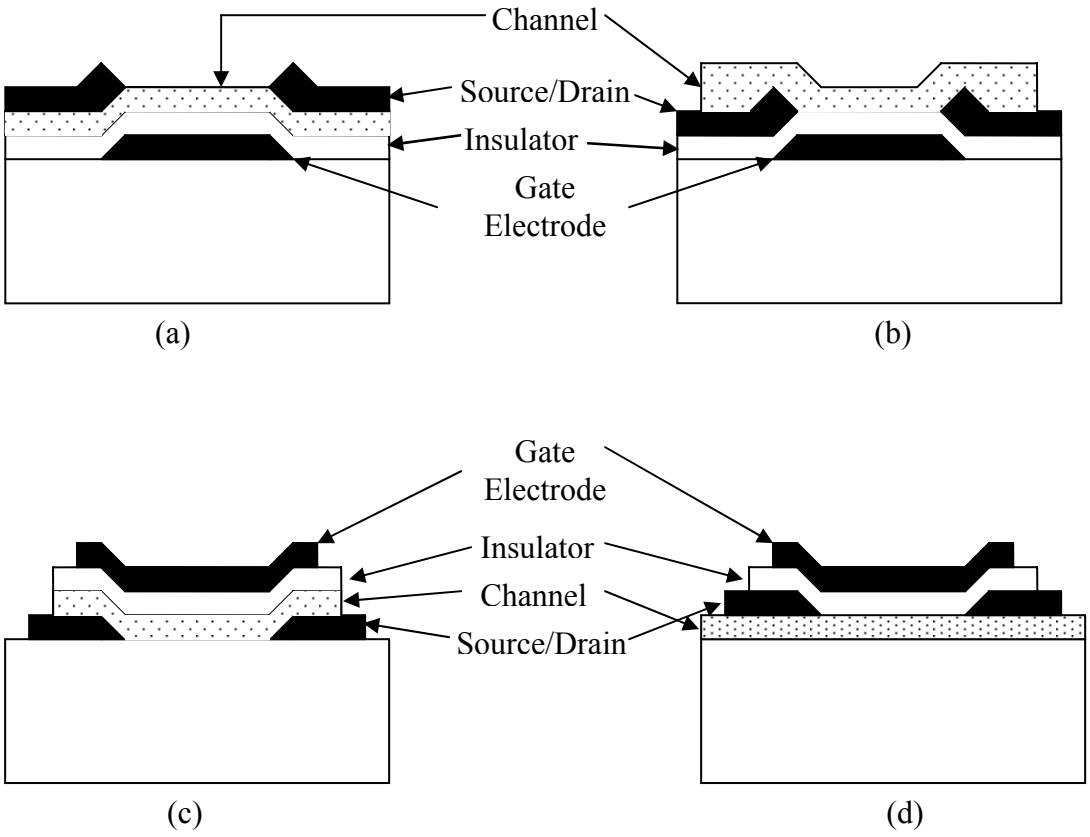


Figure 2.2: Four thin-film transistor configurations: (a) staggered bottom-gate, (b) coplanar bottom-gate, (c) staggered top-gate, and (d) coplanar top-gate.

Four TFT device structures are possible, as indicated in Fig. 2.2, and are categorized as staggered or coplanar [1]. In a staggered configuration, as shown in Figs. 2.2a and 2.2c, the source and drain contacts are on opposite sides of the channel from the insulator, whereas in a coplanar configuration, as shown in Figs. 2.2b and 2.2d, the source and drain contacts and the insulator are on the same side of the channel. Both the staggered and the coplanar configurations can further be categorized as bottom-gate and top-gate structures. A bottom-gate TFT, also referred as an inverted TFT, has the gate insulator and gate electrode located beneath the

channel, as shown in Figs. 2.2a and 2.2b. In a top-gate device, as shown in Figs. 2.2c and 2.2d, the channel is covered by a gate insulator and gate electrode.

The coplanar structure is popular in polycrystalline silicon TFTs, whereas staggered structures are commonly used in amorphous silicon TFTs. The inverted, staggered structure is the most popular amorphous silicon TFT structure, because it gives the best transistor characteristics and offers significant process latitude [5]. Top-gate TFTs are usually fabricated with an aluminum gate since gate deposition is one of the last deposition steps in the fabrication process of this type of TFT, after which no high temperature processing is required. Passivation of the channel material by the gate insulator is an added advantage of a top-gate structure.

2.2. TFT Operation

TFT and MOSFET operation is similar in that the current from the source to the drain terminal is modulated by the applied gate electric field. Current modulation in a TFT or a MOSFET can be explained if the metal-oxide-semiconductor (MOS) part of the TFT is considered as a capacitor [6]. A voltage applied between the metal and semiconductor causes a charge to build up in the semiconductor and the metal gate.

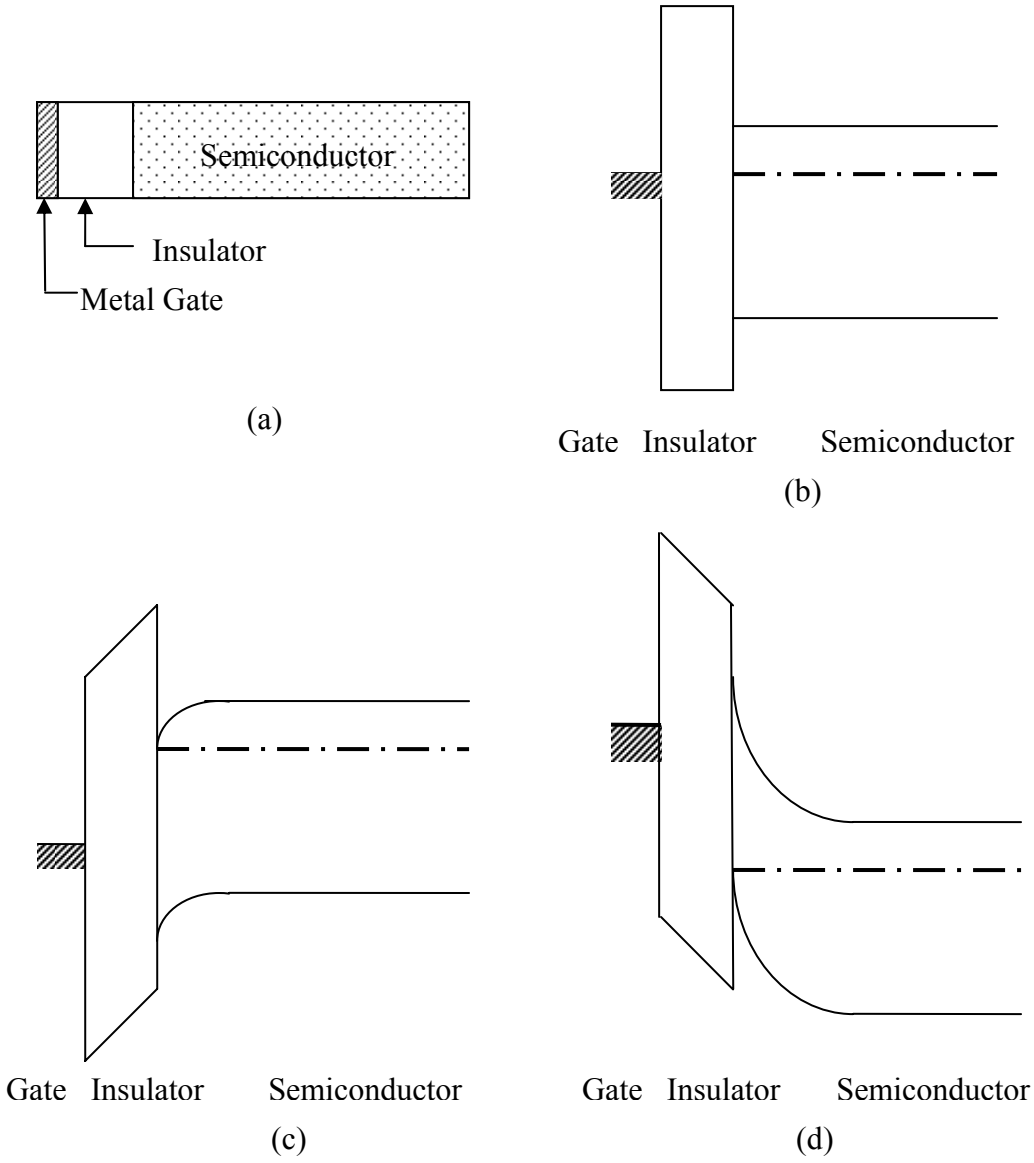


Figure 2.3: (a) The cross-section of a metal-oxide-semiconductor (MOS) capacitor and corresponding energy band diagrams for several biasing conditions: (b) equilibrium, (c) accumulation ($V_{GS} > 0$ V), and (d) inversion ($V_{GS} < 0$ V).

Figure 2.3 shows the cross-section and energy band diagrams of a MOS capacitor with an n-type semiconductor. Figure 2.3b shows the equilibrium situation, with no gate bias applied, for an ideal case in which no charge is present in the insulator or at the insulator/semiconductor interface so that the energy bands are flat.

A positive voltage applied to the gate electrode of the MOS capacitor, as shown in Fig. 2.3c, causes the energy bands to bend downward, hence increasing the electron concentration at the insulator-semiconductor interface. The interface is thus more conductive than the bulk of the semiconductor. This mode of operation in which majority carriers, electrons in this case, accumulate at the insulator/semiconductor interface and give rise to the channel current is denoted as the accumulation-mode of operation. When a small to moderate negative voltage is applied to the gate electrode, majority carrier electrons are repelled from the insulator/semiconductor interface so that a depletion layer is formed. When a larger negative voltage is applied the gate, as shown in Fig. 2.3d, the depletion layer reaches a maximum thickness after which minority carriers, holes in this case, form a conductive channel at the insulator/semiconductor interface. This conductive channel gives rise to what is denoted inversion-mode operation, since the conductivity type is inverted with respect to the semiconductor bulk. MOSFETs always operate in inversion-mode whereas TFTs operate in accumulation-mode.

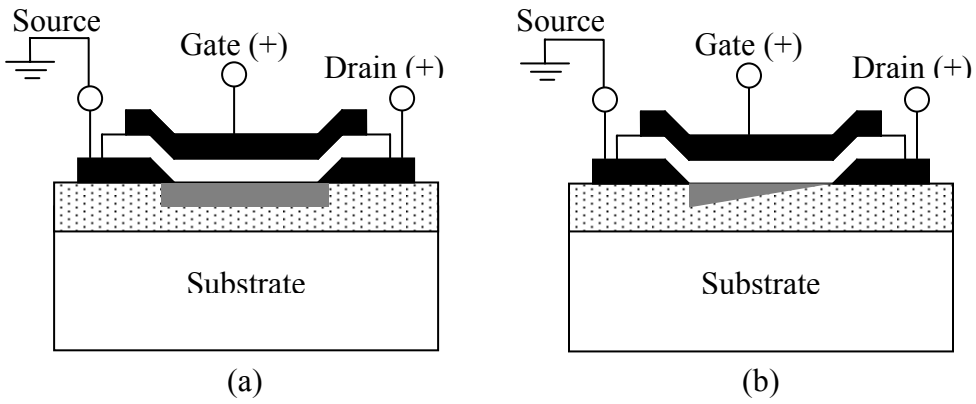


Figure 2.4: An n-channel accumulation-mode TFT operating in (a) pre-pinch-off and (b) post-pinch-off regime.

Figure 2.4 shows a three terminal n-channel TFT with appropriate biasing of the gate, source, and drain electrodes for accumulation-mode operation. A positive voltage is applied to the gate electrode to attract electrons to the insulator/semiconductor interface and form an accumulation layer. The drain electrode is biased positively with respect to the source (which is grounded) to attract electrons from the accumulation channel. At zero or small positive voltages applied to the drain electrode, the accumulation layer formed, as shown in Fig. 2.4a, is uniform from the source end to the drain end of the channel. At a small drain voltage, the TFT operates as resistor where the drain current (I_D) increases linearly with increase in the drain voltage (V_{DS}). However, at slightly larger drain voltages, the linear dependence of I_D on V_{DS} changes to a quadratic dependence on V_{DS}. This entire regime of TFT operation, where I_D increases with increasing V_{DS}, is called triode or pre-pinch-off. As V_{DS} is further increased, the effective voltage between the gate and drain (V_{GD}) decreases, which in turn decreases the electron concentration at the drain end of the accumulation layer. The drain voltage at which the accumulation channel is fully depleted of electrons, is called the pinch-off voltage and is denoted as V_{DSAT}. When $V_{DS} \geq V_{DSAT}$, drain voltage has no effect on I_D so that the drain current saturates. This is referred to as the post-pinch-off regime, and is shown in Fig. 2.4b.

Depending on the gate voltage required to form an accumulation layer, a TFT can be classified as either an enhancement-mode or a depletion-mode device. In enhancement-mode operation of an n-channel TFT, a positive voltage must be applied to the gate electrode to create an accumulation layer at the insulator/semiconductor interface. For depletion-mode operation, the accumulation layer is already present at

zero gate voltage. Thus, for an n-channel TFT, a negative gate voltage has to be applied to deplete the accumulation channel and turn the device off. Therefore, an enhancement-mode device is a "normally-off" device, whereas a depletion-mode device is "normally on". In an ideal TFT model in which traps are neglected, the TFT would be a depletion-mode device because of the presence of zero-bias carriers (bulk carriers) available for current conduction. However, the presence of empty traps, which must be filled with carriers prior to the formation of the accumulation layer, gives rise to enhancement-mode operation of the TFT [7].

2.3. Square-law Model

In this section, a derivation of the square-law model as developed by Sze [4] is presented. The basic assumptions made in the model are as follows. (1) The mobility (μ) of the carriers in the channel is constant, (2) the gate capacitance (C_G) is constant and independent of the gate voltage, (3) the source and drain electrodes are ohmic contacts to the semiconductor, (4) the initial charge density in the semiconductor (n_o) is positive for a depletion-mode TFT and negative for a enhancement-mode TFT.

An important assumption implicitly present in the square-law model presented by Sze is Shockley's gradual channel approximation. The gradual channel approximation decomposes the two-dimensional electric field problem, involving electric field components both parallel and perpendicular to the flow of current in the channel, into two separate one-dimensional problems. The gradual channel approximation assumes that the lateral change in the y-component of the electric field

along the channel is much less than the change in the x-component of the electric field perpendicular to the channel. Thus, it can be assumed that the gate voltage effects only the modulation of carriers in the channel, whereas the drain voltage effects transport of carriers along the channel. However, the gradual channel approximation is only valid for long-channel devices, where the lateral electrical field can be neglected, and for device operation in the pre-pinch-off regime.

The model development begins by treating the TFT gate, insulator, and semiconductor channel as an ideal MOS capacitor, as discussed in the previous section. The total charge induced in the semiconductor can be obtained by employing the relationship $Q = C \times V$. Substituting appropriate terms into this relationship gives,

$$q\Delta n(y) = \frac{C_G}{h}\left[V_{GS} - V(y)\right], \tag{2.1}$$

where $q\Delta n(y)$ is the induced charge density, C_G is the gate capacitance per unit area, V_{GS} is the gate voltage, h is the thickness of the semiconductor channel, and $V(y)$ is the channel voltage obtained at a distance "y" along the channel.

Assuming that the carrier transport is dominated by drift, the drain current, I_D, is given by,

$$I_D = hZ\left[\sigma_o + \sigma(y)\right]\xi(y), \tag{2.2}$$

where Z is the channel width, $\xi(y)$ is the electric field along the channel, σ_o is the channel conductivity at zero gate bias, and $\sigma(y)$ is the incremental channel conductivity due to the induced charge density. The drain current may be rewritten by noting that $\sigma = q\mu n\xi$, resulting in,

$$I_D = hZq\mu[n_o + \Delta n(y)]\xi(y), \tag{2.3}$$

where n_o is the initial charge density in the semiconductor (charge/cm^3) and $\Delta n(y)$ is the gate-induced charge density. Substituting Eq. (2.1) into Eq. (2.3) and expressing the electric field in terms of the voltage drop along the channel yields,

$$I_D = Z\mu\ C_G\left[\frac{qhn_o}{C_G} + V_{GS} - V(y)\right]\frac{dV(y)}{dy}. \tag{2.4}$$

Operating on both sides of Eq. (2.4) by *dy*, then integrating over the length of the channel, L, and dividing both sides by the channel length, L, yields

$$I_D\int_0^L dy = Z\mu C_G\int_0^{V_{DS}}\left[\frac{qhn_o}{C_G} + V_{GS} - V(y)\right]dV(y), \tag{2.5}$$

$$\Rightarrow \quad I_D = \frac{Z\mu C_G}{L}\left[(V_{GS} - V_{ON})V_{DS} - \frac{{V_{DS}}^2}{2}\right], \tag{2.6}$$

where the threshold voltage, V_{ON}, is given by,

$$V_{ON} = \frac{-qhn_o}{C_G}. \tag{2.7}$$

It is important to note that Eq. (2.6) is only valid in the pre-pinch-off regime, i.e., when $V_{GS} \geq V_{ON}$ and $V_{DS} \leq V_{DSAT}$ ($V_{DSAT} = V_{GS} - V_{ON}$). The first condition denotes that there has to be a sufficient number of carriers induced in the channel for appreciable current to flow. This gate voltage where the appreciable current flows between the source and the drain electrodes is called the threshold voltage, V_{ON}. The second condition denotes that the drain voltage is less than that required to pinch-off the channel. The channel is said to be pinched off when the effective voltage between the gate and drain (V_{GD}) is less that than the threshold voltage, V_{ON}, and is given by the condition $V_{DS} = V_{DSAT} = V_{GS} - V_{ON}$. The drain current expression for the post-pinch-

off regime is obtained by replacing V_{DS} by V_{DSAT} in Eq. (2.6) and requiring that $V_{DS} \geq V_{DSAT}$. Thus, the saturated drain current (I_{DSAT}) in post-pinch-off regime is given by,

$$I_{DSAT} = \frac{Z\mu C_G}{2L}\left(V_{GS} - V_{ON}\right)^2 . \tag{2.8}$$

Equations (2.6) – (2.8) are the central equations constituting the square-law model and are summarized in Table 2.1. It should also be noticed that the designation for threshold voltage is V_{ON} rather than V_T, as conventionally used. In this thesis V_T is used to denote the *extracted threshold voltage* by the method of linear extrapolation. The justification for the use of V_{ON} as the threshold voltage in the model equations and the differences between V_{ON} and V_T are discussed in detail in Chapter 3.

Variable designation	**Equation**
Threshold voltage	$V_{ON} = \frac{-qhn_o}{C_G}$
Pinch-off condition	$V_{DSAT} = V_{GS} - V_{ON}$

Regime of operation	**Equation**	**Constraints**
Subthreshold	$I_D = 0$	$V_{GS} < V_{ON}$
Pre-pinch-off	$I_D = \frac{Z\mu C_G}{L}\left[(V_{GS} - V_{ON})V_{DS} - \frac{V_{DS}^{\ 2}}{2}\right]$	$V_{GS} \geq V_{ON}$ $V_{DS} \leq V_{DSAT}$
Post-pinch-off	$I_{DSAT} = \frac{Z\mu C_G}{L}\left(V_{GS} - V_{ON}\right)^2$	$V_{GS} \geq V_{ON}$ $V_{DS} > V_{DSAT}$

Table 2.1: Summary of the square-law model.

2.4. Bulk and Interface Traps

The presence of traps in the semiconductor channel layer plays a major role in the operation of a TFT. This section describes the nature of bulk traps and interface states present at an insulator-semiconductor interface.

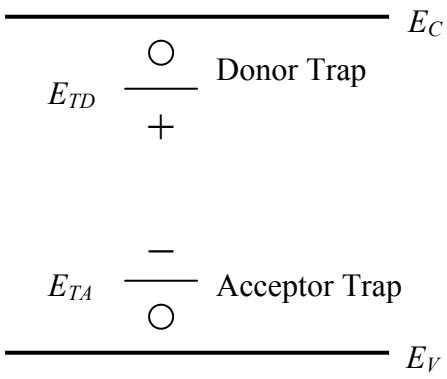


Figure 2.5: Energy band diagram of a bulk semiconductor with a donor-like trap and an acceptor-like trap with ionization energies, E_{TD} and E_{TA}, respectively.

Figure 2.5 shows an acceptor-like and a donor-like trap, with ionization energies E_{TA} and E_{TD}, respectively, present in the bulk semiconductor. Donor-like traps have ionization energies that are close to the conduction band minimum, E_C. When the Fermi level, E_F, is above E_{TD} so that the trap is filled with an electron, this trap is electronically neutral. However, if E_F is below E_{TD} so that the trap is ionized (i.e., it loses an electron), it is positively charged. In contrast, an acceptor-like trap has an ionization energy close the valance band minimum, E_V. An acceptor-like trap is neutral when E_F is below E_{TA} so that it is not filled with an electron, and is negatively charged when E_F is above E_{TA} so that it is filled with an electron. In summary, donor-like traps are positive when empty and neutral when filled; acceptor-like traps are neutral when empty and negative when filled, as indicated in Fig. 2.5.

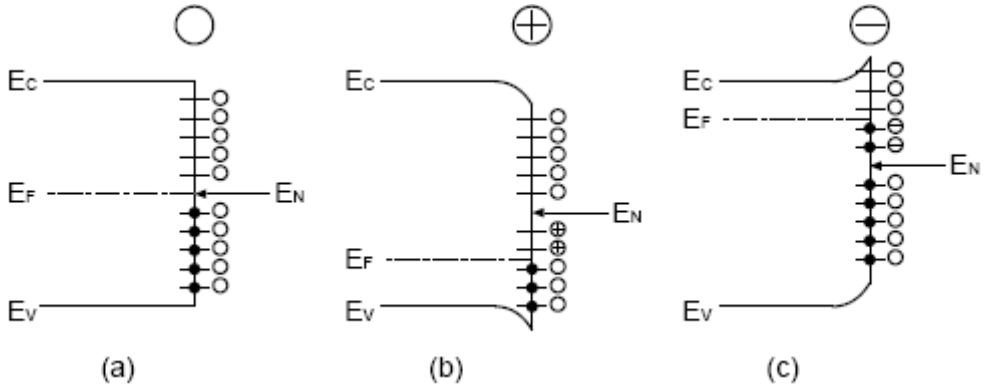


Figure 2.6: Energy band diagram considering interface states and the resultant effect of modulating the Fermi level position, E_F, with respect to the charge neutrality level, E_N. Three conditions are evaluated, (a) $E_F = E_N$, resulting in a flat-band condition, (b) $E_F < E_N$, resulting in a donor-like interface, and (c) $E_F > E_N$, resulting in an acceptor-like interface.

Although traps present everywhere in the semiconductor affect TFT operation, traps at the insulator-semiconductor interface play a major role. Interface traps are formed because of unsatisfied dangling bonds and lattice mismatch between materials at an interface.

The acceptor or the donor-like nature of the interface traps may be elucidated by taking into consideration the charge neutrality level, E_N, as shown in Fig. 2.6. When the Fermi level is present at the charge neutral level, i.e., $E_F = E_N$, the net charge at the insulator-semiconductor interface is zero, thus resulting in a flat band condition as shown in Fig. 2.6a. If $E_F < E_N$, as shown in Fig. 2.6b, a net positive charge due to ionized donor states is present at the interface, resulting in a donor-like interface. This net positive interface charge is balanced by negative space charge in the semiconductor, as is evident from the negative curvature of the energy bands. When $E_F > E_N$, as shown in Fig. 2.6c, a net negative charge is present at the interface, resulting in acceptor-like interface. This net negative charge is balanced by positive charge, as is evident from the positive curvature of the energy bands.

In the discrete trap model presented in this thesis only an acceptor-like trap is considered. This discrete trap is assumed to have a trap ionization energy E_T and a trap density N_T.

3. DISCRETE TRAP MODELING

The objective of this chapter is to present a derivation of the discrete trap model which is then employed in simulations to elucidate the primary device physics consequences of carrier trapping. The initial portion of this derivation has been previously introduced by Sze [4]. It should be noted that while Sze asserts that this is an interface trap model, certain aspects of his model development imply these traps to be bulk like.

3.1. Trap Modeling

The discrete trap under consideration is assumed to interact only with conduction band electrons (not valence band holes) so that it is characterized by its ionization energy, E_T, capture cross section, σ_n, and density, N_t.

If the density of filled traps is given by n_t, the rate of conduction band trapping is given by $\bar{v}\sigma_n(N_t - n_t)n_c$, where $\bar{v}$ is the average conduction band electron velocity, (N_t - n_t) is the density of empty traps, and n_c is the density of electrons present in the conduction band. Also, the rate of electron emission from the trap state to the conduction band is given by $\bar{v}\sigma_n n_t n_1$, where n_1 is the conduction band electron density when the Fermi-level, E_F, is equal to the trap level. n_1 is given by

$$n_1 = N_c e^{\left(\frac{-E_T}{k_B T}\right)}, \tag{3.1}$$

where N_c is the effective density of states of the conduction band and k_B is Boltzmann's constant. Thus, the net rate of change in trap occupancy is given by

$$\frac{\partial n_t}{\partial t} = \bar{v}\sigma_n\left(N_t - n_t\right)n_c - \bar{v}\sigma_n n_t n_1 . \tag{3.2}$$

In steady-state, the rate of trap emission and capture are equal so that

$$\left(N_t - n_t\right)n_c = n_t n_1 . \tag{3.3}$$

Solving for n_t yields an explicit assessment of the steady-state trap occupancy,

$$n_t = \frac{n_c N_t}{n_c + n_1} . \tag{3.4}$$

Recognizing that the total charge induced in the channel by the application of a gate voltage is distributed into both conduction band and trap states,

$$q\left(\Delta n_c + \Delta n_t\right) = q\left[\left(n_c + n_t\right) - \left(n_{co} + n_{to}\right)\right] = \frac{C_G}{h}\left[V_{GS} - V\left(y\right)\right], \tag{3.5}$$

where n_{co} and n_{to} are the initial, zero-bias densities of free conduction band electrons and trapped electrons. Rearrangement of Eq. 3.5 leads to

$$q\left(n_c + n_t\right) = \frac{C_G}{h}\left[V_{GS} - V\left(y\right) - V_{ON}\right], \tag{3.6}$$

where the V_{ON} is given by

$$V_{ON} = -\frac{qh}{C_G}\left(n_{co} + n_{to}\right). \tag{3.7}$$

Substitution of n_t from Eq. (3.4) into Eq. (3.6) yields,

$$\begin{aligned} V_c(y) &\equiv \frac{q n_c(y) h}{C_G} \\ &= \frac{1}{2}\left[\left(V_{GS} - V(y) - V_{ON}\right) - \left(V_t + V_1\right)\right] \\ &\quad + \frac{1}{2}\left\{\left[\left(V_{GS} - V(y) - V_{ON}\right) - \left(V_t + V_1\right)\right]^2 + 4V_1\left(V_{GS} - V(y) - V_{ON}\right)\right\}^{1/2} \end{aligned} , \tag{3.8}$$

where $V_t = \frac{qN_t h}{C_G}$ and $V_1 = \frac{qn_1 h}{C_G}$.

For mathematical convenience, Eq. (3.8) can be rewritten as

$$V_c(y) = \frac{1}{2}[a - V(y)] + \frac{1}{2}\left\{[a - V(y)]^2 + c[b - V(y)]\right\}^{1/2}, \tag{3.9}$$

where, $a = V_{GS} - V_t - V_{ON} - V_1$, $b = V_{GS} - V_{ON}$ and $c = 4V_1$.

Drift-dominated drain current is derived in a similar manner to the ideal square-law derivation presented in the Chapter 2.3, beginning with

$$I_D = hZn_c(y)q\mu\frac{dV(y)}{dy}. \tag{3.10}$$

Substitution of $n_c(y)$ from Eq. (3.8) into Eq. (3.10), operating on both sides of Eq. (3.8) by dy, integrating the left hand side of the equation over the channel length and dividing both sides of the equation by L leads to,

$$I_D = \frac{Z}{L}\mu C_G \int_0^{V_{DS}} V_c(y)dV(y). \tag{3.11}$$

Substitution of Eq. (3.9) for $V_c(y)$ into Eq. (3.11) and performing the integration yields,

$$\begin{aligned} I_D = \frac{Z}{L}\mu C_G \Bigg[& \frac{1}{2}aV_{DS} - \frac{1}{4}{V_{DS}}^2 + \frac{1}{4}\left(V_{DS} - a - \frac{c}{2}\right)C_1 \\ & + \ln\left(\frac{C_2}{C_3}\right)(V_t V_1) + \frac{1}{4}\left(a^2 + bc\right)^{1/2}\left(a + \frac{c}{2}\right)\Bigg], \end{aligned} \tag{3.12}$$

where, $C_1 = \left[(a - V_{DS})^2 + c(b - V_{DS})\right]^{1/2}$, $C_2 = \left(-2a - c + 2V_{DS} + 2C_1\right)$ and $C_3 = \left[-2a - c + 2\left(a^2 + bc\right)^{1/2}\right]$. Equation (3.12) constitutes the discrete trap model current-voltage characteristic equation for the above-turn-on, pre-pinch-off regime of the TFT operation, whose independent variable constraint equation are specified by

$$V_{GS} \geq V_{ON} \text{ and } V_{DS} \leq V_{DSAT}. \tag{3.13}$$

The drain current expression for the saturation (post-pinch-off) regime of TFT operation is then obtained by replacing V_{DS} by V_{DSAT} in Eq. (3.12) and requiring that $V_{DS} \geq V_{DSAT}$.

Explicitly the post-pinch-off current-voltage expression is given by

$$I_{DSAT} = \frac{Z}{L}\mu C_G\left[\frac{1}{2}aV_{DSAT} - \frac{1}{4}V_{DSAT}^{\ 2} + \frac{1}{4}\left(V_t^2 - V_1^2\right) + \ln\left(\frac{4V_t}{C_3}\right)\left(V_t V_1\right) + \frac{1}{4}\left(a^2 + bc\right)^{1/2}\left(a + \frac{c}{2}\right)\right], \tag{3.14}$$

where the corresponding constraint equations are given by

$$V_{GS} \geq V_{ON} \text{ and } V_{DS} > V_{DSAT}. \tag{3.15}$$

Finally, the pinch-off voltage for this model is given by

$$V_{DSAT} = V_{GS} - V_{ON}. \tag{3.16}$$

When V_1 and V_t are negligible (i.e., when $c \rightarrow 0$ and $a \rightarrow V_{GS} - V_{ON}$), Eqs (3.12) and (3.14) reduce to the ideal square-law model given by Eqs. (2.6) and (2.8), respectively. Table 3.1 summarizes the TFT discrete trap model.

Variable designations	**Equation**	
Turn-on voltage	$V_{ON} = -\frac{qh}{C_G}\left(n_{co} + n_{to}\right)$	
Pinch-off condition	$V_{DSAT} = V_{GS} - V_{ON}$	
Regime of operation	**Equation**	**Constraints**
Cut-off	$I_D = 0$	$V_{GS} < V_{ON}$
Pre-pinch-off	*Eq. (3.12)*	$V_{GS} \geq V_{ON}$ $V_{DS} \leq V_{DSAT}$
Post-pinch-off	*Eq. (3.14)*	$V_{GS} \geq V_{ON}$ $V_{DS} > V_{DSAT}$

Table. 3.1: Summary of the discrete trap model.

3.2. Simulation Results

Based on the discrete trap model developed in Chapter 3.1, simulations are performed in order to demonstrate the effect of the trap parameters N_T and E_T on the output and transfer current characteristics of the TFT.

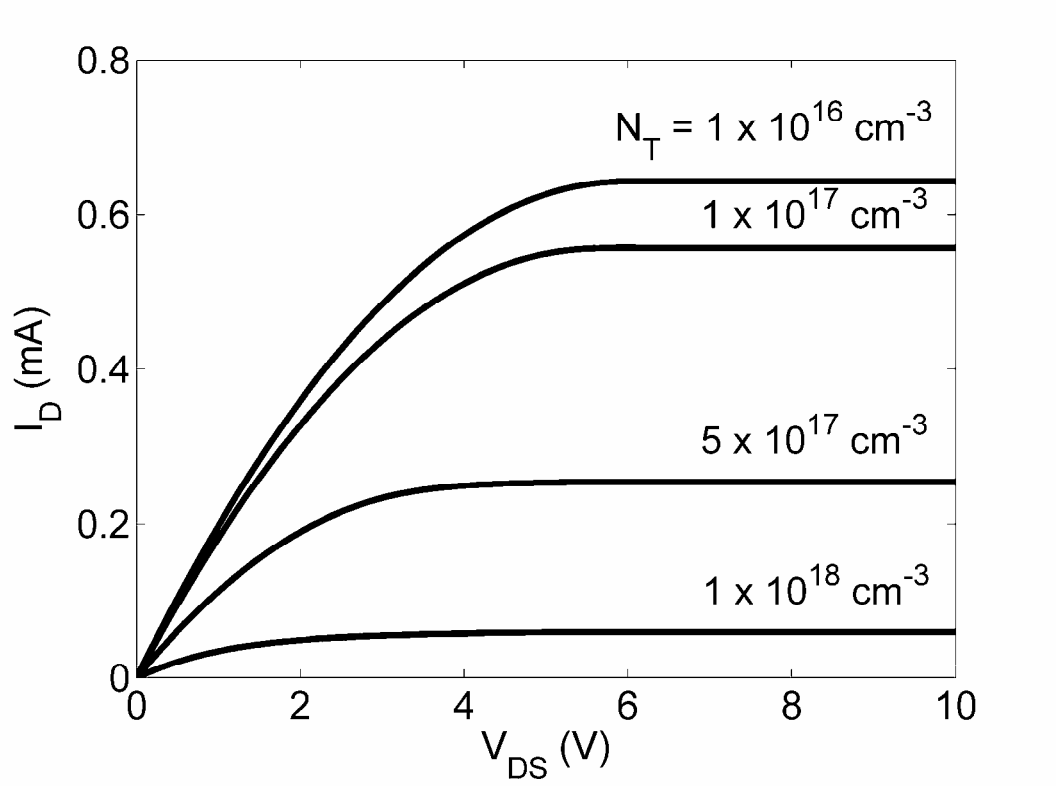


Figure 3.1: Drain current-drain voltage (I_D-V_{DS}) characteristics for an n-channel TFT corresponding to a gate voltage of 6 V and a trap depth of E_C - E_T = 0.15 *eV* below the conduction band minimum. Geometrical and channel-based parameters employed for this simulation are: Z/L = 6:1, h = 20 nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, μ = 100 cm^2/V-s, and $n_{co} = 1 \times 10^{15}$ cm^{-3}.

Figure 3.1 illustrates the output I_D - V_{DS} curves for different values of the trap density N_T at a gate voltage of *6 V* and a trap depth of *0.15 eV* below the conduction band minimum. A decrease in the drain current with increasing trap density, N_T, is observed in Fig. 3.1. As indicated by Eq. (3.4), the steady-state concentration of trapped electrons, n_t, depends directly on the trap density, N_T. An increase in N_T

causes an increase in n_t, thereby reducing the free electron concentration available for conduction and thus reducing the drain current. Moreover, a decrease in the free electron concentration translates into a corresponding decrease in the slope of the I_D curve in the pre-pinch-off regime. A decrease in the I_D slope at small V_{DS}, as shown in Fig. 3.1, indicates that the average channel mobility deteriorates as the trap density increases. Mobility trends in the context of the discrete trap model are more fully discussed in Chapter 3.4.2.

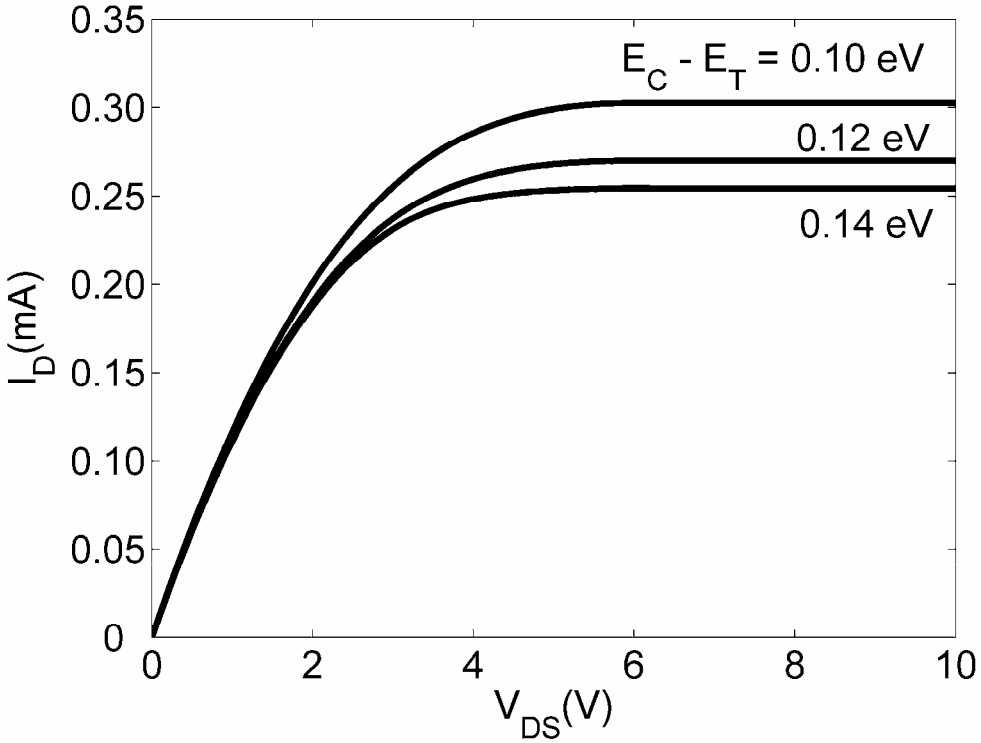


Figure 3.2: Drain current-drain voltage (I_D-V_{DS}) characteristics for an n-channel TFT corresponding to a gate voltage of 6 V and a trap density of $N_T = 5 \times 10^{17}$ cm^{-3}. The Fermi level, E_F, as established by the initial free carrier concentration, n_{co}, is $E_C - E_F$ = 0.21 eV. Geometrical and channel- based parameters employed for this simulation are: Z/L = 6:1, h = 20 nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, μ = 100 cm^2/V-s, and $n_{co} = 1 \times 10^{15}$ cm^{-3}.

Figure 3.2 demonstrates that the depth of the trap, E_T, affects the TFT $I_D - V_{DS}$ characteristics. When E_T is between E_C and E_F, a deeper trap results in a larger

reduction in the drain current, as shown in Fig. 3.2. Note, however, that when E_T drops below E_F (not shown in Fig. 3.2), there is a negligible affect on I_D. The decrease in the drain current with increasing trap depth as shown in Fig. 3.2 is attributed to the rate of trap re-emission, as discussed in the following.

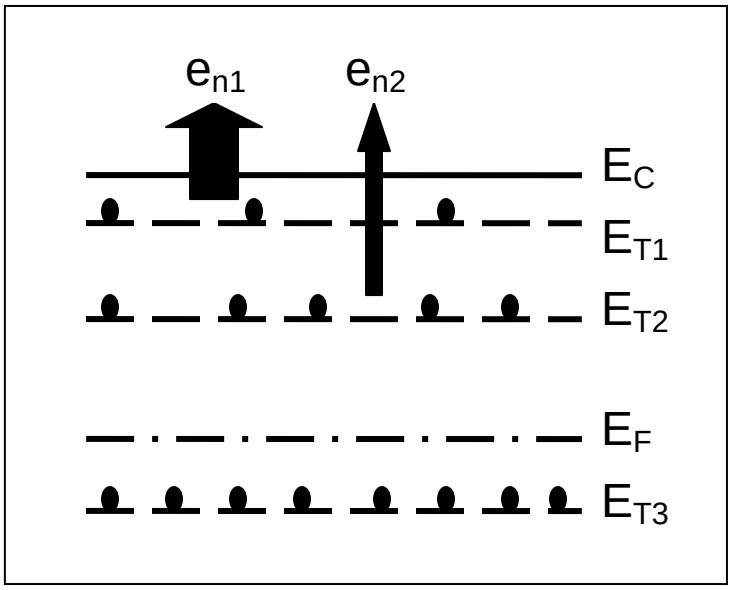


Figure. 3.3: Energy-band diagram of the upper band gap portion of the semiconductor at a flat band. Three discrete traps are present at E_{T1}, E_{T2}, and E_{T3} with respect to the conduction band minimum, E_C. E_F determines the trap occupancy, which is qualitatively indicated by the fraction of the trap states occupied by electrons (filled circles). The widths of the arrows represent the relative rate of trap emission.

Figure 3.3 shows an energy band diagram of the upper band portion of a semiconductor at flat-band with three discrete traps at E_{T1}, E_{T2}, and E_{T3} with respect to the conduction band minimum, E_C. E_F establishes trap occupancy. As indicated in Fig. 3.3, the deepest trap at energy E_{T3} is almost completely filled with electrons, because it is located below E_F. In contrast, the shallowest trap at E_{T1} traps very few electrons in steady-state because its shallow energy depth corresponds to it having a very large thermal emission rate, as given by

$$e_n = \sigma_n \upsilon_{th} N_c e^{-E_T / k_B T} \tag{3.17}$$

where υ_{th} is the thermal velocity. Thus, a deeper trap has a smaller trap re-emission rate and, hence, a larger steady-state occupancy than an otherwise identical but shallower trap; this translates into less drain current due to more trapping for a deeper trap.

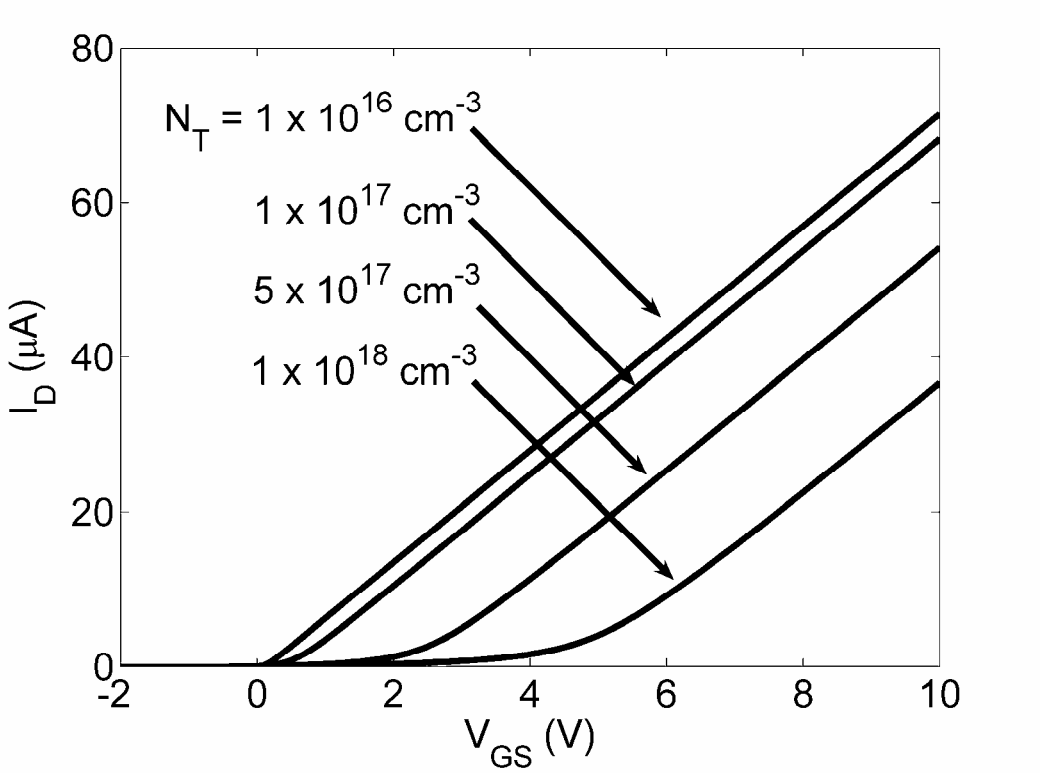


Figure 3.4: Drain current-gate voltage (I_D-V_{GS}) characteristics for an n-channel TFT corresponding to a drain voltage of 1 V and a trap depth of E_T - E_C= 0.15 *eV*. Geometrical and channel-based parameters employed for this simulation are: Z/L = 6:1, h = 20 nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, μ = 100 cm^2/V-s, and $n_{co} = 1 \times 10^{15}$ cm^{-3}.

The transfer characteristics (I_D-V_{GS}) of the TFT are also degraded by the presence of traps, as illustrated in Fig. 3.4. The primary effect of traps on the I_D-V_{GS} curves shown in Fig. 3.4 is a positive shift in the threshold voltage with increasing N_T, which is estimated from extrapolation of the linear portion of an I_D-V_{GS} curve to the V_{GS} axis. As discussed in Chapter 3.4.2, this shift in V_T results in a change in average

mobility. However, it is interesting to note that the slope of the curves are not affected by the increase in trap density, indicating that the incremental mobility of these curves are identical at high V_{GS}. Therefore the trend illustrated in Fig. 3.4 indicates, once more, that traps degrade the channel mobility. The origin of this V_T shift is related to the zero bias density of filled traps, n_{to}, which increases with increasing trap density, N_T.

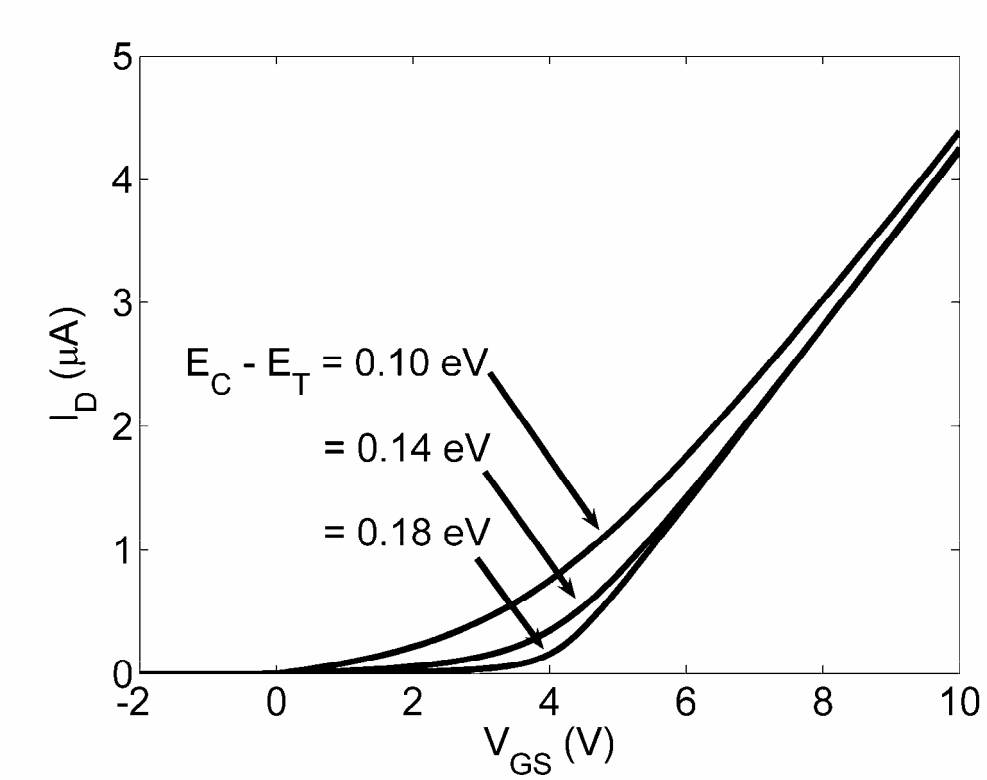


Figure 3.5: Drain current-gate voltage (I_D-V_{GS}) characteristics for an n-channel TFT corresponding to a drain voltage of 1 V and a trap density of $N_T = 8 \times 10^{17}$ cm^{-3}. An increase in the trap depth, $E_C - E_T$, causes a shift in the threshold voltage and a small change in the incremental mobility. Geometrical and channel-based parameters employed for this simulation are: Z/L = 6:1, h = 20 nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, μ = 100 cm^2/V-s, and $n_{co} = 1 \times 10^{14}$ cm^{-3}.

The trap depth, E_C - E_T, also affects the TFT threshold voltage as shown in Fig 3.5, as the trap depth increases from *0.1* to *0.18 eV*, the threshold voltage, as estimated by extrapolation of the linear portion of an I_D-V_{GS} curve to the V_{GS} axis,

changes from 3.2 to 4.0 V. This increase in threshold voltage with increasing trap depth is again physically related to the rate of trap re-emission. As explained earlier, the re-emission rate of electrons from traps decreases as the trap depth increases, resulting in larger equilibrium occupancy and, via Eq. (3.7), in a larger threshold voltage. A close examination of Fig. 3.5 reveals that the slope of the linear portion of an I_D-V_{GS} curve decreases slightly with increasing trap depth indicating a small amount of mobility degradation due to a deeper trap. A more detailed discussion of mobility and mobility degradation is presented in Chapter 3.4.2. Also, a more detailed discussion of the threshold voltage is given in the next subsection.

3.3. Subthreshold Current Considerations

Up to now, subthreshold current, i.e., the drain current obtained when the gate voltage is less than the threshold voltage, V_T, has not explicitly been considered. Here, V_T is a demarcation point, establishing the onset of subthreshold current. Additionally, V_T is sometimes used to quantify the onset of drain current conduction. However, an appreciable amount of drain current can flow even for gate voltages less than the threshold voltage, as is apparent from Fig. 3.6.

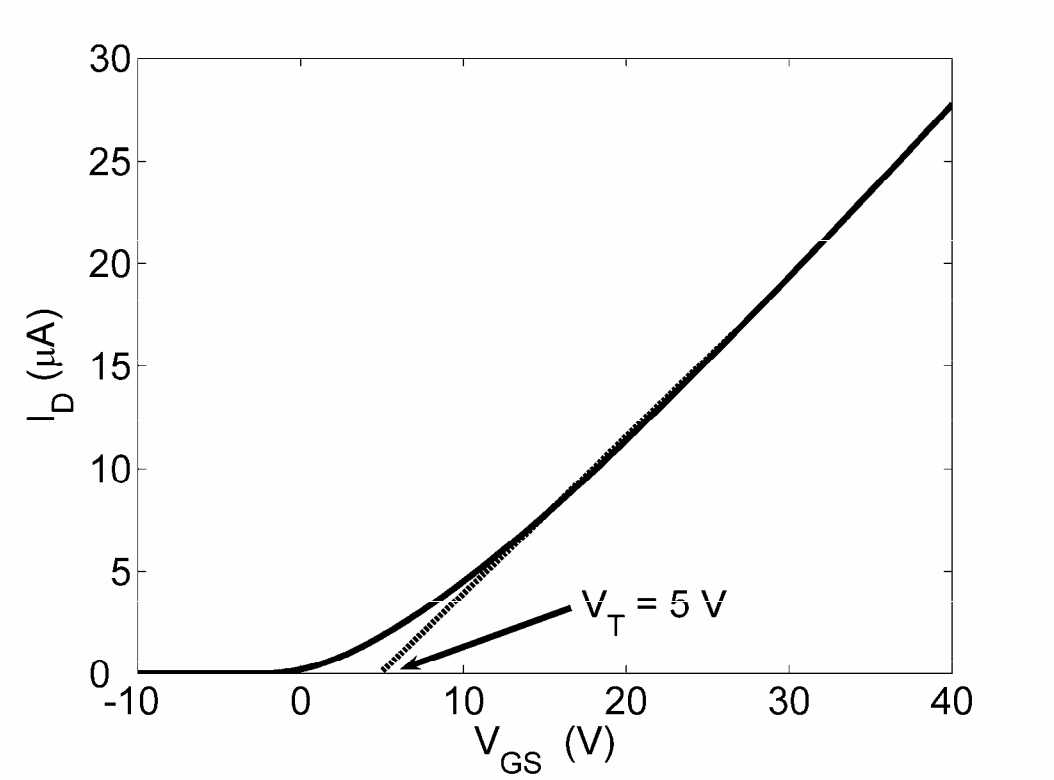


Figure 3.6: Drain current-gate voltage (I_D-V_{GS}) transfer curve for a zinc tin oxide, n-channel TFT. The threshold voltage is estimated to be ~ 5 V via extrapolation of the linear portion of this curve. Geometrical parameters for this TFT are Z/L = 5:1 and $C_G = 3.45 \times 10^{-8}$ F/cm^2.

Consider V_T and V_{ON} as drain current onset parameters for a prototypical zinc tin oxide TFT. Figure 3.6 illustrates the estimation of V_T via simple linear extrapolation of an I_D - V_{GS} transfer curve. As shown, the extrapolated value of V_T ~ 5 V is designated as the threshold voltage. Now, consider V_{ON}, which is evaluated using a log(I_D)-V_{GS} transfer, as shown in Fig. 3.7, and results in a value of -4 V for the same device. V_{ON} corresponds to the initial onset of appreciable drain current measured on a log(I_D)-V_{GS} transfer curve. This drain current onset occurs when I_D is larger than the gate leakage or the noise floor, which is established by the device under test and the precision of the measurement instrumentation. Additional

evaluation of Fig. 3.7 shows there is no compelling justification for selecting $V_T \sim 5$ V as a meaningful indicator of the onset of drain current. It is apparent that V_{ON} is a much more precise parameter to quantify drain current onset than V_T [8].

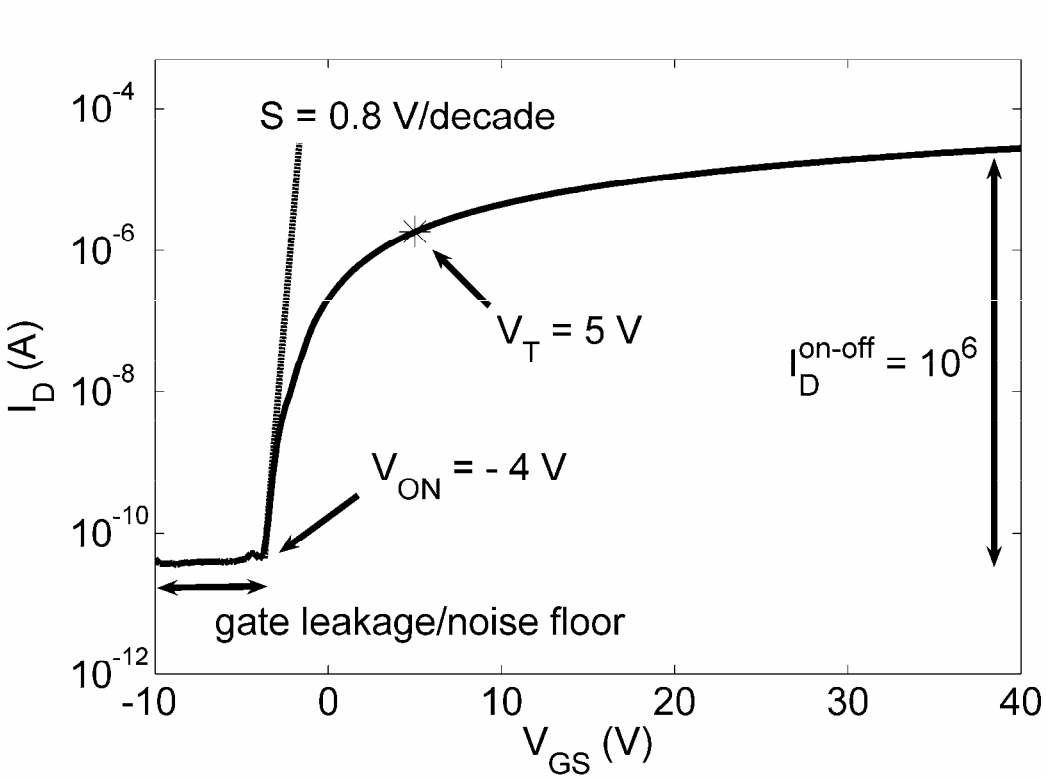


Figure 3.7: $Log(I_D)$-V_{GS} transfer curve for a zinc tin oxide, n-channel TFT. The voltage at which the TFT turns on is – 4 V. The previously extracted value of the threshold voltage, V_T = 5 V does not correspond to any obvious drain current onset. Geometrical parameters for this TFT are Z/L = 5:1 and $C_G = 3.45 \times 10^{-8}$ F/cm^2.

The other parameters labeled in Fig. 3.7 are the S parameter and the drain current on-to-off ratio. S is typically referred to as the inverse subthreshold voltage swing, but for the purposes of this thesis, S is used strictly according to its mathematical definition, $S = \left.\frac{\partial V_{GS}}{\partial \log(I_D)}\right|_{\min}$, and characterizes the effectiveness of the gate voltage in reducing the drain current to zero. A small value of S is desirable since this corresponds to a very sharp transition from on to off. The drain current on-

to-off ratio, $I_D^{on\text{-}off}$, is established by the maximum drain current and by V_{ON}. A large $I_D^{on\text{-}off}$ is desirable, since this corresponds to a more effective switch.

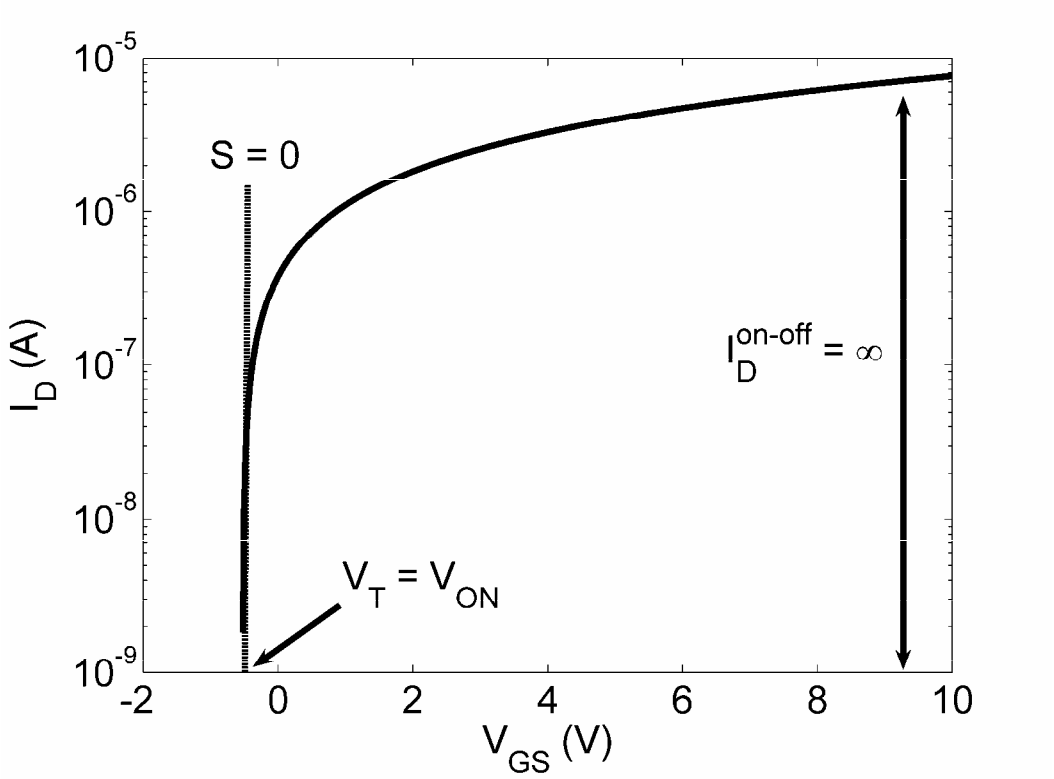
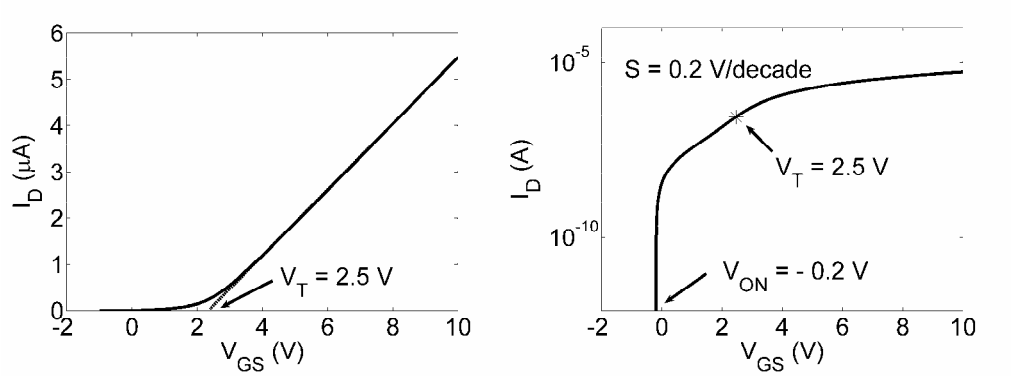


Figure 3.8: Log (I_D)-V_{GS} transfer curve simulation using the square-law model. In this ideal case, S = 0 V/decade, $V_T = V_{ON}$, and the drain current on-to-off ratio is infinite. For this simulation T = 300 K, V_{DS} = 100 mV, Z/L = 6:1, h = 20 nm, C_G = 6.04×10^{-8} F/cm^2, μ = 100 cm^2/V-s, and $n_{co} = 1 \times 10^{17}$ cm^{-3}.

Now, consider the ideal log(I_D)-V_{GS} transfer curve shown in Fig. 3.8. This curve is simulated using the ideal square-law model. Recall that the ideal square-law model assumes zero subthreshold current. This assumption leads to an ideal values of $V_T = V_{ON}$, $S = 0$, and $I_D^{on\text{-}off} = \infty$, as indicated in Fig. 3.8. Ignoring subthreshold current and electron trapping, V_T is equivalent to V_{ON}. S is equal to zero because electron trapping in the channel and/or at channel interfaces is not included in this model. $I_D^{on\text{-}off}$ is infinite because in this model gate leakage and instrumentation noise

are neglected. Thus, assessment of S and $I_D^{on\text{-}off}$ require 'real world' considerations involving traps and gate leakage/measurement noise to be taken into account.



(a) (b)

Figure 3.9: I_D-V_{GS} and log(I_D)-V_{GS} transfer curves simulated using the discrete trap model. For this simulation, T = 300 K, V_{DS} = 1 V, $N_T = 5 \times 10^{17}$ cm^{-3}, E_T = 0.15 eV below the conduction band minimum, Z/L = 6:1, h = 20 nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, μ = 100 cm^2/V-s, and $n_{co} = 1 \times 10^{15}$ cm^{-3}.

Figure 3.9 shows simulated I_D-V_{GS} and log(I_D)-V_{GS} transfer curves for a TFT using the discrete trap model. From Figs. 3.9a and 3.9b, V_T is estimated via linear extrapolation as ~ 2.5 V and V_{ON} is estimated ~ – 0.2 V, respectively.

Recall that the turn-on voltage is given by

$$V_{ON} = -\frac{qh}{C_G}\left(n_{co} + n_{to}\right), \tag{3.18}$$

where n_{co} and n_{to} correspond to the density of conduction band electrons and occupied trap states at zero bias. V_{ON} is quite small for this simulation. i.e., V_{ON} ~ - 0.2 V, as seen in Fig 3.9b, since n_{co} is chosen to be low. Since V_{ON} is negative, a negative gate voltage must be applied to remove free and trapped electrons from the channel.

V_T can also be defined quantitatively within the context of the discrete trap model. Based on the discrete trap model, V_T is equivalent to the gate voltage required to fill all traps. This is apparent by analyzing Eq. (3.8), yielding,

$$\begin{aligned} V_T &= V_{ON} + V_t + V_1 \\ &= \frac{qh}{C_G}\left(N_T - n_{to}\right) + \frac{qh}{C_G}\left(n_1 - n_{co}\right) \end{aligned} \tag{3.19a}$$

$$= V_{TRAP} + V_{ELECTRON}\,, \tag{3.19b}$$

where appropriate expressions have been substituted for V_{ON}, V_t and V_1. Rearranging the resulting equations, as shown in Eq. (3.19a), reveals that V_T is composed of two constituents, V_{TRAP} and $V_{ELECTRON}$. V_{TRAP} is associated to the gate voltage required to fill the empty traps, ($N_T - n_{to}$). However, V_{TRAP} neglects the change in conduction band electron density with applied gate voltage. This change is accounted for with $V_{ELECTRON}$. Moreover, evaluating Eq. (3.19a) using simulation parameters yields V_T = 2.5 V, which is equivalent to the estimate obtained from linear extrapolation of Fig. 3.9a.

Returning to Fig. 3.9b, as the gate voltage increases above V_{ON}, the drain current increases abruptly with an extremely large slope. As E_F moves closer to E_C and E_T, the steady-state trap occupancy, n_t increases, since $E_T - E_F$ is small. Over this domain of applied gate voltage, i.e. $-0.2 \leq V_{GS} \leq 2.5$ V, the slope of the $\log(I_D) - V_{GS}$ curve is controlled by the rate of steady-state trapping and results in a non-zero value of S; for the simulation shown in Fig. 3.9b, S is ~0.2 V/decade. Finally, at gate voltages greater than V_T, the Fermi level moves above the trap level, so that $E_T - E_F$ is negative and essentially all the traps are filled. Any further increase in the gate

voltage results in further accumulation of free electrons in the conduction band, corresponding to TFT operation without the influence of traps.

Comparing the $log(I_D) - V_{GS}$ plots for a real TFT and a simulated TFT with a discrete trap, as shown in Figs. 3.7 and 3.9b, respectively, it is apparent that the simulated curve is dissimilar to the measured curve (i.e., the simulated curve has a kink in the current near V_T) . This discrepancy is likely due to the discrete trap assumption (which is employed for computational simplicity); it is likely that there is a distribution of traps over a specific energy range. However, the overall effects of traps on device performance can still be evaluated using this discrete trap model and is summarized below.

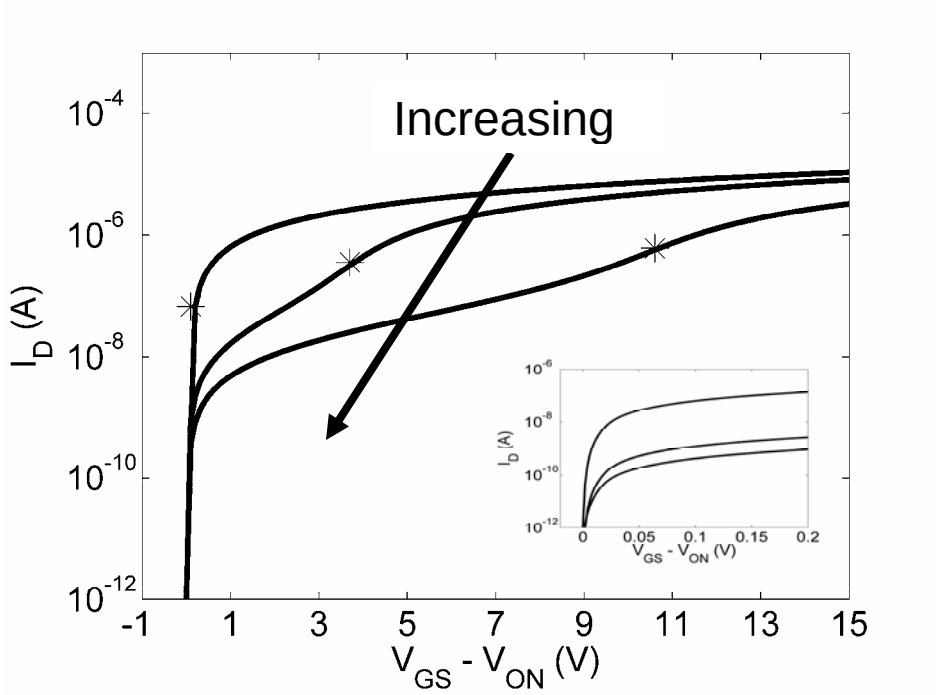


Figure. 3.10: Simulated $log(I_D) - (V_{GS} - V_{ON})$ transfer curves as a function of trap density, N_T, for a TFT using the discrete trap model. The arrow indicates the direction of increasing N_T, which are 1×10^{15}, 7×10^{17}, and 2×10^{18} cm^{-3} (and corresponds to V_{ON} = -0.1, -0.3, and -0.8 V, respectively) for these curves. V_{TRAP} is represented by '*' on each $log(I_D)$ curve. (Inset) The transfer characteristic near $V_{GS} - V_{ON}$ = 0 V is shown in the inset. For these simulations, V_{DS} = 1 V, Z/L = 6:1, h = 20 nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, μ = 100 cm^2/V-s, and $n_{co} = 1 \times 10^{17}$ cm^{-3}.

Simulated $\log(I_D) - (V_{GS}\text{-}V_{ON})$ transfer characteristics for three trap densities with a constant trap depth (i.e., $E_T \sim$ -0.15 eV) are shown in Fig. 3.10. For a trap density of 1×10^{15} cm^{-3}, V_{TRAP} is negligible. Thus, the corresponding $log(I_D)$ curve is close to that of an ideal TFT with no traps. This is not the case, however, when N_T is increased. As shown in Fig. 3.10, the current degrades as N_T is increased. Correspondingly, V_{TRAP} and S increase with increasing trap density; $V_{TRAP} \sim$ 0.01, 3.43, and 9.82 V and $S \sim$ 0.01, 0.3685, and 1.46 V/decade for $N_T = 1 \times 10^{15}$, 7×10^{17}, and 2×10^{18} cm^{-3}, respectively. S as a function of N_T is shown in Fig. 3.11; S is initially very small for trap densities less than 1×10^{17} cm^{-3} but increases significantly thereafter.

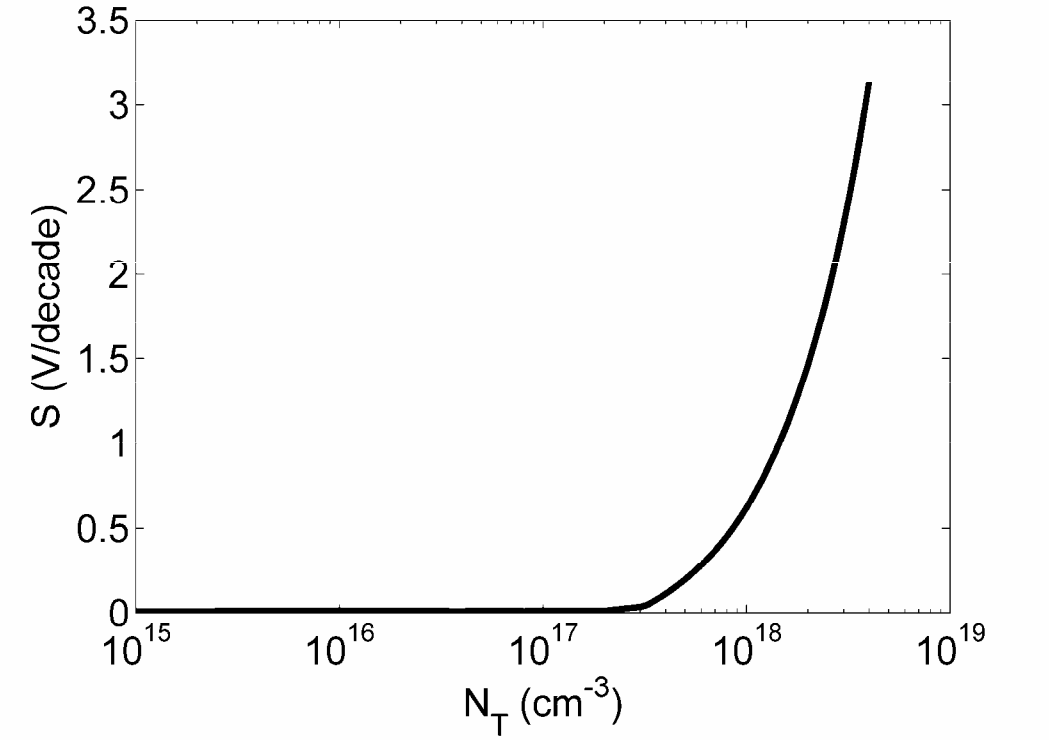


Figure 3.11: Simulated S as a function of N_T using the discrete trap model with a constant trap depth of $E_C - E_T = 0.15$ eV. For this simulation, $V_{DS} = 1$ V, $Z/L = 6{:}1$, $h = 20$ nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, $\mu = 100$ cm^2/V-s, and $n_{co} = 1 \times 10^{15}$ cm^{-3}.

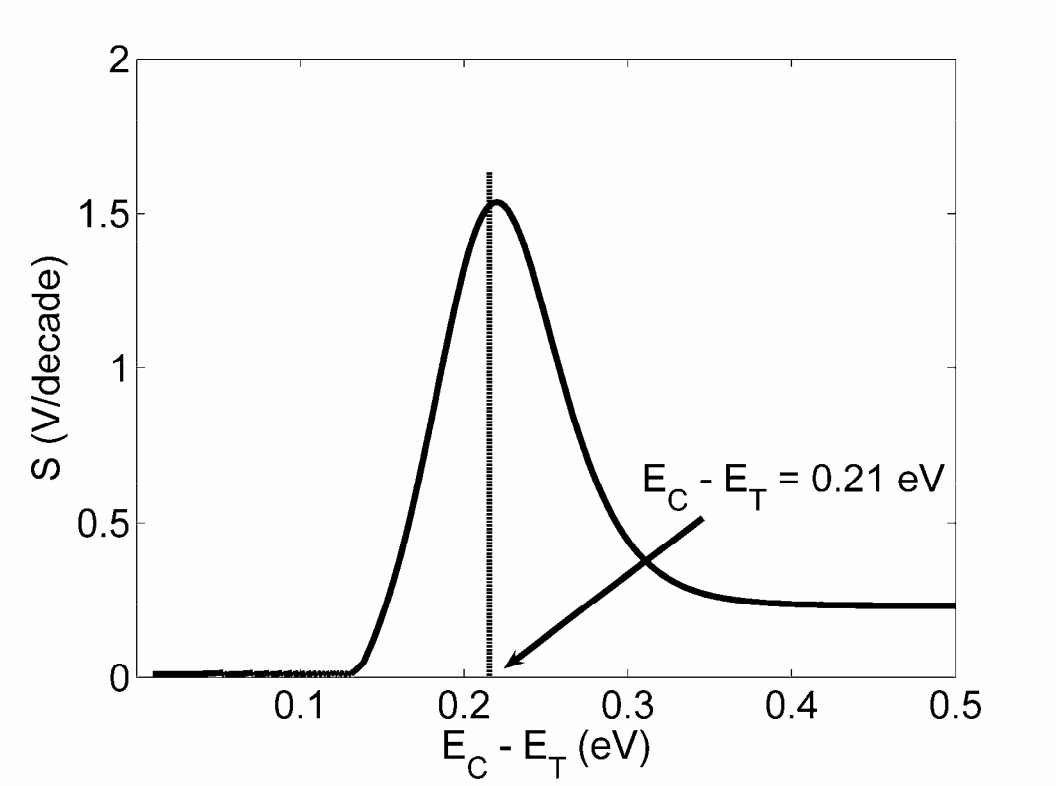


Figure 3.12: Simulated S as a function of trap depth, E_C - E_T, at a constant trap density of 5×10^{17} cm^{-3}. For this simulation, V_{DS} = 1 V, Z/L = 6:1, h = 20 nm, C_G = 6.04×10^{-8} F/cm^2, μ = 100 cm^2/V-s, and n_{co} = 1×10^{16} cm^{-3}.

The dependence of the trap depth, E_T, on S is shown in Fig 3.12 via simulation using the discrete trap model. For this simulation E_F = 0.21 eV below the conduction band, as established by n_{co}. S is small for shallow traps, i.e., $E_C - E_T \rightarrow 0$, since the gate voltage induces more electrons into conduction band states than into trap states because of their relative density of states. Moreover, the re-emission rate of electrons from shallow trap states, as given by Eq. (3.12), is very high so that their steady-state occupancy is relatively low. S increases as the trap energy increases up to E_F, but then decreases beyond E_F since these deep trap states are filled.

3.4. Mobility Degradation

3.4.1. Mobility

Mobility, μ, is defined as a linear proportionality constant relating the carrier drift velocity, v_d, to the applied electric field, ξ,

$$v_d = \mu\xi \,. \tag{3.20}$$

Ideally, the channel mobility of a TFT is a constant. However, if second order effects like interface roughness scattering, velocity saturation, electron trapping are taken into consideration, the channel mobility may vary with V_{DS} and V_{GS} [9, 10, 11].

Effective mobility, μ_{EFF}, and field-effect mobility, μ_{FE}, are the two commonly used definitions for the assessment of the mobility of carries in a field effect transistor. Effective mobility, μ_{EFF}, is extracted from the drain conductance, g_D, measured in the linear regime of operation. The expression for field effect mobility, using the pre-pinch-off square-law model in Eq. (2.6) of Chapter 2.3, at very small V_{DS} (i.e., $V_{DS} << V_{GS} - V_T$), can be derived as

$$\mu_{EFF} = \frac{g_D}{\frac{Z}{L} C_G \left(V_{GS} - V_T\right)}, \tag{3.21}$$

where $g_D = \frac{\partial I_D}{\partial V_{DS}}$ and denotes the drain conductance [11]. Similarly, field-effect mobility, μ_{FE}, is derived from the transconductance, g_m, where $g_m = \frac{\partial I_D}{\partial V_{GS}}$ and is given by,

$$\mu_{FE} = \frac{g_m}{\frac{Z}{L} C_G V_{DS}} \,. \tag{3.22}$$

Although μ_{EFF} and μ_{FE} are extensively employed in the technical literature as estimators of TFT channel mobility, a better approach is to use average and incremental mobility, μ_{AVG} and μ_{INC}, respectively, for channel mobility assessment. This preference is based on the fact that μ_{AVG} and μ_{INC} have precise physical interpretations, whereas μ_{EFF} and μ_{FE} do not [8].

The expression for average mobility is similar to Eq. (3.21) which is used to define μ_{EFF} except that V_T, is replaced by V_{ON}, yielding,

$$\mu_{AVG} = \frac{g_d}{\frac{Z}{L} C_G \left(V_{GS} - V_{ON} \right)}, \tag{3.23}$$

where V_{ON} corresponds to the onset of the flow of drain current, as assessed from a $\log(I_D) - V_{GS}$ curve. μ_{AVG} physically corresponds to the average mobility of the *total* carrier concentration in the channel. Incremental mobility, μ_{INC}, is given by,

$$\mu_{INC} = \frac{\frac{\partial g_d}{\partial V_{GS}}}{\frac{Z}{L} C_G}. \tag{3.24}$$

μ_{INC} physically corresponds to the mobility of the carriers that are incrementally added to the channel as the gate voltage incrementally increases in magnitude. This physical interpretation is based on the assumption that the mobility of carriers already present in the channel does not change.

In summary, μ_{AVG} provides a better predictor of device performance for circuit applications since it takes into account all of the carriers in the channel, whereas, μ_{INC} is of greater physical significance, as it is more directly correlated with the transport physics of carriers in the channel.

3.4.2. Mobility degradation due to a discrete trap

This subsection explores the effects of traps on the apparent average and the incremental mobility. μ_{AVG} and μ_{INC} are extracted from $I_D - V_{GS}$ curves simulated using the discrete trap model.

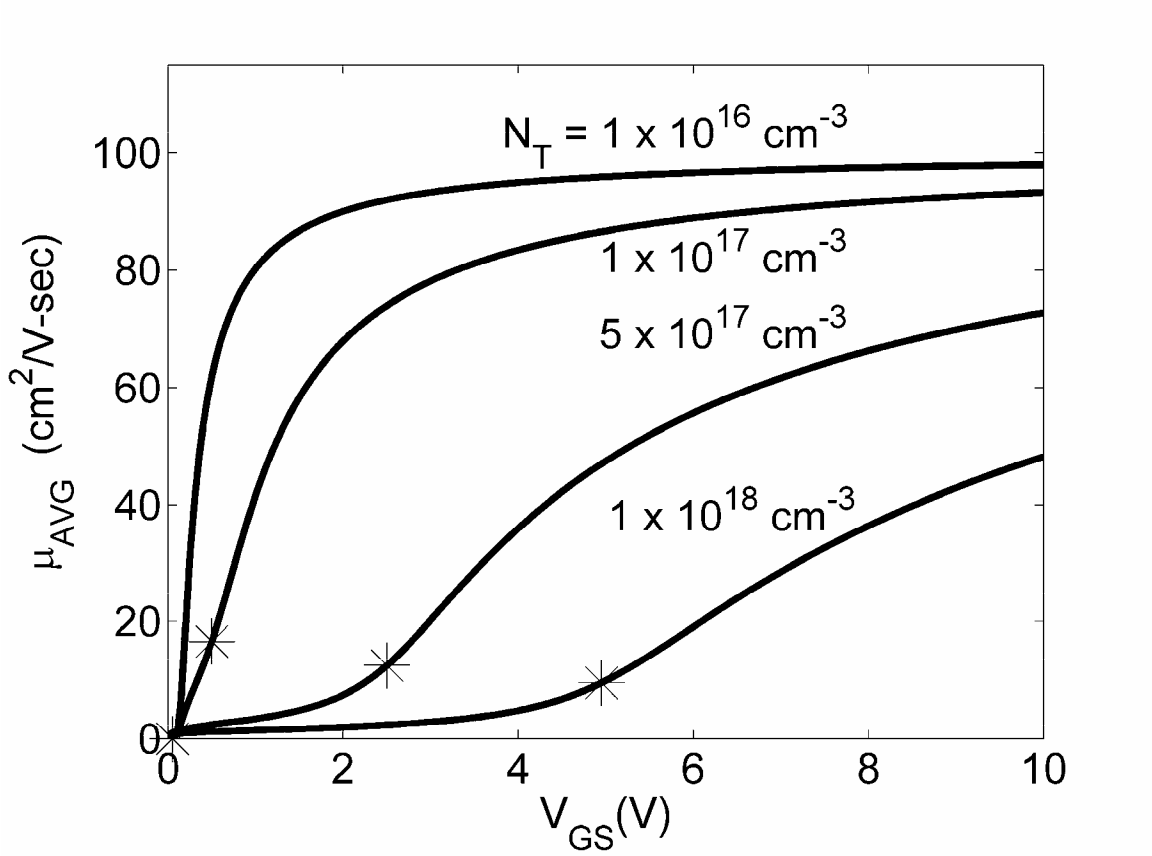


Figure 3.13: Simulated $\mu_{AVG} - V_{GS}$ characteristics as a function of trap density, N_T, for a trap depth of $E_C - E_T = 0.15$ eV and a drain voltage, $V_{DS} = 0.2$ V. The asterisk (*) on each $\mu_{AVG} - V_{GS}$ curve corresponds to V_{TRAP}, below which most of the gate voltage induced electrons are trapped. Model parameters used for this simulation: Z/L = 6:1, h = 20 nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, μ_{MODEL} = 100 cm^2/V-s, and $n_{co} = 1 \times 10^{15}$ cm^{-3}.

Figure 3.13 shows a family of $\mu_{AVG} - V_{GS}$ curves as a function of N_T extracted at $V_{DS} = 0.2$ V; μ_{MODEL} is 100 cm^2/V-sec. Figure 3.13 shows that for $N_T = 1 \times 10^{16}$ cm^{-3} $\mu_{AVG} - V_{GS}$ curve is close to ideal, since μ_{AVG} increases abruptly with an increasing gate voltage to a value close to that of the maximum value μ_{MODEL}.

The $N_T = 1 \times 10^{17}$ cm^{-3} $\mu_{AVG} - V_{GS}$ curve is less ideal, since it transitions less abruptly and saturates at a lower maximum mobility. For larger trap densities of 5×10^{17} cm^{-3} and 1×10^{18} cm^{-3} μ_{AVG} increases quite gradually, with most of the mobility increasing at $V_{GS} > V_{TRAP}$. The voltage, V_{TRAP}, below which the majority of the gate voltage induced electrons are trapped, is indicated by '*' on each of the $\mu_{AVG} - V_{GS}$ curves shown in Fig. 3.13. For gate voltages greater than V_{TRAP}, μ_{AVG} increases abruptly since most of the gate voltage induced electrons occupy the conduction band states.

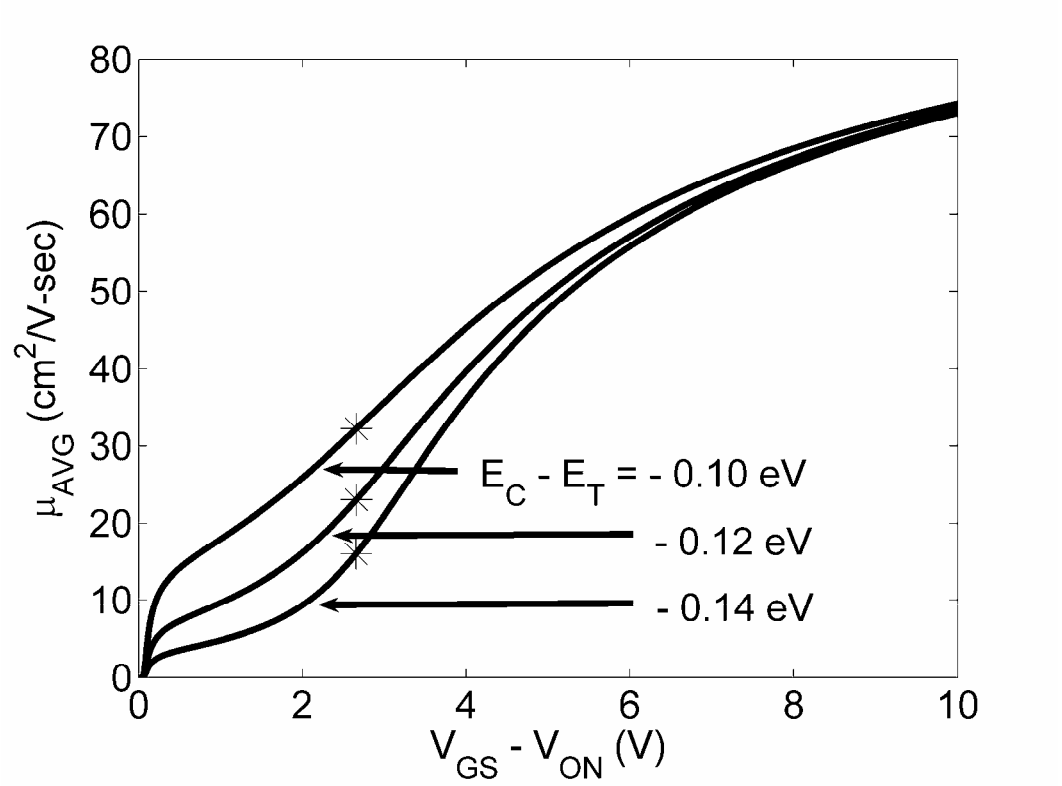


Figure 3.14: Simulated $\mu_{AVG} - (V_{GS} - V_{ON})$ characteristics as a function of trap depth, E_C - E_T, for a trap density of $N_T = 5 \times 10^{17}$ cm^{-3} and a drain voltage $V_{DS} = 0.2$ V. The asterisk (*) on each $\mu_{AVG} - V_{GS}$ curve corresponds to the voltage, V_{TRAP}, below which most of the gate voltage induced electrons are trapped. Model parameters used for this simulation: Z/L = 6:1, h = 20 nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, μ_{MODEL} = 100 cm^2/V-s, and $n_{co} = 1 \times 10^{15}$ cm^{-3}.

Figure 3.14 shows $\mu_{AVG} - V_{GS}$ curves as a function of trap depth $E_C - E_T$, at a constant trap density of 5×10^{17} cm^{-3}. Increasing trap density leads to decreasing

mobility for $V_{GS} \leq V_{TRAP}$ as traps are being filled. In contrast, μ_{AVG} is almost independent of trap depth at large values of V_{GS}, since all the traps are filled and the Fermi level is significantly above the trap level. Specifically, consider $V_{GS} = V_{TRAP} \approx V_T = 2.6$ V and notice that $\mu_{AVG} = 31, 21, 15$ cm^2/V-sec for trap depths 0.10, 0.12, and 0.14 eV below E_C. For this situation, the Fermi level is approximately located at the trap energy. Thus, the steady-state density of electrons in the conduction band is largest for the most shallow trap. Correspondingly, the highest mobility occurs for the most shallow trap since a larger fraction of the gate voltage-induced electrons occupy conduction band states.

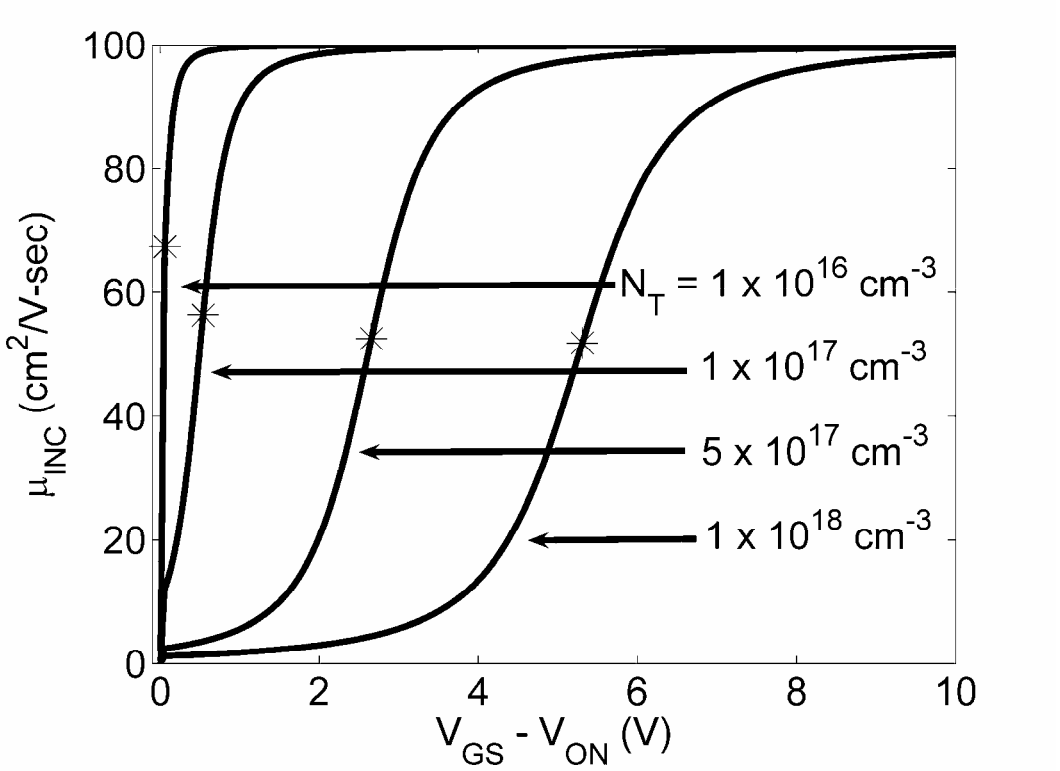


Figure 3.15: Simulated $\mu_{INC} - (V_{GS} - V_{ON})$ characteristics as a function of trap density, N_T for a trap depth $E_C - E_T = 0.15$ eV and a drain voltage $V_{DS} = 0.2$ V. The asterisk (*) on each $\mu_{INC} - V_{GS}$ curve corresponds to the voltage, V_{TRAP}, that acts as the 'mobility threshold voltage' value below which most of the induced electrons occupy the trap states. Model parameters used for this simulation: $Z/L = 6{:}1$, $h = 20$ nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, $\mu_{MDOEL} = 100$ cm^2/V-s, and $n_{co} = 1 \times 10^{15}$ cm^{-3}.

$\mu_{INC} - V_{GS}$ curves as a function of trap density, N_T, are shown in Fig. 3.15. As discussed previously μ_{INC} is the measure of the mobility of carriers differentially induced into the channel by an incremental increase in gate voltage. The $\mu_{INC} - V_{GS}$ curve transition for $N_T = 1 \times 10^{16}$ cm^{-3} is very close to an ideal step-function transition to the bulk mobility. As N_T increases, $\mu_{INC} - V_{GS}$ curves shift along the V_{GS} axes and the transition is less abrupt.

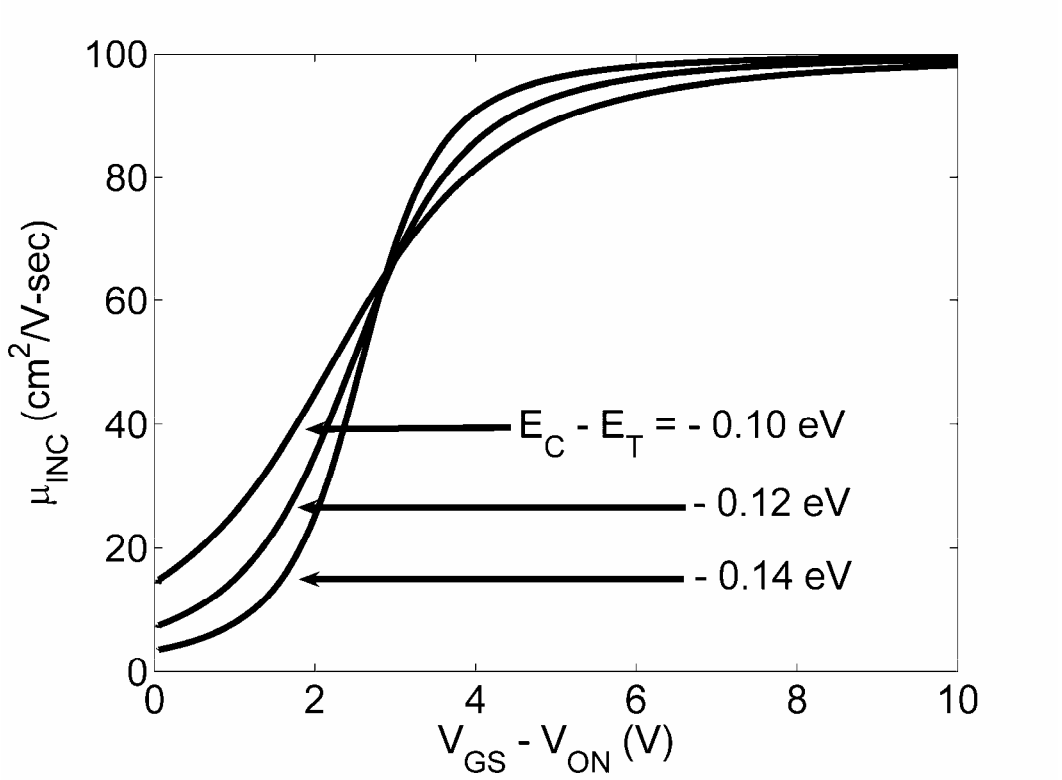


Figure 3.16: Simulated $\mu_{INC} - (V_{GS} - V_{ON})$ as a function of trap depth, E_C - E_T for trap density of $N_T = 5 \times 10^{17}$ cm^{-3} and a drain voltage, $V_{DS} = 0.2$ V. Model parameters used for this simulation: $Z/L = 6{:}1$, $h = 20$ nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, $\mu_{BULK} = 100$ cm^2/V-s, and $n_{co} = 1 \times 10^{15}$ cm^{-3}.

Figure 3.16 shows simulated $\mu_{INC} - V_{GS}$ curves as function of trap depth at a constant trap density of 5×10^{17} cm^{-3}. The important trend indicated in Fig. 3.16 is that the abruptness of the transition in the $\mu_{INC} - V_{GS}$ curve is steeper for deeper traps than for shallower traps. When a deep trap fills, the Fermi level is relatively remote

from E_C such that there are few filled conduction band states; μ_{INC} is correspondingly small. However, once the trap is completely filled, the Fermi level abruptly rises towards E_C, resulting in an abrupt increase in the density of filled conduction band states and concomitantly in an abrupt increase in μ_{INC}. In contrast, for a shallow trap, the Fermi level is much more closer to E_C such that conduction band filling and the μ_{INC} transition is less abrupt.

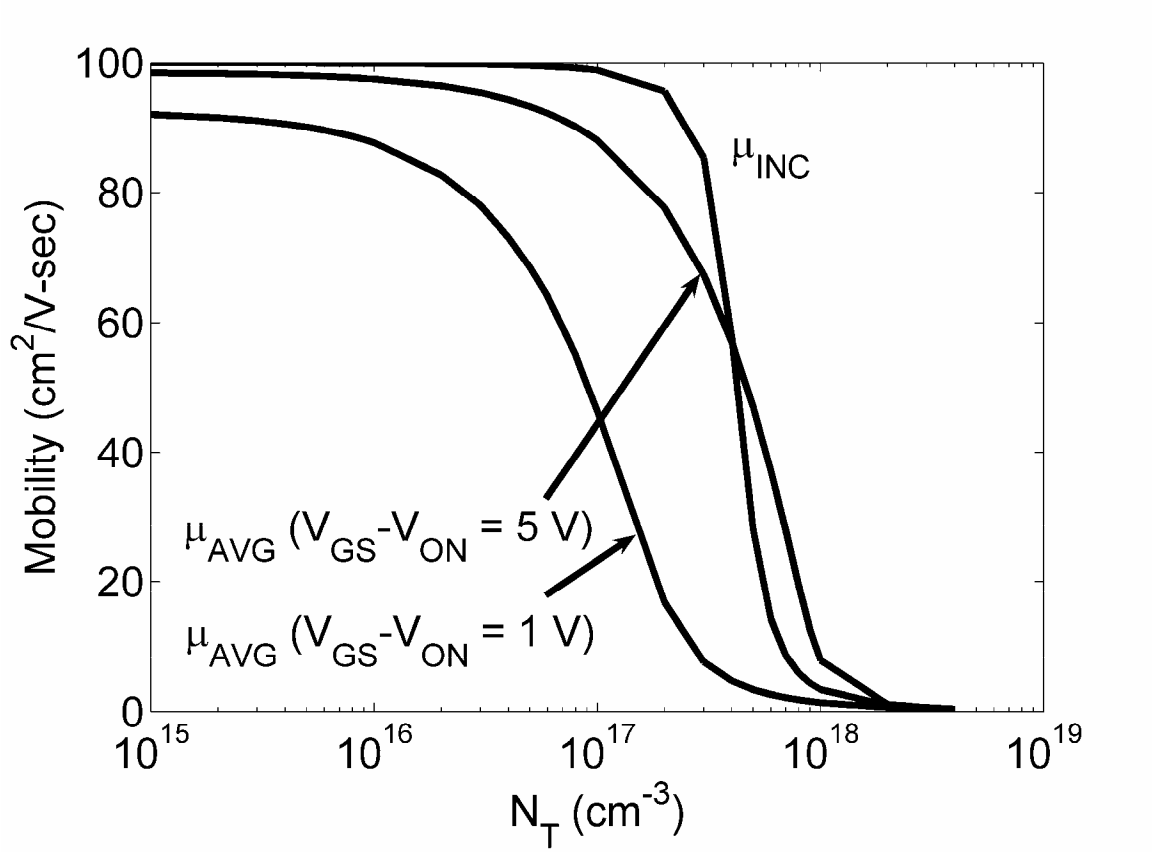


Figure 3.17: Simulated μ_{INC} and μ_{AVG} characteristics as a function of trap density, N_T. Model parameters used for this simulation: Z/L = 6:1, h = 20 nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, μ_{MODEL} = 100 cm^2/V-s, and $n_{co} = 1 \times 10^{15}$ cm^{-3}.

Figure 3.17 shows simulated μ_{AVG} and μ_{INC} curves as a function of trap density, N_T. μ_{AVG} is calculated at a drain voltage V_{DS} = 0.1 V and overvoltages of 1 V and 5 V, i.e., $V_{GS} = V_{ON} + 1$ V and $V_{GS} = V_{ON} + 5$ V, respectively. μ_{INC} is calculated at

V_{GS} = 0.2 V. Clearly above a certain trap density, $N_T \geq 3 \times 10^{17}$ cm^{-3} for this simulation, the mobility drastically decreases since most of the gate-induced channel electrons are trapped. On the other hand, when the trap concentration is reduced to less than ~10^{17} cm^{-3}, μ_{INC} is not affected by traps. At a small overvoltage, μ_{AVG} is more sensitive to the trap density, and never reaches the maximum bulk mobility even when the trap density is very low. At a large overvoltage and low trap density, μ_{AVG} approaches the bulk mobility, since the density of induced conduction band electrons is significantly larger than the trapped electron density.

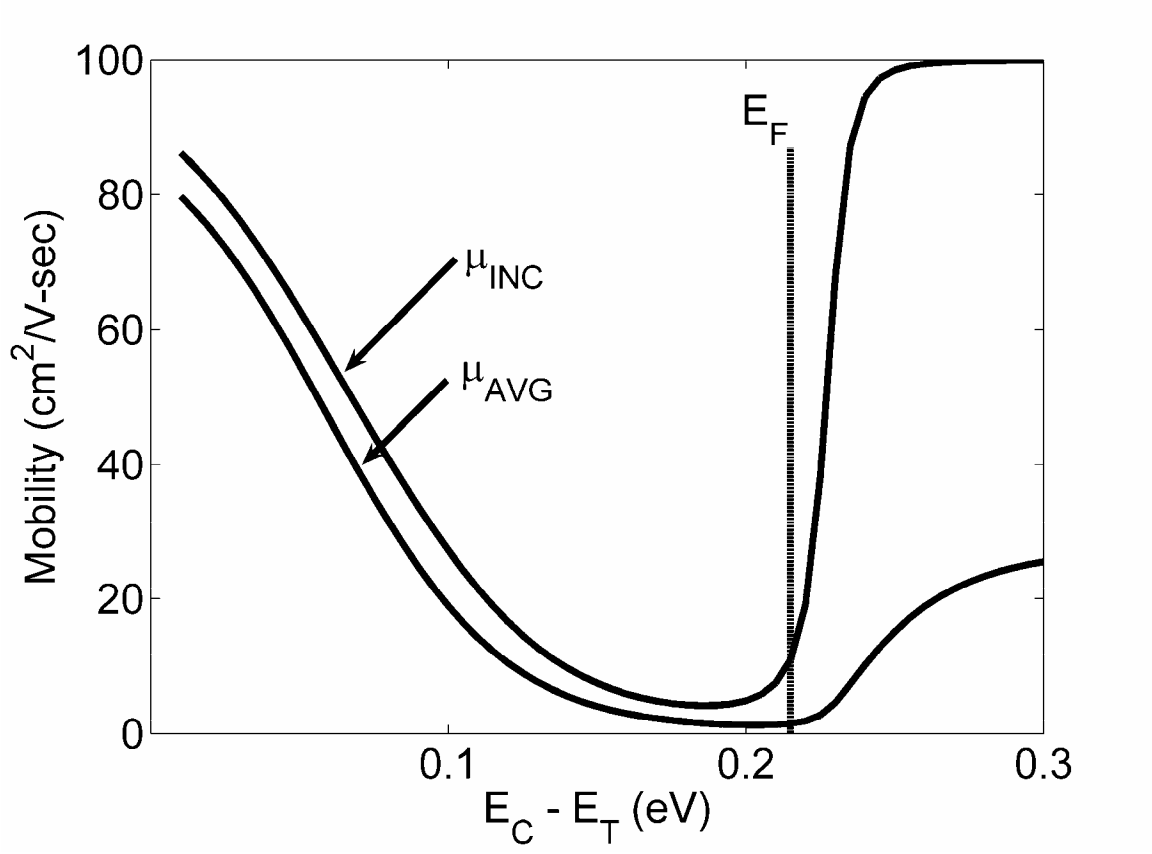


Figure 3.18: Simulated μ_{INC} and μ_{AVG} characteristics as a function of trap depth, $E_C - E_T$. The Fermi level, E_F, as established by the initial free carrier concentration is 0.21 eV below the conduction band minimum, E_C. Model parameters used for this simulation: Z/L = 6:1, h = 20 nm, $C_G = 6.04 \times 10^{-8}$ F/cm^2, μ_{BULK} = 100 cm^2/V-s, and $n_{co} = 1 \times 10^{15}$ cm^{-3}.

Simulated μ_{AVG} and μ_{INC} curves as a function of trap depth, $E_C - E_T$, are shown in Fig 3.18. μ_{AVG} and μ_{INC} are calculated at a gate voltage of 1 V. The Fermi level, E_F, as established by the initial free carrier concentration, $n_{co} = 1 \times 10^{15}$ cm^{-3} is 0.21 eV below E_C. As $E_C - E_T$ increases, both μ_{AVG} and μ_{INC} monotonically decrease in a very similar manner until $E_T \sim E_F$. This trend is a consequence of the fact that a larger fraction of the gate voltage induced electrons occupy trap states for a deeper trap. When E_T drops below E_F, both mobilities monotonically increase, and μ_{INC} attains a maximum value, μ_{MODEL}. When all the traps are deep and remain filled, they play no role in establishing μ_{INC} so that all of the electrons differentially induced into the channel by an incremental increase in the gate voltage occupy conduction band states. In contrast, μ_{AVG} is significantly smaller than μ_{INC} since it is a measure of all the electrons in the channel, the majority of which are trapped.

4. CONCLUSIONS AND RECOMMENDATION FOR FUTURE WORK

4.1. Conclusions

The primary goal of this thesis is to develop a trap- based TFT model in order to elucidate TFT device physics trends. The work presented in this thesis can be summarized according to four categories: development of the discrete trap model for a TFT, analysis of simulated output ($I_D - V_{DS}$) and transverse ($I_D - V_{GS}$) characteristics using the discrete trap model, the effect of a discrete trap on the subthreshold current, and mobility degradation due to a discrete trap. Conclusions are briefly summarized in context on these four categories.

First, starting with the model developed by Sze, a set of equations is developed to describe current-voltage characteristics of a TFT, taking into consideration a discrete acceptor-like trap. Drain current expressions are obtained for the pre-pinch-off and the post-pinch-off regimes of TFT operation, employing two model parameters, the trap density, N_T, and the trap energy depth, E_T.

Second, simulations based on the discrete trap model are performed, and the results are analyzed. $I_D - V_{DS}$ simulations show that the drain current, I_D, decreases with an increase in N_T and E_T. However, it is evident from simulation that traps below the Fermi level, E_F, do not have a strong effect on I_D. Similar I_D degradation trends are evident from simulated $I_D - V_{GS}$ transfer characteristics. It is also evident from the $I_D - V_{GS}$ simulations that V_T exhibits a positive voltage shift with an increase in N_T or E_T. The effect of N_T is stronger than the effect of E_T in shifting V_T.

Third, log (I_D)–V_{GS} simulations are performed in order to explore the effect of traps on the subthreshold current. A mathematical expression for V_T is derived and is

found to be composed of two components, V_{TRAP}, the gate voltage required to fill all the traps, and $V_{ELECTRON}$, the voltage corresponding to populating conduction band electron states. The inverse subthreshold voltage swing, S, is extracted from $\log(I_D) - V_{GS}$ curves simulated at different values of N_T and E_T. S increases monotonically as N_T increases above 1×10^{17} cm^{-3}. Also, S increases with increasing E_T, but only when $E_T < E_F$. S decreases as E_T increases below E_F, reiterating the fact that filled traps do not have a strong effect on TFT operation.

Finally, the average mobility, μ_{AVG}, and incremental mobility, μ_{INC}, are extracted from $I_D - V_{DS}$ and $I_D - V_{GS}$ curves, respectively. $\mu_{AVG} - V_{GS}$ curves show that μ_{AVG} is small until $V_{GS} < V_T$. μ_{AVG} increases as V_{GS} is further increased, and eventually saturates at a value below μ_{BULK}. The saturated value of μ_{AVG} decreases with increasing N_T. μ_{AVG} also decreases as E_T increases at smaller values of V_{GS}. However, at higher gate voltages all the traps are filled and hence E_T has no effect on TFT operation. Simulated $\mu_{INC} - V_{GS}$ curves show that μ_{INC} increases rapidly to μ_{BULK} for $V_{GS} > V_T$. As N_T increases, $\mu_{INC} - V_{GS}$ curves shift to the right along the V_{GS} axis and the transition from low mobility to μ_{BULK} is less abrupt. An increase in E_T effects only the slope of a $\mu_{INC} - V_{GS}$ curve. A $\mu_{INC} - V_{GS}$ curve is steeper for deeper traps than for shallow traps.

4.2. Recommendations for future work

Although the discrete trap model provides insight into the effects of traps on TFT performance, there are areas where it can be improved. A major deficiency of the discrete trap model is that it only considers a discrete, acceptor-like trap.

Inclusion of donor-like and/or distributed trap states would improve the scope and applicability of the model. The presence of traps at semiconductor-contact interfaces could also be included. Finally, the current version of the discrete trap model only accounts for DC operation. Transient modeling of traps is not accomplished. Transient modeling of traps and inclusion of parasitic capacitances would allow for transient and AC analysis of TFTs.

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