

A Comparative Study of 20-Gb/s NRZ and Duobinary Signaling Using Statistical Analysis

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Abstract—A statistical analysis technique for estimating bit-error rate (BER) and eye opening is presented for both NRZ and duobinary signaling schemes. This method enables fast and accurate BER distribution simulation of a serial link transceiver including channel and circuit imperfections, such as finite pulse rise/fall time, duty cycle variation, and both receiver and transmitter forwarded-clock jitter. A comparison between 20-Gb/s NRZ and duobinary transmitters using this simulator shows that while duobinary transmission relaxes the requirements on the receiver equalizer due to the lower Nyquist frequency of the transmitted data, significant eye-opening and BER degradation can arise from clock non-idealities. The proposed statistical analysis is verified against traditional time-domain, transient eye-diagram simulations at 20-Gb/s, transmitted through measured s-parameter channel characteristics.

Index Terms— Bit-error rate (BER), inter-symbol interference (ISI), eye diagram, jitter, duobinary, non-return-to-zero (NRZ), serial link.

Footnotes

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I. INTRODUCTION AND MOTIVATION

The demand for higher bandwidth chip-to-chip interconnections has been increasing dramatically, as future many-core systems require significant aggregate I/O bandwidth to keep computational units occupied. Recent publications have shown that hundreds of Gb/s to several Tb/s of off-chip bandwidth will be required for future applications [1], [2]. Fortunately, link parallelization [3], [4], circuit innovations, and higher transistor transition frequency (f_T) due to CMOS transistor scaling can help enable energy-efficient, off-chip communications. On the other hand, lossy channel bandwidth critically limits the maximum data rate due to inter-symbol interference (ISI), making a higher order modulation (e.g. PAM-4, partial response such as duobinary) necessary.

Chip-to-chip communications can show widely varying channel losses (e.g. -3dB to -30dB at Nyquist) due to variations in trace length, PCB material, connector type, via stubs, and proximity to aggressor signal coupling. For next generation serial links above 20-Gb/s data rate, such as in short-range chip-to-chip applications [5], the channel typically exhibits moderate losses of -20dB or less. Fig. 1 depicts the measured channel losses of typical FR4 PCB traces from 10cm to 80cm long, showing that for a 40cm trace length, the measured channel loss at 10GHz is -18.9dB. While such channel losses may contribute to a reduced signal-to-noise ratio (SNR) in the eye opening, other non-ideal effects beyond channel losses may also contribute to performance degradation, such as PLL jitter, crosstalk, duty cycle distortion (DCD), jitter amplification, and finite rise/fall time of the data symbol.

Besides the issue of channel and circuit impairments, another critical problem is the difficulty in achieving simulation accuracy at the circuit transistor level for data rates above 20-Gb/s. As data rate goes up, the time step for simulation becomes smaller. Therefore, excessive transient simulation time is required for the same accuracy; otherwise, simulation inaccuracy will appear due to the incomplete characterization of the link performance. For example, the simulation length of a random input sequence exhibiting error-free operation should be at least three times the inverse of the expected bit-error rate (BER), in order to obtain reasonable accuracy with a 95% confidence level [6]. For a typical serial link application with an expected BER of 10^{-12} , the data sequence needs to be at least 3×10^{12} symbols long, which requires a significant amount of simulation time even for a 64-bit workstation. Moreover, to accurately model the jitter, duty cycle variation and finite symbol rise/fall time, the time step of the simulator must be further reduced, again resulting in increased simulation time. Worst-case analysis has been proposed in [7], [8] for obtaining quick link estimation, but is unable to provide more complete link characteristics, such as BER versus eye sampling location.

Statistical analysis techniques [7], [9]-[12] enable accurate and more efficient methods to estimate the performance of serial links beyond conventional transient simulations. These simulators calculate the BER distribution plot by convolving the probability density function (PDF) of all individual cursors of the pulse response. While the PDF of interference sources such as crosstalk can be easily added by summing the corresponding

aggressor responses, timing uncertainty such as accurate analysis of transmitter jitter is more difficult to perform [10]. For example, the original work in [7] simply treats transmitter jitter similarly to receiver jitter, though it has travelled through the lossy channel which causes jitter amplification. In [9], jitter from both the transmitter and receiver are converted to an equivalent voltage noise, based on a jittered pulse decomposition model that gives accurate results in the voltage domain. Extending on the work in [7], a more accurate analysis of transmitter jitter was proposed in [10], [11], which requires extensive calculations to take almost every possible position of the transmitted pulse shapes into account according to the PDF of the transmitter jitter. However, this will degrade the efficiency of the statistical analysis. Furthermore, it treats individual transmit jitter shaped by the PDF separately as a time offset from an ideal pulse, regardless of its frequency content. This can be problematic, as the transmitted sequence will be fed to an ideal high-pass filter in order to capture the jitter amplification at high frequency [13], [14] -- resulting in the same inaccuracy problem as the conventional transient simulation mentioned above. For 20-Gb/s data rates or above, these timing uncertainties become even more critical for accurate analysis and prediction of link performance across various modulation schemes.

In this paper, we propose a statistical analysis technique for multi-Gb/s serial links that not only includes the effect of channel loss such as ISI and equalization, but also predicts the effects of transmitter jitter amplification, random receiver jitter, finite rise/fall time, and clock duty cycle variation. Furthermore, this analysis at 20-Gb/s data rate compares the conventional NRZ signaling with duobinary modulation, which has recently been

shown to relax the requirements on the channel equalization [15], [16], assuming a simplified, ideal clock behavior. In order to understand the proposed statistical analysis methodology, we first present an overview of NRZ and duobinary signaling in Section II. In Section III, the proposed statistical method is described, along with the enhancements needed to accurately model the timing inaccuracies. In Section IV, simulation results using actual measured channel characteristics are presented, thereby verifying the statistical analysis implementation.

II. OVERVIEW OF NRZ AND DUOBINARY SIGNALING

NRZ signaling is commonly used in high-speed chip-to-chip communications due to its simplicity and therefore straightforward design in both the transmitter and receiver circuit architectures. In the frequency domain, its main spectral lobe occupies bandwidth up to its data rate of $1/T_b$, where T_b is the period of a symbol. To relieve ISI due to channel loss, equalization is predominantly used to flatten the channel response. The tap coefficients of the equalization filter can be calculated by zero-forcing the nearby cursors except for the main cursor. For example, the coefficients $(c_{-1} \ c_0 \ c_1 \ c_2)^T$ of a 4-tap feed-forward equalization (FFE) for a channel pulse response shown in Fig. 2 can be solved by

$$\begin{pmatrix} \mathbf{g}_{-1} \\ \mathbf{g}_0 \\ \mathbf{g}_1 \\ \mathbf{g}_2 \end{pmatrix} = \begin{pmatrix} \mathbf{g}_{F,0} & \mathbf{g}_{F,-1} & \mathbf{g}_{F,-2} & \mathbf{g}_{F,-3} \\ \mathbf{g}_{F,1} & \mathbf{g}_{F,0} & \mathbf{g}_{F,-1} & \mathbf{g}_{F,-2} \\ \mathbf{g}_{F,2} & \mathbf{g}_{F,1} & \mathbf{g}_{F,0} & \mathbf{g}_{F,-1} \\ \mathbf{g}_{F,3} & \mathbf{g}_{F,2} & \mathbf{g}_{F,1} & \mathbf{g}_{F,0} \end{pmatrix} \begin{pmatrix} c_{-1} \\ c_0 \\ c_1 \\ c_2 \end{pmatrix} \quad (1)$$

where targeted cursors $(g_{-1} \ g_0 \ g_1 \ g_2)^T$ are $(0 \ 1 \ 0 \ 0)^T$ for NRZ; $g_F(t)$ is the pulse response of the channel and $g_F(t-kT_b)$ is noted as $g_{F,k}$.

Duobinary is a partial response signaling scheme that introduces controlled ISI to reduce the transmitted bandwidth. Its main spectral lobe occupies bandwidth up to only half the data rate, or $1/2T_b$. In theory, duobinary is performed as the exclusive-or sum of the current bit and the preceding one within a NRZ sequence, resulting in a 3-level signaling constellation [17]. In practice, it can be achieved by combining both the channel low-pass characteristics and the transceiver equalization together. For example, the coefficients of a 4-tap FFE used for duobinary can be calculated from (1) with targeted cursors $(g_{-1} \ g_0 \ g_1 \ g_2)^T$ equivalent to $(0 \ 0.5 \ 0.5 \ 0)^T$. To prevent error propagation, a precoder and decoder must be implemented at baseband. Fig. 2 and Fig. 3 show the pulse and frequency responses before and after equalization for both NRZ and duobinary signaling, using a 4-tap FFE through a 40cm FR4 PCB trace at a 20-Gb/s data rate. The smaller bandwidth of duobinary modulation confirms its higher spectral efficiency, showing less loss than NRZ for the same data rate.

A general block diagram of a serial link transceiver for chip-to-chip interconnection is shown in Fig. 4. On the transmitter side, several data sequences are multiplexed, with the transmitted symbol pulse width and position determined by the clock shape and data multiplexing ratio. The multiplexed data sequence $\{d_k\}$ is equalized by the FFE and fed into the channel by the output driver. After passing through a receiver linear equalizer

(LE) and/or nonlinear decision feedback equalizer (DFE), the data is then recovered and demultiplexed by the quantizer(s). For NRZ signaling, the receiver uses the quantizer to slice the 2-level analog input into a single digital value. For duobinary modulation, an LSB distiller or 3-level ADC [16] (not shown in Fig. 4 for simplicity) is necessary to convert the recovered sequence to NRZ, resulting in two digital outputs for each 3-level duobinary analog input.

III. STATISTICAL METHOD ON SERIAL LINK

A. Background of Statistical Analysis

As previously mentioned in Section I, since the BER for a typical serial link can be less than 10^{-12} and random noises are boundless, transient simulations of eye diagrams and SNR are both excessively time-consuming and difficult to process (due to the large amount of sampled data). Statistical analysis, on the other hand, can give a detailed eye plot of the BER distribution across both different timing offsets and decision thresholds [7], [9]-[11]. Based on the transmitted pulse response through the channel, statistical analysis convolves all the PDFs of the residual ISI to produce the BER eye. For NRZ signaling, the PDF of the ISI from the k^{th} preceding bit can be expressed as

$$ISI_k = P_0\delta(x) + P_1\delta(x - g_{F,k}), \quad k \neq 0 \quad (2)$$

where P_0 and P_1 are the probability of transmitting ZERO and ONE symbols, with typical values of 0.5 for equal possibility of ZERO and ONE. $\delta(x)$ is the unit impulse function. When $k > 0$, ISI results from the postcursor tails of previous bits, while when $k < 0$, the

ISI arises from the precursor of proceeding bits. The total ISI is then calculated by convolving all the ISIs as:

$$ISI = \dots \otimes ISI_{-2} \otimes ISI_{-1} \otimes ISI_1 \otimes ISI_2 \otimes \dots \quad (3)$$

The PDFs of the main cursor with symbols ZERO and ONE are:

$$main_0 = \delta(x), \quad main_1 = \delta(x - g_{F,0}) \quad (4)$$

Then the PDFs of ZERO and ONE interfered by the ISI are:

$$pdf_0 = main_0 \otimes ISI, \quad pdf_1 = main_1 \otimes ISI \quad (5)$$

Hence, the BER of NRZ signaling for a given decision threshold y_T can be written as:

$$\begin{aligned} BER_{NRZ}(y_T) &= P_0 \cdot P(D_1 | H_0) + P_1 \cdot P(D_0 | H_1) \\ &= P_0 \int_{y_T}^{\infty} pdf_0 dx + P_1 \int_{-\infty}^{y_T} pdf_1 dx \end{aligned} \quad (6)$$

where $P(D_1|H_0)$ is the probability of transmitting a ZERO but mistaking it as a ONE at the receiver, while $P(D_0|H_1)$ is the opposite scenario. The BER distribution at any single time instance is obtained by sweeping y_T across the input dynamic range. After repeating the above steps across one complete symbol period, the entire BER eye plot can be derived.

B. Statistical Analysis for duobinary

Duobinary modulation introduces controlled ISI, implicit within the coding. Therefore, there exist two large distributions (one caused by the main cursor and the other by the 1st postcursor) in pdf_0 and pdf_1 , instead of only one as in case of NRZ. Also because of the three-level signaling, two decision boundaries v_{TH1} and v_{TH2} need to be set in order to obtain the BER for duobinary:

$$BER_{duo}(y_T) = \begin{cases} \int_{y_T}^{v_{TH1}} (P_0 \cdot pdf_0 + P_1 \cdot pdf_1) dx, & y_T \leq v_{TH1} \\ \int_{v_{TH1}}^{y_T} (P_0 \cdot pdf_0 + P_1 \cdot pdf_1) dx, & v_{TH1} < y_T < v_{mid} \\ \int_{y_T}^{v_{TH2}} (P_0 \cdot pdf_0 + P_1 \cdot pdf_1) dx, & v_{mid} \leq y_T < v_{VT2} \\ \int_{v_{TH2}}^{y_T} (P_0 \cdot pdf_0 + P_1 \cdot pdf_1) dx, & v_{TH2} \leq y_T \end{cases} \quad (7)$$

where v_{mid} is the position of the peak impulse from the sum of pdf_0 and pdf_1 . The decision boundaries v_{TH1} and v_{TH2} can be obtained by searching for the minimum BER located around the position of $v_{mid} \pm 0.5 \max(g_F(t))$, such that the BER can be low enough to open the eye near the boundaries.

C. Clock Non-idealities

In addition to ISI, clock non-idealities such as transmitter jitter, receiver jitter, rise/fall time and duty cycle variation will also degrade the performance of a serial link receiver.

When the jittery data sequence is transmitted through the channel and arrives at the input of the receiver, the jitter value will be increased, especially for its high frequency portion. This is typically referred to as jitter enhancement or jitter amplification in [13], [14], and

it worsens as data rate increases. One way to quantify the amount of jitter amplification is to use the jitter impulse response (JIR) and jitter transfer function (JTF). The JIR at a given data rate can be extracted by comparing the ideal zero-crossings with the zero-crossings of the response where the data sequence gives a single-shot of a small time offset. Then JTF can be obtained by calculating the Fourier transformation of the JIR. Fig. 5 shows the JIR and JTF of the 40cm FR4 PCB trace at a 20-Gb/s data rate. Assuming the transmitter jitter sequence J_{TX} is wide-sense stationary (WSS), the mean of the jitter response at the input of the receiver J'_{TX} can be expressed as:

$$E[J'_{TX}] = E[JIR \otimes J_{TX}] = E[J_{TX}] \int_{-\infty}^{\infty} JIR dt = E[J_{TX}] JTF(0) \quad (8)$$

where $E(x)$ is the expected value or mean of x [18]. S_{TX} and S'_{TX} , which are the power spectral density (PSD) of the J_{TX} and J'_{TX} , can be related as the well-known equation:

$$S'_{TX} = |JTF(f)|^2 S_{TX} \quad (9)$$

Then the auto-covariance C'_{TX} of J'_{TX} is

$$C'_{TX}(\tau) = R'_{TX}(\tau) - E^2[J'_{TX}] = \mathcal{F}^{-1}(S'_{TX}) - E^2[J'_{TX}] \quad (10)$$

where R'_{TX} is the auto-correlation of J'_{TX} , while the second equation comes from Wiener-Khinchin theorem. From (8)-(10), if the distribution of J_{TX} is known, we can obtain both the mean and auto-covariance of its response J'_{TX} through the channel. Moreover, if the input process J_{TX} is a Gaussian WSS random process, the output J'_{TX} will also be a Gaussian WSS random process [18]. Thus, the mean and auto-covariance will be sufficient to determine the distribution of J'_{TX} .

It should be noted that while the jitter is amplified as it passes through the channel, the sampling clock can track some amount of this jitter, such that the total degradation on BER can be mitigated. This jitter tracking is constrained by the bandwidth limitation of a clock data recovery (CDR) circuit* [14] (which generates the clock for the receiver in Fig. 4) in an embedded clock architecture, or from the mismatch observed between the data and clock paths in the forwarded clock architecture. To model this effect, we assume a first order low-pass system to track the jitter up to its tracking bandwidth BW_{track} , with only the portion outside this tracking bandwidth is integrated. The transfer functions of the ‘jitter tracking’ and the ‘not tracking’ can be expressed as below:

$$H_{track} = \frac{1}{1 + \frac{j\omega}{BW_{track}}}, \quad H_{not_track} = 1 - H_{track} = \frac{\frac{j\omega}{BW_{track}}}{1 + \frac{j\omega}{BW_{track}}} \quad (11)$$

By doing so, the transmitter jitter is converted to its equivalent jitter distribution at the receiver side.

The random timing jitter uncertainty at the receiver side can be modeled as a Gaussian distribution. Though a Gaussian distribution is boundless, the probability that the random variable exceeds 7.0345σ is only 10^{-12} , where σ is its standard deviation [18]. We include the range between $\pm N_s\sigma$ in the calculation, where N_s is chosen as 8 in order to leave sufficient margin for a BER of 10^{-12} . The time positions of the cursors in the pulse

response $g_F(t)$, shown in Fig. 2, are disturbed by the presence of the jitter. Therefore, the PDFs of the ISI and the main cursor ONE can be modified from (2) and (4) to:

$$ISI_{k,j} = P_0 \delta(x) + P_1 \sum_{\tau=-N_s \sigma}^{N_s \sigma} \left[\delta(x - g_F(t - kT - \tau)) \cdot gs(\tau) \right] \quad (12)$$

$$main_{1,j} = \sum_{\tau=-N_s \sigma}^{N_s \sigma} \left[\delta(x - g_F(t - \tau)) \cdot gs(\tau) \right] \quad (13)$$

where $gs(\tau)$ is the PDF of the jitter. Different PDFs of uncorrelated jitter sources can be convolved together to obtain the total equivalent PDF at the receiver side.

The effects of finite rise/fall time and duty cycle variation are added to this analysis by directly shaping the input symbol pulse according to its rise/fall time and pulse width, and then regenerating the pulse response through the channel.

* Interested readers can refer to [9], [20] for detailed CDR modeling.

D. Sub-block Modeling of Serial Link

As shown in Fig. 4, the sub-blocks of a serial link transceiver includes the channel, FFE, LE and DFE. The channel pulse response can be extracted from the inverse FFT of the S-parameters of the channel [7]. Because the FFE and DFE are discrete-time in nature, they are easily included in the analysis, as the tap coefficients calculated from (1) can be used

directly as the coefficients for the FIR filter of the FFE or DFE. The receiver front-end LE, on the other hand, is the analog component that works at the highest frequency of all the receiver blocks. It is usually implemented as a source-degenerated, linear equalizer [19], as shown in Fig. 6. Its voltage gain can be written as:

$$A_v = G_m R_{out} \approx \frac{g_m}{1 + g_m \left(R_s // \frac{1}{j\omega C} \right)} \left(R_D // \frac{1}{j\omega C_L} \right) = \frac{g_m R_D}{1 + g_m R_s} \frac{1 + j\omega / \omega_z}{(1 + j\omega / \omega_p)(1 + j\omega / \omega_{p,out})} \quad (14)$$

where g_m is transconductance of the input transistor pair, $\omega_z = 1/R_s C$, $\omega_p = (1 + g_m R_s) / R_s C = (1 + g_m R_s) \omega_z$, and output pole $\omega_{p,out} = 1/R_D C_L$. Therefore, R_s and C introduce a zero ω_z before the pole ω_p . If the output pole $\omega_{p,out}$ is designed to be larger than the zero, the gain will be boosted between ω_z and the smaller one of ω_p and $\omega_{p,out}$. By increasing the value of the degenerated resistor R_s , the DC gain will decrease and ω_z will be smaller. However, the location of two poles will not change significantly, resulting in an effective high-pass filtering effect with a constant frequency peak that compensates for some of the channel loss. Finally, the BER distribution plot with equalization can be obtained from the resulting pulse response convolving with the impulse responses of the equalizers.

IV. BEHAVIORAL SIMULATIONS

The above analysis is verified using behavioral simulations in MATLAB. Several FR4 PCB traces with two SMA connectors for different lengths from 10cm to 80cm were measured (Fig. 1). The impulse responses of the channels were derived from the

measured S parameters. Unless otherwise stated, the default settings for the simulations below are 20-Gb/s data rate with 0.5V transmitter amplitude and 20mV tap coefficient resolution through the 40cm PCB trace.

Due to the large channel loss of the 40cm trace, the eye without equalization will be closed. Therefore, the effectiveness of the statistical analysis is verified by traditional transient simulation with 4-tap FFE equalization for both NRZ and duobinary. The two methods exhibit similar horizontal and vertical openings, as shown in Fig. 7 and Fig. 8. Note that for the transient results, 10k bits are simulated in order to trade-off between accuracy and simulation time. The proposed statistical analysis not only provides similar eye diagram with less simulation time but also includes sufficient BER information. This BER eye plot can easily be converted to the conventional bathtub curve for a given decision threshold.

To fairly compare the performance of NRZ without equalization, NRZ with equalization and duobinary equalization, the tap coefficients of the 4-tap FFE are normalized. Each modulation scheme is analyzed by comparing the area of the region where $BER < 10^{-12}$ in the BER eye plot, in unit ps*V. As there are two eye openings for duobinary signaling, only the minimum of the two is counted as the worst case when there are uneven eyes for duobinary. As shown in Fig. 9, the eye is almost closed after 20cm if no equalization is performed. As duobinary equalization relies on a faster decreased channel loss in the frequency domain, it is not as effective as NRZ equalization for small channel losses.

However, for severe loss channels like those longer than 40cm, its eye opens more compared with NRZ equalization.

The effects of finite rise/fall time and duty cycle deviation are shown in Fig. 10 and Fig. 11. Here it is observed that NRZ equalization does not degrade as much as duobinary due to these variations. Interestingly, the eyes improve slightly with small rise/fall time, because the finite transition times smooth the pulse shape and excite less interference. Fig. 12 shows the BER eye openings of NRZ and duobinary signaling with different receiver and transmitter jitter values, where the eye opening of duobinary degrades faster than that of NRZ in the existence of jitter. Thus, while the eye opening of jitter-free duobinary is larger than that of NRZ, as the jitter value increases, duobinary performs worse than NRZ.

Fig. 13 shows that a larger jitter tracking bandwidth will help to improve the BER performance. The eye openings for different FFE and DFE taps are plotted in Fig. 14. As the number of taps increases, residual ISI becomes less severe, opening the eyes of both NRZ and duobinary. However, as duobinary requires 3-level signaling, its eye is more likely to be limited by its voltage headroom than by residual ISI. Therefore, when a large number of equalizing taps are used, the duobinary eye with limited voltage headroom may perform unfavorably when compared with NRZ.

V. CONCLUSION

A statistical method to analyze serial link systems for NRZ and duobinary signaling is presented, incorporating non-ideal effects such as transmitter jitter and receiver jitter, jitter tracking bandwidth, finite rise/fall time and duty cycle deviation. Using this analysis tool, a comparison of the performance between NRZ and duobinary at 20-Gb/s is then performed. While duobinary achieves less channel loss due to the reduced Nyquist bandwidth, in general, it suffers more than NRZ from non-idealities arising from the imperfect clock source. Only for long channels with significant attenuation does 20-Gb/s multi-level, duobinary signaling have a BER advantage over NRZ, given the expected amount of clock uncertainty. The proposed statistical analysis can therefore give early insight for quick and accurate system design tradeoffs for multi-Gb/s interconnections.

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Fig. 13. Eye opening area for $BER < 10^{-12}$ with different jitter tracking bandwidth for 40cm trace with both 1ps RMS TX and RX jitter.

Fig. 14. Eye opening area for $BER < 10^{-12}$ with different FFE and DFE taps for 40cm trace (for FFE, with 1 precursor tap and varying no. of postcursor taps).

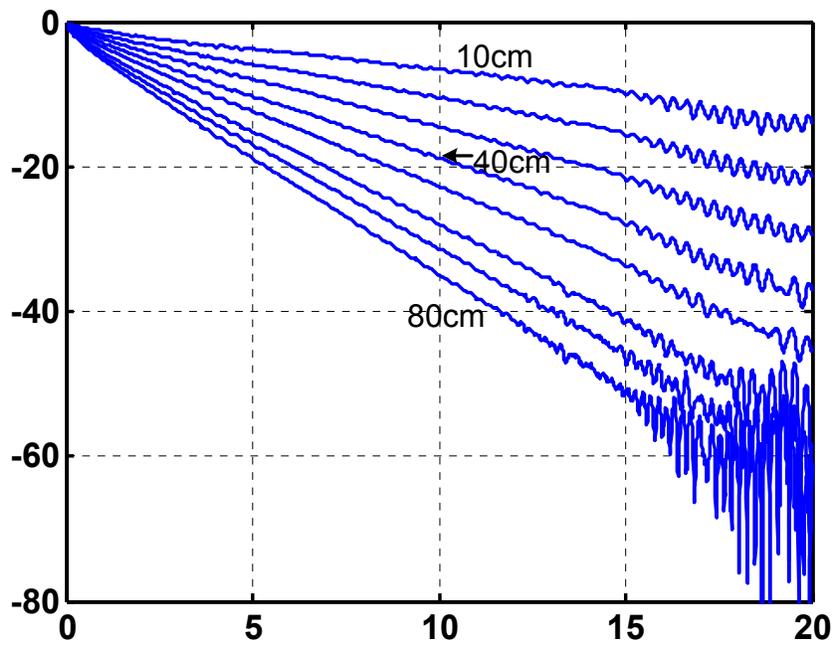


Fig. 1. Measured channel loss of 10cm to 80cm PCB traces (from top to bottom), showing -6,6dB, -18.9dB,-35dB loss at 10GHz for 10cm, 40cm and 80cm PCB traces respectively.

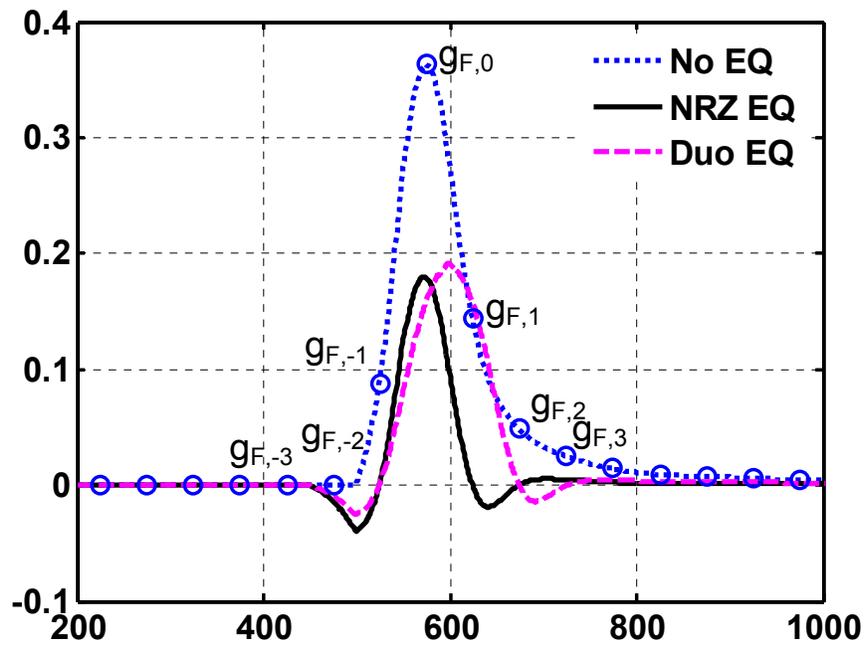


Fig. 2. Pulse response to a 50ps (20-Gb/s) pulse before equalization, after NRZ equalization, and duobinary equalization of 40cm PCB trace.

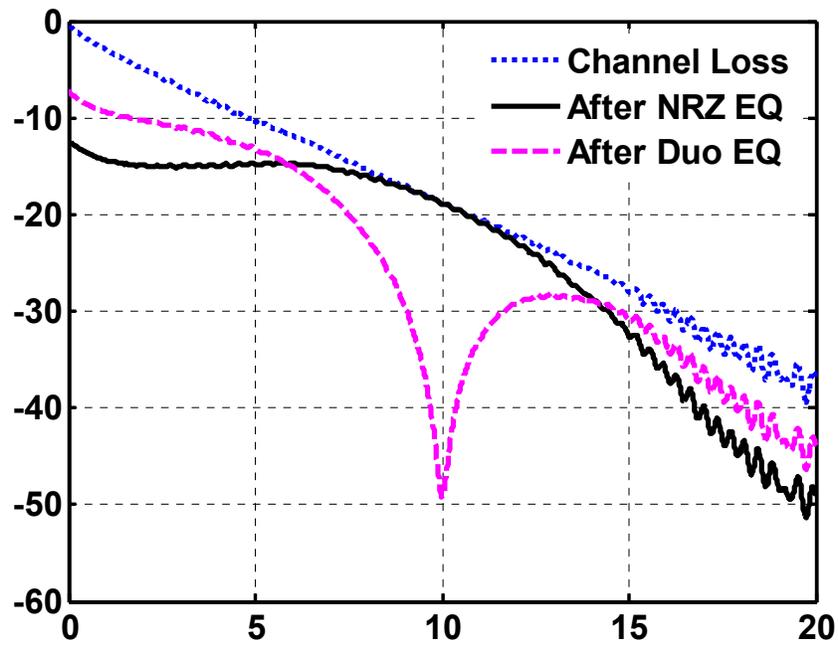


Fig. 3. Frequency response before equalization, after NRZ equalization and duobinary equalization of a 40cm PCB trace.

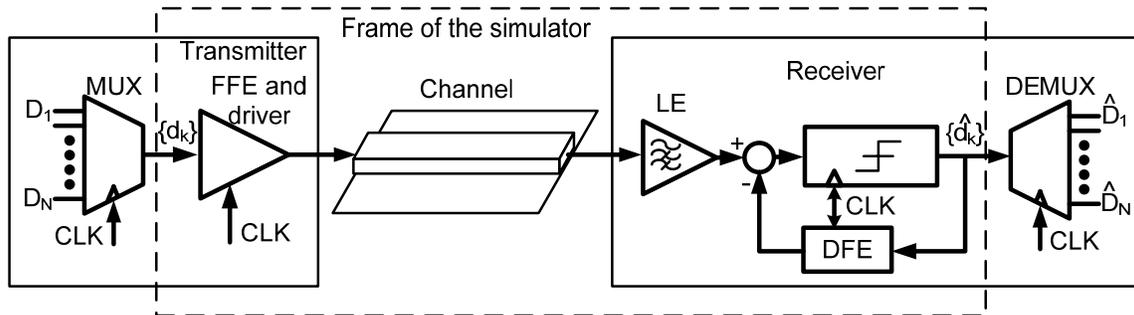
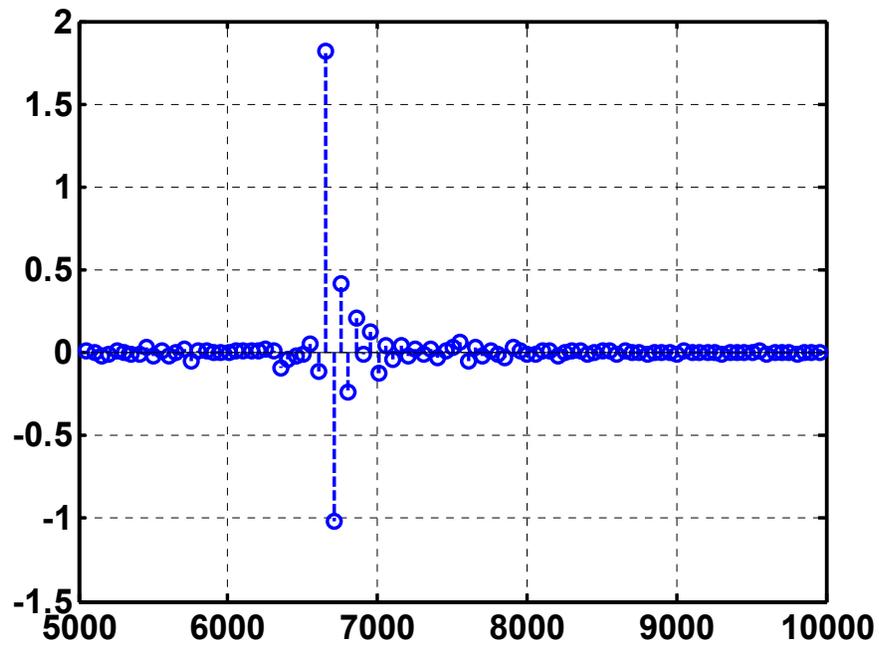
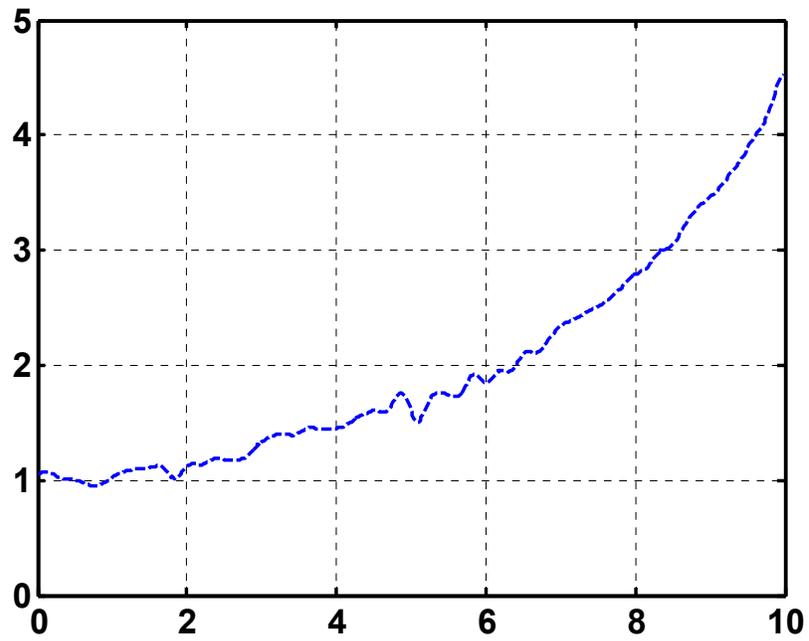


Fig. 4. Simplified architecture of a typical serial link transceiver.



(a)



(b)

Fig. 5 (a) Jitter impulse response and (b) jitter transfer function of a 40cm PCB trace at 20-Gb/s.

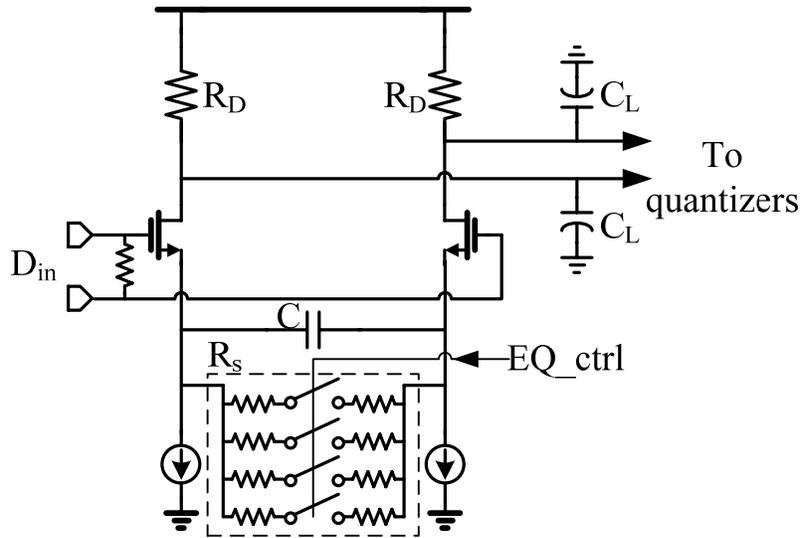
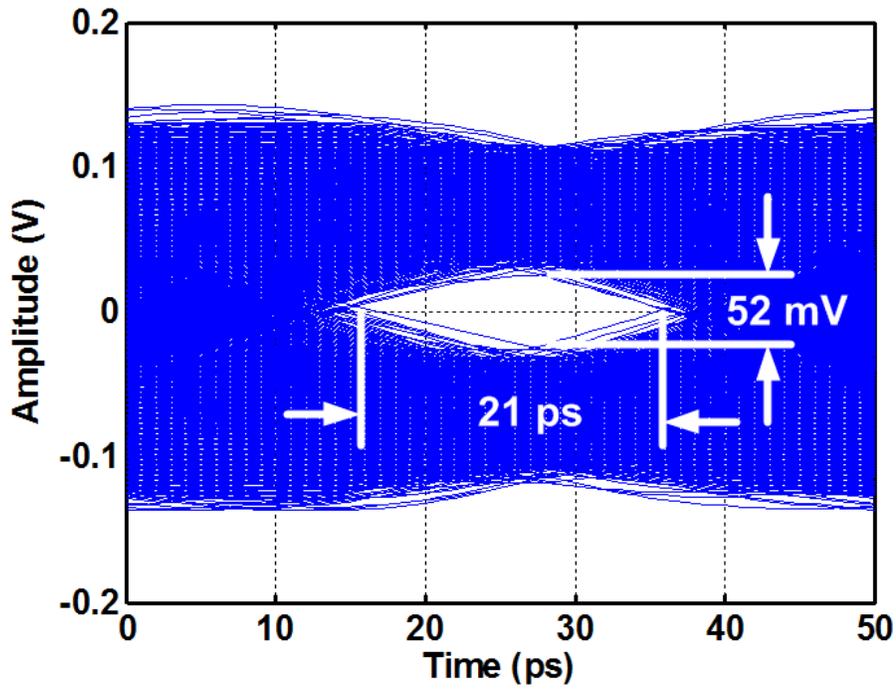
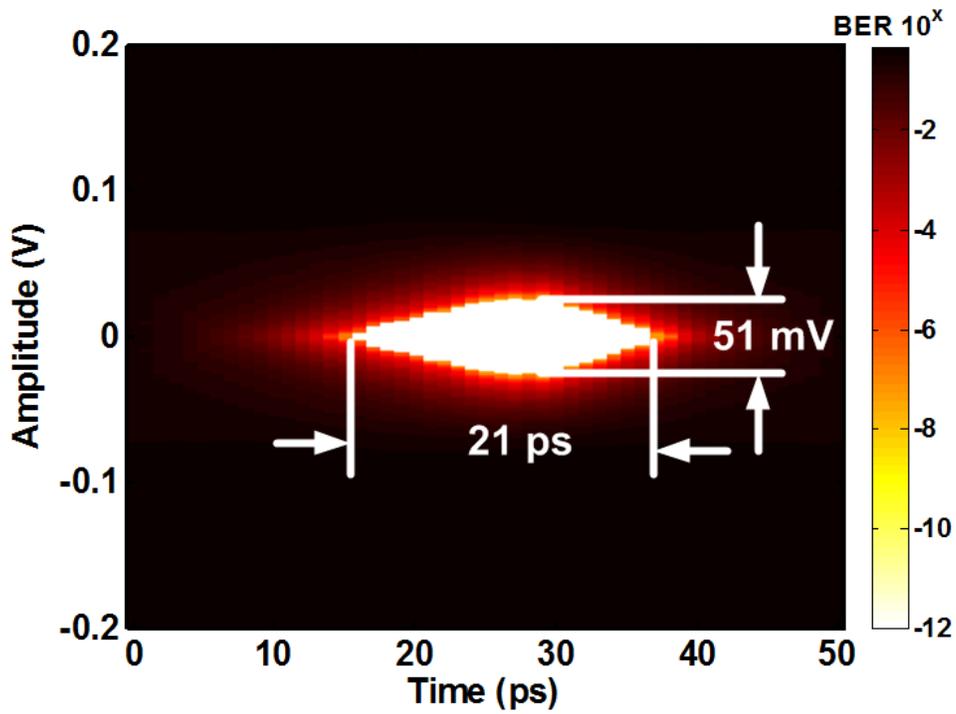


Fig. 6 Schematic of receiver linear equalizer.

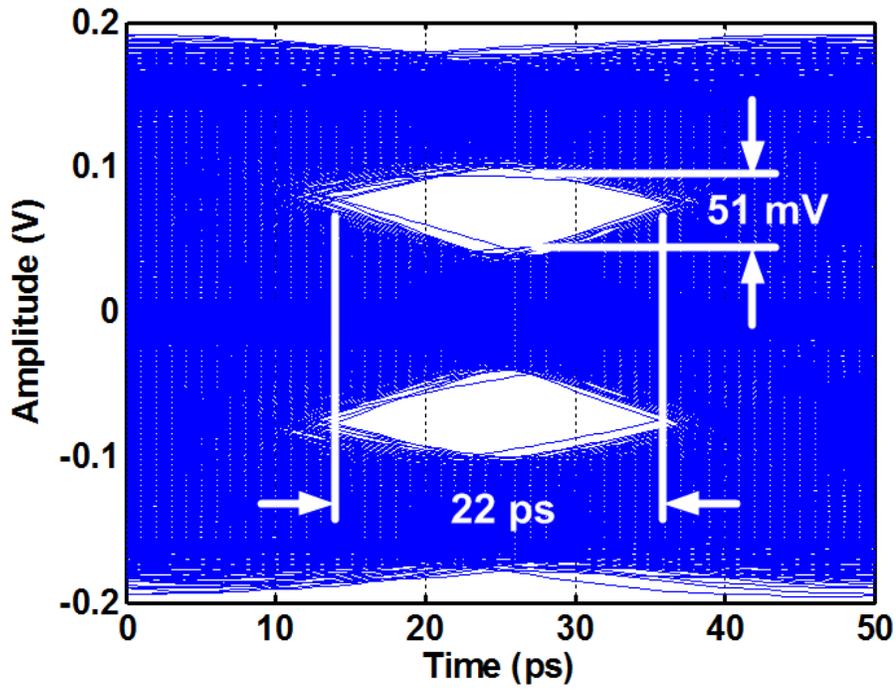


(a)

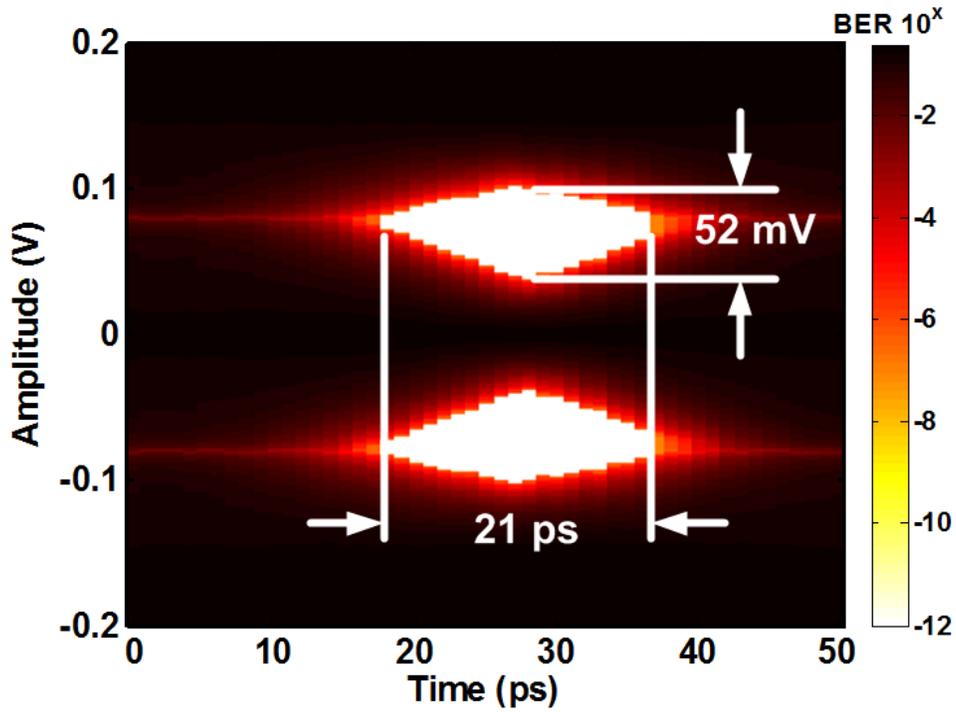


(b)

Fig. 7. Eye diagram of 40cm trace after NRZ equalization, (a) transient simulation of 10k random bits and (b) statistical analysis.



(a)



(b)

Fig. 8. Eye diagram of 40cm trace after duobinary equalization, (a) transient simulation of 10k random bits and (b) statistical analysis.

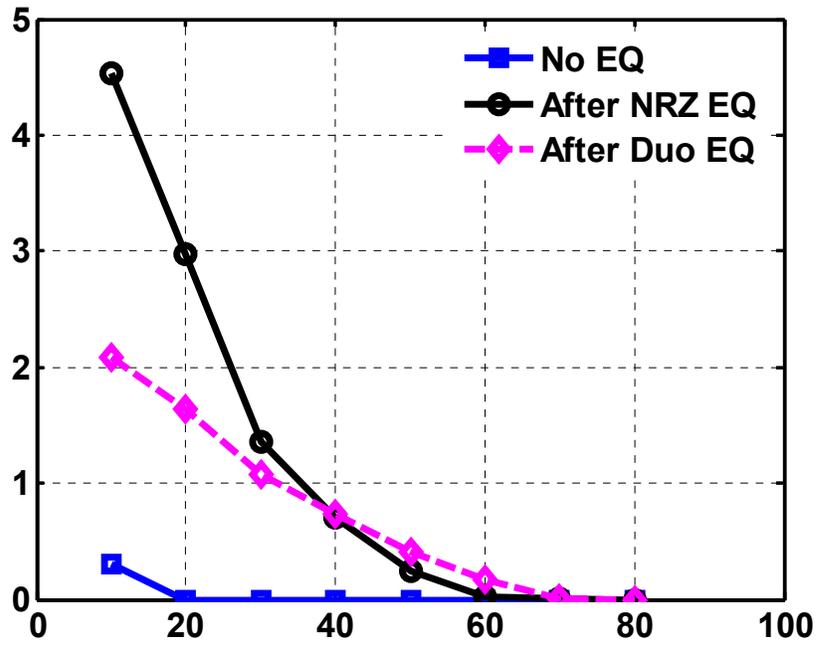


Fig. 9. Eye opening area for $BER < 10^{-12}$ with different length of traces.

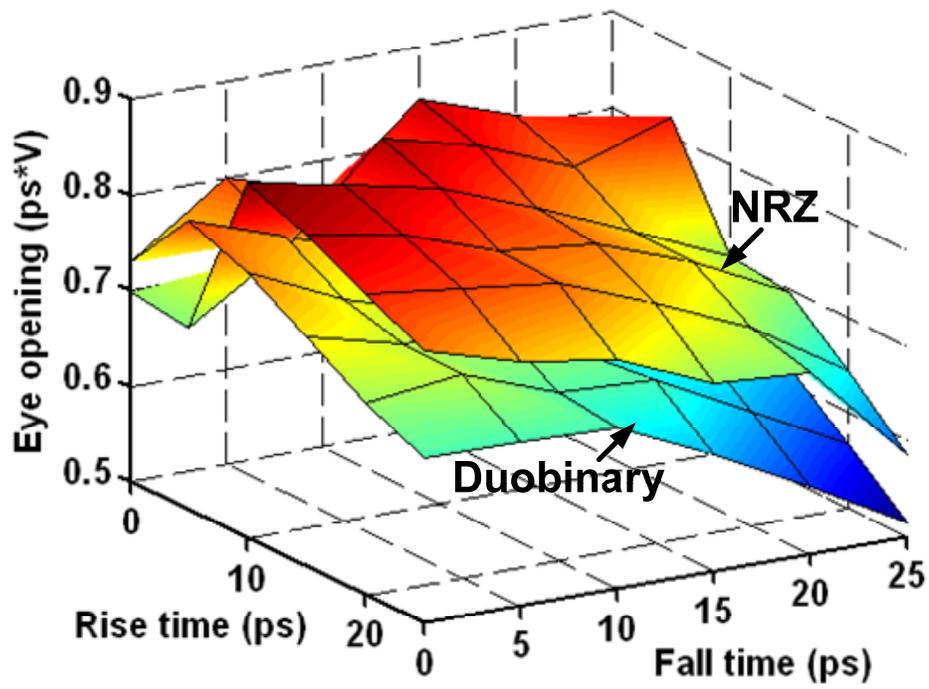


Fig. 10. Eye opening area for $BER < 10^{-12}$ with different rising and falling times for 40cm trace.

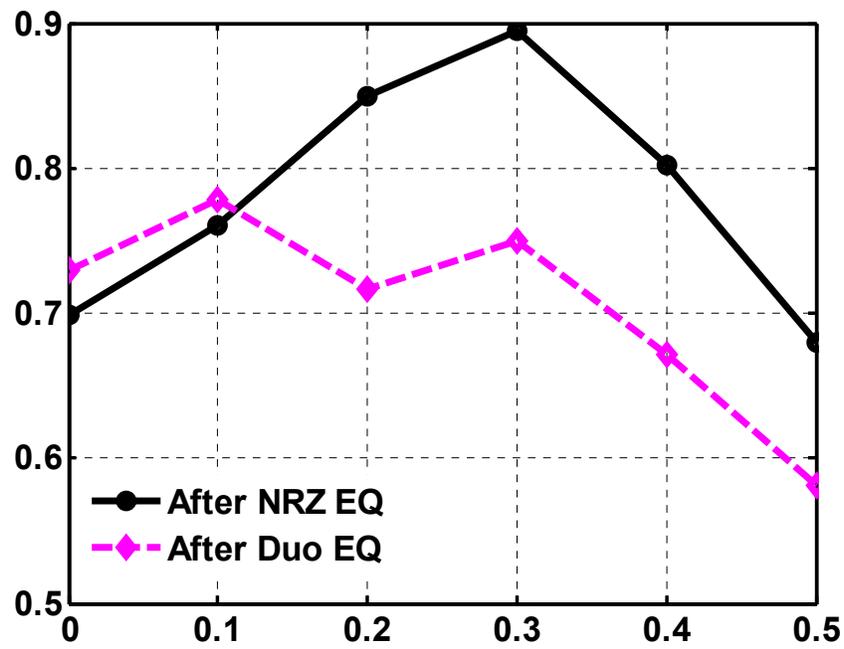


Fig. 11. Eye opening area for $BER < 10^{-12}$ with different duty cycle deviations for 40cm trace.

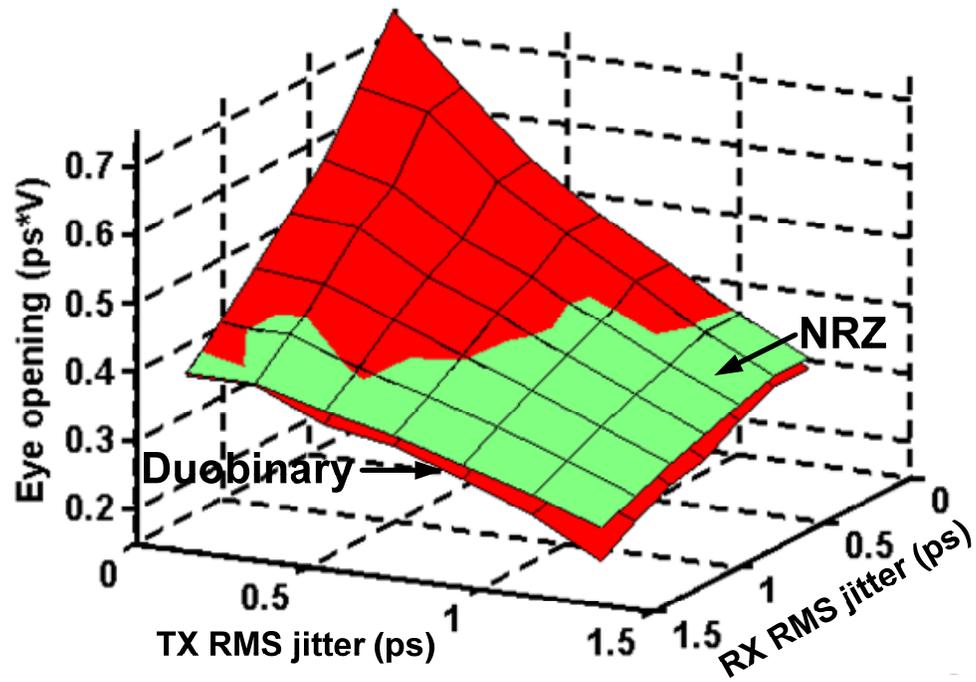


Fig. 12. Eye opening area for $BER < 10^{-12}$ with different receiver and transmitter RMS jitter for 40cm trace.

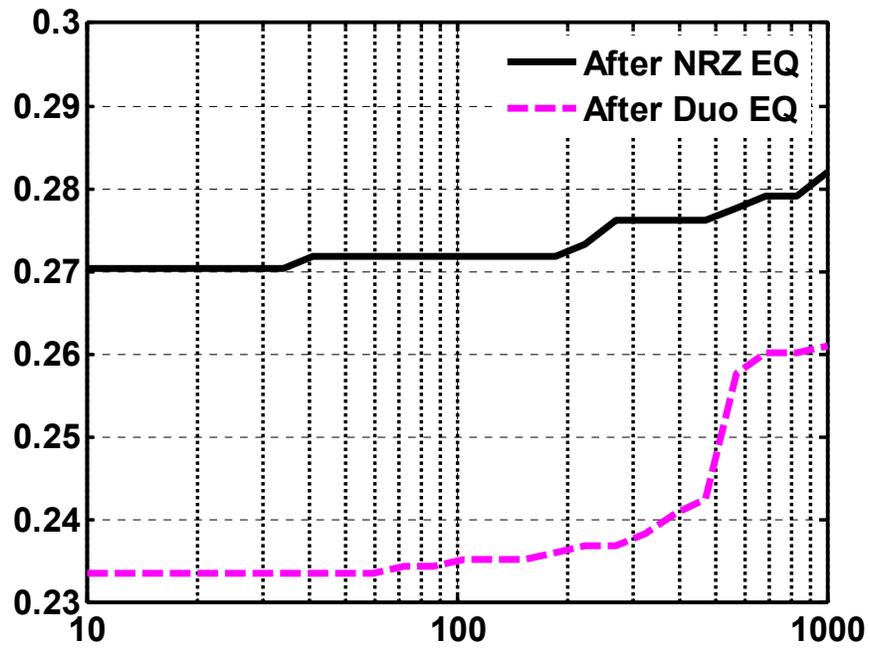


Fig. 13. Eye opening area for $BER < 10^{-12}$ with different jitter tracking bandwidth for 40cm trace with both 1ps RMS TX and RX jitter.

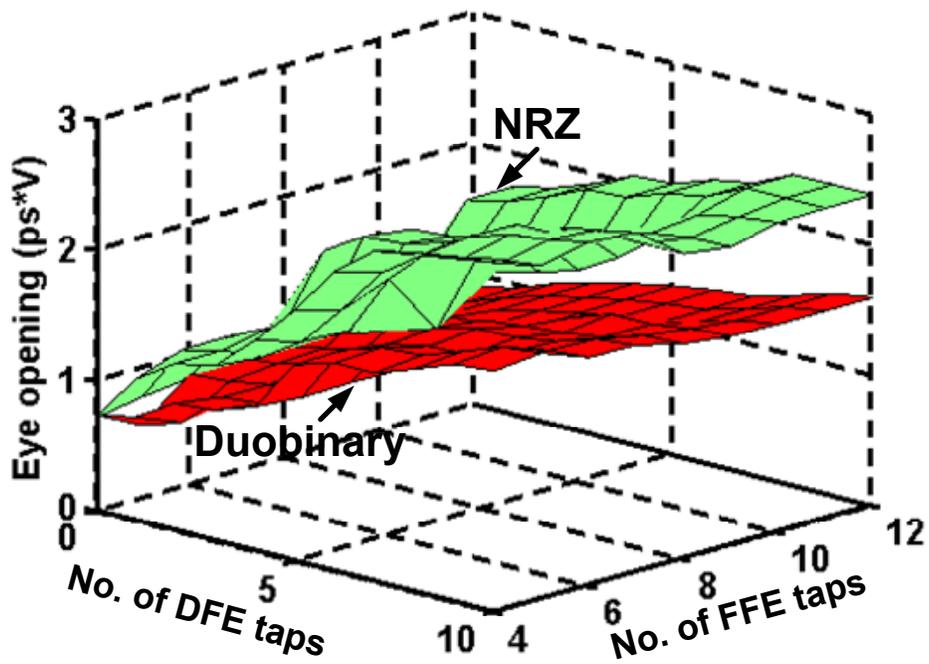


Fig. 14. Eye opening area for $BER < 10^{-12}$ with different FFE and DFE taps for 40cm trace (for FFE, with 1 precursor tap and varying no. of postcursor taps).