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This thesis describes the analysis and comparison of Folded Source-Coupled Logic (FSCL) with standard static CMOS, cascode voltage-switch logic and differential split-level logic gates. The advantages of FSCL are low switching noise and high operating speed. The effect of voltage and device scaling on these topologies is evaluated in terms of average delay, power dissipation at maximum frequency, power-delay-product and current spike noise. Several two-summand adders are designed and simulated using MOSIS 1-μm CMOS process parameters and evaluations are performed in terms of area, delay, noise and power dissipation.

Comparison and Analysis of Current-Mode Logic Circuits with Differential and Static CMOS

by

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THESIS

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COMPARISON AND ANALYSIS OF CURRENT-MODE LOGIC CIRCUITS WITH DIFFERENTIAL AND STATIC CMOS

Chapter 1. Introduction

The demand for higher levels of analog and digital integration on the same IC has led to the development of mixed-mode VLSI systems. Mixed-mode integrated circuits achieve higher performance, are more compact and are economical than separate analog and digital integrated circuits [1]. However, due to the coupling of noise between subsections of the IC, the performance of the system can be degraded.

Standard digital CMOS circuits generate large overlap current spikes during switching transitions. Fig. 1.1 shows the current spike generated during the switching transition of a static inverter. These noise spikes can propagate to the analog subsection via supply lines and the substrate, degrading the accuracy and dynamic range of the analog circuitry. The propagation of digital switching noise to the analog subsection can be classified into two mechanisms [2-3]. The first is the induced noise caused by the coupling from one signal node to the adjacent nodes. The other is power bus noise due to the current spikes propagating through the resistance and inductance of the chip's power bus, bonding wires and package interconnects.

Several techniques have been proposed to reduce the digital noise [4]. These include guardbanding to increase the isolation between the analog and digital circuitry, use of separate power and ground lines for the analog and digital subsystems and filtering the power busses using on-chip active filters [5]. However, these techniques have the disadvantage of increased chip area (guardbanding) or higher system cost. Also, as the

speed of digital circuits increases, the magnitude of the noise increases and the standard noise reduction techniques such as guardbanding become less effective.

Another approach to minimizing noise problems is to minimize the generation of noise. To that end, low-noise current-mode Folded Source-Coupled Logic (FSCL) has been recently developed [6]. These circuits have low switching noise, small propagation delays and low energy losses in stray capacitances, thereby leading to higher performance and ease of implementation in mixed-mode systems.

The objective of this thesis is to analyze FSCL gates and compare them with some common differential topologies. Chapter 2 presents a review of FSCL gates. In Chapter 3, a theoretical analysis of the noise margin and switching delay of the FSCL inverter is shown. Chapter 4 presents the comparison of FSCL inverters with standard CMOS, CVSL and DSLL inverters. This chapter also presents the comparison of carry ripple, carry skip and carry look-ahead full adders in each one of these topologies. Finally, Chapter 5 summarizes the thesis and presents some possibilities for future research.

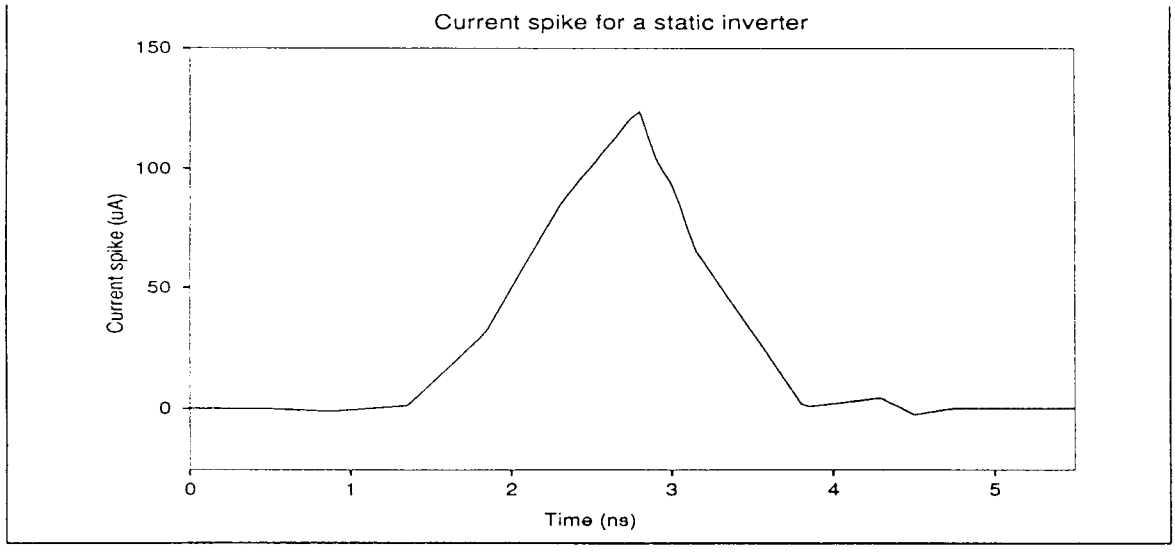

Fig. 1.1 Current spike for a static inverter

Chapter 2. Folded Source-Coupled Logic, CVSL, DSLL

CMOS Folded Source-Coupled Logic (FSCL) has been recently developed as a low-noise differential topology for use in mixed-mode circuits. FSCL is a current-mode logic where the output logic levels are obtained by steering a constant current through the different branches. This results in a constant current being drawn from the power supply for each gate with very small current spikes. The current spikes can be further reduced by using cascode current mirrors for the current sources.

2.1 Operation of the FSCL Inverter

Fig. 2.1 shows the FSCL inverter with I_1 and I_2 being constant current sources commonly generated by using current mirrors. The transistors M_1, M_2 are the input differential pair transistors and M_3, M_4 are the diode-connected output load transistors. The FSCL inverter operates as follows. When **A** is high, $\overline{\mathbf{A}}$ is low, the transistor M_1 is on and M_2 is off. Therefore current I_1 flows through M_1 and produces a current $(I_2 - I_1)$ through M_3 and I_2 flows through M_4. The output loads produce a voltage proportional to the current flows, hence, the output node $\overline{\mathbf{Q}}$ is low and **Q** is high.

2.1.1 Output Voltage Swing

When transistor M_1 is on and a current $(I_2 - I_1)$ is flowing through transistor M_3, the output voltage low, V_{OL}, at node $\overline{\mathbf{Q}}$ is obtained.

$$V_{OL} = V_T + \sqrt{\frac{2(I_2 - I_1)}{K_N (W/L)_{M3}}} \tag{2.1}$$

where $K_N = \mu C_{ox}$. Similarly, when M_1 is off, current I_2 is flowing through M_3, and the output voltage high, V_{OH}, is obtained at node $\overline{\mathbf{Q}}$.

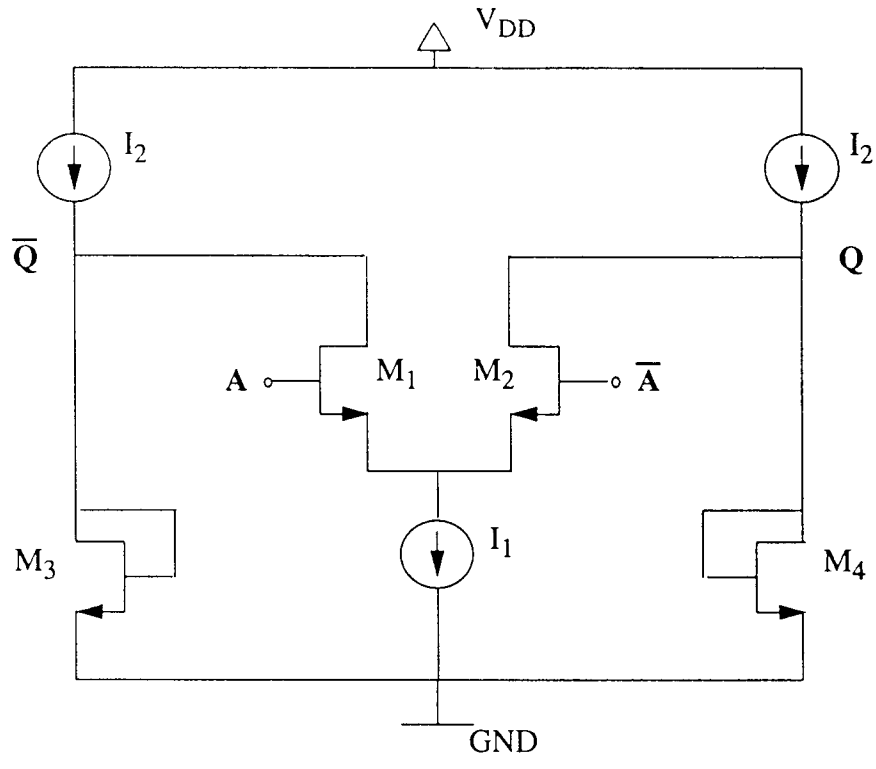

Fig. 2.1 Basic FSCL inverter

$$V_{OH} = V_T + \sqrt{\frac{2I_2}{K_N(W/L)_{M3}}} \tag{2.1}$$

Thus, the output voltage swing, ΔV_O, at the nodes $\overline{\mathbf{Q}}$ and $\mathbf{Q}$ is given by:

$$\Delta V_O = V_{OH} - V_{OL} = \sqrt{\frac{2I_2}{K_N(W/L)_{M3}}} - \sqrt{\frac{2(I_2 - I_1)}{K_N(W/L)_{M3}}} \tag{2.2}$$

Assuming $I_2 = \alpha I_1$ where $\alpha > 1$, we can rewrite the above equation as follows:

$$\Delta V_O = \sqrt{\frac{2I_2}{K_N(W/L)_{M3}}} \cdot \left(1 - \sqrt{1 - \frac{1}{\alpha}}\right) \tag{2.3}$$

The power dissipation of the FSCL inverter is directly proportional to I_2. Hence by using minimum device sizes for $(W/L)_{M3}$ and $\alpha \equiv 1$, the required output voltage

swing is obtained by varying I_2.

2.1.2 Voltage Gain

The voltage gain at the switching transition determines the noise margins of the FSCL inverter. A high gain implies that the input differential voltage required to obtain the output voltage swing is small and thus the noise margins are large. Fig. 2.3 shows the transfer characteristic obtained for a 2-μm process FSCL inverter with $\alpha = 1.2$, $\beta = 3$, $I_1 = 79\ \mu A$, $(W/L)_{M3} = (4/2)$ and $K_N = 62.5\ \mu A/V^2$. The output voltages are $V_{OL} = 1.2$ V and $V_{OH} = 1.88$ V.

The maximum input voltage required to turn M_1 off is given by

$$V_{IL} = V_{DSI1} + V_T \tag{2.4}$$

where V_{DSI1} is the drain-source voltage of the current source transistor M_{I1} (Fig. 2.2) and V_T is the threshold voltage for transistor M_1. Also, the minimum input voltage

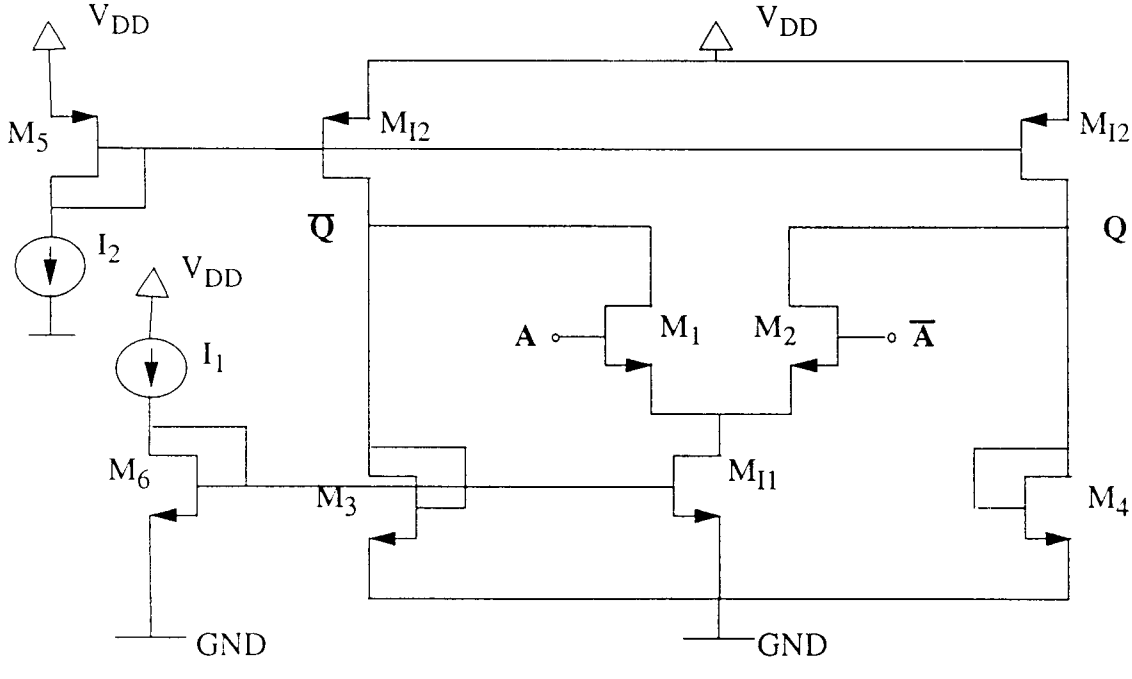

Fig. 2.2 FSCL inverter with current mirrors

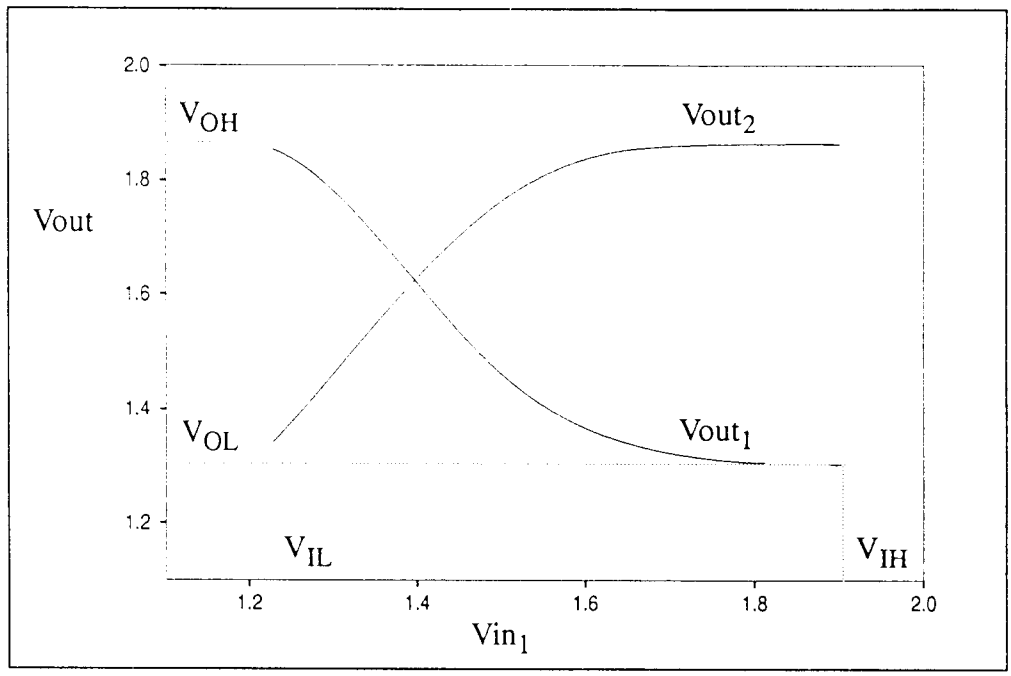

Fig. 2.3 Transfer characteristics of a FSCL inverter

required for M_1 to conduct current I_1 is given by:

$$V_{IH} = V_{DSI1} + V_T + \sqrt{\frac{2I_1}{K_N (W/L)_{M1}}} \tag{2.1}$$

Let $(W/L)_{M1} = \beta(W/L)_{M3}$ where $\beta > 1$ is used to obtain a high gain. The first-order approximation for the voltage gain, A_V, is given by:

$$A_V = \frac{V_{OH} - V_{OL}}{V_{IH} - V_{IL}} = \frac{\sqrt{\frac{2I_2}{K_N (W/L)_{M3}}} - \sqrt{\frac{2(I_2 - I_1)}{K_N (W/L)_{M3}}}}{\left(V_{DSI1} + V_T + \sqrt{\frac{2I_1}{K_N \beta (W/L)_{M3}}}\right) - (V_{DSI1} + V_T)}$$

$$= \sqrt{\beta} \cdot (\sqrt{\alpha} - \sqrt{\alpha - 1}) \tag{2.2}$$

For a typical value of $\alpha = 1.2$, $\beta \cong 3$ is required to obtain a gain $A_V = 1.12$.

2.2 Complex FSCL Gates

Higher-level FSCL gates are developed by replacing the transistors M_1 and M_2 of the FSCL inverter (Fig. 2.1) with stacked differential NMOS transistors. This technique is known as "series gating" and allows the generation of complex functions without any more power dissipation than that of the FSCL inverter [7].

A general complex FSCL gate is shown in Fig. 2.4. The FSCL NAND/AND, FSCL NOR/OR and FSCL latch are shown in Fig. 2.5, Fig. 2.6 and Fig. 2.7 respectively.

2.3 CVSL

Cascode voltage switch logic is a differential CMOS topology which is generally used to restore healthy bipolarity CMOS signals from deteriorated bi-polarity signals. The circuit consists of a pair of cross-coupled PMOS transistors with conditional NMOS

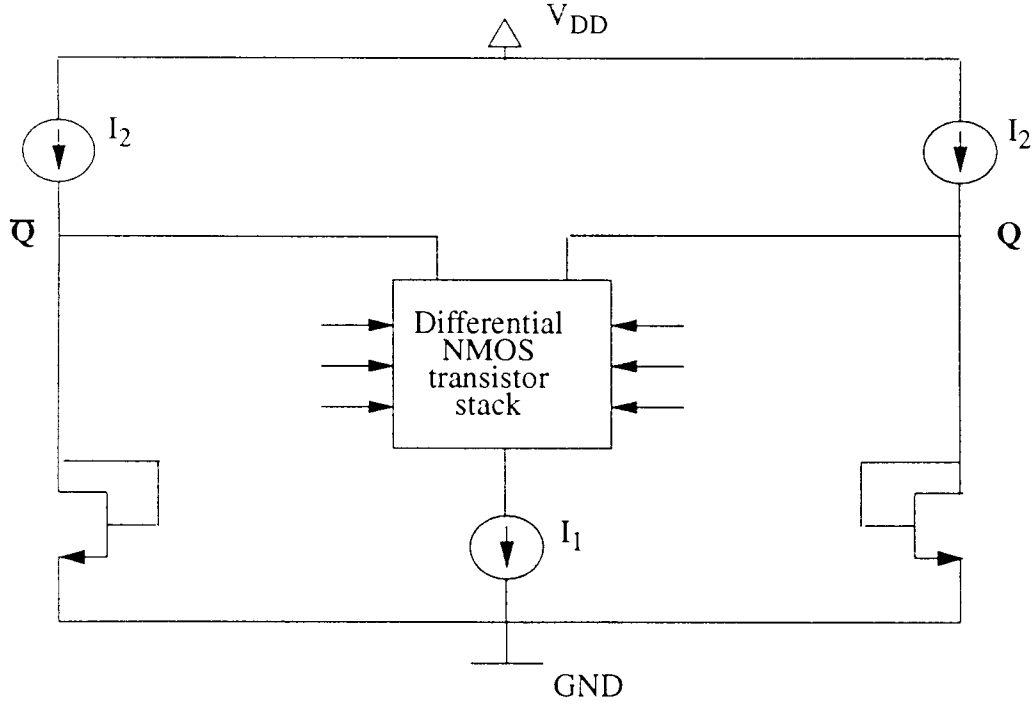

Fig. 2.4 Schematic of a complex FSCL gate

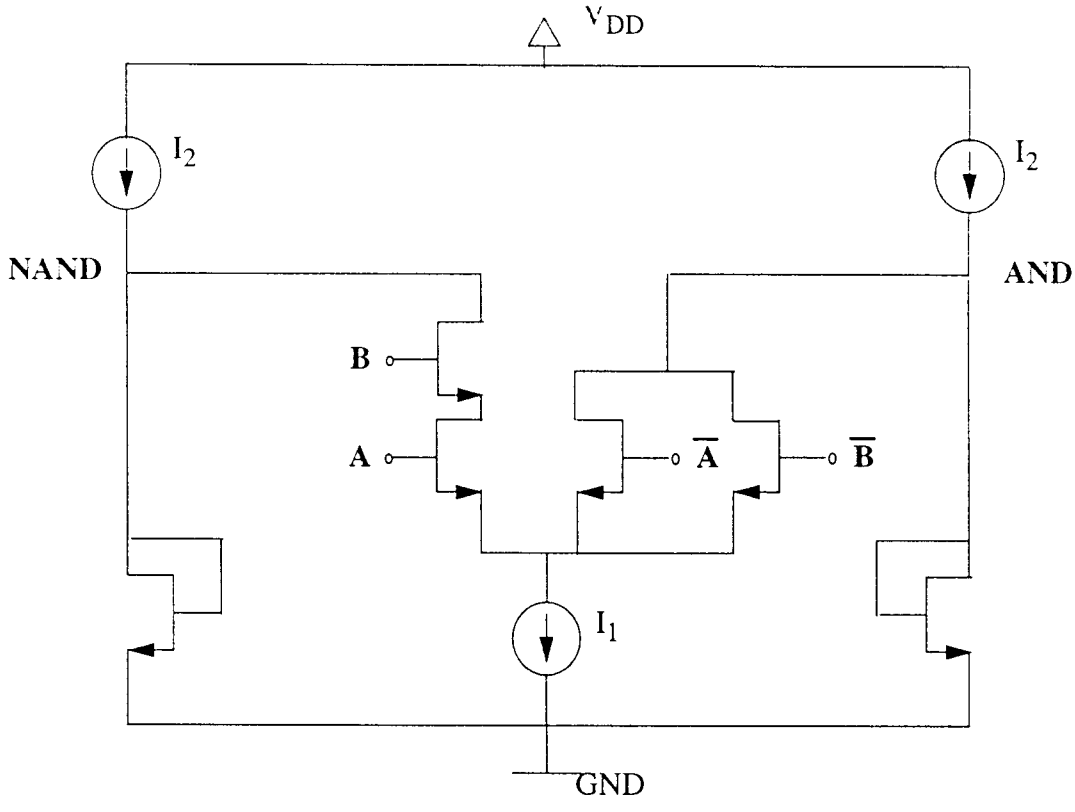

Fig. 2.5 Schematic of a FSCL NAND/AND gate

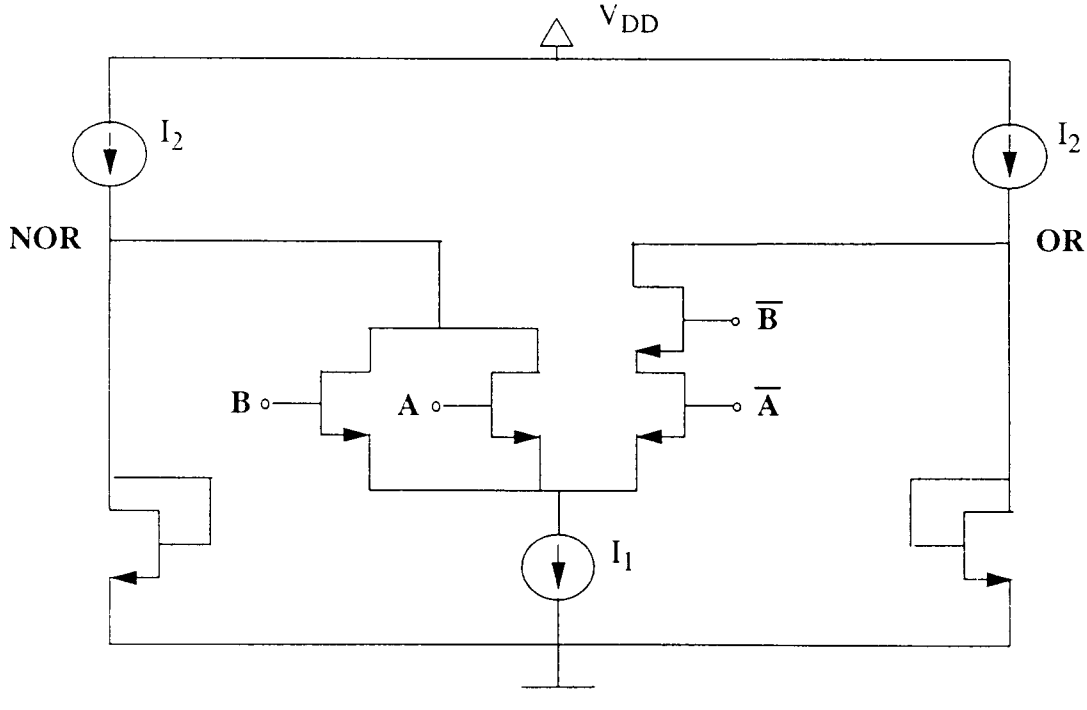

Fig. 2.6 Schematic of a FSCL NOR/OR gate

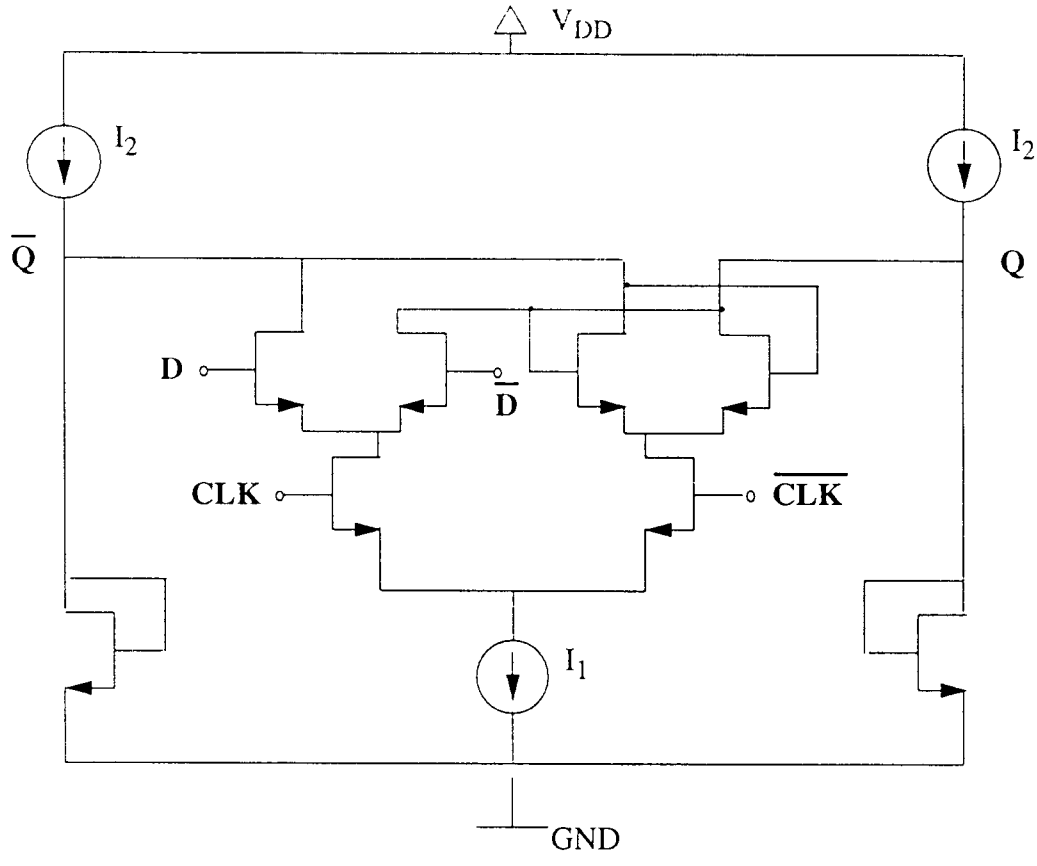

Fig. 2.7 Schematic of a FSCL latch

pull-down paths. CVSL circuits require two more FETs than conventional static CMOS gates and require both polarities of each input. Fig. 2.8 shows a CVSL inverter where the pull-down paths consist of one NMOS each.

2.4 DSLL

Differential split-level logic is similar to CVSL, but the operating principles are different. Fig. 2.9 shows the schematic of a DSLL inverter. The reference voltage, V_{REF}, is set at $(V_{DD}/2) + V_{TN}$, where V_{TN} is the threshold voltage of the NMOS, including the back-bias effect. When transistors M_1 is on and M_2 is off, the node $\overline{\mathbf{Q}}$ is pulled down to 0 V and node **Q** is pulled up to $V_{DD}/2$. Thus the voltage swing at these nodes is reduced

to half the power supply voltage.

DSLL gates require two more transistors than corresponding CVSL gates and four more transistors than conventional static CMOS gates.

2.5 Comparison of Different Topologies

The advantages offered by FSCL over conventional static CMOS can be summarized as follows [7]:

1) Low power bus noise (at least 100 times smaller that static CMOS logic).

2) Reduced output voltage swing resulting in reduced dynamic power dissipation.

3) Small delays leading to high frequencies of operation.

4) Higher noise immunity due to differential input topology.

5) Reduced area for complex digital blocks as compared to static CMOS.

6) Complementary outputs.

The disadvantages of FSCL are as follows:

1) Static power dissipation due to current-mode operation.

2) Increased area for simple digital blocks as compared to static CMOS.

The device counts for a few basic and complex gates in FSCL, static CMOS,

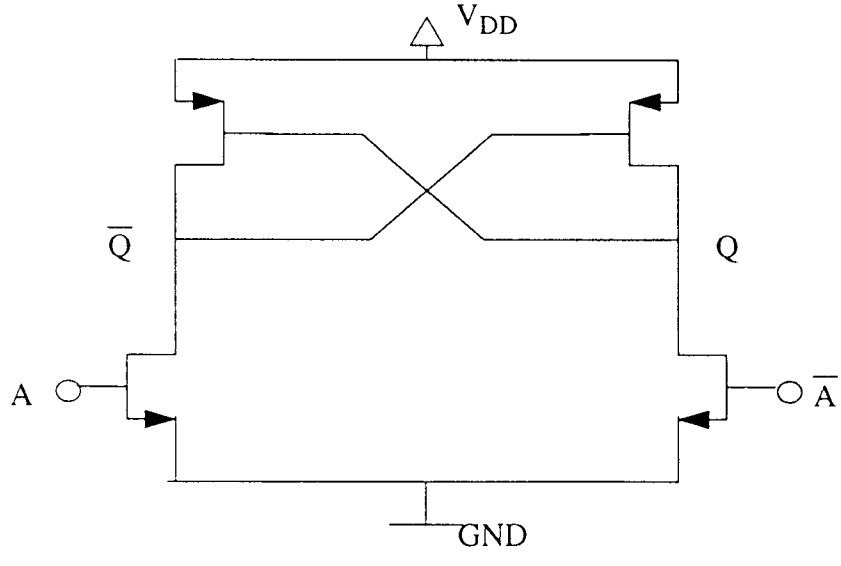

Fig. 2.8 Schematic of a CVSL inverter

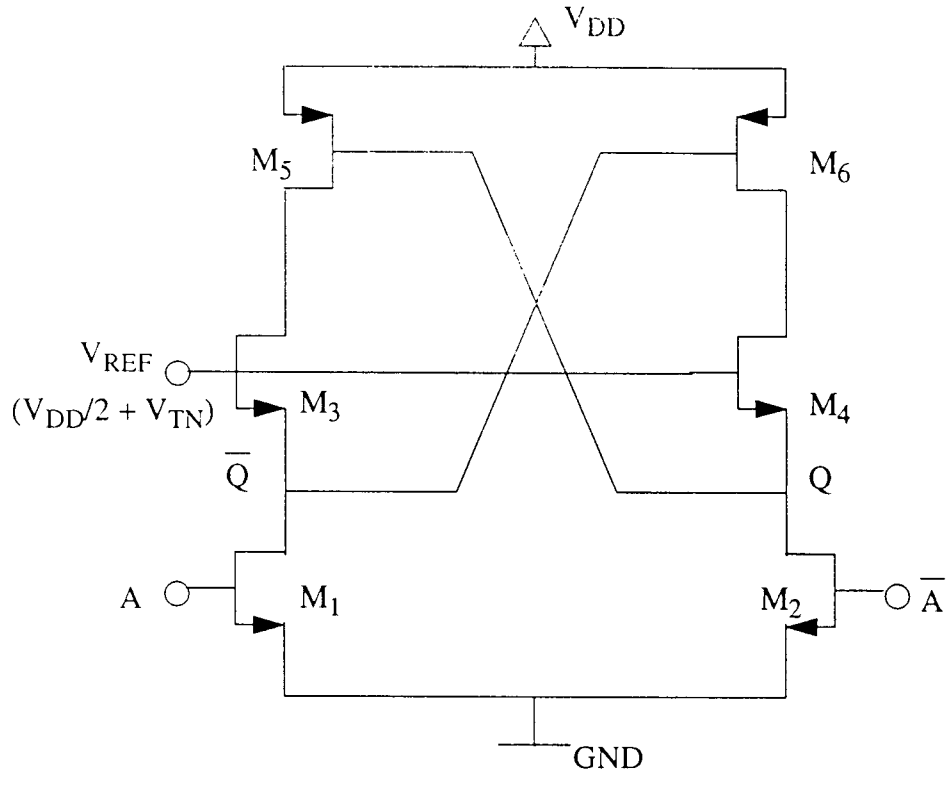

Fig. 2.9 Schematic of a DSLL inverter

CVSL and DSLL is shown in Table 2.1

.

Table 2.1: Gate device count: PMOS/NMOS

	FSCL	Static CMOS	CVSL	DSLL
Inverter	2 / 5	1 / 1	2 / 2	2 / 4
$\overline{A \cdot B}$	2 / 7	2 / 2	2 / 4	2 / 6
$A \cdot B$	2 / 7	3 / 3	2 / 4	2 / 6
$\overline{A \cdot B \cdot C}$	2 / 9	3 / 3	2 / 6	2 / 8
Full Adder	4 / 24	15 / 15	4 / 20	4 / 24

For the primitive inverter and nand/and gates, the number of transistors required is more for the differential circuits than that required for the conventional static CMOS equivalents. However, for complex functions like full addition, the number of transistors required is less in differential circuits than that for the static CMOS full adder.

Chapter 3. Analysis of the FSCL Inverter

In these sections, theoretical analysis of the FSCL inverter for the noise margins and the switching characteristic is given.

3.1 Noise Margin

The high and low noise margins of a FSCL inverter are dependent on the values for α, β and the current I_1.

Referring to Fig. 2.1, the noise margins are determined at the input voltages for which transistor M_1 is about to turn off at V_{IL} and when its on and conducting current I_1 at V_{IH} and the output voltages at node **Q** are V_{OH} and V_{OL} respectively. Using equations (2.1), (2.2), (2.5) and (2.6), the high noise margin is:

$$NM_H = V_{OH} - V_{IH} = \left(V_T + \sqrt{\frac{2I_2}{K'_N (W/L)_{M3}}}\right) - \left(V_{DSI1} + V_T + \sqrt{\frac{2I_1}{K'_N (W/L)_{M1}}}\right)$$

$$= \sqrt{\frac{\alpha I_1}{K_N}} - \sqrt{\frac{I_1}{\beta K_N}} - V_{DSI1} \qquad (3.1)$$

where $I_2 = \alpha I_1$, $(W/L)_{M1} = \beta(W/L)_{M3}$, $K'_N = \mu C_{ox}$ and $K_N = K'_N.(W/L)_{M3}$. Similarly, the low noise margin is calculated as:

$$NM_L = V_{IL} - V_{OL} = (V_{DSI1} + V_T) - \left(V_T + \sqrt{\frac{2(I_2 - I_1)}{K_N (W/L)_{M3}}}\right)$$

$$= V_{DSI1} - \sqrt{\frac{\alpha I_1 - I_1}{K_N}} \qquad (3.2)$$

Proper operation requires that both NM_H and NM_L be greater than zero. Hence,

$$NM_H > 0 \Rightarrow \sqrt{\frac{\alpha I_1}{K_N}} - \sqrt{\frac{I_1}{\beta K_N}} - V_{DSI1} > 0$$

or,
$$\sqrt{\alpha} - \frac{1}{\sqrt{\beta}} > \sqrt{\frac{K_N}{I_1}} \cdot V_{DSI1} \tag{3.3}$$

$$NM_L > 0 \Rightarrow V_{DSI1} - \sqrt{\frac{\alpha I_1 - I_1}{K_N}} > 0$$

or,
$$\sqrt{\alpha - 1} < \sqrt{\frac{K_N}{I_1}} \cdot V_{DSI1} \tag{3.4}$$

By combining equations (3.3) and (3.4), the following constraints must be satisfied:

$$\sqrt{\alpha - 1} < \sqrt{\frac{K_N}{I_1}} \cdot V_{DSI1} < \sqrt{\alpha} - \frac{1}{\sqrt{\beta}} \tag{3.5}$$

With $\alpha \cong 1$ to maximize the output voltage swing and given the value of ΔV_O, which then determines the currents I_1 and I_2, the device ratio β can be determined by the above relation.

3.1.1 Noise Margin for sub-micron devices

As technology scales down and gate lengths approach below 1μm, the effect of velocity saturation becomes significant and I_{DS} is a linear function of V_{GS}:

$$I_{DS} = g_m (V_{GS} - V_T)$$

The relations for the input and output high and low voltages are given by,

$$V_{OH} = V_T + \frac{\alpha I_1}{g_m} \qquad V_{OL} = V_T + \frac{(\alpha - 1) I_1}{g_m}$$

$$V_{IH} = V_{DSI1} + V_T + \frac{I_1}{\beta g_m} \qquad V_{IL} = V_{DSI1} + V_T \tag{3.6}$$

The output voltage swing is, $\Delta V_O = V_{OH} - V_{OL} = \frac{I_1}{g_m}$ (3.7)

The noise margins are given by,

$$NM_H = V_{OH} - V_{IH} = \frac{\alpha I_1}{g_m} - \frac{I_1}{\beta g_m} - V_{DSI1}$$

$$NM_L = V_{IL} - V_{OL} = V_{DSI1} - \frac{(\alpha - 1) I_1}{g_m} \tag{3.8}$$

As before, we combine the relations for $NM_H > 0$ and $NM_L > 0$ to get the following inequality for the sub-micron linear case as:

$$\alpha - 1 < \frac{g_m}{I_1} \cdot V_{DSI1} < \alpha - \frac{1}{\beta} \tag{3.9}$$

Equation (3.5) is used for 2μm device lengths and equation (3.9) is used for 1μm device lengths. By knowing ΔV_O and α, the value of β for a given noise margin can be calculated.

Using MOSIS 1μm process parameters with $\alpha = 1.1$, $\beta = 3$ and $\Delta V_O = 0.5$ V, the noise margin as a percentage of the output voltage swing is shown in Table 3.1 for each topology. In this table three inverter sizes are used: minimum $(W/L)_{M3}$ (K=1), two times minimum (K=2) and four times minimum (K=4).

Table 3.1: FSCL, Static CMOS, CVSL and DSLL Noise Margins

		K = 1	K = 2	K = 4
FSCL	NM_H	9.7%	6.7%	6.0%
	NM_L	4.6%	4.2%	2.6%
Static CMOS	NM_H	36%	36%	36%
	NM_L	24.6%	24.6%	24.6%
CVSL	NM_H	7.2%	7.2%	7.2%
	NM_L	57.4%	57.4%	57.4%
DSLL	NM_H	10.6%	10.6%	10.6%
	NM_L	47.6%	47.6%	47.6%

3.2 Delay

The rising and falling transition delays of the FSCL inverter can be determined by performing a transient analysis on the FSCL inverter.

3.2.1 Rising edge delay

Consider the circuit shown in Fig. 3.1. The switch S represents the input differential NMOS logic block and capacitor C_L represents the sum of the load, parasitic and wiring capacitances.

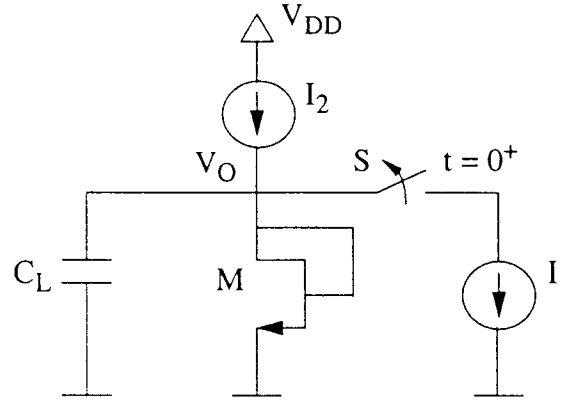

Fig. 3.1 Circuit representing transient operation of a FSCL inverter

Initially, at time $t \leq 0$, the switch S is closed. Thus the steady-state current flowing through transistor M is $(I_2 - I_1)$ and the voltage at the output node, V_{OL}, is given by:

$$V_{OL} = V_T + \sqrt{\frac{I_2 - I_1}{K_n}} \tag{3.10}$$

At time $t = 0^+$, the switch S opens and current I_2 flows through transistor M and capacitor C_L. Using KCL:

$$I_2 = K_n (V_O - V_T)^2 + C_L \frac{dV_O}{dt} \tag{3.11}$$

After transients, the current I_2 flows through the transistor M and the output voltage V_{OH} is:

$$V_{OH} = V_T + \sqrt{\frac{I_2}{K_n}} \tag{3.12}$$

and $I_2 = K_n (V_{OH} - V_T)^2$

Substituting I_2 into equation (3.12):

$$K_n (V_{OH} - V_T)^2 = K_n (V_O - V_T)^2 + C_L \frac{dV_O}{dt} \tag{3.13}$$

$$\frac{dV_O}{dt} + \frac{K_n}{C_L} \cdot V_O^2 - 2\frac{K_n}{C_L} V_T \cdot V_O = \frac{K_n}{C_L} V_{OH} (V_{OH} - 2V_T) \tag{3.14}$$

The solution to this differential equation is [3]:

$$V_O = V_{OH} + \frac{1}{-\frac{K_n}{g_m} + c \cdot e^{\frac{g_m}{C_L} \cdot t}} \tag{3.15}$$

where $g_m = 2K_n(V_{OH} - V_T)$, $c = \frac{K_n}{g_m} + \frac{\sqrt{K_n}}{\sqrt{I_2 - I_1} - \sqrt{I_2}}$

Fig. 3.2 shows a comparison of the output obtained with the HSPICE simulation of a FSCL inverter with that calculated from the transient analysis.

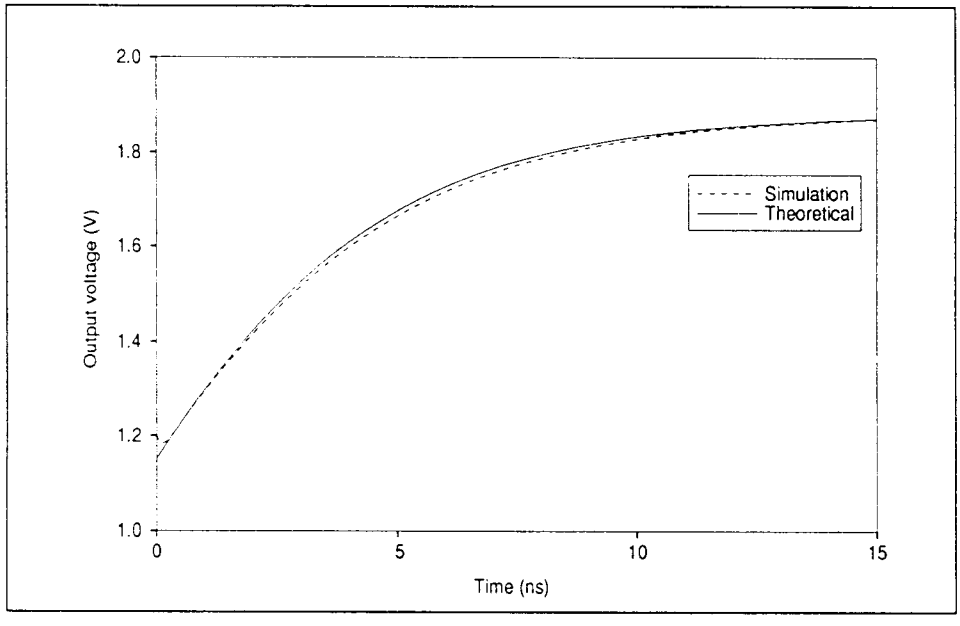

Fig. 3.2 Comparison of simulation and analytical results

It can be seen that the theoretical derivation is a good approximation of the simulation result. The slight discrepancy between the two curves at is due to the fact that the value of K_n is not constant over the output voltage range (K_n = 65.6 μA/V^2 at V_O =1.2 V, K_n = 60.3 μA/V^2 at V_O = 1.8 V). The theoretical derivation assumes that K_n is constant over the voltage range.

3.2.2 Falling edge delay

High-to-low voltage transition analysis is also modeled using the circuit shown in Fig. 3.1. In this case the switch is open at time $t \leq 0$ when the output voltage is V_{OH}. At time $t = 0^+$ the switch closes and the current (I_2 - I_1) flows through transistor M and

capacitor C_L. By applying KCL at the output node:

$$I_2 - I_1 = K_n (V_O - V_T)^2 + C_L \frac{dV_O}{dt} \tag{3.16}$$

The steady-state output voltage is V_{OL}. The solution is similar to the previous case and is given by:

$$V_O = V_{OL} + \frac{1}{-\frac{K_n}{g_m} + c \cdot e^{\frac{g_m}{C_L} \cdot t}} \tag{3.17}$$

where $g_m = 2K_n (V_{OL} - V_T)$ and $c = \frac{K_n}{g_m} + \frac{\sqrt{K_n}}{\sqrt{I_2} - \sqrt{I_2 - I_1}}$

The delays for the high-to-low transition and the low-to-high transition are determined at the mid-point of the output voltage swing, that is, at $V_O = \frac{V_{OH} + V_{OL}}{2}$. Table 3.2 presents the simulated and theoretically determined delays for both the transitions using $\alpha = 1.2$, $I_1 = 79\ \mu A$, $I_2 = 94.8\ \mu A$, $K_n = 62.5\ \mu A/V^2$, $V_T = 0.65$ V, $V_{OL} = 1.2$ V, $V_{OH} = 1.88$ V and a load capacitance $C_L = 0.5$ pF. The load capacitance is chosen large so that the effect of extraneous parasitic capacitances is minimized. The theoretical analysis does not consider the effect of parasitic capacitances separately, hence, the error will be more if a smaller load capacitance is driven by the output node.

Table 3.2: Simulation and Theoretical Delays

Output voltage	Simulation delay	Theoretical delay	Error
L → H	3.25 ns	3.15 ns	3.1%
H → L	3.80 ns	3.80 ns	0.0%

Chapter 4. Simulation of Simple and Complex Gates in Different Topologies

The previous chapter described the analysis of a FSCL inverter gate and some of the theoretical considerations that have to be taken into account in the design of these gates. This chapter presents the comparison of a simple gate (inverter cell) and a complex gate (full-adder cell) in the FSCL topology with some other common topologies: standard static CMOS, cascode voltage switch logic (CVSL)[9] and differential split-level logic (DSLL) [10]. The comparison is made in terms of the simulated gate delay, current spike noise generation, power dissipation at maximum frequency and the power-delay-product for several different power supply voltages, device sizes and capacitive loads. Finally, the performance of these topologies in the design of 8-bit adder sub-systems is evaluated.

4.1 Basic Inverter Simulation System

Each of the four topologies is simulated as a set of 4 inverters shown in Fig. 4.1. The input to the first inverter (G_1) was a pulse with a low-to-high transition at time 0 and high-to-low transition at a later time after the outputs of all the inverters had settled to within 10% of the final output voltage. This ensured that the inverter chain was clocked at the maximum possible frequency. The circuit was simulated in HSPICE using HP 2–μm process parameters from MOSIS to obtain the desired characteristics.

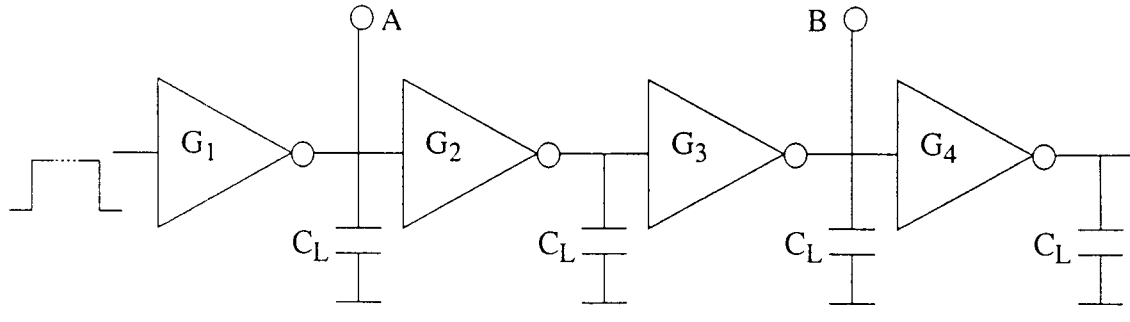

Fig. 4.1. Basic inverter simulation system

The delay was measured at $V_{DD}/2$ between a pair of inverters at points A and B and then divided by two. This took into account low-to-high and high-to-low output transitions for the inverters G_2 and G_3. The power dissipation (at maximum frequency) was measured for inverter G_2 for both the output transitions. The power-delay-product was determined by the product of the average delay and the power dissipated at maximum frequency. Finally, supply noise was measured as the maximum magnitude of the current spikes in the V_{DD} power supply during both output transitions.

4.2 Voltage Scaling effects on Delay, Power, PDP and Noise

The delay, power, PDP and noise of an inverter in each topology was measured for a range of power supply voltages between 2 V and 5 V. The static CMOS, CVSL and DSLL inverters used (4/2) NMOS devices and (8/2) PMOS devices. The FSCL inverter used (4/2) load transistors, $\alpha = 1.2$, $\beta = 3$, $I_1 = 79\ \mu A$ and $\Delta V_O = 0.7$ V.

4.2.1 Delay

The delay of an inverter as a function of power supply with a constant load capacitance is determined by three factors. These are (1) maximum saturation current I, (2) parasitic (C_P) plus load capacitance (C_L) and (3) output voltage swing V. The delay is related to these factors as: $T_D \propto \frac{C \cdot V}{I}$, where $C = C_P + C_L$. The maximum saturation current is proportional to V^2 (long-channel quadratic model). The drain and source parasitic capacitances are dependent on the voltage across the PN junction as given by the following relation [3]:

$$C_P = \sqrt{\frac{\varepsilon_s q N}{2V}} \tag{4.1}$$

where ε_s = dielectric constant of silicon, q = electronic charge, N = substrate doping.

Thus the parasitic capacitances are proportional to $V^{-1/2}$. For no load capacitance, the parasitic capacitances are significant and the delay is dependent on the capacitance and saturation current. For a large load capacitance, the parasitics are dominated and the delay does not significantly depend on voltage variation in parasitic capacitances. The effect of voltage scaling on the delay can thus be described as:

$$\text{Small } C_L: \qquad T_D \propto \frac{C \cdot V}{I} \propto \frac{V^{-1/2} \cdot V}{V^2} = V^{-1.5} \tag{4.2}$$

$$\text{Large } C_L: \qquad T_D \propto \frac{C \cdot V}{I} \propto \frac{const \cdot V}{V^2} = V^{-1} \tag{4.3}$$

The delay versus supply voltage graph for $C_L = 0$ pF is shown in Fig. 4.2. The static CMOS, CVSL and DSLL inverters exhibit $V^{-1.5}$ dependence. For instance, using polynomial fit, the CVSL curve is described by the polynomial $(1.464 + 57.94V^{-1.5})$. However, as shown in Fig. 4.2, FSCL delay does not depend on supply variations since its delay is a function of constant currents I_1 and I_2 (Fig. 2.1).

Fig. 4.3 shows the delay curves when the load capacitance is increased to 0.3 pF. The delays for static CMOS, CVSL and DSLL topologies increase as supply voltage is decreased as $T_D \propto V^{-1}$. Again the FSCL delays are almost constant for a given current.

4.2.2 Power

The dynamic power dissipated in a static topology circuit is given by:

$$P = fCV^2 \tag{4.4}$$

The overlap current also causes power dissipation, however, its magnitude is small as the inverters are switched at maximum frequency. This component of power dissipation is neglected here. The maximum frequency of operation is inversely proportional to the gate switching delay T_D of the pull-up/pull-down FETs. Thus the dependence of power dissipation on voltage at maximum frequency is:

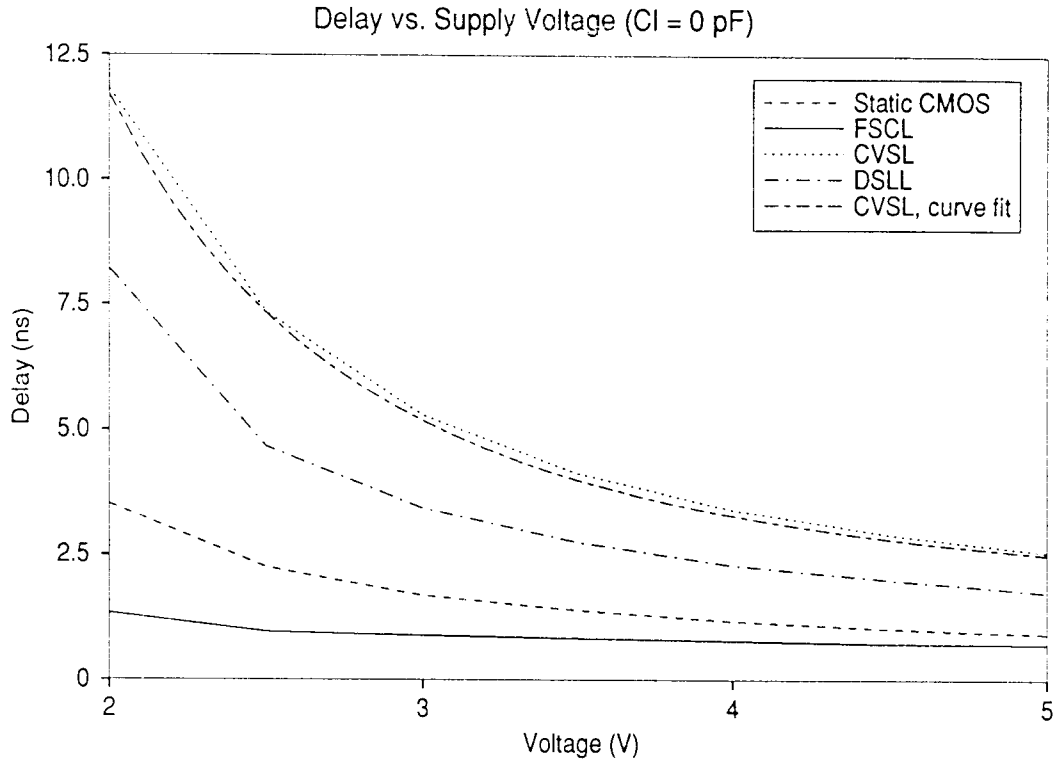

Fig. 4.2 Delay with voltage scaling for C_L = 0 pF

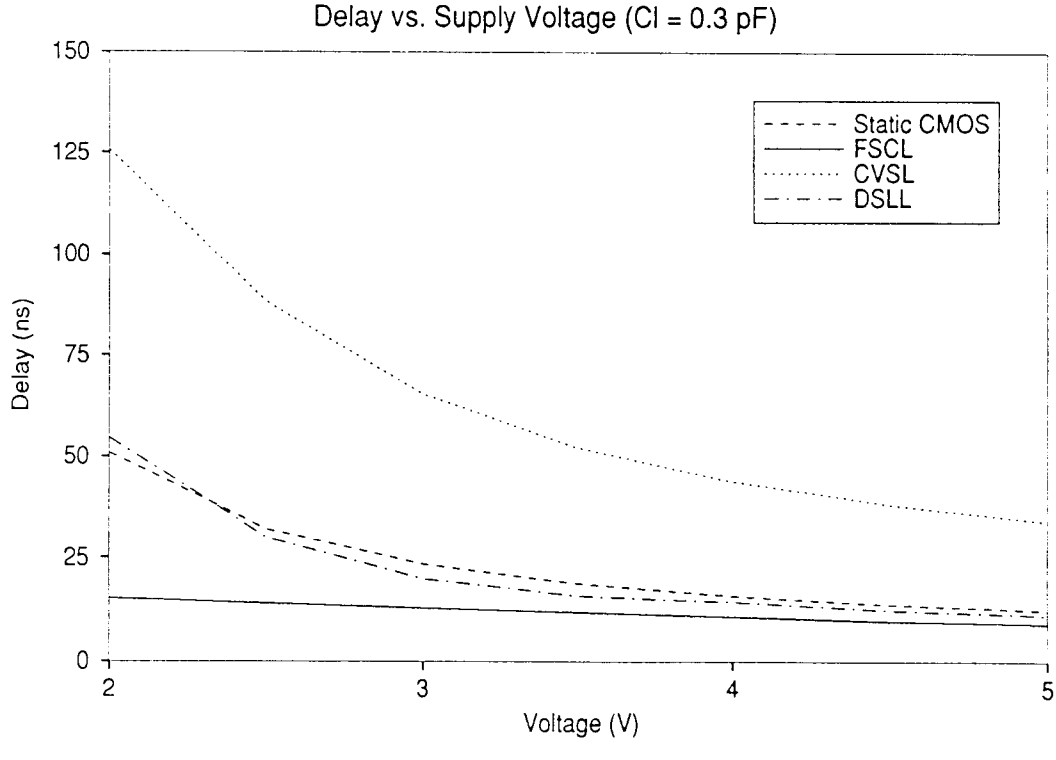

Fig 4.3 Delay with voltage scaling for C_L = 0.3 pF

$$P = f_{max} CV^2 \propto T_D^{-1} CV^2 \propto \frac{I}{CV} CV^2 \propto \frac{V^2}{V} V^2 = V^3 \tag{4.5}$$

as $I \propto V^2$. The capacitance C does not affect the power dissipation at maximum frequency.

For FSCL current-mode operation, the power is $2I_2V$. Since I_2 is constant, the dependence of power dissipation in FSCL is:

$$P = 2I_2V \propto const \cdot V \propto V \tag{4.6}$$

Fig. 4.4 shows the power versus supply voltage for 0 pF load capacitance. Static CMOS, CVSL and DSLL show V^3 dependence as the static CMOS curve fit polynomial ($-1.78 + 1.21V^3$) indicates. The power in FSCL increases linearly with voltage.

The power dissipation with a load capacitance of 0.3 pF is graphed in Fig. 4.5. Again the curve fit polynomial ($1.95 + 1.29V^3$) indicates V^3 dependence for static CMOS, and FSCL has a linear graph. The power dissipation values are similar to those observed in Fig. 4.4. This can be explained as follows. When the load capacitance is increased by a factor α to αC, the maximum frequency of operation decreases by the same factor to f/α because the delay is proportional to the capacitance. Hence the product fC remains constant for voltage variation.

4.2.3 Power-delay-product

The power-delay-product (PDP), defined as the "energy per switching event", varies with voltage scaling as,

Small C_L: $$PDP = P \cdot T_D \propto V^3 \cdot V^{-1.5} = V^{1.5} \tag{4.7}$$

Large C_L: $$PDP = P \cdot T_D \propto V^3 \cdot V^{-1} = V^2 \tag{4.8}$$

For FSCL the dependence is,

$$PDP = P \cdot T_D \propto V \cdot const \propto V \tag{4.9}$$

Figures 4.6 and 4.7 show the simulation data for load capacitances of 0 pF and 0.3 pF. For FSCL, the PDP has linear dependence on voltage.

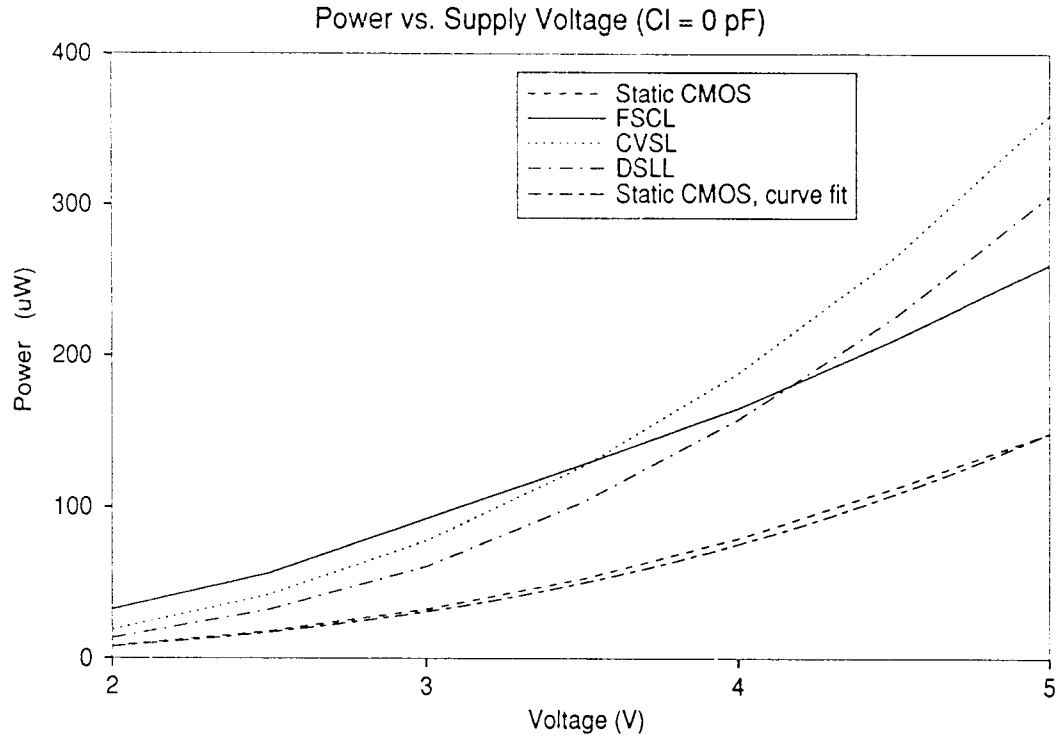

Fig 4.4 Power dissipation with voltage scaling for C_L = 0 pF

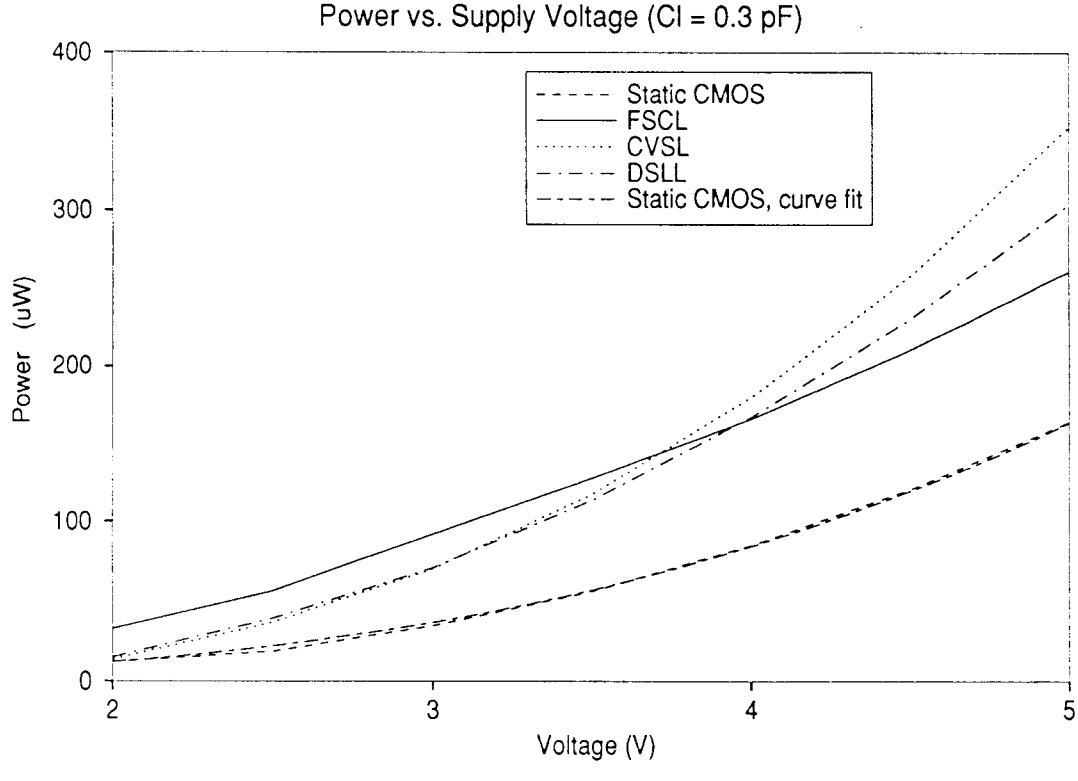

Fig 4.5 Power dissipation with voltage scaling for C_L = 0.3 pF

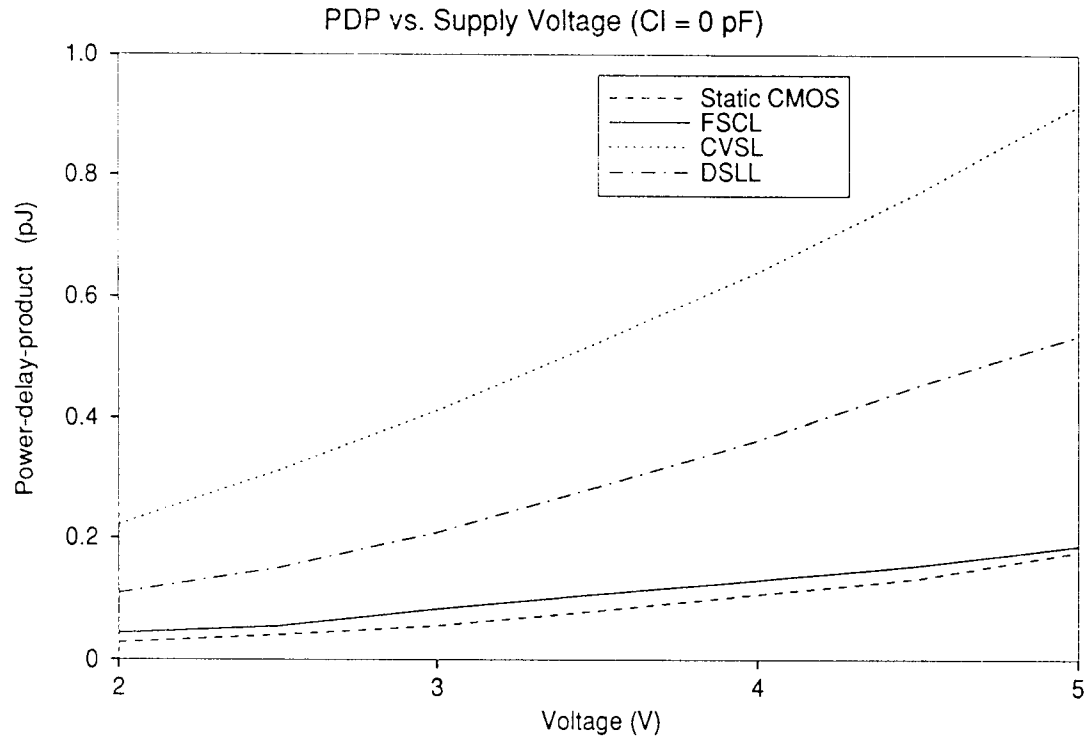

Fig 4.6 Power-delay-product with voltage scaling for C_L = 0 pF

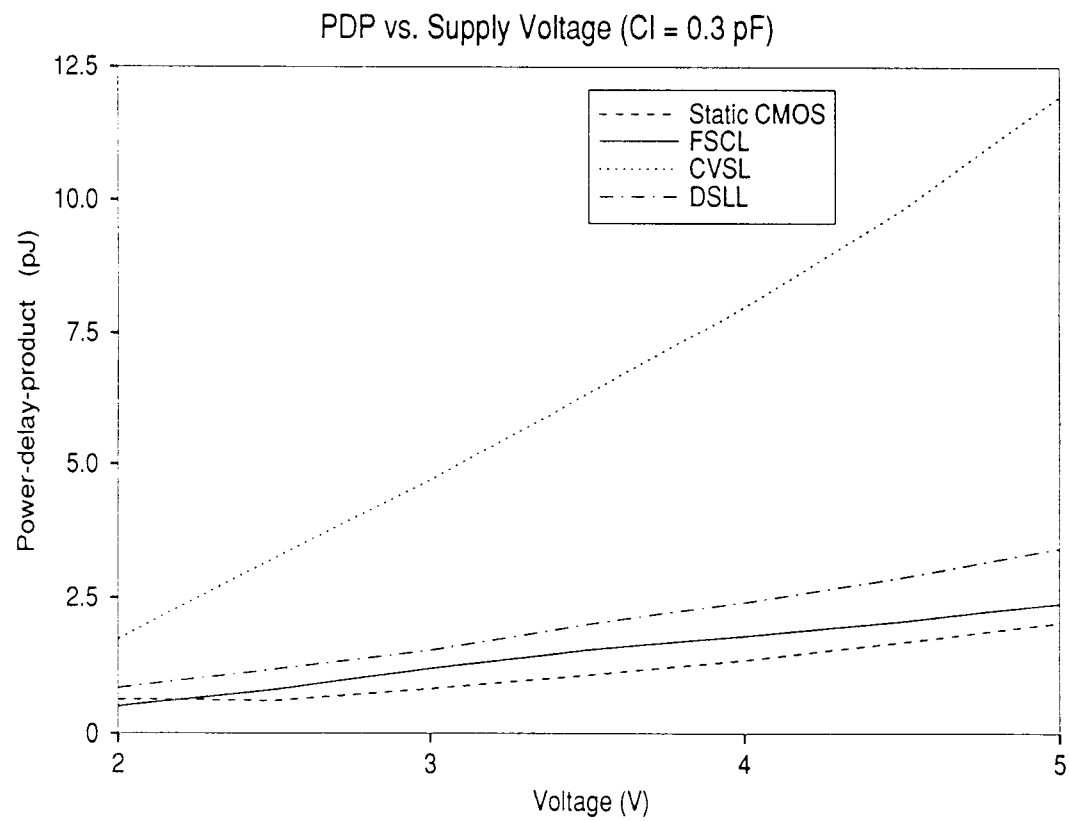

Fig 4.7 Power-delay-product with voltage scaling for C_L = 0.3 pF

4.2.4 Noise

The current spike noise generated by FSCL is on average one to two orders of magnitude lower than in other topologies (Fig. 4.8). The noise generated in static CMOS, CVSL and DSLL is larger at higher voltages because the delays are less and thus the current spikes are larger. At 0.2 pF load capacitance (Fig. 4.9) the noise generated in FSCL is lower while in the other circuits it remains approximately the same.

4.3 Device Scaling effects on Delay, Power, PDP and Noise

The device sizes were scaled for each of the circuits while supply voltages are kept constant at 3.3 V. The device scaling factor (K) varied from 0.25 to 16 with an increase of a factor of 2 at each step. Device size K=1 corresponded to (W/L) = 2/1 for NMOS transistors and (W/L) = 4/1 for PMOS transistors. The delay, power, PDP and noise parameters were measured for each value of K for the topologies.

4.3.1 Delay

For each topology the delay is proportional to C_T/I, where C_T is the total capacitance at the output node and I is the pull-up or pull-down current. The capacitance C_T is the sum of the load capacitance C_L, gate capacitance C_G of the next inverter and the drain and source parasitic capacitance C_P. C_G and C_P are each proportional to the (W.L) product of the corresponding transistors. For device sizes greater than K=1, W increases and hence capacitance is proportional to K. For device sizes less than 1, L increases and again capacitance increases. Thus we can write,

For $K \geq 1$, $C \propto K$

For $K < 1$, $C \propto 1/K$ (4.11)

where $C = C_G + C_P$.

In the case of static CMOS, CVSL and DSLL, $I = \mu C_{OX} K (W/L)_{min} (V_{GS} - V_T)^2$ and hence $I \propto K$. When there is no load capacitance, the relationship of delay T_D to the

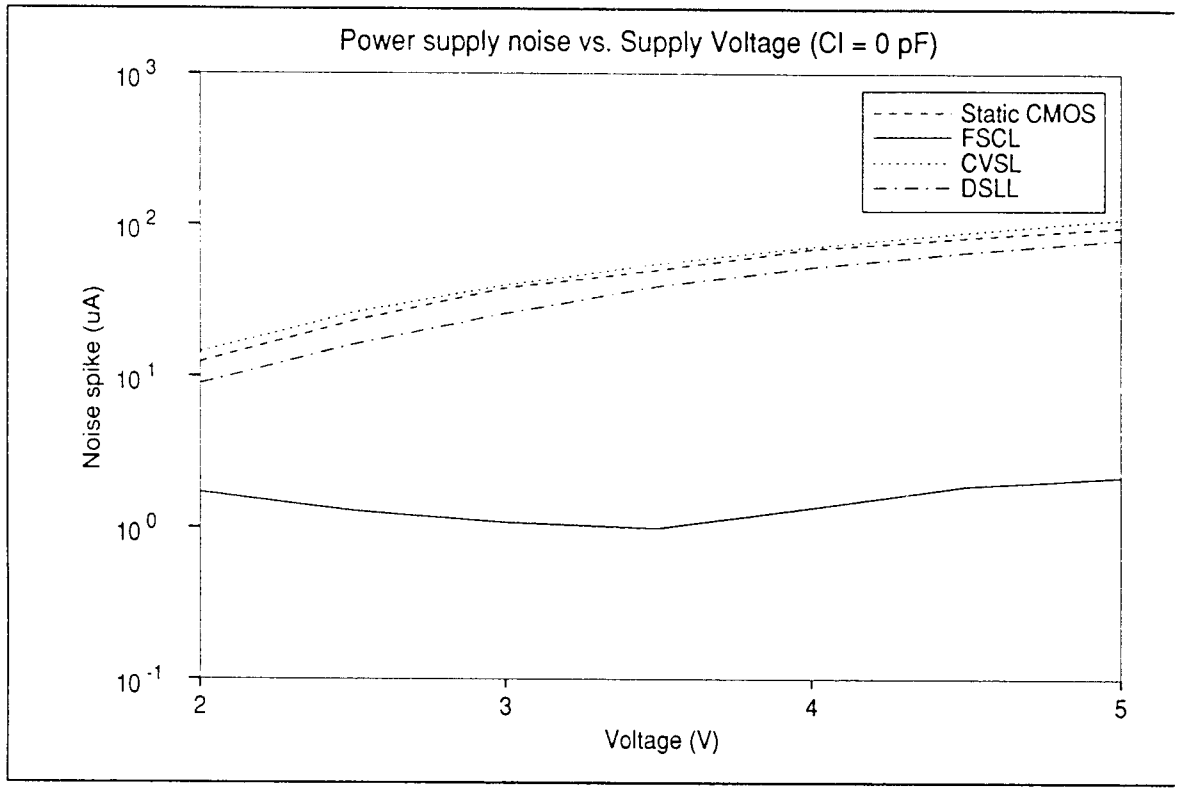

Fig 4.8 Power supply noise with voltage scaling for C_L = 0 pF

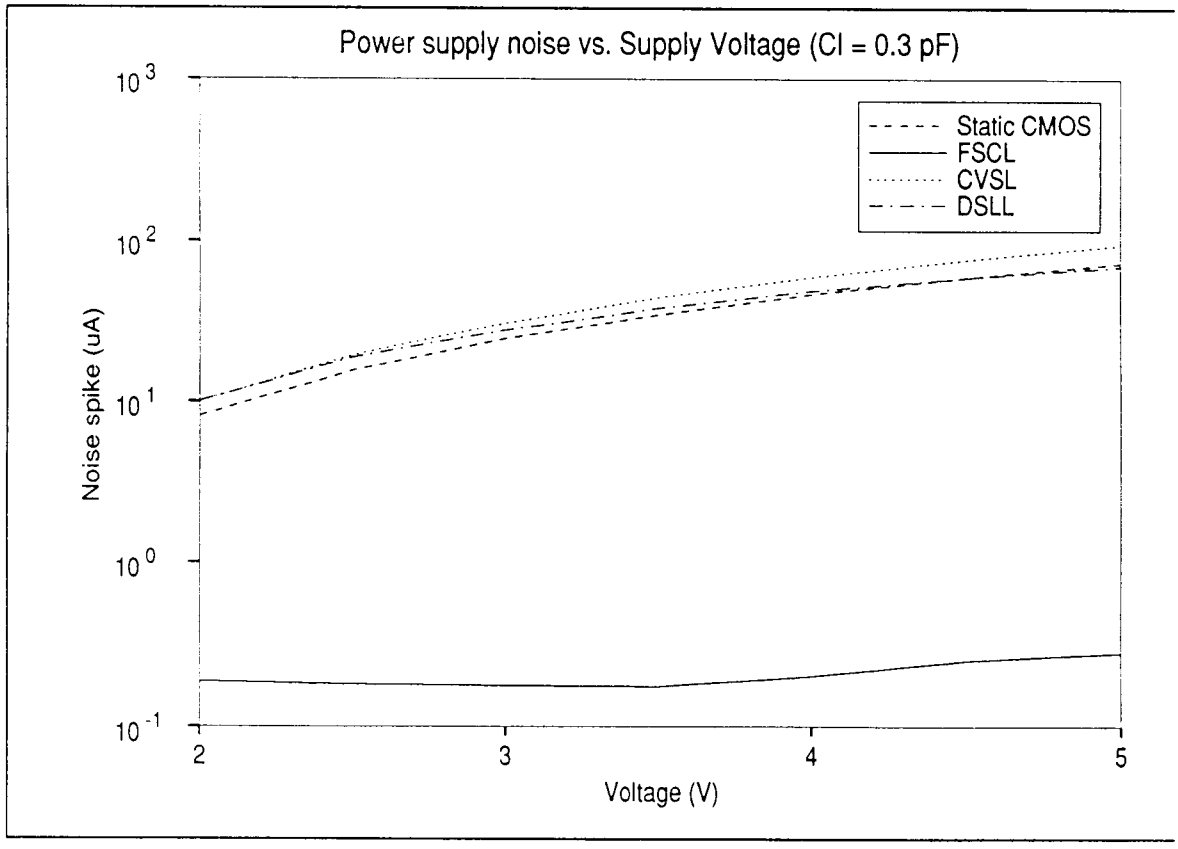

Fig 4.9 Power supply noise with voltage scaling for C_L = 0.3 pF

scaling factor K is given by,

$$T_D \propto \frac{C}{I} \propto K \cdot \frac{1}{K} = const \qquad \text{for } K \geq 1$$

$$\propto \frac{1}{K} \cdot \frac{1}{K} = \frac{1}{K^2} \qquad \text{for } K < 1 \tag{4.12}$$

When there is a large load capacitance, the changes in C_G, C_P due to scaling are dominated by C_L which is constant and then the delay is inversely proportional to I. Thus,

$$T_D \propto \frac{1}{I} \propto \frac{1}{K} \tag{4.13}$$

In the case of FSCL, the output voltage swing ΔV_O is kept constant for all device sizes. From eqn. 2.4, the change in I_2, I_1 required to keep ΔV_O constant when device size changes by a factor K is equal to K itself. Thus $I \propto K$. This dependence of I on K is the same as for the other topologies and hence the relations for T_D are the same for FSCL.

Fig. 4.10 shows the delays obtained for load capacitances of 0 pF and 0.5 pF. For C_L = 0pF, the delays are constant for $K > 1$ as predicted and increase rapidly for $K < 1$. For the large capacitance C_L = 0.5 pF, the delays are proportional to K^{-1} and each curve has a slope of -1 on the log-log graph.

4.3.2 Power

The power dissipation in static CMOS, CVSL and DSLL circuits is given by $P = fC_TV_{DD}^2$. Voltage being constant, we have $P \propto fC_T$. f is the frequency of maximum operation and hence $f \propto T_D^{-1}$. Thus $P \propto C_T/T_D$. Using the relations developed in the previous section we can write the dependence of P on scaling factor K for small and large load capacitances as follows,

Small C_L: $$P \propto \frac{C}{T_D} \propto \frac{K}{const} = K \qquad \text{for } K \geq 1$$

$$\propto \frac{1}{K} \cdot \frac{1}{K^{-2}} = K \qquad \text{for } K < 1 \tag{4.14}$$

Large C_L: $$P \propto \frac{C_L}{T_D} \propto \frac{const}{K^{-1}} = K \tag{4.15}$$

The power dissipation is proportional to device scaling factor over the whole range, irrespective of the load capacitance.

In the case of FSCL, the power dissipation is $2I_2V_{DD}$. As we have seen, $I \propto K$. Thus $P \propto K$, V_{DD} being constant. This relation is same as for the other topologies.

Fig. 4.11 shows the power dissipation for $C_L = 0$ pF. Each of the topologies has a linear curve. The same linearity is also seen for $C_L = 0.5$ pF (Fig. 4.12).

Comparing Fig. 4.11 and Fig. 4.12, we observe that the power dissipation for each topology is very close for both load capacitances. This is explained as follows. Let P_K be the power dissipation at scaling factor K. Then,

$$P_{K,\,C_L = 0pF} = f_K C_K V_{DD}^2 \tag{4.16}$$

where C_K is the sum of gate and parasitic capacitances at scaling factor K. If we now connect a large fixed load capacitor of value αC_K at the output node the effect of C_K is suppressed. The maximum frequency of operation immediately fall by α to f_K/α. Thus,

$$P_{K,\,C_L = \alpha C_K} = \left(\frac{f_K}{\alpha}\right)(\alpha C_K) V_{DD}^2 = f_K C_K V_{DD}^2 \tag{4.17}$$

The same power dissipation is obtained in both cases.

4.3.3 Power-delay-product

We have seen that $P \propto K$ and delay can be expressed by different relations depending on the value of C_L. Combining these, the relations for PDP are developed,

Small C_L: $$PDP = P \cdot T_D \propto K \cdot const \propto K \qquad \text{for } K \geq 1$$

$$\propto K \cdot \frac{1}{K^2} = \frac{1}{K} \qquad \text{for } K < 1 \tag{4.18}$$

Large C_L: $$PDP = P \cdot T_D \propto K \cdot \frac{1}{K} = const \tag{4.19}$$

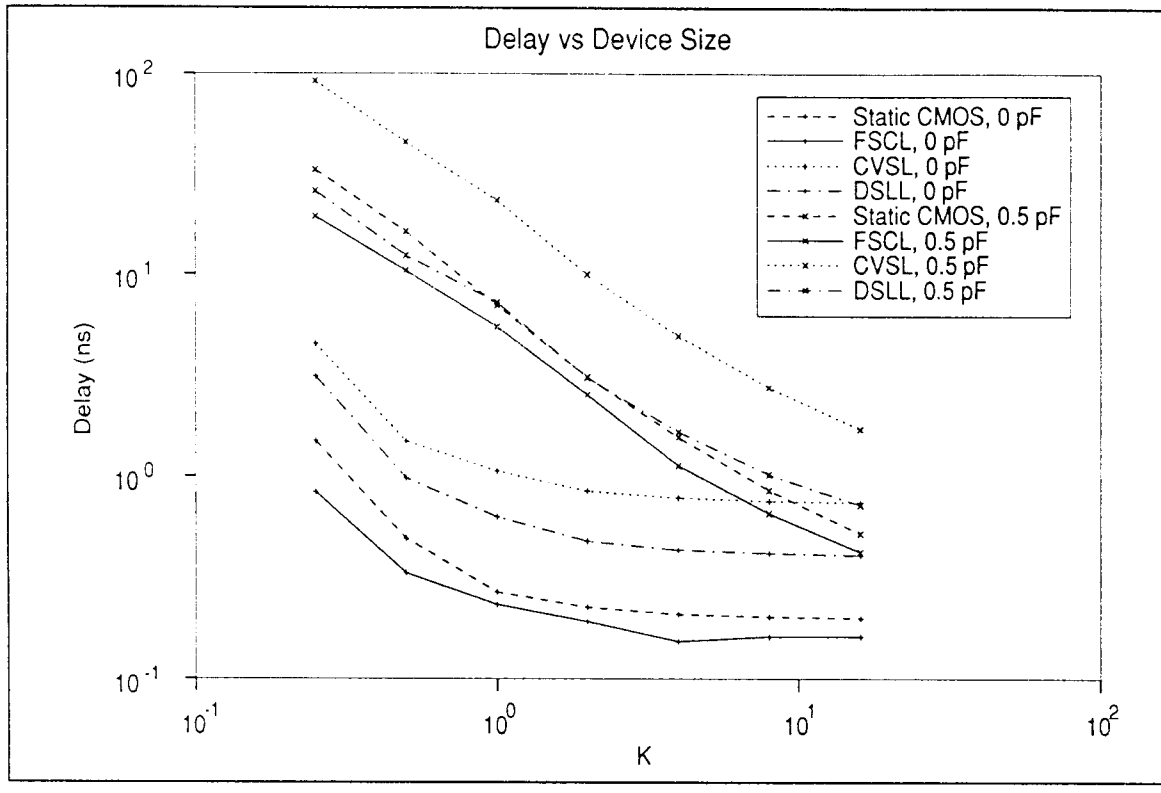

Fig. 4.10 Delay with device scaling for C_L = 0 and 0.5 pF

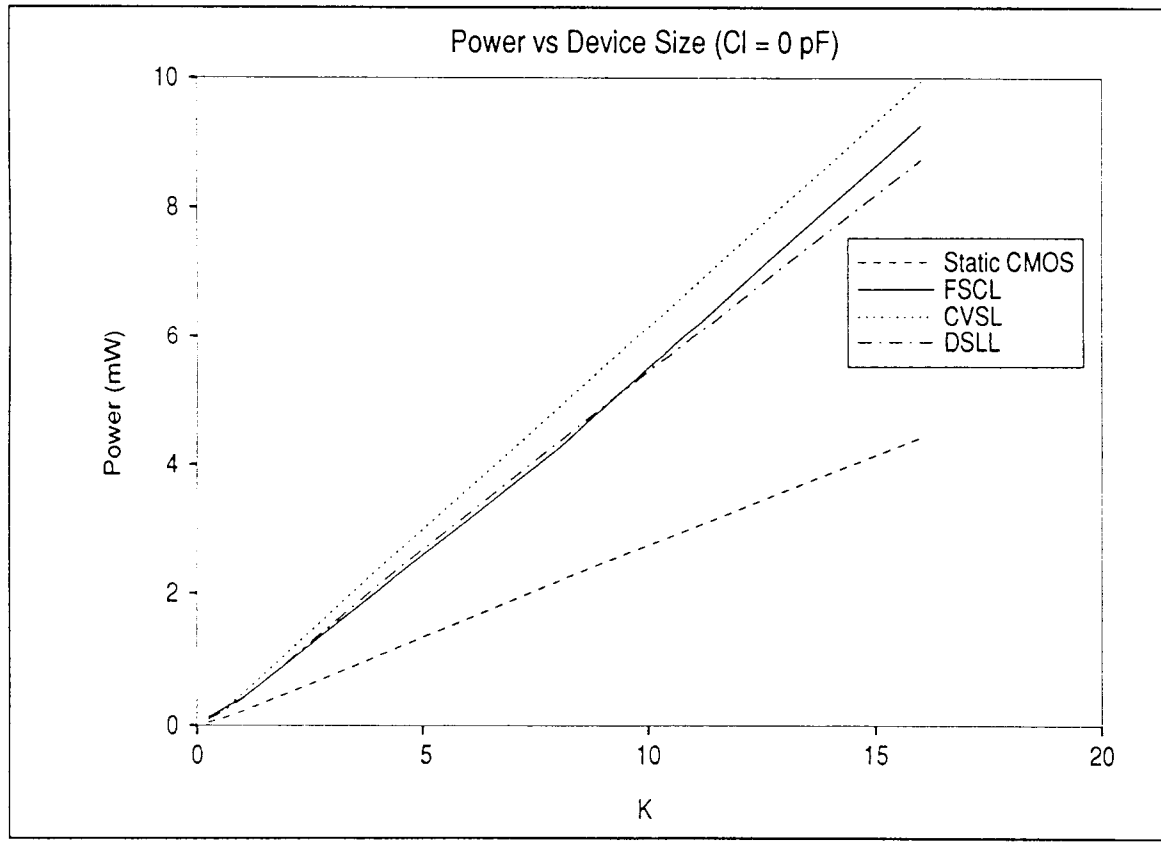

Fig. 4.11 Power dissipation with device scaling for C_L = 0 pF

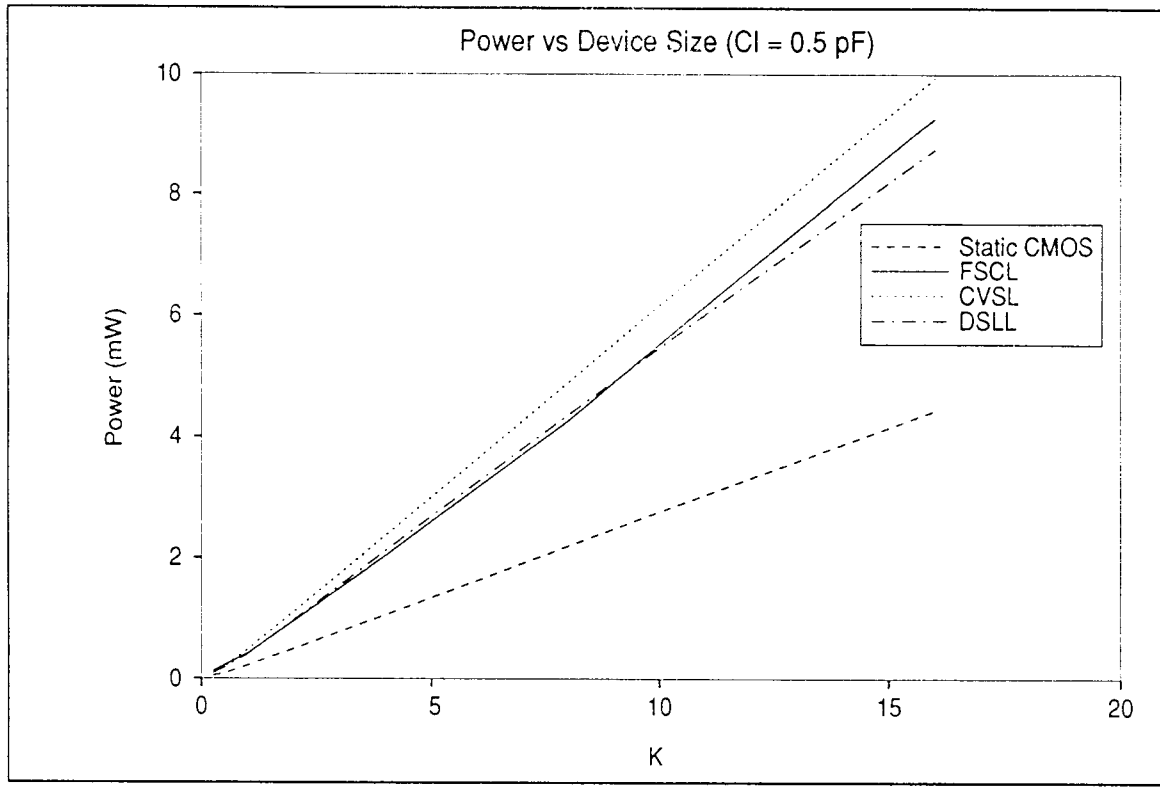

Fig. 4.12 Power dissipation with device scaling for C_L = 0.5 pF

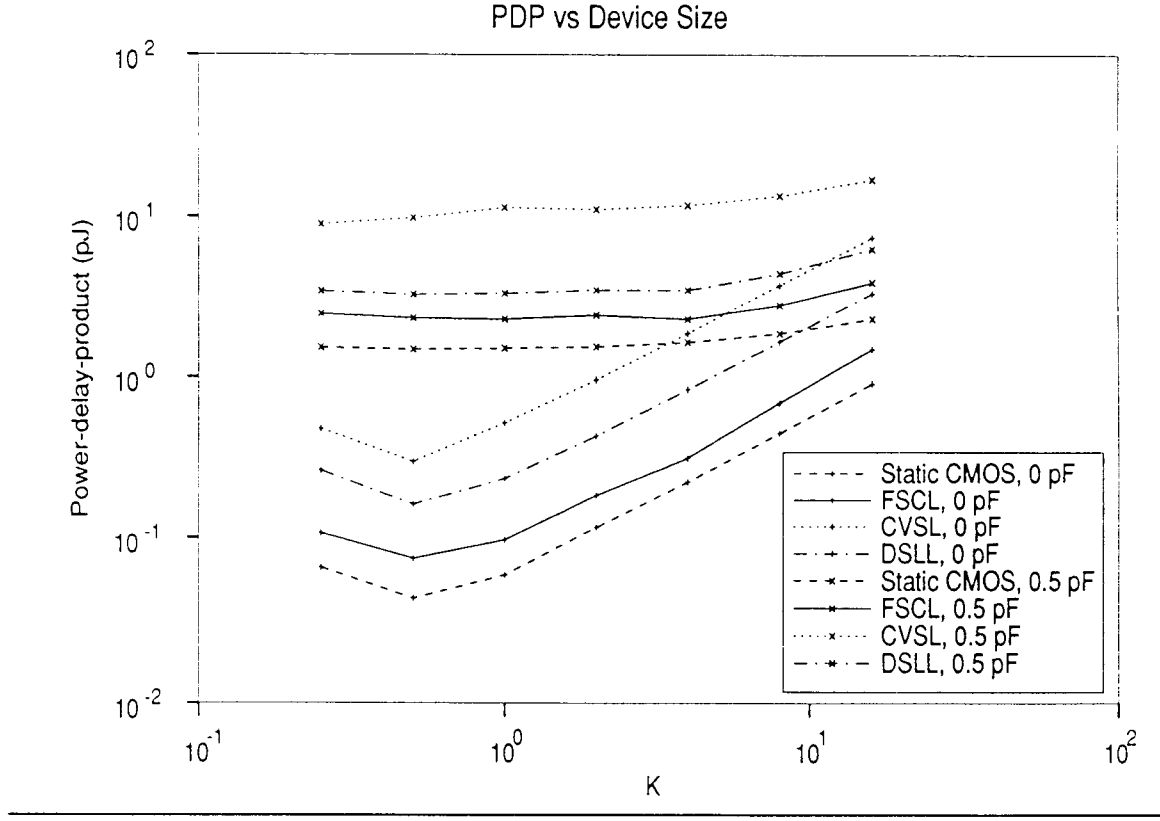

Fig. 4.13 Power-delay-product with device scaling for C_L = 0 and 0.5 pF

This dependence of PDP on K is the same for each topology and is shown in Fig. 4.13. For the case of C_L = 0 pF, the curves have a minimum power-delay-product at K=0.5 and then increases linearly with slope 1 for $K \geq 1$. For C_L = 0.5 pF the PDP does not show much change over the whole range of scaling, as predicted.

4.3.4 Noise

The power supply current spike noise generation in the FSCL inverter is lower by a factor of 20 than in the other topologies when the load capacitance in 0 pF (Fig. 4.14). For C_L = 0.5 pF (Fig. 4.15), the difference in noise becomes two orders of magnitude. In each case the noise increases linearly with K.

4.4 Delay vs. Load Capacitance

From simulation it is seen that the delay for each topology increases linearly with load capacitance. Fig. 4.16 shows the delays obtained for K=8 device sizes and V_{DD}=5 V. The increase in delay is lowest for static CMOS and FSCL inverters. Fig. 4.17 shows the delays when K=0.5 and supply voltage is reduced to 3.3 V. Here also the increase in delay is linear.

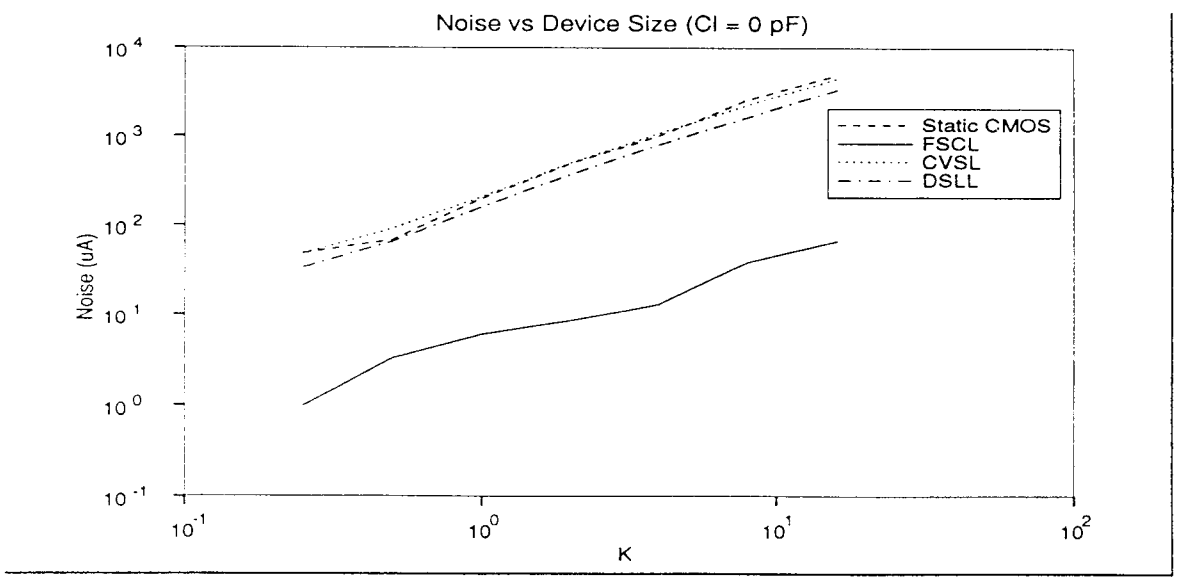

Fig 4.14 Power supply noise with device scaling for C_L = 0 pF

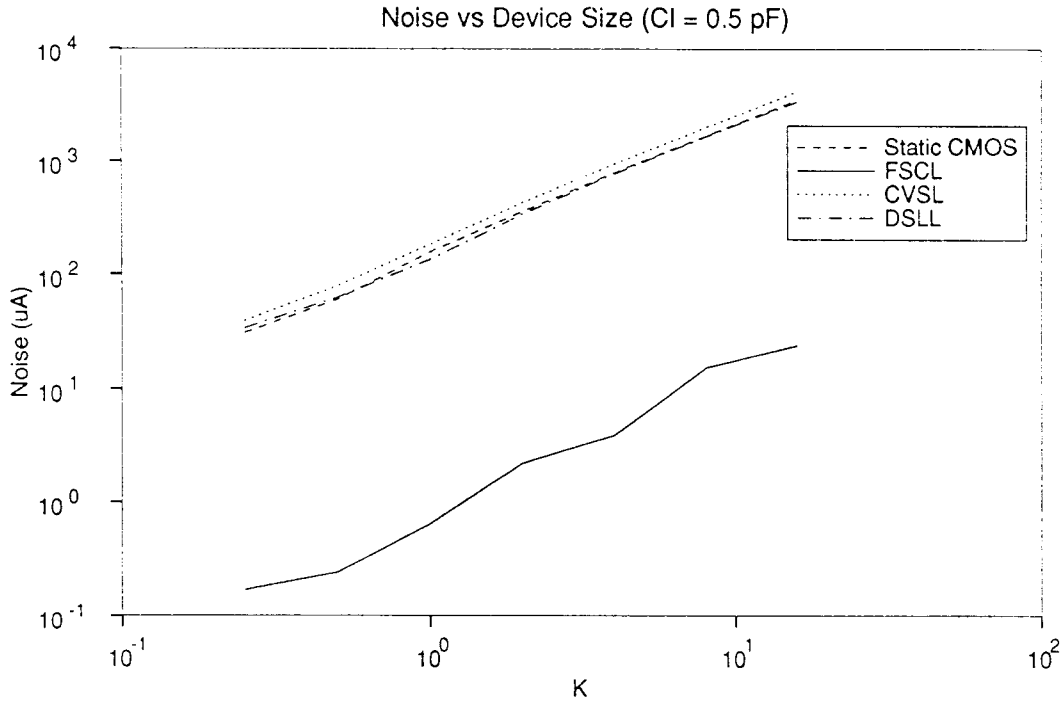

Fig 4.15 Power supply noise with device scaling for C_L = 0.5 pF

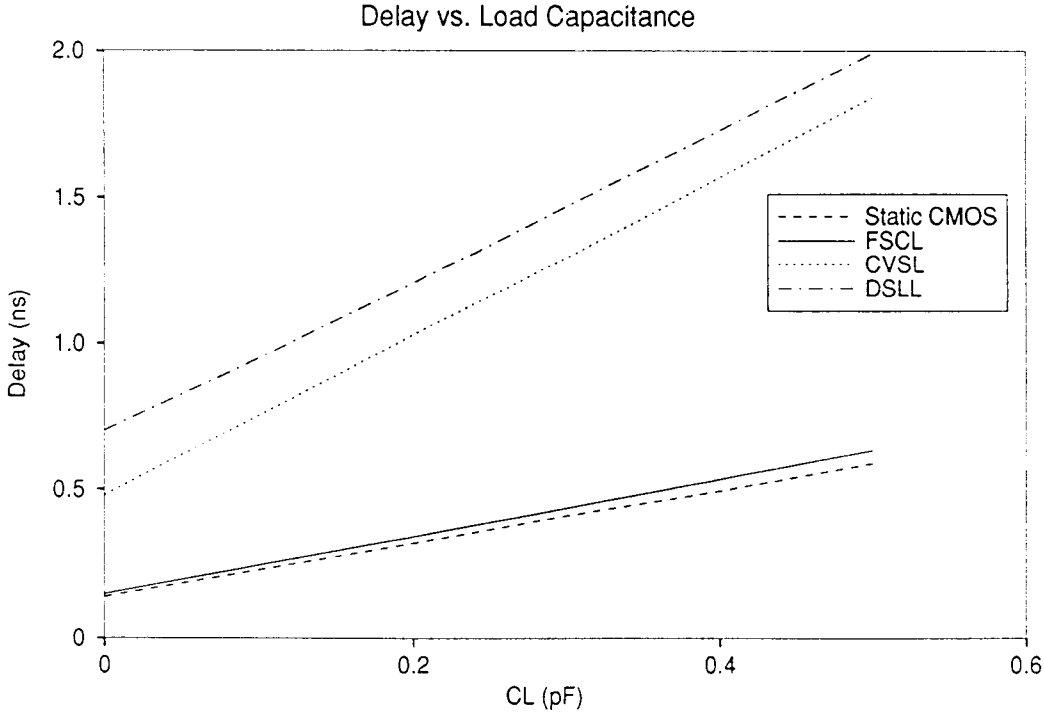

Fig. 4.16 Delay vs. Load Capacitance for K=8 and V_{DD}=5 V

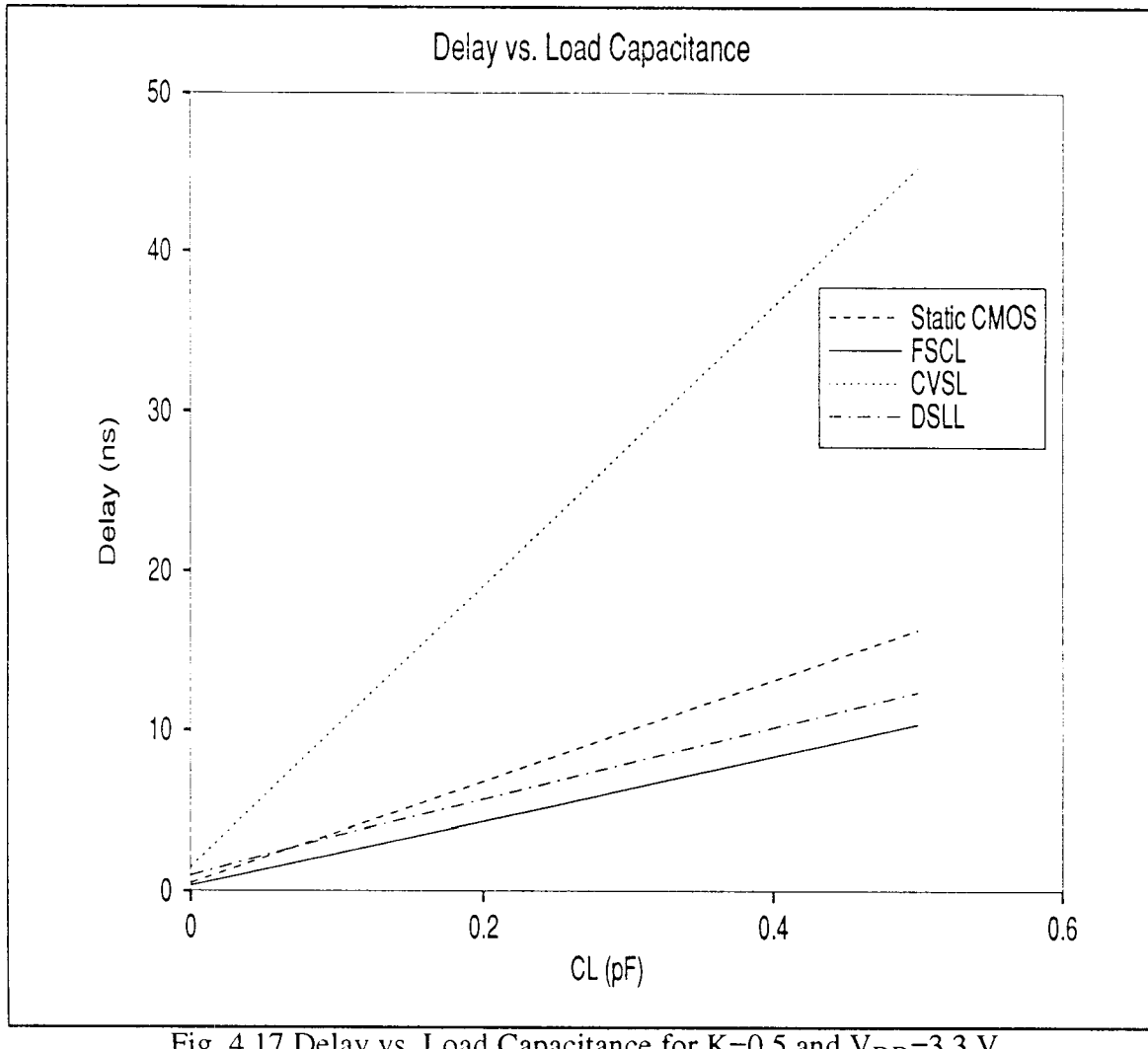

Fig. 4.17 Delay vs. Load Capacitance for K=0.5 and V_{DD}=3.3 V

4.5 Comparison of Full-Adders

In the previous sections the characteristics of a simple inverter gate in FSCL, CVSL, DSLL and standard static CMOS were compared. However, to gain a deeper understanding of the merits and demerits of each topology, it is necessary to extend the comparison to more complex gates. In the rest of this chapter, a full adder gate is developed in FSCL, CVSL, DSLL and static CMOS and is then used to construct a carry-ripple adder, carry-skip adder and a carry-lookahead adder. Comparisons are made among these topologies in terms of delay, power, power-delay-product, noise spikes and area.

4.6 The Full-Adder Cell

The full adder is one of the basic gates and is the main "number-crunching" element in microprocessors and digital filters. It is clearly a subsystem which deserves some attention. Various topologies can be used to implement adders subsystems and the speed limitation of fast mixed-mode systems will depend on the correct choice.

The full adder was implemented in FSCL, CVSL, DSLL and static CMOS and simulated using HSPICE with level-3 parameters from a typical MOSIS 1–μm process. Each adder cell implemented the sum and carry equations as follows:

$$S = (A \cdot \overline{B} + \overline{A} \cdot B)\,\overline{C}_{in} + (A \cdot B + \overline{A} \cdot \overline{B})\,C_{in}$$

$$C_{out} = A \cdot B + (A \cdot \overline{B} + \overline{A} \cdot B)\,C_{in} \qquad (4.20)$$

Fig. 4.18 shows the block diagram of the system used for simulating the full adder. A pulse input was provided to the inputs of the adders A_1 and A_2. These adders converted the input pulse to a realistic output waveform that was provided as input to the test adder A_T. The adder A_L acts as the load device to the test adder, as would be the case if the adder under test was a part of a carry ripple chain. When the pulse input is low, the inputs to the test adder are low and when the input pulse goes high, all the test adder inputs go high. This provides the worst-case delays on the sum and carry-out outputs of the test adder.

The FSCL implementation of the full adder is shown in Fig. 4.19 and 4.20. Fig. 4.19 shows the sum part and Fig. 4.20 shows the carry part of the full adder. The device sizes chosen for the FSCL full adder circuit are shown in Table 4.1. The load transistors are minimum size (2/1). The input pull-down path is made two times larger than the load transistor to obtain adequate noise margins and to ensure that the output voltage

does not degrade. As there are at most 3 transistors in series in the pull-down path, each input transistor is of size 12/1.

Table 4.1: FSCL adder device sizes

M_{I1}, M_{I21}, M_{I22}	M_{L1}, M_{L2}	M_1 through M_{10}
8 / 1	2 / 1	12 / 1

The value of α (I_2/I_1) chosen is 1.2. The current I_1 is 95 μA which gives an output voltage swing of 0.5 V. The current I_2 is $1.2 * I_1 = 114$ μA.

The simulation results obtained for static CMOS, FSCL, CVSL and DSLL full adders are presented in Table 4.2.

Table 4.2: Comparison of full adders implemented with different logic structures

	# of N devices / # of P devices	Delay carry propagation time (ns)	Power dissipation at max. freq. (mW)	Power-Delay-Product (pJ)	Current spike noise (μA)
Static CMOS	15 / 15	0.70	1.03	0.72	2374
FSCL	24 / 4	0.56	1.53	0.85	13
CVSL	20 / 4	0.92	1.90	1.75	852
DSLL	24 / 4	0.58	1.75	1.02	684

These results indicate that the FSCL full adder is faster than the static CMOS adder by a factor of 1.25. FSCL is also faster than the other differential logic structures tested, being 64% faster than CVSL and 4% faster than DSLL. DSLL exhibits speed comparable to FSCL because the voltage swing at some to the internal nodes is only half of V_{DD}. The highest speed in FSCL is due to the low output voltage swing of only 0.5 V. The time taken to charge and discharge the load capacitance is less and the dynamic

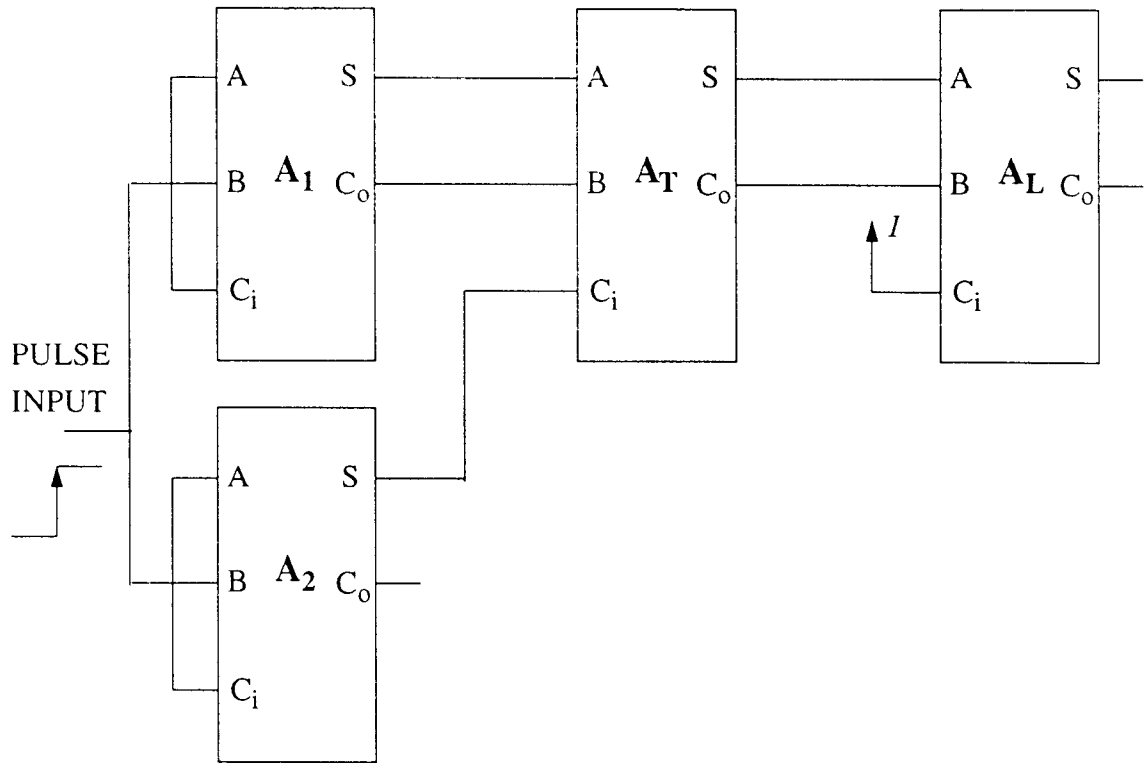

Fig. 4.18 Block diagram of the adder system used for HSPICE

power dissipation is also less. However, the FSCL gate exhibits static power dissipation and thus the power dissipated at maximum frequency is greater than that dissipated in static CMOS. In the CVSL and DSLL differential circuits, the larger voltage swings and positive feedback latches cause increased dynamic power losses and short-circuit (or overlap) currents. Thus the total power losses are greater than in static CMOS and FSCL, with DSLL showing slightly less power dissipation due to reduced voltage swing.

The energy per "switching event", as defined by the power-delay product is slightly greater for FSCL than for static CMOS. However, it should be noted that the power dissipation is calculated at the maximum switching frequency and that at lower frequencies the static

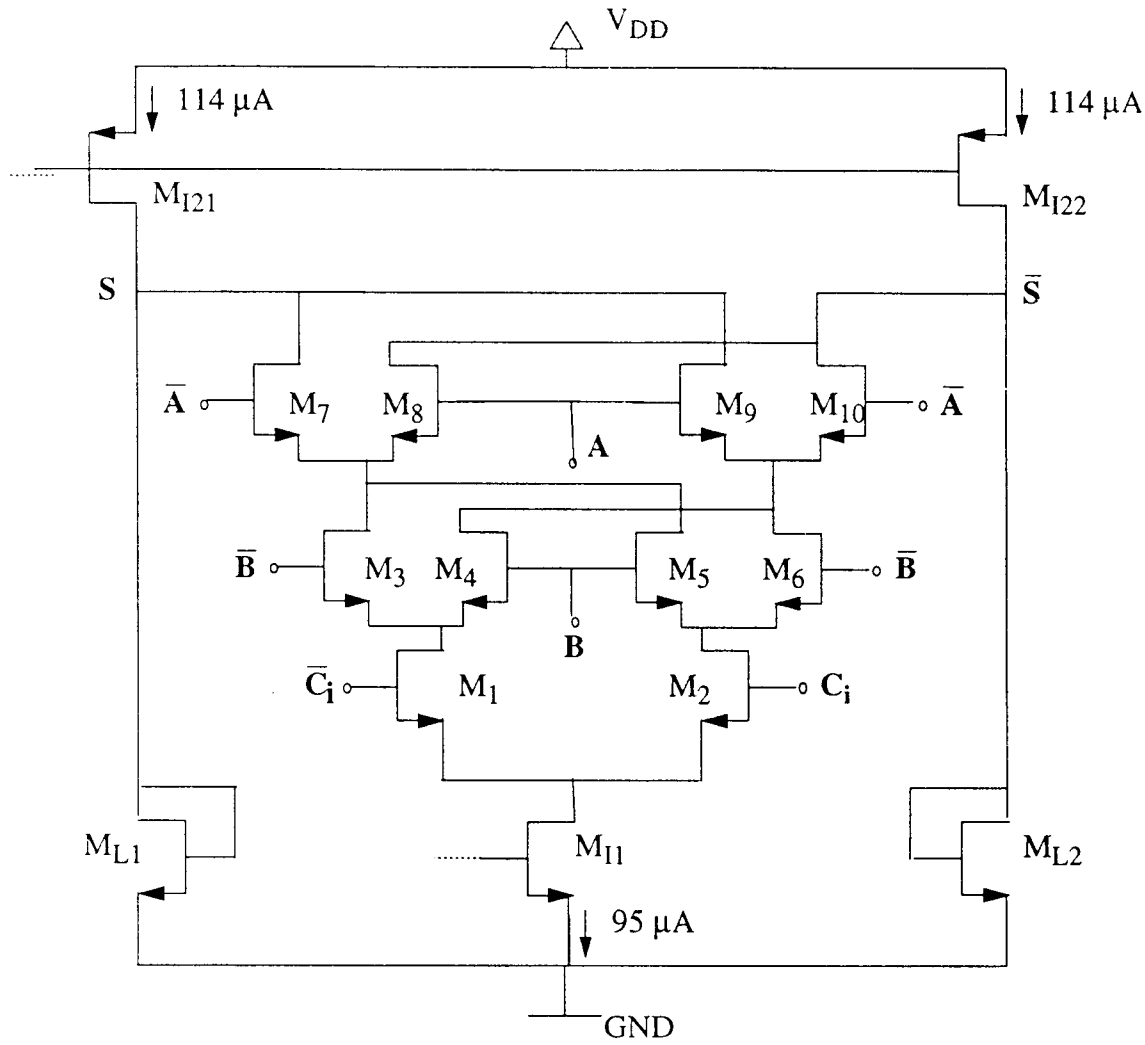

Fig. 4.19 Schematic for FSCL sum generation circuit

power dissipation dominates in FSCL and PDP increases. In other topologies the average power decreases with decreasing frequency leading to decreasing PDP. Thus the optimal use of FSCL will be in very high speed applications, where the data is pipelined so that switching frequencies approaching the maximum possible are obtained.

The suitability of FSCL for mixed-mode systems is indicated by the power supply current spike data. The current-mode operation of FSCL leads to noise spikes that are at

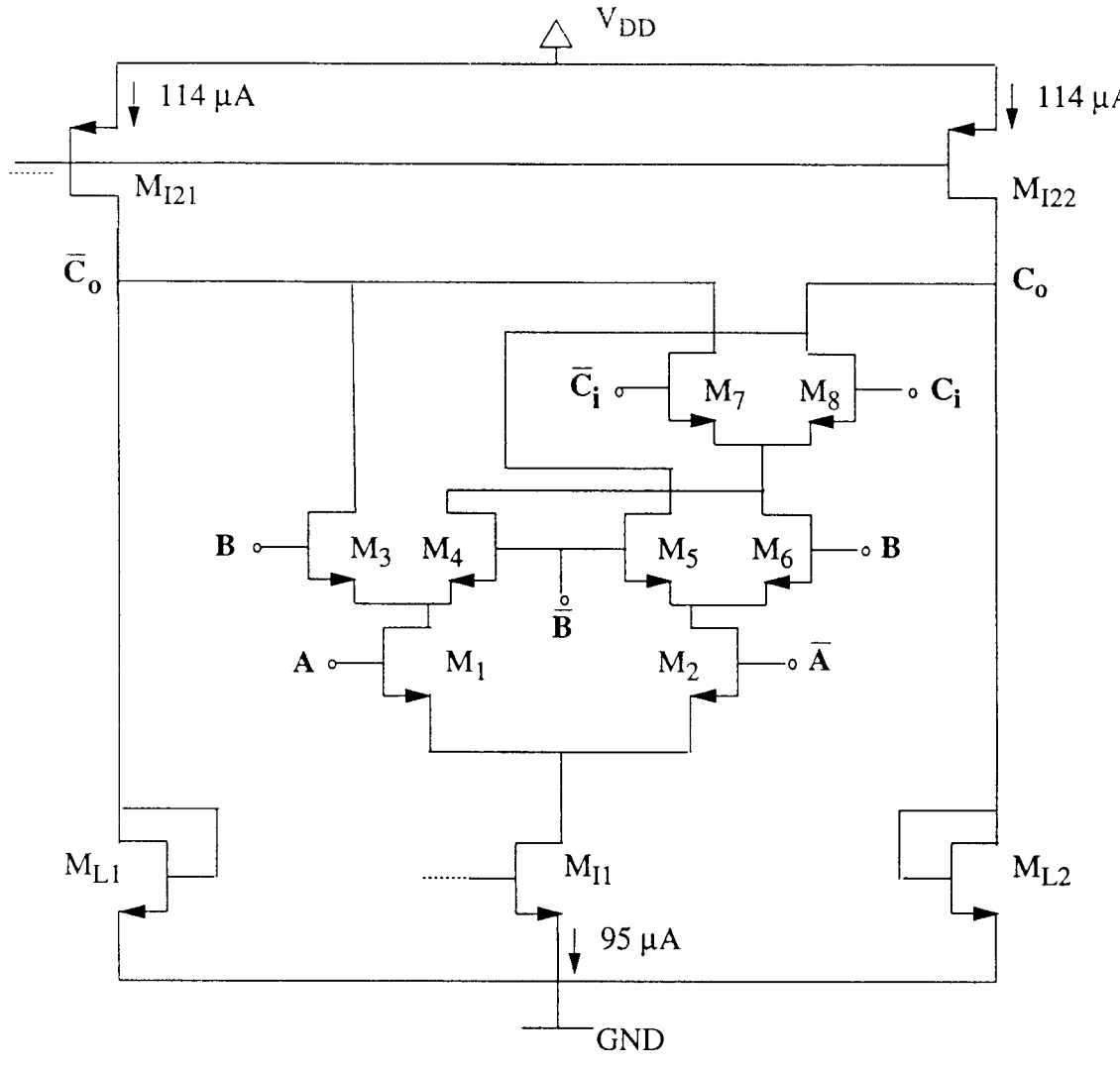

Fig. 4.20 Schematic for FSCL carry-out generation circuit

least 53 times lower than any other logic structure. This "quiet operation" is indispensable to complex high-precision mixed-mode systems like delta-sigma converter and other data converters.

4.7 Carry-Ripple Adder

The carry-ripple adder (CRA) is implemented by cascading 8 full adders in a carry ripple chain. Comparisons of various implementations of CRA are made in terms of

average per bit delay, power dissipation, current noise spikes and area. The delay is obtained from the addition of the input vectors (11111111) and (00000000) having first bit carry input equal to a step function at time zero.

The delays obtained for the four different implementations of the CRA with different logic structures are summarized in Fig. 4.21. As expected, the FSCL implementation is the fastest with a slight speed advantage over DSLL and up to 27% and 75% speed advantage over static CMOS and CVSL respectively. The carry propagation delays per bit closely follow the average delays for the full adder cell described in Section 4.6.

In Fig. 4.22, the average power dissipation at maximum frequency is plotted for the different logic structures. FSCL has the highest power dissipation due to the large static current flow of 3.6 mA for the entire 8-bit CRA. The noise performance is compared in Fig. 4.23. The static CMOS, CVSL and DSLL implementations show power supply cur rent spikes that are more than two orders of magnitude higher than in the FSCL CRA.

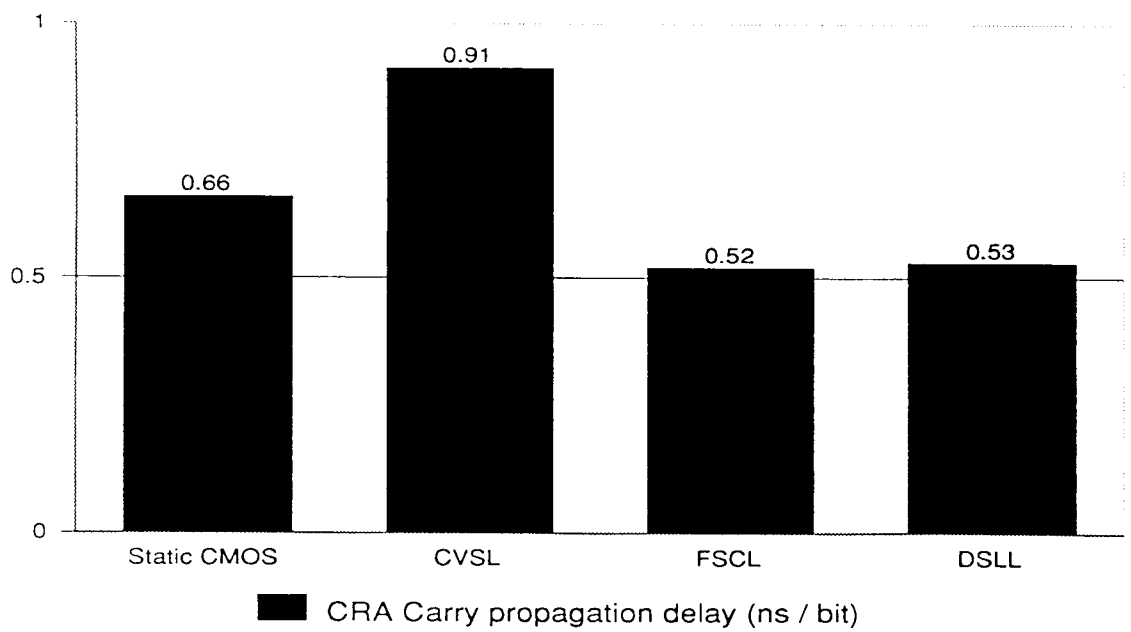

Fig. 4.21 CRA Delay comparison for different logic structures

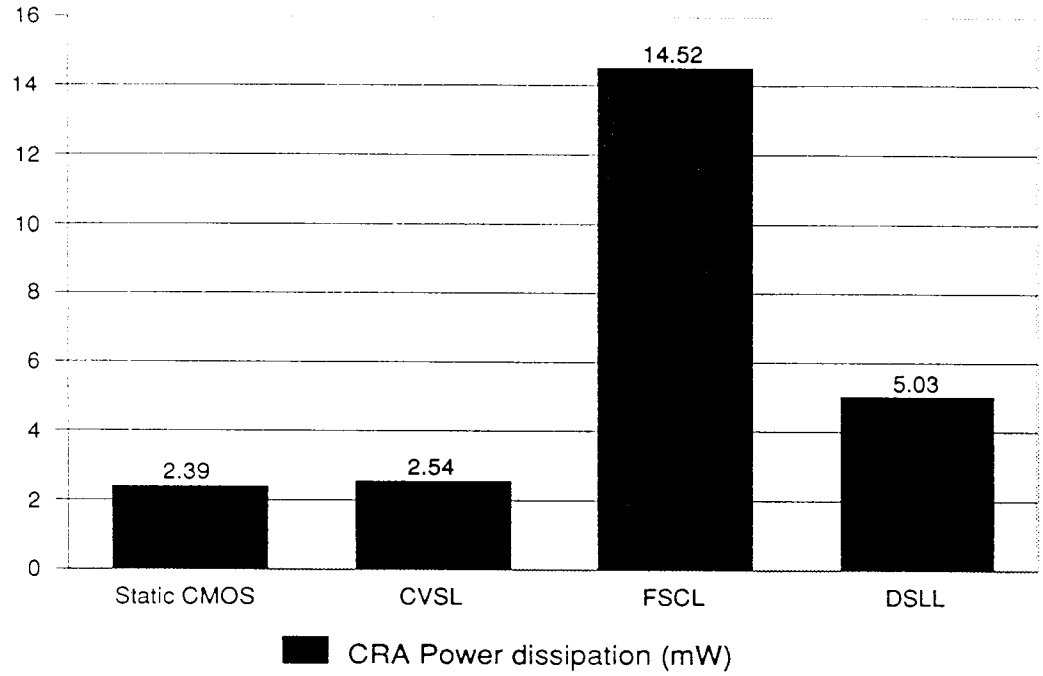

Fig. 4.22 CRA Power comparison for different logic structures

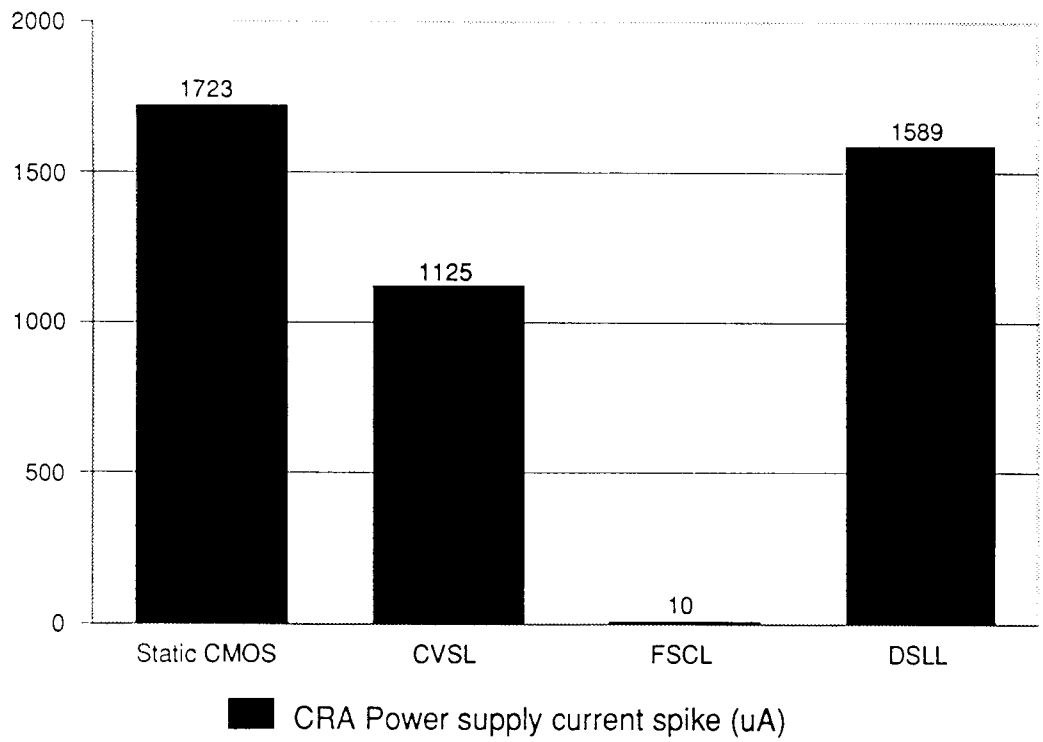

Fig. 4.23 CRA Power supply noise generation

4.8 Carry-Skip Adder

The carry-skip adder (CSA) uses a simple and area efficient way to speed up the carry propagation. An 8-bit CSA was constructed with 2 sections of 4 bits each. Each section was a 4-bit carry-ripple adder with the first section having a carry bypass circuit as illustrated in Fig. 4.24. The carry generated by the carry bypass circuit is obtained as follows:

$$P_i = A_i + B_i$$

$$G_i = A_i \cdot B_i$$

$$C_4 = G_4 + P_4G_3 + P_4P_3G_2 + P_4P_3P_2G_1 + P_4P_3P_2P_1C_0 \qquad (4.21)$$

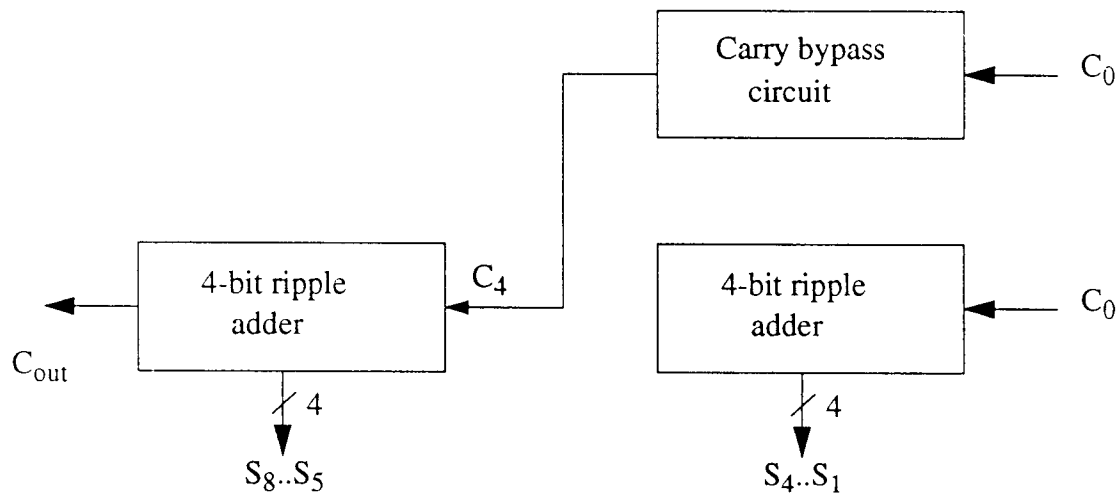

Fig. 4.24 Block diagram of a 4-bit section carry-skip adder

The simulation results obtained for the CSA are shown in Figs. 4.25-4.27. The delay comparison (Fig. 4.25) shows that, again, the FSCL implementation is the fastest with a delay per bit of only 0.24 ns. DSLL exhibits the next smallest delay and static CMOS is 108% slower than FSCL. Fig. 4.26 summarizes the power dissipation. The high static power loss in FSCL gates leads to an overall power dissipation approximately 4 times that in DSLL and 9 times that observed in static CMOS and CVSL logic structures. The power supply current spike comparison in Fig. 4.27 again proves that

FSCL is the logic of choice in mixed-mode systems, generating on average 75 times lower magnitude of switching noise spikes.

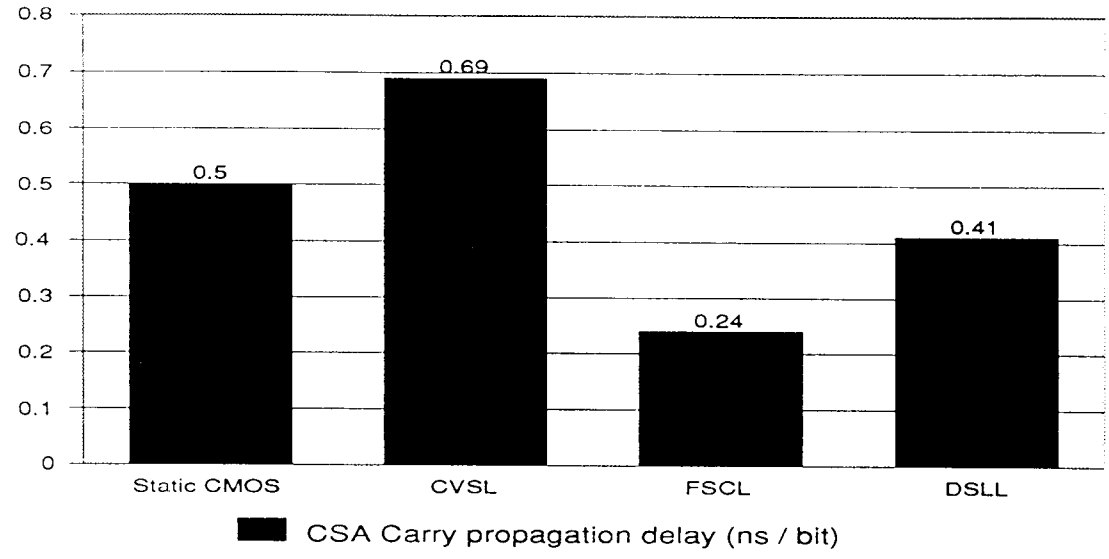

Fig. 4.25 CSA Delay comparison for different logic structures

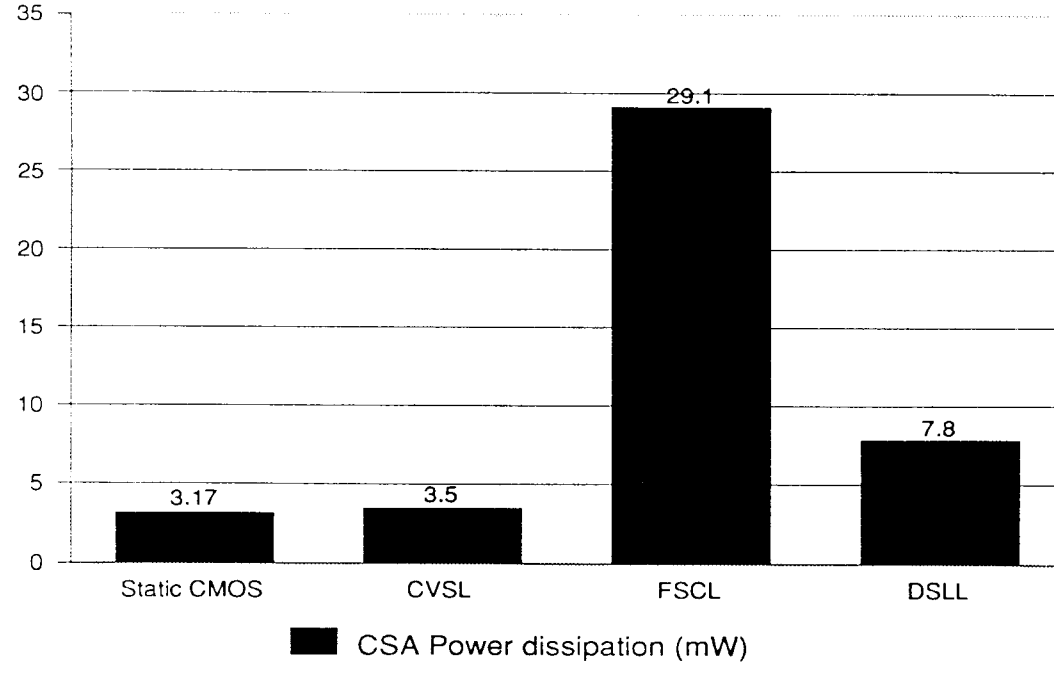

Fig. 4.26 CSA Power comparison for different logic structures

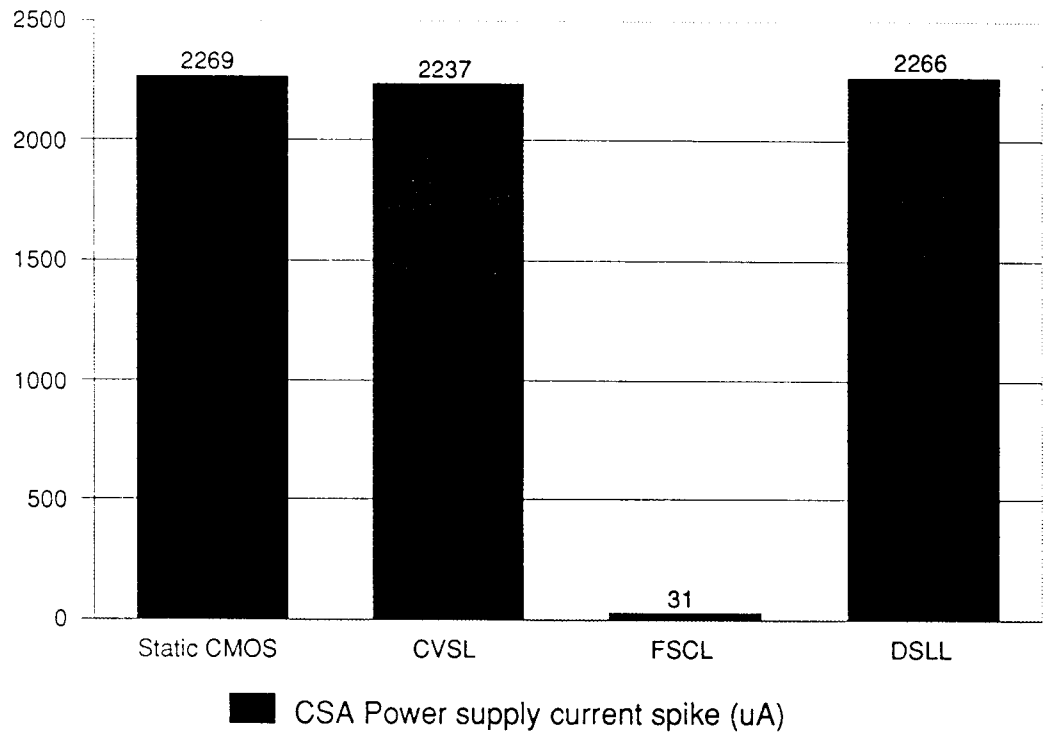

Fig. 4.27 CSA Power supply noise generation

4.9 Carry-Lookahead Adder

The carry-lookahead adder (CLA) is the fastest way to implement the addition of two binary numbers. However, the CLA is very area inefficient due to long and irregular interconnections. An 8-bit CLA was implemented with the different logic structures, with the carry-lookahead circuit obtained as follows[11]:

$$C_1 = G_1 + P_1 C_0$$

$$C_2 = G_2 + P_2 C_1 = G_2 + P_2 (G_1 + P_1 C_0)$$

$$C_n = G_n + P_n G_{n-1} + \ldots + P_n P_{n-1} P_{n-2} G_{n-3} + \ldots + P_n P_{n-1} \ldots P_2 P_1 C_0 \quad (4.22)$$

The carry functions were generated with two-input OR and AND gates for maximum speed. The delay obtained for the FSCL CLA was 1.80 ns, which is 0.23 ns per bit. As

compared to the FSCL CSA (0.24 ns per bit), the speed advantage is insignificant and does not justify the increased complexity and area of the CLA. Comparison with other logic structures is shown in Fig. 4.28.

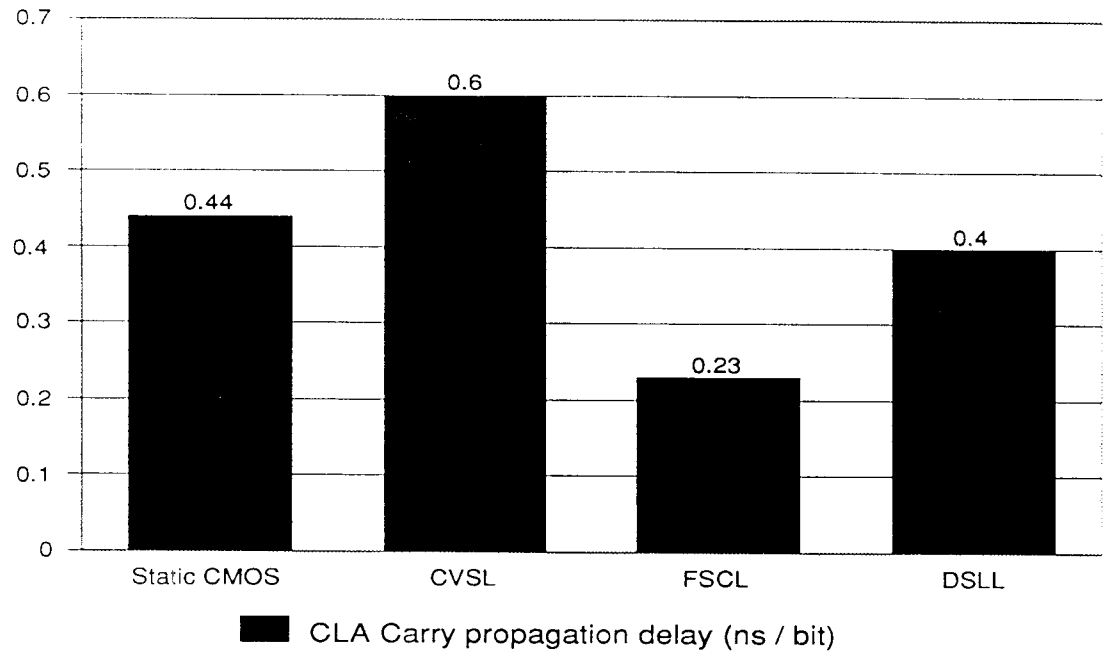

Fig. 4.28 CLA Delay comparison for different logic structures

The power dissipated is summarized in Fig. 4.29. FSCL dissipates 3.6 times more power than DSLL and approximately 12 times more power than CVSL and static CMOS. As was the case in the CRA and CSA, the power supply current spike magnitude (Fig. 4.30) in the CLA is 100-200 times lower in FSCL as compared to the other logic structures.

The normalized areas of the CRA, CSA and CLA are plotted in Fig. 4.31. The CVSL implementation of the CRA has the smallest area and is assigned a normalized area of 1.0. For each of the adders, the FSCL implementation occupies the most die area, about 3.2 times more area than CVSL and 2 times the area of the static CMOS implementation.

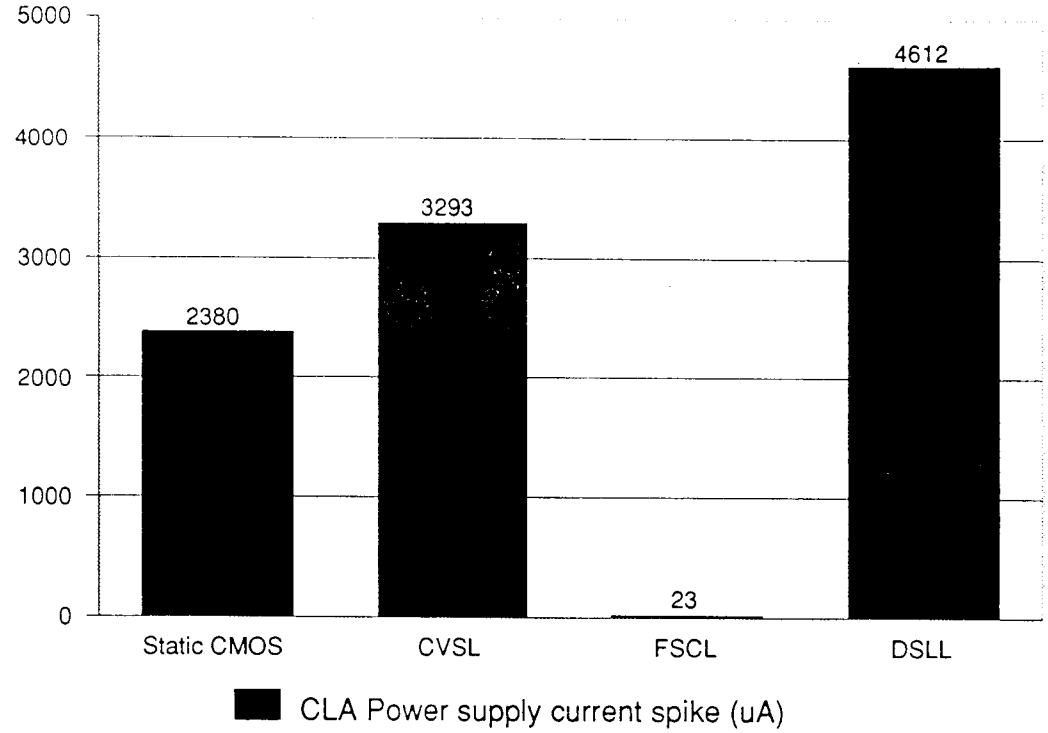

Fig. 4.29 CLA Power comparison for different logic structures

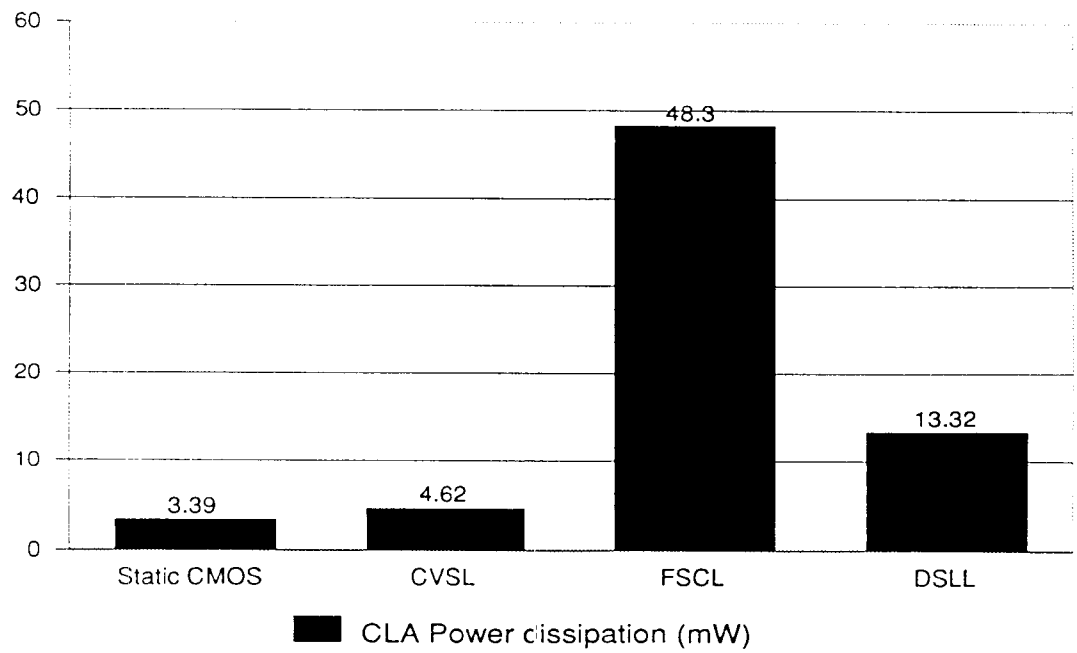

Fig. 4.30 CSA Power supply noise generation

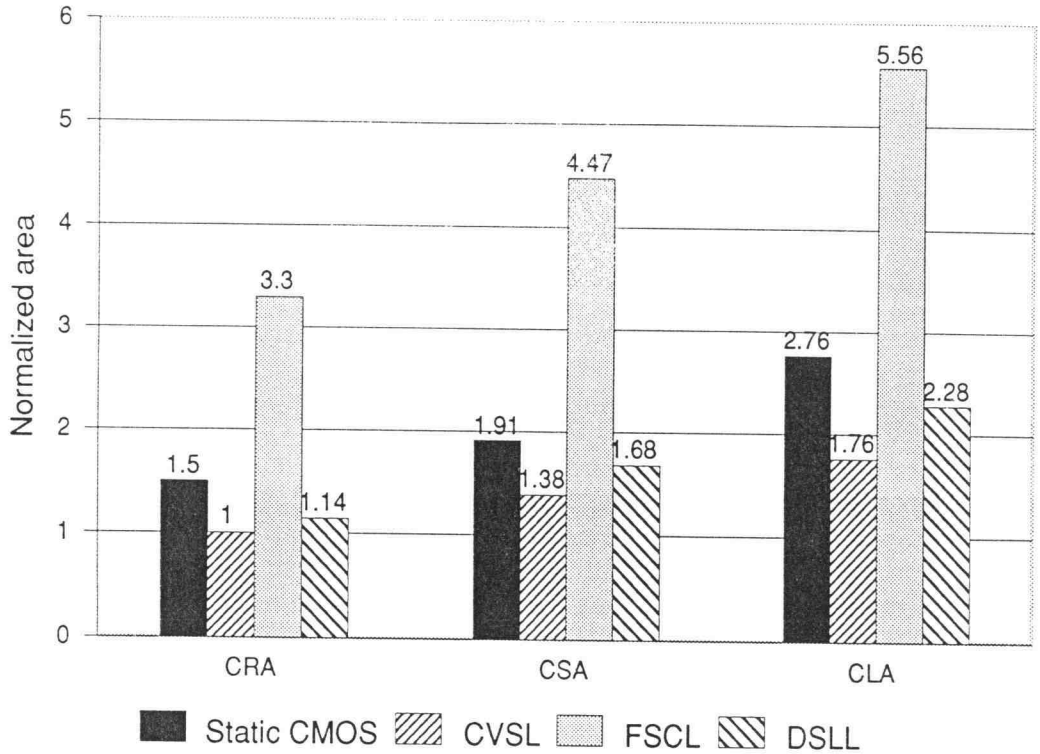

Fig. 4.31 Area comparison of different logic structures

In conclusion, FSCL logic is suitable for high-speed low-noise mixed-mode integrated circuits. The disadvantages of complex FSCL circuits are high power dissipation and increased die area compared to other logic structures. However, the speed can be traded for reduced power dissipation by using 3-input gates wherever possible. Since each gate has the same static power loss, the reduced number of 3-input gates required will mean a lower system power loss.

5. Conclusion and Future Research

The FSCL inverter is analyzed in terms of the noise margin, delay and voltage and current scaling. A set of constraints are developed for selecting the values of α, β and I_1 in the design of a FSCL gate. The minimum sized FSCL inverter is shown to have noise margins NM_H and NM_L of the order of 10% and 5% respectively. The FSCL gate has a trade-off between power consumption and gate area at a constant gate delay. The power consumption is reduced by 20% when transistor sizes are increased by a factor of 5 for the case of parasitic capacitances equal to gate capacitance.

The effect of voltage and device scaling on the average delay, power dissipation at maximum frequency and power-delay-product for FSCL, static CMOS, CVSL and DSLL inverters is summarized in Tables 5.1 and 5.2.

Table 5.1: Voltage scaling

	FSCL	Static CMOS, CVSL, DSLL	
		Small C_L	Large C_L
Delay	*const*	$V^{-1.5}$	V^{-1}
Power	V	V^3	V^3
PDP	V	$V^{1.5}$	V^2

The power supply current spike noise is one and one-half orders of magnitude lower in FSCL than in other topologies at no load capacitance and is 2 orders of magnitude less at 0.5 pF load capacitance.

The FSCL full-adder gate has a carry propagation delay of only 0.56 ns compared to 0.70 ns for a static CMOS adder. The full-adder gate is used to implement a carry-ripple adder, carry-skip adder and carry-lookahead adder. The FSCL topology has the smallest carry delay per bit for each type of adder and lowest noise. However, the

Table 5.2: Device scaling

	Device size	FSCL, Static CMOS, CVSL, DSLL	
		Small C_L	Large C_L
Delay	$K \geq 1$	*const*	K^{-1}
	$K < 1$	K^{-2}	K^{-1}
Power	all K	K	K
PDP	$K \geq 1$	K	*const*
	$K < 1$	K^{-1}	*const*

FSCL adders show highest power dissipation and maximum die area. The CVSL topology occupies minimum area and the FSCL adders are on average 3.3 times more expensive in terms of silicon area.

For future research, the following improvements are suggested. The simple current mirrors in the FSCL gate can be replaced by cascode current mirrors. This will yield even lower power supply current spikes leading to use in very accurate and "quiet" mixed-mode applications. Also the high power dissipation can be reduced by turning off the current sources in-between logic operations. This can be done in an asynchronous manner to spread out the resulting noise. Thus in a carry-ripple adder, each block can turn off after performing its computation.

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