AN ABSTRACT OF THE THESIS OF

Jenna Y. Gorecki for the degree of Master of Science in Chemical Engineering presented on June 1, 2016.

Title: Low-temperature, Inkjet-printed p-Type Copper(I) Iodide-based Thin-Film Transistors.

Abstract approved: ____

Chih-Hung Chang

Inkjet-printed p-type copper(I) iodide-based TFTs were successfully fabricated. As-printed copper(I) halide semiconductor films, such as CuI, CuBrI, and CuClI, were used as p-type active channel layers for TFTs. The entire process of the TFTs fabrication was maintained under 150 °C, which is compatible with flexible plastic substrates and transparent glass substrate. Various printing temperatures, drop spacing, W/L ratios, and TFT structures were tested in order to find the optimum device properties for p-type copper(I) iodide-based TFT. In addition, inkjet-printed CuI, CuBrI, and CuClI films were characterized to study optical, electrical, and morphological properties. Furthermore, device performance of printed copper(I) iodide-based p-type TFTs was also investigated. Among them, CuI TFTs with SU-8 encapsulation exhibited outstanding p-type transistor behaviours with field-effect mobility as high as 4.36 $cm^2\ V^{-1}\ s^{-1}$ and I_{on}/I_{off} ratio of $10^{3.24}$ on the silicon substrate. Also, CuBrI TFTs resulted in successful p-type transistor behaviours with average

field-effect mobility of 2.4 $cm^2\ V^{-1}\ s^{-1}$ and I_{on}/I_{off} ratio of $10^{1.9}$ on the glass substrates when the molar ratio of CuBr:CuI was 1:1. In addition, CuClI TFTs were successfully fabricated with field-effect mobility as high as 1.02 $cm^2\ V^{-1}\ s^{-1}$ and I_{on}/I_{off} ratio of $10^{0.73}$ on the silicon substrates when the molar ratio of CuCl:CuI was 1:9. The device performances were comparable to reported p-type metal oxide TFTs. This study suggests promising candidates of low-temperature printed p-type TFTs that can be used for complementary inorganic circuits.

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Low-temperature, Inkjet-printed p-Type Copper(I) Iodide-based Thin-Film Transistors

by
Jenna Y. Gorecki

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APPROVED:

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Head of the School of Chemical, Biological, and Environmental Engineering

Dean of the Graduate School

I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Jenna Y. Gorecki, Author

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1. Introduction

1.1 Metal Oxide Thin-Film Transistors

In recent years, metal based oxide thin-film transistors (TFTs) have attracted increasing attention as a promising candidate to replace the conventional amorphous hydrogenated silicon (a-Si:H) TFTs due to their superior properties such as higher mobility and lower off-state current. [1], [2] Although low electronic properties of a-Si:H semiconductor (carrier mobility < 1 cm^2/Vs) were sufficient for Liquid Crystal Displays application, the switching elements for Active-Matrix Organic Light-Emitting Diode (AMOLED) require higher electronic properties, which a-Si:H semiconductor cannot achieve. Metal oxide semiconductors and low-temperature polycrystalline Si (poly-Si) have been extensively studied recently in order to replace a-Si:H for AMOLED display application. Although poly-Si TFTs can achieve high mobility and on/off ratio, they have device uniformity issues due to the grain boundaries in the film. Amorphous metal oxide semiconductors have novel and uniform device performances (carrier mobility ~ 1-100 cm^2/Vs) due to the lack of grain boundaries, unlike in the poly-Si TFTs. [1] Various oxide semiconducting materials from binary (ZnO, In_2O_3, SnO_2) to quaternary (IGZO, IZTO) oxide compounds have been researched for the TFTs application. [3]–[5] However, most of the reported oxide TFTs have been mainly focused on n-type semiconductors and only a few studies have been reported about p-type oxide semiconductors TFTs. Since all-oxide electronics will enable high charge carrier mobility with low-cost and scalable processes, developing p-type oxide semiconductors is still necessary. Therefore, finding the p-type semiconductor candidates, which have high electronic properties comparable to n-type counterparts, would be a crucial step for entering the next generation of electronics applications.

1.2 Solution-processed p-Type TFTs

Recently, solution-processed fabrication of TFTs, which enables a simple and low-cost fabrication, has extensively been introduced as a promising alternating method to conventional vacuum processes. Printing technology is one of the most promising solution-based techniques that facilitates a direct writing of materials, reduction of chemical waste, and good reproducibility with a high-resolution scale.[6] Since Lee et al. [7] reported the low-cost and general way of fabricating solution-processed metal oxide semiconductors, extensive research has been conducted on manufacturing solution-processed metal oxide TFTs. In addition, developing solution-fabricated p-type semiconductors that have comparable properties as their n-type counterparts will enable the development of complementary metal-oxide-semiconductor circuits as well as p-n diodes via flexible and controllable solution-based manufacturing processes. [8]–[10] P-type organic semiconducting materials have been studied for a long time but they have limitations due to low mobility and their instability in ambient air.[10] Also, SnO and Cu_2O have been studied extensively as p-type channel layers of TFTs mainly by vacuum-processed fabrications. Yao et al. [11] reported p-type Cu_2O TFTs on flexible polyethylene terephthalate substrate with field effect mobility of ~2.40 cm^2 V^{-1} s^{-1} and on/off ratio of ~3.96×10^4 by magnetron sputtering at room temperature. Al-Jawhari et al. [12] reported Cu_2O/SnO bilayer p-type TFTs. The SnO film was sputtered as an active channel layer and the Cu_2O film was sputtered as a capping layer onto the tin oxide layer. The optimum bilayer TFT was fabricated with 10 nm of Cu_2O and 15 nm of SnO with the field effect mobility of ~0.66 $cm^2\ V^{-1}\ s^{-1}$ and on/off ratio of ~1.5×10^2. In addition, solution-processed p-type metal oxide TFTs have also been reported several times. Kim et al. [8] reported sol-gel spin coated cuprous oxide (Cu_2O) TFTs with field effect mobility of 0.16 $cm^2\ V^{-1}\ s^{-1}$ and on/off ratio of ~10^2. Also, Pattanasattayavong et al. [9] reported spray pyrolysis fabricated Cu_2O TFTs with field effect mobility of 10^{-4} - 10^{-2} $cm^2\ V^{-1}\ s^{-1}$ and on/off ratio of 4×10^3. Despite the recent extensive research on p-type oxide TFTs, the field-effect mobility is still not satisfactory.

1.3 Solution-processed Copper(I) Iodide-based TFTs

Copper(I) halides (CuI, CuBr, and CuCl) have been studied as good candidates for p-type semiconductors especially in solar cell applications. [13] While CuI, CuBr, and CuCl have three different crystalline phases, α, β, and γ, γ-copper(I) halides semiconductor exhibit p-type characteristics. The copper halide film has several advantages as an active channel layer for p-type TFTs, such as high transparency in the visible wavelengths (Eg ~ 2.9 – 3.4 eV) and a simple film preparation method.[13] Also, due to their intrinsic p-type semiconductor properties, copper(I) iodide-based TFTs do not require an oxidation step, which means no annealing step is needed. Therefore, fabricating TFTs with copper(I) halide channel layer enables the overall process temperature to be reduced significantly; the entire process of the TFTs fabrication is maintained under 150 °C in this research. Considering low-temperature low-cost solution-processes have the potential to be a mainstream fabricating method which will replace conventional high-cost vacuum processes, Copper(I) halides are the ideal p-type semiconductor candidates for future electronics applications. In this work, we demonstrate solution-processed Copper(I) Iodide-based p-type TFTs for the first time.

2. Literature Review

2.1 Vacuum-processed p-type TFTs

Most of reported p-type oxide TFTs were mainly fabricated by vacuum-based techniques, such as radio-frequency (RF) magnetron sputtering and pulsed laser deposition. [14], [15] While most of reported Cu_2O TFTs deposited by vacuum-processed techniques showed low hole mobility (< 1 cm^2 V^{-1} s^{-1}) and on/off ratio, most of vacuum-processed SnO TFTs showed closer or above 1 cm^2 V^{-1} s^{-1}, which indicated that SnO could be more promising than Cu_2O for p-type TFT application. [16]

2.1.1 SnO TFTs

There has been a lot of efforts to control the stoichiometry of metal to oxide ratio for metal oxide semiconductor. Several studies reported that optimizing the annealing conditions, such as oxygen partial pressure or annealing time, was crucial to deposit continuous and pure p-type SnO semiconductor layer.

Fortunato et al. [17] showed the effect of oxygen partial pressure (O_{pp}) during annealing on forming p-type SnO film. It was found that metallic β-Sn was the dominate phase at $O_{pp} < 5\%$, and p-type polycrystalline film with α-SnO_x and β-Sn were formed when $5\% < O_{pp} < 15\%$. Also, n-type SnO_2 film was formed when $O_{pp} >$ 15%. They successfully fabricated SnO_x (x<2) TFTs with the field-effect mobility (μ_{FE}) of 1.1-1.2 cm^2 V^{-1} s^{-1} and on/off ratio (I_{on}/I_{off}) of 10^3. The film was deposited by RF magnetron sputtering at room temperature (RT) and annealed at 200 °C for 1 hr with 0.2 Pa of Ar and O_2.

Zhong et al. [18] investigated the crystalline structure and composition of the channel layer film while varying oxygen annealing time in order to find an optimized annealing condition. The channel layer was deposited by sputtering at RT and post-annealed at 300 °C with oxygen pressure of 0.3 Torr. While as-deposited film showed n-type Sn-dominated film with high electron concentration, the 30 min annealed film showed p-type characteristics, and the drain current was further improved for 45 min annealed film. Also, they found that the amorphous as-deposited film changed to polycrystalline film after annealing for 30 min. They fabricated p-type SnO TFTs with the μ_{FE} of 3.24 $cm^2\ V^{-1}\ s^{-1}$ and I_{on}/I_{off} larger than 10^3.

In addition, Cu_2O/SnO bilayer p-type TFTs was reported by Al-Jawhari et al.[12]. SnO film was sputtered as an active channel layer, and Cu_2O film was sputtered as a capping layer onto the tin oxide layer. It was suggested that the Cu_2O capping layer improved the electrical properties of the TFT by reducing the surface leakage current as well as enhancing the oxidation of SnO layer. While the oxygen partial pressure (O_{pp}) during deposition of Cu_2O kept as 10 %, the O_{pp} of SnO deposition varied to find the optimum condition for TFT application. As shown in Figure 3, the bilayer device exhibited n-type at high O_{pp} of SnO, when O_{pp} was 5 % and 9 %, since the extra oxygen from Cu_2O layer influenced the transformation of SnO to Sn_2O. In addition, 3% of O_{pp} of SnO was required to achieve p-type transistor behaviour. Also, TFT device with 0% of O_{pp} of SnO was found to have no TFT functionality, since the oxygen delivered from Cu_2O capping layer was not enough to convert Sn to SnO film. The optimum bilayer TFT was fabricated with 10 nm of

Cu_2O (10% O_{pp}) and 15 nm of SnO (3 % O_{pp}) with the μ_{FE} of ~0.66 $cm^2\ V^{-1}\ s^{-1}$ and I_{on}/I_{off} of ~1.5×10^2.

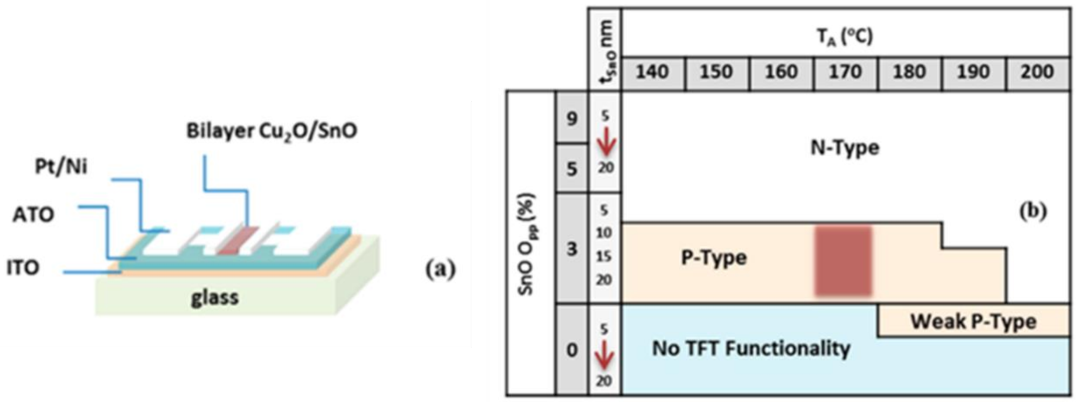

Figure 1. (a) Schematic diagram of Cu2O/SnO bilayer TFT and (b) the TFT polarity obtained under different oxygen partial pressures (Opp) and annealing temperatures. (Reproduced from [12]).

2.1.2 Cu_2O TFTs

Yao et al. [11] demonstrated that the growth temperature affected the microstructure and electrical transport properties of Cu_2O films by changing the sputtering temperature from RT to 500 °C. They found that the Cu_2O film that was sputtered at RT had good electrical performance. They achieved superior transfer performance of p-type Cu_2O TFTs on flexible polyethylene terephthalate (PET) substrate with μ_{FE} of ~2.40 $cm^2\ V^{-1}\ s^{-1}$ and I_{on}/I_{off} of ~3.96×10^4 by magnetron sputtering at RT without post-annealing.

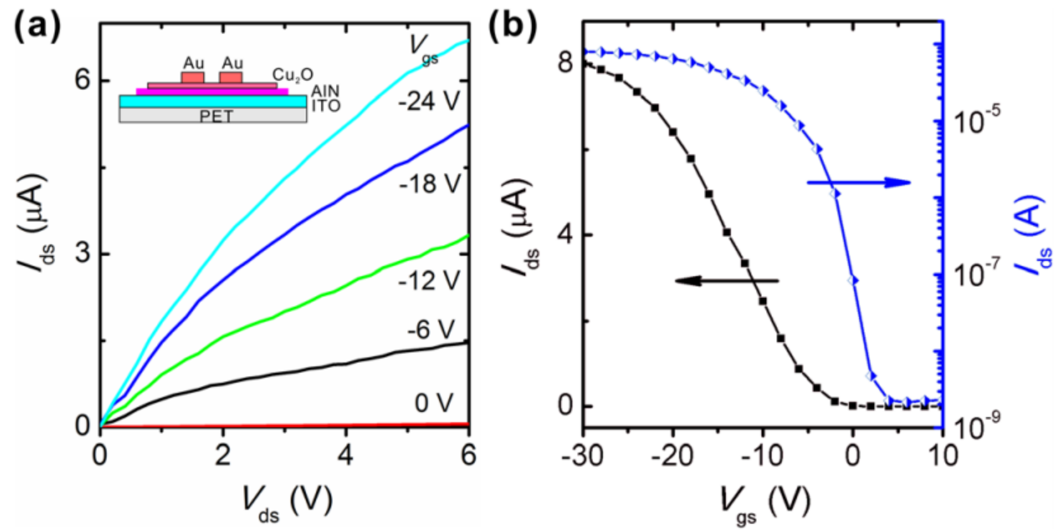

Figure 2. (a) Drain current-drain voltage (Ids-Vds) characteristics of p-type Cu2O TFT grown on PET. (b) Ids-Vgs plots of the same device at a fixed Vds of þ5 V. Inset in (a) shows the schematic device structure of the Cu2O TFTs. (Adapted from [11])

Figueiredo et al.[19] investigated the impact of sputtering O_{pp} on forming Cu_xO film. They deposited Cu_xO film by RF magnetron sputtering, while varying the O_{pp} from 0% to 100%. They showed that a metallic Cu film was formed at O_{pp} was 0%, and was transformed to Cu_2O phase when O_{pp} was 9%. Also, CuO phase was formed when O_{pp} was 25% and 50%. They fabricated p-type TFT with Cu_xO film, deposited when O_{pp} was 9%, had μ_{FE} of $7x10^{-3}$ cm^2 V^{-1} s^{-1} and I_{on}/I_{off} of 10^3.

Nam et al. [20] demonstrated that the device performance of Cu_2O TFTs was substantially affected by the active layer thickness. They varied the film thickness from 15nm to 155 nm in order to investigate optical, structural, and electrical properties of the TFTs. They concluded that 45 nm was optimum film thickness since the device exhibited the cleanest transfer function with small subthreshold slope.

2.2 Solution-processed p-type TFTs

Significant progress of device performance of solution-based p-type oxide TFTs has been made recently, some of which are comparable with the vacuum-based p-type oxide TFTs performance. The solution-processed technique enables simple and low cost fabrication and it has a potential to replace the conventional vacuum-processed fabrication.

2.2.1 Cu_2O TFTs

Kim et al. [8] successfully fabricated sol-gel spin coated cuprous oxide (Cu_2O) TFTs with Cu(II) acetate as a metal cation precursor. As-coated film went through two-step annealing process, first N_2 annealing at 400 °C for 30 minutes and then O_2 annealing at 700 °C for 30 minutes, in order to improve the morphology of the film. N_2 annealing before the oxidation step helped to improve the uniformity and continuity of the film, which is favourable as a channel layer of TFT application. Also, they showed that the TFT performance was also affected by the oxygen partial pressure (O_{pp}) in the second step of annealing. While uniform Cu_2O thin film was formed under low oxygen partial pressure (O_{pp} = 0.04 - 0.2 Torr), CuO as well as Cu_2O were formed as a rough film with many voids at higher oxygen partial pressure (O_{pp} = 0.9 Torr). They fabricated p-type Cu_2O TFT with μ_{FE} of 0.16 cm^2 V^{-1} s^{-1} and I_{on}/I_{off} of ~10^2 of which annealed at O_{pp} of 0.04.

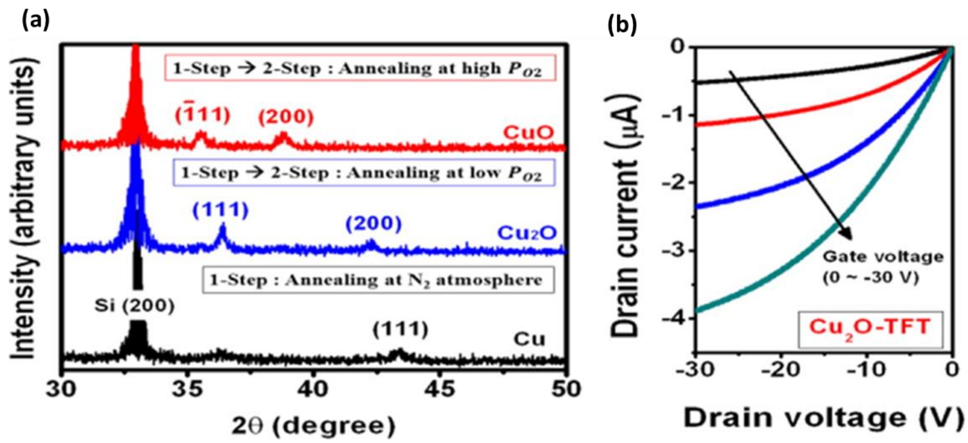

Figure 3. (a) XRD spectra of copper oxide films as-annealed in N2 atmosphere and two-step annealed under high and low oxygen partial pressures. (b) Output characteristics of copper oxide TFTs annealed at Opp of 0.04 Torr (Adapted from [8]).

Yu et al. [21] fabricated spin-coated Cu_2O TFTs with one-step vacuum annealing, in order to effectively transform CuO into Cu_2O. They tested different annealing temperature from 400 °C to 700 °C. It was found that the grain size and surface roughness of the films increased as annealing temperature increased. They found that 600 °C is the optimum annealing temperature for TFT application. They reported the device performance of the spin-coated Cu_2O TFTs as μ_{FE} of 0.29 cm^2 V^{-1} s^{-1} and I_{on}/I_{off} of 1.6×10^4.

2.2.2 CuO TFTs

Jang et al. [22] fabricated solution-processed p-type CuO TFTs as well as Cu2O TFTs using a sol-gel route. They deposited copper (II) acetate precursor by sol-gel route and sintered at various temperature from 200-500 °C. It was found that Cu was formed when sintered at 200 and 300 °C, while mixture of Cu, Cu_2O, and CuO were formed at 400 °C. Pure CuO film was formed when sintered at 500 °C for more than 30 minutes. The author successfully fabricated p-type Cu2O TFTs, after sintering at 200 C for 4hr, as well as p-type CuO TFTs, sintering at 400C for 1hr. The resulting p-type CuO and Cu_2O TFTs exhibited μ_{FE} of 0.01 $cm^2\ V^{-1}\ s^{-1}$ and $2x10^{-3}$ $cm^2\ V^{-1}\ s^{-1}$ respectively, and I_{on}/I_{off} of ~10^3.

2.2.3 SnO TFTs

Okamura et al. [23] fabricated spin-coated SnO TFTs which achieved μ_{FE} of 0.13 $cm^2\ V^{-1}\ s^{-1}$ and I_{on}/I_{off} of $10^{1.9}$. They tested various precursor ($SnCl_2 \cdot 2H_2O$ in methanol) concentration from 0.05-0.5 M and various post-annealing conditions from 200-600 °C in order to find the optimum condition. It was found that SnO crystallites monotonically grew in the temperature range of 300-450 °C, while SnO began to decompose into Sn and SnO_2 at 500 °C, and completely decomposed at 600 °C. It was found that precursor concentration of 0.1 M and post-annealing temperature of 450 °C were the optimum condition for fabricating transistors that demonstrated superior performance.

2.2.4 PbS TFTs

Carrillo-Castillo et al. [24] fabricated PbS TFTs by chemical bath deposition. While as-deposited TFT showed channel mobility of ~0.09 cm^2/Vs, the mobility for devices annealed at 150 °C increased to ~0.14 cm^2/Vs.

3. Materials and Method

3.1 Materials

SiO_2/Si substrates were used to fabricate Copper(I) Iodide-based TFTs. The substrate has a gold (Au) layer of 100 nm thickness as a contact layer sputtered on silicon substrate. SiO_2 layer of 100nm thickness was thermally grown on the other side of silicon substrate as a dielectric layer. All of the substrates were treated using oxygen plasma cleaning prior to the deposition. Copper(I) iodide (γ-CuI, anhydrous, 99.995%), copper(I) bromide (99.999%, Metal basis), and copper(I) chloride (>=99.995%) were purchased from Sigma-Aldrich. A solvent of acetonitrile (HPLC>99.9%) was purchased from Fisher Scientific. Also, SU-8 was purchased from Micro Chem. 0.05 M CuI, 0.05M Cu(Br, I) (with various molar ratio of CuBr : CuI), and 0.05M Cu(Cl, I) (with various molar ratio of CuCl : CuI) solutions were sonicated for 30 min and filtered with syringe filter (Nonsterile, PTFE 25mm x 0.20um) purchased from VWR. The resulting precursor solution served as a printing ink without any additives. As-printed CuI, Cu(Br, I), and Cu(Cl, I) films were dried at 120 °C for 30 minutes and SU-8 was applied on it in order to prevent moisture from reacting with the channel layer.

3.2 Film Fabrication by Inkjet Printer

Piezoelectric inkjet printer (Dimatix DMP-2831, Fujifilm) was used to manufacture the CuI, Cu(Br, I), and Cu(Cl, I) films. The dimension of the printed film was controlled by software installed in the printer. The CuI, Cu(Br, I), and Cu(Cl, I) films were printed on SiO_2/Si substrates, which was oxygen plasma treated enabling the surface to be hydrophilic. The temperature of substrates while printing varied from RT, 30 °C, 40 °C, 50 °C, to 60 °C in order to investigate the optimized condition. As-printed film was placed on a hot plate set to 120 °C for 30 minutes, allowing solvent to evaporate. The as-printed films were able to be converted into dense and uniform films after simply drying at 120 °C. A gold layer of 50 nm thickness then was deposited as source and drain by thermal evaporator using a shadow mask for patterning. The active channel layer was defined as 1000 µm and 200 µm for width and length, respectively (Figure 4b). All investigated TFTs are fabricated in the described bottom gate bottom contact structure (Figure 4a). After depositing source and drain, the device was placed on a hot plate at 150 °C for 30 minutes in order to get rid of moisture that might have remained in the CuI, Cu(Br, I), and Cu(Cl, I) films. Then, SU-8 was applied on the printed CuI, Cu(Br, I), and Cu(Cl, I) area as an encapsulation layer in order to prevent moisture and impurities from contacting the channel layer, which helps to improves device performance.

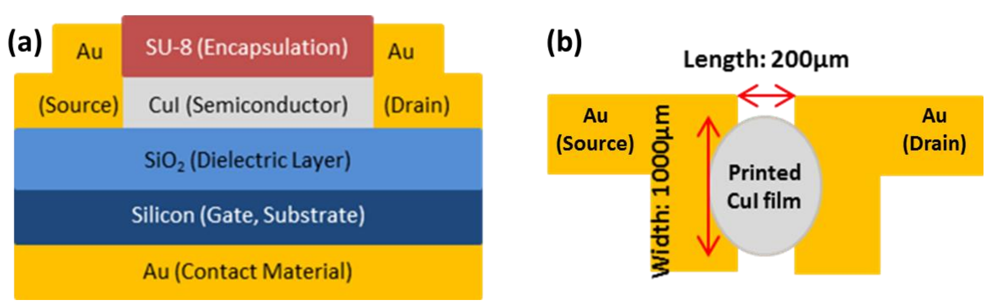

Figure 4. (a) The schematic diagram of CuI TFT on the SiO2/Si substrate, (b) The scaled schematic diagram of printed CuI film with gold source/drain conductors. The width and length of channel layer of CuI TFT are 1000 µm and 200 µm, respectively.

3.3 Characterization

Optical, electrical, and morphological properties of CuI films were investigated. The cross-sectional morphology of the CuI films was characterized by scanning electron microscopy (SEM, FEI Helios 650). Atomic force microscope (AFM, Veeco Nanoscope digital instruments) was employed to analyze the surface morphology and roughness of the films. The films were characterized by X-ray diffraction (XRD, Bruker D8 discover) to investigate the crystalline structure. The optical properties of the films were studied using UV-vis spectroscopy (Jasco, V-670 Spectrophotometer). For the transmittance measurement, CuI film was deposited on bare soda lime glass substrate. Device properties of TFTs, such as output characteristics (I_D-V_D), mobility, and transfer characteristics (I_D-V_G, on/off ratios), of encapsulated CuI TFTs were measured using an Agilent Technologies E5270B Semiconductor Parameter Analyzer under ambient conditions.

4. Results and Discussion: Copper(I) Iodide TFTs

4.1 Characterization of CuI film

Inkjet-printed CuI film on SiO_2/Si substrate was characterized by AFM, SEM, and XRD (Figures 5, 6, and 8). Electrical properties of the films were studied by using Hall Effect measurement (Table 1). CuI solution was also spin-coated on a soda lime glass substrate for analyzing band gap (Figure 7).

4.1.1 Morphology of CuI film

CuI film was printed on a SiO_2/Si at RT (~21°C), 30 °C, 40 °C, 50 °C, and 60 °C; while the temperature of the CuI ink in the cartridge was kept at RT. The AFM images (Figure 5) showed different CuI forming at various temperatures of substrates.

Printed CuI film at RT showed uniformly distributed small grains of ~20 nm with nano-holes, which traps charge carriers resulting degrading the performance of transistors when applied as a channel layer (Figure 5a). In order to reduce the voids in the film, various printing temperatures were tested. When the film printed at 30 °C, partial coffee-ring pattern was formed while increasing the size of voids drastically, leading to form discontinuous film (Figure 5b). As the printing temperature increased to 40 °C, the size of the voids decreased, and the film became more continuous while forming the network of coffee-ring pattern (Figure 5c). It was inferred that Marangoni flow, which moved the interior particles toward to edge of the film, induced to form coffee ring pattern when the printing temperature was between RT and 40 °C. As printing temperature increased to 50 °C, the film became denser with a few cracks and voids (Figure 5d). Finally, the CuI film that was deposited at 60 °C had the densest and most continuous film without any voids (Figure 5e). It was inferred that when the printing temperature was higher than 50 °C, the fast evaporation helped to form crystallization faster while overcoming Marangoni flow effect. It was found that dense and continuous film with larger grains were formed at printing temperature between 50 °C and 60 °C. The printing temperature higher than 60 °C were not tested due to the limitation of the printer capacity; however, the thicker film is expected to be form at higher temperature which is not desirable for TFT application.

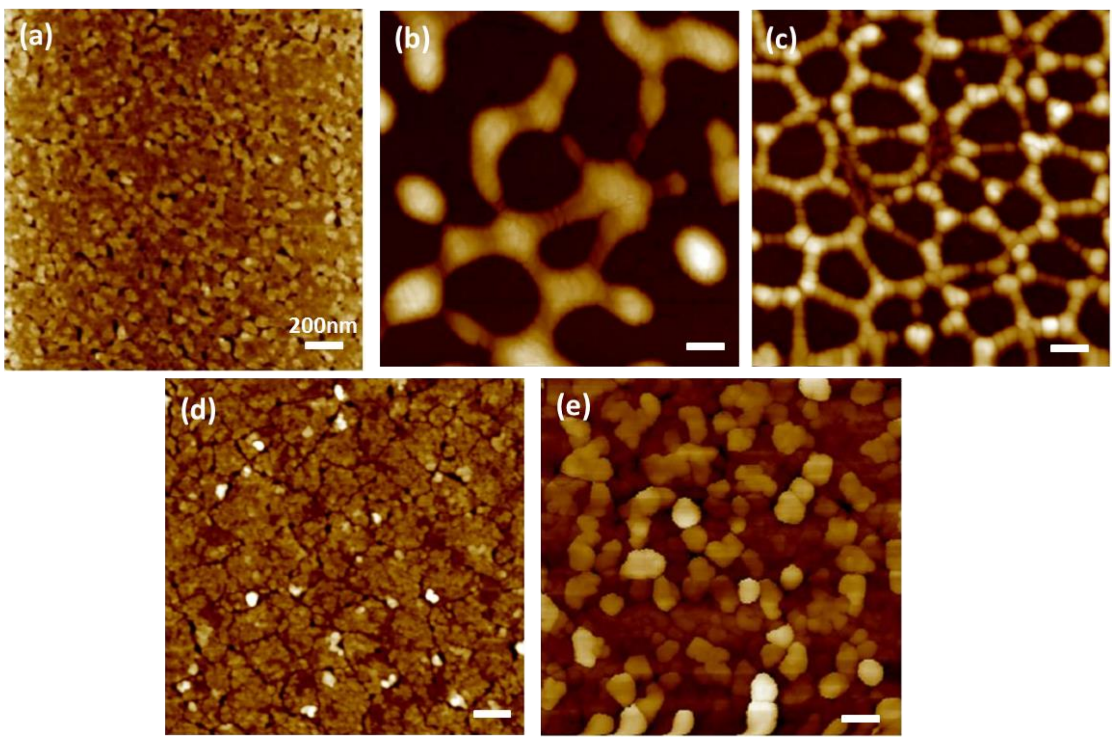

Figure 5. AFM images of the printed CuI films on SiO_2/Si substrate printed at (a) RT, (b) 30 °C (c) 40 °C, (d) 50 °C, and (e) 60 °C.

Cross-sectional SEM image of printed CuI films was investigated by Helios SEM using a milling technique with a Focused Ion Beam (FIB). Figure 6 shows the cross-sectional SEM images of CuI films printed at RT and 60 °C. As-printed CuI films were annealed at 120 °C for 30 minutes in ambient air and coated with a gold/platinum protective layer. The CuI films were milled with an FIB for cross-sectional morphology investigation. Printed CuI film at RT had a highly porous film with thickness of ~1500 nm. Printed CuI film at 60 °C formed a free-void densely packed film with thickness of ~150 nm. It was inferred that the higher temperature formed more uniform and continuous film while suppressing creating voids. This result indicates that at printing temperature as high as 60 °C, the fast evaporation helped me form crystalline faster resulting in continuous and dense film, which is good agreement with AFM results.

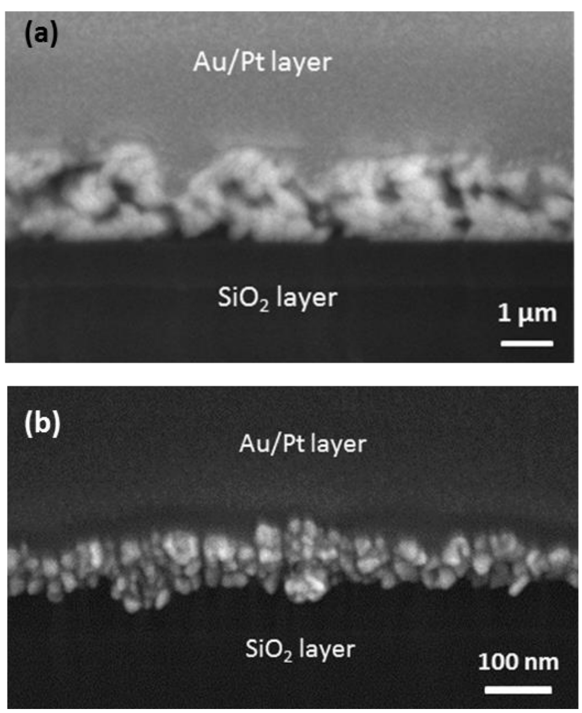

Figure 6. Cross-sectional SEM images of CuI film printed on SiO_2/Si substrate (a) at RT and (b) at 60 °C.

4.1.2 Optical property of CuI film

The optical properties of spin-coated CuI film was investigated by UV-Vis spectroscopy. CuI film was spin-coated at RT on soda lime glass and was dried at 120 °C for 30 minutes before measuring the optical properties. The bandgap was expected to be ~2.95 eV, indicating the transparency in the visible wavelengths (Figure 7a). The expected bandgap of CuI film was smaller than the widely known value (~3.1 eV) [13]. Similar band gap value was reported for a spray-coated CuI film (~2.97 eV) [25]. Also, the film had 70~90% transmittance in the visible range (Figure 7b), which also elucidated the transparency of CuI film.

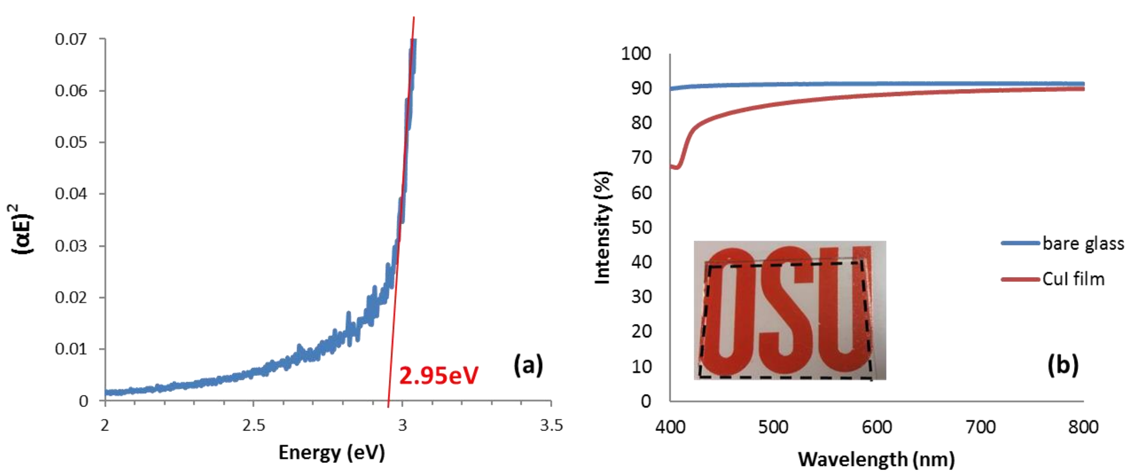

Figure 7. (a) Calculated band gap and (b) transmittance spectrum of spin-coated CuI film at RT.

4.1.3 Crystal structure of CuI film

CuI film printed on SiO_2/Si substrates at RT and 60 °C were used for XRD analysis. It was found that the film formed preferably with (111) crystal plane (Figure 8), which match with the reported results for spray-coated CuI film [25] and spin-coated CuI film [26]. The increased intensity of the peak for the CuI film printed at 60 °C, compared to the peak for the CuI film printed at RT, indicates that the crystallinity was enhanced at higher printing temperature.

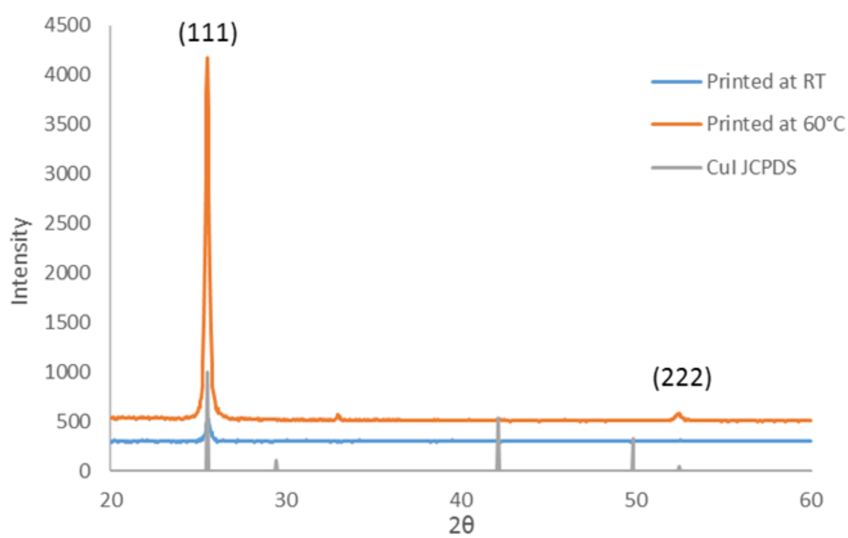

Figure 8. XRD patterns of CuI films printed at RT and 60 °C. The printed CuI films were dried at 120 °C for 30min after printing.

4.1.4 XPS of CuI film

X-ray photoelectron spectroscopy of CuI film was measure in order to confirm the oxidation state of the film (Figure 9). O 1s spectra had a peak at 532.8 eV which showed that all oxygen can be accounted for by bonds with Si and/or Carbon; in other words, there is no evidence for oxidized Cu species on the film. While I 3d spectra showed two peaks at 620eV and 631.6 eV, Cu 2p spectra showed two peaks at 933 eV and 952.8 eV. The asymmetry on the low binding energy side of the Cu $2p_{3/2}$ peak was due to the overlapping I $3p_{1/2}$ signal [27].

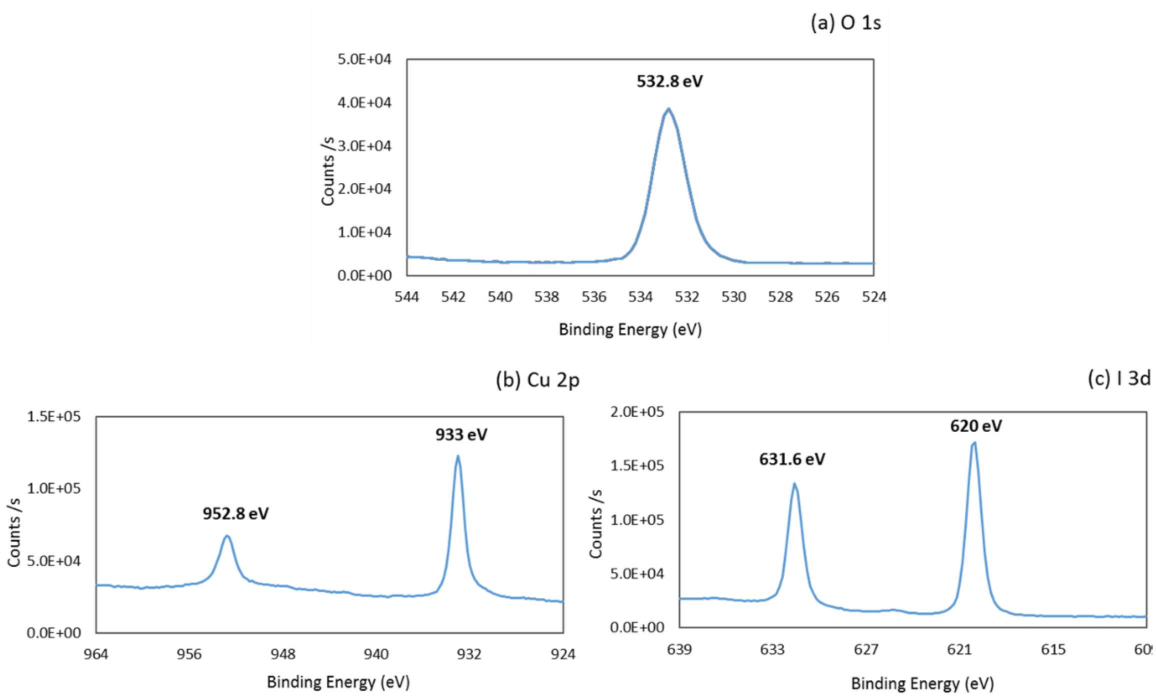

Figure 9. (a) O 1s, (b) Cu 2p, and (c) I 3d XPS spectra of printed CuI film at RT. The film was dried at 120 °C for 30 min after printing.

4.1.5 Electrical properties of CuI film

Table 1. Electrical properties of printed CuI film at RT on soda lime glass substrate.

Electrical properties	Resistivity [Ω cm]	Conductivity [Ω cm]$^{-1}$	Avg. Hall Coeff.	Hall mobility [cm^2/Vs]
Results	0.12	8.99	1.22 (p-type)	11.2

Table 1 shows electrical properties of printed CuI film at RT on soda lime glass substrates. The result demonstrates that the printed CuI film possesses the p-type nature with average Hall coefficient of 1.22. These results showing consistent electrical properties clearly indicate that the continuous and dense CuI film was successfully fabricated via inkjet printing technique.

4.2 Device performance of CuI TFTs

4.2.1 Effect of printing temperature (RT – 60 °C)

Inkjet-printed CuI film was used as an active channel layer for fabricating TFT devices. The Bottom-Gate Top-Contact (BGTC) TFT structure was fabricated. Device performances of the CuI TFT improved dramatically after the SU-8 encapsulation, showing an excellent gate modulation, saturated drain current at high drain voltage, and less off-state current.

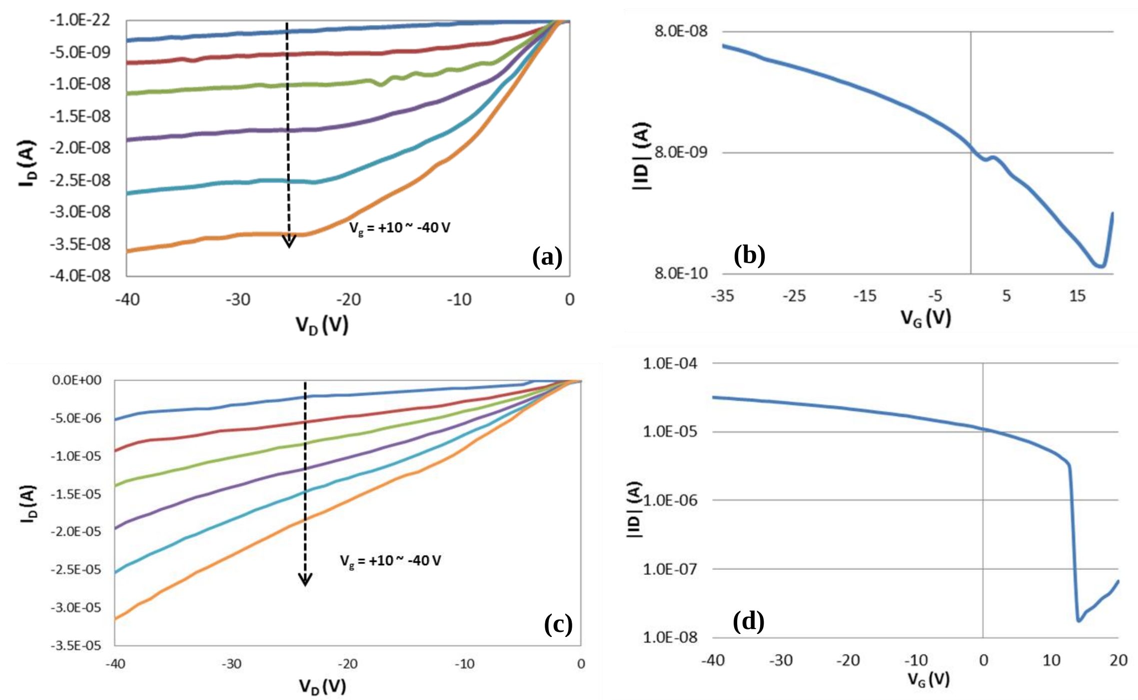

Figure 10. (a) The drain current-drain voltage (ID-VD) output characteristics (b) drain current-gate voltage (ID-VG) transfer characteristics (ID plotted logarithmically) at VDS = - 40 V of RT printed CuI TFT on the SiO2/Si substrate. (c) ID-VD output characteristics (d) ID-VG transfer characteristics of 60 °C printed CuI TFT on the SiO2/Si substrate.

Figure 10 shows the drain current-drain voltage (I_D-V_D) output characteristics and the drain current-gate voltage (I_D-V_G) transfer characteristics of CuI TFTs printed at RT and 60 °C, respectively. Both transistors that were fabricated at RT and 60 °C exhibited great gate-modulated behavior with drain-current saturation (soft-saturation for the device printed at 60 °C). The average field-effect mobility (μ_{FE}) and on/off ratio (I_{on}/I_{off}) of CuI TFTs printed at RT were 0.11 cm^2 V^{-1} s^{-1} and $10^{1.7}$, respectively. The highest μ_{FE} and I_{on}/I_{off} of CuI TFTs printed at 60 °C were 4.4 cm^2 V^{-1} s^{-1} and $10^{3.2}$, respectively. The mobility was determined from the transconductance of the device at V_{DS} = - 1 V and the I_{on}/I_{off} was determined at V_{DS} = - 40 V.

Device performances of CuI TFTs were measured at ambient conditions. Figure 11 shows the μ_{FE} and I_{on}/I_{off} data for CuI TFT devices as a function of the printing temperature from RT to 60 °C. The AFM and SEM data (Figure 5, 6) suggested that printing temperature affected crystallinity and continuity of the printed CuI film; while CuI film printed at RT had a porous structure, the film printed at 60 °C formed dense and continuous film. It is preferred for the channel layer of TFT device to have dense and continuous film without voids, which trap charge carriers, in order to have superior TFT device properties. Also, the grain size of printed CuI film increased when printed at 60 °C which resulting reduction in grain boundaries at the semiconductor and dielectric interface resulting in less carrier scattering [24]. Therefore, the p-type CuI TFT printed at 60 °C showed the maximum μ_{FE} and I_{on}/I_{off}.

The variation of mobility and on/off data for the same printing temperature might be due to the dissimilarity among ejected CuI ink droplets. Even with the same printing setting, the ejected CuI ink droplet varies every time when printing which affects the uniformity when forming the films.

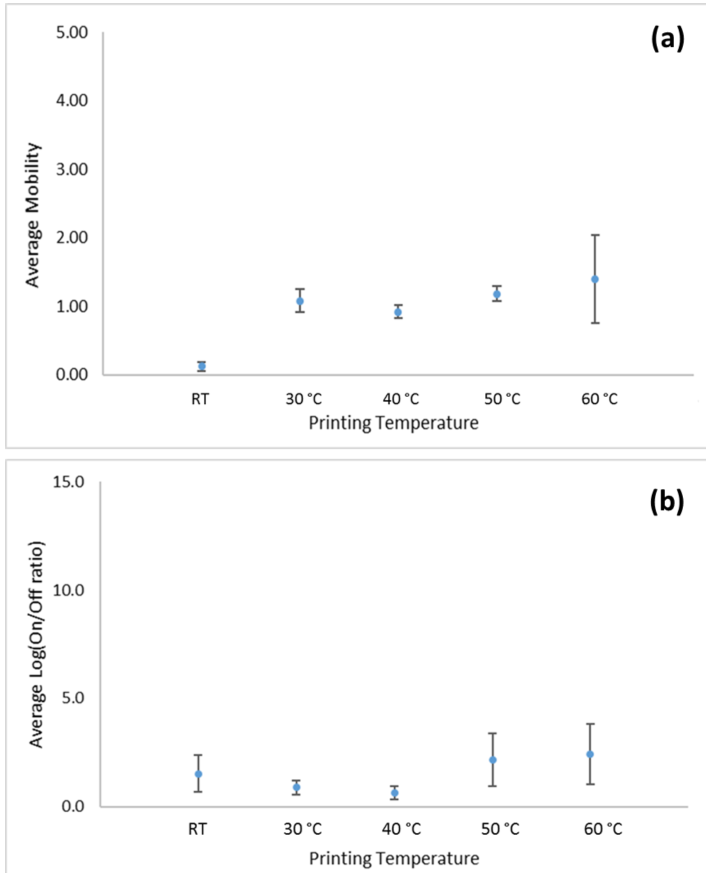

Figure 11. (a) Average field effect mobility and (b) average Log(on/off ratio) data of CuI TFTs printed at various substrate temperature from RT to 60 °C (with standard deviation error bars).

4.2.2 Effect of Drop spacing (10 – 40 µm)

In this study, CuI film was deposited on SiO_2/Si substrate by piezoelectric inkjet printer, where piezoelectric materials were controlled by high electric field and the deformation of the materials ejecting the ink towards the substrate (Figure 12 a) [6]. In the meantime, the film deposition can be varied by changing the drop spacing, which is the distance between the printed droplets on the substrate (Figure 12 b, c). Drop spacing of the printed CuI film was in the range from 10 µm to 40 µm.

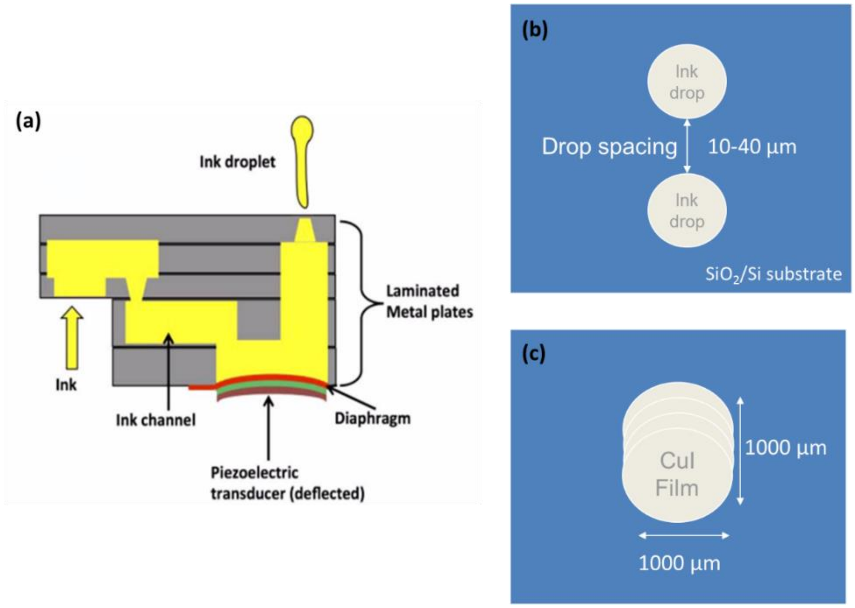

Figure 12. Schematic diagram of (a) piezoelectic inkjet printer (adapted from [6]*), (b) exaggerated illustration of drop spacing, the distance between printed droplets, and (c) realistic illustration of printed CuI film with the overlapped printed droplets of which drop-spacing is in the range from 10 µm to 40 µm.*

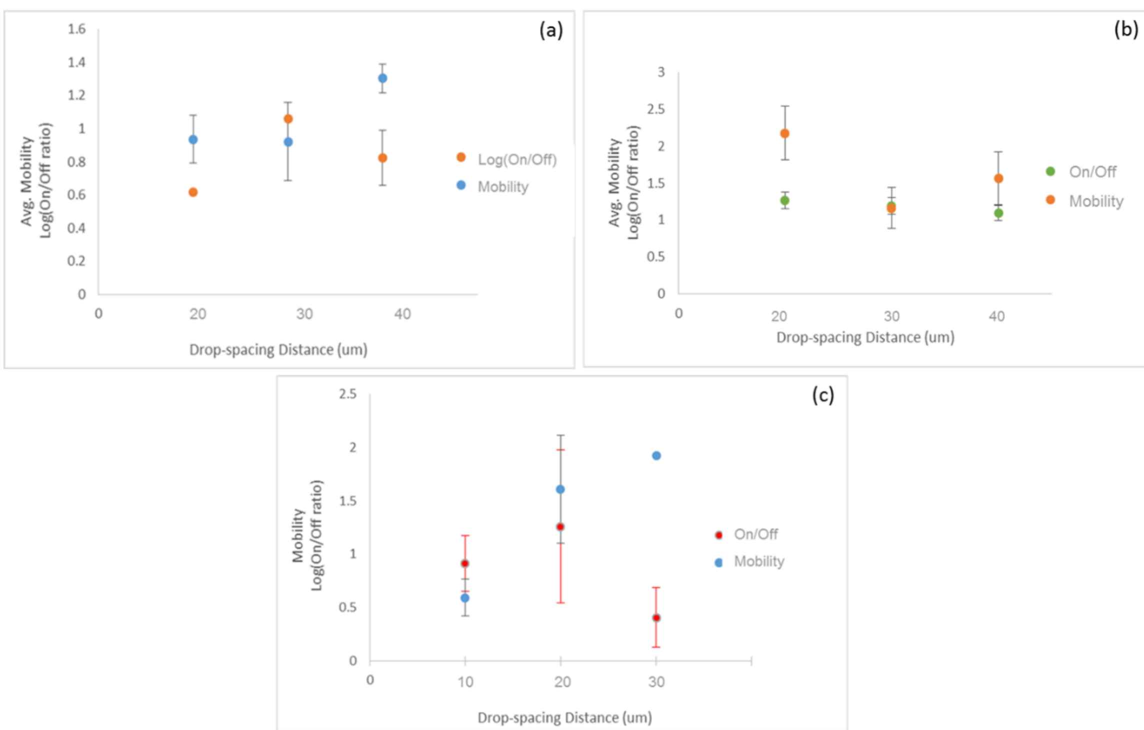

Figure 13. Effect of drop spacing in piezoelectric inkjet printer on mobility and log(I_{on}/I_{off}) of p-type CuI TFTs printed at (a) 30 °C, (b) 50 °C, and (c) 60 °C.

The various drop spacing distances were tested for printing CuI films at different printing temperatures in order to optimize the device properties of CuI TFT. Figure 13 shows the mobility and log(on/off ratio) data with various drop spacing distances from 10 µm to 40 µm when CuI film was printed on the substrate of 30 °C (Figure 13 a), 50 °C (Figure 13 b), and 60 °C (Figure 13 c). It was concluded that 30 µm is the optimum drop-spacing for 30 °C printing setting and 20 µm for 50 °C and 60 °C printing settings.

4.2.3 Effect of W/L ratios (W/L = 1.4 – 5)

Channel layer width (W) and length (L) were varied to optimize the device performance of p-type CuI TFT. While fixing the length of the channel layer as 200 µm, the width of the channel layer was varied from 280 µm to 1000 µm (Figure 14). While the printed CuI film had less overlapped area and formed almost single layer at W/L=1.4, there were multiple overlapped area in the CuI film when W/L=5. The μ_{FE} was as high as 6.54 $cm^2\ V^{-1}\ s^{-1}$ and I_{on}/I_{off} ratios of $10^{1.1}$ for CuI TFT printed at 60 °C when W/L=1.4. It was expected that the overlapped area of CuI film helped to reduce the off-current state. Therefore, the p-type CuI TFTs were fabricated with W/L=5 channel layer. It was inferred that the overlapped area might influence the variation of device performance as shown in the error bars for the TFTs in Figure 7.

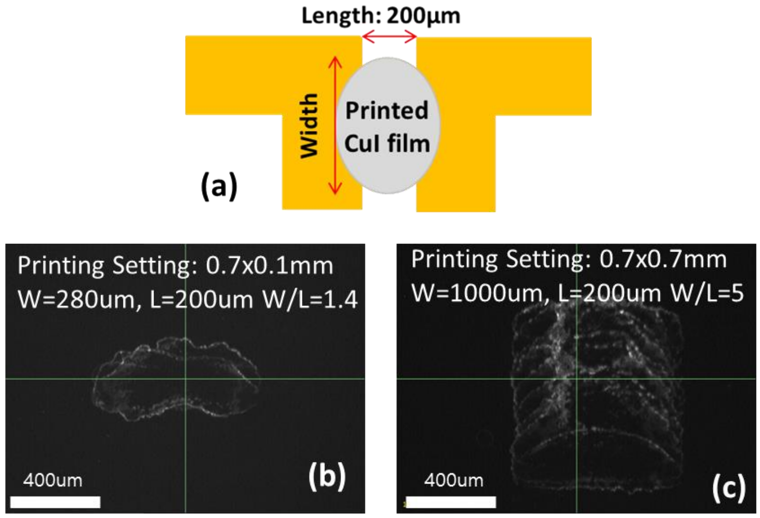

Figure 14. (a) Schematic diagram of printed CuI channel layer and deposited gold as a source and drain with defined channel width and length (b) optical top-view of printed CuI film at 60 °C with W=280 µm, L=200 µm, and (c) with W=1000 µm, L=200 µm.

Table 2 shows summarized results of device performance of p-type CuI TFTs with various drop spacing and W/L ratios. The CuI films of the devices were printed at 60 °C. It turned out that the device performance of CuI TFT was optimized when W/L = 5 and drop spacing was 20 µm.

Table 2. Average mobility and on/off ratio data of p-type CuI TFTs printed at 60 °C which were fabricated with various drop spacing (10 - 30 µm) and W/L ratios (1.4 - 5).

Printed at 60 °C	**L=200 µm, W varied**					
	W/L=5		**W/L=2.5**		**W/L=1.4**	
drop spacing	**Avg. Mobility**	**Avg. I_{on}/I_{off}**	**Avg. Mobility**	**Avg. I_{on}/I_{off}**	**Avg. Mobility**	**Avg. I_{on}/I_{off}**
10 µm	0.99	$10^{0.59}$	-	-	-	-
20 µm	2.20	$10^{1.28}$	1.75	$10^{0.69}$	3.09	$10^{0.48}$
30 µm	0.53	$10^{1.68}$	-	-	-	-

4.2.4 Effect of TFT structures (BGTC, BGBC)

Different TFT structures were applied for fabricating p-type CuI TFTs in order to find the best performing device structure. Bottom-Gate Top-Contact (BGTC) and Bottom-Gate Bottom-Contact (BGBC) were applied when fabricating CuI TFTs (Figure 15). The active channel layers which were printed at 60 °C, 20 μm drop-spacing, and W/L=5 were used to fabricate CuI TFT for each structure. While the BGTC CuI TFT had the highest μ_{FE} as 4.4 $cm^2\ V^{-1}\ s^{-1}$ and and I_{on}/I_{off} ratios of $10^{3.2}$ with great gate-modulation and drain-current saturation, the BGBC CuI TFT had the highest μ_{FE} as 1.83 $cm^2\ V^{-1}\ s^{-1}$ and I_{on}/I_{off} ratio of $10^{0.4}$ with less gate-modulation and lack of drain-current saturation. The inferior device properties of the BGBC structure were expected to be due to lack of uniformity of the channel layer. It was inferred that since gold was deposited as a source and drain first and then the channel layer was printed for the BGBC structure, the CuI film at the edge of the source/drain interacted with the gold layer surface. This deposition process made CuI film form a meniscus shape, instead of a uniform horizontally parallel film.

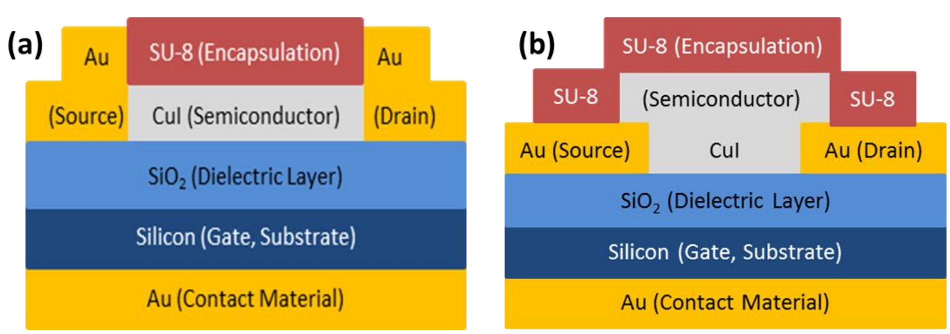

Figure 15. P-type CuI TFT with (a) Bottom-Gate Top-Contact (BGTC) structure, and (b) Bottom-Gate Bottom-Contact (BGBC) structure.

5. Results and Discussion: Copper (I) Iodide-based TFTs

In order to improve device performance, different copper(I) halides (CuX, X=Br, Cl) were implemented for fabricating copper(I) iodide-based TFTs. It was expected that implementing different halide materials would reduce the carrier concentration which could lead to less conductivity and better saturation for resulting transistor devices. While CuI was used as a base material, CuBr and CuCl were added in precursor solutions which resulted in CuBrI and CuClI ink. Since the crystalline structure of CuX is the same as CuI, the powder form of them was simply mixed with CuI powder in solvent when preparing the precursor ink. Various molar ratios were tested in order to find optimum conditions for CuBrI and CuClI solution for TFT application.

5.1 Characterization of CuBrI film

Inkjet-printed CuBrI film on PECVD-SiO_2/glass substrate was characterized by AFM and XRD (Figures 16, 17). CuBrI solution was also spin-coated on a soda lime glass substrate for analyzing band gap.

5.1.1 Morphology of CuBrI film

CuBrI film was printed at RT on PECVD-SiO_2/glass and thermally-grown-SiO_2/Si (TG-SiO_2/Si) substrates. The AFM images (Figure 16) showed different CuBrI forming with respect to different substrates. It was found that the nature of substrate affected forming CuBrI films, in terms of reaction kinetics and the adhesion of the deposited film [28]. While only islands were formed, which resulted in discontinuous film on TG-SiO_2/Si substrate, more continuous film was formed on PEVCD- SiO_2/glass substrate.

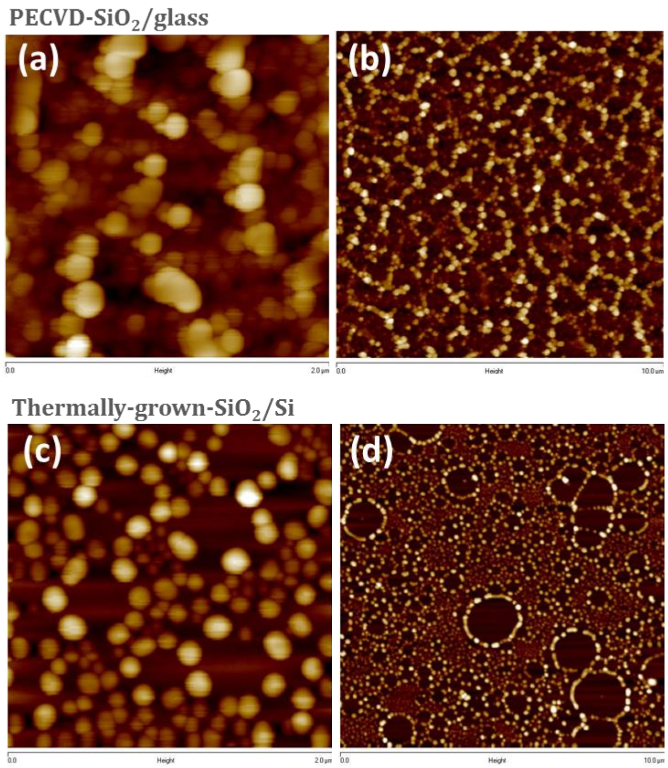

Figure 16. AFM images of CuBrI film printed at RT of (a) 2x2 μm, (b) 10x10 μm on PECVD-SiO_2/Si substrates; (c) 2x2 μm, (d) 10x10 μm on thermally-grown SiO_2/Si substrate.

5.1.2 Optical property of CuBrI film

The optical properties of spin-coated CuBrI film was investigated by UV-Vis spectroscopy. CuBrI film was spin-coated at RT on a soda lime glass and was dried at 120 °C for 30 minutes before measuring the optical properties. The bandgap was expected to be ~2.85 eV and ~3.1 eV, which agreed to the reported values [13], indicating CuI and CuBr crystalline were formed separately (Figure 17). The estimated bandgap indicated the transparency of printed CuBrI film in the visible wavelengths.

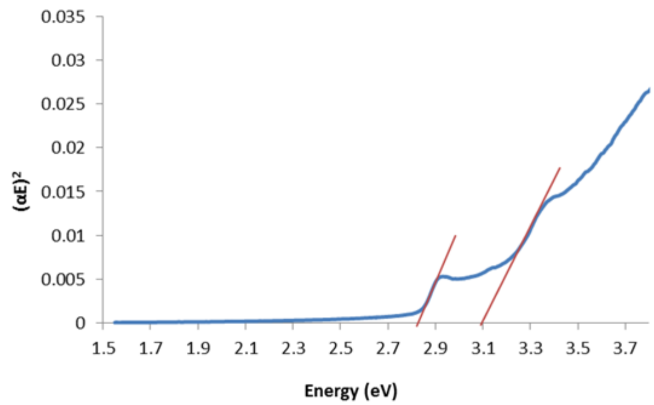

Figure 17. Estimated bandgap of spin-coated CuBrI film on soda lime glass at RT. The spin-coated film was dried at 120 °C for 30 min before measurement.

5.1.3 Crystal structure of CuBrI film

The CuBrI film printed at RT, CuBr powder, and CuI powder were used for XRD analysis. It was found that the film formed preferably with (2 2 0) crystal plane (Figure 18) which agreed with reported data [13].

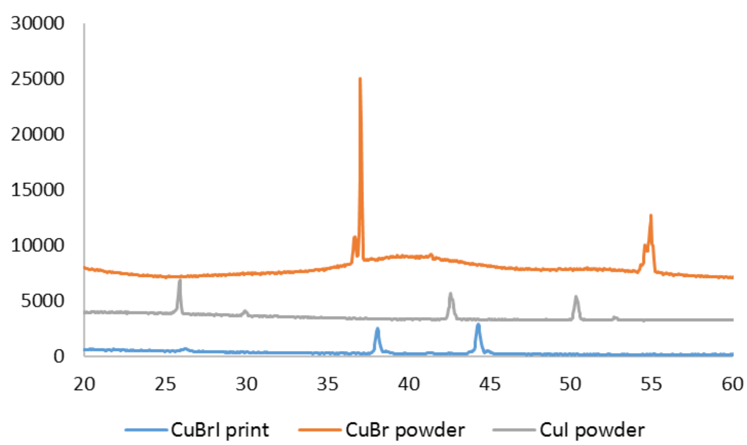

Figure 18. XRD patterns of CuBrI film printed at RT, CuBr powder, and CuI powder. The printed CuBrI films were dried at 120 °C for 30min after printing.

5.2 Device Performance of CuBrI TFTs

5.2.1. CuBrI TFTs printed at RT

Inkjet-printed CuBrI film was used as an active channel layer for fabricating TFT device on PECVD-SiO_2/glass substrate without SU-8 encapsulation. The Bottom-Gate Top-Contact (BGTC) TFT structure was fabricated. It was found that the transistors exhibited good gate-modulated behavior with drain-current saturation without SU-8 encapsulation, unlike CuI TFTs. It was inferred that CuBr helped the film to be more compatible for TFT application in terms of durability and moisture sensitivity. While the CuBrI film printed at RT on TG-SiO_2/Si substrate was not applicable as a TFT device, the film printed at RT on PECVD-SiO_2/glass substrate was successfully implemented into a TFT device. It was inferred that the film morphology affected the feasibility of TFT application; the CuBrI film printed on TG- SiO_2/Si formed mostly islands, while the film printed on PECVD- SiO_2/glass substrate was more continuous film (Figure 16).

Figure 19 shows the drain current-drain voltage (I_D-V_D) output characteristics and the drain current-gate voltage (I_D-V_G) transfer characteristics of CuBrI TFTs printed at RT. The average field-effect mobility (μ_{FE}) and on/off ratio (I_{on}/I_{off}) of CuBrI TFTs printed at RT were 2.39 $cm^2\ V^{-1}\ s^{-1}$ and $10^{1.9}$. The mobility was determined from the transconductance of the device at V_{DS} = - 1 V and the I_{on}/I_{off} was determined at V_{DS} = - 40 V.

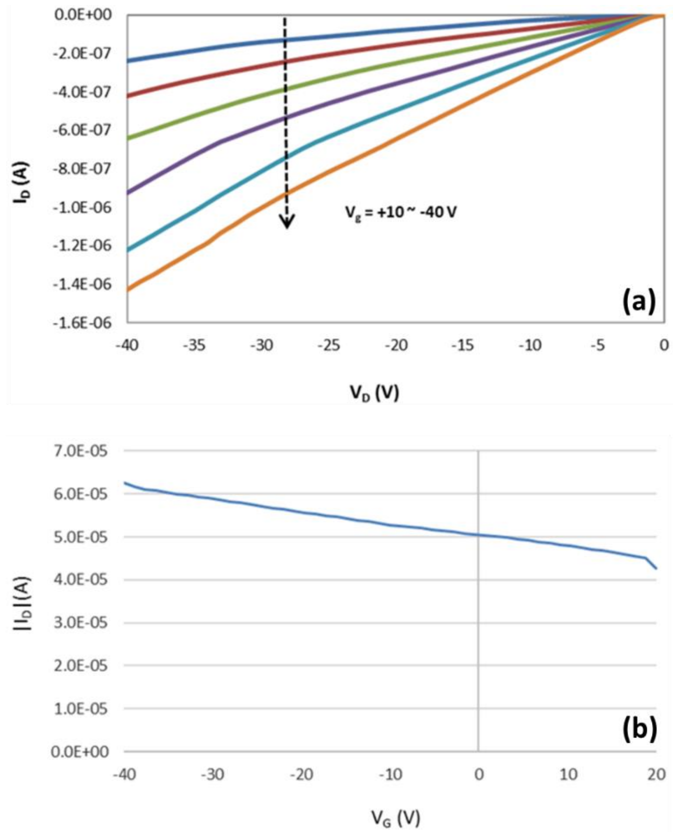

Figure 19. (a) The drain current-drain voltage (I_D-V_D) output characteristics (b) drain current-gate voltage (I_D-V_G) transfer characteristics (I_D plotted logarithmically) at V_{DS} = - 40 V of CuBrI TFT printed at RT on the PECVD-SiO_2/glass substrate.

5.2.2. Effect of molar ratio of CuBrI TFTs

Various molar ratios of CuBr : CuI were tested in order to find the optimized condition for CuBrI TFT application (Table 2). P-type CuBrI TFTs for 1:1, 3:7, and 7:3 molar ratio of CuBr : CuI were successfully realized on PECVD-SiO2/glass substrate. 1:1 molar ratio was found to be the optimum condition for CuBrI transistor printed at RT on PECVD-SiO_2/glass substrate. In addition, the films printed on TG-SiO_2/Si substrate were also tested for 1:1, 3:7, and 1:9 molar ratios for printing temperature of RT and 60 °C. The film printed at RT on TG-SiO_2/Si substrate was not feasible for TFT application, while the CuBrI film of which 3:7 and 1:9 molar ratios of CuBr : CuI printed at 60 °C were successfully implemented into TFTs on $TG-SiO_2/Si$ substrates.

Table 3. Device performance of CuBrI TFTs for various molar ratios of CuBr:CuI on PECVD-SiO2/glass and TG-SiO2/Si substrate printed at RT and 60 °C, respectively.

PECVD-SiO2/Glass				**Thermally-Grown-SiO2/Si**			
RT	**1:1**	**3:7**	**7:3**	**60 °C**	**1:1**	**3:7**	**1:9**
μ_{FE} (cm2/Vs)	2.38	0.033	0.013	μ_{FE} (cm2/Vs)	-	0.78	0.95
I_{on}/I_{off} ratio	$10^{1.9}$	$10^{0.16}$	$10^{1.39}$	I_{on}/I_{off} ratio	-	$10^{0.48}$	$10^{0.54}$

5.3 Device Performance of CuClI TFTs

The CuClI film inkjet-printed at 60 °C was used as an active channel layer for fabricating TFT devices on $TG-SiO_2/Si$ substrate. The Bottom-Gate Top-Contact (BGTC) TFT structure was fabricated. It was found that the transistors exhibited good gate-modulated behavior, but conductive compared to CuI and CuBrI TFTs. Also, SU-8 encapsulation was needed in order to have a better gate-modulation, like in CuI TFTs. Various molar ratios of CuCl : CuI were tested in order to find the optimized condition. It was found that only the film with 1:9 ration of CuCl : CuI was working as channel layer of p-type TFT device.

Figure 20 shows the drain current-drain voltage (I_D-V_D) output characteristics and the drain current-gate voltage (I_D-V_G) transfer characteristics of CuClI TFTs printed at RT. The highest μ_{FE} and I_{on}/I_{off} of CuClI TFTs printed at 60 °C were 1.02 $cm^2\ V^{-1}\ s^{-1}$ and $10^{0.73}$. The mobility was determined from the transconductance of the device at V_{DS} = - 1 V and the I_{on}/I_{off} was determined at V_{DS} = - 40 V.

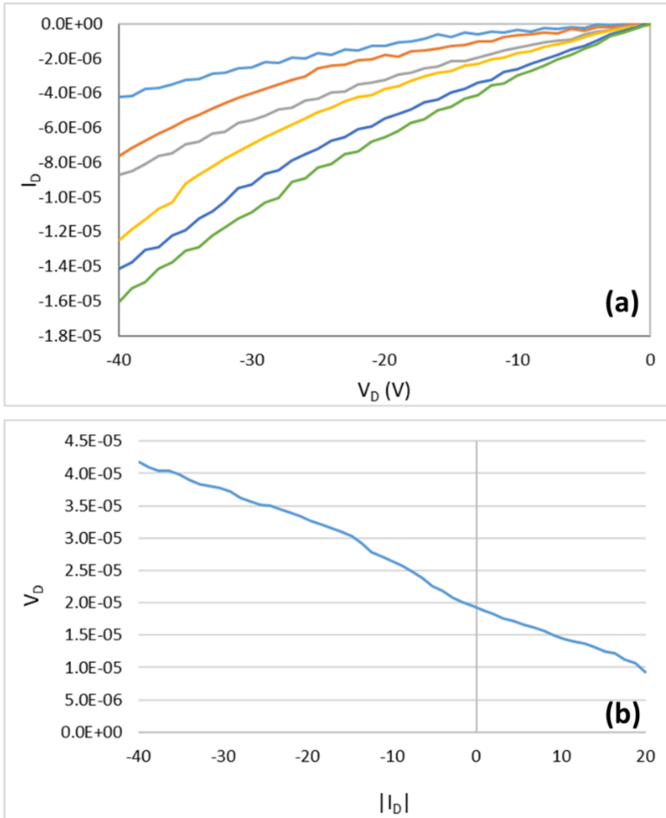

Figure 20. (a) The drain current-drain voltage (ID-VD) output characteristics (b) drain current-gate voltage (ID-VG) transfer characteristics (ID plotted logarithmically) at VDS = - 40 V of CuClI TFT printed at 60 °C on the TG-SiO2/glass substrate, when CuCl:CuI ratio was 1:9.

6. Conclusion

Inkjet-printed Copper(I) Iodide-based p-type TFTs were fabricated for the first time. CuI, CuBrI, and CuClI films were printed at room temperature. As-printed copper(I) halides films were used as p-type active channel layers for TFTs after drying at 120 °C. The entire process of fabricating TFTs was kept under 150 °C, which is compatible with flexible plastic substrates and transparent glass substrate. Various different printing temperatures, drop spacing, W/L ratios, and TFT structures were tested in order to find the optimum device properties for p-type copper(I) iodide-based TFT. It was found that the BGBC CuI TFTs with 60 °C printed channel layer which has 20 µm drop-spacing and W/L ratio as 5 have the most superior device properties. CuI TFTs with SU-8 encapsulation exhibited outstanding p-type transistor behaviors with field-effect mobility as high as 4.36 $cm^2\ V^{-1}\ s^{-1}$ and and I_{on}/I_{off} ratios of $10^{3.24}$ for CuI films that were printed at 60°C on the silicon substrates. Also, CuBrI TFTs resulted in successful p-type transistor behaviours with average field-effect mobility of 2.4 $cm^2\ V^{-1}\ s^{-1}$ and I_{on}/I_{off} ratio of $10^{1.9}$ on the glass substrates when the molar ratio of CuBr:CuI was 1:1. In addition, CuClI TFTs were successfully fabricated with field-effect mobility as high as 1.02 $cm^2\ V^{-1}\ s^{-1}$ and I_{on}/I_{off} ratio of $10^{0.73}$ on the silicon substrates when the molar ratio of CuCl:CuI was 1:9. The device performance were comparable to reported p-type metal oxide TFTs. This study suggests that copper(I) iodide-based semiconductors could be promising low-temperature inkjet-printed p-type semiconductor candidates for TFT application.

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