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Title: Design Techniques for PVT Tolerant Phase-Locked Loops

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Un-Ku Moon Kartikeya Mayaram

The continued scaling of deep-submicron CMOS technology enables low-voltage high-frequency phase-locked loops (PLLs) to be fully integrated in complex mixed-signal systems. However, fluctuations due to the manufacturing process and variations in environmental conditions, such as supply voltage and temperature, are also significantly increased. As a result, the performance of PLLs that are susceptible to process, voltage, and temperature (PVT) variations are dramatically affected.

To truly benefit from process scaling, PVT tolerant designs of high-performance PLLs are essential. In this dissertation, circuit techniques that can mitigate the impacts of PVT variations on PLL performance are presented. In the context of ring voltage-controlled oscillator (VCO) based PLLs, an on-chip calibration technique for reducing the supply voltage sensitivity is described. This method rejects supply noise while avoiding the use of supply regulation, which makes it more desirable in the design of low-voltage high-performance ring VCOs. In a wide-tuning

range LC-VCO based PLL frequency synthesizer, design techniques for maintaining a constant loop bandwidth are presented. Having a constant loop bandwidth that is insensitive to PVT variations helps PLL frequency synthesizers to achieve optimum performance in all frequency bands. The proposed circuit techniques are validated by measurement results obtained from prototype chips. The concepts that have been presented in the context of analog PLL implementations can be easily migrated to digital PLLs.

Design Techniques for PVT Tolerant Phase-Locked Loops

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APPROVED:

Co-Major Professor, representing Electrical and Computer Engineering

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Co-Major Professor, representing Electrical and Computer Engineering

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Director of the School of Electric Engineering and Computer Science

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Dean of the Graduate School

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Ting Wu, Author

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Chapter 1 – Introduction

1.1 Motivation

Today's rapid advance in fiber-optic links, radio-frequency (RF) communications, and multi-gigahertz microprocessors have led to an exponential expansion of data rate and data volume. A phase-locked loop (PLL) provides the timing basis for all of the above modern communication and digital systems. A PLL is a feedback system that generates an output signal whose frequency/phase accurately tracks that of an input reference. Early PLLs were designed in 1930s and used for radio systems. But they used expensive discrete components. Today, low-cost integrated PLLs have become ubiquitous in both wired and wireless communication systems.

The analysis and design of PLLs have been well established after Gardner's work [1]. However, there is still significant research interest in the design of PLLs for deep submicron processes. One of the reasons is that many benefits and challenges arise due to technology scaling. Deep submicron processes enable multi-gigahertz PLLs to be implemented using complementary-metal-oxide-semiconductor (CMOS) technology. CMOS technology is attractive due to its high density, good reliability, low power consumption, and low cost. A high density also implies enhanced levels of integration, which further reduces the cost of integrated circuits. In addition, as CMOS transistors scale down, their performance

(e.g., transistor f_T) improves significantly. PLLs that operate at millimeter-wave frequencies have been demonstrated using CMOS technology rather than conventional gallium arsenide (GaAs) or silicon germanium (SiGe) technologies.

One of the challenges in CMOS PLL design is to keep pace with new technology trends, which requires operating at higher frequencies and at lower supply voltages. The design of analog integrated circuits is more complicated in deep submicron CMOS processes due to the decreased voltage headroom and increased gate leakage. Accurate modeling of both active and passive devices becomes increasingly important. Additionally, a higher level of integration results in substantial digital switching noise that can be coupled through the power supply and substrate into the noise-sensitive analog circuits.

Finally, increased parameter variations in scaled CMOS technologies are posing a major challenge for the design of high performance PLLs. These variations include fluctuations due to the manufacturing process and variations in the environmental conditions, such as the supply voltage and temperature. As a result, the performance of traditional PLLs that are susceptible to process, voltage, and temperature (PVT) variations are dramatically affected. To meet the stringent specifications of PLLs for modern communication systems, circuit designers have to perform a large number of simulation runs under various operating conditions at the expense of time and manpower. Moreover, conservative operating points are commonly used and, hence, an optimum PLL performance may not be achieved. Therefore, it is imperative to understand the impact of PVT variations and to make PLL designs tolerant to PVT variations.

1.2 PVT Variations in Scaled Processes

Driven by Moore's law, CMOS technology continues to scale down. The scaling trend is provided by the International Technology Roadmap for Semiconductors (ITRS) [2]. Fig. 1.1(a) shows the steady decrease in transistor gate length and accordingly the increase in local clock frequencies (defined as the delay of 12 inverters). On the other hand, supply voltages are dramatically reduced as depicted in Fig. 1.1(b).

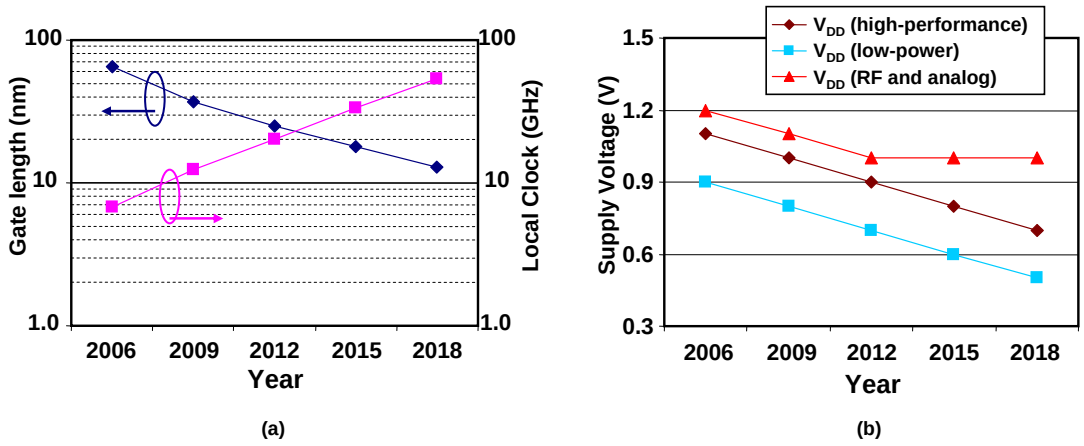


Figure 1.1: Continued scaling of CMOS technology. (a) Gate length and local clock frequencies. (b) Supply voltages.

As the technology continues to scale beyond 90nm, parameter variations are changing design problems from deterministic to probabilistic [3]. The PVT variations are posing a major challenge to the future design of PLLs. The performance, in terms of speed, noise, and power can vary significantly under PVT variations. Therefore, PVT variation tolerant design is imperative for the design of next-generation high-performance PLLs. In this chapter, the PVT variations and their

impact on circuits are briefly introduced. The circuit techniques that can mitigate the impact of PVT variations on PLL performance are discussed in the next chapters.

Process Variations

Process variations are mainly due to the variations in transistor threshold voltage and channel length. The variations in threshold voltage and channel length are normally distributed, with the standard deviations of σ_{VT} and σ_L, respectively. In a 180-nm CMOS logic technology, $3\sigma_{VT}$ is about 30 mV [3]. For the effective channel length, $3\sigma_L$ is about 20% of the nominal gate length [4].

Each generation of transistor scaling yields a 30% decrease in gate delay time and accordingly a 43% improvement in clock frequency. Assuming only L and the corresponding parameters are varied, projections for the 50-nm technology generation indicate that a generation of performance gain can be lost due to systematic within-die fluctuations [4].

Supply Voltage Variations

The demand for low power consumption implies that supply voltages continue to scale down. The power supply noise is proportional to the maximum current rate of change $\Delta i/\Delta t$. With each process generation, Δi increases and Δt decreases, resulting in a quadratic increase in supply noise [5]. Since the packaging and platform technologies do not follow the scaling trends of CMOS processes, the

power delivery impedance does not scale with V_{DD} [3]. Therefore, the supply voltage variation ΔV_{DD} has become a significant percentage of V_{DD}.

Since the oscillation frequency of a ring oscillator is a strong function of the supply voltage, the power supply noise can impair the performance of ring oscillators significantly. As a consequence, supply noise must be suppressed in the design of ring oscillator based PLLs.

Temperature Variations

Within die temperature fluctuations have existed as a major performance and packaging challenge for many years [3]. The performance of both devices and interconnects depend on temperature, resulting in circuit performance degradation at higher temperatures. For example, an increase in the temperature causes both the mobility of carriers and transistor threshold voltage to decrease.

1.3 Thesis Organization

In Chapter 2, PLL fundamentals and noise analysis are reviewed. The analog and digital techniques that overcome PVT variations in PLLs are discussed. The fundamental limitations of digital PLLs are examined.

To suppress the supply noise of ring oscillators, traditional techniques use regulators at the expense of reduced voltage headroom. However, supply regulation is not preferred in the future processes due to the reduced supply voltages. In Chapter 3, an on-chip calibration technique for reducing supply voltage sensitivity

in ring VCOs is described. The prototype chip measurement results demonstrate robust performance of a ring VCO based PLL in the presence of VCO supply noise.

Chapter 4 presents the design of a constant loop bandwidth LC-VCO based frequency synthesizer. Since LC-VCO gain varies substantially across the operating frequency, the PLL bandwidth changes, which may result in performance degradation. The existing solutions that compensate for the LC-VCO gain variations are not only process and temperature dependent, but also designed for narrow-band applications. A new PLL frequency synthesizer with a dual-tuned LC-VCO using a novel averaging varactor and a charge-pump biasing circuit that tracks the PLL operating frequency is presented. A relatively constant PLL bandwidth over a wide frequency tuning range is validated by measurement results.

Chapter 2 – Design Techniques for PVT Tolerant PLLs

2.1 PLL Basics and Noise Analysis

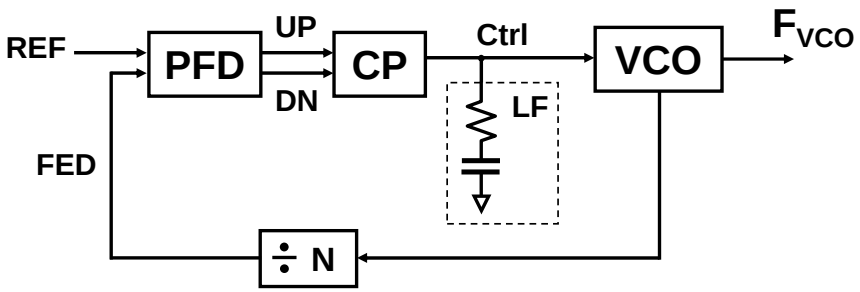


Figure 2.1: A typical charge-pump PLL block diagram.

The block diagram of a commonly used charge-pump (CP) PLL is shown in Fig. 2.1. It consists of a phase and frequency detector (PFD), a CP, a loop filter (LF), a voltage controlled oscillator (VCO) and a divide-by-N divider. Via the divider, the VCO output is fed back to the PFD with a divided-down signal (FED). The other input to the PFD is a fixed reference frequency/phase (REF). The PFD compares the frequency and phase difference between the two inputs. The CP produces a current that has an average value proportional to the phase error. The LF smooths the current into a voltage on the control node (Ctrl), which in turn drives the VCO. In the steady state, the PFD inputs are equal in phase and frequency. The phase error is zero and the loop is in a locked condition. The VCO

has an output frequency equal to

$$F_{VCO} = F_{REF} \cdot N \tag{2.1}$$

where F_{VCO} and F_{REF} are the frequencies of the VCO and the reference, respectively. This equation suggests that the PLL generates stable high frequencies from a low-frequency reference. Hence, any system that requires stable high frequency tuning can benefit from the phase-locking technique. Examples of these applications include clock generation, clock recovery, and wireless systems such as base stations, handsets, pagers, etc.

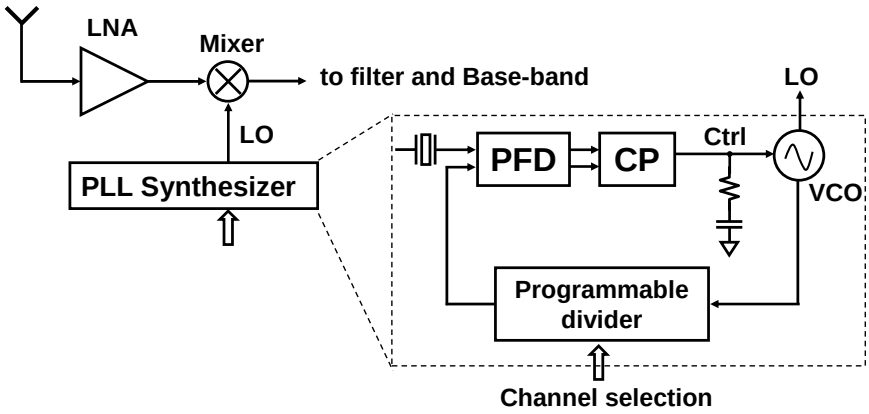


Figure 2.2: A PLL frequency synthesizer used in a wireless receiver.

As an example, consider a PLL frequency synthesizer used in a wireless receiver. Fig. 2.2 shows a typical block diagram. The role of a PLL frequency synthesizer is to provide the reference frequency for frequency translation. Ideally, the PLL synthesizer generates a single frequency tone (LO). The received RF signal spectrum is amplified by an LNA and mixed with the LO by a mixer. After filtering, only

the spectrum in the baseband is left for further demodulation and processing. Using a fixed reference frequency provided by a low noise crystal oscillator, different VCO output frequencies (channels) are achieved by changing the division ratio in a programmable divider.

Ideally, the LO signal in a RF receiver is a single tone in the frequency spectrum. In practice, however, random and systematic phase deviations from the desired values produce energy in frequencies other than the desired frequency. To quantify the noise level, phase noise is defined as the ratio of the noise in a 1-Hz bandwidth at a specified frequency offset to the signal power at the center frequency f_o. When an LO signal with phase noise is mixed with the RF signal, the nearby RF can be down-converted to the baseband, causing performance degradation.

In the context of a clock generation or a clock recovery system, the timing jitter is a key specification. Jitter is an undesired perturbation or uncertainty in the timing of events. Jitter and phase noise are related. In fact, the equivalent rms jitter can be obtained by integrating the phase noise power over the frequency range of interest. As a result, the phase noise of a PLL is an important parameter. In order to quantify the PLL phase noise and identify the noise contributions from each noise source, a frequency domain analysis of a closed-loop PLL is needed.

Fig. 2.3 shows the linear model of a typical PLL. In this model, the phase detector (PD) has a gain of K_d (A/radian), the loop filter has a transfer function F(s) (Ω), and the VCO has a gain of K_o (radian/s/V). Since the VCO output phase is an integrated value of frequency, an integrator (1/s) is also included in

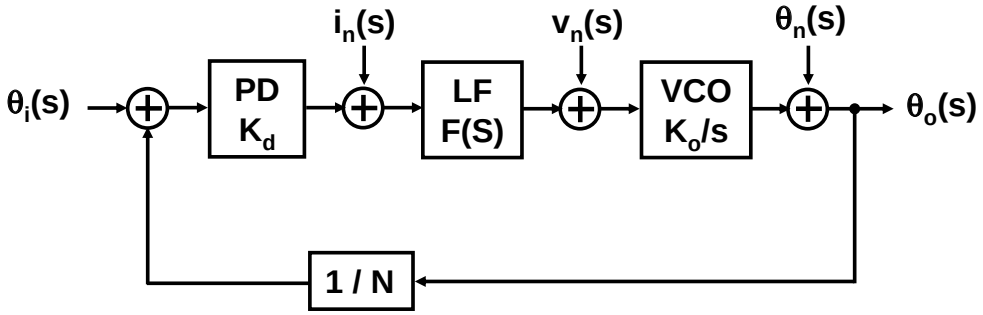


Figure 2.3: Linear model of a PLL.

the VCO model. It can be shown that, the open loop gain $G(s)$ is given by

$$G(s) = \frac{K_d F(s)}{N} \frac{K_o}{s} \tag{2.2}$$

In order to calculate the phase noise at the PLL output, the noise sources should be identified first. There are four main phase noise contributors, as shown in Fig. 2.3. They are the reference (and the divider) noise $\theta_i(s)$, the PD noise $i_n(s)$, the LF noise $v_n(s)$, and the VCO noise $\theta_n(s)$. Each term contributes to the overall phase noise. Multiplying the noise power at a noise source by the squared magnitude of the corresponding noise transfer function gives the noise contribution to the output. Hence, the noise transfer function from each noise source needs to be established.

The PLL output phase is denoted by $\theta_o(s)$. The noise transfer functions from various inputs can be derived to yield

$$H_{in}(s) = \frac{\theta_o(s)}{\theta_i(s)} = N \frac{G(s)}{1 + G(s)} \tag{2.3}$$

$$H_{PD}(s) = \frac{\theta_o(s)}{i_n(s)} = \frac{N}{K_d}\frac{G(s)}{1+G(s)} \tag{2.4}$$

$$H_{LF}(s) = \frac{\theta_o(s)}{v_n(s)} = \frac{K_o/s}{1+G(s)} \tag{2.5}$$

$$H_{VCO}(s) = \frac{\theta_o(s)}{\theta_n(s)} = \frac{1}{1+G(s)} \tag{2.6}$$

Note that the noise transfer function $H_{in}(s)$, from the reference to output, is equivalent to the overall closed loop transfer function $H(s)$. This is a low-pass transfer function with a gain of N. This suggests that, at low offset frequencies, the noise contributed from the reference and the divider is increased by a factor of $20log_{10}N$ and passes to the PLL output. However, this noise is suppressed at high offset frequencies. Intuitively, at frequencies that are higher than the loop bandwidth, the loop is not fast enough to follow the input. As a result, the high frequency noise is attenuated. In addition, since the difference between the noise transfer function $H_{PD}(s)$ and $H_{in}(s)$ is only a factor of K_d, $H_{PD}(s)$ from the PD is also a low-pass transfer function.

The noise transfer function from the loop filter to the output, $H_{LF}(s)$, is typically a band-pass function. It is worthwhile to mention that $H_{LF}(s)$ is proportional to the VCO gain K_o. As a consequence, the noise contributed from the LF can be decreased by reducing the VCO gain.

Finally, the noise transfer function from the VCO to the output, $H_{VCO}(s)$, is a high-pass function. Intuitively, the VCO noise at low frequencies can be corrected

by the relatively fast feedback loop. However, the loop is not fast enough to correct any error at high frequencies, and hence, the high frequency noise passes to the PLL output.

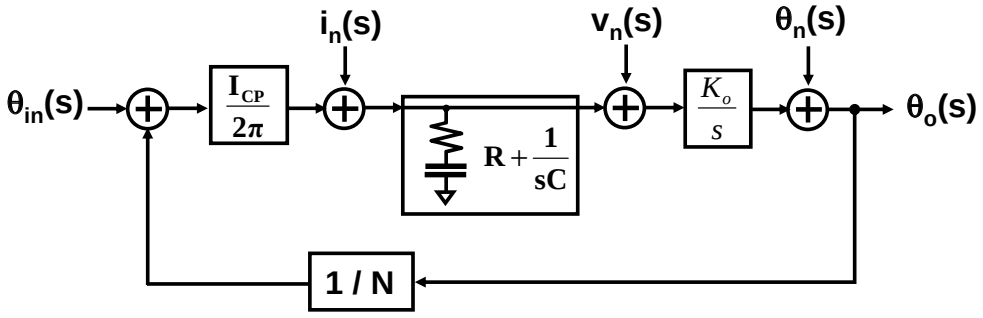


Figure 2.4: Liner model for a second-order CP PLL.

Next, consider a typical charge-pump PLL with a combination of the PFD and CP. To simplify the analysis, the loop filter is a first-order R-C filter. Thus the PLL becomes a second-order feedback loop. The corresponding linear model is shown in Fig. 2.4. Although typically a ripple capacitor is also connected on the control node to reduce the ripple and hence the reference sidebands, this ripple capacitor is commonly very small. Thus it only has a negligible impact on the analysis below. It can be shown that,

$$K_d = \frac{I_{CP}}{2\pi} \tag{2.7}$$

$$F(s) = R + \frac{1}{sC} = R(1 + \frac{1}{sRC}) = R(1 + \frac{\omega_z}{s}) \tag{2.8}$$

where ω_z is the zero of the open loop gain $G(s)$, and is given by

$$\omega_z = \frac{1}{RC} \tag{2.9}$$

From Eq. (2.2), the open loop gain $G(s)$ equals

$$G(s) = \frac{I_{CP}}{2\pi} R(1 + \frac{\omega_z}{s}) \frac{K_o}{s} \frac{1}{N} = \omega_c (1 + \frac{\omega_z}{s}) \frac{1}{s} \tag{2.10}$$

where ω_c is defined by Eq. (2.11). As will be shown shortly, ω_c is approximately the closed-loop bandwidth.

$$\omega_c = \frac{I_{CP}}{2\pi} R \cdot \frac{K_o}{N} \tag{2.11}$$

From (2.3) to (2.6), the noise transfer functions can be found to be

$$H_{in}(s) = \frac{\theta_o(s)}{\theta_i(s)} = N \frac{\omega_c(\omega_z + s)}{s^2 + \omega_c(\omega_z + s)} \tag{2.12}$$

$$H_{PD}(s) = \frac{\theta_o(s)}{i_n(s)} = \frac{RK_o(\omega_z + s)}{s^2 + \omega_c(\omega_z + s)} \tag{2.13}$$

$$H_{LF}(s) = \frac{\theta_o(s)}{v_n(s)} = \frac{K_o s}{s^2 + \omega_c(\omega_z + s)} \tag{2.14}$$

$$H_{VCO}(s) = \frac{\theta_o(s)}{\theta_n(s)} = \frac{s^2}{s^2 + \omega_c(\omega_z + s)} \tag{2.15}$$

Consider an example of a 2^{nd}-order PLL with design parameters listed in Ta-

Table 2.1: Example of PLL design parameters.

Output center frequency	2.0 GHz
Reference frequency	20 MHz
Division ratio N	100
CP current I_{CP}	0.1 mA
VCO gain K_o	2π·100 M rad/s/V
Loop Filter Resistor R	6.28 kΩ
Loop Filter Capacitor C	2.5 nF

ble 2.1. The noise transfer functions from each noise source can be calculated by using (2.12) to (2.15). Particularly, the noise transfer functions from the VCO, the input reference, and the LF are plotted in Fig. 2.5, respectively. As shown in the figure, $H_{VCO}(s)$ has a high-pass characteristic, $H_{in}(s)$ has a low-pass characteristic, and $H_{LF}(s)$ has a band-pass characteristic. Notice that if the ripple capacitor is added in the LF, the PLL becomes a 3^{rd}-order loop. At high frequencies, $H_{in}(s)$ would roll-off at -40 dB/decade rather than -20 dB/decade.

From Fig. 2.5, the -3dB bandwidth for $H_{VCO}(s)$ and $H_{in}(s)$ is coincident at the PLL closed-loop bandwidth (100 kHz approximately). To find the loop bandwidth, we need to consider the closed-loop transfer function $H(s)$. $H(s)$ is equivalent to $H_{in}(s)$, and given by

$$H(s) = H_{in}(s) = N\frac{2\xi\omega_n s + {\omega_n}^2}{s^2 + 2\xi\omega_n s + {\omega_n}^2} = N\frac{1 + \frac{s}{z_1}}{(1 + \frac{s}{p_1})(1 + \frac{s}{p_2})} \tag{2.16}$$

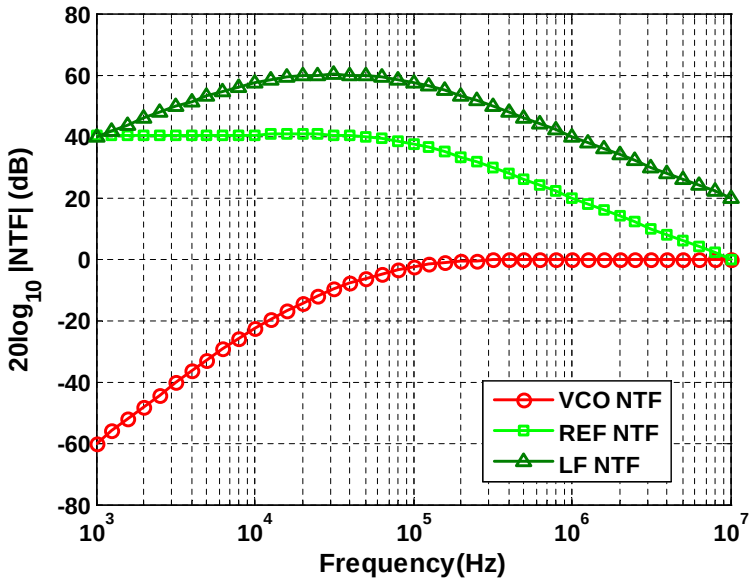


Figure 2.5: Noise transfer functions from VCO, REF, and LF to output.

where the natural frequency ω_n and the damping factor ξ are given by

$$\omega_n = \sqrt{\omega_c \omega_z}$$
$$\xi = \frac{\omega_c}{2\omega_n} \tag{2.17}$$

The corresponding closed-loop zero is z_1, and the poles are p_1 and p_2. For many applications, the PLL operates in the overdamped case where $\xi > 1$. Given this constraint, it can be shown that the zero z_1 will effectively cancel one of the poles, leaving the other pole to set the closed-loop bandwidth [6]. Interestingly, the closed-loop bandwidth is approximately equal to ω_c, and given by

$$\omega_{-3dB} \approx \omega_c = \frac{I_{CP}}{2\pi} R \cdot \frac{K_o}{N} \tag{2.18}$$

The loop bandwidth is a critical parameter in the design of PLLs. First of all, the loop bandwidth should be less than the reference frequency by a factor of 10 to guarantee loop stability. In addition, the loop bandwidth balances the trade-off between the in-band phase noise (e.g., contribution from the reference clock) and the out-of-band phase noise (contributed from the VCO). For a noisy VCO, a higher loop bandwidth would be desirable since the VCO noise within the bandwidth will be attenuated. On the other hand, when the reference clock is not clean compared to the VCO, a lower loop bandwidth would be desirable in order to filter the input noise from the reference clock. However, a small bandwidth would result in a slow transient response. The loop bandwidth calculation, therefore, must trade off the transient response and the total output phase noise. In order to achieve the best phase noise performance while maintaining loop stability and satisfying the settling time requirements, the loop bandwidth must be optimized.

To appreciate the importance of the PLL loop bandwidth, let us consider the previous PLL design example, where the division ratio N is 100. Also, assume that the VCO and the reference clock are the dominant sources of phase noise. The phase noise plots for the open-loop VCO and the reference clock are shown in Fig. 2.6(a), respectively. In the PLL, the in-band noise from the reference clock will be increased by a factor of $20log_{10}N$, or 40 dB. The figure also shows the increased reference noise after the division ratio N is taken into account. The optimum bandwidth should be determined at the frequency where the VCO phase noise and the increased reference phase noise cross each other. In this example, the optimum bandwidth is at 100 kHz. At this operating point, the overall phase

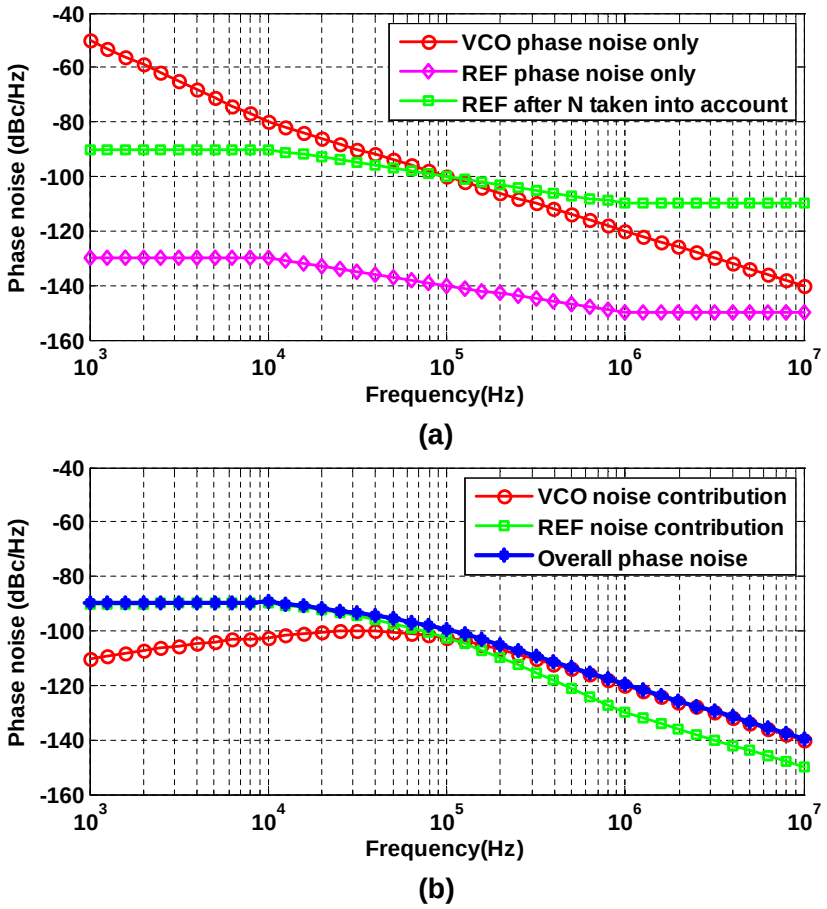


Figure 2.6: (a) Phase noise of VCO and REF input. To achieve minimum overall phase noise, the loop bandwidth should be set to 100 kHz. (b) Calculated phase noise using the design parameters in Table 2.1.

noise at the PLL output would be a minimum. A lower bandwidth or a higher bandwidth would result in more phase noise than the minimum value achievable. Recall the design example with the PLL parameters given in Table 2.1. The PLL loop bandwidth is approximately 100 kHz. Using the noise transfer functions for the VCO and the reference (Fig. 2.5), the overall phase noise can be calculated and

shown in Fig. 2.6(b). It is apparent that the reference noise is dominant within the loop bandwidth, while the VCO noise is dominant outside the loop bandwidth.

As seen from Eq. (2.18), the PLL loop bandwidth is proportional to the charge-pump current, the loop filter resistance, and the VCO gain. Given a designed VCO with a gain of K_o, the loop bandwidth can be set to the desired value by adjusting the charge-pump current I_{CP} and the loop filter resistor R. However, PVT variations may lead to uncertainties in the PLL parameters, for example, the VCO gain K_o. As a consequence, the loop bandwidth would deviate from the optimum, degrading the PLL phase noise performance. In order to maintain the optimum bandwidth, design techniques for an adaptive bandwidth PLL have been reported in [7, 8, 9], and have been summarized in [10].

2.2 Analog Techniques for PVT Tolerant PLLs

Adaptive bandwidth PLLs refer to a class of PLLs that scale their loop dynamics proportional to the reference frequency. In such PLLs, a constant ratio between the natural frequency ω_n and the reference frequency ω_{ref} is maintained. The damping factor ξ is also kept constant over PVT variations.

An adaptive bandwidth can be achieved by using self-biased technique [7, 9], where a symmetric load is used in a ring oscillator. The VCO output frequency ω_{VCO} is inversely proportional to the symmetric load resistance R_{sym}. R_{sym} can be approximated to $1/g_m$, where g_m is the small signal transconductance of the

symmetric load transistor. Hence,

$$\omega_{ref} = \frac{\omega_{VCO}}{N} \propto \frac{g_m}{N} \propto \frac{\sqrt{I_B}}{N} \tag{2.19}$$

where I_B is the VCO bias current. From Eq. (2.17),

$$\begin{aligned} \frac{\omega_n}{\omega_{ref}} &\propto \sqrt{\frac{I_{CP}}{I_B} N \frac{K_o}{C}} \\ \xi = \frac{1}{2} RC\omega_n \propto RC\omega_{ref} &\propto \frac{Rg_m}{N} C \end{aligned} \tag{2.20}$$

For the VCO with a symmetric load, the gain K_o is nearly a constant. Assuming the loop filter capacitor C is also fixed, then the requirements for an adaptive bandwidth PLL can be found to be

$$\begin{aligned} I_{CP} &\propto \frac{I_B}{N} \\ R &\propto \frac{N}{g_m} \end{aligned} \tag{2.21}$$

To realize Eq. (2.21), the charge-pump current I_{CP} is scaled with the VCO bias current I_B, and is generated by a programmable $1/N$ current mirror [9]. To produce a proper resistance R, in the loop filter proportional path, the self-biased PLL uses a $1/g_m$ resistance from the VCO bias generator. Additionally, the dependence of R on the division ratio N is implemented by using a sampled feedforward filter, which holds the sampled error charge for the entire reference cycle [9]. Moreover, the sampled loop filter also reduces the reference sidebands due to the ripple on

the control node, similar to [11].

An alternative technique for an adaptive bandwidth PLL is the regulated supply technique [8], where similar design principles are applied. However, both the self-biased technique and the regulated supply technique rely on the fact that the large-signal resistance R_{sym} is inversely proportional to the small-signal transconductance g_m. As shown in [10], this assumption is only valid when the VCO voltage swing is sufficiently larger than the transistor threshold voltage V_T. When the voltage swing approaches V_T, both the ratio of ω_n to ω_{ref} and the damping factor ξ would change. Since the V_{DD} to V_T ratio decreases with CMOS technology scaling, this poses a challenge for future adaptive bandwidth PLL designs. In [10], the authors suggested the use of zero-threshold voltage devices for the symmetric load to mitigate this problem. However, this approach would be limited by the available process.

A current-mode loop filter [12] has also been implemented for an adaptive bandwidth PLL. The current-mode filter drives a current controlled oscillator (ICO). The charge-pump current I_{CP} is scaled with the control current of the ICO. This technique resulted in a simpler circuit and robust performance to PVT variations and division ratio.

All the above techniques were implemented with ring oscillators. For an LC-VCO based PLL, the loop bandwidth may vary substantially due to the variations in the VCO gain K_o under PVT conditions. To achieve the best phase noise performance, the loop bandwidth has to be optimized. One approach to achieving the optimum loop bandwidth is on-chip calibration [13]. The open-loop gain was

determined by measuring the settling behavior. To compensate for the variations in K_o, the charge-pump current I_{CP} was adjusted according to the measured settling time.

It has been demonstrated that the PLL design parameters have a strong impact on the achieved jitter performance [14]. Background calibration can aid the design of PLLs to achieve minimum jitter [15]. By monitoring the output timing jitter on-chip, PLL parameters, such as the charge-pump current I_{CP} and the loop filter components, can be trimmed to optimum values.

Decreasing the VCO gain K_o reduces the control node sensitivity, thereby reducing the noise contributions from the CP and the LF. The reference spurs can also be reduced, as implied by Eq. (2.22) [16].

$$\frac{A_{spur}}{A_{carrier}} = \frac{1}{2}\frac{K_o V_m}{\omega_{ref}} \tag{2.22}$$

where A_{spur} and $A_{carrier}$ are the amplitude for the reference spur and carrier, respectively, and V_m is the amplitude of the ripple (assuming a sinusoidal waveform) on the control node. To ensure a small K_o and to cover a wide tuning range, a digital band-switching technique is widely used. To find the proper tuning curve that contains the target center frequency, a robust search algorithm is required to overcome the PVT variations. Many calibration algorithms have been developed, for instance, [16] for an LC-VCO and [17] for a ring VCO.

2.3 Digital Techniques for PVT Tolerant PLLs

Unlike analog circuits, digital circuits are tolerant to PVT variations. Intuitively, analog PLLs can be replaced with inherently PVT insensitive digital counterparts. Early digital PLLs (DPLLs) [18] were designed for clock generation in a microprocessor. Recently, DPLLs have received increased attention and have been developed for a wide variety of applications in the multi-GHz frequency range, such as clock generation [19, 20, 21], clock recovery [22, 23], and wireless transceivers [24]. For future sub-100nm CMOS processes, DPLLs have promising advantages over the traditional analog PLL. These include the inherent tolerance to PVT variations, the immunity to supply and substrate noise, and the ease of scaling with process. In addition, DPLLs are predictable, programmable, and adaptable, making the design period for DPLLs much shorter than their analog counterparts.

A typical block diagram of a state-of-the-art DPLL is shown in Fig. 2.7. The loop filter is a pure digital loop filter. It drives a digitally controlled analog oscillator (DCAO) via a digital control word. The VCO output is fed back to the PFD through a divider as in the analog PLL. The phase error from the PFD is converted to a digital word for the digital loop filter by using a time-to-digital converter (TDC).

Because the digital loop filter is scalable with process and has no leakage issue, it provides many benefits over the traditional analog loop filter. In contrast, the design of an analog loop filter must trade off between performance and die area. A high performance PLL frequency synthesizer has a stringent requirement on the

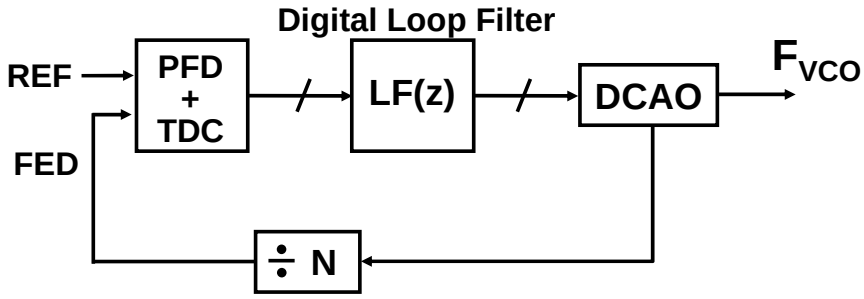


Figure 2.7: Block diagram of a digital PLL.

level of reference spurs. The leakage in the PLL loop filter is the main cause of reference spurs. To improve the leakage problem, a metal-insulator-metal capacitor has to be used for the integrator capacitor. This not only occupies a significant die area, but is also difficult to scale with process[1]. In applications where there are constraints on the die area, a MOS capacitor can be used for the loop filter at the cost of high leakage current. However, the leakage from a MOS transistor would be even worse in future processes and the analog PLL may not be functional.

Although most building blocks in a DPLL are inherently digital circuits, there are two exceptions. First, DCAOs continue to be analog blocks. The input of the DCAOs is a digital word rather than an analog voltage or current, but the output is essentially an analog clock signal. Second, most TDCs have a resolution that is determined by the minimum gate delay time, which is again PVT sensitive. As a consequence, both the DCAO and the TDC are not tolerant to PVT variations, and hence, they are becoming the bottlenecks in the design of future high-performance PLLs.

[1]A capacitor is defined according to its vertical dimension, which is more difficult to scale than the lateral dimension.

On-chip calibration has also been widely employed in DPLLs. For example, by calibrating the DCAO digital setting with respect to the TDC delay in a start-up normalization procedure, an adaptive loop bandwidth can be achieved in a DPLL [19]. To compensate for the gain variations in an LC-VCO, a gain estimation technique was proposed in [25]. This approach is very similar to the open-loop gain calibration technique [13] in an analog frequency synthesizer. However, the implementation of a similar calibration algorithm is much simpler in digital PLLs than their analog counterparts.

Because PLL phase noise (or jitter) performance and power consumption are highly dependent on the VCO, the VCO design is the most critical part in the design of high performance PLLs. Since DCAOs are essentially analog oscillators, they are the fundamental bottlenecks in the design of DPLLs. In the context of ring oscillators, supply noise is a major design concern. Conventional techniques that employ supply regulation are not preferred in the design of low-voltage VCOs. Chapter 3 describes an on-chip calibration technique for reducing supply voltage sensitivity in ring VCOs. In the context of LC-based oscillators, LC-VCO gain K_o varies substantially, This results in PLL loop bandwidth variations with the operating frequency, which may lead to significant performance degradation. To maintain a constant loop bandwidth, Chapter 4 presents a new PLL frequency synthesizer that achieves a constant loop bandwidth over a wide frequency tuning range.

2.4 Summary

The linear model of a charge-pump PLL and its noise analysis are presented in this chapter. Since timing jitter can be obtained from phase noise, PLL phase noise is analyzed in detail. Based on the derived noise transfer functions, the phase noise contribution from each noise source can be calculated. To achieve the minimum overall phase noise, the closed-loop bandwidth must be optimized. It is also desirable to make the optimum bandwidth setting robust to PVT variations and scalable with the reference frequency. The requirements for an adaptive loop bandwidth are derived. A number of proposed techniques for achieving adaptive bandwidth are surveyed. Digital PLLs are promising solutions to overcome PVT variations. However, the DCAOs continue to be analog and hence, they are becoming one of the bottlenecks in the design of high performance PLLs. Finally, to make PLLs tolerant to PVT variations, on-chip calibration is extensively used for both analog and digital PLLs.

Chapter 3 – On-Chip Calibration for Reducing Supply Sensitivity in Ring VCOs

As introduced in the last chapter, supply noise is a major design concern for ring oscillators as the oscillation frequency of a ring VCO is highly dependent on the supply voltage. To suppress the change in frequency of a ring VCO with supply noise, traditional methods employ voltage regulators [8, 26, 27] at the cost of reduced voltage headroom. However, with the scaling down of supply voltages, the lowered voltage swings make supply regulated ring oscillator based PLL designs difficult. For the design of ring VCOs and PLLs at 1V supply, alternative techniques ought to be considered.

One of these alternative techniques employs compensation [28]. However, due to process variations and the dependence of the compensation on the oscillation frequency, it is practically impossible to achieve accurate compensation. Since process variations continue to increase as CMOS technology scales down, adaptive compensation techniques are required.

This chapter describes one such technique [29] for reducing the supply voltage sensitivity in ring oscillators. The chapter is organized as follows. An adaptive supply compensation technique using on-chip calibration is described in Section 3.1. Section 3.2 presents the proposed on-chip calibration algorithm and circuits. This

is followed by measurement results in Section 3.3. Section 3.4 discusses the impact of temperature variations on the new calibration technique and presents an enhanced scheme for making the design tolerant to temperature variations.

3.1 Supply Compensation Technique

Conventional Ring VCO

Consider a conventional ring oscillator based PLL with a 4-stage ring VCO, as shown in Fig. 3.1. The commonly used Lee-Kim delay cell [30] is employed in this VCO. Like most ring VCOs, the frequency is tuned by controlling the pMOS transistors. In particular, the gates of the two pMOS transistors M_{p1} and M_{p2} are controlled. To minimize supply noise coupling, the PLL loop filter is connected to V_{DD} instead of ground, thus the V_{GS} of the pMOS transistors is fixed. However, the V_{DS} of the pMOS transistors varies with a variation in the supply voltage, causing the current in the delay cell to change. An increase in the supply voltage leads to an increase in the current hence an increase in the oscillation frequency. On the other hand, since the VCO outputs swing from rail-to-rail, an increase in the supply voltage results in an increased swing hence a lowered speed. As a result, while the first is dominant, the VCO suffers from supply noise due to these two opposing effects.

To evaluate the supply noise immunity, supply voltage sensitivity is commonly used [28]. This sensitivity is defined by a percentage change in the oscillation

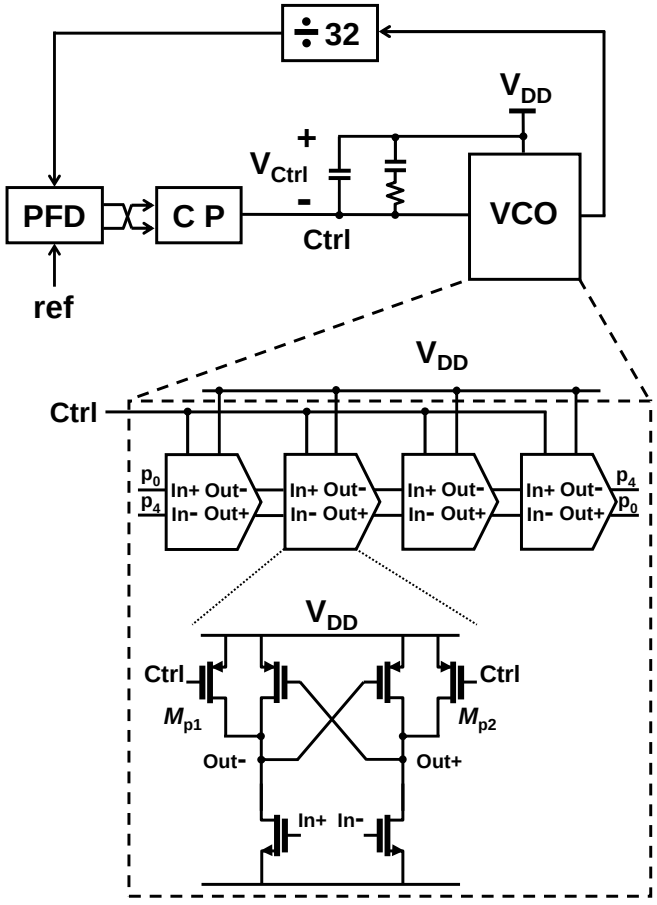


Figure 3.1: Conventional ring oscillator based PLL.

frequency to a percentage change in the supply voltage, i.e., $\partial f_{VCO}(\%)/\partial V_{DD}(\%)$. Fig. 3.2 shows the simulated supply voltage sensitivity of the ring VCO in Fig. 3.1 for operating frequencies from 600 MHz to 2 GHz. The simulations have been performed at different process corners. As shown in the figure, the supply sensitivity decreases with an increase in the operating frequency. Moreover, at the highest operating frequency, the supply sensitivity even falls below zero to a negative value.

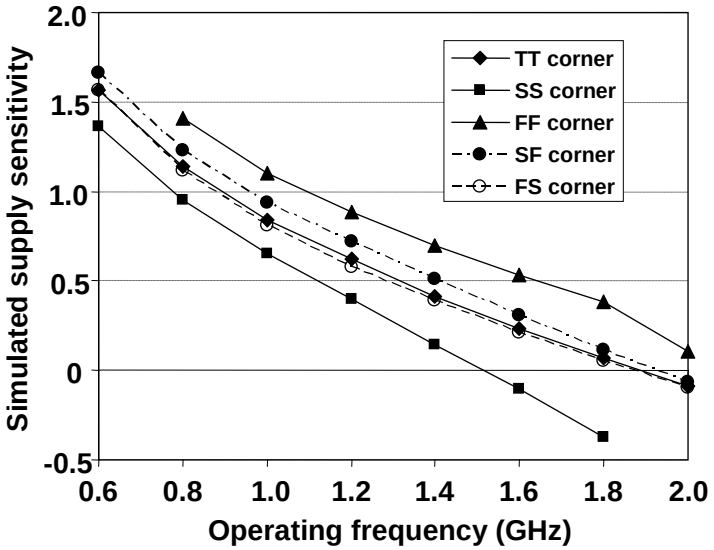


Figure 3.2: Simulated VCO supply sensitivity for different process corners.

Supply Compensation Technique

Since the VCO has a positive supply voltage sensitivity for most operating frequencies, adding a compensation circuitry with a negative supply voltage sensitivity can reduce the total sensitivity. The concept of supply compensation is illustrated in Fig. 3.3, where V_1, V_2, and V_3 are three different supply voltages. The VCO supply is V_2 under typical operating conditions. The dotted and dashed lines correspond to the positive sensitivity due to the ring VCO and a negative sensitivity due to the compensation circuitry, respectively. If both are properly combined, the dependence of the oscillation frequency f_{VCO} on the supply voltage would be cancelled, leading to a reduced supply voltage sensitivity.

At a given operating frequency, the goal of the compensation scheme is to

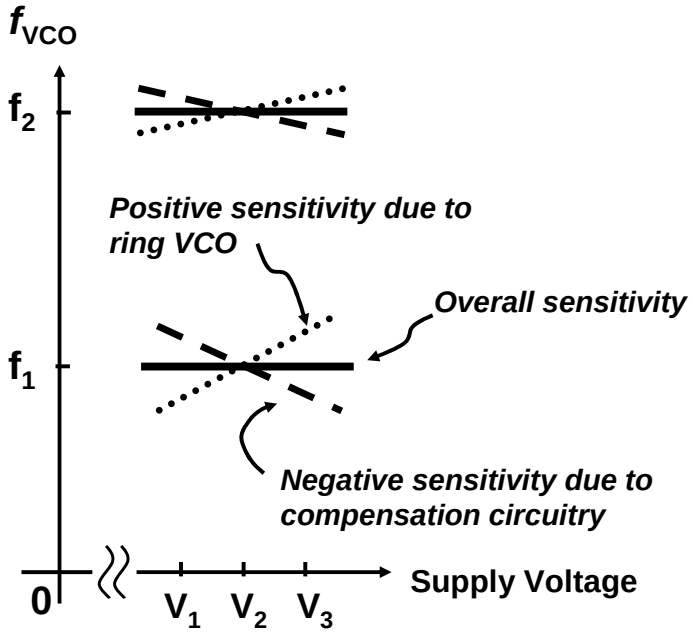


Figure 3.3: Concept of supply sensitivity compensation. V_1, V_2, and V_3 are three different supply voltages; the VCO supply is V_2 under typical operating conditions. The VCO has a larger sensitivity at a lower frequency f_1 compared with f_2. To provide an optimum compensation at each operating frequency, the negative sensitivity due to a compensation circuitry needs to be controlled.

make the oscillation frequency insensitive to supply voltage for voltages V_1 to V_3. As indicated in Fig. 3.2, due to the dependence of the VCO supply sensitivity on the operating frequency, the negative sensitivity due to the compensation scheme should be adjusted for different frequencies. Specifically, since the VCO has a larger sensitivity at a lower frequency f_1 compared with f_2 (Fig. 3.3), the added negative sensitivity at f_2 should be smaller. To provide an optimum compensation for the supply voltage sensitivity at each operating frequency, the compensation circuitry needs to be appropriately adjusted.

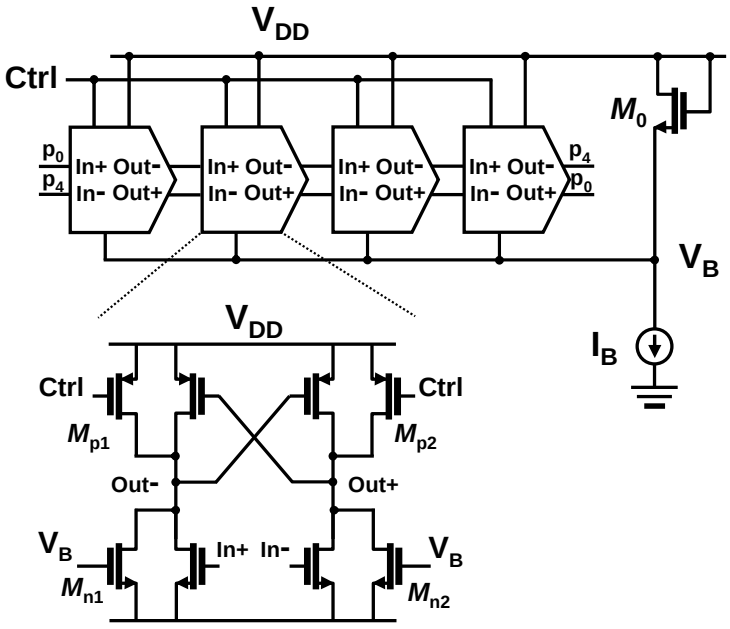


Figure 3.4: VCO with the proposed compensation circuitry. The nMOS transistors M_{n1} and M_{n2} compensates for the changes in oscillation frequency due to supply variations. The magnitude of the compensation is controlled by the current I_B.

The compensation circuitry proposed is shown in Fig. 3.4. Based on the Lee-Kim delay cell, transistors M_{n1} and M_{n2} have been added between the output nodes and ground. The gates of M_{n1} and M_{n2} are connected to the diode connected nMOS transistor M_0 (node V_B), which is biased by a programmable current I_B. When the supply voltage increases, the current in the pMOS transistors increases. The voltage V_B also increases due to M_0, causing M_{n1} and M_{n2} to sink more current to ground. This mechanism slows the oscillator and thus compensates for the increase in the oscillation frequency due to an increase in the VCO supply voltage. If the increase in the currents of M_{n1} and M_{n2} is the same as the increase in the currents

of the pMOS transistors, the VCO would maintain the same oscillation frequency. The VCO supply sensitivity would be effectively reduced to zero.

The magnitude of the negative sensitivity is controlled by the bias current I_B. For each operating frequency, a corresponding current I_B needs to be determined to achieve the optimum compensation.

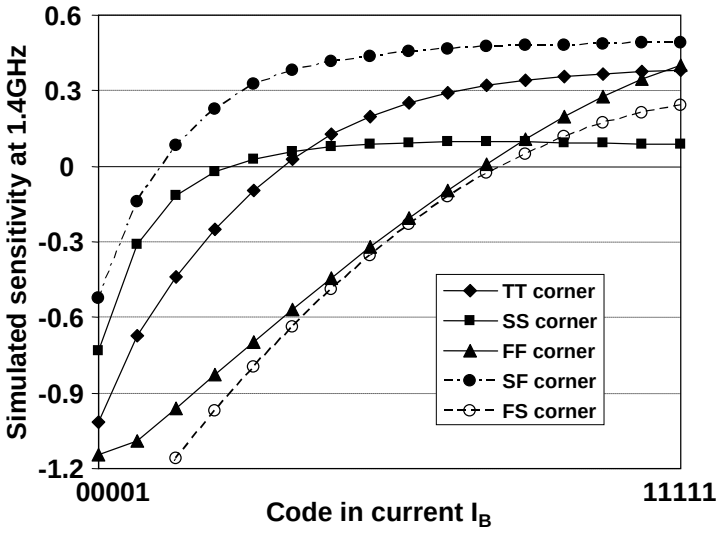


Figure 3.5: Simulated VCO supply sensitivity with proposed compensation circuitry for different process corners.

As an example, consider the VCO operating at 1.4 GHz. The simulated overall sensitivity of the VCO with the compensation circuitry is shown in Fig. 3.5. The current I_B is digitally controlled by a 5-bit word. The code "11111" corresponds to a conventional VCO without the compensation circuitry. As expected, the sensitivity increases with an increase in the bias current I_B. The optimum code for I_B is obtained when the sensitivity is reduced to zero. As shown in Fig. 3.5, the optimum code varies with process variations and cannot be determined a priori.

Therefore, an on-chip calibration is needed to ensure optimum compensation under process variations.

3.2 Calibration Algorithm and Circuit

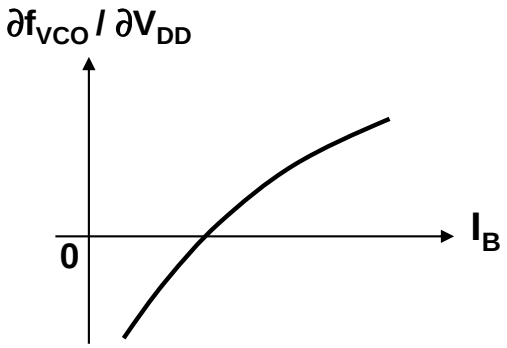


Figure 3.6: Relationship between the supply voltage sensitivity and I_B.

The simulation results of Fig. 3.5 are simplified for illustration purposes in Fig. 3.6. The relationship between the overall supply voltage sensitivity and the current I_B is shown in the figure. Our calibration algorithm uses a binary search based on this relationship. The flowchart of the algorithm is given in Fig. 3.7. The procedure starts by "10000" reset, and the algorithm determines all five bits in I_B in five calibration cycles. In each calibration cycle, the polarity of the supply voltage sensitivity is measured. This is performed by comparing the oscillation frequencies for two different supply voltages V_1 and V_3 (Fig. 3.3). If the VCO runs faster for the higher supply voltage V_3 than at V_1 ($f_{OSC}|_{V3} > f_{OSC}|_{V1}$), the supply sensitivity measured is positive, hence, the current I_B should be decreased.

Conversely, when $f_{OSC}|_{V3} < f_{OSC}|_{V1}$, I_B should be increased. This trimming procedure is continued from the MSB to the LSB until all five calibration cycles are completed, and thus the equilibrium ($f_{OSC}|_{V3} \approx f_{OSC}|_{V1}$) is reached to the LSB precision. Next, the supply voltage V_2 is used for the VCO. Since V_2 is in between V_1 and V_3, this provides a VCO supply voltage sensitivity that is closer to zero.

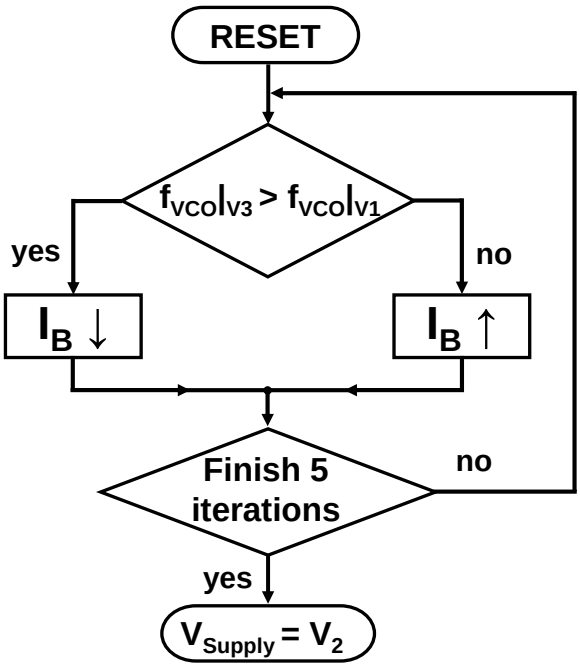
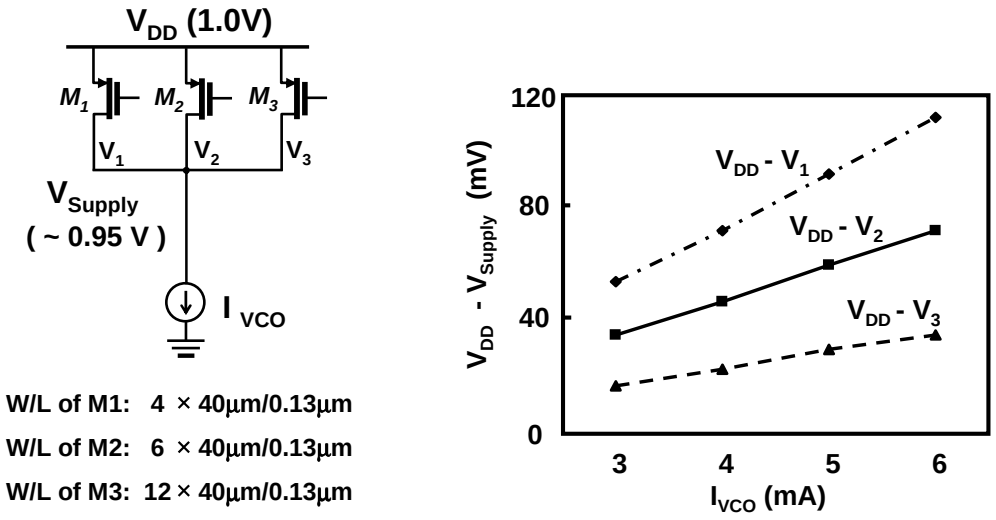


Figure 3.7: Flowchart of the proposed calibration algorithm.

Circuits

To implement the above algorithm, a variable supply voltage is needed to measure the supply sensitivity. As shown in Fig. 3.8(a), three pMOS transistors with



(a) (b)

Figure 3.8: (a) pMOS transistors in series with V_{DD} are used to vary the supply voltage. (b) Comparison of the simulated voltage drops with different settings of the VCO supply voltages.

different sizes have been inserted in series between V_{DD} and the supply node of the VCO. The three pMOS transistors operating in the triode region have nominal series resistance values of 18, 12, and 6 ohms. By turning on one of the transistors M_1, M_2, and M_3, different supply voltages V_1, V_2, and V_3 can be provided to the oscillator. Fig. 3.8(b) summarizes the simulated voltage drops between V_{DD} and the three possible supply voltages. The reductions in the voltage headroom are small. Furthermore, the series resistance provides a small amount of supply isolation.

The simplified schematic of the resulting VCO is shown in Fig. 3.9. It incorporates dual-delay paths [31] to extend the frequency range for low supply voltage

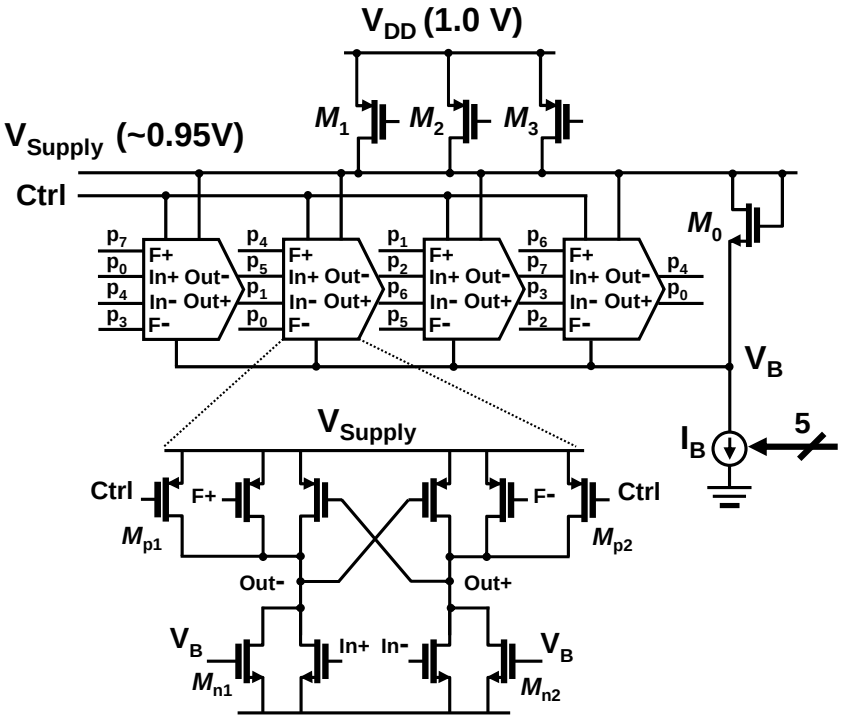


Figure 3.9: Final VCO schematic.

operation. For a typical supply voltage V_2, since the transistor M_2 operates in the triode region, the reduction in voltage headroom (from V_{DD} to V_{Supply}) is about 50 mV. Further reduction is also feasible.

Next we need to address how the VCO oscillation frequencies are compared for different supply voltages. In a PLL, the VCO output frequency is corrected by the feedback loop to lock to the reference frequency. When the supply voltage changes from V_3 to V_1, the VCO output frequency does not settle to a new value but the control voltage V_{Ctrl} does. Conceptually it is possible that the previous value of V_{Ctrl} can be stored on a capacitor and the change of V_{Ctrl} can be detected

by using a high precision comparator. Based on this change (either an increase or a decrease), the code in I_B can be determined via a successive approximation register (SAR). This is illustrated in Fig. 3.10. This scheme can be easily implemented in a digital PLL, since the control word (voltage for an analog PLL) is digital and is easily compared. In an analog PLL, however, it requires a very high precision comparator because the VCO has a large gain which is typically about 4GHz/V. An observed change in the oscillation frequency can lead to a less than 1mV change in V_{Ctrl}. Virtually an offset free comparator would be required.

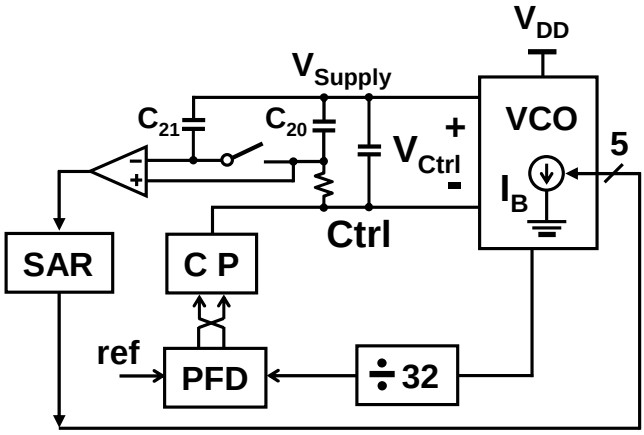
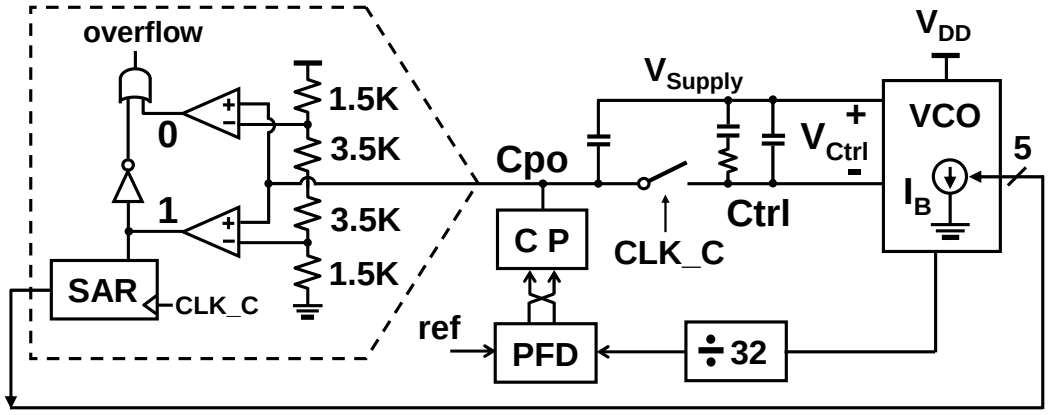
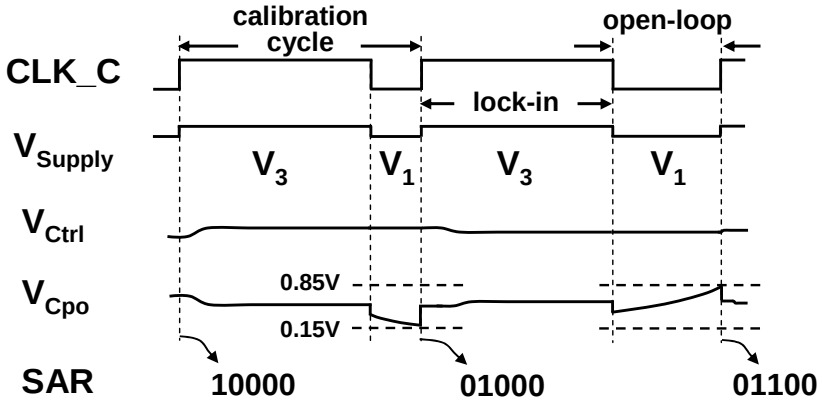


Figure 3.10: Schematic of PLL with calibration.

To eliminate the need for a good comparator, an open loop scheme is proposed and has been implemented in our prototype chip. The schematic of the PLL including the calibration circuitry is shown in Fig. 3.11(a). Fig. 3.11(b) shows the timing diagram. Each calibration cycle consists of lock-in and open-loop phases. To provide an open-loop, a CMOS switch has been added between the CP and the



(a)



(b)

Figure 3.11: (a) Schematic of the implemented PLL with calibration. (b) Timing diagram.

loop filter. The charge injection of the switch is negligible, since the capacitance of the switch is much smaller than that of the loop filter. In the lock-in phase, the supply voltage V_3 is used for the VCO. The signal CLK_C is kept "1" for a time

period of $2^6/f_{ref}$ to ensure that the PLL settles, where f_{ref} is the reference clock frequency. In the following open-loop phase, the VCO supply voltage is changed to V_1 and CLK_C breaks the loop. Because V_{Ctrl} does not change, the free-running VCO oscillation frequency changes only due to the change in the supply voltage. This frequency change is observed at the output of the CP, causing the output V_{CPO} to significantly increase or decrease. The CP output is fed to two comparators. The voltage V_{CPO} continues to either increase or decrease until it causes one output of the comparators to flip, which triggers an overflow signal to complete the open-loop phase. The open-loop phase also terminates if none of the comparators trigger within the time period of $2^6/f_{ref}$. At the end of the open-loop phase, the current bit of the SAR is determined and the next significant bit is preset to "1". This calibration cycle starts with the MSB and is repeated until all five bits have been determined.

Ground Noise

Most supply regulated PLLs only reduce supply noise. However, ground noise can be equally important in deep-submicron CMOS process. Adding decoupling capacitors between V_{DD} and ground can attenuate ground noise at the cost of die area. A differential supply regulated design [27] suppresses the ground noise with a reduced headroom in the ground rail.

Although the proposed VCO and the calibration technique have been designed to reduce the supply noise, ground noise is also reduced at no additional cost. In

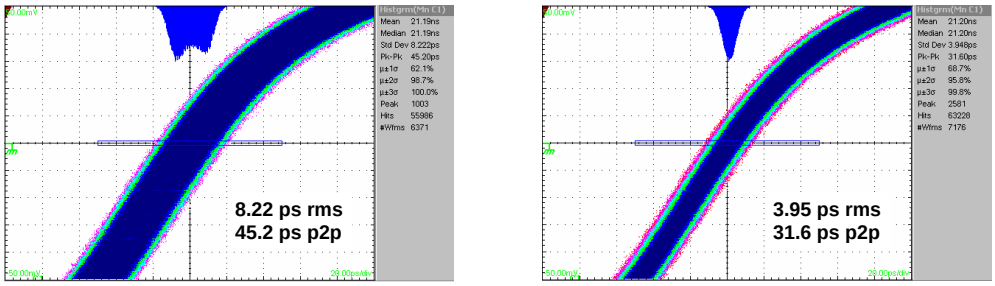
Fig. 3.9, assume that there is a decrease in the voltage on the ground node. As a result, the common mode of the VCO delay cell outputs also reduces by the same amount. The increase in the currents of the pMOS transistors due to an increase in V_{DS} is the same as the increase in the currents of the nMOS transistors M_{n1} and M_{n2} due to an increase in V_{GS}. This condition is exactly the same as when the supply voltage changes, and it is compensated for by the same on-chip calibration. Another way of looking at why the ground noise is also suppressed is because our proposed supply noise compensation is built within the oscillator itself. It does not distinguish between the positive or the negative supplies, unlike supply regulation based techniques. This is an important advantage of our technique over the traditional supply regulated PLL designs.

3.3 Measurement Results

The proposed PLL with the calibration circuitry (Fig. 3.11) has been fabricated in a 0.13-μm CMOS process. To evaluate the supply noise suppression, the PLL performance was measured in the presence of VCO supply noise[1]. A 10 mV noise tone was added to the V_{DD} of the VCO at different modulation frequencies. At an operating frequency of 1.4GHz, the on-chip auto-calibration circuit converges to the code "01001", whereas the conventional VCO design is equivalent to using the code "11111". Fig. 3.12(a) and Fig. 3.12(b) show the measured PLL jitter histograms of the conventional PLL and the proposed PLL with calibration, respectively, at a

[1]The supply sensitivity can not be measured since the control node was not brought out in the prototype chip.

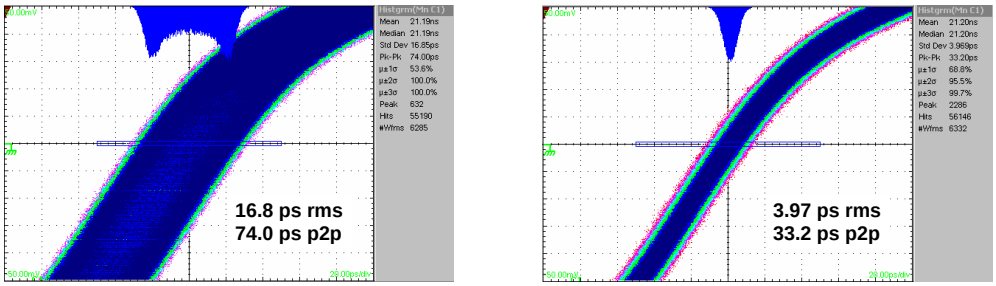
1 MHz modulation frequency. The measured rms jitter is improved from 8.22 ps to 3.95 ps, and the peak-to-peak jitter improved from 45.2 ps to 31.6 ps. Fig. 3.13(a) and Fig. 3.13(b) compare the jitter histograms of the conventional design and the proposed design at a 10 MHz modulation frequency. The measured rms and peak-to-peak jitter are improved from 16.8 ps to 3.97 ps and from 74.0 ps to 33.2 ps, respectively.



(a) (b)

Figure 3.12: Measured jitter histogram for a 1 MHz modulation frequency. (a) Conventional VCO. (b) Proposed VCO with calibration.

The measured performance is shown in Fig. 3.14 for a range of modulation frequencies. Since the noise tone at the VCO supply is band-pass filtered by the PLL, the conventional design exhibits a bell-shaped curve. The curve is flattened by the VCO, indicating that the proposed VCO with on-chip calibration suppresses the supply noise for any supply modulation frequency. The VCO consumes 5.4 mA (including I_B), which reflects a 23% overhead compared to the conventional VCO (measured at code "11111" excluding I_B for a fair comparison). Other circuits in the PLL draw 4.2 mA from the 1 V supply.



(a) (b)

Figure 3.13: Measured jitter histogram for a 10 MHz modulation frequency. (a) Conventional VCO. (b) Proposed VCO with calibration.

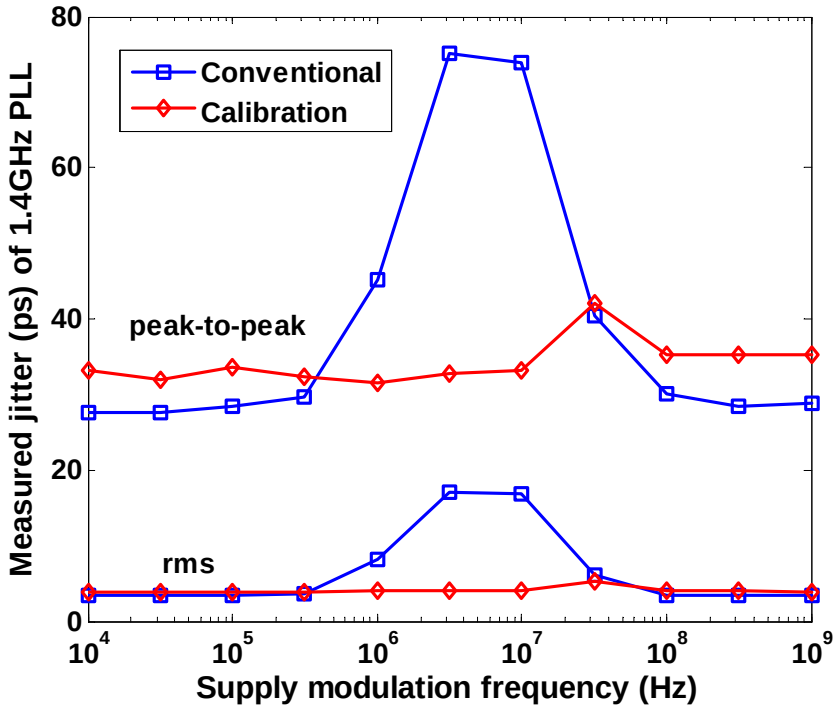


Figure 3.14: Measured jitter with supply modulation frequency.

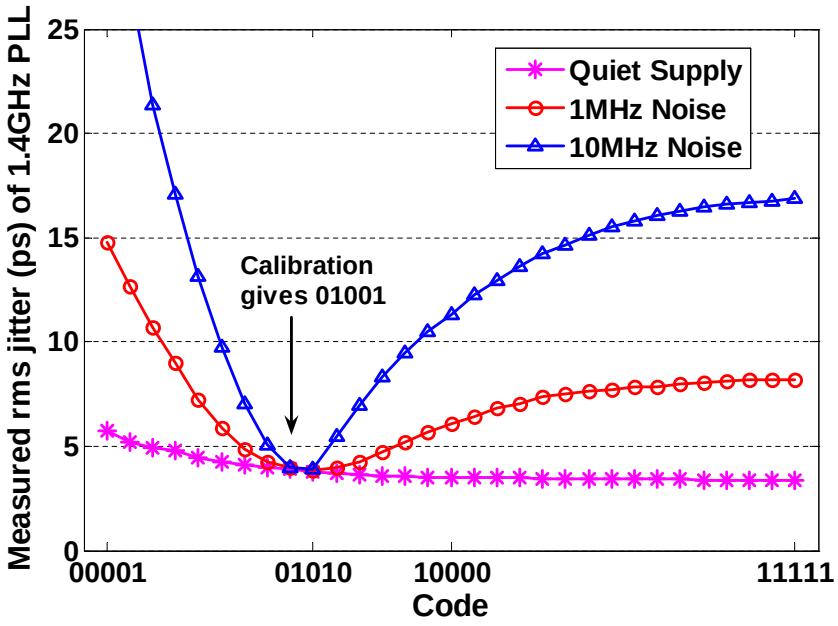
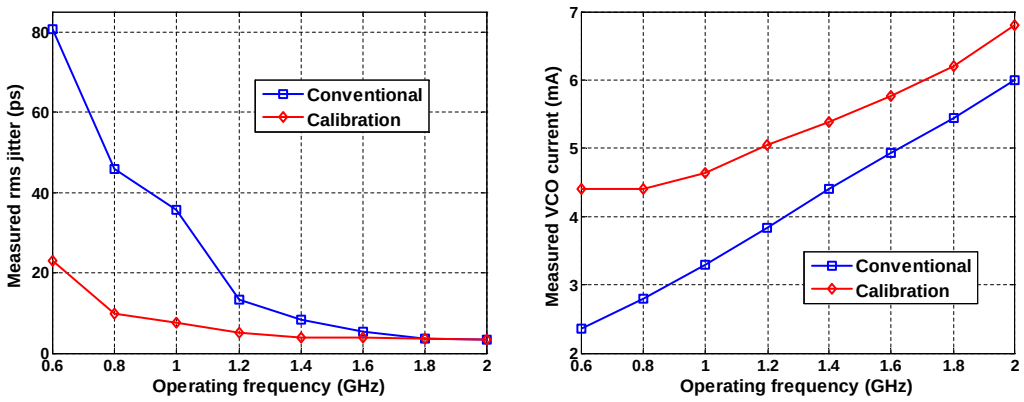


Figure 3.15: Measured rms jitter of 1.4 GHz PLL.

The SAR can be also controlled manually for evaluation purposes. The measured rms jitter of the PLL versus a 5-bit word control for I_B at 1.4 GHz operation is shown in Fig. 3.15. The optimum code (i.e., the best performance) that is manually reached at 1 MHz modulation frequency is "01010". The on-chip auto-calibration circuit converges to a code with only one bit offset. As seen from Fig. 3.15, the overall jitter performance could be modestly improved even when the VCO is compensated with a fixed code (e.g., a digital code of "10000"). However, a fixed compensation would be highly susceptible to process variations. Hence, the resulting performance would fall short of the desired optimum that can be reached via an automatic calibration. With a quiet supply, the measured rms jitter increases with a decrease in the code for two reasons. Adding the transistors

M_{n1} and M_{n2} in the proposed VCO delay cell (Fig. 3.9) degrades the phase noise performance. Simulation results indicate that, depending on the code, the phase noise is worse by up to 3 dB at 1 MHz offset. Secondly, the VCO gain K_{VCO} increases with a decrease in the code, leading to an increased jitter as well. Note that the PLL loop bandwidth is kept roughly the same for each code by changing the CP current in order to evenly maintain the impact on performance due to the PLL loop bandwidth.



(a) (b)

Figure 3.16: Comparisons of measured (a) performance, and (b) VCO current consumption.

The proposed PLL demonstrates robust performance against VCO supply noise over the full operating frequency range from 0.5 GHz to 2 GHz. With a 1 MHz modulation frequency, the measured PLL rms jitter for the conventional design and the proposed design is compared in Fig. 3.16(a). The proposed VCO with the help of calibration improves the VCO robustness to the supply noise significantly.

The overhead in power consumption is indicated in Fig. 3.16(b). In particular, for a lower operating frequency, the performance improves more significantly, and with a larger power overhead.

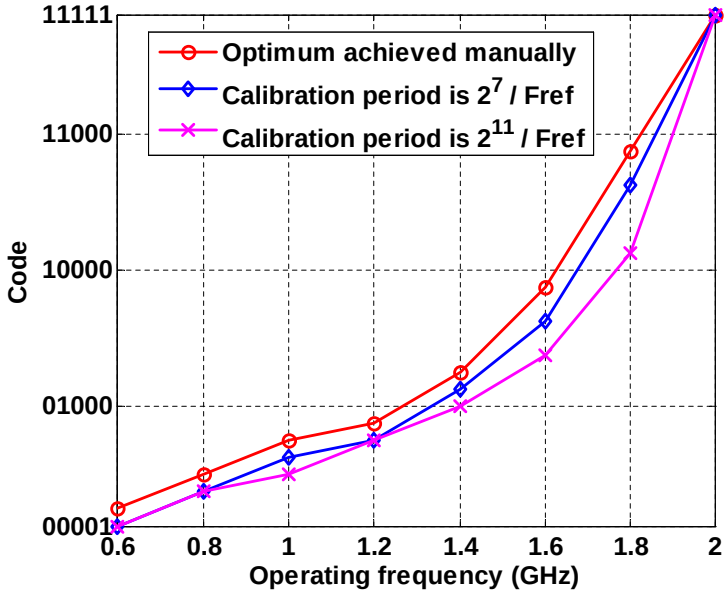


Figure 3.17: Comparison between the optimum code and the calibrated code.

Fig. 3.17 shows the comparison between the code given by the on-chip calibration and the optimum code that is reached manually. The code increases with an increase in the operating frequency and converges to "11111" at the highest frequency. As suggested in Fig. 3.2, at a lower frequency a larger compensation is needed, but no compensation is necessary at the highest frequency since the VCO sensitivity is negative. Compared with the optimum code, the on-chip calibration yields a negative offset of 1 or 2 LSBs. The error becomes larger when the calibration period is increased from $2^7/f_{ref}$ to $2^{11}/f_{ref}$. We suspect that this

error is mainly due to the leakage in the PLL loop filter. In our implementation, a pMOS capacitor is used for the loop filter in order to reduce die area. To reduce the leakage, a thick oxide MOS capacitor or a metal capacitor can be employed. Furthermore, the leakage problem can be eliminated if the proposed VCO and calibration technique are integrated in a digital PLL where the loop filter is purely digital.

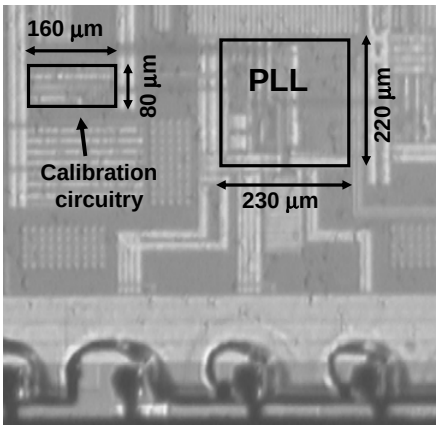


Figure 3.18: Die photo of PLL with calibration circuitry.

The die photo of the prototype chip is shown in Fig. 3.18[2]. The core areas of the PLL and the calibration circuitry are 0.051 mm^2 (230 μm $\times$ 220 μm) and 0.013 mm^2 (160 μm $\times$ 80 μm), respectively. The pMOS transistors M_1, M_2, and M_3 (Fig. 3.9) occupy a negligible amount of die area. Table 3.1 summarizes the performance of the proposed VCO and PLL with on-chip calibration.

[2]Unlike in the prototype chip, the PLL and calibration circuitry should be laid out close to each other to minimize the length of the control line.

Table 3.1: Performance summary.

Technology	0.13-μm CMOS
Supply voltage	1.0 V
Frequency range	0.5-2.0 GHz
Die area (PLL core) Die area (calibration circuitry)	0.051 mm^2 0.013 mm^2
Power dissipation (1.4 GHz)	9.6 mW
Loop bandwidth at (1.4 GHz)	3 MHz
Jitter with clean VCO supply Jitter with a 10 mV, 1 MHz supply noise Jitter with a 10 mV, 10 MHz supply noise	3.90 ps rms (1.4 GHz) 3.95 ps rms (1.4 GHz) 3.97 ps rms (1.4 GHz)

3.4 Discussion

We now consider the impact of temperature variations on our calibration technique. A large change in temperature affects transistor threshold voltages significantly. An increase in the temperature causes the threshold voltage to reduce. As a consequence, both the voltage V_B and the currents in M_{n1} and M_{n2} increase (Fig. 3.9), leading to an over compensation. Thus the relationship between the VCO supply sensitivity and I_B (Fig. 3.6) is shifted to the right for high temperatures. Fig. 3.19 shows the simulated VCO sensitivities as the temperature varies from 27 °C to 120 °C. The optimum code has been changed by 8 LSBs, which can significantly impair the PLL performance. To ensure an optimum compensation over temperature variations, the VCO should be calibrated periodically.

Fig. 3.20 compares the measured jitter between 22 °C and 90 °C[3] in the presence of a 1 MHz supply noise. As expected, the curve is shifted to the right for a

[3]A 104A-1 thermo probe was used in the measurement. However, the on-die temperature is unknown.

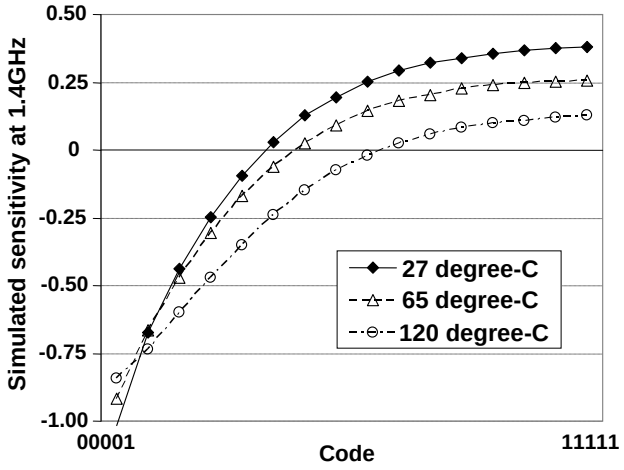


Figure 3.19: Simulated sensitivity with temperature variations.

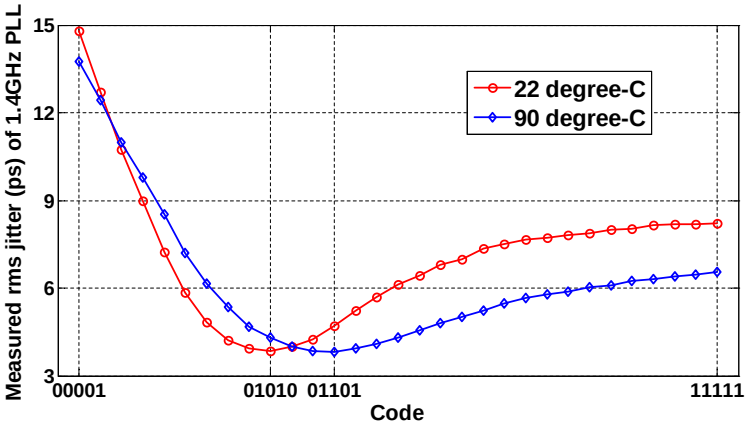
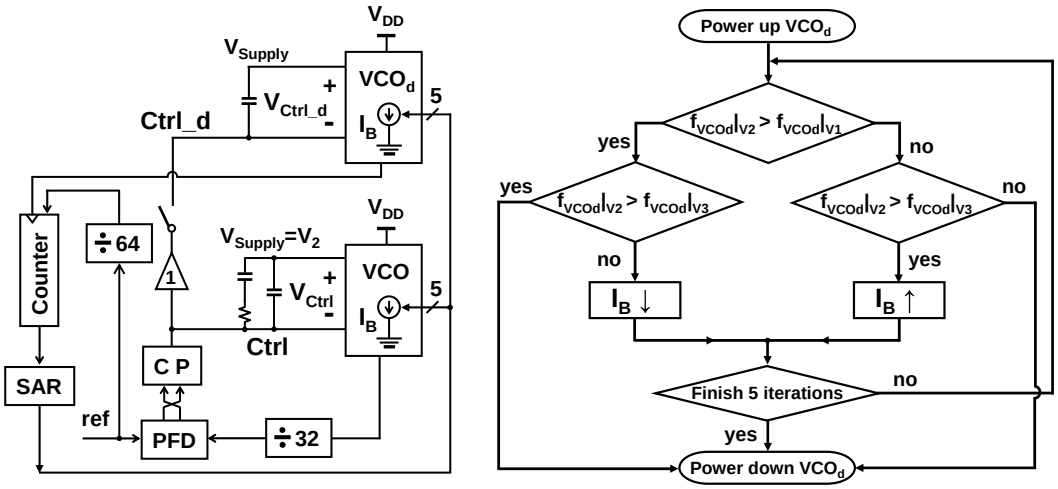


Figure 3.20: Measured rms jitter in the presence of a 1 MHz supply noise.

higher temperature. The optimum code changes from "01010" to "01101". A re-calibration at 90 °C converges to the code "01011", which is also close to the optimum.

The initial calibration is performed after the system is powered up. As long as the noise in the supply voltage is much less than the difference between V_1 and V_3,

a re-calibration in a noisy environment has negligible impact on the obtained code. However, the PLL timing jitter may increase significantly during a re-calibration, not only due to the break in the loop but also because the supply voltage alternates between V_3 and V_1. One method to tackle the problem is to re-calibrate the PLL during system standby. Nevertheless, the system operation has to be interrupted. This is undesirable for many applications. To enhance the calibration technique, a background calibration would be desirable.



(a) (b)

Figure 3.21: Enhanced PLL with background calibration. (a) Schematic. (b) Flowchart.

One way a background calibration can be implemented is by adding a dummy PLL. This dummy PLL can be periodically powered up to perform a calibration in order to obtain the code in I_B, while the main PLL maintains normal operation. An even simpler method is shown in Fig. 3.21(a). A dummy VCO has been added

in parallel with the main VCO. The main VCO always operates with the supply voltage V_2. Fig. 3.21(b) shows the calibration algorithm, which is similar to the previous one. One calibration cycle has two phases. In each phase, the supply voltage of the dummy VCO is changed from V_2 to V_1 and from V_2 to V_3, respectively. At the beginning of each calibration phase, the dummy VCO uses a supply voltage V_2, and the switch is closed. Since both the supply voltage and the control voltage are the same for the two VCOs, their oscillation frequencies are also the same, assuming there is good matching between them. Then the switch is opened and the supply voltage of the dummy VCO is changed. The oscillation frequency also changes due to the change in the supply voltage. The dummy VCO output feeds a 12-bit counter to count the divided reference clock. The polarity of the change in the dummy VCO oscillation frequency can be detected by observing the MSB of the counter output. The calibration procedure would continue until either all five cycles are completed or until the polarity of the frequency change in one calibration cycle is the same between the two phases, which suggests that a close-to-zero sensitivity (given sufficient matching) is reached.

3.5 Summary

This chapter describes a ring-oscillator based PLL with an on-chip calibration technique that enables successful integration of a supply noise insensitive PLL. Over a wide operating frequency range, the 1 V, 0.13-μm CMOS prototype IC measurement results have confirmed robust operation in the presence of VCO supply

noise. The proposed work rejects supply noise while avoiding the use of supply regulation, which makes the proposed technique more desirable in the design of low-voltage high-performance ring VCOs. A feasible implementation of a background calibration technique which would be robust to temperature variations has also been presented. The concepts presented in the context of the prototype analog PLL implementation can be easily migrated to a digital PLL.

Chapter 4 – Design Techniques for Constant Loop Bandwidth Frequency Synthesizers

PLL based frequency synthesizers are widely used in RF applications. The output of a PLL frequency synthesizer is tuned by changing the division ratio N. If N is an integer, then the synthesizer is called an integer-N frequency synthesizer. If N is a fraction, then the synthesizer is called a fractional-N frequency synthesizer. In this chapter, we focus on the design of an integer-N frequency synthesizer. However, the proposed techniques can be also migrated to fractional-N synthesizers.

The design of PLL frequency synthesizers is a challenging task due to the conflicting requirements of small integrated phase noise, fast settling time, small level of reference spurs, and low power consumption. The need to meet these specifications in all frequency bands of a given standard further complicates the design. The PLL loop bandwidth is an important design parameter that, unfortunately, controls most of these performance parameters. Therefore, the loop bandwidth of a PLL frequency synthesizer must be optimized.

Chapter 2 provides a review of many design techniques for adaptive loop bandwidth PLLs, where the loop bandwidth is proportional to the reference clock frequency. For a PLL frequency synthesizer, the reference clock is typically provided by a low noise crystal oscillator with a fixed frequency. Therefore, the design of

an adaptive loop bandwidth PLL synthesizer is equivalent to the design of a constant loop bandwidth PLL synthesizer. Previous adaptive loop bandwidth PLLs were implemented using ring oscillators. In order to satisfy the stringent phase noise specifications in RF applications, most PLL frequency synthesizers employ LC-based oscillators. Hence, the focus of this work is on LC-VCO based PLLs.

The loop bandwidth of a PLL is proportional to the VCO gain K_o. In order to reduce the control voltage sensitivity to both random and deterministic noise, a small K_o is desirable. A reduced VCO gain also improves the VCO supply noise rejection. Furthermore, since the charge-pump noise is proportional to $\sqrt{I_{CP}}$, for a given loop bandwidth, the PLL phase noise is improved by increasing I_{CP} and decreasing K_o by the same factor.

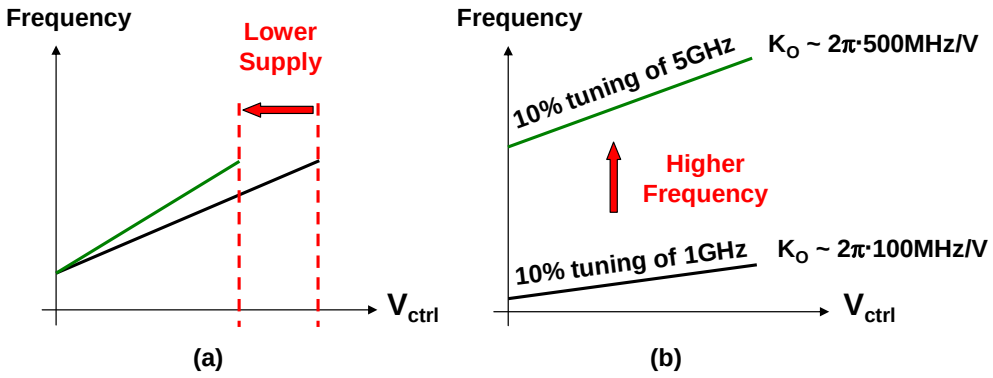


Figure 4.1: Increased VCO gain K_o with technology scaling.

However, the VCO gain K_o increases with technology scaling. There are three reasons for the increase in K_o. First, as shown in Fig. 4.1(a), the operating range of the control voltage V_{ctrl} is decreased due to the reduced power supply voltage. This results in an increased K_o for the same operating frequency range. Second,

higher operating frequencies obtainable with scaled processes cause K_o to increase for the same percentage of frequency tuning range (Fig. 4.1(b)). Third, driven by today's wideband applications, the percentage of frequency tuning range also increases. For example, to cover all the frequency bands in wireless-local-area-network (WLAN) applications, a 20% tuning range is required [32]. An almost 100% tuning range is needed for ultra wideband (UWB) applications [33].

Conventionally, the VCO gain K_o varies significantly across the frequency of operation. As a result, the loop bandwidth varies substantially and hence degrades the performance of PLL frequency synthesizers. This problem is made even worse due to the increased VCO gain and the extended frequency tuning range of future processes. This chapter describes circuit techniques for maintaining a constant loop bandwidth in LC oscillator based PLL frequency synthesizers. The chapter is organized as follows. Section 4.1 discusses the requirements for a constant loop bandwidth PLL synthesizer and presents the proposed PLL architecture. The design of the building blocks are described in Section 4.2. Measurement results are presented in Section 4.3. Section 4.4 discusses the impact of PVT variations on the proposed techniques and presents an enhanced digital scheme.

4.1 PLL Synthesizer and Proposed Architecture

As derived in Chapter 2, the loop bandwidth of an overdamped PLL is approximated by

$$\omega_{-3dB} \approx \omega_c = \frac{I_{CP}}{2\pi} R_2 \cdot \frac{K_o}{N} = \frac{I_{CP}}{2\pi} R_2 \cdot \frac{K_o}{\omega_{osc}/\omega_{ref}} \tag{4.1}$$

where I_{CP} is the charge pump current, R_2 is the loop filter resistor, N is the division ratio, ω_{osc} is the VCO operating frequency, and ω_{ref} is the reference frequency.

The loop filter resistor R_2 is process and temperature dependent. In order to suppress this dependence, the charge pump current I_{CP} can be generated by using a temperature independent band-gap voltage V_B and a resistor R_B that is matched to R_2.

$$I_{CP} = \frac{V_B}{R_B} \tag{4.2}$$

From Eq. (4.1), the loop bandwidth can be found to be

$$\omega_{-3dB} = \frac{V_B}{2\pi} \cdot \frac{R_2}{R_B} \cdot \frac{K_o}{\omega_{osc}/\omega_{ref}} \tag{4.3}$$

The focus next is on suppressing the bandwidth variations due to changes in K_o. The VCO gain K_o is defined as

$$K_o = \left|\frac{\partial \omega_{osc}}{\partial V_{ctrl}}\right| = \left|\frac{\partial \omega_{osc}}{\partial C_{var}}\right| \cdot \left|\frac{\partial C_{var}}{\partial V_{ctrl}}\right| \tag{4.4}$$

where V_{ctrl} and C_{var} are the VCO control voltage and the effective capacitance of the controlled varactor, respectively. The first term $|\partial\omega_{osc}/\partial C_{var}|$ reveals the dependence of the varactor capacitance on the oscillation frequency, and the second term $|\partial C_{var}/\partial V_{ctrl}|$ is the control voltage sensitivity of the varactor. The oscillation frequency of an LC VCO is given by

$$\omega_{osc} = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{L(C_{fix} + C_{var})}} \tag{4.5}$$

where L and C are the inductance and capacitance of the LC-tank, respectively, and C_{fix} is the LC-tank capacitance excluding the varactor capacitance C_{var}. Using this equation, we have

$$\left|\frac{\partial \omega_{osc}}{\partial C_{var}}\right| = \frac{L}{2} \cdot \omega_{osc}^3 \tag{4.6}$$

Combining (4.4) and (4.6), the VCO gain K_o can be found to be

$$K_o = \frac{L}{2} \cdot \omega_{osc}^3 \cdot \left|\frac{\partial C_{var}}{\partial V_{ctrl}}\right| \tag{4.7}$$

This equation shows that K_o is proportional to the LC-tank inductance L, which is process sensitive. To suppress the bandwidth dependence on L, an on-chip calibration technique [13] can be used. The loop bandwidth can be optimized for the best phase noise performance. However, this technique is susceptible to variations in K_o resulting in a loop bandwidth that varies significantly with the operating frequency. Consequently, when the PLL output frequency changes, the loop bandwidth has to be re-calibrated. This is undesirable due to the stringent settling time requirements. In order to obviate these issues, a technique that maintains a constant loop bandwidth over a wide frequency tuning range is desirable.

From (4.7), the VCO gain K_o is proportional to the voltage sensitivity of the varactor $|\partial C_{var}/\partial V_{ctrl}|$. However, due to the varactor's nonlinearity, $|\partial C_{var}/\partial V_{ctrl}|$ varies with the control voltage. To reduce the effect of the varactor nonlinearity, conventional designs use a digital split-tuning technique in LC-VCO based PLL frequency synthesizers [32]. The block diagram is shown in Fig. 4.2. The VCO is controlled by a small varactor as well as a bank of switched capacitors. An

auto-tuning circuitry controls the bank of switched capacitors and brings the VCO frequency close to lock. By doing so, both a wide frequency tuning range and a small value of the VCO gain K_o are achieved. Moreover, increasing the number of the switched capacitors can further reduce the control voltage variation, leading to a reduced K_o dependence on the varactor.

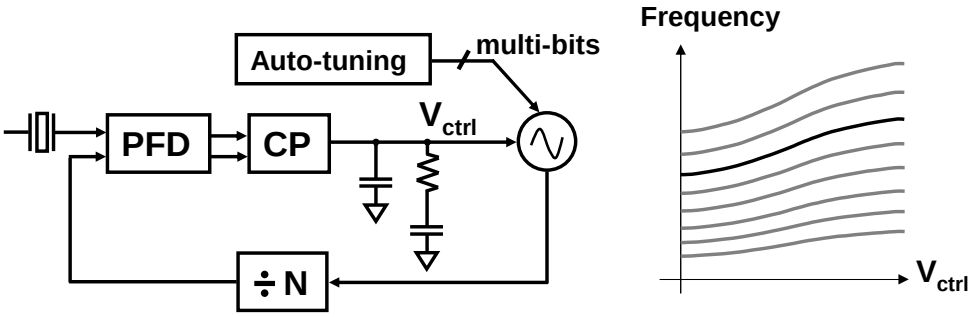


Figure 4.2: Digital split-tuning PLL frequency synthesizer.

There are a number of drawbacks in this digital split-tuning scheme. First, a robust frequency calibration algorithm is needed to ensure frequency lock under PVT variations. Second, there is a limitation in the quality factor of the switched capacitors [34]. Moreover, due to the granularity of the auto-tuning scheme and PVT variations, the varactor can be potentially biased in its nonlinear region. In order to keep the loop bandwidth constant, the charge-pump current can be adjusted to compensate for K_o variations (Eq. (4.1)). In [35], a linearization circuitry compares the control voltage with a number of threshold voltages and adjusts I_{CP} inversely to K_o by means of a step piecewise linear fitting. This linearization technique was improved by using an analog folding circuit to generate

the charge-pump current directly from the control voltage [33, 36].

Although the bandwidth can be made relatively constant, the above techniques are process and temperature dependent [36]. In addition, these techniques can not be applied for wide-band frequency synthesizers. From Eq. (4.7), K_o is also a strong function of the operating frequency ω_{osc}. This suggests that, even for the same control voltage V_{ctrl}, the VCO gain would be different for different frequency tuning curves (Fig. 4.2). Since K_o scales with ${\omega_{osc}}^3$, for example, a 30% increase in the operating frequency would lead to a 120% increase in the VCO gain K_o due to the dependence on ${\omega_{osc}}^3$. This observation is also validated from measurement results [37]. Using a 6-bit digitally controlled switched capacitor bank, the VCO achieved an operating frequency range from 1.6 GHz to 2.1 GHz (31% increase in frequency) with a VCO gain of 21 MHz/V for the bottom tuning curve and 45 MHz/V for the top tuning curve (114% increase in K_o).

To mitigate both the varactor nonlinearity and the operating frequency dependence on K_o, alternative techniques need to be developed. The design objectives for high performance LC-VCO based PLL frequency synthesizers include:

- Wide tuning range,
- Small VCO gain K_o, and
- PVT tolerant constant loop bandwidth.

In order to achieve the above design objectives, an analog split-tuning architecture depicted in Fig. 4.3 is adopted. This architecture has been implemented using both LC-VCOs [38] and ring VCOs [39, 40]. The VCO is controlled by two varactors: a small varactor tuned by a fine control voltage V_{ctrl} and a large var-

actor tuned by a coarse control voltage V_C. An additional frequency locking path integrates the voltage across the loop filter integrator capacitor and generates the coarse control voltage V_C to drive the VCO towards frequency lock. The integrator also biases the fine control voltage V_{ctrl} to a known reference voltage V_{ref}. In order to ensure loop stability, the coarse loop is made slow enough compared to the loop bandwidth.

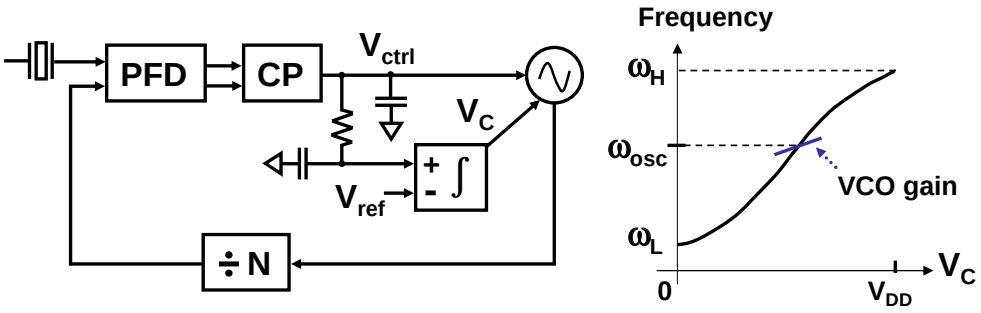


Figure 4.3: Analog split-tuning PLL frequency synthesizer.

Fig. 4.3 also shows the frequency tuning curve with the coarse control V_C. Assume that the VCO has a gain of K_{of} at the fine control node and a gain of K_{oc} at the coarse control node. When K_{of} is much smaller than K_{oc} ($K_{of} \ll K_{oc}$), analog split-tuning PLL frequency synthesizers offer the benefits of both a wide frequency tuning range and a small VCO gain.

Additionally, the design of a high performance CP circuit is made simpler. In the conventional digital split-tuning PLLs, it is difficult to match the charge-pump currents I_{UP} and I_{DN} for a range of the VCO control voltage. The unmatched charge-pump currents cause a static phase offset at the PFD input and, hence, reference sidebands at the PLL output. In contrast, the analog split-tuning ar-

chitecture forces the fine control voltage V_{ctrl} to be V_{ref} under locked conditions. Typically, V_{ref} is set to be $V_{DD}/2$. For a fixed CP output voltage, it is much simpler to achieve matched I_{UP} and I_{DN}.

Finally, the varactor dependence on the loop bandwidth is suppressed in the analog split-tuning PLLs. Combining (4.1) and (4.7), the ratio of the loop bandwidth to the reference frequency is given by

$$\frac{\omega_{-3dB}}{\omega_{ref}} = \frac{I_{CP}}{4\pi} \cdot R_2 \cdot L \cdot \omega_{osc}^2 \cdot \left| \frac{\partial C_{var}}{\partial V_{ctrl}} \right| \tag{4.8}$$

Since V_{ctrl} is fixed, $|\partial C_{var}/\partial V_{ctrl}|$ is a constant, i.e., the variation of the VCO gain K_{of} due to the varactor nonlinearity is suppressed. The bandwidth of the analog split-tuning PLL synthesizer depends only on the operating frequency ω_{osc}.

In order to maintain a constant loop bandwidth, Eq. (4.8) illustrates that the charge-pump current I_{CP} should be proportional to ${\omega_{osc}}^{-2}$. This proportionality can be achieved by making I_{CP} scale with N^{-2}. However, for a large N, the computation of N^{-2} incurs a large hardware overhead. An alternative approach is to use the coarse control voltage V_C, as the frequency ω_{osc} can be written as a function of V_C. In Fig. 4.3, assume the lowest operating frequency ω_L is obtained when V_C is zero, and the highest operating frequency ω_H is obtained when V_C reaches the supply voltage V_{DD}. Using a linear approximation, the operating frequency ω_{osc} for a coarse control voltage V_C is approximated by

$$\omega_{osc} \approx \omega_L(1 + \frac{\omega_H - \omega_L}{\omega_L} \cdot \frac{V_C}{V_{DD}}) \tag{4.9}$$

As a consequence, a constant loop bandwidth only requires the charge-pump current to be

$$I_{CP} \propto (1 + \frac{\omega_H - \omega_L}{\omega_L} \cdot \frac{V_C}{V_{DD}})^{-2} \tag{4.10}$$

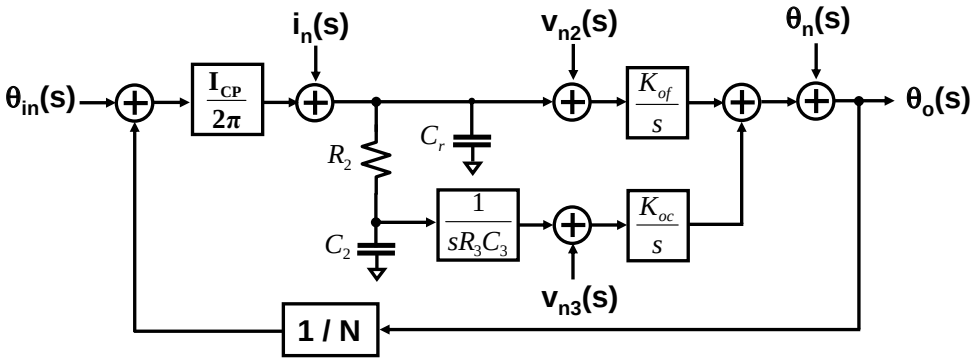


Figure 4.4: Linear model of the analog split-tuning PLL.

In the above analysis, we have assumed that the coarse loop has a negligible impact on the PLL bandwidth and phase margin. Now we consider the necessary conditions for this assumption to be valid. The linear model for the analog split-tuning PLL is shown in Fig. 4.4. A 2^{nd}-order loop filter is employed, with a zero frequency of $\omega_z = \frac{1}{R_2 C_2}$ and a pole frequency of $\omega_r = \frac{1}{R_2 C_r}$ in the open-loop response. The coarse loop employs a first order integrator with a transfer function $(1/sR_3C_3 = 1/s\omega_3)$, where ω_3 is defined by

$$\omega_3 = \frac{1}{R_3 C_3} \tag{4.11}$$

The PLL overall loop gain $G_T(s)$ can be expressed as the sum of the fine loop gain $G_F(s)$ and the coarse loop gain $G_C(s)$. Assuming $\omega_z \ll \omega_r$ $(C_2 \gg C_r)$, which is

typically true, it can be shown that

$$G_F(s) = \frac{I_{CP}}{2\pi} R_2 (1 + \frac{\omega_z}{s}) \frac{\omega_r}{s + \omega_z + \omega_r} \frac{K_{of}}{s} \frac{1}{N} \approx \frac{\omega_c}{s} (1 + \frac{\omega_z}{s}) \frac{\omega_r}{s + \omega_r} \tag{4.12}$$

$$G_C(s) = \frac{I_{CP}}{2\pi} \frac{\omega_r}{s + \omega_z + \omega_r} \frac{1}{sC_2} \frac{1}{sR_3C_3} \frac{K_{oc}}{s} \frac{1}{N} \approx \frac{\omega_c \omega_z \omega_3}{s^3} \frac{K_{oc}}{K_{of}} \frac{\omega_r}{s + \omega_r} \tag{4.13}$$

where ω_c is approximately the loop bandwidth (Eq. (4.1)). The overall loop gain $G_T(s)$ can be found to be

$$G_T(s) = G_F(s) + G_C(s) = \frac{\omega_c}{s} \frac{\omega_r}{s + \omega_r} (1 + \frac{\omega_z}{s} + \frac{K_{oc}}{K_{of}} \frac{\omega_z \omega_3}{s^2}) \tag{4.14}$$

A point of interest is the frequency where the fine loop gain and coarse loop gain are equal. It can be shown that this frequency ω_e is approximated by

$$\omega_e = \frac{K_{oc}}{K_{of}} \omega_3 \tag{4.15}$$

The bode plot of the loop gains are conceptually shown in Fig. 4.5. In the overall loop gain $G_T(s)$, the coarse loop gain $G_C(s)$ is dominant at frequencies below ω_e, and the fine loop gain $G_F(s)$ is dominant at frequencies larger than ω_e. In order for the coarse loop to have a negligible impact on the loop bandwidth and phase margin, the frequency ω_e should be lower than ω_z.

$$\omega_e < \omega_z \tag{4.16}$$

As an example, Fig. 4.6 shows the simulated open loop gain and phase responses

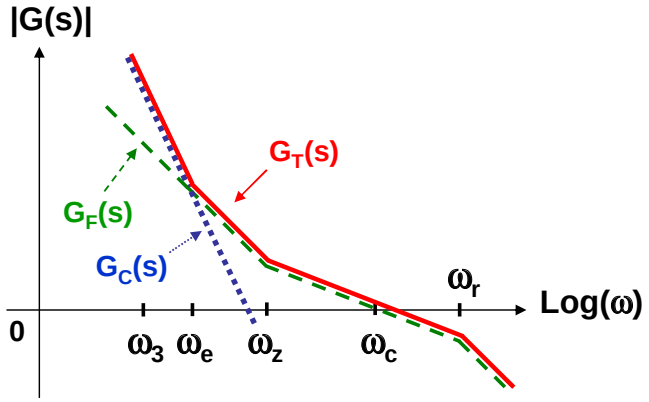


Figure 4.5: Bode plot of open loop gains. The coarse loop gain $G_C(s)$ is dominant at frequencies below ω_e, and the fine loop gain $G_F(s)$ is dominant at frequencies larger than ω_e.

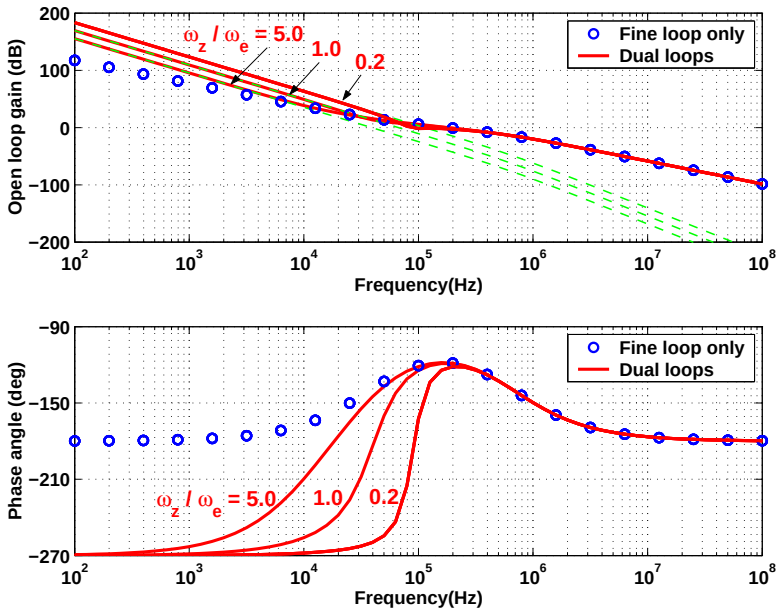


Figure 4.6: Stability analysis for the analog split-tuning PLL. (a) Loop gain magnitude response. (b) Phase response. The loop stability is degraded with a reduced ratio of ω_z/ω_e.

for an analog split-tuning PLL. In this example, ω_z, ω_c, and ω_r are $2\pi \cdot 40kHz$, $2\pi \cdot 200kHz$, and $2\pi \cdot 600kHz$, respectively. The simulations are performed with values of 5, 1, and 0.2 for the ratio of ω_z to ω_e, respectively. As can be seen from the figure, the loop stability is degraded with a reduced ratio of ω_z to ω_e, and the loop will be unstable when ω_z/ω_e is 0.2.

The coarse loop parameters (R_3C_3) can be derived from (4.11), (4.15), and (4.16),

$$R_3C_3 > \frac{K_{oc}}{K_{of}} R_2C_2 \tag{4.17}$$

Eq. (4.17) illustrates a lower limit for the coarse loop parameters R_3C_3 due to the loop stability constraint. On the other hand, during the lock-in process, the charge-pump output voltage V_{ctrl} would saturate to either the power or ground rail. The coarse loop aids the PLL frequency lock by slewing up or down the coarse control voltage V_C to the desired value. The slew-rate SR for V_C is given by

$$SR = \frac{V_{DD}}{2R_3C_3} \tag{4.18}$$

Assume the settling time of the PLL is dominated by the coarse control voltage settling time. If the PLL is required to switch an output frequency from ω_{osc} to $(\omega_{osc} \pm \Delta\omega_{osc})$ within a time period of T_S, then

$$R_3C_3 < \frac{V_{DD}}{2} T_S \frac{K_{oc}}{\Delta\omega_{osc}} \tag{4.19}$$

This equation yields an upper limit for the parameters R_3C_3. As a consequence,

the design of the coarse control loop must trade off between the loop stability and settling time. For high performance PLL frequency synthesizers, there is always a stringent settling time specification. In order to decouple this trade-off and to reduce the settling time, new techniques need to be developed.

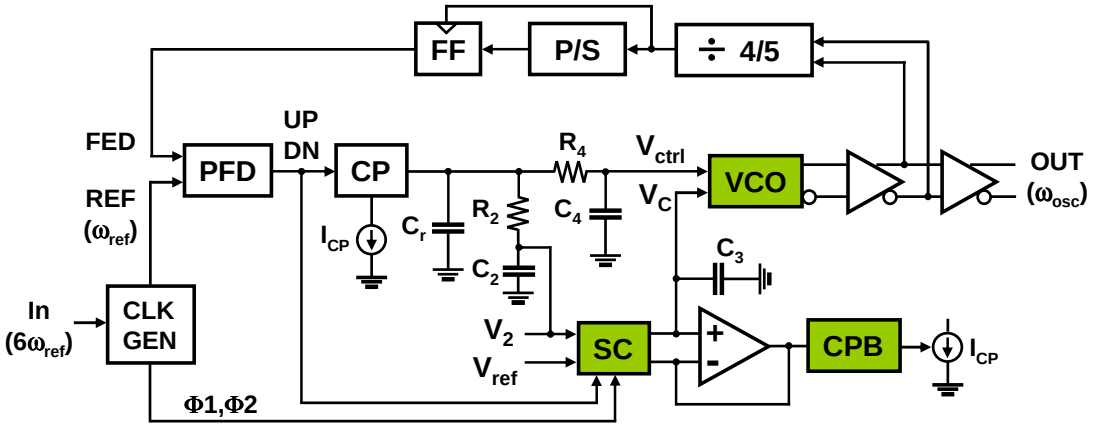


Figure 4.7: Proposed constant loop bandwidth PLL frequency synthesizer with an adaptively tuned coarse loop.

Fig. 4.7 shows the proposed wide tuning range PLL frequency synthesizer. The PLL is designed to operate in the 3 to 4 GHz frequency range. The PLL consists of a PFD, a CP, a 3^{rd} order loop filter, an analog split-tuning LC-VCO, and a pulse-swallow counter. An additional low-pass filter, consisting of R_4 and C_4, is used in the loop filter to further attenuate the reference sidebands at the PLL output. The corresponding additional pole is at the frequency $\omega_4 = \frac{1}{R_4 C_4}$. The coarse loop employs a switched-capacitor (SC) integrator. A rail-to-rail amplifier [41] is used in the SC integrator. To scale the charge-pump current proportional to ${\omega_{osc}}^{-2}$, the coarse control voltage V_C is fed to a CP biasing circuitry to generate I_{CP}. A

clock generator block generates the clock reference (ω_{ref}) for the PLL. The clock generator also produces two non-overlapping clock phases with the same frequency as ω_{ref} for the SC integrator. To improve the PLL settling, an adaptively tuned SC circuit is proposed. The exclusive-OR (XOR) of UP and DN pulses from the PFD is fed into the SC integrator. When the loop is in lock, the time constant of the SC integrator remains the same. But when the loop is unlocked, the XOR output reduces the time constant, and, hence, reduces the settling time.

4.2 Circuit Design

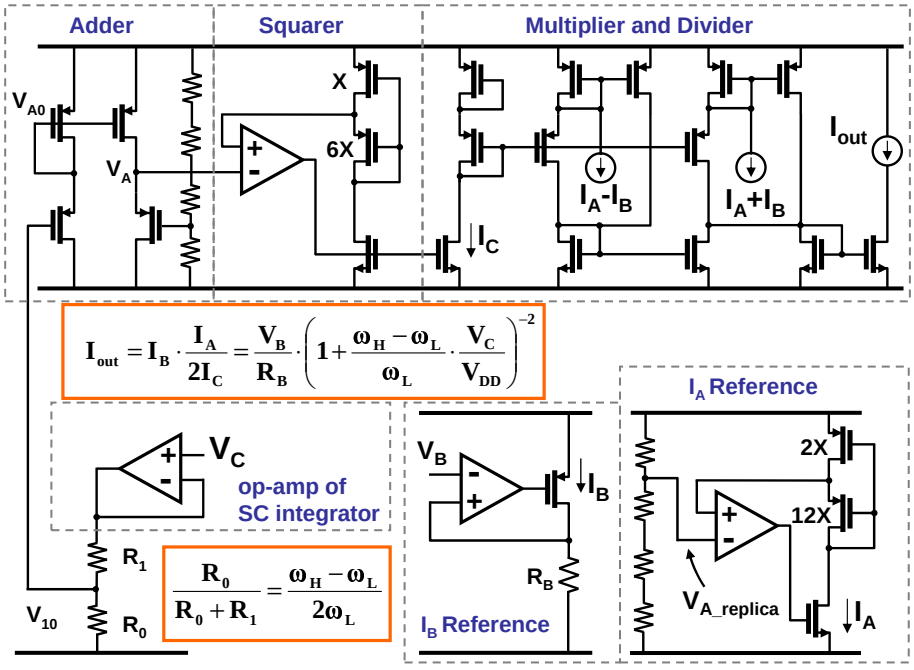


Figure 4.8: Simplified charge-pump biasing circuits for CP current to be inversely proportional to ${\omega_{osc}}^2$.

A constant loop bandwidth requires the charge-pump current I_{CP} to be inversely proportional to ${\omega_{osc}}^2$ (Eq. (4.10)), where ω_{osc} is the PLL output frequency. Fig. 4.8 shows the CP biasing circuitry. It consists of an analog adder, a squarer [42], and a multiplier/divider [43]. It can be shown that

$$\begin{aligned} V_{10} &= V_C \cdot \frac{R_0}{R_0 + R_1} \\ V_{A0} &= \frac{1}{2}(V_{DD} + V_{10}) \\ V_A &= \frac{5}{4}V_{DD} - V_{A0} \end{aligned} \tag{4.20}$$

and

$$\begin{aligned} I_C &= \frac{k}{2} \cdot 6X \cdot (\frac{V_{DD} - V_A}{\sqrt{7} - 1})^2 \\ I_A &= \frac{k}{2} \cdot 12X \cdot (\frac{V_{DD} - \frac{3}{4}V_{DD}}{\sqrt{7} - 1})^2 \end{aligned} \tag{4.21}$$

where I_A is a replica of I_C, which is obtained by feeding a reference input voltage rather than V_C. The divider output current I_{out} is given by [43]

$$I_{out} = I_B \cdot \frac{I_A}{2I_C} = \frac{V_B}{R_B} \cdot \frac{I_A}{2I_C} \tag{4.22}$$

where the current I_B is obtained from a band-gap voltage V_B and a resistor R_B matched to the loop filter resistor R_2. Therefore, the dependence of the resistance

on the PLL bandwidth is suppressed. If the resistors R_0 and R_1 have a relationship,

$$\frac{R_0}{R_1 + R_0} = \frac{\omega_H - \omega_L}{2\omega_L} \tag{4.23}$$

then from (4.20) to (4.23), I_{out} can be found to be

$$I_{out} = \frac{V_B}{R_B} \cdot (1 + \frac{\omega_H - \omega_L}{\omega_L} \cdot \frac{V_C}{V_{DD}})^{-2} \tag{4.24}$$

Thus, we arrive at Eq. (4.10), which requires the charge-pump current I_{CP} to be inversely proportional to ${\omega_{osc}}^2$. Moreover, the process and temperature dependent parameters, such as carrier mobility, are cancelled by using the replica circuitry. In the prototype chip, for simplicity I_B is an input bias current only.

Two LC-VCOs were designed in the prototype chip. One uses a pMOS top bias and nMOS cross-coupled topology (VCO1). Another VCO uses the complementary cross-coupled topology (VCO2). The schematics of VCO1 and VCO2 are shown in Fig. 4.9 and Fig. 4.10, respectively. VCO1 is integrated in the PLL frequency synthesizer.

Note that a linear approximation for the VCO coarse frequency tuning curve is used in Eq. (4.10). To make this assumption valid, the varactor linearity is critical. Designing a wide-tuning range linear varactor is very challenging. The linearity of a varactor can be improved by combining P- and N-type varactors in a differentially controlled PLL [44, 45]. But a differential loop filter increases the die area for a low bandwidth PLL synthesizer. To alleviate the problem, an averaging varactor is employed in both VCOs. Three MOS varactors are connected in parallel

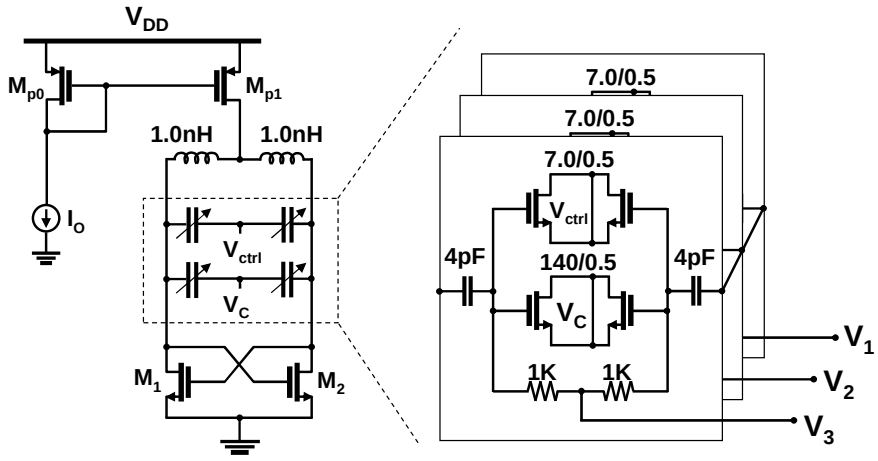


Figure 4.9: Schematic of VCO1 with nMOS cross-coupled transistors and pMOS top-bias. An averaging varactor improves the linearity of the frequency tuning curve.

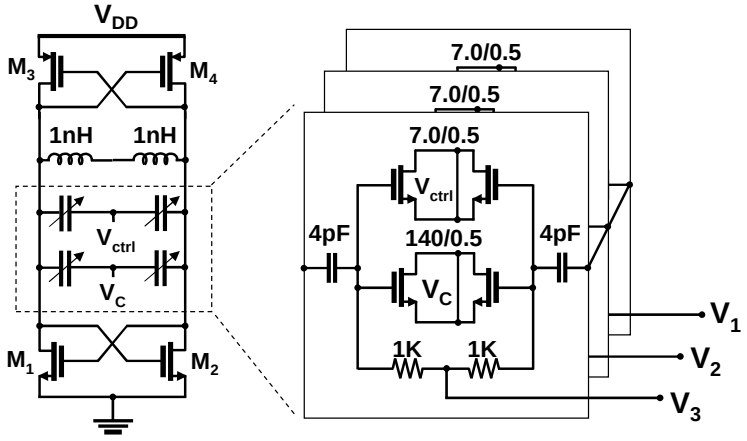
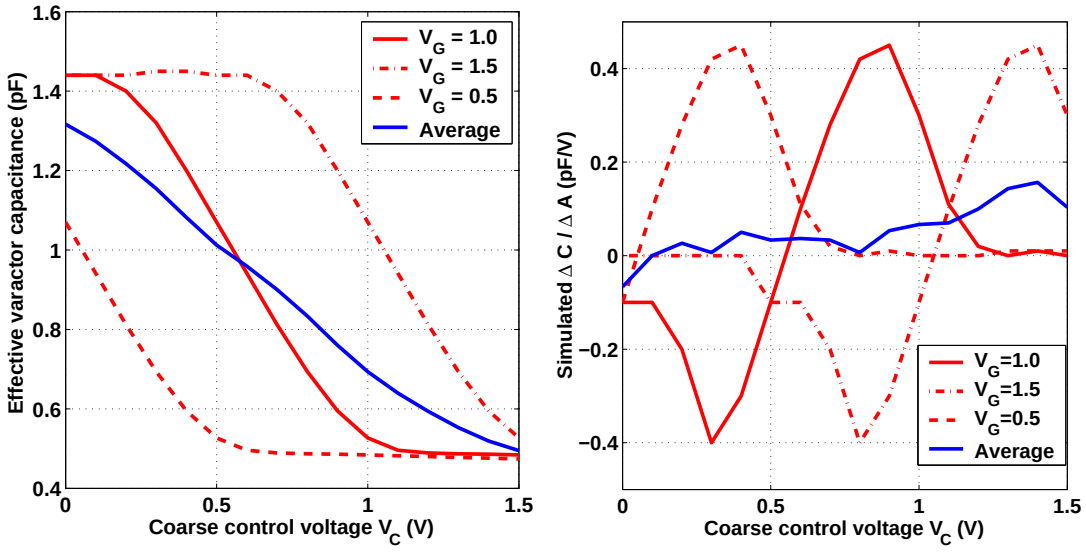


Figure 4.10: Schematic of VCO2 with complementary cross-coupled transistors. An averaging varactor improves the linearity of the frequency tuning curve.

with DC bias voltages V_1 to V_3. Rather than using a fixed DC bias voltage (i.e., $V_1 = V_2 = V_3$) as in the traditional varactor designs, the averaging varactor uses distributed voltage values for V_1 to V_3. As a result, the nonlinearities of the three

varactors are cancelled to a first order. Fig. 4.11(a) shows the simulated effective capacitance of the conventional varactor when the DC bias voltage V_G is set to be 0.5, 1.0, and 1.5, respectively, compared with the averaging varactor.



(a) (b)

Figure 4.11: Comparisons of simulated (a) effective capacitance of varactor, (b) sensitivity of VCO output voltage.

Improving the linearity of the varactor also improves the VCO phase noise. Due to the varactor's nonlinearity, any amplitude variations in the VCO output modulates the varactor capacitance and the oscillation frequency, resulting in VCO phase noise. This mechanism, called amplitude-modulation (AM) to frequency-modulation (FM) noise conversion [46], is a significant source of VCO phase noise. This noise is related to the sensitivity of the VCO output voltage, $\Delta C/\Delta A$, where ΔC is the change in the varactor capacitance due to a change in the VCO output

voltage ΔA. As shown in Fig. 4.11(b), this sensitivity is reduced by using the averaging varactor. Simulation results also show that at 1 MHz offset, a 3 dB improvement in phase noise is achieved over a wide frequency range of 3.1 to 3.9 GHz. Although the averaging varactor is similar to the varactor proposed in [47], the conclusions regarding the phase noise performance differ in our work.

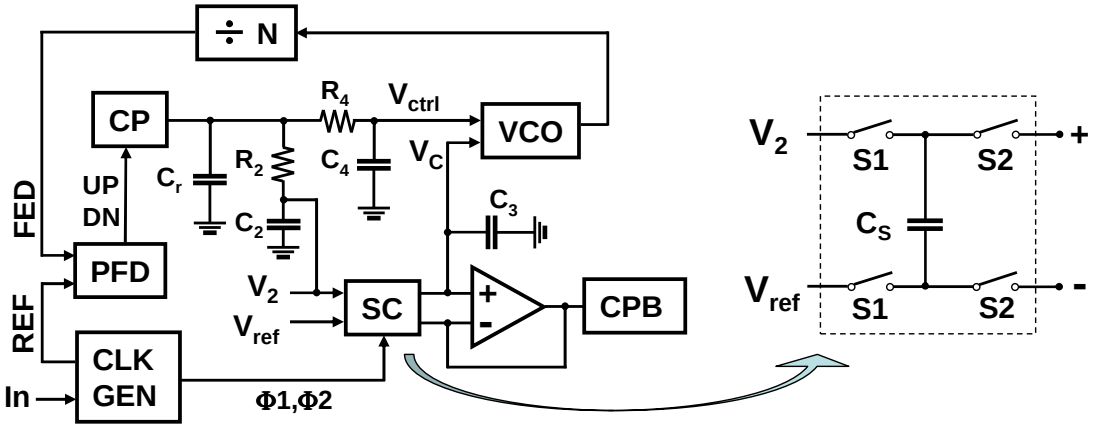


Figure 4.12: A conventional switched-capacitor integrator in the coarse loop.

A switched-capacitor (SC) integrator is employed in the frequency locking control path. A conventional SC circuit is shown in Fig. 4.12. A clock generator produces two non-overlapping phases $\Phi 1$ and $\Phi 2$ for the SC integrator. With a sampling capacitor C_S, the equivalent coarse loop parameters R_3C_3 are given by

$$R_3C_3 = \frac{1}{f_{ref}}\frac{C_3}{C_S} \tag{4.25}$$

where f_{ref} is the reference clock frequency (in Hz). To ensure loop stability, it is desirable to make the capacitor ratio C_3/C_S large. However, this increases R_3C_3

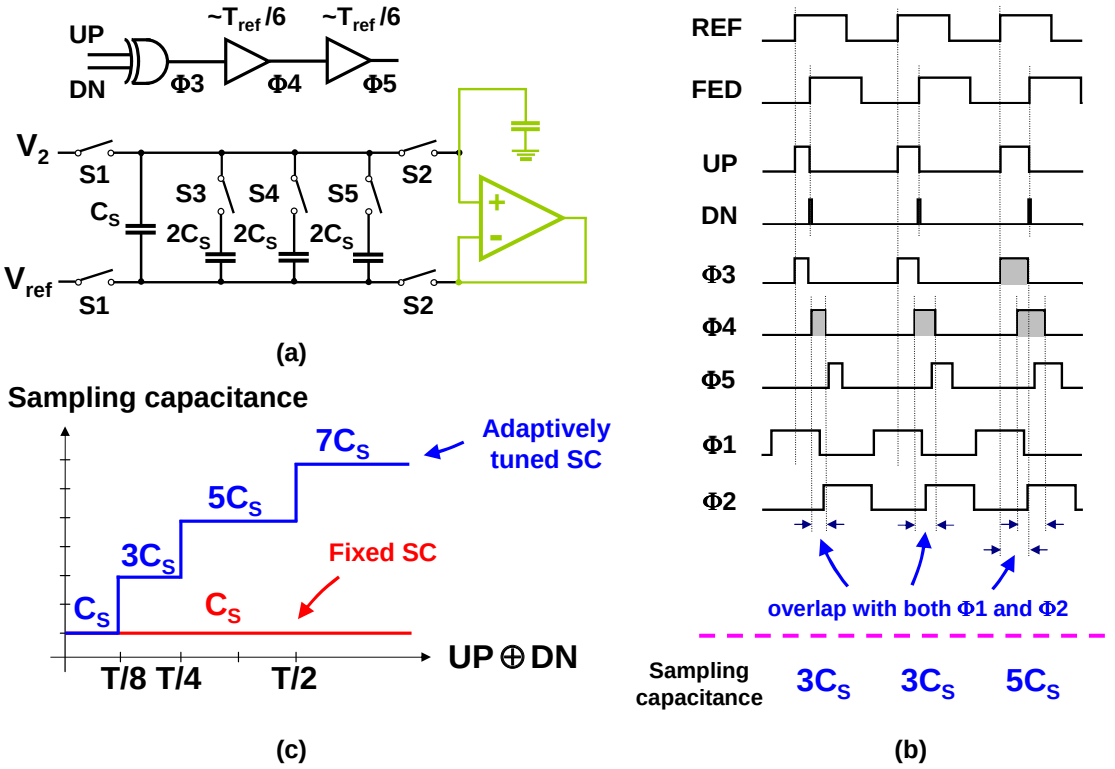


Figure 4.13: Proposed adaptively tuned switched-capacitor integrator in the coarse loop. (a) Schematic. (b) Timing diagram. (c) Effective sampling capacitance.

and hence the settling time. To eliminate this trade-off, an adaptively tuned SC circuit depicted in Fig. 4.13(a) is proposed[1]. In addition to the small sampling capacitor C_S, three sampling capacitors with capacitance values of $2C_S$ are inserted and controlled by signals $\Phi 3$, $\Phi 4$, and $\Phi 5$, respectively. To generate $\Phi 3$, the PFD output UP and DN pulses are fed into an XOR gate. The pulses $\Phi 4$ and $\Phi 5$ are simply the delayed outputs of $\Phi 3$. The timing diagram is shown in Fig. 4.13(b). When the loop is in lock, the XOR output is zero. The additional

[1]Note that the phases $\Phi 1$ and $\Phi 2$ have a 90° phase shift with respect to the reference clock.

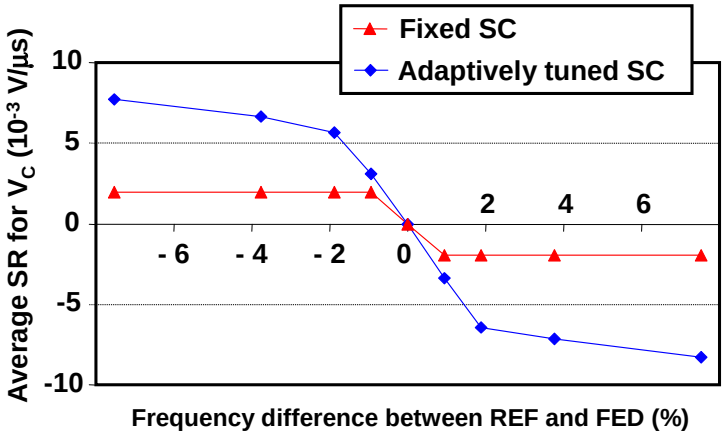


Figure 4.14: Comparison of the simulated average slew rates for V_C.

sampling capacitors have no impact on the original SC integrator. When the loop is unlocked, an increased phase error between the reference and feedback clocks leads to an increased pulse width of the XOR output. If the XOR and its delayed outputs have an overlap with both phases $\Phi 1$ and $\Phi 2$, the additional sampling capacitors are effectively added in parallel with the original capacitor C_S. The increased sampling capacitance will reduce the time constant of the SC integrator, thereby improving the PLL settling behavior. As depicted in Fig. 4.13, the effective sampling capacitance is still C_S when the loop is in lock, but it will become $3C_S$, $5C_S$, and $7C_S$ when the XOR output pulse width is larger than 1/8, 1/4, and 1/2 of the reference clock period.

Fig. 4.14 shows the simulated average slew rate (SR) for the coarse control voltage V_C with the frequency difference between the reference clock and the feedback clock. When the two frequencies are close, the adaptively tuned SC circuit behaves the same as the conventional SC circuit. When the two frequencies differ from each

Table 4.1: Designed loop parameters.

Parameter	Value	Parameter	Value
I_{CP}	0.4 (0.3-0.5) mA	N	240 - 299
K_{of}	$2\pi\cdot$ 50 (30-70) MHz/V	K_{oc}/K_{of}	20
ω_c	$2\pi\cdot$ 200 kHz	R_2	16 k Ω
ω_c/ω_z	5	C_2	30 $\times$ 8.6 pF
ω_z/ω_e	5	C_r	2 $\times$ 8.6 pF
ω_r/ω_c	3	C_S	50 fF
ω_4/ω_c	24	C_3	33 $\times$ 8.6 pF
ω_{-3dB}	$2\pi\cdot$ 250 kHz	R_4	4 k Ω
Phase margin	54°	C_4	8.6 pF

other, i.e., the loop is unlocked, the adaptively tuned SC integrator provides an increased slew rate for V_C with an increased frequency difference. As a result, the settling time is reduced without any penalty in the loop stability.

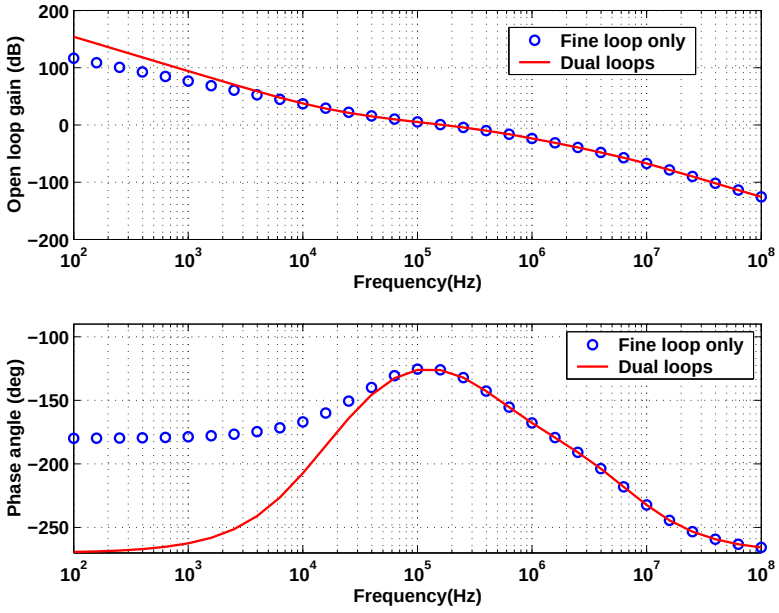


Figure 4.15: Simulated PLL open-loop gain and phase responses.

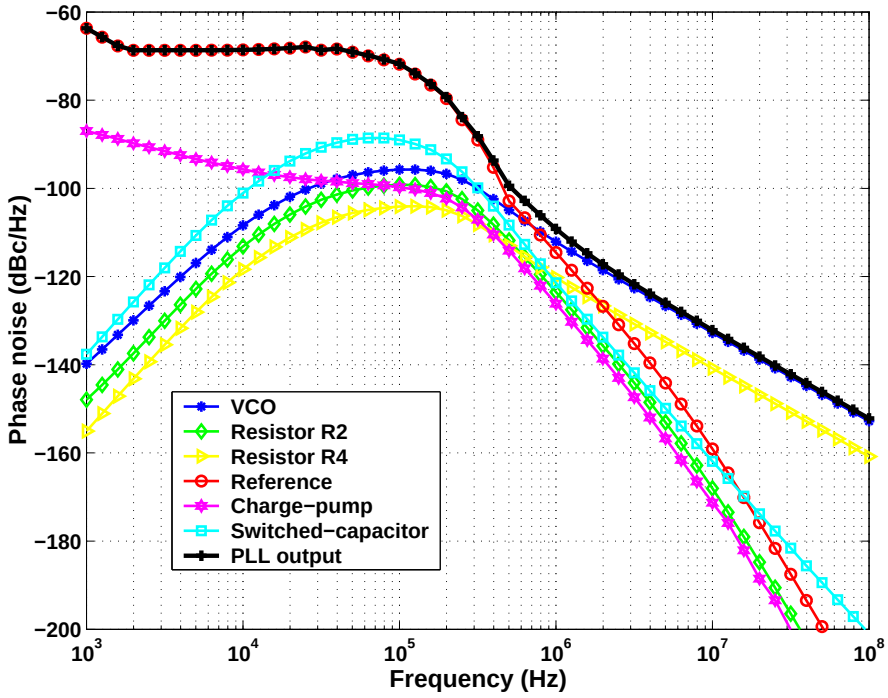


Figure 4.16: PLL noise analysis based on measured phase noise data from reference and simulated phase noise data from VCO, loop filter resistors $R2$ and $R4$, charge-pump and switched-capacitor integrator.

The design parameters for the PLL frequency synthesizer are summarized in Table 4.1. The open-loop gain and phase responses are shown in Fig. 4.15. The coarse loop has a negligible impact on the bandwidth and phase margin compared to the PLL with fine loop only.

The PLL noise analysis is depicted in Fig. 4.16. The overall phase noise includes the noise contributions from the reference input, the VCO, the loop filter resistors $R2$ and $R4$, the charge-pump circuit, and the switched-capacitor integrator. The phase noise data of the reference input is obtained by measuring a RF signal generator that is used as the reference of the PLL synthesizer in the prototype

chip measurement. The remaining noise sources are obtained from simulations. Fig. 4.16 reveals that the reference and the VCO are the dominant noise sources within and outside the loop bandwidth, respectively.

4.3 Measurement Results

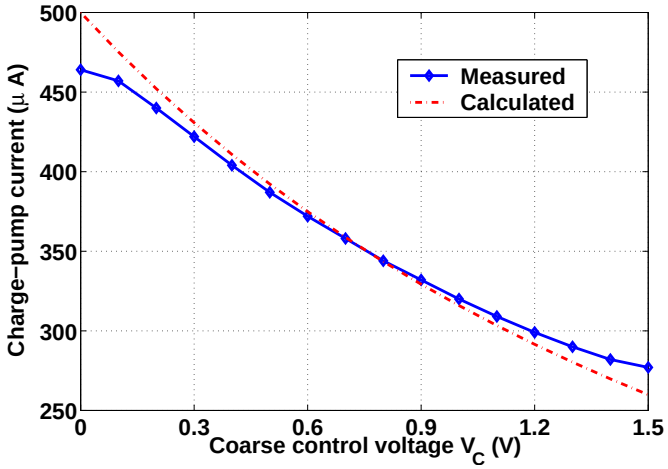


Figure 4.17: Comparison between the measured and calculated charge-pump currents.

Both VCOs and the PLL frequency synthesizer have been fabricated in a 0.13μm CMOS process. To evaluate the charge-pump tracking circuitry, I_{CP} is measured. Fig. 4.17 shows that the measured charge-pump currents match well with the calculated charge-pump currents for a large range of the coarse control voltage V_C.

Both VCOs are measured at a 1.5 V supply voltage. VCO1 oscillates at frequencies up to 4.2 GHz, however, with only a 150 MHz frequency tuning range.

It fails to oscillate at lower frequencies due to losses in the varactor. Typically in an LC-tank oscillator, the loss of the inductor is much worse than the loss of the varactor. However, this is not the case in our design due to a large varactor capacitance. Because the quality factor of the varactor, Q_C, is inversely proportional to the varactor capacitance, Q_C is decreased at reduced operating frequencies. This reduced Q_C is the dominant factor for the tank Q at lower frequencies, resulting in a failure of operation.

The metal wire connected between the VCO output and the varactor were laid out with only a 0.6-μm width in order to reduce parasitic capacitances. This results in about a 30 Ω resistance on the gate of the varactor and accounts for the loss of the varactor. To improve Q_C of the varactor, the width of the wire should be increased.

Compared to VCO1, VCO2 oscillates at a lower frequency for the same control voltage due to the smaller gate capacitance at the VCO output nodes. Since VCO2 has complementary cross-coupled transistors, it has a large enough loop gain to maintain oscillation at lower frequencies. Therefore, VCO2 oscillates across the entire control voltage range.

Fig. 4.18(a) shows the measured VCO2 tuning curves when the fine control voltage V_{ctrl} is fixed to V_{ref}. The averaging varactor significantly improves the linearity of the frequency tuning curve with a negligible reduction in the frequency tuning range. The measured K_o with respect to the fine control voltage is shown in Fig. 4.18(b). As expected, K_o scales proportional to ${\omega_{osc}}^3$.

As shown in Fig. 4.19, the measured phase noise of VCO2 operating at 3.6 GHz

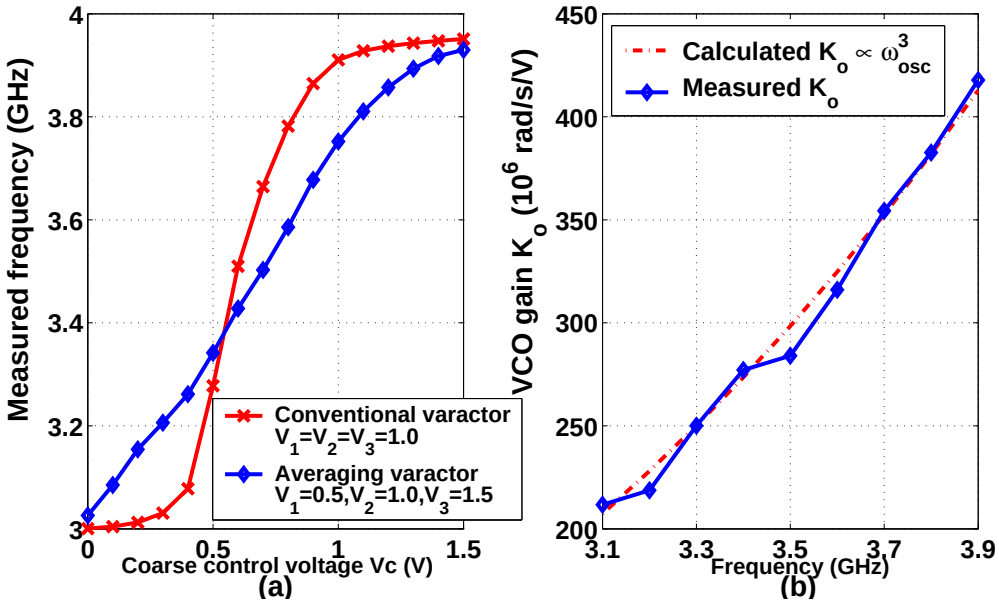


Figure 4.18: The measured VCO2 (a) tuning curves for a fixed fine control voltage V_{ctrl}, (b) K_o with respect to V_{ctrl}. K_o scales proportional to ${\omega_{osc}}^3$.

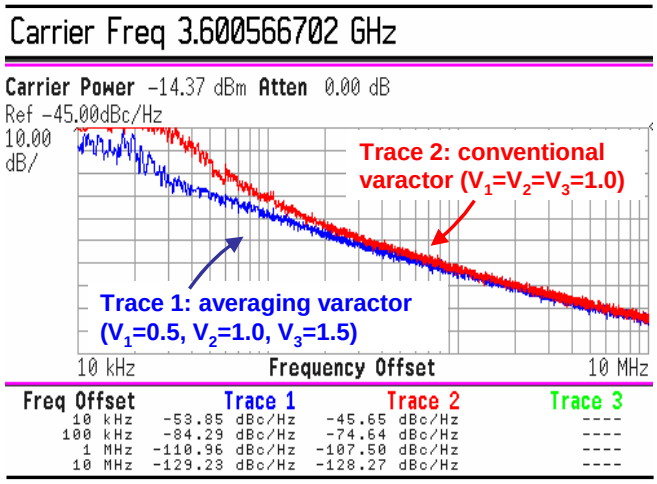


Figure 4.19: Comparison of the measured VCO2 phase noise for an operating frequency of 3.6 GHz. A 3 dB improvement in the measured phase noise at 1 MHz offset is achieved compared to the conventional design.

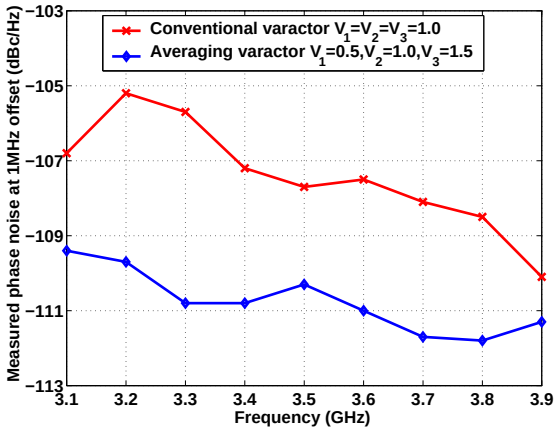


Figure 4.20: Comparison of the measured VCO2 phase noise at 1 MHz offset.

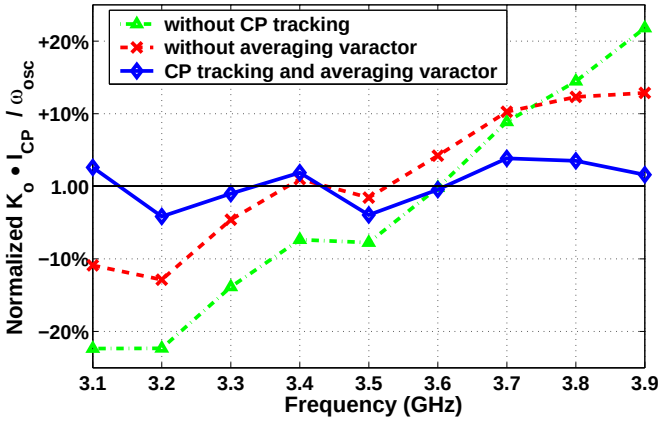


Figure 4.21: Normalized $K_o \cdot I_{CP}/\omega_{osc}$ extracted from measurements.

is -111 dBc/Hz at 1 MHz offset, which is a 3 dB improvement compared to the conventional design. Fig. 4.20 shows the improvements of phase noise performance at 1 MHz offset for a frequency range of 3.1 to 3.9 GHz [2]. At a 1.5 V supply voltage, VCO2 draws 8 mA.

To evaluate the loop bandwidth control over a wide tuning range, the mea-

[2]The figure also illustrates that the phase noise performance is degraded at lower frequencies.

surement results obtained from VCO2 are used. The measured $K_o \cdot I_{CP}/\omega_{osc}$ is normalized to its average value and is shown in Fig. 4.21. This is equivalent to $K_o \cdot I_{CP}/N$ for a fixed reference frequency, which determines the loop bandwidth (Eq. (4.1)). With a fixed I_{CP}, the loop bandwidth increases proportional to ${\omega_{osc}}^2$, and has more than ±20% variation from 3.1 to 3.9 GHz. Using the conventional VCO, the loop bandwidth variation is more than ±10% due to the nonlinearity of the coarse tuning curve. By combining the CP current tracking technique with the averaging varactor, the loop bandwidth is controlled to within ±4% for a frequency range of 3.1 to 3.9 GHz.

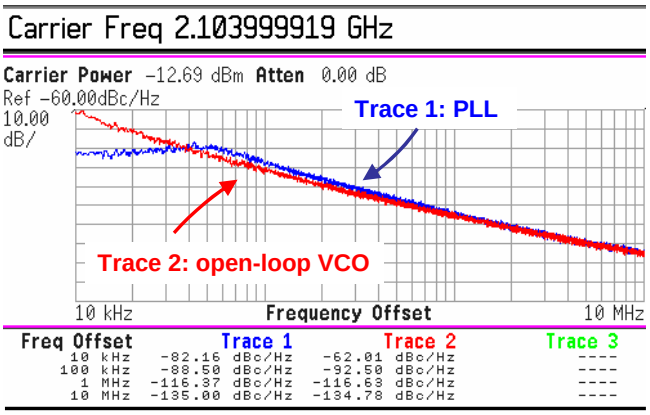


Figure 4.22: Comparison of the measured phase noise for the PLL synthesizer and open-loop VCO1 at the divided output (half of the oscillation frequency). The PLL out-band phase noise is dominated by the VCO1 phase noise.

Due to the limited oscillation frequency range in VCO1, the PLL frequency synthesizer measures from 4.09 to 4.21 GHz. The corresponding division ratio N is varied from 256 to 263 for a 16 MHz reference frequency. In the prototype chip, the PLL output is followed by a divider and a buffer. Operating at 4.208

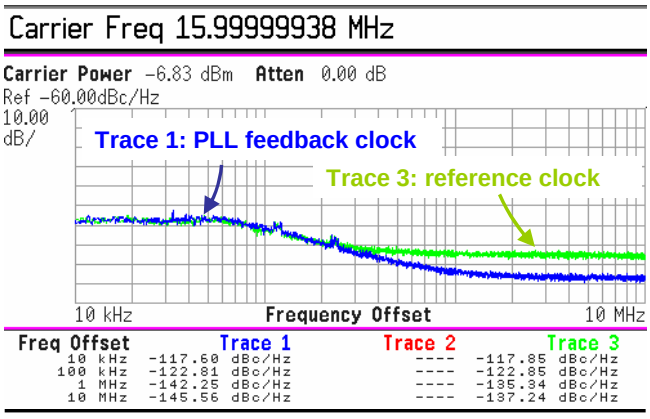


Figure 4.23: Comparison of the measured phase noise for the reference clock and the feedback clock. The PLL in-band phase noise is dominated by the input reference phase noise.

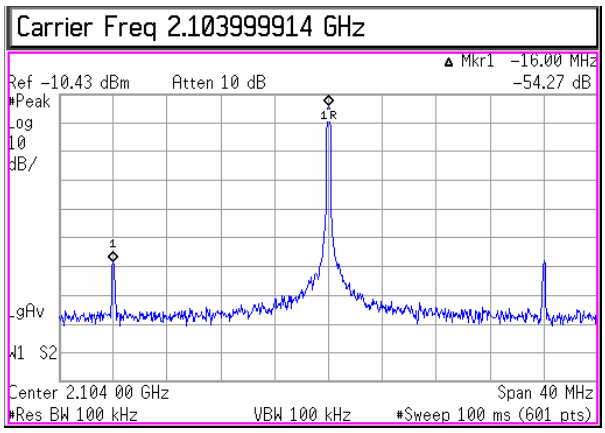


Figure 4.24: Measured spurs on the PLL divided output. The adjusted reference sideband levels after taking into account the division are -48 dB.

GHz, the measured phase noise plots for the PLL and the open-loop VCO1 at half the oscillation frequency are shown in Fig. 4.22. At 100 kHz and 1 MHz offsets, the phase noise is measured to be -88 dBc/Hz and -116 dBc/Hz, respectively. These noise levels need to be adjusted by $(20\log_{10}(2) = 6$ dB) to account for the

frequency division. This indicates that the phase noise of the 4.2 GHz PLL is -110 dBc/Hz at 1 MHz offset. The noise from VCO1 is dominant at higher offset frequencies. Fig. 4.23 shows the phase noise comparison between the reference clock and the feedback clock at 16 MHz. These plots are coincident at offset frequencies lower than the loop bandwidth of 200 kHz, suggesting that the noise from the input reference is dominant within the loop bandwidth. The measured reference sideband levels are -54 dB, as shown in Fig. 4.24. These levels also need to be adjusted by 6 dB to account for the frequency division. Therefore, the reference sideband levels (spurs) are -48 dB.

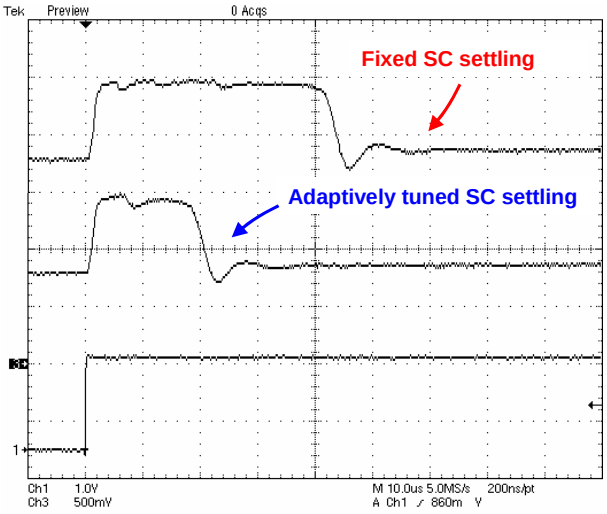


Figure 4.25: Comparison of the measured settling for the fine control voltages for the fixed and adaptively tuned SC circuits. The settling time is improved by a factor of 1.5.

To evaluate the adaptively tuned SC circuits, the settling behavior is measured when the division ratio N is changed from 260 to 263. In Fig. 4.25, the fine control voltages (V_{ctrl}) are initially close to V_{ref}. When N is increased, V_{ctrl} is increased

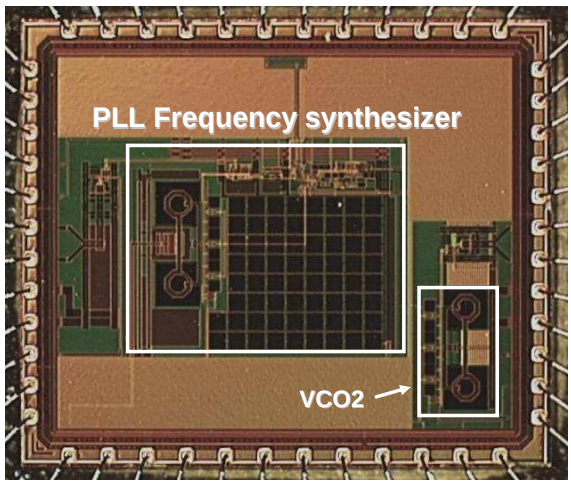


Figure 4.26: Die photo of the PLL frequency synthesizer and VCO2.

and saturates to V_{DD} until the coarse loop brings the PLL close to lock. Finally V_{ctrl} decreases and settles to V_{ref} when the PLL is in lock. Compared to the fixed SC circuit, the adaptively tuned SC circuit improves the settling time from 75 μs to 50 μs by a factor of 1.5.

The die photo of the prototype chip is shown in Fig. 4.26. The die areas of the PLL synthesizer and each VCO are 1.5 mm^2 (1.3 mm $\times$ 1.15 mm) and 0.25 mm^2 (0.7 mm $\times$ 0.36 mm), respectively.

Table 4.2 summarizes a comparison to previous work reported on integer-N frequency synthesizers operating in the 2 GHz to 5 GHz range. Different PLL architectures are noted in the comparison[3]. The noise performance of the proposed PLL frequency synthesizer compares well with previous publications. Additionally, a much faster settling time is measured in the PLL compared to the conventional analog split-tuning PLL.

[3]In [48], two CPs are used to drive two loop filters for the fine and coarse control paths.

Table 4.2: Summary and comparison of the PLL frequency synthesizer.

	[36]	[32]	[48]	[38]	This work
Architecture	traditional	digital-split	dual-loop	analog-split	analog-split
Technology	0.4-μm CMOS	0.25-μm CMOS	0.25-μm CMOS	0.12-μm CMOS	0.13-μm CMOS
Supply	2.6 V	2.5 V	2.5 V	1.5 V	1.5 V
Reference	11.75 MHz	13.3 MHz	4 MHz	25 MHz	16 MHz
Frequency	2.585-2.644 GHz	3.2-4.0 GHz	4.12-4.72 GHz	2.4 GHz	4.096 - 4.208 GHz
Die area	2.0 mm^2	1.7 mm^2	N.A.	0.7 mm^2	1.5 mm^2
Power	47 mW	93 mW	117.5 mW	31.8 mW	48 mW
Bandwidth	N.A.	N.A.	N.A.	2 MHz	200 kHz
Phase noise (at offset)	-115 dBc/Hz (at 10 MHz)	-118.5 dBc/Hz (at 1 MHz)	N.A.	-108 dBc/Hz (at 1 MHz)	-110 dBc/Hz (at 1 MHz)
Spurs	-53 dBc	-64 dBc	-45 dBc	N.A.	-48 dBc
Settling time	40 μs	150 μs	50 μs in simulation	few ms	50 μs

4.4 Discussion

Now we consider the impact of PVT variations on the proposed techniques. To compensate for the change in VCO gain K_o, the CP current I_{CP} should scale proportional to ${\omega_{osc}}^{-2}$. The CP tracking circuitry generates an output current as

$$I_{out} \propto (1 + \frac{\omega_H - \omega_L}{\omega_L} \cdot \frac{V_C}{V_{DD}})^{-2} \tag{4.26}$$

Ignoring the linear dependence of the coarse tuning curve, Eq. (4.26) illustrates that I_{CP} is sensitive to process variations due to the terms ω_H and ω_L. These

frequencies are given by

$$\omega_H = \frac{1}{\sqrt{L(C_{fix} + C_{min})}}$$
$$\omega_L = \frac{1}{\sqrt{L(C_{fix} + C_{max})}} \tag{4.27}$$

where C_{fix} is the tank capacitance excluding the varactor, such as the gate capacitances and parasitic capacitances. C_{min} and C_{max} are the minimum and maximum of the varactor capacitances across the control voltage, respectively. Let us define C_{ratio} as

$$C_{ratio} = \frac{C_{max}}{C_{min}} \tag{4.28}$$

Then it can be shown that

$$\frac{\omega_H}{\omega_L} = \sqrt{\frac{C_{max} + C_{fix}}{C_{min} + C_{fix}}} = \sqrt{\frac{C_{ratio} \cdot \frac{C_{min}}{C_{fix}} + 1}{\frac{C_{min}}{C_{fix}} + 1}} \tag{4.29}$$

With the values chosen in the PLL, a 10% variation in C_{fix} results in 1.3% and 2.7% variations in ω_H/ω_L and I_{out}, respectively. As a consequence, the difference between the designed and actual values of ω_H and ω_L would lead to only a small amount of error in the bandwidth control. Furthermore, this process dependence can be suppressed by calibrating the frequencies ω_H and ω_L during power-up.

Eq. (4.26) illustrates that the output current is susceptible to the supply noise. To alleviate this problem, a voltage regulator can be used for the CP circuitry. Because the PLL frequency is primarily controlled by the coarse loop, the reduced

CP voltage headroom due to supply regulation would not limit the frequency tuning range.

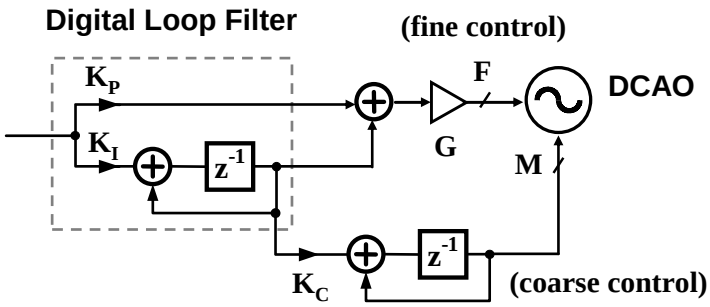


Figure 4.27: Migration of proposed techniques to a digital PLL.

The proposed techniques for designing a constant loop bandwidth PLL frequency synthesizer can also be migrated to digital PLLs. The block diagram of a possible implementation is shown in Fig. 4.27. Traditional designs use a digital control path with a digital word F. In parallel with this fine control, a coarse control with a digital word M is inserted. Similar to the analog split-tuning PLL, the coarse control can be achieved by adding another integral path across the loop filter. Assume the unit capacitances at the fine control node and the coarse control node are C_F and C_M, respectively. The oscillation frequency is then given by

$$\omega_{osc} = \frac{1}{\sqrt{L(C_{fix} + FC_F + MC_M)}} \tag{4.30}$$

The VCO gain K_o can be found to be

$$K_o = \left| \frac{\partial \omega_{osc}}{\partial F} \right| = \frac{L}{2} \cdot \omega_{osc}^3 \cdot C_F \tag{4.31}$$

Compared to Eq. (4.7), the voltage sensitivity of the analog varactor $|\partial C_{var}/\partial V_{ctrl}|$ is eliminated in digital PLLs. To maintain a constant loop bandwidth, again, the gain from the PD and the LF should scale proportional to ${\omega_{osc}}^{-2}$. This can be achieved by scaling the gain factor G (Fig. 4.27). From (4.30), we have

$$ {\omega_{osc}}^{-2} \propto (C_{fix} + FC_F + MC_M) \tag{4.32} $$

Assuming the oscillation frequency is mainly determined by the coarse loop, i.e., $FC_F \ll MC_M$, then

$$ G \propto {\omega_{osc}}^{-2} \propto (\frac{C_{fix}}{C_M} + M) \tag{4.33} $$

Consequently, a constant loop bandwidth that is insensitive to supply voltage is achieved in LC-VCO based digital PLLs. Although the ratio between C_{fix} to C_M is process dependent, this dependence may be suppressed by calibrating the capacitance ratio on chip.

4.5 Summary

This chapter describes an LC-VCO based PLL frequency synthesizer. Design techniques for maintaining a constant loop bandwidth have been presented. The loop bandwidth variation is mainly due to the change in the VCO gain K_o. Analysis shows that K_o is not only a strong function of the varactor, but also scales with the oscillation frequency. An analog split-tuning architecture has been adopted to suppress the dependence of K_o on the varactor. A CP tracking circuitry scales I_{CP}

with the oscillation frequency. The 1.5 V, 0.13-μm CMOS prototype IC measurement results have confirmed a relatively constant $K_o \cdot I_{CP}/N$, which determines the loop bandwidth. In VCOs, both the frequency tuning curve linearity and the phase noise performance are improved by using an averaging varactor. The concepts presented in the context of the prototype analog PLL frequency synthesizer can be easily migrated to a digital PLL.

Chapter 5 – Conclusion

The continued scaling of deep-submicron CMOS processes poses many challenges in the design of high-performance PLLs. These include the increased noise coupling between digital circuits and analog circuits, reduced voltage headroom, increased gate leakage current, and the difficulty in the modeling of active and passive devices, etc. Also, process, voltage, and temperature (PVT) variations are significantly increased. Therefore, PLL design techniques that address these problems are of importance.

5.1 Contributions

This dissertation focused on circuit techniques that can reduce the impact of PVT variations on the performance of VCOs and PLLs. Two issues with VCOs were considered in depth.

For ring VCOs, supply voltage sensitivity is a major design concern as the oscillation frequency of a ring VCO is highly dependent on the supply voltage. Conventional methods employ voltage regulation at the expense of reduced voltage headroom. However, supply regulation is not preferred in future scaled processes due to the reduced supply voltages. The supply voltage sensitivity can be also decreased by using compensation which, unfortunately, is sensitive to pro-

cess variations. To alleviate the problem, an on-chip calibration technique was developed. The optimum compensation for supply voltage sensitivity is achieved adaptively. Measurement results from a prototype chip confirmed robust operation in the presence of VCO supply noise for a large range of noise modulation frequencies. Therefore, this on-chip calibration technique offers an attractive alternative to the design of low-voltage supply noise insensitive ring oscillator based PLLs. Finally, a feasible implementation of a background calibration technique that would be robust to temperature variations was also presented.

Chapter 4 dealt with the design of a constant loop bandwidth LC-VCO based PLL frequency synthesizer. The loop bandwidth of a PLL synthesizer is a critical design parameter that controls almost all of the specifications. As a consequence, the PLL bandwidth has to be optimized and then be maintained in all frequency bands. The contribution of this work is to make the loop bandwidth constant once it has been optimized. Due to changes in the LC-VCO gain K_o, the PLL bandwidth varies significantly with operating frequency. Analysis shows that K_o is not only a strong function of the varactor, but also scales with ${\omega_{osc}}^3$. To suppress the dependence of K_o on the varactor, an analog split-tuning architecture was employed. A novel CP tracking circuitry that scales I_{CP} with the oscillation frequency was presented. By using an averaging varactor, both the frequency tuning curve linearity and the phase noise performance are improved in VCOs. A relatively constant $K_o \cdot I_{CP}/N$, which determines the loop bandwidth, was validated by the measurement results obtained from a prototype chip.

Although the proposed techniques were demonstrated in analog PLLs, the con-

cepts that have been presented in this dissertation can be easily migrated to digital PLLs. Compared to the prototype chips, digital implementations would be even simpler and more robust to PVT variations.

5.2 Suggestions for future work

With increasing variations in future deep-submicron processes, it is essential to consider PVT variations in the design of PLLs. New circuit techniques that can be explored include:

(1) Adaptive compensation for variations in the VCO gain of ring oscillators under PVT variations.

(2) Reduced K_o variations in LC VCOs. Using the techniques presented in Chapter 4, a relatively constant loop bandwidth over a wide-tuning range can be achieved. But K_o scales with ${\omega_{osc}}^3$, leading to performance variations with frequency. For instance, the level of reference sidebands, which is proportional to K_o (Eq. (2.22)), would vary substantially. Hence, it is desirable to compensate for the dependence of oscillation frequency on K_o within the VCO. By doing this, a constant loop bandwidth could be achieved with reduced K_o variations.

(3) Robust calibration techniques for LC-VCOs using bond-wire inductors. Passive bond-wire inductors offer the benefits of both low-cost and high-performance compared to on-chip inductors. However, bond-wire inductance varies significantly from chip to chip. As shown in Chapter 4, the loop bandwidth is proportional to the inductance value. Therefore, when bond-wire inductors are used in LC-VCO

based PLLs, robust calibration techniques are required for both frequency locking and loop bandwidth optimization.

(4) Development of an on-chip jitter/phase noise monitoring system. This real-time measurement will aid PLLs to achieve the optimum performance with a background calibration. Driven by process scaling, the design of such an on-chip monitor would be made simpler by using high-speed and low-cost digital circuits.

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