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Andrew Siv-Anne Chow for the degree of Master of Science in Electrical and Computer Engineering presented on May 10, 1990.

Title: Application and Analysis of CMOS FSCL for Mixed-Mode Analog/Digital ICs

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Sayfe Kiaei

The new CMOS folded source-coupled logic (FSCL) technique intended for mixed-mode integrated circuits has been designed. It has advantages over conventional CMOS circuit in terms of reduced current spike, circuit delay, logic flexibility, and layout density. A simple CPU implemented in 2 μm CMOS technology with a 5.0 volt supply has resulted in 500 μA current spike and operation frequency of 60 MHz.

Application and Analysis of CMOS FSCL for Mixed-Mode Analog/Digital ICs

by

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I would also like to thank my family members, especially my beloved wife, Jasmine, and friends for their love and encouragement during my pursuit of education at Oregon State University.

Most of all, I would like to thank my God for being my constant companion even when answers aren't enough.

... Of making many books there is no end, and much study wearies the body. Now all has been heard; here is the conclusion of the matter: Fear God and keep his commandments, for this the whole duty of man. For God will bring every deed into judgement, including every hidden thing, whether it is good or evil.

Ecclesiastes 12:11-14

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APPLICATION AND ANALYSIS OF CMOS FSCL FOR MIXED-MODE ANALOG/DIGITAL ICs

1. INTRODUCTION

The demand for greater levels of system integration in the ASIC market has pushed for an analog and digital circuit on the same chip. The mixed-mode analog/digital integrated circuit has not only provided high integration, but also low production costs, high performance, and ease of implementation [1]. There is a problem when having the analog and digital circuit on the same chip. This problem is due to digital switching noise finding its way into the sensitive analog circuit. This will limit the analog circuit dynamic range. The dynamic range is measured as the usefulness of the analog circuit. As a result, chip performance is limited [2].

The noise spikes in digital VLSI circuits were summarized by Wallmark [3]. In general, there are two distinct sources of noise in CMOS VLSI chip. The first is an induced noise that is the noise voltage coupled from one signal node to adjacent nodes. Shoji has discussed the induced noise in conventional CMOS circuits [4]. The other is power bus noise, due to the current spikes of conventional CMOS circuit effects on resistance and inductance, which affects all circuits on the chip a through common substrate.

The current spike is generated every time a conventional CMOS gate changes state as shown in Figure 1. When a large number of conventional CMOS gates change state simultaneously, several milliamperes of current spike will be generated [5][6]. As the current spike flows through power and ground lines, there is a voltage drop in the resistance (IR) and the inductance (LdI/dt). In order to prevent latch-up, the substrate of PMOS is connected to the power line and NMOS is connected to the ground line. This voltage drop will result in a noise to the circuit. This noise will penetrate through power lines, ground lines, and the common substrate into the analog circuitry [7].

As to date, there are three methods being used to minimize the current spike noise. One method uses a differential pair as an input for an analog circuit to desensitize the analog circuit from the current spike noise. The second method uses separate power lines and ground lines for the noisy and quiet channels. It also uses guardring by introducing diffusion lines to isolate noisy channels from quiet channels. Additional pins and separate pads are sometime used. The third method reduces the substrate contact in the digital circuit to prevent the digital circuit from generating the current spike [8].

However, as the speed of the digital circuit is increased, more current spike will be generated. The above methods mentioned will no longer be as effective in

minimizing the noise. Therefore, a new design technique is needed. The objectives of this thesis are to (1) develop a new design technique for minimizing current spike noise (2) investigate the current spike noise of the new design and compare it with the conventional CMOS gate (3) design a simple CPU chip for testing the functionality and performance of this new design technique. This new design technique is comprised of CMOS source-coupled logic (SCL) and CMOS folded source-coupled logic (FSCL). In the sections to follow, the design and analysis of CMOS source-coupled logic (SCL), CMOS folded source-coupled logic (FSCL), and simple CPU will be discussed.

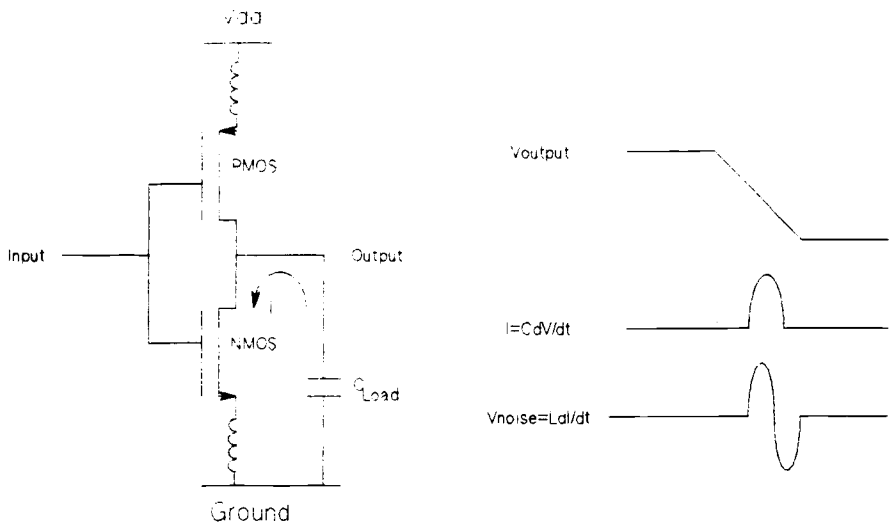

Figure 1 Conventional CMOS current spike noise

2. CMOS SOURCE-COUPLED LOGIC (SCL)

Power bus noise generated by the current spike of conventional CMOS circuit is large when there are a large number of gates switching simultaneously. In the mixed-mode integrated circuit application, this power bus noise will significantly degrade the accuracy of analog circuit. As the digital speeds increase, analog resolution will increase, and additional analog circuitry will be included. As a result, power bus noise will be worsened. Therefore, it is necessary to minimize the current spike generated by CMOS circuit.

One method to minimize the digital circuit noise is by maintaining a constant current flow. This will eliminate the current spike. With this strategy in mind we have found in my lab that the source-coupled pairs design technique to be the ideal solution. A CMOS source-coupled logic (SCL) inverter, as shown in Figure 2, uses the emitter-coupled-logic (ECL) design technique. The ECL is commonly used in bipolar technology [9][10]. In the following, CMOS SCL operation, current spike, and power consumption will be analyzed.

2.1. CMOS SCL OPERATION

The operation of a current-source-biased NMOS source-coupled pair is fundamental to the CMOS SCL operation. Thus, in the paragraphs to follow, the basic

operation of a current-source-biased NMOS source-coupled pair will be discussed.

The basic operation of a current-source-biased NMOS source-coupled pairs is to steer the bias current flow through Q_1 or Q_2 as shown in Figure 3. A few assumption are made with this operation; Q_1 and Q_2 are matched, lambda and gamma effect are negligible, and Q_1 and Q_2 are operated in saturation region. The steering mechanism will be dependent on the differential input voltage (V_{id}). The sum of the two input voltage sources and the two gate-to-source voltage of NMOS devices are as follows [11]:

$$V_{in1} - V_{gs1} - V_{gs2} - V_{in2} = 0 \qquad (1.1)$$

$$V_{in1} - V_{in2} = V_{gs1} - V_{gs2} \qquad (1.2)$$

$$V_{id} = V_{in1} - V_{in2}$$

$$V_{gs} = [I_d/(K/2)]^{\frac{1}{2}} + V_t \qquad (1.3)$$

Where

$$K = [K_p(W/L)] \qquad (1.4)$$

K_p = the intrinsic transconductance

W = the wide of the transistor

L = the length of the transistor

V_{gs1} = gate-to-source voltage of transistor Q_1

V_{gs2} = gate-to-source voltage of transistor Q_2

V_{in1} = input voltage source

V_{in2} = input voltage source

Substituting equation (1.3) into equation (1.2)-

$$V_{id} = [I_{d1}/(K/2)]^{\frac{1}{2}} + [I_{d2}/(K/2)]^{\frac{1}{2}} \qquad (1.5)$$

$$I_{ee} = I_{d1} + I_{d2} \tag{1.6}$$

Substituting equation (1.6) into equation (1.5) and forming a quadratic-

$$AI_{d1}^2 - BI_{d1} + C = 0 \tag{1.7}$$

Where

$A = 1$

$B = I_{ee}$

$C = [(I_{ee}/2) - ((KV_{id}^2)/4)]^{\frac{1}{2}}$

Solving the quadratic equation-

$$I_{d1} = (I_{ee}/2) + (I_{ee}/2)[[(KV_{id}^2)/I_{ee}] - \tfrac{1}{4}[(KV_{id}^2)/I_{ee}]^2]^{\frac{1}{2}} \tag{1.8}$$

$$I_{d1} = (I_{ee}/2) - (I_{ee}/2)[[(KV_{id}^2)/I_{ee}] - \tfrac{1}{4}[(KV_{id}^2)/I_{ee}]^2]^{\frac{1}{2}} \tag{1.9}$$

The equation (1.8) and (1.9) is valid only when both devices are operated in the saturation region, this is true if

$$[(KV_{id}^2)/I_{ee}] \leq 2 \tag{1.10}$$

$$V_{id} = [I_d/(K/2)]^{\frac{1}{2}} \tag{1.11}$$

Therefore, the differential input voltage required to cut off one of the device is a function of bias current and device size.

The minimum differential input voltage required to cut off one of the device in a balance condition when the differential input voltage is zero is

$$V_{id}(Min) = [2]^{\frac{1}{2}}[(I_{ee}/2)/((K/2)]^{\frac{1}{2}} \tag{1.11}$$

$$V_{id}(Min) = [2]^{\frac{1}{2}}V_{ds1} \tag{1.13}$$

$V_{ds1} \approx 300$ mV for subthreshold region

$$V_{id}(Min) \approx 420 \text{ mV} \quad (1.14)$$

approximately 500 mV. The NMOS differential pairs switching mechanism is simulated and shown in Figure 4. As the current flow through transistor Q_1 (I_{d1}) increases, the current flow through transistor Q_2 (I_{d2}) then decreases and vice versa. When the differential input voltage reaches above its minimum, the bias current will flow through one side of the NMOS differential pairs only.

A complete circuit of a CMOS SCL inverter is shown in Figure 5. It consists of two stages. The first stage, input stage, is a NMOS source-coupled pairs and the second stage, output stage, is a NMOS source-follower circuit. The function of the input stage is to steer the bias current flow through one side only based on applied input voltages. The differential input voltage (V_{id}) of 800 mV is designed for the input stage operation. The input voltage swing required to steer the bias current is as follows. Starting from a balance condition where V_{in1} is equal to V_{in2}, the bias current is divided equally between Q_1 and Q_2. An increase of V_{in1} by 800 mV will cause virtually all of the bias current to flow through Q_1. Conversely, an increase of V_{in2} by 800 mV will cause virtually all the bias current to flow through Q_2. The output voltage is determined by the PMOS diode-connected transistors Q3 and Q4. The desired differential output voltage (V_{od}) is obtained by sizing the transistors Q3 and Q4.

$$V_{od} = [I_d/(K/2)]^{\frac{1}{2}} \qquad (1.15)$$

The differential output voltage of 1 V is designed for the output stage operation. This will provide a noise margin of 200 mV. The function of the output stage is to shift the output voltage level down. This will make the output voltage compatible with the voltage required to drive the input of another CMOS SCL circuit. The output stage is designed to provide an output voltage logic high of 3.85 V and logic low of 2.85 V. The speed of the CMOS SCL circuit is based on the size of transistors Q_5 and Q_6. The desired speed can be obtained by sizing the transistors Q_5 and Q_6 appropriately to drive the capacitance load.

2.2. CMOS SCL CURRENT SPIKE NOISE

Ideally, the CMOS SCL circuit will not generate any current spike due to the fact that the current flow through the circuit is constant. However, this is not so. The NMOS source-follower has to charge and discharge the load capacitance. The current flow from power supply line, Vdd, into the drain of transistor Q5, Id5, plus the displacement current, CLdVout/dt, is equal to the bias constant current, IL. The displacement current causes the current flow from power supply line into transistor Q5 to be no longer constant. Thus, there will be some current spike generated by the CMOS SCL circuit. Since the overlap current in Id5 (which is caused by the displacement current) is

complementary to the overlap current in Id6, some of the overlap current will cancel out each other and the differential output voltage will be small. This current spike will be relatively small compared to the conventional CMOS circuit.

2.3. CMOS SCL POWER CONSUMPTION

Power dissipation in the CMOS SCL circuit is due to two parts. The first part is due to the internal switching current (input stage). The other part is due to the output load currents (NMOS source-follower). The internal switching current and output load current are dependent on the designer's choice. Since these current sources and supply voltage are constant, the power dissipation in CMOS SCL circuit is fixed and independent of switching frequencies. This is unlike the conventional CMOS circuit where its power dissipation is dependent on the switching frequency. The power dissipation of CMOS SCL circuit is compatible to the conventional CMOS circuit in the high frequencies.

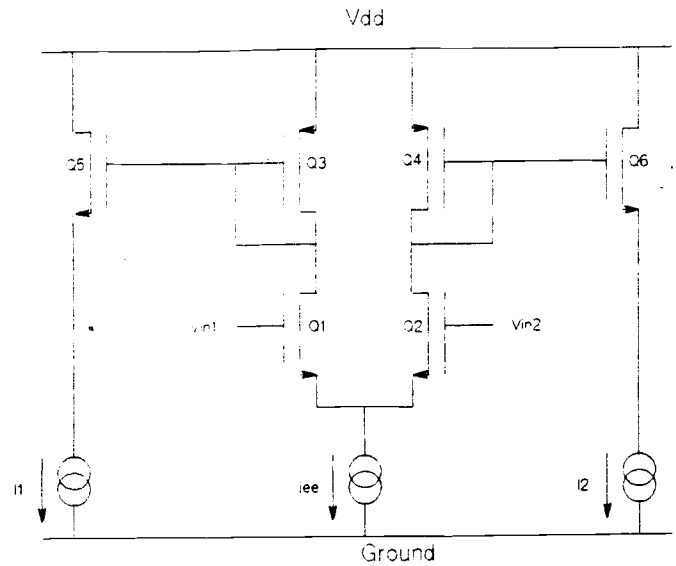

Figure 2 CMOS source-couple logic (SCL) circuit

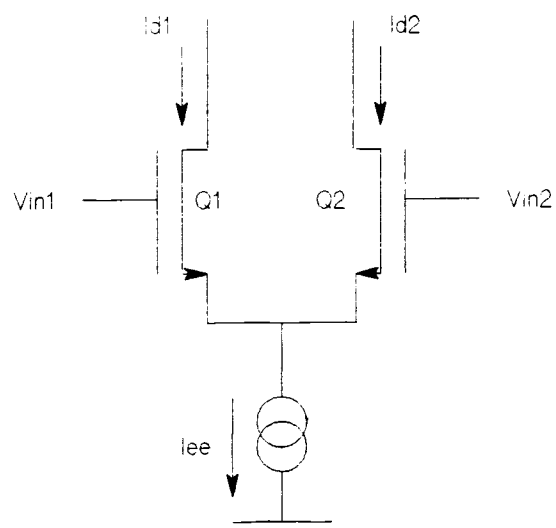

Figure 3 NMOS source-couple pair circuit

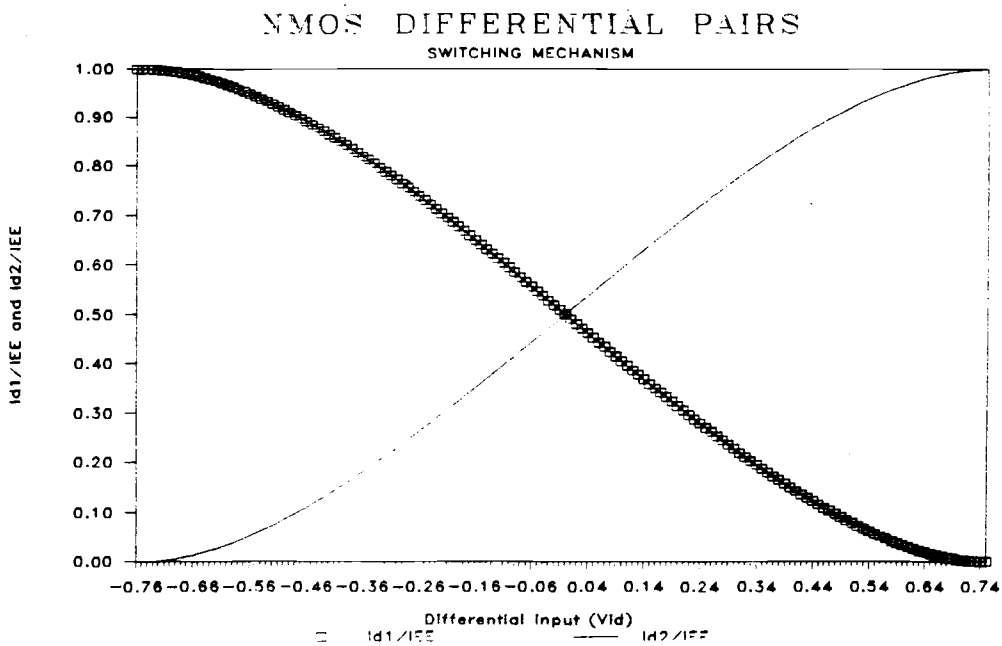

Figure 4 NMOS source-couple pair output waveform

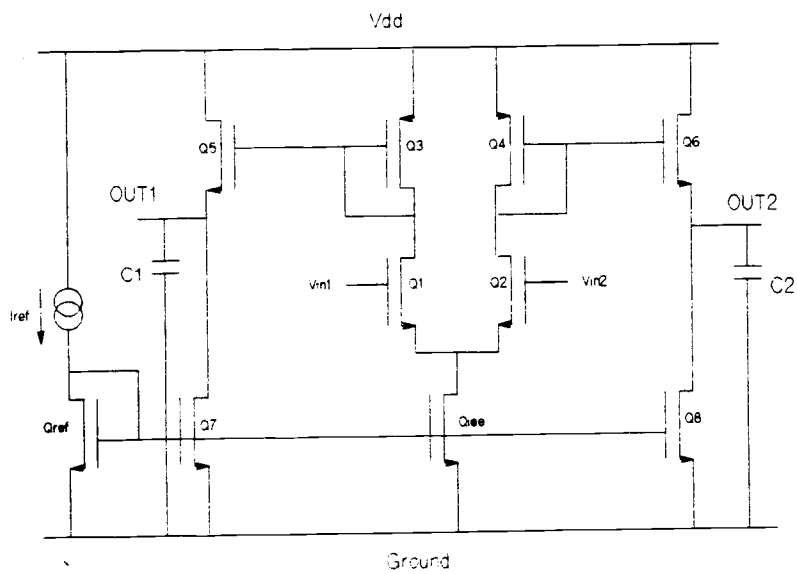

Figure 5 A complete circuit of CMOS SCL inverter

3. CMOS FOLDED SOURCE-COUPLED LOGIC (FSCL)

Based on the principles of the CMOS SCL circuit (discussed in the preceding section), a CMOS Folded Source-Coupled Logic (FSCL) circuit is designed. The CMOS FSCL circuit is mainly derived from the folded cascode amplifier [12][13]. The motivation is as follows; the mirror of Q3/Q5 is not used to reflect signal current from drain of Q1 to the source of Q5. Likewise, the mirror of Q4/Q6 is not used to reflect signal current from drain of Q2 to the source of Q6. Instead, these currents are directly injected into the drain of Q5/Q6. This will maintain a constant current flow from Vdd to the internal switching current due to a bias constant current source is directly injected into the internal switching current. This will also eliminate the need for transistors Q4 and Q3. Thus, a smaller current spike and a faster speed than the CMOS SCL circuit are expected to be generated by CMOS FSCL circuit. Again, the idea is to use NMOS source-coupled pairs to steer the current flow through one branch or the other. In following, a design of CMOS FSCL circuit, its current spike, fanout, and power consumption will be discussed.

3.1. CMOS FSCL Operation

The operation of the CMOS FSCL circuit is very similar with the CMOS SCL circuit. Again, there are two stages. The first stage is the input which is the internal

current switching mechanism. Its purpose is to steer the bias current flow through one branch or the other. The second stage is the output. The output voltages are based on the voltage drop across the source and gate of PMOS transistors Q_{B1} and Q_{B2} which are dependent on the amount of current flow through them and the transistors size ratio (W/L). The output voltage swing, output voltage logic low, output logic voltage high, and input differential voltage swing are calculated as follows:

Output Low (V_L):

$$V_{sg1} = [I_{b1}/(K/2)]^{\frac{1}{2}} + V_{tpb1} \tag{2.1}$$

Where

$$V_{tpb1} = V_{tp} + \tau[(V_{SBL} + 2\mu_F)^{\frac{1}{2}} - (2\mu_F)^{\frac{1}{2}}]$$

$$I_{b1} = I_{sup1} - I_{d1}$$

Output High (V_H):

$$V_{sg1} = [I_{b1}/(K/2)]^{\frac{1}{2}} + V_{tpb1} \tag{2.2}$$

Where

$$V_{tpb1} = V_{tp} + \tau[(V_{SBH} + 2\mu_F)^{\frac{1}{2}} - (2\mu_F)^{\frac{1}{2}}]$$

$$I_{b1} = I_{sup1}$$

Output Swing (V_{od}):

$$V_{od} = V_H - V_L$$

$$V_{od} = [I_{b1}/(K/2)]^{\frac{1}{2}} - [(I_{sup1} - I_{d1})/(K/2)]^{\frac{1}{2}} + V_{tpb1} \tag{2.3}$$

Where

$$V_{tpb1} = V_{tp} + \tau[(V_{SBH} + 2\mu_F)^{\frac{1}{2}} - (V_{SBH} + 2\mu_F)^{\frac{1}{2}}]$$

Input Swing (V_{id}):

$$V_{id} = [I_{b1}/(K/2)]^{\frac{1}{2}} \qquad (1.11)$$

The CMOS FSCL inverter is shown in Figure 6. A differential input voltage (V_{id}) of 0.85 volt, output voltage (V_{od}) of 1 volt, noise margin of 150 mV, current supply (Isup1 or Isup2) of 200 μA, steering current (Iee) of 120 μA, the output voltage logic high (V_H) of 3.85 volt and output voltage logic low (V_L) of 2.85 volt are chosen. Substituting these values in equation (1.11) and equation (2.1), this will give the sizes of NMOS differential pairs of W = 15 μm and L = 2 μm, the sizes of transistors Qp1, Qp2 of W = 20 μm and L = 2 μm, the sizes of transistors Qb1, Qb2 of W = 8 μm and L = 2 μm, and the size of transistor Qiee of W = 11 μm and L = 2 μm.

The operation of CMOS FSCL inverter is as follows; transistor Q1 is assumed on and Q2 assumed off. Thus, all the bias current, Iee, flown through Q1 and the current flow into the source of Qb1, Ib1, are decreased by the amount of bias current, Iee. This will define the output voltage at node OUT1 as logic low. On the other side, all the supply current, I2, is flown into the source of Qb2. This will define the output voltage at node OUT2 as logic high. If transistor Q2 is on and Q1 is off, the output voltage at node OUT2 will be defined as logic low and node OUT1 as logic high.

3.2. CMOS FSCL Current Spike

Ideally, there will not be any current spike generated by the CMOS FSCL circuit since there is only constant current flow from the supply line, Vdd, into the circuit. Thus, the displacement current, CLdV/dt, will not effect the supply line noise unlike the CMOS SCL circuit.

The comparison between a current spike generated by CMOS FSCL inverter and conventional CMOS inverter is shown in Figure 7. The same NMOS sizes are used for making a comparison. CMOS FSCL inverter generates about 12 μA of current spike where as conventional CMOS inverter generates about 2000 μA of current spike. This resulted in a reduction of two orders of magnitude of current spike.

3.3. CMOS FSCL Fanout

The comparison between a fanout of the CMOS FSCL inverter and conventional CMOS inverter is shown in Figure 8. The CMOS FSCL inverter propagation delay is compatible to the conventional CMOS inverter. The rise and fall time of the CMOS FSCL inverter is about two times slower than the CMOS static inverter. The driving strength of the CMOS FSCL inverter is dependent on the devices size ratio (W/L) of transistors Q_{B1} and Q_{B2}, transconductance of the differential pair, and the supply current.

3.4. CMOS FSCL Power-Delay-Product

The speed power delay product is shown in Figure 9. The sizes of the NMOS source-coupled pairs can be chosen based on the amount of power dissipation and propagation delay. Since the propagation delay is relatively constant, the sizes of the NMOS source-coupled pairs are chosen based on the least amount of power dissipation. Power dissipation is compatible with conventional CMOS circuits and dependent on the speed of operation.

3.5. Design Procedures for CMOS FSCL Circuits

The CMOS FSCL circuit has many advantages over the conventional CMOS circuit. There are less transistors used especially in the PMOS. The circuit delay is shorter since a number of delay stages are compressed into a single delay stage. This also reduced the chip area. The major advantage of CMOS FSCL circuit is the logic flexibility, especially the complex function [14]. Another advantage is that the output of a CMOS FSCL circuit is fully differential. Thus, both outputs of logic function are available.

There are two parts involved in design the CMOS FSCL circuit (Figure 10). The first part is the internal current switching mechanism which consists of cascoding a MOS source-coupled pairs. The complex Boolean logic functions can be designed within a single circuit delay by cascoding

MOS differential pairs into combinational logic tree networks. There are several method that have been used to design these combinational tree networks. The first method is the Algebraic technique which involves decomposition and factorization the Boolean function. The second method is the Karnaugh map (K-map) techniqueS which can handle up to five variables. More than five variables K-map technique will be too complex to use. The third method is the Tabulation technique [15][16][17]. The design of this internal current switching mechanism can be done in an automatic fashion by stacking MOS differential pairs onto the previous one as shown in Figure 11. Depending on the logic function, either a two MOS differential pairs or a one MOS differential pairs is used to stack onto the previous one. The second part in designing the CMOS FSCL circuit is the output stage. The output stage is independent of the internal current switching mechanism. Its consists of the constant current sources, Qp1 and Qp2, and bias PMOS transistors, Qb1 and Qb2. Transistors, Qb1 and Qb2, define logic high and low of the circuit.

3.6. CMOS FSCL NAND/AND GATE

The CMOS FSCL NAND/AND gate is shown in Figure 12. The design of the CMOS FSCL NAND/AND gate involves two stages, the input stage and the output stage. The output stage has been described early. Given the constant current source and output voltage logic high and low, the size of transistors, Qp1, Qp2, Qb1, and Qb2 can be calculated. The

input stage consist of stacks NMOS differential pairs. The design of input stage involves two steps. The first step is to minimize the expression. This can be done by either the algebraic method, or K-map method, or tabulation method. The second step is to factor out the expression into subexpression where input A will be one subexpression and inverted input A will be the other subexpression. This subexpression is again factored out into another subexpression within its subexpression. This process will continue until to the last variable. After the expression is minimized and factored, the designing of the input stage is done by cascoding the NMOS source-coupled pairs and connecting the appropriate logic signals together. For the two-input-NAND/AND gate, its signals are as follows:

NAND = A*B

Given the bias current source, Iee, the sizes of the NMOS differential pairs transistors are calculated as described earlier and the sizes of NMOS differential pairs are all the same.

The comparison between a current spike generated by CMOS FSCL NAND/AND gate and conventional CMOS NAND gate is shown in Figure 13. The same NMOS device sizes are chosen for making the comparison. With CMOS FSCL circuit, a two orders of magnitude of noise has been reduced.

The fanout of the CMOS FSCL NAND/AND gate is shown in Figure 14. The driving strength of CMOS FSCL NAND/AND

gate is dependent on the device sizes of the transistors Q_{B1} and Q_{B2}, transconductance of the differential pair, and the supply current.

3.7. CMOS FSCL NOR/OR GATE

The CMOS FSCL NOR/OR gate is shown in Figure 15. The CMOS FSCL NOR/OR gate is the same as the CMOS FSCL NAND/AND gate except that the input signals are inverted (by De Morgan's Theorems). Thus, the CMOS FSCL NOR/OR gate circuit parameters and the circuit behavior will be the same as the CMOS FSCL NAND/AND gate.

3.8. CMOS FSCL Other Gate

A CMOS FSCL NXOR/XOR gate is shown in Figure 16. The design of a two-input-NXOR/XOR is as follows:

XOR = A'*B + A*B'

By cascoding the NMOS source-coupled pairs and connecting the appropriate signals together, the circuit is constructed.

A CMOS FSCL D-Flip/Flop gate is shown in Figure 17. The design of a D-Flip/Flop signals is as follows:

Q = D'*CLK + Q*CLK'

By cascoding the NMOS source-coupled pairs and connecting the appropriate signals together, the circuit is constructed.

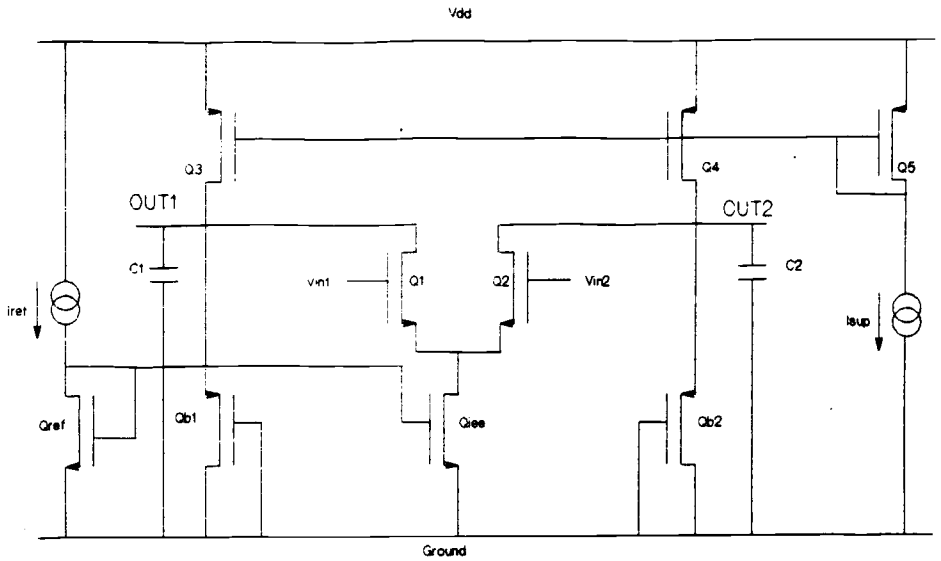

Figure 6 CMOS FSCL inverter circuit

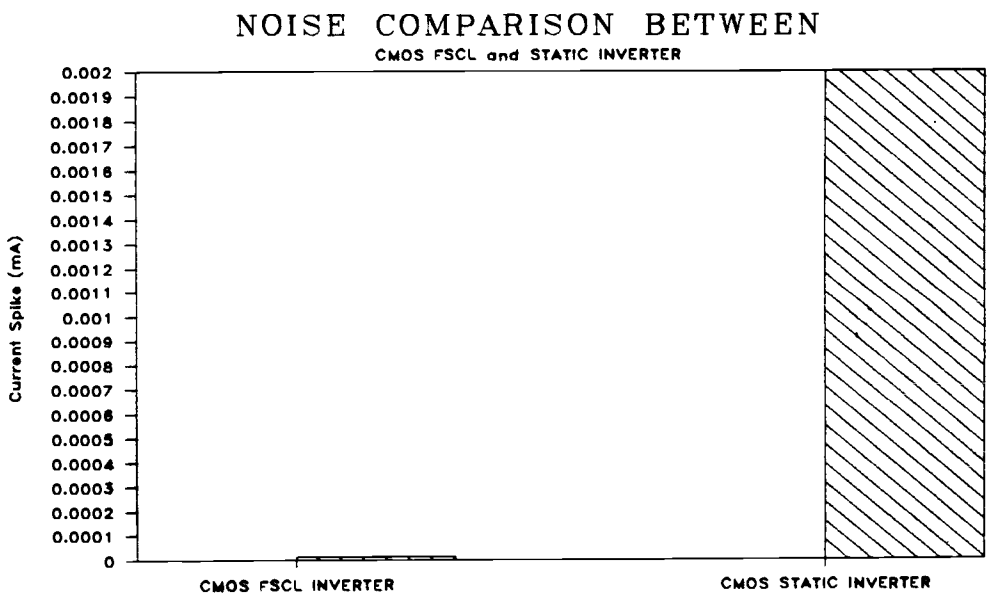

Figure 7 The comparison between the current spike generated by CMOS FSCL and conventional CMOS inverter circuit.

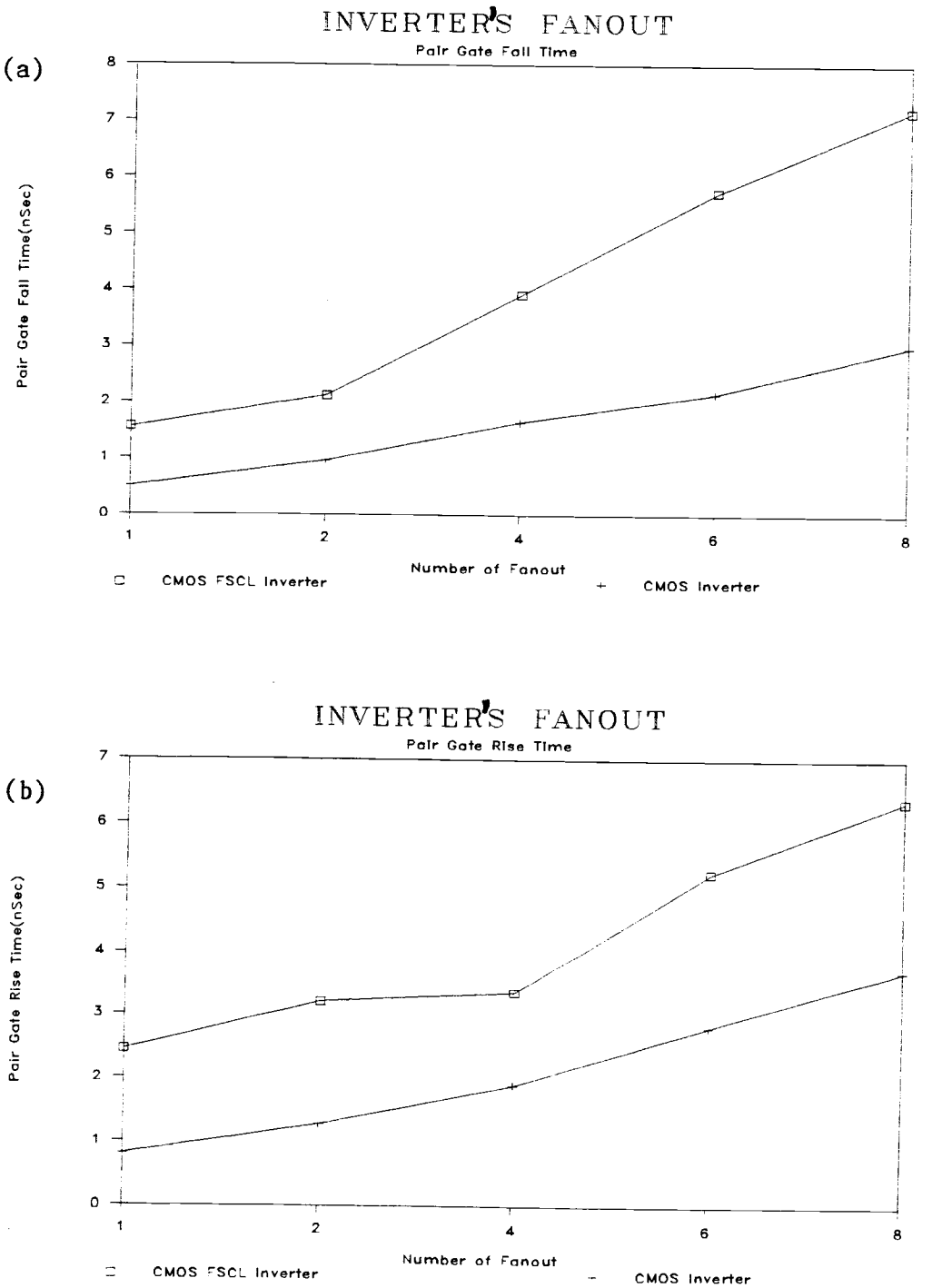

Figure 8 The comparison between a fanout of the CMOS FSCL and conventional CMOS inverter.

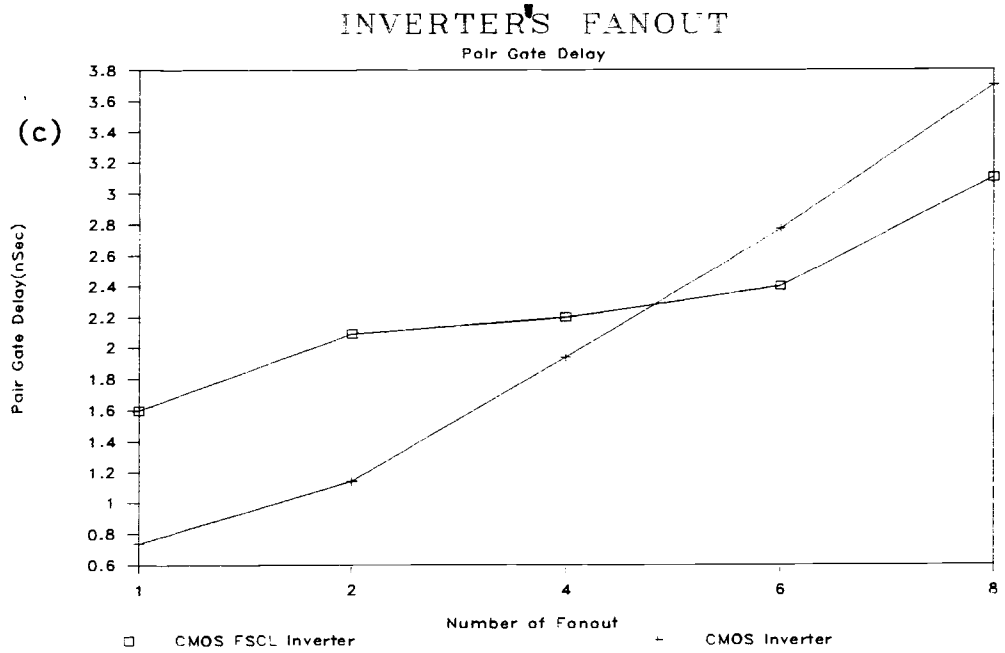

Figure 8 Continued.

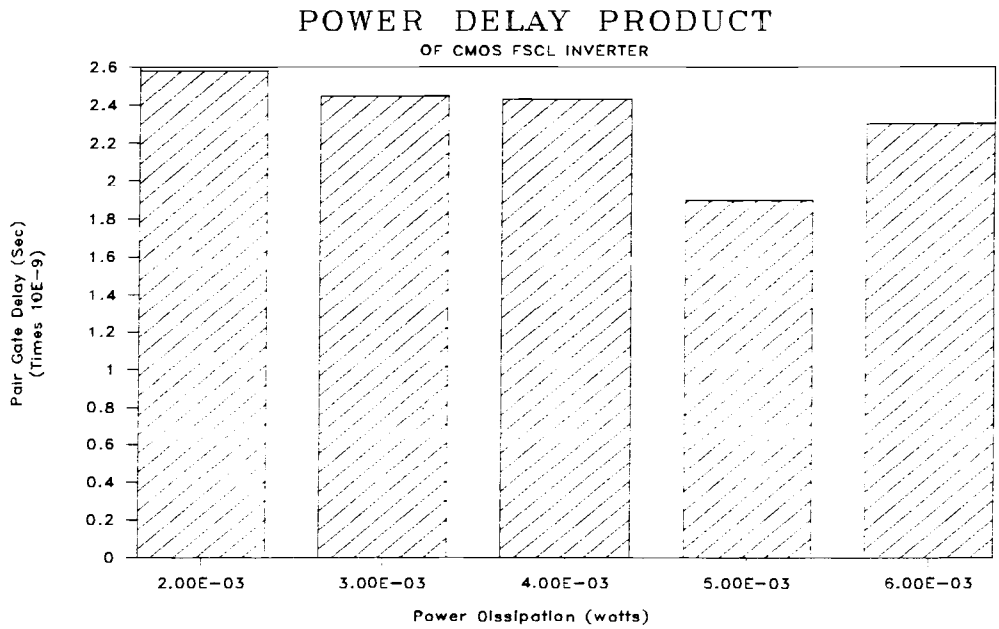

Figure 9 The speed power delay product

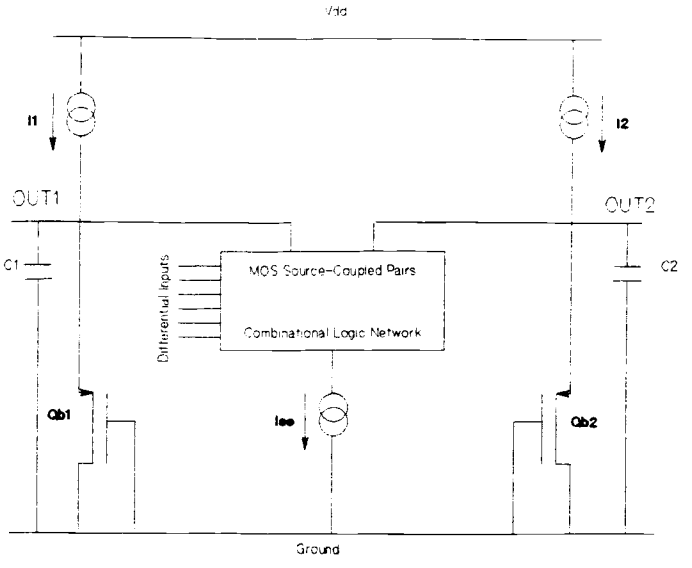

Figure 10 The basic building block of CMOS FSCL circuit

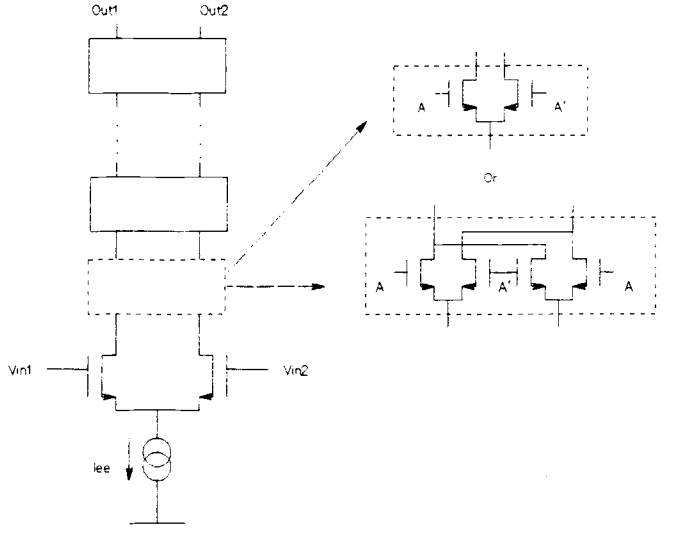

Figure 11 The basic building block of internal current switching mechanism

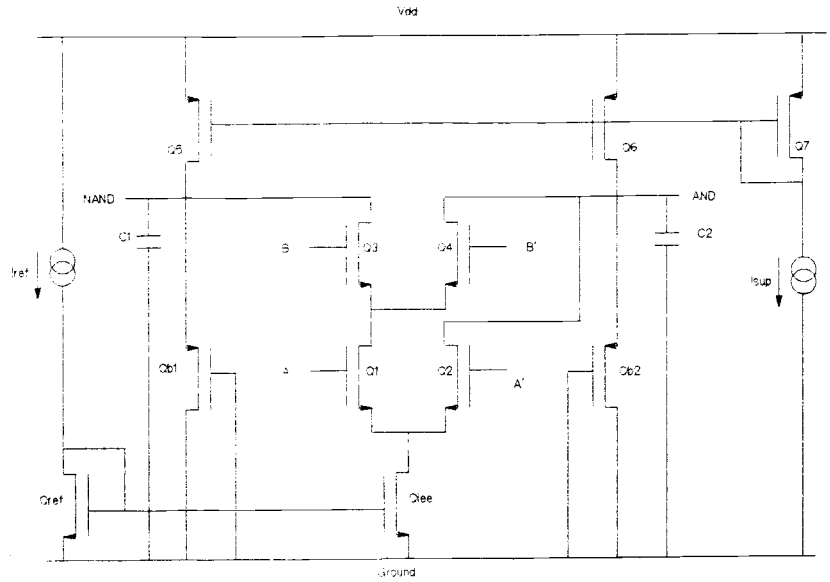

Figure 12 CMOS FSCL NAND/AND circuit

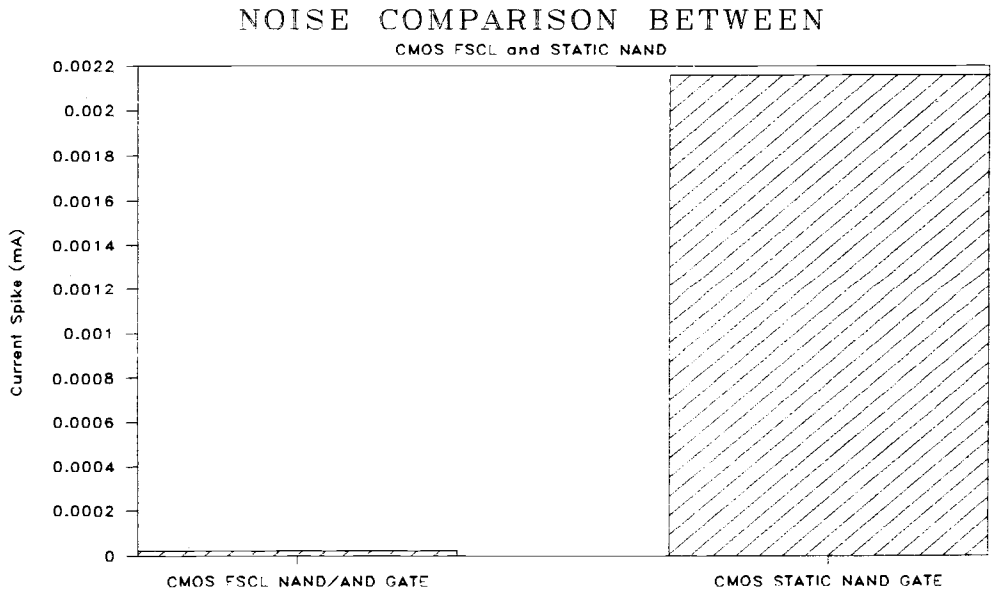

Figure 13 The comparison between the current spike generated by CMOS FSCL and conventional CMOS NAND/AND circuit.

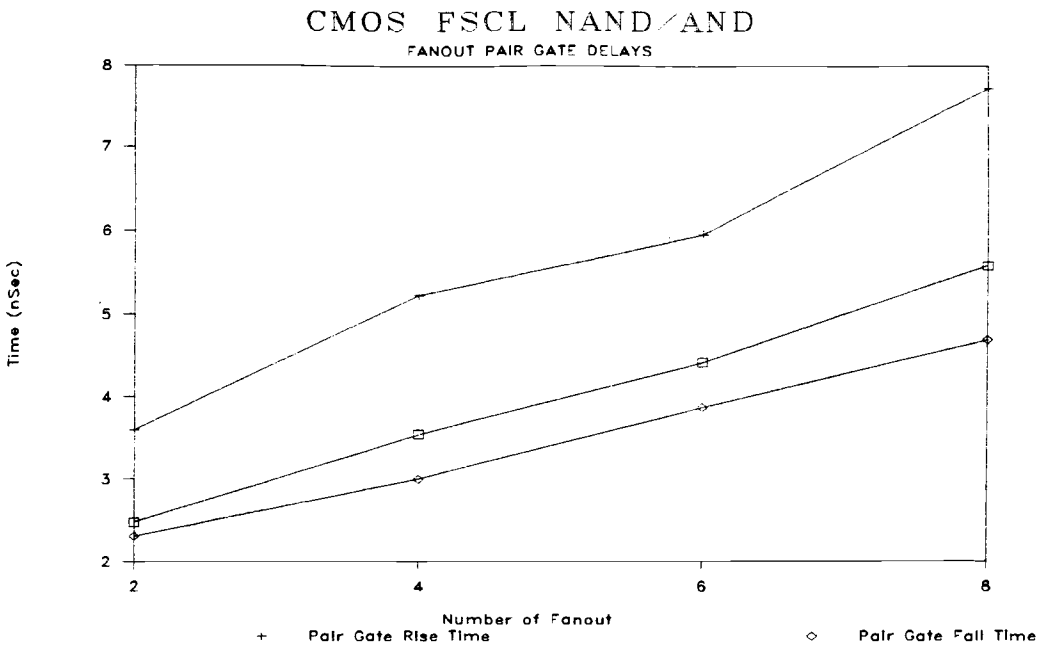

Figure 14 The comparison between a fanout of the CMOS FSCL and conventional CMOS NAND/AND circuit.

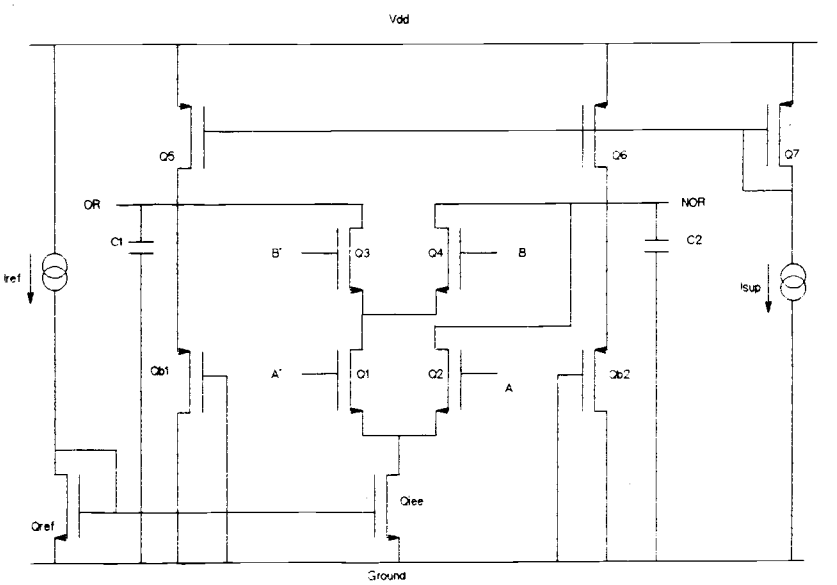

Figure 15 CMOS FSCL NOR/OR circuit

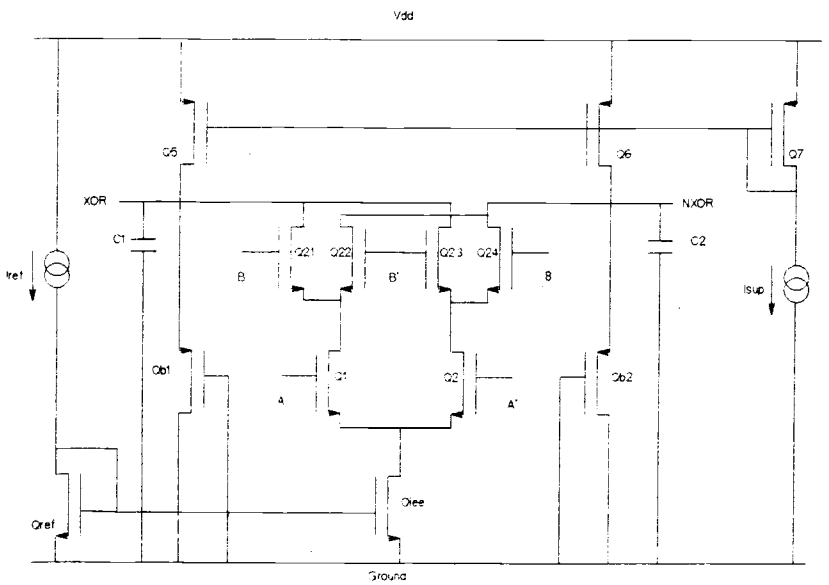

Figure 16 CMOS FSCL NXOR/XOR circuit

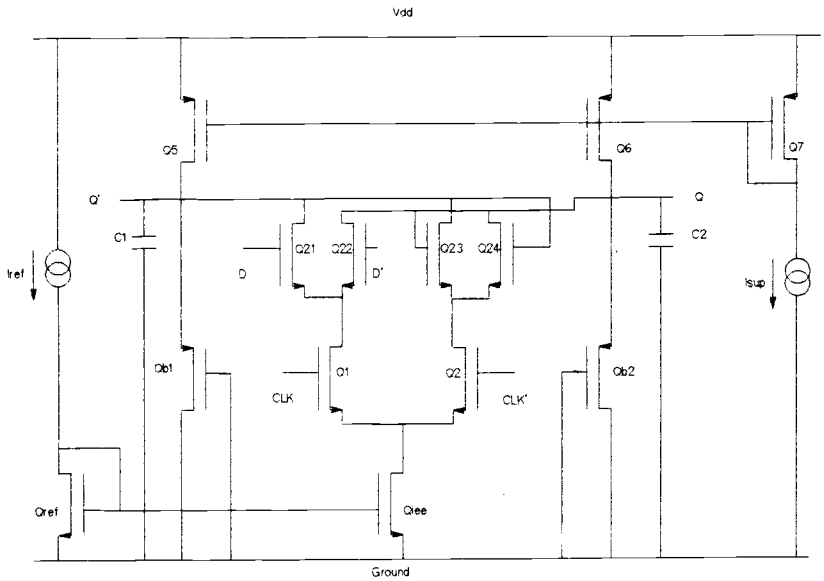

Figure 17 CMOS FSCL D-F/F circuit

4. A SIMPLE CPU

A simple CPU of 4bit adder and comparator has been designed to test the functionality and performance of the CMOS FSCL circuit. A block diagram of the simple CPU is shown in Figure 18. It is consists of two input-buffers, two input-registers, two output-buffers, two output-registers, a 4bit adder, and three 4bit comparators. A total of 28 pins were used. Eight were designated for data inputs, eight for data outputs, two for clocks, two for bias current sources, four for noisy power supply lines, and four for quiet power supply lines. The area of the tiny chip is about 2500 X 2300 μm square. The K-map method is used for minimizing the Boolean functions for this design. In the following, the design of a 4bit adder and comparator, output buffer, input buffer, and performance is discussed.

4.1. CMOS FSCL 4bit adder

A ripple adder technique was used to design the CMOS FSCL 4bit adder. A CMOS FSCL 1bit adder is shown in Figure 18. The design of a full adder requires two CMOS FSCL circuits. One is to perform the carry function and another to perform the sum function. The minimal Boolean expression of the sum function is as follows:

Sum = A'*B'*Cin + A'*B*Cin' + A*B'*Cin' + A*B*Cin

This is a three-input-exclusive-OR function. Factor this expression into subexpression as follows:

Sum = Cin*(A'*B' + A*B) + Cin'*(A'*B + A*B')

From this expression, the sum function can be designed by cascoding a two NMOS differential pairs and connecting the appropriate signals together. The CMOS FSCL sum circuit is constructed as shown in Figure 19A. The minimal Boolean expression of the carry function is

Carry = A*B + A*C + B*C

Factor this expression into subexpression

Carry = C*(A + B) + A*B

Where

(A + B) = A'*B + A*B' + A*B

Thus, the expression of carry function is

Carry = C*(A'*B + A*B') + A*B

By cascoding a two-NMOS-differential-pairs and one-NMOS-differential-pairs and connecting the appropriate signals together, the CMOS FSCL carry function is constructed as shown in Figure 19B. The 4bit adder is constructed by cascading four of the 1bit adder.

4.2. CMOS FSCL 4bit comparator

A 4bit comparator consists of an equal-flag, greater-than-flag, and less-than-flag functions. The CMOS FSCL circuit provides many advantages. It provides a fully differential output, very small current spike, and uses fewer transistors than conventional CMOS circuit. Many more advantages were mentioned previously. The CMOS FSCL circuit

also has its own disadvantages especially fanin limitation. Right now the CMOS FSCL circuit can handle 3 or 4 fanins only. This limitation is due to the design parameters. As the stacked NMOS differential pairs get higher, the driving strength of the input voltage sources are weakened. As a result, the differential input voltage source is no longer able to cause the NMOS differential pairs to steer the bias current flow through one branch only. This disadvantage can be eliminated by having different design parameters. One of the parameters is the differential input voltage. Instead of having 1 volt, 2 or 3 volts can be used to drive the input stage. There will be more details on this in the conclusion section where future works will also be discussed. The truth table is listed in Table I [18]. In the following, the equal-flag, greater-than-flag, and less-than-flag function will be analyzed.

4.2.1. CMOS FSCL Equal-Flag Circuit

The CMOS FSCL equal-flag circuit is shown in Figure 20. The Boolean expression of the 4bit equal-flag function is derived directly from its truth table, Table I, as shown below:

EQUAL = (A3*B3 + A3′*B3′)*(A2*B2 + A2′*B2′)*(A1*B1 + A1′*B1′)*(A0*B0 + A0′*B0′)

The fanin limitation causes the CMOS FSCL equal-flag circuit to divide into subcircuits. Each of the four subcircuits is

used to perform 1bit equal-flag function and connected together using the FSCL CMOS AND gates. The 1bit CMOS FSCL equal-flag circuit is shown in Figure 20A. The design of the 1bit CMOS FSCL equal-flag circuit is straightforward. By cascoding a two-NMOS-differential-pairs and connecting the appropriate signals together, the circuit is constructed. By connecting a four 1bit CMOS FSCL equal-flag circuit together with a four input AND gate, the 4bit CMOS FSCL equal-flag circuit is constructed (Figure 20B).

4.2.2. CMOS FSCL Greater-Than-Flag Circuit

The CMOS FSCL greater-than-flag circuit is shown in figure 20. The Boolean expression of the 4bit greater-than-flag function is derived directly from its truth table, Table I, as shown below:

GREAT = (A3*B3′) + (A3*B3 + A3′*B3′)*[(A2*B2′) + (A2*B2 + A2′*B2′)*[(A1*B1′) + (A1*B1 + A1′*B1′)*(A0*B0′)]]

This expression is divided into subexpression as follows:

GREAT = F3(A3,B3,F2(A2,B2,F1(A1,B1,F0(A0,B0))))

Where

F0(A0,B0) = A0*B0′

F1(A1,B1,F0) = (A1*B1′) + (A1*B1 + A1′*B1′)*F0

F2(A2,B2,F1) = (A2*B2′) + (A2*B2 + A2′*B2′)*F1

F3(A3,B3,F2) = (A3*B3′) + (A3*B3 + A3′*B3′)*F2

The expressions of F1, F2, and F3 perform the same function with the different input signals. Thus, the performance of

the 4bit greater-than-flag function required only two circuits. One circuit is to perform F0 and the other is to perform F1, F2, and F3 functions. F0 is a two-input-CMOS-FSCL-AND gate as shown in Figure 12. The CMOS FSCL circuit for F1, F2, and F3 is shown in Figure 21A. The CMOS FSCL 4bit greater-than-flag is constructed by cascading the circuits in Figure 12 and Figure 21A together as shown in Figure 21B.

4.2.3. CMOS FSCL Less-Than-Flag Circuit

The CMOS FSCL less-than-flag circuit is shown in figure 21. The Boolean expression of the 4bit less-than-flag function is derived directly from its truth table, Table I, as shown below:

LESS = (A3'*B3) + (A3*B3 + A3'*B3')*[(A2'*B2) + (A2*B2 + A2'*B2')*[(A1*B1') + (A1*B1 + A1'*B1')*(A0'*B0)]]

The design procedure is the same as the greater-than-flag circuit. Again, the expression is divided into subexpression as follows:

LESS = F7(A3,B3,F6(A2,B2,F5(A1,B1,F4(A0,B0))))

Where

F4(A0,B0) = A0'*B0

F5(A1,B1,F0) = (A1'*B1) + (A1*B1 + A1'*B1')*F4

F6(A2,B2,F1) = (A2'*B2) + (A2*B2 + A2'*B2')*F5

F7(A3,B3,F2) = (A3'*B3) + (A3*B3 + A3'*B3')*F6

The CMOS FSCL circuit for F4 function is shown in Figure 12

and F5, F6, and F7 functions in Figure 22A. By cascading the these circuits together, the less-than-flag is constructed (Figure 22B).

4.3. CMOS FSCL Output Buffer Circuit

CMOS FSCL circuit provides differential output. By taking advantage of this, a one-stage-differential-input-comparator is used to make the output voltage logic level compatible with conventional CMOS circuit. This will convert the CMOS FSCL output voltage logic low of 2.85 Volt to 0 Volt and logic high of 3.85 Volt to 5 Volt. A series of conventional CMOS inverters are used to drive the capacitance load as show in Figure 23.

4.4. CMOS FSCL Input Buffer Circuit

The CMOS FSCL inverter is used as an input buffer with one input source biased with 2.5 Volt as shown in Figure 24. This will convert input voltage of 5 volts to 3.85 volts and 0 volt to 2.85 volts. The CMOS FSCL inverter works perfectly as the input buffer since CMOS FSCL inverter provides a differential output.

4.5. CMOS FSCL Performance

The overall picture of the chip is shown in Figure 25. The CMOS FSCL simple CPU has been designed and

fabricated through MOSIS. All the design parameters are listed in Table II. The characteristics of this CMOS FSCL simple CPU are listed in Table III. The frequency of operation is about 60 MEGAHERTZ and less than one milliampere of current spike is generated.

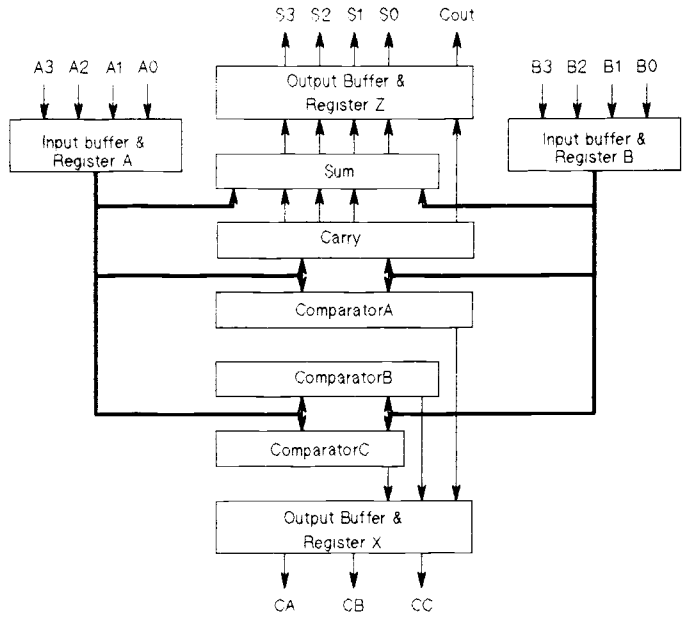

Figure 18 A block diagram of a simple CPU chip

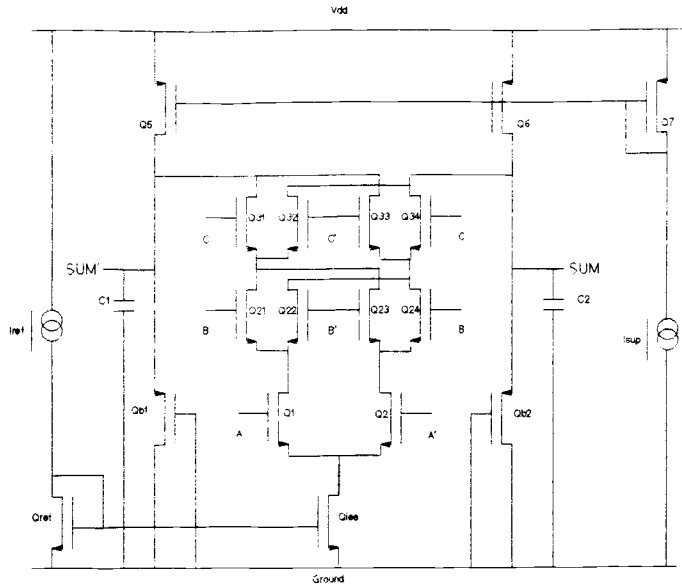

Figure 19A 1bit CMOS FSCL SUM circuit

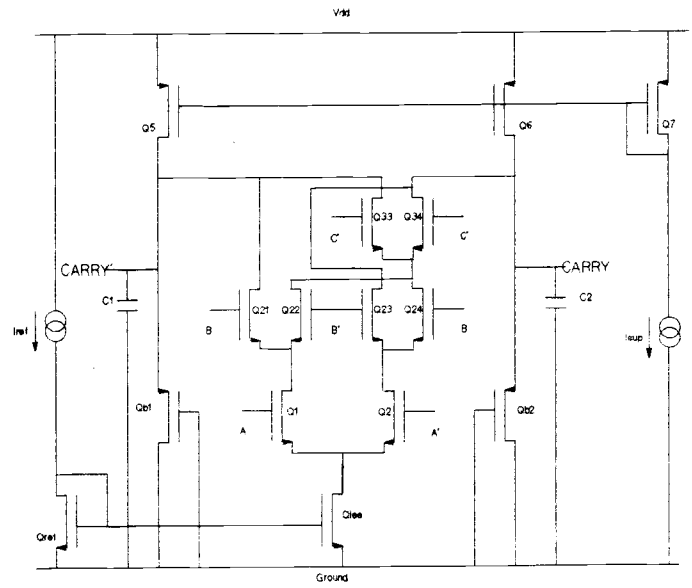

Figure 19B 1bit CMOS FSCL CARRY circuit

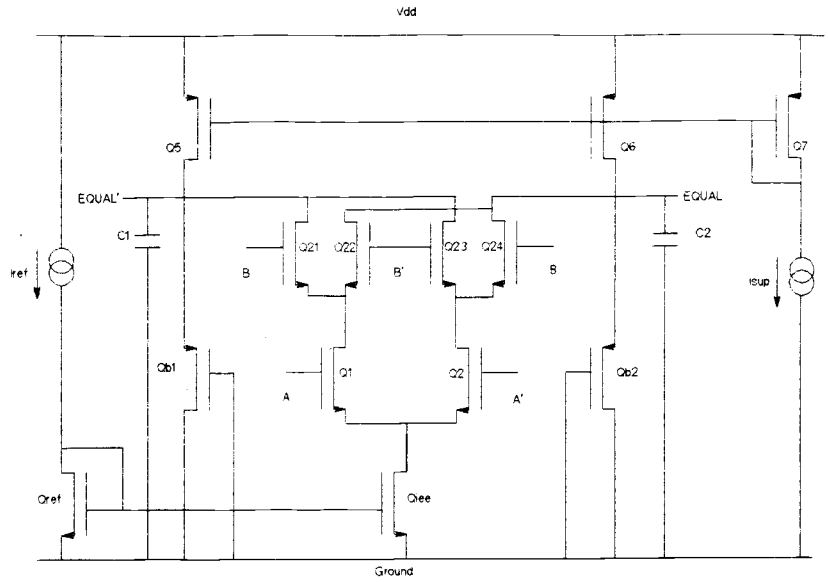

Figure 20A 1bit CMOS FSCL EQUAL-FLAG circuit

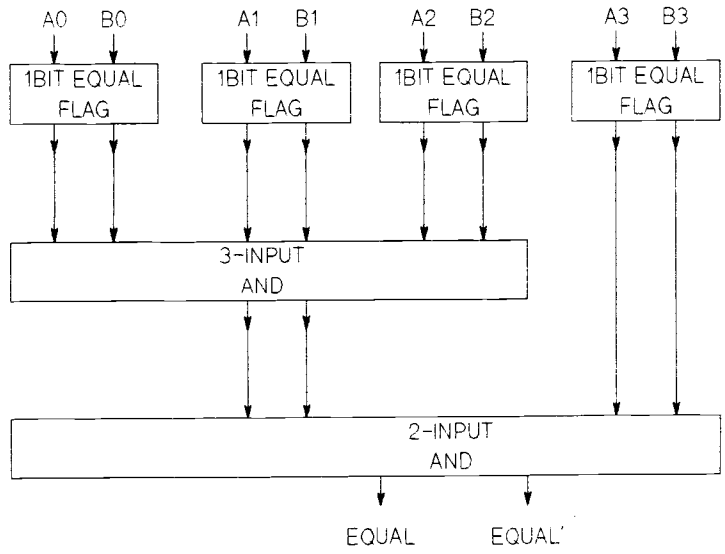

Figure 20B 4bit CMOS FSCL EQUAL-FLAG circuit

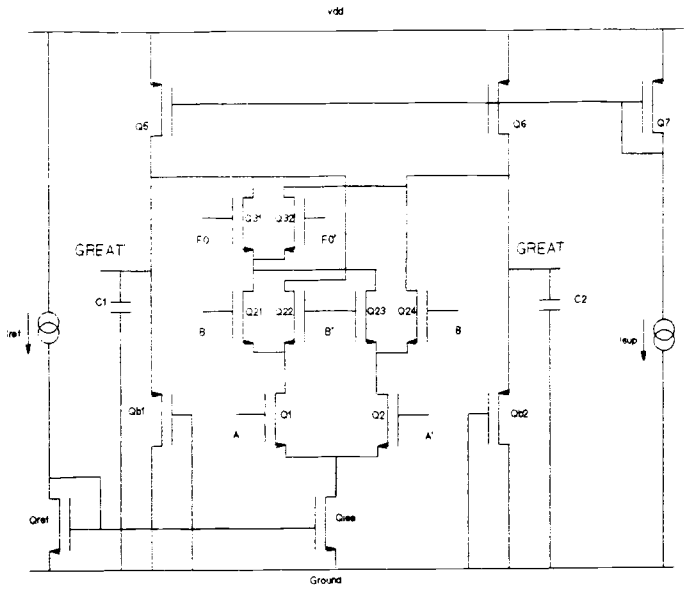

Figure 21A 1bit CMOS FSCL GREATER-THAN-FLAG circuit

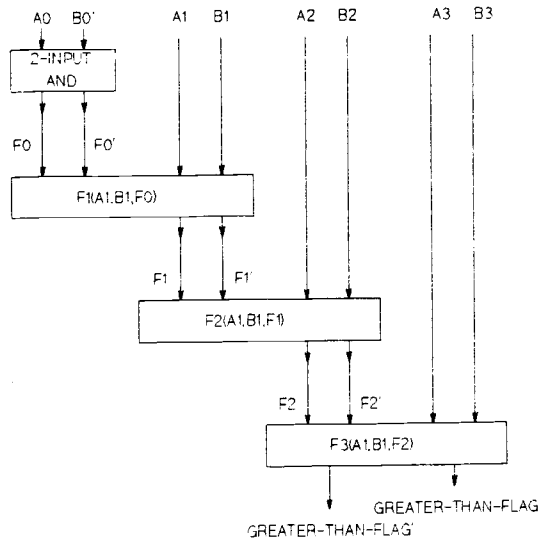

Figure 21B 4bit CMOS FSCL GREATER-THAN-FLAG circuit

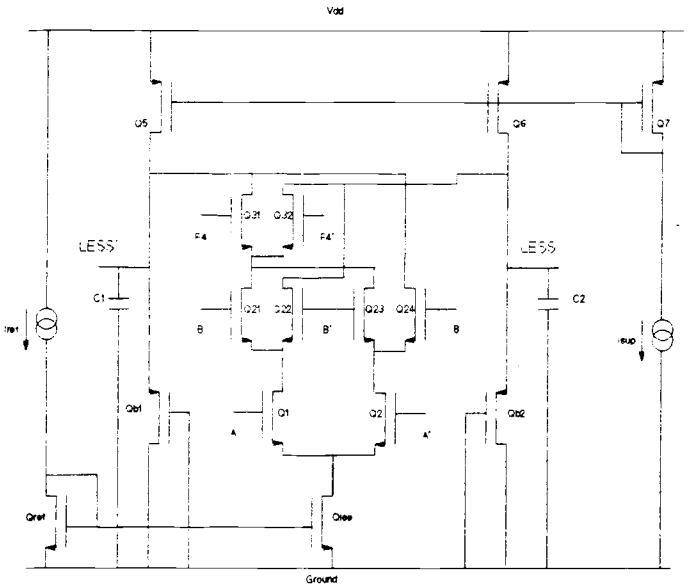

Figure 22A 1bit CMOS FSCL LESS-THAN-FLAG circuit

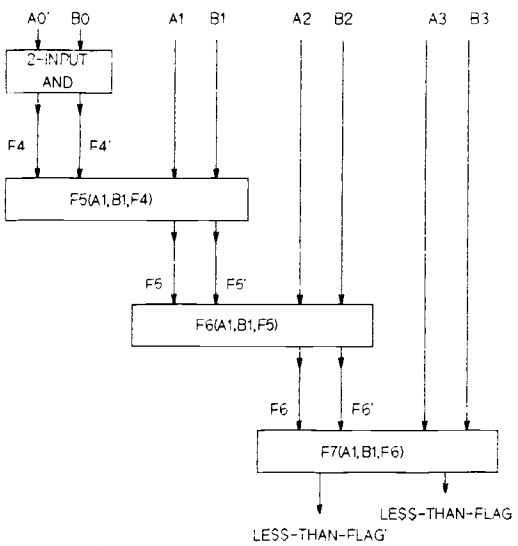

Figure 22B 4bit CMOS FSCL LESS-THAN-FLAG circuit

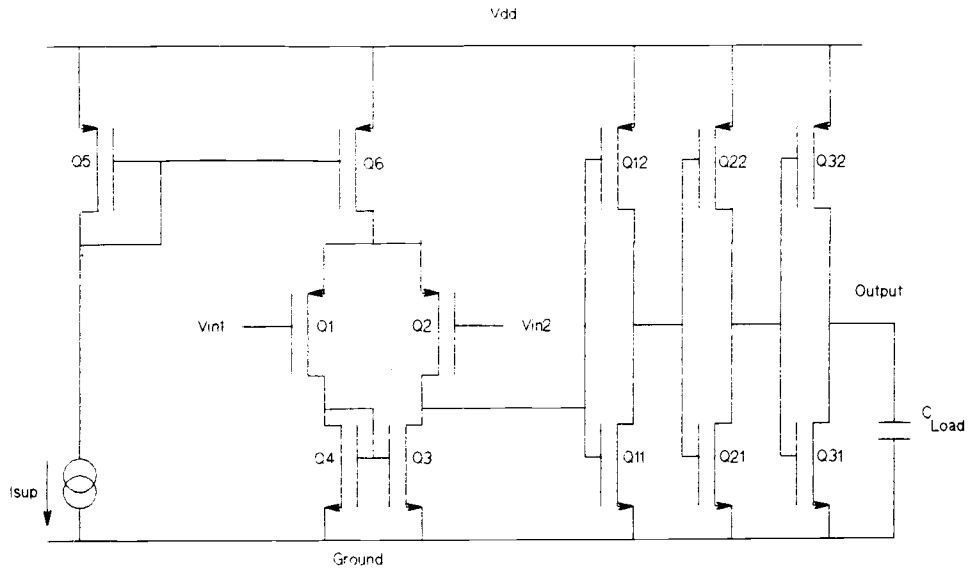

Figure 23 The CMOS FSCL output buffer circuit

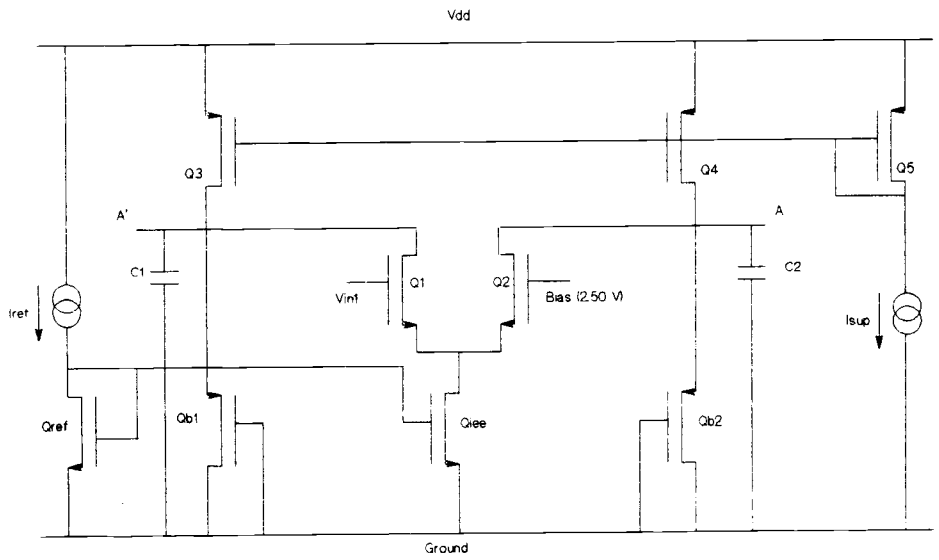

Figure 24 The CMOS FSCL input buffer circuit

Table I. The truth table for 4bit comparator.

Inputs				Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A=B	A>B	A<B
A3>B3	X	X	X	L	H	L
A3<B3	X	X	X	L	L	H
A3=B3	A2>B2	X	X	L	H	L
A3=B3	A2<B2	X	X	L	L	H
A3=B3	A2=B2	A1>B1	X	L	H	L
A3=B3	A2=B2	A1<B1	X	L	L	H
A3=B3	A2=B2	A1=B1	A0>B0	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L

Table II. The CMOS FSCL circuit devices size

NMOS differential pairs (W/L)	(15μm)/(2μm)
Bias current (Iee)	120 μA
Supply current (Isup)	200 μA
Qb1 and Qb2 (W/L)	(8μm)/(2μm)
Q5 and Q6 (W/L)	(20μm)/(2μm)
Qiee and Qee	(11μm)/(2μm)

Table III. The characteristics of CMOS FSCL simple CPU

Number of transistors	858
Frequency of operation	60 MHz
Power dissipation	110 mWatts
Current spike noise	70 μA

5. CONCLUSION

The current spike of the conventional CMOS circuit is a major problem in the mixed-mode integrated circuit. In this project, a CMOS FSCL family has been designed to overcome the problem. All the data of this thesis are produced from MSPICE simulation. A reduction of two orders of magnitude of current spike generated by CMOS FSCL circuit compared with the conventional CMOS circuit has been accomplished. A simple CPU is simulated, fabricated, and will be tested. This simple CPU comprised of about 800 transistors and less than 1 mA of current spike generated. This simple CPU operates at about 60 MHz and can be further improved.

The unique design of the CMOS FSCL circuit offers many attractive advantages. Among them are-

* negligible amount of current spike noise
* high performance
* high integration
* flexibility in the design of complex functions
* power consumption is compatible to the conventional CMOS circuit.

The CMOS FSCL circuit is the first of its kind ever invented. It opens up many possible directions for future work. Two-stages-comparator can be used to drive the off chip load capacitance (Figure 26). By increasing the differential input voltage, the fanin limitation can be

eliminated. The CMOS FSCL circuit operates at a small differential input voltage. Thus, the supply voltage can be reduced which in turn will reduce the power dissipation.

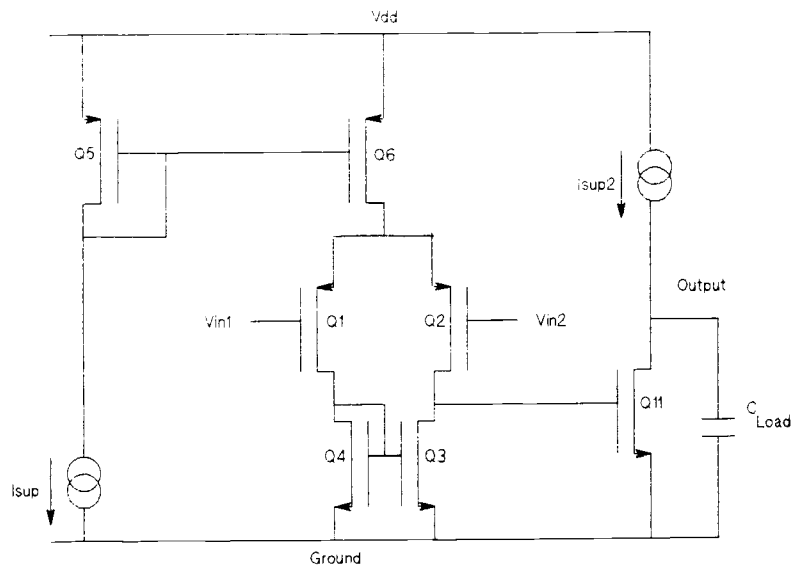

Figure 25 The two-stages-comparator output buffer

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APPENDIX

7. APPENDIX A Circuit Layouts

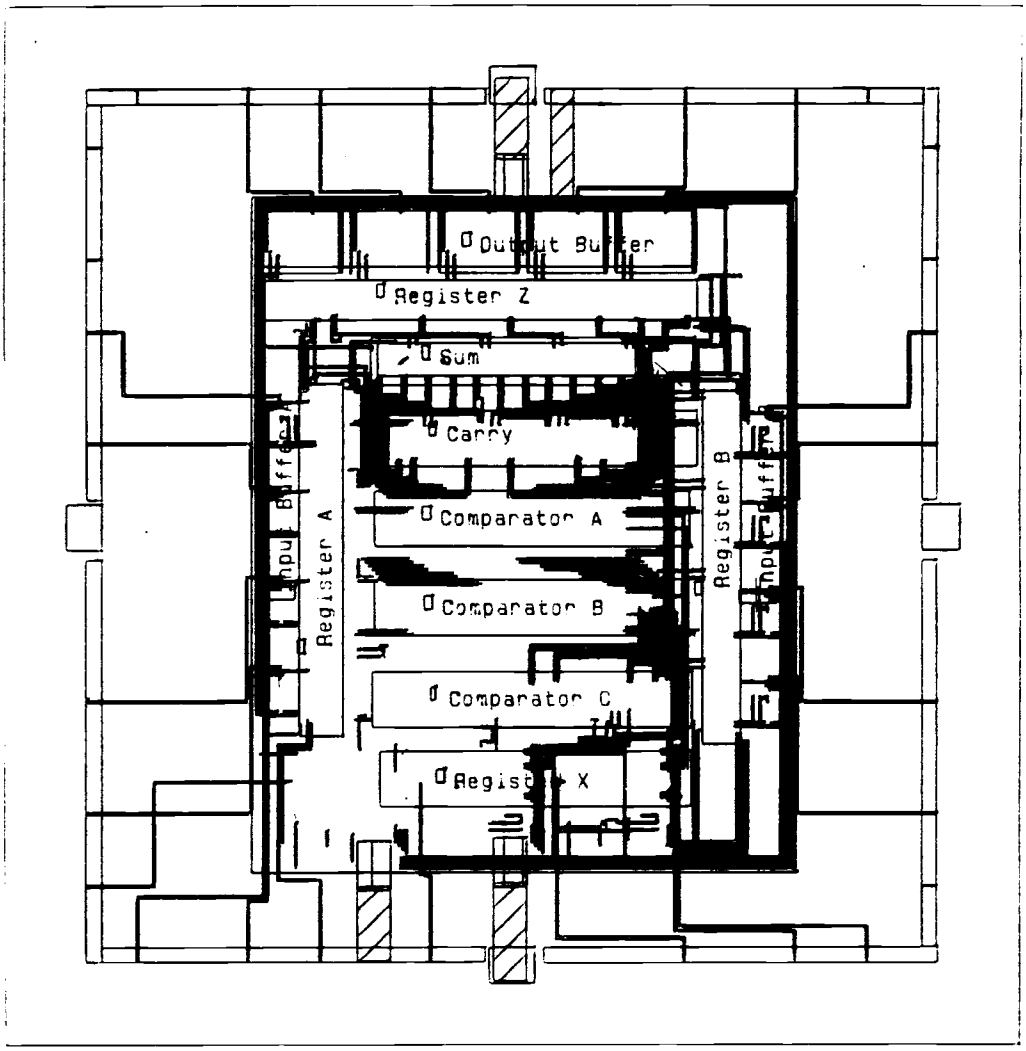

Figure 26 The CMOS FSCL simple CPU chip