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The transition from second-generation (2G) to third-generation (3G) wireless cellular and cordless telephone systems requires multi-standard adaptability in a single RF receiver equipment. An important answer to this request is the use of Delta-Sigma modulators for IF-to-baseband conversion, which will satisfy the dynamic range requirements for digital signal processing, and at the same time, add adaptability and programmability to the characteristics of a RF receiver.

This thesis addresses the issues of designing a Delta-Sigma modulator for a multi-standard wireless receiver. A single-loop third-order modulator topology suitable for low power and high integration multi-standard receiver design is proposed. The trade-offs in the modulator design are also presented and explained. The modulator, which has been implemented as a part of a monolithic receiver chip, will be fabricated in a standard 0.35-μm CMOS process. The post-layout simulation results have verified the outcomes of system analysis.

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The Design of Delta-Sigma Modulators for Multi-Standard RF Receivers

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CHAPTER 1. INTRODUCTION

1.1. Motivation

Over the past few years, the tremendous growth in the mobile communications industry has dramatically increased the number of subscribers to second-generation (2G) digital cellular and cordless telephony systems (e.g., GSM, IS-95/54, DECT, and DPRS), which were created to address the need for increased system capacity over first-generation analog systems (e.g., AMPS). At the same time, the enormous demand for voice, data, short-messaging and mobile video services has led to the evolution of the wireless infrastructure to support third-generation (3G) standards (e.g., EDGE, WCDMA, CDMA-2000, IMT and UMTS) and services. Figure 1.1 shows the wireless technology trend from 1G to 3G.

However, a complete transition from 2G to 3G in a short period of time is not yet feasible, considering the vast volume of existing 2G services and the time, infrastructure, and capital expense needed to achieve competent quality and popularity for a ubiquitous 3G wireless system. In order to take advantage of both 2G and 3G standards and services during this transition period, quite a few research efforts have been made to create wireless transceivers that can provide multi-band and multi-standard performance capabilities [1] [2] [3] [4] [5] [6].

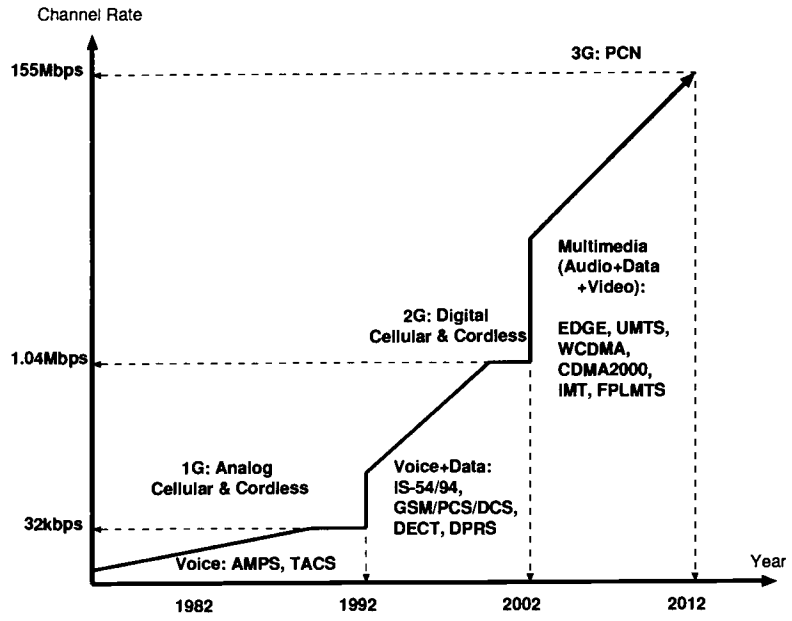

Figure 1.1: The trend of wireless technologies and standards.

Accommodating multiple standards in one RF transceiver intuitively means additional complexity in both the RF and the baseband parts, which results in low integration and high power consumption. On the other hand, it is well known that area and power dissipation of digital circuits reduce as the fabrication process shrinks; Furthermore, the continuously downscaling of CMOS technologies has allowed for more aggressive digital signal processing at a lower price. To take advantage of this in the wireless transceiver design, efforts are needed to convert the incoming analog signals into digital as close as possible to the antenna [3], which implies that most of the RF/IF (intermediate-frequency) and the entire baseband signal processing will be done in the digital domain. In addition, digital filters can provide the adaptability needed to support multi-standard radio transceivers. However, the transition from single-standard to multi-standard is not at all trivial. It requires a complete reconsideration of the RF front-end design. The tradeoffs among performance, complexity,

and expense make the design of a successful multi-standard receiver very challenging.

One notable challenge lies in the design of low-power, high dynamic range analog-to-digital converters, which digitize the small signal in the presence of strong blockers and interferers. Since the neighboring blockers have not been satisfactorily attenuated by filtering (i.e., the bulky high-Q SAW filters in conventional transceivers are replaced by low-cost low-Q analog anti-aliasing filters), and as a result, the desired small signal is submerged by them and won't be detected unless the ADC has high input dynamic range. Delta-Sigma modulator is one of the best solutions for this data acquisition interface because the quantization noise is shaped out-of-band with a high-pass characteristic, and the decimation filtering can be combined with selective digital filtering and IF mixing in order to attenuate both the quantization noise and neighboring blockers. Moreover, by choosing different sampling rates (i.e., different oversampling ratios), the same Delta-Sigma modulator architecture can adapt to the different signal bandwidth, dynamic range, signal-to-noise-ratio (SNR) and intermodulation requirements imposed by multiple RF standards [7]. Finally, compared to the Nyquist-rate data converters, oversampled Delta-Sigma data converters have demonstrated lower sensitivity to the analog component imperfections, thanks to a higher sampling rate and more complex digital signal processing. The desire to design Delta-Sigma modulators for low-power and high-integration multi-standard RF receivers has motivated the research work described in this thesis.

1.2. Research Goal

The goal of this research project is to design a single-path, third-order Delta-Sigma modulator with a single-bit quantizer for a multi-standard RF receiver in

standard 0.35-μm CMOS technology. Table 1.1 summarizes the post-layout simulated performance of the proposed modulator.

Table 1.1: Summary of the modulator's performance.

Standards	GSM/WCDMA/DECT
Receiver architecture	Single-IF Super-Heterodyne
Sampling scheme	IF-band sampling
OSR values	192(GSM), 24(WCDMA) and 64(DECT)
Dynamic range	90 dB(GSM), 70 dB(WCDMA) and 76 dB(DECT)
SNDR	80 dB(GSM), 55 dB(WCDMA) and 65 dB(DECT)
SNR	83 dB(GSM), 57 dB(WCDMA) and 67 dB(DECT)
IP3	-28 dBV$_{rms}(GSM)$, $-19.4 dBV_{rms}(WCDMA)$ and -17 dBV$_{rms}(DECT)$
Total capacitance	6.24 pF
Capacitance spread ratio	24:1
Power consumption	$\leq 14mW(GSM)$, $\leq 15mW(WCDMA)$ and $\leq 20mW(DECT)$
Reference voltage	1.25 V
Supply voltage	2.5 V
Process	0.35-μm CMOS

In particular, the oversampled modulator is designed to meet the requirements for the following standards: Global System for Mobile communications (GSM), Wideband Code-Division Multiple Access (WCDMA), and Digital Enhanced Cordless Telecommunications (DECT). The modulator is to be implemented in amulti-standard receiver employing the Single-IF Super-Heterodyne (or Digital High IF) architecture [8].

1.3. Thesis Outline

Following this chapter, Chapter 2 provides an overview of various receiver architectures, along with a brief description of IF sampling by using lowpass Delta-Sigma modulators. Chapter 3 presents the fundamentals of oversampled Delta-Sigma modulators. Analytical and theoretical explanations of different loop filter topologies are also presented in this chapter. Chapter 4 covers the system-level design of the proposed third-order Delta-Sigma modulator, followed by its simulated performance. The nonidealities in the modulator design are explored in this chapter. The circuit implementation of individual building blocks is explained in Chapter 5. Chapter 6 presents the results of circuit-level implementation. Chapter 7 summarizes the research work and provides a few suggestions for future work.

CHAPTER 2. RECEIVER SYSTEMS

2.1. Introduction

This chapter starts with explaining the key figures of merit that are usually used in evaluating the performance of a RF receiver system. Then it will provide an overview of various receiver architectures. It is followed by a brief description of IF sampling/digitizing by using a pair of lowpass Delta-Sigma modulators. This chapter concludes with a brief explanation of how the modulator specifications are determined.

2.2. Figures of Merit

The key figures of merit in wireless receivers design include sensitivity, selectivity, linearity and dynamic range. Sensitivity is defined as the lowest available signal power that a RF receiver can detect in the presence of electronic noise, while providing an adequate signal-to-noise ratio (SNR) at the receiver output for demodulation [9]. It is often determined by the quality factors of the RF front-end components. System-level simulations are usually used in the evaluation of the minimum bit error rate (BER) in order to define the minimum SNR necessary for the satisfactory reproduction of the desired signal. Another popular measure of sensitivity is the minimum detectable signal (MDS) [10].

Selectivity is a measure of the receiver's ability to extract a weak desired signal in the presence of strong adjacent interferers and channel blockers. Usually the performance of the IF channel select filters sets the selectivity of the entire receiver [9] [10].

Linearity defines the receiver's ability to suppress the inter-modulation products, and to process a signal in the presence of an acceptable distortion level. The third-order intercept point (IP3) can be specified from the results of a two-tone test measurement and is usually used to express the degree of linearity. The 1-dB compression point, at which the power gain is 1-dB down from the ideal point, is an alternative to IIP3. The dynamic range defines the receiver's ability to detect a weak signal above the noise floor and process a large signal without severe distortion. The lower limit set by the dynamic range requirement is somewhat equivalent to what defines the sensitivity performance. And the upper limit set by the dynamic range requirements is largely dependent upon the choice of architecture. The spurious free dynamic range and the blocking dynamic range (BDR) are the two mostly seen figures of merit in measuring the receiver's dynamic range [9].

2.3. Receiver Topologies

2.3.1. Conventional Super-Heterodyne Receiver

The conventional Super-Heterodyne receiver shown in Figure 2.1 has been a widely used topology in wireless design since its invention in 1917. It can attain excellent selectivity and sensitivity performance by proper choice of IF frequency and filters. It is not prone to the dc offset and LO leakage problems because it employs the two-step down-conversion scheme. In addition, when a high IF is chosen, the requirements of the image-rejection (IR) filter can be relaxed. However, the Super-Heterodyne architecture uses external image-rejection (IR) and IF filters, which bring about a big disadvantage when it comes to the adaptation to an integrated solution

[1].

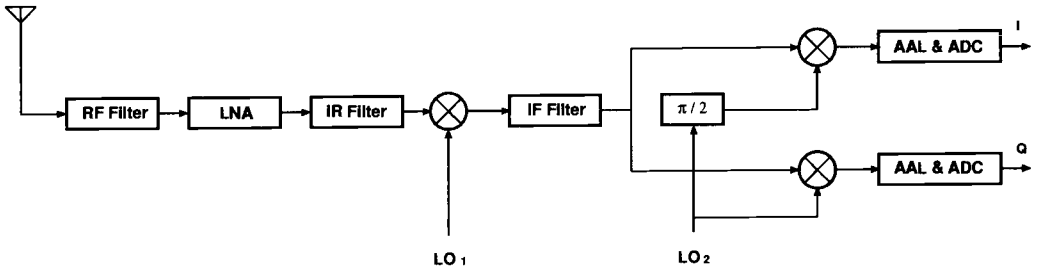

Figure 2.1: The conventional Super-Heterodyne architecture.

2.3.2. Zero-IF(Homodyne) Receiver

Figure 2.2 shows the Zero-IF (Homodyne, or Direct-conversion) receiver. It has been the result of eliminating the external IR and IF filters from the heterodyne receiver for the purpose of improving integration [11]. In this topology, the entire RF signal spectrum is directly down-converted to baseband. The Direct-conversion topology no longer suffers from severe image interferences, but a time-varying dc offset is introduced at the mixer output due to the self-mixing of the original and leaked LO signals. Moreover, because this topology employs one-step frequency transition and the channel selection is done mainly by a digital lowpass filter (LPF), a high-frequency, low-noise frequency synthesizer is needed to provide variable LO frequencies for channel selection, which is not easy to implement with the on-chip low-Q components. Finally, the dynamic range requirement of the baseband ADC is non-trivial since its input has not experienced much selective filtering.

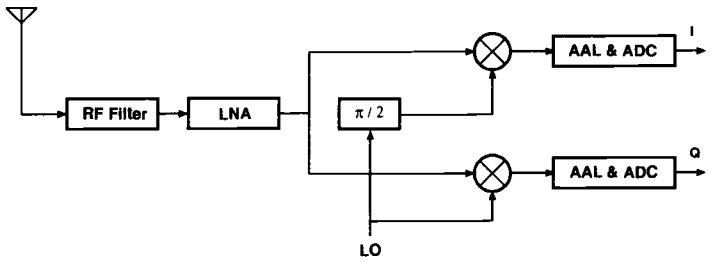

Figure 2.2: The Zero-IF (Homodyne) architecture.

2.3.3. Low-IF Single-Conversion Receiver

The concept of on-chip bandpass filtering has led to the Low-IF Single-conversion receiver topology, which is shown in Figure 2.3. In this topology, the IF is chosen at a low frequency (typically hundreds of kHz) instead of dc. Thus, it alleviates most of the dc offset and low-frequency noise (e.g., flicker noise) problems, which appear in Zero-IF receivers. However, due to its one-step down-conversion characteristic, the Low-IF topology still suffers from the same design constraints that occur in the Zero-IF topology: a high-frequency synthesizer providing variable LO frequencies, and a high dynamic-range baseband ADC. Moreover, the ADC has to be of wide-bandwidth (0 to 2 MHz), because the desired signal is usually more than two channels away from dc. Finally, a high-Q bandpass filter is needed to suppress the strong blockers folded in close to the desired signal.

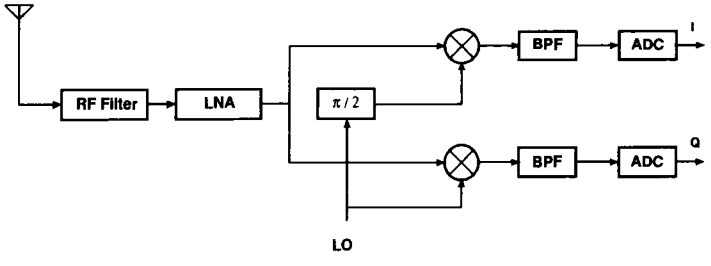

Figure 2.3: The Low-IF single-conversion architecture.

2.3.4. Wideband IF Double-Conversion (WIFDC) Receiver

The Wideband IF Double-conversion receiver shown in Figure 2.4 employs a two-step down-conversion as in the conventional Super-Heterodyne topology. The major difference between WIFDC and Super-Heterodyne receivers is that the second LO frequency (instead of the first LO frequency as in the conventional Super-Heterodyne topology) is made programmable to select the desired channel band. Compared to the Zero-IF topology, WIFDC mitigates the dc offset errors due to the LO self-mixing. Compared to the Low-IF topology, it avoids the RF frequency-synthesizer because only low-frequency (on the kHz level) variable LO's need to be generated, and it also removes the need for a high-Q bandpass filter [4]. However, in essence WIFDC carries out baseband sampling and channel selections, which implies adjacent channel blockers will cause severe dc offsets. As a result, a high dynamic-range ADC and a good anti-alias filter (AAL) are still needed. Finally, as shown in Figure 2.4, the elimination of the bandpass filter is achieved by adding more mixers at the second down-conversion stage, which cause extra problems in terms of power and LO mismatching.

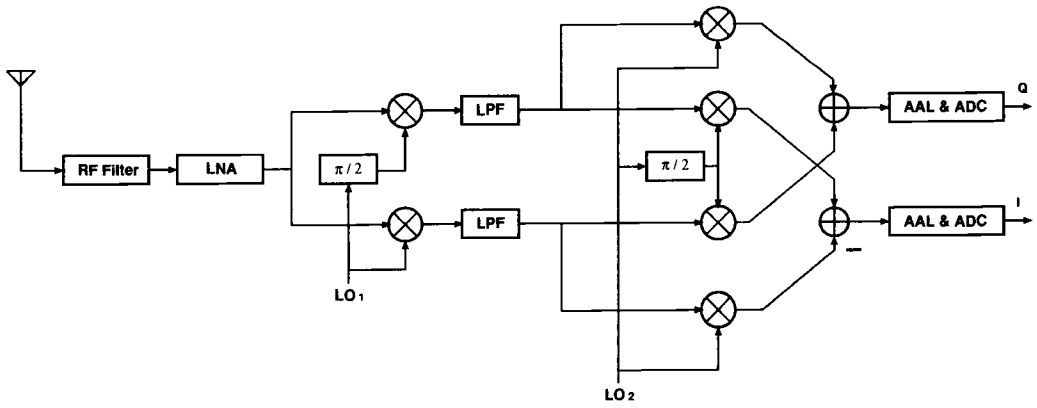

Figure 2.4: The Wideband IF double-conversion architecture.

2.3.5. Digital IF Receiver

With the emergence of more advanced complementary metal-oxide semiconductor (CMOS) process in terms of size, speed and power dissipation, the IF-to-baseband conversion and filtering can be pushed into the digital domain. This transition from analog to digital will add more flexibility and programmability to the characteristics of wireless receivers. The digitization of the IF stage has been implemented in Super-Heterodyne with a high IF (i.e., about 100-MHz) [12] [13] [14], Low-IF [15] [16] and Zero-IF [5] [6] architectures.

As mentioned in the previous sections, Delta-Sigma modulator is chosen because of its inherent programmability, which is essential for the realization of a multi-standard RF receiver. Also, its ability of performing sampling and filtering operations simultaneously makes it extremely attractive for the same purpose.

Both lowpass and bandpass modulators have been reported to fulfill the task. Their design methodologies are somewhat analogous to one another. Bandpass modulators are inherently immune to low-frequency flicker noise. In addition, because quadrature mixing is done digitally after the bandpass modulation, I/Q mismatching caused by analog component imperfections is avoided. Nevertheless, bandpass modulators are usually clocked at a sampling rate twice as that of lowpass modulators, which implies a difference in power dissipation and often leads to the use of continuous-time method in bandpass design to avoid Sample-and-Hold errors [17].

In this thesis, a Super-Heterodyne receiver with a digitized high-IF (around 100-MHz) is chosen because it is the most widely seen topology in the existing mature second-generation (2G) cellular and cordless product lines. Figure 2.5 shows a digital high-IF topology using lowpass modulators for IF sampling. The IF-to-baseband

section is split into two paths, which leads to a clock rate that is half the effective sampling rate. The advantages of this architecture over others were explained in [14] and [18], where Delta-Sigma modulators were designed for a dual-standard (GSM/WCDMA) RF receiver. One important advantage is that a high-IF digitizing has relaxed the requirements of image rejections, since the IF frequency is at least 10 times higher than the desired signal bandwidth. Lowpass Delta-Sigma modulators are chosen over the bandpass modulator to perform IF sampling and digitizing for the sake of lower sampling rates and hence power saving. In addition, a pair of lowpass modulators can achieve a channel bandwidth of 4 MHz when the IF sampling scheme is employed. A lowpass modulator employing a topology different from that in [14] will be designed and implemented for a multi-standard (GSM/WCDMA/DECT) receiver. Oversampling ratios such as 192 (GSM), 24 (WCDMA) and 64 (DECT) have been chosen. Details on the lowpass modulator design will be explained in Chapter 4.

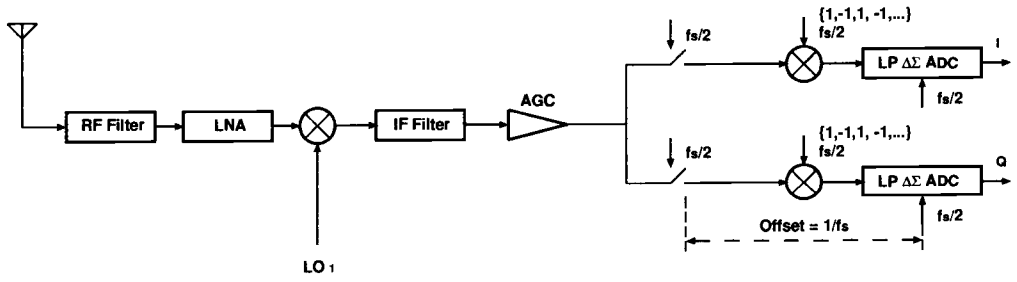

Figure 2.5: The Digital High IF architecture.

2.4. IF Sampling

2.4.1. Analog vs. Digital Channel Selection

In order to avoid separate front-end paths in a multi-standard RF receiver, a programmable channel-select filter shared by different wireless standards is often used. The channel selection can be done either in the analog domain or in the digital domain.

Analog CMOS channel-select filters implemented in G_m-C [19] [20] and switched-capacitor (SC) [21] techniques have been reported recently. G_m-C channel-select filters usually suffer low dynamic range, especially when the power-supply voltage is decreased to below 3-V level. In contrast, SC filters provides relatively good dynamic range performance. However, in a RF environment, a SC filter needs wideband and linear op amps in order to run at a high sampling rate, which results in a large current budget and hence high power consumption. Moreover, a high resolution and high dynamic-range ADC seems not necessary here since the preceding SC filter has already provided sufficient automatic gain control for various channels, which in turn relaxed the frequency tuning and dynamic range requirements of the subsequent stages. Therefore, Delta-Sigma modulators that aim at both resolution and dynamic range are not suitable for analog channel selection.

Alternatively, digital channel selection is carried out, usually by using a digital FIR filter after the ADC [3]. One noticeable advantage of digital channel-select filter over the analog one is the programmability and accuracy that it provides. Another benefit comes from the removal of a high-Q SC filter at high frequencies. Nevertheless, a high resolution and high dynamic range ADC is needed because the incoming signal does not experience much prefiltering, especially in topologies like Zero-IF, Low-IF, WIFDC and Digital High-IF, where the requirements on external RF filters have been relaxed. As a result, Delta-Sigma modulator becomes the most suitable solution to multi-standard receivers employing the above topologies.

2.4.2. IF Sampling by Delta-Sigma Modulators

Figure 2.6 illustrates the noise transfer functions (NTF) for GSM and WCDMA when IF sampling scheme is employed. Instead of using a single sixth-order bandpass Delta-Sigma modulator with a high center frequency (i.e., a high f_{IF}), a pair of parallel third-order lowpass modulator offset by $\pi/2$ phase shift are used to acquire the same magnitude response. Compared to the bandpass modulator, the lowpass modulators ease the circuit design by lowering the modulator order and by reducing the bandwidth requirement. Moreover, the stability of a third-order modulator is easier to control than that of a sixth-order one.

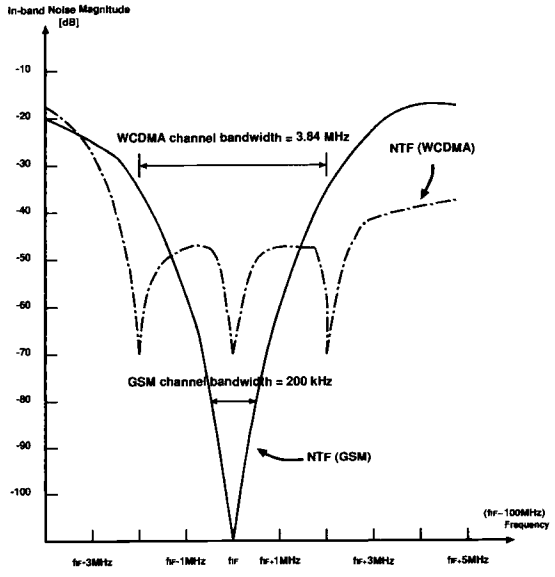

Figure 2.6: IF Sampling: NTFs for GSM and WCDMA.

2.5. Modualtor Specifications

The specifications of Delta-Sigma modulator are derived based on noise, in-

termodulation and blocking performance requirements of the multi-standard receiver. Table 2.1 summarizes the radio specifications of the multi-standard wireless receiver [23] [24] [25].

Table 2.1: Radio specifications of the multi-standard receiver.

Standards	GSM	WCDMA	DECT
Modulation scheme	GMSK	QPSK/RRC	GFSK/DBFSK
Access scheme	TDMA FDMA	CDMA B-CDMA	TDMA FDMA
RX Band(MHz)	935-960 1850-1910	1920-1980 2110-2170	1880-1900 1910-1930
Signal bandwidth(MHz)	0.2	3.84	1.40
Channel rate(Mbps)	0.271	3.84	1.152
Channel spacing(MHz)	0.2	5	1.728
Sensitivity(dBm) @ BER=0.001	-100	-110	-83
Desired Signal level (dBm)	-99	-108	-80
Interferer level(dBm)	-49	-46	-46
Max. In-band blocker level (dBm)	-23	-44	-33
Overall NF(dB)	12	9	18
Frontend NF(dB)	8	5	14
Baseband NF(dB) (input-referred)	4	4	4
IP3(dBV_{rms})	-25	-18	-16

Both interfering and blocking signal levels must be taken into accounts in order to derive the required dynamic range of the modulator. The bottom line is that the residual dynamic range [14] has to be covered by the overall dynamic range of the modulator. As for the signal-to-noise ratio (SNR), the modulator's noise floor should be constrainted to at least 10 dB below the noise floor of the frontend chain (i.e., from RF filter's output to modulator's input), so that its contribution to the overall noise figure (NF) is considered trivial. The derivation of the required IP3 is not easy because

a reasonable estimation is not possible until all of the following figures are measured: the frontend chain gain, the attenuation of the interferers and in-band blockers by the IF filter, the intermodulation performance (IP3) of the mixers. Nevertheless, the results from most state-of-art design using Delta-Sigma modulators [7] [14] [18] [26] have shown that the modulator's contribution to the overall intermodulation figure can be considered negligible, only if the IF filter is able to provide a sufficient stopband attenuation (e.g., 36dB at 4 MHz cutoff band for WCDMA). Readers are referred to [6] for detailed system analysis. Table 2.2 summarizes the target specifications for the lowpass modulator [7] [14].

Table 2.2: Target Specifications of the Delta-Sigma modulator.

Standards	GSM	WCDMA	DECT
Dynamic range(dB)	86	54	72
SNDR(dB)	72	52	63
SNR(dB)	76	56	67
IP3(dBV_{rms})	-26	-18.2	-15

2.6. Summary

This chapter reviewed the key figures of merit in RF system design and analysis. It then investigated a wide of variety of receiver architectures and demonstrated the system design trade-offs that would lead to the selection of a particular topology. The idea IF sampling by using a pair of lowpass Delta-Sigma modulators was shown. It concluded by explaining how the modulator's specifications were derived.

CHAPTER 3. DELTA-SIGMA ($\Delta\Sigma$) MODULATORS

3.1. Introduction

This chapter will provide an overview of Delta-Sigma ($\Delta\Sigma$) modulators. It starts with a brief review of the noise-shaping concept. The motivation for using high-order single loops in this modulator design will be presented. Finally, several existing loop filter topologies for high-order single-bit $\Delta\Sigma$ modulators will be examined.

3.2. The Noise-Shaping Concept

Quantization of a continuous amplitude produces quantization errors in the time-domain. The correlation between quantization errors from sample to sample is largely broken if the input changes randomly by amounts much greater than the spacing of discrete levels. Statistically, the mean-square value of the quantization error can be used to represent the quantization noise level, whose spectral elements evenly fall into the entire sampling bandwidth according to the additive white-noise assumption [27]. Increasing the sampling rate to a level much higher than the Nyquist-rate can spread the noise power to a wide frequency range. The actual reduction of in-band power level is estimated by a factor of OSR (oversampling ratio).

In addition to the increased oversampling ratio, $\Delta\Sigma$ modulator takes advantage of negative feedback to reduce in-band quantization noise power. The linearized model of the first-order modulator shown in Figure 3.1 employs the additive white noise assumption, and the quantization error is assumed to be independent of the

busy input, uniformly distributed in $[-\Delta/2, \Delta/2]$ (Δ is the step size of the quantizer). Thus, the quantization noise, q can be represented as an additional input to the system.

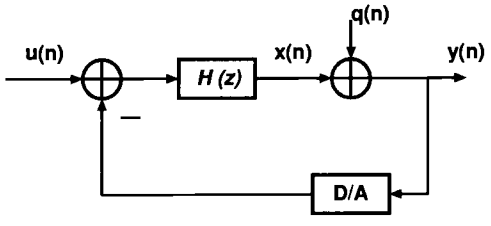

Figure 3.1: The linearized model of a first-order modulator.

Based on the linearized model, z-domain analysis is employed to explore the noise-shaping concept. The output of the modulator Y(z) can be expressed as:

$$Y(z) = STF(z)U(z) + NTF(z)Q(z)$$

where STF(z) is the signal transfer function and NTF(z) is the noise transfer function. Solving the above equation for STF(z) and NTF(z), and expressing them in terms of H(z), one yields the following:

$$STF(z) = \frac{Y(z)}{U(z)}\Big|_{Q(z)\equiv 0} = \frac{H(z)}{1+H(z)}$$

$$NTF(z) = \frac{Y(z)}{E(z)}\Big|_{Q(z)\equiv 0} = \frac{1}{1+H(z)}$$

If H(z) is realized by a delayed non-inverting integrator, then

$$H(z) = \frac{1}{z-1}$$

$$STF(z) = \frac{H(z)}{1 + H(z)} = \frac{1}{z}$$

and

$$NTF(z) = 1 - \frac{1}{z}$$

The foregoing equation suggests that the quantization noise experienced a modulation of high-pass fashion. For this reason, most of the quantization noise power would be pushed to higher frequencies. Figure 3.2 illustrates the process of first-order noise shaping as an example.

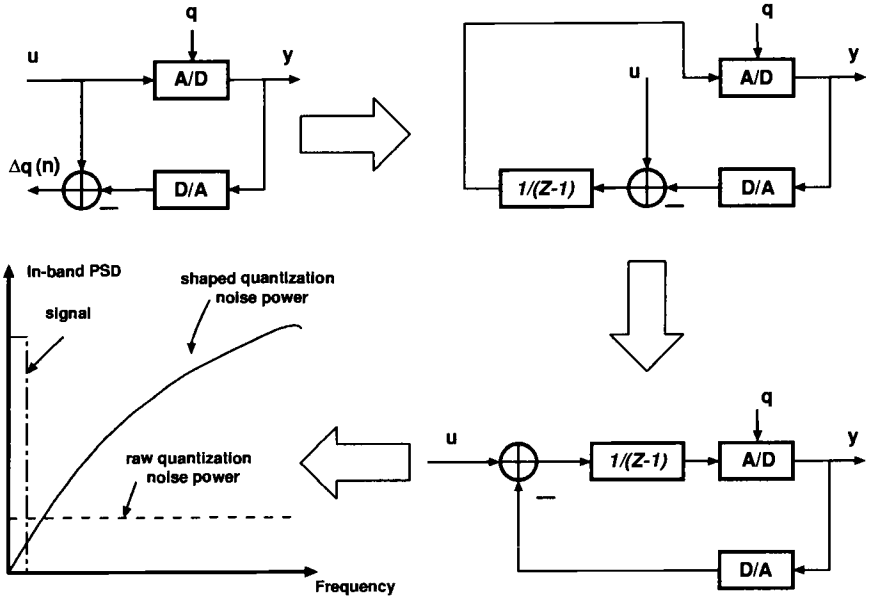

Figure 3.2: First-order noise-shaping.

3.3. Motivation for a High-Order Single-Bit Modulator

Delta-Sigma modulators can be roughly categorized into the following types: low-order (L≤2) single-bit single-loop, high-order single-bit single-loop, single-bit multiloop (cascaded or MASH), and multibit (single-loop or multiloop). Each topology has its own share of advantages and disadvantages. For example, a second-order single-bit single-loop modulator is robustly stable and easy to design, but it needs high oversampling ratio (e.g., 256 or more) in order to achieve a SNR of above 100 dB. Table 3.1 summarizes the advantages ($\surd$) and disadvantages ($\times$) of these modulator types.

Table 3.1: Comparisons of modulator types.

Modulator type	SNR vs. OSR ratio	Idle-tones/ Linearity	Circuit design simplicity	Stability issues	Decimation filter simplicity
Low-order 1-bit single-loop	$\times$	$\times$	$\surd$	$\surd$	$\surd$
High-order 1-bit single-loop	$\surd$	$\surd$	$\surd$	$\times$	$\surd$
Single-bit multiloop	$\surd$	$\times$	$\times$	$\surd$	$\times$
Multibit	$\surd$	$\times$	$\times$	$\surd$	$\times$

Power and area are the two biggest concerns in regard to a multi-standard receiver, which must be taken into account in the design of $\Delta\Sigma$ modulators. The SNR *vs.*OSR ratio shown in Table 3.1 defines the modulator's ability of achieving high SNR for modest OSR values, which also indicates its adaptability to low power design. Modulators with multibit quantizers are subject to dc non-linearity problems due to imperfect matching of multibit D/A levels, which lead to the need for auto-calibration or dynamic element matching techniques. The use of multibit quantizers

and DAC error correction increases the complexity of the circuitry and hence more chip area and power budget. Multiloop or cascaded modulators provide guaranteed stability performance by employing lower order coders in each stage. However, the complete cancellation of the quantization noise from the first loop is not achievable unless a perfect matching between analog interstage gain and its digital prediction. For a fourth-order cascaded (2-2) modulator like the one reported in [7], a relative interstage mismatch ratio of 0.02 will result in more than 25 dB increase in the in-band quantization noise power, even under the assumption of perfect integrators. If the finite op amp dc gain problem is taken into account, the resulting leaky integrators will further degrade the SNR performance of the modulator. Finally, both multibit and cascaded topologies impose additional pressure on the decimation filter since it must allow for multibit streams at it input, which increases the complexity of circuit design.

Thus, a high-order single-bit single-loop $\Delta\Sigma$ modulator is chosen because of its advantages shown in Table 3.1. However, a high-order single-bit single-loop modulator doesn't unconditionally aquire a guaranteed stability performance. In fact, the STF and NTF responses should be analyzed carefully to ensure that certain stability criteria be satisfied [28]. Fortunately, as will be explained in Chapter 4, a third-order, instead of a fifth or sixth-order single-bit modulator, is needed in this thesis in light of the selected digital high-IF receiver architecture and IF sampling. The effort to maintain stability is therefore greatly eased. The next section will examine the existing loop filter topologies.

3.4. Loop Filter Topologies

There are various architectures for realizing the loop filter in a $\Delta\Sigma$ modulator. Most of the existing single-bit single-loop topologies, especially those suitable for switched-capacitor (SC) implementations, are listed as follows (Note that all the integrators mentioned in this thesis are delayed non-inverting SC integrators):

1. Cascade-of-Integrators with weighted quantizer inputs:

In this topology, the NTF will have all its zeros at dc (z=1), which usually results in a Butterworth highpass NTF response. Analog weighted summation circuit is needed in front of the quantizer, which implies an op amp in real circuit and hence additional analog circuit noise. Note that H(z) is equal to $1/(z\text{-}1)$ in this thesis. Figure 3.3 illustrates a third-order example.

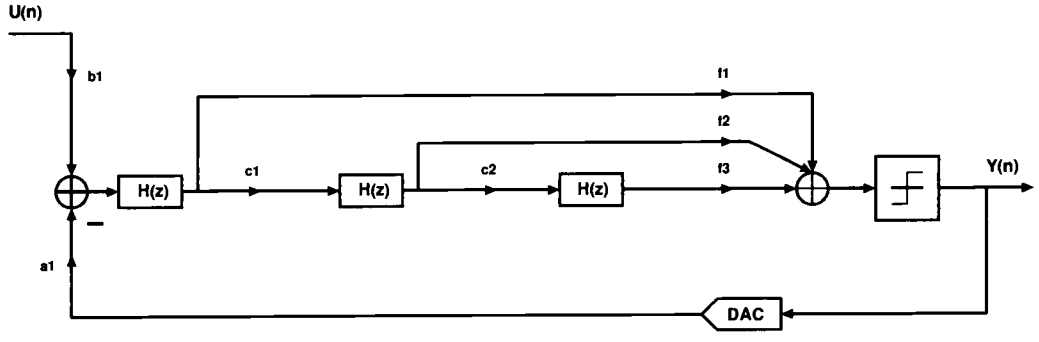

Figure 3.3: Cascade-of-Integrators w/ weighted quantizer inputs.

2. Cascade-of-Integrators with weighted quantizer inputs and local resonator feedbacks:

The NTF's zeros are spread to finite positive frequencies by employing local negative-feedbacks around integrator pairs, which usually result in a Inverse Chebyshev high-

pass NTF response. If these NTF zeros are very close to dc, then the feedback factor (g_i) will be much smaller than other system coefficients, which means a large capacitance spread ratio and hence higher power consumption. This topology is prone to STF peaking in the presence of large transient inputs. Analog weighted summing junction in front of the quantizer is needed. A third-order example is shown in Figure 3.4.

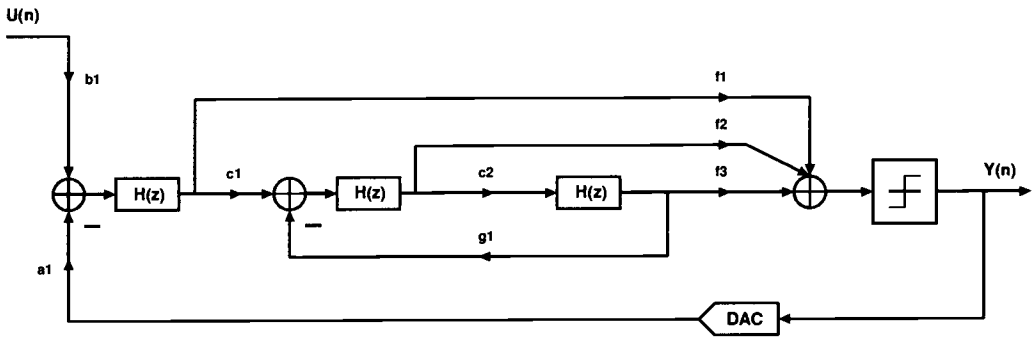

Figure 3.4: Cascade-of-Integrators w/ weighted quantizer inputs and local resonator feedbacks.

3. Cascade-of-Integrators with weighted quantizer inputs and weighted distributed feedbacks:

The addition of properly weighted distributed feedbacks can acquire a smooth NTF magnitude response, while dynamic range scaling is required to avoid integrator overloading. Analog weighted summing junction in front of the quantizer is still needed. Figure 3.5 illustrates a third-order topology as an example.

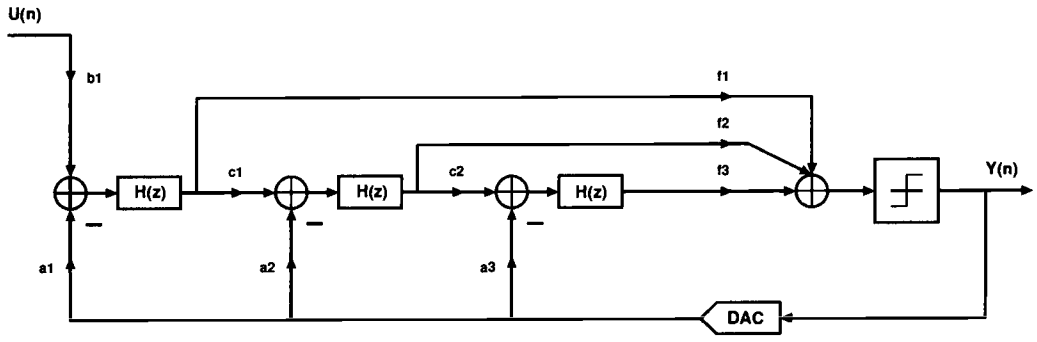

Figure 3.5: Cascade-of-Integrators w/ weighted quantizer inputs and weighted distributed feedbacks.

4. Cascade-of-Integrators with weighted quantizer inputs, local resonator feedbacks and weighted distributed feedforward inputs:

The NTF's zeros are spread to finite positive frequencies. The addition of input feedforward paths allows a certain degree of freedom in specifying both the STF and NTF [29]. Analog weighted summing junction before quantizer is needed. This topology is also referred to as Cascade-of-integrators, feedforward form (CIFF) in [30]. Figure 3.6 illustrates a third-order single-bit CIFF $\Delta\Sigma$ modulator.

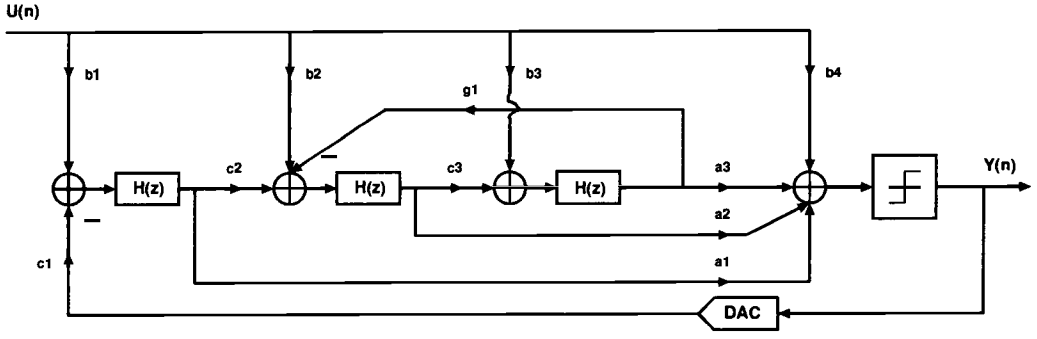

Figure 3.6: A third-order CIFF $\Delta\Sigma$ modulator.

5. Cascade-of-Integrators with weighted distributed feedbacks, local res-

onator feedbacks and weighted distributed feedforward inputs:

Similar to CIFF, the addition of input feedforward paths allows a certain degree of freedom in specifying both the NTF and STF. And local resonator feedbacks help spread NTF zeros across a finite band, which help suppress in-band noise power. Dynamic range scaling is needed to avoid overloading the integrators. In [30], this topology is referred to as Cascade-of-integrators, feedback form (CIFB). Figure 3.7 illustrates a third-order single-bit CIFB $\Delta\Sigma$ modulator.

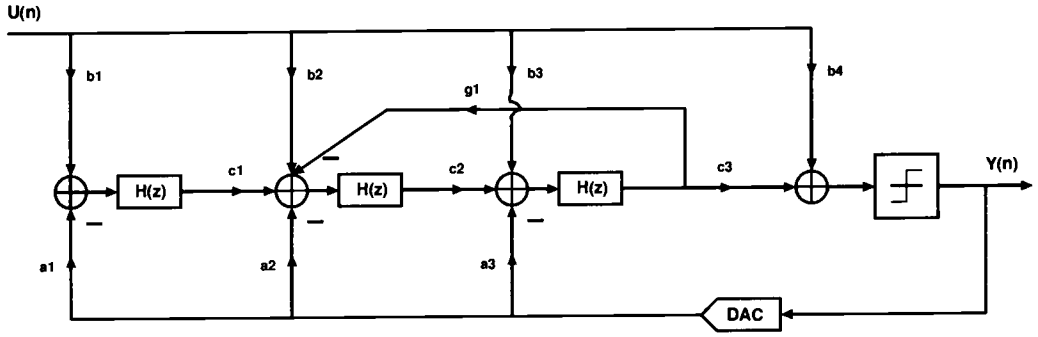

Figure 3.7: A third-order CIFB $\Delta\Sigma$ modulator.

If the "STF$\equiv$1 across the passband" assumption must be satisfied for the sake of a robust stability, then the weighted distributed feedforward inputs are needed to cancel the STF poles except for the real one. Thus, more capacitors are used and the gain factors or system coefficients (i.e., $C_{sampling}$ $vs.C_{integrating}$ ratios) will become fractions, which are 100-1000 times smaller than one [29]. From a circuit design point of view, these coefficients result in a large capacitance spread ratio, which implies high power consumption in practical switched-capacitor implementations. In fact, "STF$\equiv$1" is a rather strong prerequisite for maintaining modulator's stability. A ripple, say 0.5 dB, in passband STF response will not cause severe stability problems but slightly reduce the allowable input signal range. $\Delta\Sigma$ modulators that can't satisfy

this specific condition, yet still maintain good stability, have been reported [31] [32] [33]. A simplified version of CIFF or CIFB is derived by eliminating the weighted distributed feedforward input paths from the original system. Figure 3.8 illustrates a third-order single-bit *simplified* CIFB (SCIFB) $\Delta\Sigma$ modulator. After all feedforward inputs except for the one into the first integrator are removed, the "STF$\equiv$1" assumption is not likely to be satisfied all the time. However, a flat passband STF reponse (but STF$\neq$1) can still be achieved by adjusting the system coefficients.

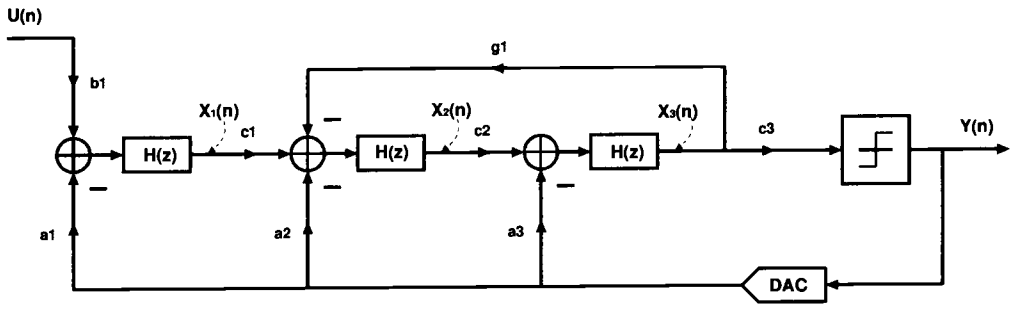

Figure 3.8: A simplified third-order CIFB $\Delta\Sigma$ modulator.

Compared to a simplified CIFF (SCIFF) topology, SCIFB trades the weighted quantizer inputs for the distributed DAC feedbacks. In SCIFB, each integrator's output (X_i) must contain a dc element so that the dc signal within the DAC feedback can be compensated to a certain extent, which imposes additional constraints on the integrators to avoiding overloading. The SCIFF doesn't suffer from this problem because its DAC feedback is only fed into the first integrator, whose output contains no input dc element and theoretically, only quantization noise will be passed on to the subsequent stages. Nevertheless, the analog summation circuit in front of its quantizer requires an extra low-noise op amp, which inevitably increases the circuitry's complexity.

In this thesis, a third-order single-bit SCIFB $\Delta\Sigma$ modulator is designed. In

Chapter 4, details on the system-level design of this modulator will be presented. The nonidealities that are often encountered in the design process will also be explained and analyzed.

3.5. Summary

This chapter reviewed the key idea of noise-shaping. It explained the reason why a high order single-loop modulator with a single-bit quantizer is selected for this particular project. It concluded with an investigation of various existing loop filter topologies.

CHAPTER 4. MODULATOR DESIGN

4.1. Introduction

This chapter will explain the system-level design of the third-order SCIFB $\Delta\Sigma$ modulator mentioned in Chapter 3. The oversampling ratios (OSR) and loop filter's order will be determined. The results of discrete-time system simulations will be presented. Nonidealities such like finite op amp dc gain and limited slew rate will be explained and their effects on the modulator's performance will be discussed.

4.2. IF Frequencies and OSR

As mentioned in Chapter 2, a high IF frequency will relax the selectivity requirements of the RF filter. The IF frequency is usually chosen to be no more than 1/4-1/10 of the RF frequency. An IF around 100 MHz is preferred in the digital high IF receivers [8] [14]. In this thesis, three different IF frequencies are chosen: 78 MHz for GSM, 138.24 MHz for WCDMA, and 110.59 MHz for DECT.

According to the target specifications of the $\Delta\Sigma$ modulator shown in Table 2.2, the in-band quantization noise level N_e should be lower than -76 dBFS for GSM, lower than -56 dBFS for WCDMA, and lower than -67 dBFS for DECT. It is well known that the value of N_e is roughly determined by the following formula [22]:

$$N_e \propto OSR^{-(2L+1)}$$

As mentioned in the previous chapter, an order of 3 (L=3) is chosen for the

loop filter. For a third-order modulator, a 3-fold difference in OSR is sufficient to provide a 30 dB difference in quantization noise level, according to the foregoing formula. An OSR of 192 is chosen for GSM to achieve a high SNR in the order of 100 dB without optimizing NTF zeros. For DECT, 64 is chosen as the value of its OSR. The OSR is chosen as low as 24 since a signal bandwidth of 2 MHz is needed for WCDMA.

Having determined the OSR values, the sampling rates for three standards can be derived. Note that the sampling rate is determined in a way that itself and the channel symbol rate have a integer ratio, which will lead to a nearly constant timing offset over the duration of one symbolic block, and as a result, the requirements of decimation filters are relaxed [14]. The resulting effective sampling rates are as follows: 104 MSample/s for GSM, 184.32 MSample/s for WCDMA, and 147.46 MSample/s for DECT. And the lowpass modulators are clocked at half the effective sampling rates, thanks to the two-path IF-to-baseband scheme illustrated in Figure 2.5.

4.3. Modulator Design for GSM

To meet the modulator's specifications for GSM, a third-order lowpass modulator is needed. A SCIFB topology without using local resonator feedbacks to spread NTF zeros is already sufficient because the signal bandwidth requirement is moderate (100 kHz for GSM). The Delta-Sigma Toolbox (DST) [30] provides a few examples for modulator design. One of the SCIFB examples is shown in Figure 4.1. A -6 dBFS input at 15 kHz (i.e., 15 kHz offset from the IF frequency) is added to the system. The spectrum of the modulator's output is illustrated in Figure 4.2. A peak SNR (PSNR)

of 113.2 dB has been achieved (A signal bandwidth of 270 kHz has been used to evaluate the SNR performance). Figure 4.3 demonstrates its NTF magnitude response. Note that the system coefficients of this modulator stand for capacitance ratios in real circuits. The coefficients shown in Figure 4.1 impose difficulty on the realization of capacitors, especially when parasitics are in presence. Therefore, topologies with better coefficients are needed.

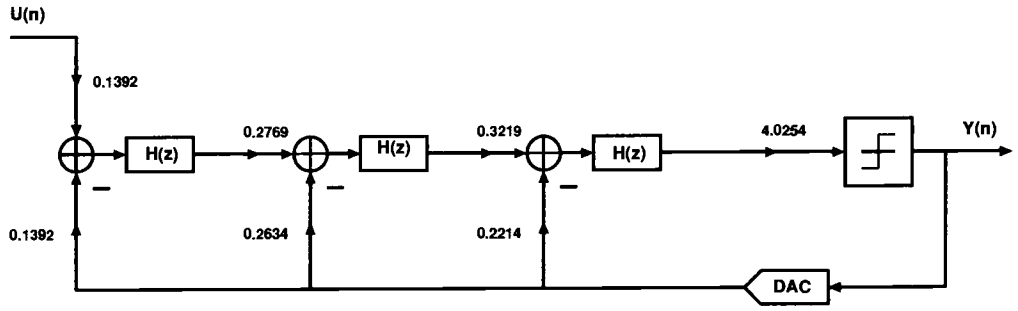

Figure 4.1: A third-order SCIFB: DST's topology.

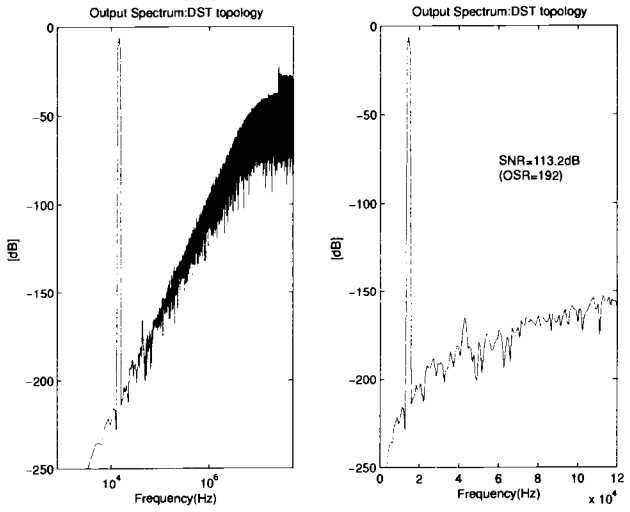

Figure 4.2: Output spectrum: DST's topology (input@15kHz).

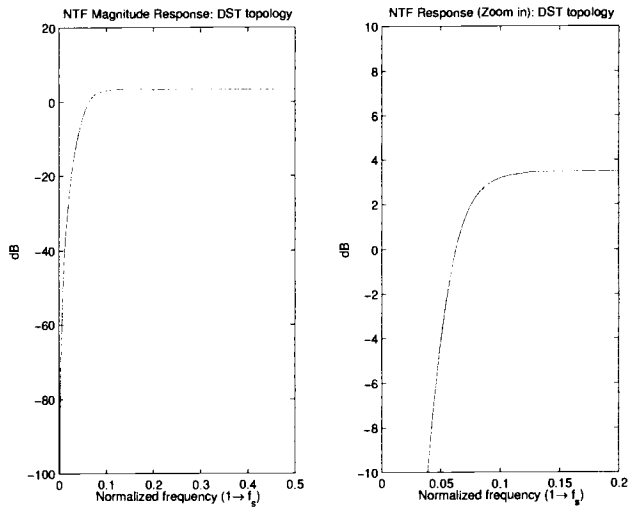

Figure 4.3: NTF magnitude response: DST's topology

In [33], a third-order SCIFB topology was reported (Figure 4.4). Its system coefficients are much easier to implement than those of the DST's topology in switched-capacitor circuits. Moreover, each pair of integrator input and DAC feedback share the same capacitance ratio, which further simplifies the circuitry and saves the chip area. The output of its spectrum is shown in Figure 4.5. In Figure 4.6, the modulator's NTF magnitude response is illustrated. The curve of SNR *vs.* input amplitude level is shown in Figure 4.7.

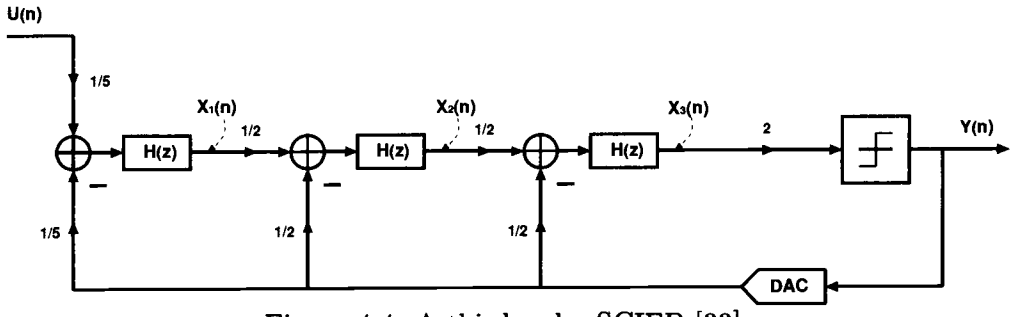

Figure 4.4: A third-order SCIFB [33].

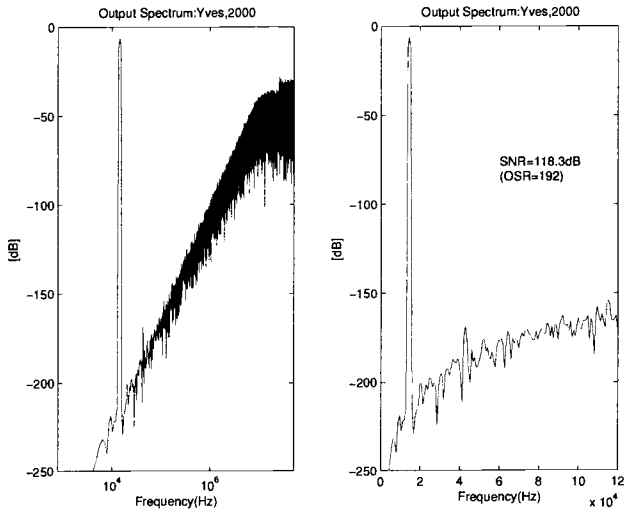

Figure 4.5: Output spectrum: Geerts' topology (input@15kHz).

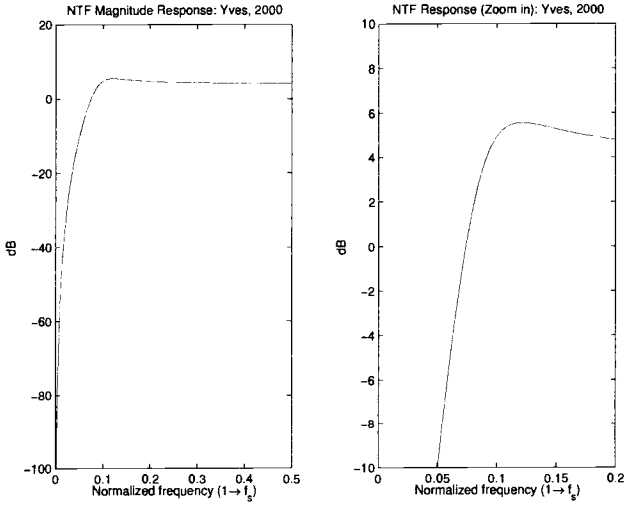

Figure 4.6: NTF magnitude response: Geerts' topology.

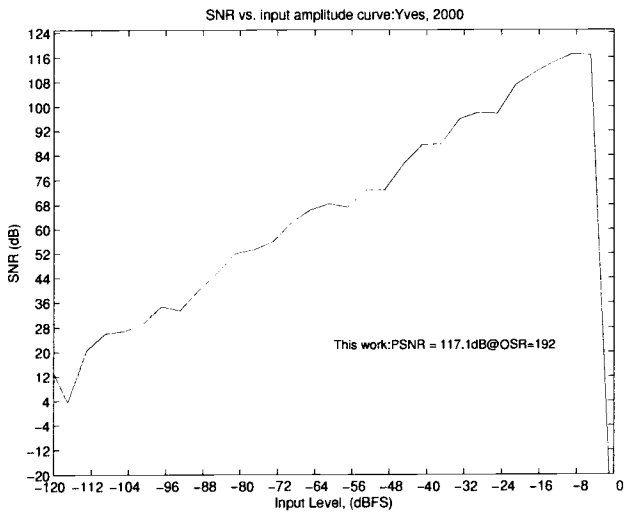

Figure 4.7: SNR vs. input level: Geerts' topology.

One noticeable requirement on a chain of cascaded integrators is that all three integrators have approximately the same output overload level, which is critical for wide dynamic range design when the supply voltage is decreased. Figure 4.8 demonstrates the normalized outputs of the three integrators. An input of -6 dBFS is employed. As shown, both the second and the third integrators have output levels that exceed the maximum normalized limits (1 and -1). Therefore, additional signal scaling is needed.

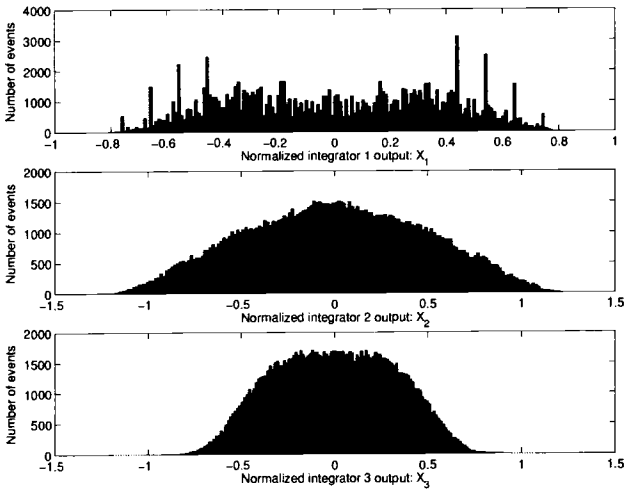

Figure 4.8: The integrator outputs : Geerts' topology.

There are a number of choices in scaling the gain factors based on Yves's topology. Figure 4.9 shows one of the scaled topologies, which is the proposed modulator for GSM applications in this thesis. Figure 4.10 demonstrates the normalized outputs of its three integrators. An input of -6 dBFS at 15 kHz is employed. And a PSNR of 117.6 dB has been achieved with respect to this particular input. Its output spectrum can be found in Figure 4.11. And Figure 4.12 demonstrates its NTF magnitude response. Notice that a small peaking can be seen in the NTF response, but it has not violated Lee's rule of stability [28]. And the curve of SNR *vs.* input amplitude level is shown in Figure 4.13.

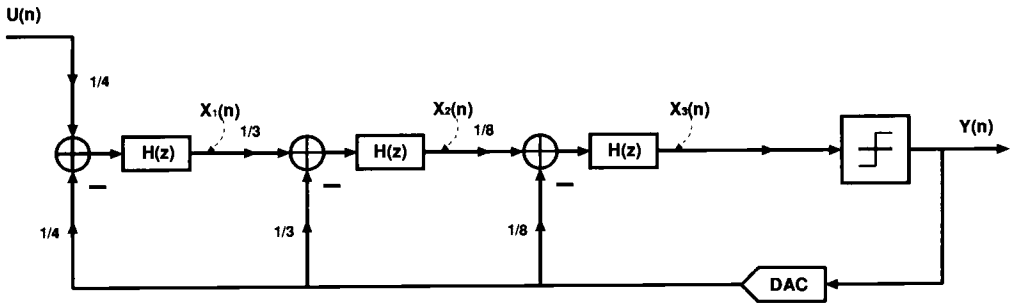

Figure 4.9: The proposed SCIFB topology for GSM applications.

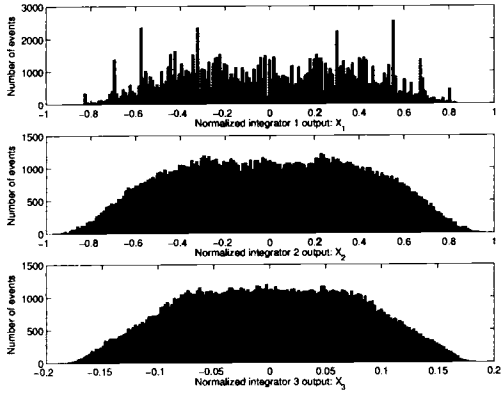

Figure 4.10: The integrator outputs: GSM.

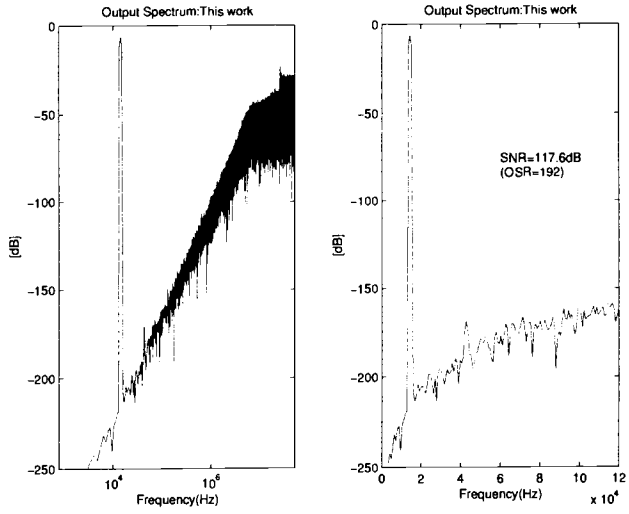

Figure 4.11: Output spectrum: Proposed for GSM applications.

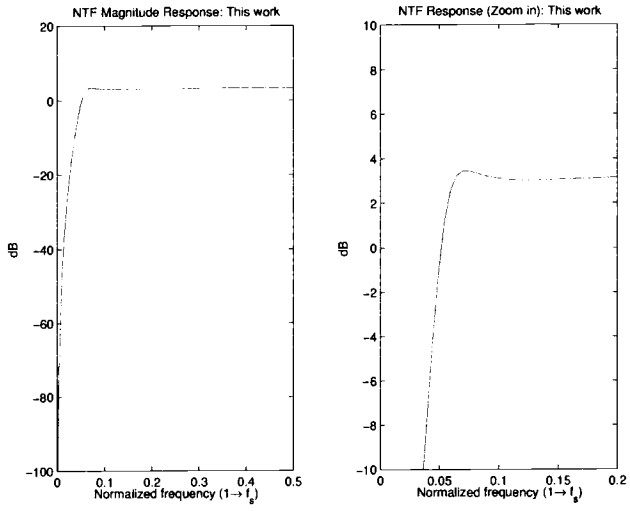

Figure 4.12: NTF magnitude response: Proposed for GSM applications.

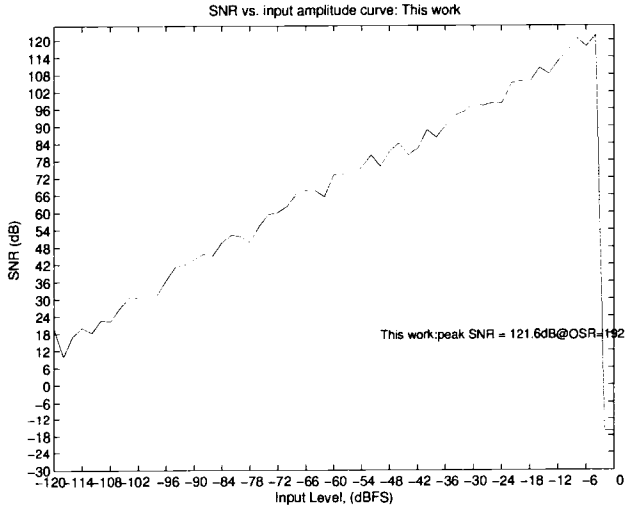

Figure 4.13: SNR vs. input level: GSM.

4.4. Modulator Design for WCDMA

A third-order SCIFB topology with a local resonator feedback (i.e., with optimized NTF zeros) is needed for WCDMA since the signal bandwidth requirement

has been increased to 1.92 MHz. Based on the modulator for GSM described in the previous section, a slightly modified topology is derived for WCDMA by merely changing the feedback factor g_1 from 0 to 1/9, as illustrated in Figure 4.14. This means an additional local resonator feedback path will be activated for WCDMA but disactived for GSM. In the real world, this can be realized by an AND gate in the driving circuitry of the NMOS switch [14]. Figure 4.15 shows the modulator's output spectrum. An input of -6 dBFS at 100 kHz is employed. A PSNR of 57.8 dB has been achieved (A signal bandwidth of 1.92 MHz has been used in evaluating the SNR performance). The modulator's NTF magnitude response is shown in Figure 4.16 and it has obeyed to Lee's rule. The curve of SNR *vs.* input amplitude level is shown in Figure 4.17. And Figure 4.18 illustrates the normalized outputs of its three integrators with an input of -6 dBFS.

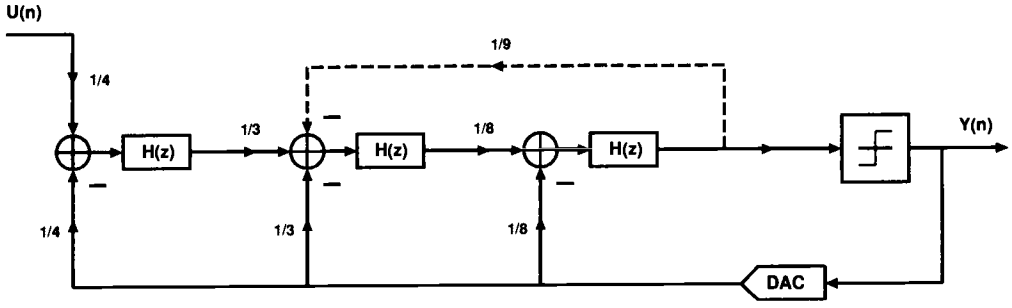

Figure 4.14: The proposed SCIFB topology for WCDMA applications.

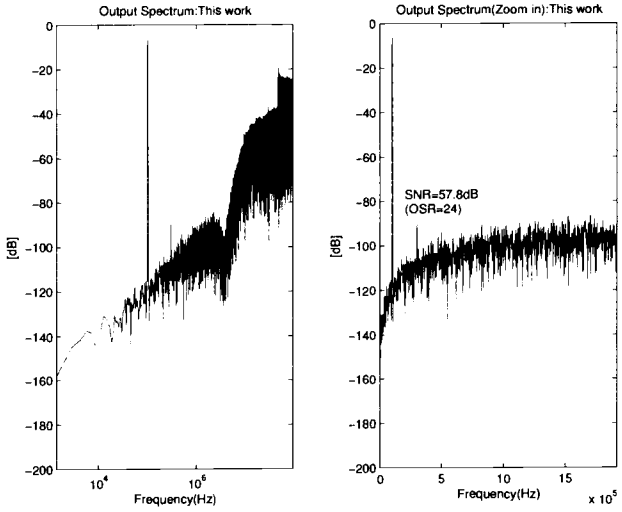

Figure 4.15: Output spectrum: Proposed for WCDMA applications.

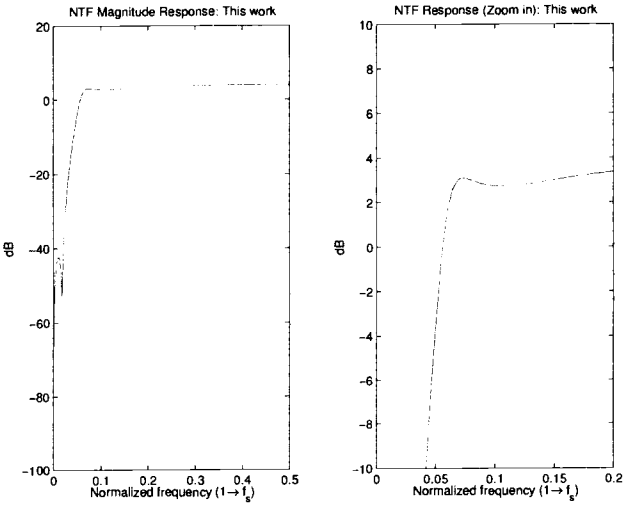

Figure 4.16: NTF magnitude response: Proposed for WCDMA applications.

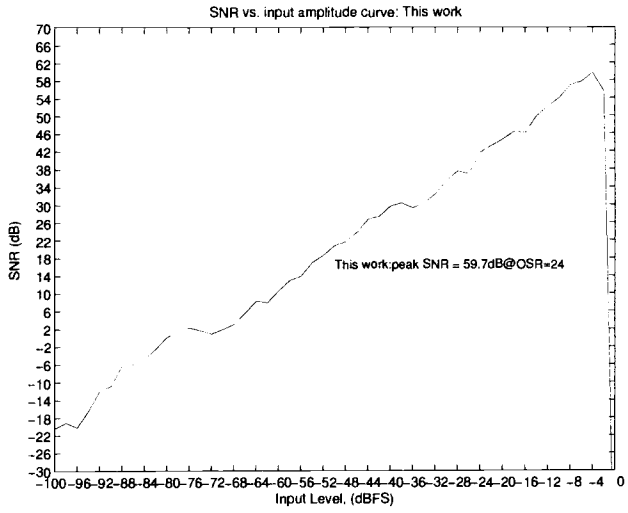

Figure 4.17: SNR vs. input level: WCDMA.

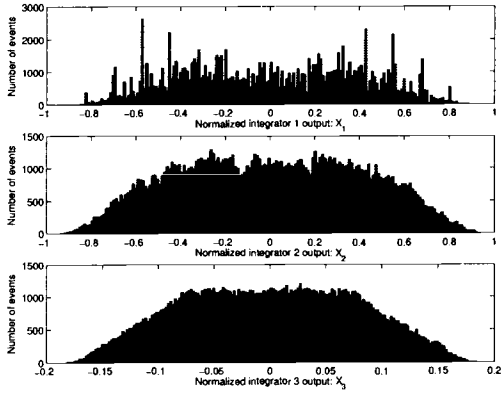

Figure 4.18: The integrator outputs: WCDMA.

4.5. Modulator Design for DECT

DECT and GSM will share the same modulator topology and system coefficients, except that the OSR value is now changed from 192 to 64. Figure 4.19 shows the modulator's output spectrum. An input of -6 dBFS at 100 kHz is employed. A PSNR of 84.4 dB has been achieved (A signal bandwidth of 576 kHz has been used

in evaluating the SNR performance). A third-order harmonic element (300 kHz) is noticeable but it can be suppressed to a large extent if fully differential configuration is employed in the circuit implementation. Since DECT's modulator uses the same topology as that for GSM, its NTF response and integrator output levels are somewhat similar to those acquired in the design of GSM's modulator. Alternatively, DECT can share the same modulator topology with WCDMA. But its SNR performance will get worse. A comparison between the resulting curves of SNR *vs.* input is demonstrated in Figure 4.20. Note that GSM/DECT means the modulator for DECT would use the topology shown in Figure 4.9. WCDMA/DECT means that the modulator for DECT would use the topology illustrated in Figure 4.14.

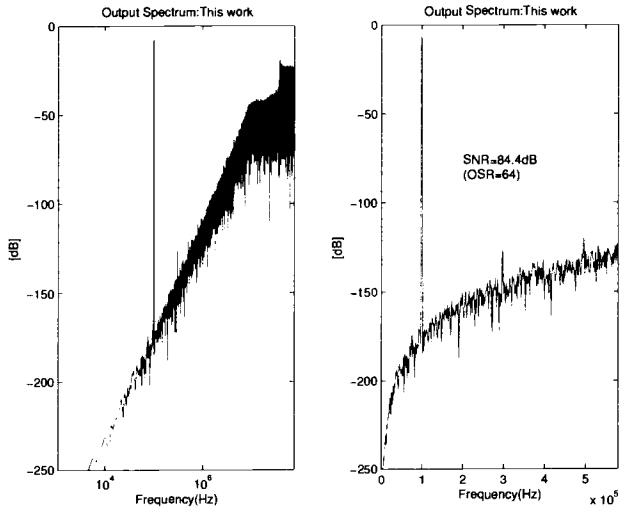

Figure 4.19: Output spectrum: Proposed for DECT applications.

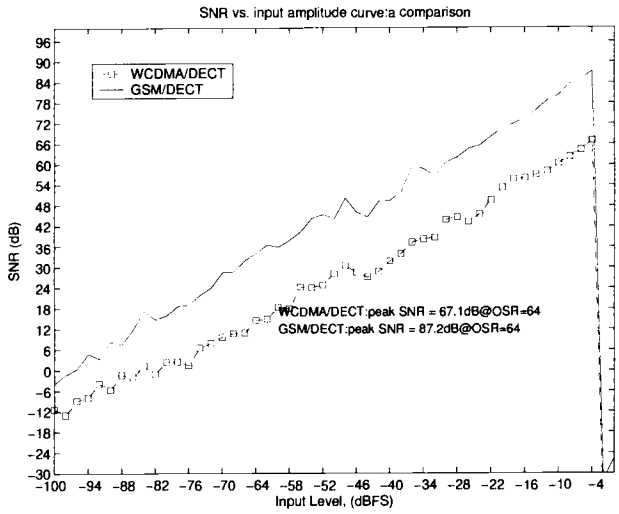

Figure 4.20: SNR vs. input level: A comparison.

4.6. Sampling and Integrating Capacitors

In the real world, thermal noise (referred to as sampling or $kT/C_{Sampling}$ noise in SC circuits) rather than quantization noise may dictate the final SNR performance of a $\Delta\Sigma$ modulator, which is often determined by the first SC integrator when OSR is high. The sizes of the sampling capacitors ($C_{Sampling}$) are usually determined by the $kT/C_{Sampling}$ noise requirement. The following formula is used to calculate the size of $C_{Sampling}$ in the first stage [22]:

$$20\log(\sqrt{\frac{4kT}{OSR \times C_{Sampling}}} \cdot \frac{1}{V_{Ref}}) \leq -(SNR_{Desired} + 3dB)$$

From calculations one can derive that the sizes of $C_{Sampling}$ for all three wireless standards. For GSM (OSR=192), if $SNR_{Desired}$ and V_{Ref} are set to 100 dB and 1.25 V, respectively, then the minimum sampling capacitance in the first integrator

should be 0.6 pF. For WCDMA (OSR=24), the calculated result is 4.42×10^{-2} pF when $SNR_{Desired}$ and V_{Ref} are set to 70 dB and 1.25 V, respectively. And the result for DECT is 0.17 pF (OSR=64), if $SNR_{Desired}$ and V_{Ref} are set to 90 dB and 1.25 V, respectively. Thus, $C_{Sampling}$ of GSM's modulator dictates the minimum sampling capacitance. A capacitance of 0.72 pF is chosen for $C_{Sampling}$ in its first integrator. The $C_{Sampling}$(s) in the second and third integrator can be scaled down in size by a ratio of 1/2-1/10, thanks to preceding noise shaping. For the sake of simplicity, all three RF standards will employ the same set of sampling capacitors. The size of each capacitor can be cut in half if fully differential integrators are used. The sizes of $C_{Integrating}$ and $C_{Feedback}$ (for WCDMA only) are determined by the system coefficients (a_i, b_i, c_i or g_i) derived in the previous section. The capacitors used in this work are listed in Table 4.1. The total capacitance is 6.24 pF (excluding parasitics) and the largest capacitance spread ratio is equal to 24:1. The unit capacitance is 0.06 pF. In order to check the correctness of the system-level analysis, switch-level simulations [37] are carried out. In Figure 4.21, the curve of SNR *vs.* input amplitude level (WCDMA's modulator) as the result of switch-level simulations is illustrated (An op amp dc gain of 80 dB is assumed). Compared to the result of system-level simulations, a PSNR loss as small as 0.6 dB is shown after the sampling and integrating capacitors are taken into consideration. And Figure 4.22 illustrates the normalized outputs of the three integrators with an input of -6 dBFS at 100 kHz. As shown, no additional dynamic range scaling on capacitance is needed.

Table 4.1: Sampling and integrating capacitances.

C_{S1}	0.36 pF	C_{I1}	1.44 pF
C_{S2}	0.18 pF	C_{I2}	0.54 pF
C_{S3}	0.06 pF	C_{I3}	0.48 pF
$C_{Feedback}$	0.06 pF (WCDMA)		

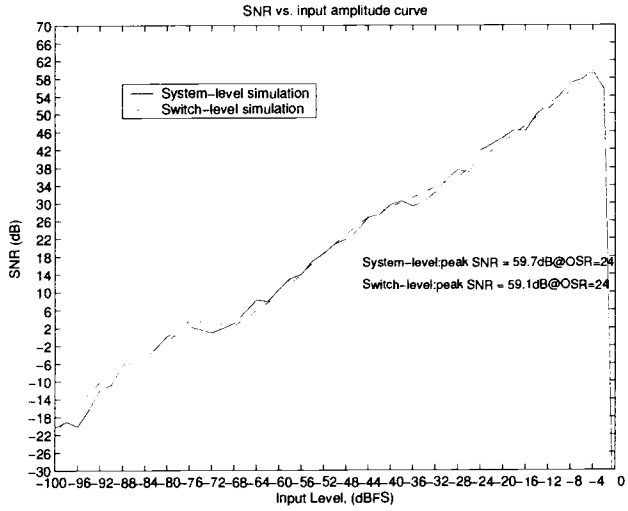

Figure 4.21: SNR vs. input: System and switch-level.

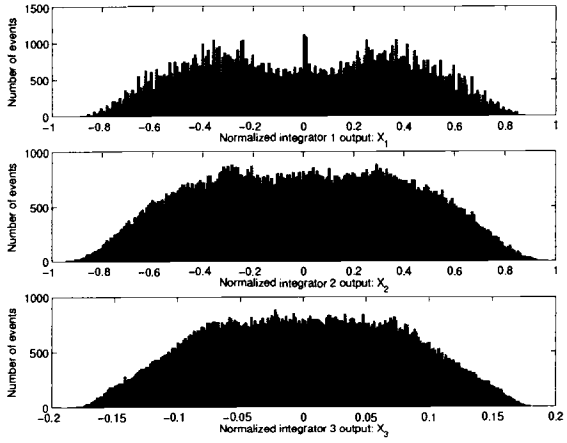

Figure 4.22: The integrator outputs: Switch-level(WCDMA).

4.7. Nonidealities in Modulator Design

4.7.1. Finite Op amp Gain

One of the nonidealities that often appears in the design of $\Delta\Sigma$ modulators is

the finite op amp gain problem. It is well known that an integrator's transfer function can be shown as:

$$H(z) = \frac{z^{-1}}{1-(1-\mu)z^{-1}}$$
$$(\mu = \frac{1}{A_{vgain}})$$

It has been reported that the finite op amp gain problem introduces not only a gain error but also a pole shift in the integrator's transfer function [22]. The pole shift causes a displacement of the NTF zero(s) from its original position, which results in an increase of the in-band quantization noise power level and hence degrades the SNR performance. Figure 4.23 illustrates the simulated SNR loss as a function of the op amp dc gain. The GSM's modulator suffers most SNR loss since it employs the highest OSR value. As shown in the figure, an op amp dc gain of 1500 (63.5 dB) is sufficient to maintain the SNR loss no more than 0.1 dB for all three standards, if other nonidealities are not taken into consideration. In practice, larger op amp gains are needed to reduce harmonic distortions.

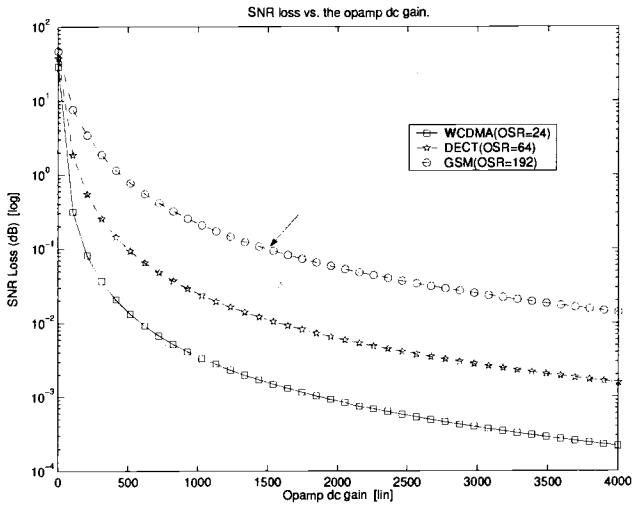

Figure 4.23: SNR loss vs. op amp dc gain.

4.7.2. Finite Op amp Bandwidth and Slew Rate

If a switched-capacitor (SC) integrator output voltage doesn't fully settle within half clock period ($T_{sample}/2$), then harmonics will appear in its output spectrum. Incomplete SC integrator settling is usually caused by a combination of finite op amp bandwidth and slew rate [34]. Finite op amp bandwidth is evaluated by measuing the closed-loop UGBW (unity-gain bandwidth), which is roughly determined by the transconductance of the op amp (g_m) divided by the equivalent loading capacitance at the end of the integration phase (i.e., $g_m/C_{eq.load}$). Slew rate is determined by the available current to charge or discharge $C_{eq.load}$ and is usually given by $I_{tail}/C_{eq.load}$. In the beginning of settling, the slew rate limitation is dominant because $C_{eq.load}$ is being charged and a large-signal effect is caused by the rising edge of clock. Once the charging is done and both input devices are turned on (fully differential op amps), the effect of finite op amp bandwidth takes over. Figure 4.24 illustrates

the slewing and settling process of a non-inverting SC integrator's output during the integration phase. It can be derived that the power consumption ratio (W_1/W_2) is proportional to g_m/I_{tail}. In the state-of-art short channel CMOS process, the g_m/I_{tail} ratio has been reduced, which means the bandwidth requirement (UGBW) is going to dictate the minimum op amp power dissipation.

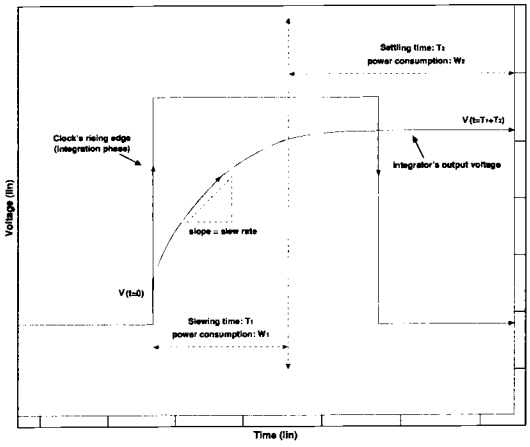

Figure 4.24: Slewing and settling of a SC integrator.

The UGBW and slew rate requirements of SC integrators (particularly the one in the first-stage) can be derived by behavioral level simulation [7] [35] [36]. A simple single-pole op amp model has been used in the simulation and its dc gain is assumed to be 66 dB. Since the modulator for WCDMA will have the highest sampling rate and signal bandwidth, the settling requirements of its integrators are dominant and hence only its settling performance is estimated for simplicity. In Figure 4.25(a) contours of constant peak SNDR (for the first integrator only) are illustrated as a function of g_m of the input device, and the tail current or slewing current I_{tail}. The integrator is usually designed for the flat region where its settling performance is independent of small deviation in amplifier settling accuracy [36]. As shown in Figure 4.25(a), a g_m of 7 ms and a I_{tail} of 500 μA are sufficient for the first integrator to settling

appropriately if other nonidealities are not taken into consideration. Figure 4.25(b) shows contours of constant peak SNDR (for the first integrator only) as a function of UGBW and slew rate, which are given by $g_m/C_{eq.load}$ and $I_{tail}/C_{eq.load}$, respectively. According to Figure 4.25(b), a closed-loop bandwidth of 400 MHz and a slew rate of 100 V/μs are sufficient if other nonidealities are not taken into consideration.

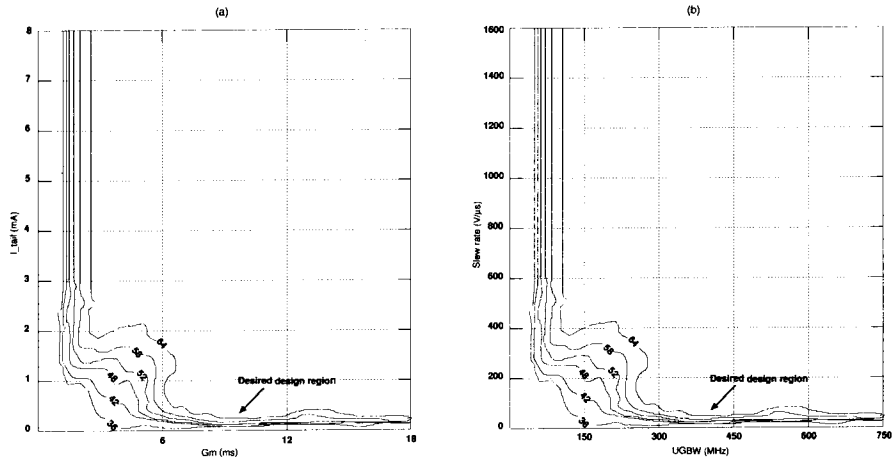

Figure 4.25: Peak SNDR vs. (a) g_m and I_{tail};
(b) closed-loop bandwidth and slew rate.

Alternatively, there are other ways to quantify the minimum UGBW for the sake of accurate intergrator settling. To guarantee a 0.1-percent settling within half the sample period, the UGBW must reach the limit set by the following formula [34]:

$$f_{UGBW} = \frac{7}{\pi} \times f_{Sampling}$$

Since the highest effective $f_{Sampling}$ is equal to 184.32 MHz for WCDMA, a f_{UGBW} as high as 411 MHz is needed. This result matches what has been illustrated in Figure 4.25(b).

4.7.3. Nonideal Switches

MOSFET switches (NMOS or PMOS) usually suffer from non-idealities including charge injection, clock feedthrough, switch kT/C noise, and non-zero switch resistance. Signal-dependent charge injection can be reduced by using the bottom-plate sampling technique with a delayed clock phase or by using the clock-boosted technique [38] [39]. Clock feedthrough can be reduced by employing fully differential configurations and by using smaller switches. Switch kT/C noise can be reduced by using a larger $C_{Sampling}$, as mentioned in Section 4.6. The non-zero on resistance degrades the settling performance of the SC integrator. When a MOS device is operated in linear region, it behaves as a resistor. If a non-zero switch resistance is added to a SC integrator model, the direct outcome is the introduction of gain and pole shift errors in the integrator transfer function because the charging time is now dependent upon the RC constant of the SC network. The change in the integrator transfer function alters the NTF/STF responses of the modulator and increases the in-band quantization noise level. In addition, during the sampling phase, the sampling switch's on resistance is largely dependent upon input signal, which causes harmonic distortions. By making the switch size large enough, one can not only reduce the non-zero on resistance, but also decrease the voltage drop across the switch and hence reduce harmonic distortions [38]. The appropriate NMOS switch size for the sampling network can be roughly estimated by the following formula,

$$\left(\frac{W}{L}\right)_{min} \simeq \frac{7}{\mu_N C_{OX}} \cdot \frac{C_{max} \cdot f_{Sampling}}{(V_{GS} - V_{TH})}$$

The highest effective $f_{Sampling}$ is equal to 184.32 MHz (for WCDMA) and

C_{max} is 1.44 pF in the first stage. The latter implies that switches in the first stage are larger than those in the second and third stages in size. The overdrive voltage, (V_{GS}-V_{TH}), is dependent on process parameters and can be roughly estimated to be 0.7 V for a 2.5 V power supply. The product of μ_N C_{OX} is estimated to be 1×10^{-4} for a general CMOS process. From calculations, the minimum NMOS switch size is determined by a width-to-length ratio of 20/1, which leads to an allowed maximum switch on resistance ($R_{on.max}$) of approximately 350 Ω. Since PMOS device is usually 2-3 times slower than its NMOS counterpart, the minimum PMOS switch's width-to-length ratio is at least 40/1.

4.7.4. Flicker Noise

Thermal noise and flicker noise are the two most important types of intrinsic noises in MOS devices. As mentioned in Section 4.6, thermal noise is attenuated by using large sampling capacitors in SC circuits. Flicker noise (also called 1/f noise) has a spectral power density that is roughly inversely proportional to frequency, which implies that it is predominant at lower frequencies, and as a result, aliasing does not have to be taken into consideration and the in-band noise power won't be reduced substantially by merely increasing the OSR. Although flicker noise can be decreased by increasing the gate area of the MOSFETs, it is not desirable in the low power and high integration design. Alternatively, either autozeroing [22] or chopping [40] can be employed to solve this problem. For the ΔΣ modulator in this thesis, two choppers clocked at a quarter of the $f_{Sampling}$ are placed around the op amp in the first integrator, which pushes most of the amplifier 1/f noise and dc offset to higher frequencies (e.g., $f_S/4$ and $3f_S/4$) by a pair of modulation/demodulation operations.

Figure 4.26 illustrates the implementation of the choppers.

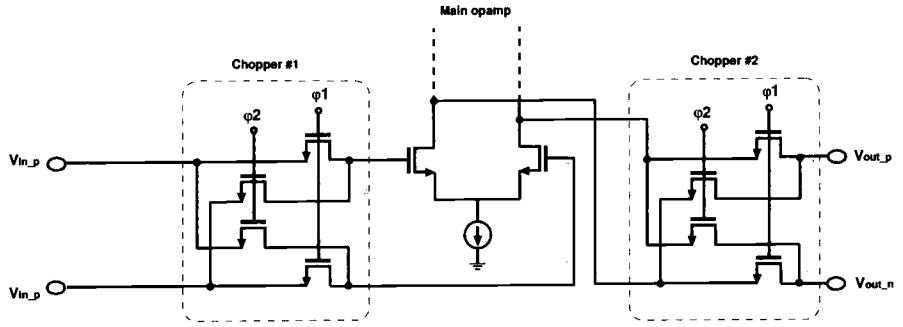

Figure 4.26: Chopping in the first op amp.

4.7.5. Capacitor Mismatch

Capacitor mismatch degrades the accuracy of the modulator coefficients, which changes the integrator transfer function and consequently the NTF and STF responses of the $\Delta\Sigma$ modulator. In a state-of-art CMOS process, the relative accuracy of capacitor ratio can be within 0.1 percent. In order to model the mismatch error of a capacitor, a Gaussian-distributed random sequence, E_N, with standard deviation of ± 0.001 is generated. The original capacitor C_i is replaced by $C_i(1+E_i)$. And the $\Delta\Sigma$ modulator is simulated on the switch-level. In Figure 4.27, the variation of PSNR caused by capacitor mismatch is illustrated. As shown, for the proposed third-order SCIFB $\Delta\Sigma$ modulator, there is no significant change in SNR performance due to capacitor mismatch.

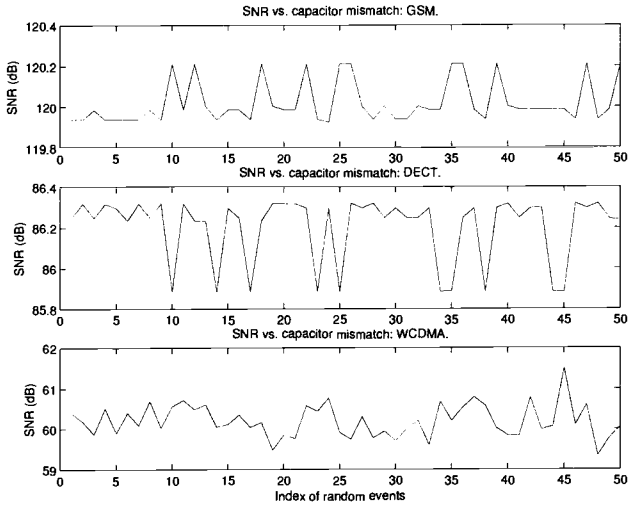

Figure 4.27: Peak SNR variation as a function of capacitor mismatch.

4.8. Summary

This chapter explained the system-level design of the third-order SCIFB $\Delta\Sigma$ modulator. The IF frequencies and oversampling ratios (OSR) were determined. The results of both system level and switch level simulations were presented. Nonidealities including finite op amp dc gain, linear settling, limited slew rate, nonideal switches, flicker noise and capacitor mismatch were explained and their effects on the modulator's performance were discussed.

CHAPTER 5. CIRCUIT IMPLEMENTATIONS

5.1. Introduction

This chapter will describe the circuit-level design of the key building blocks of the proposed third-order SCIFB $\Delta\Sigma$ modulator (Figure 5.1), which include switched-capacitor integrators, operational transconductance amplifiers (OTA), a single-bit quantizer (a latched comparator followed by a static SR latch) and a clock generator. The three integrators and the comparator are controlled by two-phase, non-overlapping clocks, ck1 and ck2; an early clock phase ck1e to strobe the latched comparator; two delayed clock phases, ck1d and ck2d; and complements of the delayed phases, ck1db and ck2db. The timing diagram of the clock phases is illustrated in Figure 5.2.

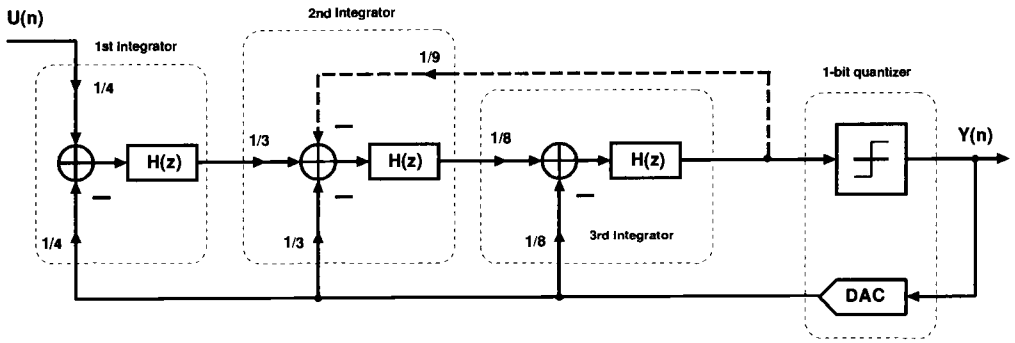

Figure 5.1: The proposed third-order $\Delta\Sigma$ modulator.

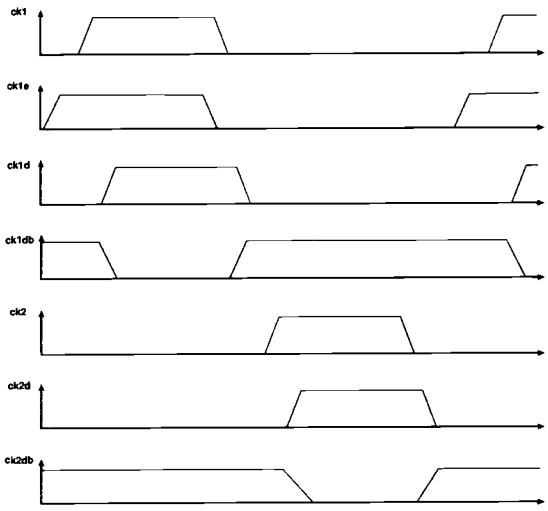

Figure 5.2: Timing diagram of clock phases.

5.2. Circuit Blocks

5.2.1. SC Integrators

The first integrator is shown in Figure 5.3. During ck1, the input voltage, V_i, is sampling onto $C_{Sampling}$. During ck2, charge proportional to the difference between V_i and DAC refence voltage, V_{ref}, is transferred from $C_{Sampling}$ to $C_{Integrating}$. The sampling and integrating capacitances are shown in Figure 5.3. The input common-mode voltage, V_{cm_i} is set to 0.9 V for a 2.5 V supply, which allows switches S_3 and S_4 to be implemented using only NMOS devices. The implementation of the switches are listed in Table 5.1. The sizing of these switches obeys to the calculation results in Section 4.7.3, where NMOS switch's W/L ratio is at least 20/1, and the minimum PMOS switch's W/L ratio is 40/1. S_1 and S_2 are CMOS transmission gates in order to diminish the influence of input signal upon switch on-resistance [22]. The delayed clock phases ck1d and ck2d reduce signal-dependent charge injection from switches S_3

and S_4 onto $C_{Sampling}$ and $C_{Integrating}$ [41]. First, switches labeled ck1(2) are turned off, the charge injection from those switches remains independent of the input signal. Because one of plates is now floating, turning off switches labeled ck1(2)d shortly after does not introduce additional signal-dependent charge-injection errors. S_5 resets the integrating capacitors during power-on or the transformation from one standard to another. In addition, it also serves as clipper for the integrator output voltages at high swing, which is often referred to as the integrator reset approach for modulator stability [22].

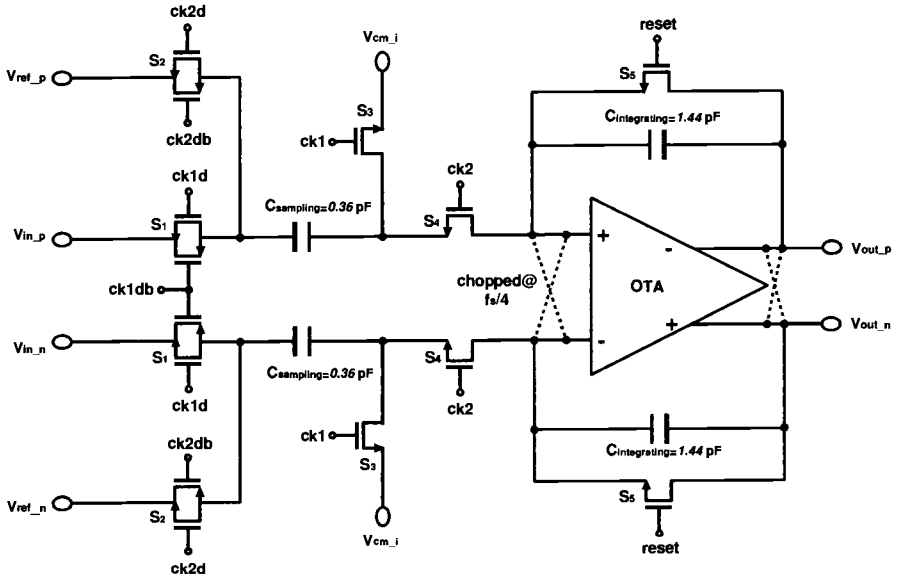

Figure 5.3: The first integrator.

Table 5.1: Switches in the first integrator.

Switch	Type	Size(in μm)
S_1	CMOS	7/0.35(NMOS);21/0.35(PMOS)
S_2	CMOS	7/0.35(NMOS);21/0.35(PMOS)
S_3	NMOS	14/0.35
S_4	NMOS	14/0.35
S_5	NMOS	1/0.35

The second integrator is shown in Figure 5.4. The input common-mode voltage, V_{cm_i} is set to 0.9 V and the mid-supply reference voltage, V_{mid}, is 1.25 V for a 2.5 V supply. The additional feedback branch, which creates the local resonator in the case of WCDMA, is controlled by the enable signal, en_{WCDMA} and ck1d, through a MOS AND gate. The sampling and integrating capacitances are shown in Figure 5.4. And the implementation of the switches are listed in Table 5.2.

Table 5.2: Switches in the second integrator.

Switch	Type	Size(in μm)
S_6	CMOS	5/0.35(NMOS);15/0.35(PMOS)
S_7	CMOS	5/0.35(NMOS);15/0.35(PMOS)
S_8	NMOS	10/0.35
S_9	NMOS	10/0.35
S_{10}	NMOS	10/0.35
S_{11}	NMOS	5/0.35
S_{12}	CMOS	5/0.35(NMOS);15/0.35(PMOS)
S_{13}	NMOS	1/0.35

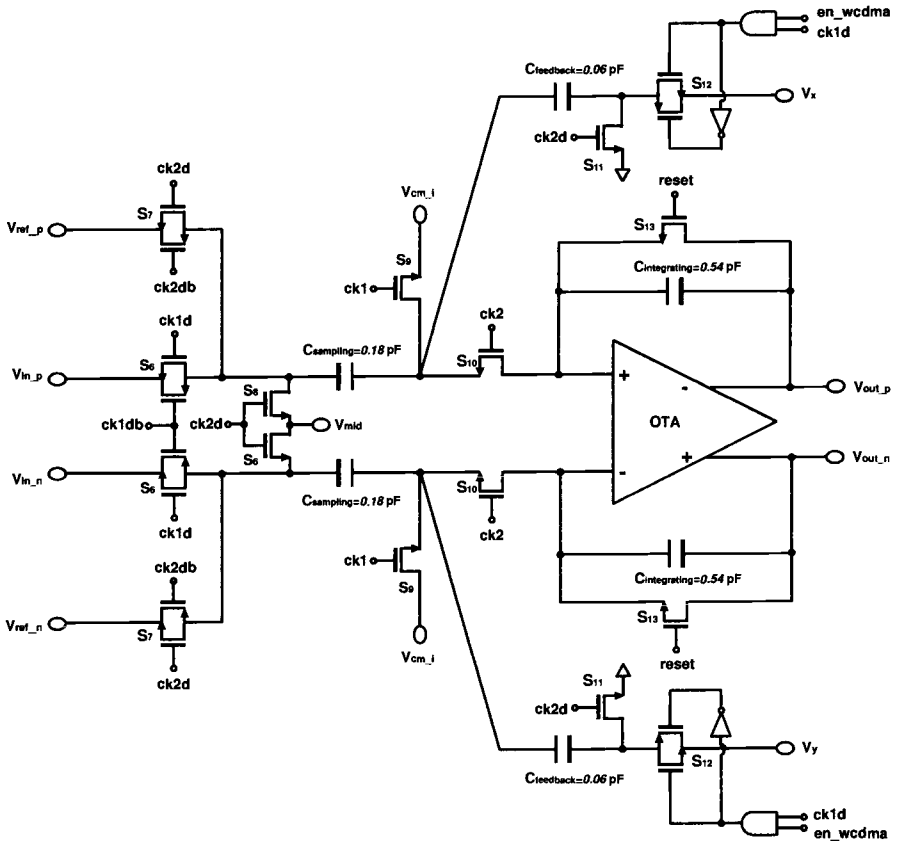

Figure 5.4: The second integrator.

The third integrator is shown in Figure 5.5. Its schematic is similar to that of the first integrator. Note that V_x and V_y are marked on purpose, which implies that the inverting feedback coefficient can be acquired by reversing the polarity at the output. The sampling and integrating capacitances are shown in the same figure. And the implementation of the switches are listed in Table 5.3.

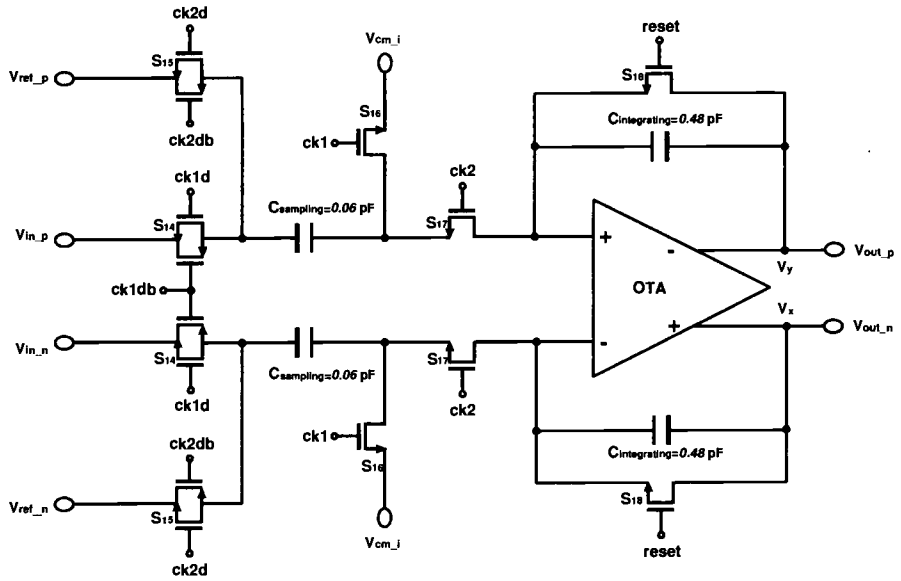

Figure 5.5: The third integrator.

Table 5.3: Switches in the third integrator.

Switch	Type	Size(in μm)
S_{14}	CMOS	5/0.35(NMOS);15/0.35(PMOS)
S_{15}	CMOS	5/0.35(NMOS);15/0.35(PMOS)
S_{16}	NMOS	10/0.35
S_{17}	NMOS	10/0.35
S_{18}	NMOS	1/0.35

5.2.2. Operational Transconductance Amplifier (OTA)

Operational Transconductance Amplifiers (OTA) are critical in the design of $\Delta\Sigma$ modulators. High gain and high bandwidth OTAs are needed for the proposed modulator due to the SNR specifications and high clock rates. Gain boosting techniques [42] are employed in the design of OTA in order to acquire high gain and high bandwidth at the same time. The basic principle is that a dc gain enhancement can be acquired without affecting the gain and phase characteristics of the op amp at high

frequencies. In order to meet the settling requirements imposed by a clock rate over 100 MHz while maintaining a low power consumption, a telescopic amplifier topology (Figure 5.6) is chosen for the main amplifier because of its good frequency response and relatively low bias current budget. The switched capacitor common-mode feedback (CMFB) circuit [43] is used to track the output common-mode voltage level. The value of tail current, I_{tail}, is 590 μA for the main amplifier in the first stage. To save power, the value of I_{tail} can be scaled down by a ratio of 1/2 and 1/4 for the OTAs in the second and third stage, respectively. The sizing of the transistors in the main amplifier is described in Table 5.4.

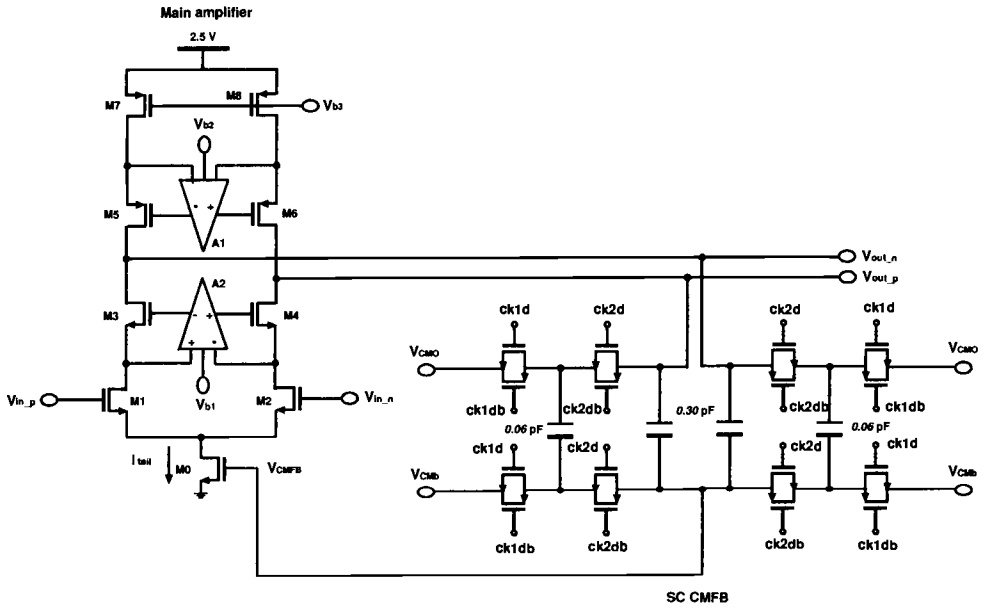

Figure 5.6: Main amplifier schematic.

Table 5.4: Device sizing in the main amplifier.

Device	Type	Size(in μm)
$M_{1,2}$	NMOS	120/0.35
$M_{3,4}$	NMOS	50/0.35
$M_{5,6}$	PMOS	80/0.35
$M_{7,8}$	NMOS	200/1

The auxiliary amplifiers are designed using the folded-cascode topology, which aims to provide sufficient dc gain enhancement. A1, shown in Figure 5.7, is on the PMOS side and has a pair of NMOS differential input devices for the sake of wide voltage swing [44]. The same strategy applied to the auxiliary amplifier on the NMOS side, A2, shown in Figure 5.8, in which a pair of PMOS transistors are used as the input devices. The CMFB loop is built by connecting the output nodes to gates of two large transistors, which are working in the linear region. In both auxiliary amplifiers, I_{D7}, I_{D9} and I_{D11} are biased at 40 μA, 20 μA and 20 μA, respectively. The biasing plan is the following: (1) Individual biasing network is used for each main amplifier to provide sufficient isolation; (2) The auxiliary amplifiers in three integrators share the same biasing network in order to save power. The high-swing current mirror known as Sooch Mirror [45] is used in the design of biasing network to achieve sufficient output swing for a 2.5 V supply.

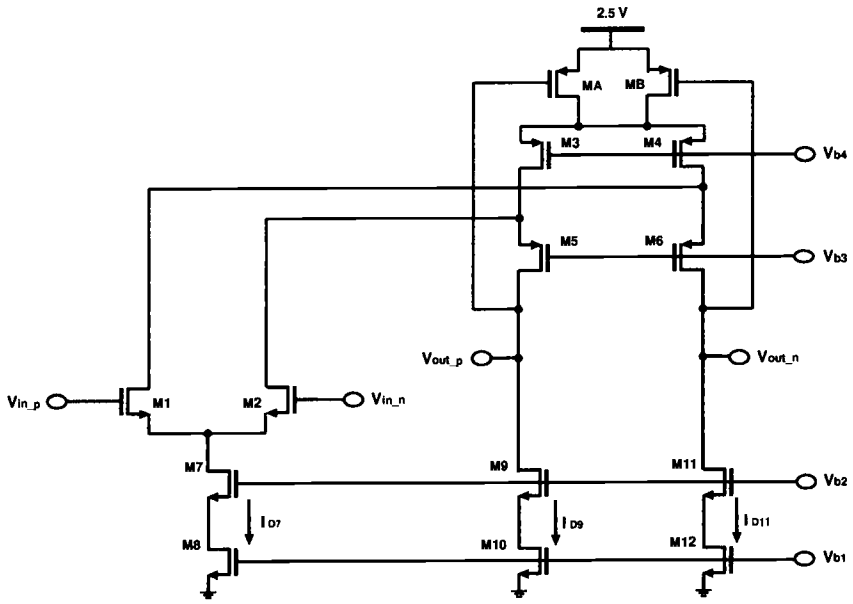

Figure 5.7: Auxiliary amplifier schematic: A1.

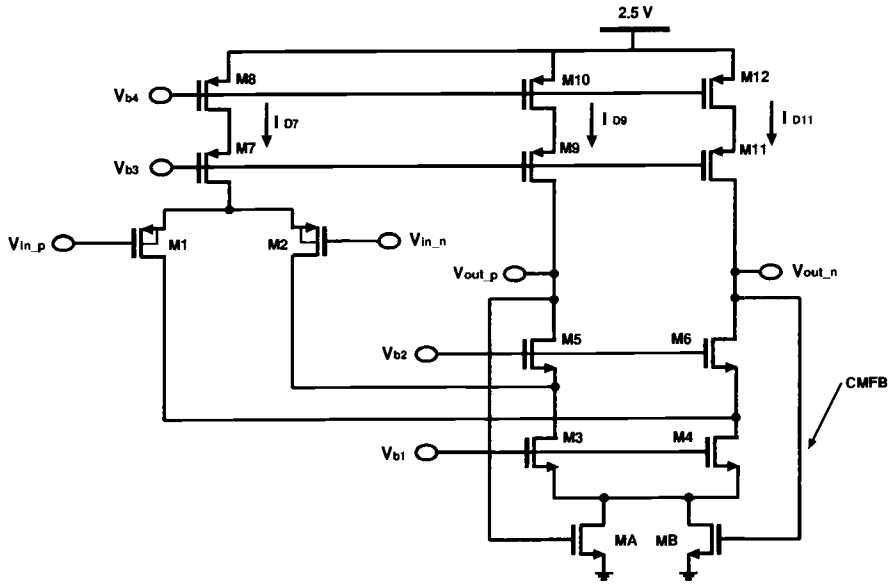

Figure 5.8: Auxiliary amplifier schematic: A2.

The simulated UGBW and phase margin (PM) of the OTA are 480 MHz and 56 degree, respectively. The simulated dc gain is 83 dB. The idea of the foregoing gain boosting scheme is that the dc gain is determined mainly by the folded-cascode auxiliary amplifiers, while the telescopic main amplifier is optimized for high bandwidth. The direct undesirable result of this configuration is a lower dc gain. To alleviate this problem, a preamplifier can be added in front of the main amplifier [46], as illustrated in Figure 5.9. A dc gain as high as 96 dB has been reported using this amplifier topology [47]. However, this amplifier inevitably consumes more power than the previous one (extra 2 to 3 mW at a 2.5 V supply).

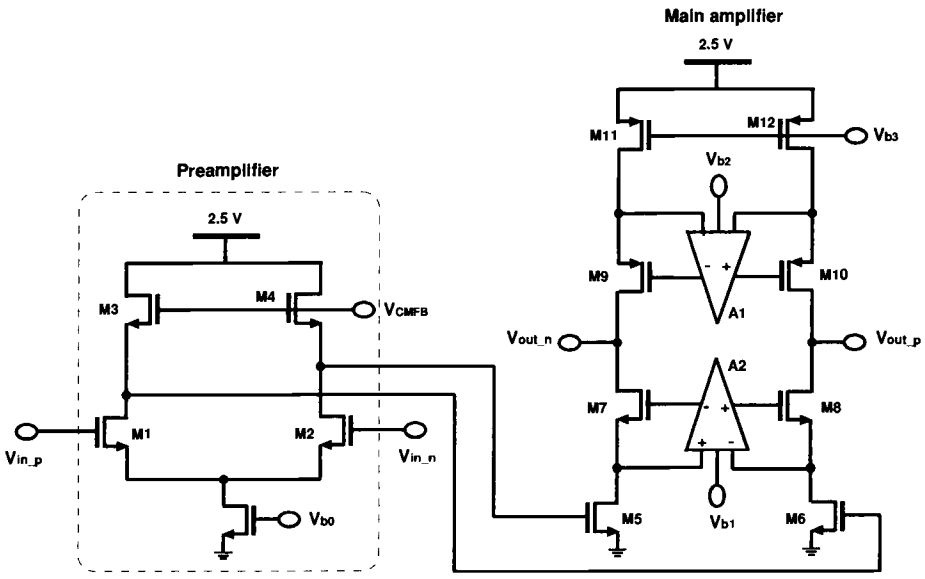

Figure 5.9: Main amplifier w/ a preamplifier.

5.2.3. Single-Bit Quantizer

The single-bit quantizer is composed of a dynamic regenerative comparator

and a static SR latch, as shown in Figure 5.10. The comparator is based on the design of [46] for the sake of low power consumption. The comparator is in the reset mode when the clock phase ck1e is low, and the outputs are set to V_{DD} by M_9 and M_{10}. When ck1e goes high, the comparator enters the regenerative mode, and M_3-M_8 form a positive feedback loop in order to amplify the input difference, which is sensed by M_1 and M_2, to a full-scale rail-to-rail output. Once the comparator makes a decision, the cross-coupled transistors $M_{3,4}$ and $M_{7,8}$ will shut down all connections between V_{DD} and V_{SS}, which leads to null dc power consumption. This operation is illustrated in Figure 5.10: When V_{inp} is high and V_{inn} is low, V_x becomes low and V_y becomes high. As a result, M_3 and M_8 are on ($\surd$) but M_4 and M_7 are off ($\times$) and current flow exists, hence the comparator is turned off. The sizing of the transistors in the comparator is described in Table 5.5.

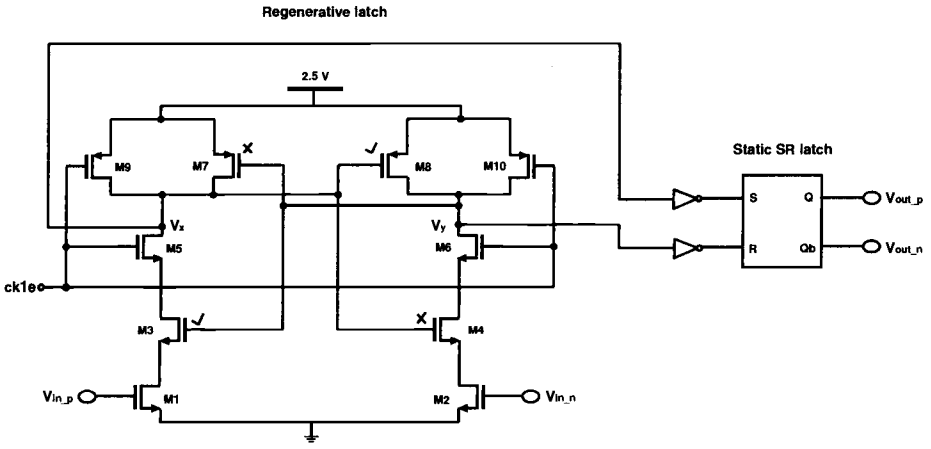

Figure 5.10: Single-bit quantizer.

Table 5.5: Device sizing in the comparator.

Device	Type	Size(in μm)
$M_{1,2}$	NMOS	16/0.35
$M_{3,4}$	NMOS	10/0.35
$M_{5,6}$	NMOS	10/0.35
$M_{7,8}$	PMOS	30/0.35
$M_{9,10}$	PMOS	10/0.35

5.2.4. Clock Generation

The clock generator is based on the design of [48]. The delayed version of the two non-overlapping clocks is created in order to reduce signal-dependent charge injection [22]. The inversed version of clocks are also needed since CMOS transmission gates are used. No clock booster is used.

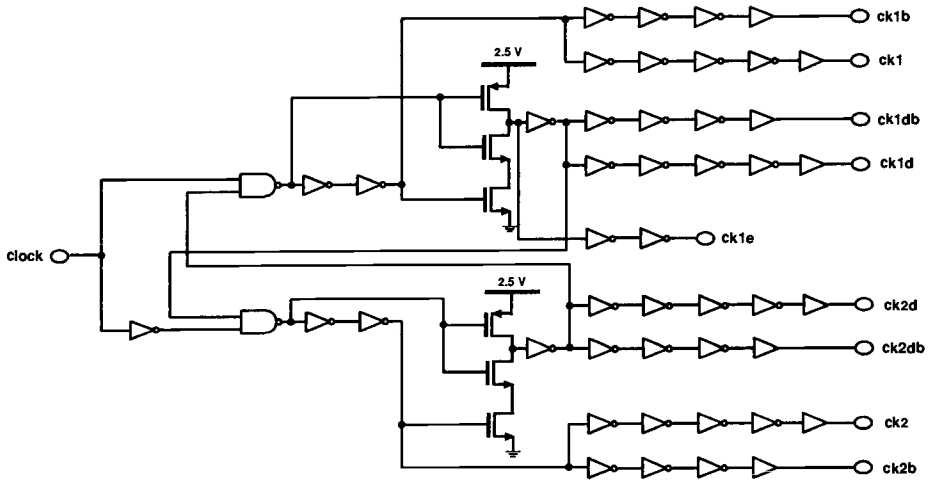

Figure 5.11: Clock generator schematic.

5.3. Layout Considerations

Since the proposed $\Delta\Sigma$ modulator will be implemented as part of a multi-standard RF receiver chip, a clear separation between analog and digital building

blocks is required. Moreover, the I/Q paths should be laid out symmetrically and share the clock generator and the clock bus in order to reduce the timing offsets between two channels. Figure 5.12 illustrates the floor plan.

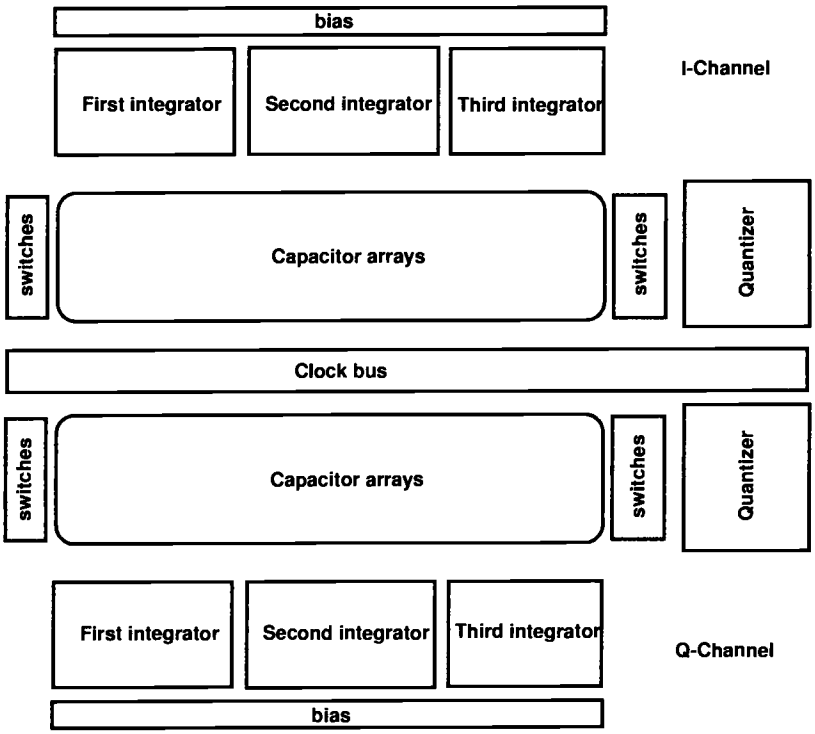

Figure 5.12: Layout floor plan.

5.4. Summary

This chapter explained the circuit implementations of a third-order $\Delta\Sigma$ modulator. The design of building blocks, which include SC integrators, OTAs, a single-bit quantizer, and a clock generator, were explained. This chapter concluded with the floor plan.

CHAPTER 6. POST-LAYOUT SIMULATION RESULTS

The proposed third-order $\Delta\Sigma$ modulator is part of a multi-standard RF receiver, which will be fabricated in a 0.35-μm TSMC, DP5M 2.5 V CMOS process. Based on the post-layout simulation, the total receiver active area is estimated to be $16mm^2$ and the modulator (without the decimation filter) will roughly take up $0.5mm^2$. The fully differential sinusoidal input signal (the IF signal) is bandpass filtered before entering into the modulator. During the simulation, the acquired data stream is stored in a file, which is then loaded into MATLAB for post-filtering and spectral analysis. Intermodulation are tested only for GSM, since its IP3 requirements dictate. Two sinusoids, one of which has a frequency 100 kHz lower than the IF center frequency and the other 200 kHz higher than the IF frequency, are sent into the modulator. A noticeable image component of -30 dB appears at 300 kHz offset from the IF center frequency, which prevents the IP3 performance of GSM from meeting the specifications listed in Table 2.2. The simulated IIP3 (Input-referred IP3) value for GSM is 28 dBV.

Figure 6.1 shows the simulated fast Fourier transform (FFT) of the modulator for the GSM standard. An IF input signal at 15-kHz offset from the IF center frequency (78 MHz) is driving the modulator. Compared with the output spectrum illustrated in Figure 4.11, where only quantization noise is taken into account, the spectrum shown in Figure 6.1 indicates that thermal noise is responsible for a 30 dB loss in overall SNR performance, and hence the noise floor seen here is dictated by thermal noise. The thermal noise floor is flat up to 100 kHz, which is half the signal bandwidth for GSM standard. A noticeable harmonic at 45 kHz (third-order) dictates the signal-to-noise and distortion ratio (SNDR) performance.

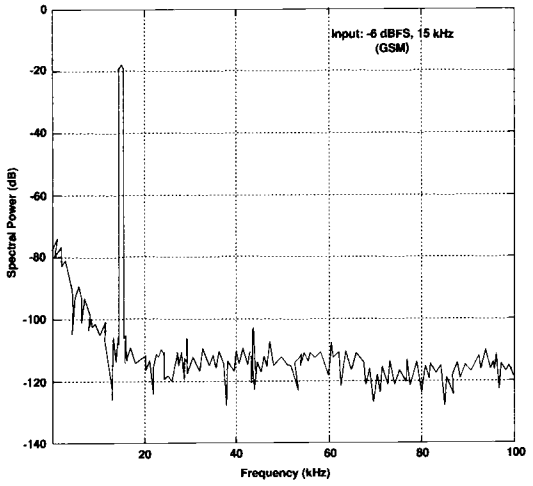

Figure 6.1: Simulated output spectrum: GSM.

Figure 6.2 shows the simulated FFT of the modulator for the WCDMA standard. An IF input signal at 100-kHz offset from the IF center frequency (138.24 MHz) is added. Compared with the output spectrum illustrated in Figure 4.15, where only quantization noise is taken into account, the spectrum shown in Figure 6.2 indicates that thermal noise floor is higher than the quantization noise floor for frequencies up to 800 kHz. The thermal noise floor is roughly flat up to 2 MHz, which is half the signal bandwidth for WCDMA standard.

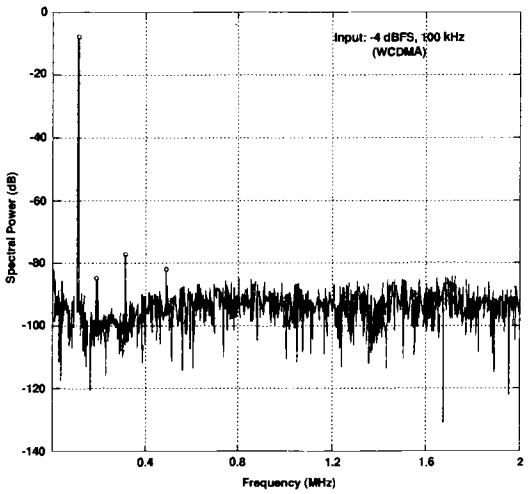

Figure 6.2: Simulated output spectrum: WCDMA.

Figure 6.3 shows the simulated FFT of the modulator for the DECT standard. An IF input signal at 100-kHz offset from the IF center frequency (110.59 MHz) is driving the modulator. Compared with the output spectrum illustrated in Figure 4.19, the spectrum shown in Figure 6.3 indicates that thermal noise floor is higher than the quantization noise floor for frequencies up to 300 kHz. The thermal noise floor is roughly flat up to 576 kHz, which is half the signal bandwidth for DECT standard. A noticeable harmonic at 300 kHz (third-order) limits the SNDR performance.

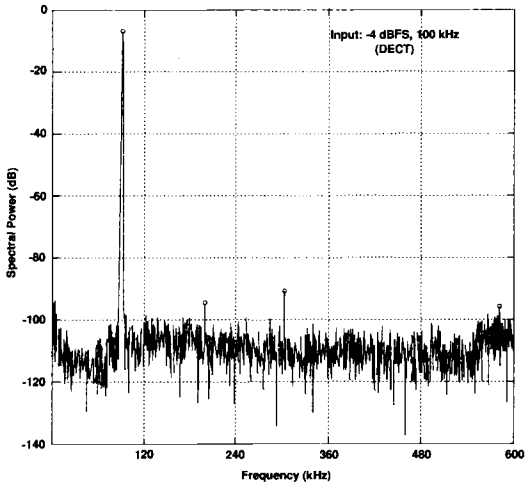

Figure 6.3: Simulated output spectrum: DECT.

Figure 6.4 illustrates the simulated SNDR *vs.* input amplitude level curves for all three standards. As shown, the simulated peak SNDR values are 80.1 dB (GSM), 55.3 dB (WCDMA), and 64.9 dB (DECT). The simulated dynamic range (DR) values are 90 dB (GSM), 70 dB (WCDMA), and 76 dB (DECT).

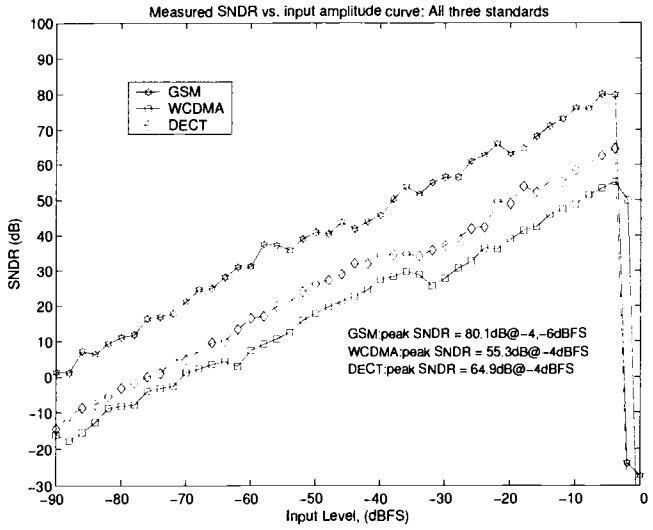

Figure 6.4: Simulated SNDR vs. input: all three standards.

The post-layout simulation results of the proposed modulator are given in Table 6.1. For comparison purposes, the modulator specifications reported in [7] and [14] are also listed. The dynamic range (DR) performance of this single-loop modulator is worse than that reported in [7], where a cascaded (MASH) 2-2 topology was used at a price of, however, much higher power consumption (65 mW in total for GSM/DECT applications with a 3.3 V supply).

Having demonstrated the post-layout simulation results, the author believes that it is instructive to mention the chip-level test plan, since the receiver is already in the process of fabrication (a standard 0.35 μm, 2.5 V, DP5M CMOS process in this case). During the test, a fully differential sinusoidal input signal (i.e., the IF signal) will be off-chip bandpass filtered before entering into the modulator. The digital output will be acquired with a test board, and the acquired data stream will then be transferred to a workstation for spectral analysis. The clock for the modulator will be generated from a off-chip RF pulse generator and brought onto chip through a bondpad and then amplified to a 2.5 V rail-to-rail swing. Although there are bandgap references available on-chip, a clean off-chip voltage reference will be used for the modulator measurement, in order to diminish the effect of distortion due to an unclean reference [22].

Table 6.1: Comparison of simulated performance.

Ref.	[7]	[14]	This work
Standards	GSM DECT	GSM WCDMA	GSM WCDMA/DECT
Receiver topology	Wideband IF double-conversion	Digital high IF	Digital high IF
OSR values	128(GSM) 32(DECT)	192(GSM) 24(WCDMA)	192(GSM) 24(WCDMA) 64(DECT)
Dynamic range	96 dB(GSM) 82 dB(DECT)	86 dB(GSM) 54 dB(WCDMA)	90 dB(GSM) 70 dB(WCDMA) 76 dB(DECT)
SNR	92 dB(GSM) 76 dB(DECT)	76 dB(GSM) 53 dB(WCDMA)	83 dB(GSM) 57 dB(WCDMA) 67 dB(DECT)
SNDR	90 dB(GSM) 75 dB(DECT)	72 dB(GSM) 52 dB(WCDMA)	80 dB(GSM) 55 dB(WCDMA) 65 dB(DECT)
IP3	-26 dBV(GSM) -12 dBV(DECT)	-26 dBV(GSM) -18 dBV(WCDMA)	-28 dBV(GSM) -19.4 dBV(WCDMA) -17 dBV(DECT)
Modulator topology	MASH 2-2	CIFF $3_{rd} - order$	CIFB $3_{rd} - order$
Capacitance	14.4 pF	5.41 pF	6.24 pF
Cap. spread	64:1	48:1	24:1
Power consumption	65 mW (total)	11.5 mW(GSM) 13.5 mW(GSM)	13 mW(GSM) 14.8 mW(WCDMA) 19.1 mW(DECT)
$V_{Reference}$	1.5 V	1.25 V	1.25 V
V_{Supply}	3.3 V	2.5 V	2.5 V
Process	0.35-μm CMOS DP, 5M	0.25-μm CMOS DP, 5M	0.35-μm CMOS DP, 5M
Active area	$1.5mm^2$	$0.36mm^2$	$0.5mm^2$

CHAPTER 7. CONCLUSIONS

This thesis described the design of a Delta-Sigma ($\Delta\Sigma$) modulator for a multi-standard RF receiver. The designed modulator is part of a monolithic CMOS receiver for cellular GSM/WCDMA, and cordless DECT standards. An overview of existing receiver systems was given in Chapter 2. The fundamentals of $\Delta\Sigma$ modulators were explained in Chapter 3. System-level architecture design of the proposed third-order SCIFB modulator was presented in Chapter 4, and the circuit-level design of building blocks was explained in Chapter 5. Chapter 6 summarized the post-layout simulated performance of the $\Delta\Sigma$ modulator.

The prime purpose of this thesis is to design a $\Delta\Sigma$ modulator for multi-standard RF receptions. The feasibility of high-frequency IF signal digitization by using a single $\Delta\Sigma$ modulator is demonstrated. The suggestions for future work are as follows: (1) The interaction between IF filter and the baseband ADC needs to be investigated to a more exhaustive extent, since the dynamic range requirements of the ADC will be relaxed in the presence of a high-attenuation IF bandpass filter; (2) Since high dynamic range cascaded $\Delta\Sigma$ modulators suit for wideband baseband applications, but at the same time, consume more power and area than single-loop modulators do, efforts are needed to find the optimum balancing point, both on system and on circuit level; (3) The design of the automatic gain controller (AGC) may be associated with that of the $\Delta\Sigma$ modulators for the sake of high integration, since they both have similar DR and linearity requirements.

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