

AN ABSTRACT OF THE THESIS OF

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A fully integrated CMOS latched comparator is presented for use as a wake-up circuit that is attached to an RF energy harvester in a battery free wireless sensor network. The system consumes less than 36nA static current at 20°C and dissipates 2pJ of energy per conversion. The comparator comprises of a series of level-shifting leakage-mode inverters. Its latching behavior is obtained by supplying the power to each stage from the inverted output of the last stage via a resistor-string voltage divider. This 45nW circuit is the solution with the lowest static power consumption proposed to date for synchronizing nodes in a sensor network.

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A Nano-Power Wake-Up Circuit for RF Energy Harvesting Wireless Sensor Networks

by

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Christopher J. Lindsley, Author

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The notion to become an engineer entered my head when I was in third grade. My teacher, Mr. Paul Bradley, introduced me to the simple machines and the strength of the triangle. He started me on the path to become an engineer.

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A Nano-Power Wake-Up Circuit for RF Energy Harvesting Wireless Sensor Networks

1. INTRODUCTION

Battery-free wireless sensor networks offer a highly flexible and low-cost method to monitor environmental conditions with minimal human interference [1]. Early generation wireless sensor networks operated with relatively high power, necessitating the use of batteries [2]. Periodic replacement of the batteries adds maintenance that becomes difficult if the sensor network is deployed in hard to access areas. Recent developments in powering wireless sensors have made it possible to harvest power from a remote source [3]. However, the power available in the environment, either ambient power or power delivered from an RF source, is not enough to power the sensor continuously. To reduce the power consumption, the sensor can enter a sleep mode. A wake-up circuit then activates the sensor and returns it to normal operation.

State-of-the-art sensors with wireless communication consume significantly more power than is typically available in the environment. There are two methods to address this problem and allow wireless sensors to operate without a battery: decrease the power consumed by the sensors and increase the available power. Radiating power from a central hub at radio frequencies is one way to power the sensor nodes. However, there is a legal limit to the amount of power that can be transmitted wirelessly, physical limits to the efficiency of transmission, and technological limits to how much can be scavenged. The FCC limit for the maximum peak continuous output power of an intentional radiator is 1W, (30dBm) [4]. Physical laws limit the amount of power that one antenna can radiate to another for a given distance and frequency. Free-space path loss (FSPL), Eq. (1), is the loss of signal strength in a line-of-sight configuration between two antennas [5],

$$FSPL = \left(\frac{4\pi df}{c} \right)^2 \quad (1)$$

where d is the distance in meters, f is the frequency in Hertz, and c is the speed of light. A simplified version where the physical constants are embedded is:

$$\begin{aligned}
10 \log_{10} FSPL &= 10 \log_{10} \left(\frac{4\pi d(f \times 10^6)}{c} \right)^2 \\
FSPL(dB) &= 20 \log_{10} \left(\frac{4\pi d(f \times 10^6)}{c} \right) \\
&= 20 \log_{10}(d) + 20 \log_{10}(f) + 20 \log_{10} \left(\frac{4\pi \times 10^6}{2.998 \times 10^8} \right) \\
&= 20 \log_{10}(d) + 20 \log_{10}(f) - 27.552 \text{dB}
\end{aligned} \tag{2}$$

where f is the frequency in MHz, d is the distance in meters, and the $FSPL$ is in decibels. For a fixed distance and frequency, the $FSPL$ limits RF power reception.

The final limitation on scavenging power is the state of the technology of RF energy harvesters. An RF energy harvester with a peak efficiency of 15.43% can be constructed using off-the-shelf components [6]. A custom, fully integrated, RF-harvester using a full-wave floating-gate rectifier is presented in [7] with a peak efficiency of 60.0%, which corresponds to a loss of 2.218dB.

With a harvester efficiency of 60.0%, Eq. (3) shows that the maximum power that can be harvested from a 1W, 900MHz, isotropic radiator from an identical antenna 10 meters away cannot exceed 4.22μW.

$$\begin{aligned}
P_{harvest} &= 30\text{dBm} - [20 \log(10) + 20 \log(900) - 27.552 + 2.218]\text{dBm} \\
&= -23.751\text{dBm} = 4.22\mu\text{W}
\end{aligned} \tag{3}$$

This is the maximum continuous power available for a battery-free wireless sensor under these conditions, and it is significantly less than the power required to operate the most efficient receivers and transmitters reported to date. Table 1 reports the power requirement of recent wireless sensor network receivers and transmitters.

Table 1 – Performance of wireless sensor network receivers and transmitters.

	Otis 2005 [8]	Cook 2006[9]	Panitantum 2008 [10]	Ayers 2008 [11]
RX Power (μW)	400	300	–	244
TX Power (μW)	1600	700	1940	–
Frequency (MHz)	1900	2400	900	900
Modulation	OOK	BFSK	BFSK	BFSK

For an RF-harvester to power a wireless sensor's receiver and transmitter, it must harvest and store energy over a long period for the sensor to sense and communicate over a shorter period. During the storage time, the only operable part of the sensor is the circuit that wakes up the sensor when it is time to sense and communicate. Therefore, it is a requirement of the system that the wake-up method use an insignificant portion of the harvested power.

Because the wake-up circuit must operate at all times while the sensor is asleep, its power consumption directly reduces the power available for storage from the harvester. Consequently, increasing the power consumption of the wake-up circuit increases the time required to store enough energy to power the sensor. Mathematically, this is expressed in Eq. (4).

$$\begin{aligned} E_{req} &= P_{store} \times t_{sleep} \\ &= (P_{harvest} - P_{wake-up}) \times t_{sleep} \end{aligned} \quad (4)$$

where E_{req} is the minimum energy required for the sensor to complete one sensing and communicating cycle, P_{store} is the storage power, t_{sleep} is the time the sensor is asleep, $P_{harvest}$ is the harvested power, and $P_{wake-up}$ is the power consumption of the wake-up circuit. Eq. (4) shows that the power consumption of the wake-up circuit directly affects the overall system performance. Specifically, decreasing $P_{wake-up}$ decreases t_{sleep} and increases the number of times the sensor can sense and communicate per day.

Regardless of what type of circuit activates the sensor, it is equally important that the sensor activate at a known time with a fine resolution. If sensors in a network are not synchronized, and activate at random or unpredictable times, the sensor must power its RF receiver for a longer period. Figure 1.1 illustrates a theoretical situation where a sensor is activated using a 10kHz interrupt timer. The length of time that the receiver must be active is increased by a non-ideal clock. The receiver must turn on early and stay on later to ensure it does not miss the message due to the large coarse resolution of the non-ideal clock.

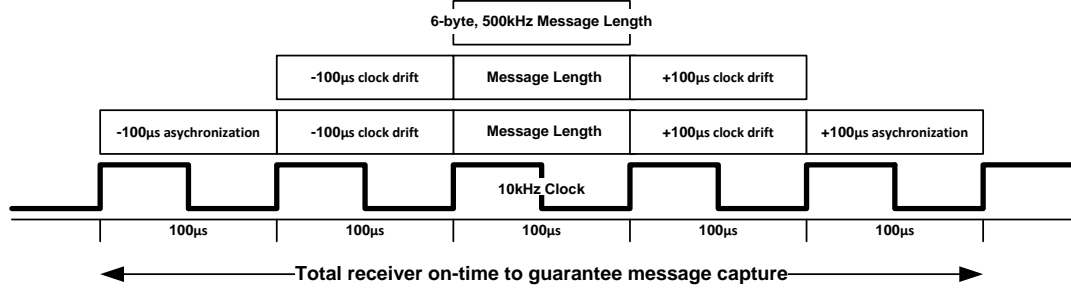


Figure 1.1 – Total receiver on-time for a theoretical system with single-period clock drift and a maximum possible 100μs asynchronization time.

With an ideal clock, the receiver could turn on the instant before the transmitter sends the message. Clock drift error is defined as the error introduced by non-ideal set-up and hold times, requiring the receiver to turn on the clock one cycle prior to the arrival of a message. The magnitude of the error due to clock drift is lessened by a faster clock with a shorter period. However, a faster clock consumes more power. If the clock shown above is an ideal clock that is only consuming power to charge and discharge a capacitor, the minimum dynamic power of the clock is [12]

$$P_{clock} = \frac{fCV_{DD}^2}{2} \quad (5)$$

where V_{DD} is the supply voltage, f is the frequency, and C is the load capacitance. For example, an ideal clock with a 1.25V supply, a frequency of 10kHz (100μs resolution), and a load capacitance of 10pF consumes a minimum power of 125nW. In a recent wireless sensor network [13], the interrupt timer alone consumed 5.68μW. In addition to the interrupt clock, the sensor also needs a programmable sleep period and an event handler, both of which consume additional power.

Asynchronization error is defined as the error introduced by clocks with non-ideal frequencies. Over time, the transmitter and receiver clocks can become asynchronous. The magnitude of this error is system dependent and could be greater than the single-period asynchronization shown in Figure 1.1.

In a battery powered system, a globally broadcast RF clock can be used to keep the transmitter and receiver's clocks synchronous [14], but this can use approximately 10μW of power using a rudimentary low power RF receiver. This approach requires

that a simple RF receiver stays on at all times to receive the timestamp information from a central hub and then synchronize its internal clock to the source.

There is then a design trade-off between wasting power on increased clock precision or wasting power on activating the RF receiver early. Furthermore, in each of the cases described above, the wake-up method consumes dynamic power. The circuit presented in this thesis utilizes a RF energy harvesting topology to achieve wake-up resolution analogous to a 125kHz clock, but uses tens of nano-watts of static leakage power and near-zero dynamic power. This is several orders of magnitude less than any other reported method.

This thesis is organized as follows. Chapter 2 describes the system design including system restrictions and external interfaces. Chapter 3 covers the proposed topology and circuit design. Chapter 4 describes the test setup and the measured results. Chapter 5 concludes this thesis.

2. SYSTEM DESIGN

2.1. System Overview

The wake-up circuit described in this thesis utilizes RF energy harvesting technology to synchronize the sensors in a network by monitoring the rectified RF power source and waking the sensor when the RF power source turns off. While the central hub is radiating power to the sensors, shown in Figure 2.1, the radiated RF power disrupts all sensor-to-sensor and sensor-to-hub communications.

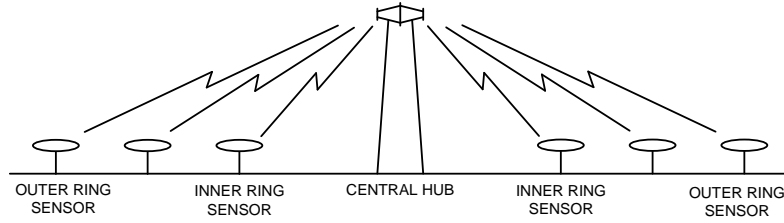


Figure 2.1 – RF power broadcast for a three-ring network.

Because the central RF power source must cease broadcasting to allow the sensors to communicate, it is convenient to wake up the sensors when the RF power source turns off. Figure 2.2 is a timing diagram of the transmitter and receiver schedule for a theoretical three-ring wireless sensor network.

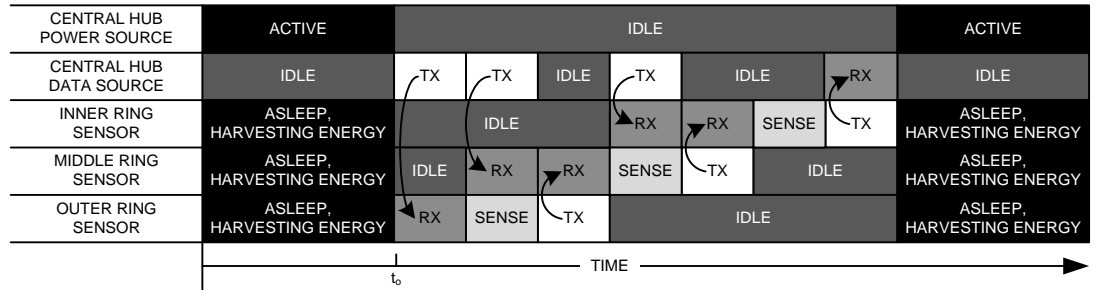


Figure 2.2 – Transmitter and receiver operation schedule for a three-ring network assuming each sensor does a complete receive-sense-transmit cycle.

While the RF power source is active, all the sensors are asleep and harvesting energy. At time t_0 , the RF power source ceases broadcasting and the sensors execute their default command. Sensors in the outer ring will have previously been programmed to initialize their receivers at time t_0 . Sensors in the middle and inner rings enter an idle state while their internal clocks delay the initialization of their

receivers for a pre-programmed amount of time. The actions for the sensors in each ring of the wireless sensor network execute in the same order following the initial delay. First, the sensor receives data from the central hub. Second, the sensor receives data from a sensor further from the central hub if there is one. Third, the sensor senses and processes its data. Fourth, the sensor transmits its data to a sensor closer to the central hub or to the central hub itself. Fifth, the sensor enters a low-power mode. Finally, the sensor goes to sleep and resumes harvesting power when the central RF power source resumes broadcasting.

In addition to the power savings discussed earlier, waking up when the RF power source turns off is a de facto global clock synchronization signal. The loss of RF power is a global event experienced by all the sensors in the network at the same time. This gives all the benefits of the globally distributed clock discussed in the previous section without an active receiver. Additionally, synchronizing the nodes with the RF power source eliminates the problem of clock drift.

2.2. System Constraints

Figure 2.3 illustrates the functional blocks that interface to the wake-up circuit. The multistage rectifier converts the RF energy into DC energy stored on a large, low-leakage capacitor. The rectified voltage can be as high as 12V. The regulator converts the rectified voltage into a 1.25V supply voltage for powering the circuits. The wake-up circuit drives a switch that controls the power for a finite state machine (FSM). The FSM in turn controls the reset signal for the wake-up circuit. The FSM also interfaces with the on-chip sensor, receiver (RX), and transmitter (TX).

For the whole system to operate at peak efficiency, each sensor must wake up at a programmable time with strict timing requirements. The wake-up circuit presented here synchronizes the actions of wireless nodes with a central hub. If there are inconsistencies in the propagation delay, the window allocated for specific operations must be widened. The propagation delay, t_p , for the circuit shown in Figure 2.3 is defined as the time from the falling edge of V_{IN} to the rising edge of V_{OUT} .

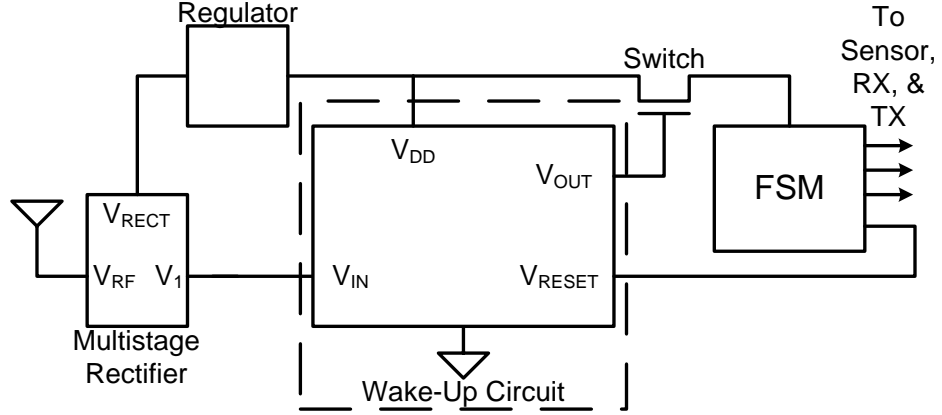


Figure 2.3 – Wake-up circuit's interface to other on-chip functional blocks.

The absolute value of propagation delay across this circuit is not as important as the consistency of that delay for each value of V_{IN} . Once a sensor is placed at a static location a constant distance from an RF power source broadcasting at a constant frequency, then from Eq. (2) the free-space path loss (FSPL) will be constant. Therefore, if the RF power source is broadcasting at a constant power level, the RF energy harvester will receive a constant input power and the DC value of V_{IN} at that location will remain constant.

Once the sensor has completed all sensing and communication and is ready to sleep, the FSM sends the wake-up circuit a reset signal. If the RF power source is broadcasting, the sensor goes to sleep and the RF-harvester resumes harvesting power.

2.3. Electrical Constraints

The wake-up circuit monitors the RF power signal by tapping onto the output of the first stage, V_1 , of a multistage rectifier shown in Figure 2.4. Connecting the wake-up circuit to any stage marginally adds an additional load to the rectifier. The capacitive loading of a single gate is insignificant compared to the $C_{2,n}$ capacitors in Figure 2.4. More significantly, resistive loading occurs due to gate leakage currents flowing from the gate to the substrate. Gate leakage occurs when a voltage potential is applied across the gate-substrate terminals. The magnitude of the leakage current increases as the gate-substrate voltage increases [15]. Connecting the wake-up circuit to the lowest potential node reduces the gate leakage and reduces the resistive loading of the rectifier.

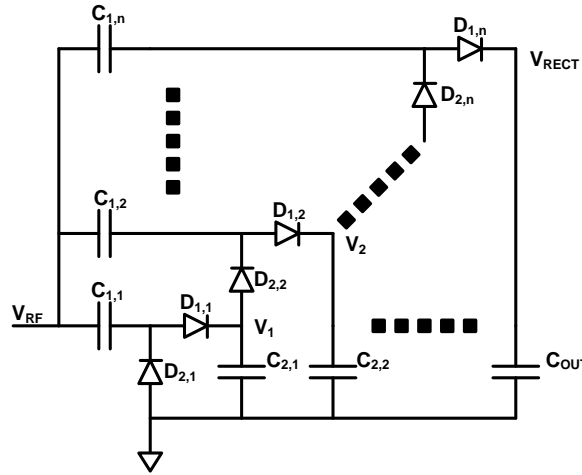


Figure 2.4 – Architecture of a multistage RF rectifier [7].

The system design is further constrained by the supply voltage provided by the regulator shown in Figure 2.3. The harvester/regulator circuit described in the previous section supplies a regulated voltage of 1.25V [16].

Due to FSPL, the amplitude of V_{RF} and subsequently the DC value of V_{RECT} are proportional to the square root of the distance to the RF power source for far-field distances, Eq. (1). For a sensor with a 36-stage RF energy harvester, the output of the first stage, V_1 , will be $1/36^{\text{th}}$ of the rectified voltage. A sensor placed 15 meters away from the RF power source will have a V_{RECT} of $\sim 2.1\text{V}$. For a sensor at 1 meter, V_{RECT} will be $\sim 9\text{V}$ [16]. Therefore, the DC values of V_{IN} for the wake-up circuit will lie in the range of 58mV to 250mV.

The output of the wake-up circuit, V_{OUT} , must drive a CMOS pass-gate switch that supplies power to the FSM. To reduce the on resistance of the switch, V_{OUT} should be the highest obtainable voltage available that will not damage the switch. This design uses the output of the regulator to drive the switch.

2.4. Standard Comparator

The standard way to trigger a logical ‘1’ output from a known analog signal is to use a comparator with a reference voltage [17]. Figure 2.5 shows three low-power CMOS comparators with cross-coupled input devices.

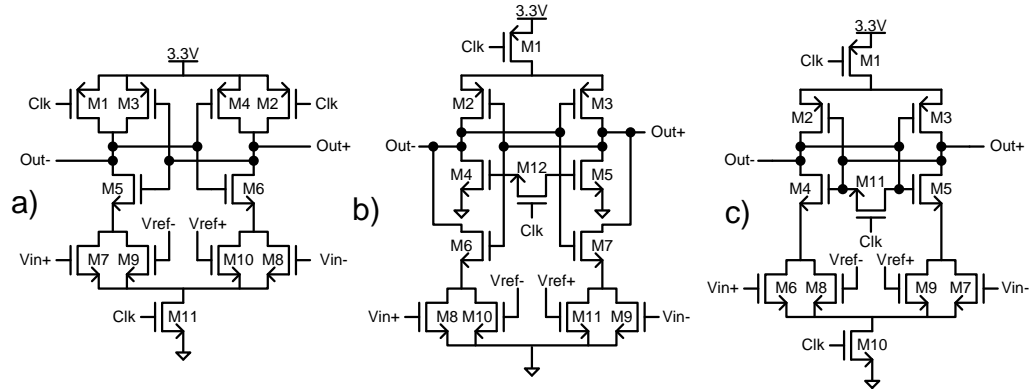


Figure 2.5 – Alternative comparator topologies. a) Low power differential current. b) Resistive divider. c) Charge sharing [18].

Table 2 summarizes the performance of the latching comparators shown in Figure 2.5. Each topology consumes orders of magnitude more power than is available to the wake-up circuit. Additionally, the input offset voltage, V_{OS} , is within an order of magnitude of the minimum value of V_{IN} . With an offset voltage of this magnitude, these comparators could never reliably monitor the RF power source.

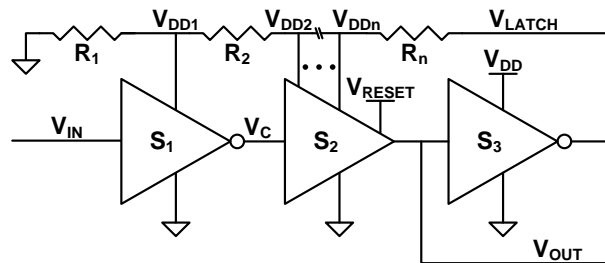
Table 2 – Performance of latched comparators [18].

Type	Power [μ W]	V_{OS} [mV]
Low power differential current	138.15	164
Resistive divider	114.02	31.9
Charge Sharing	88.19	32.1

In addition to the power consumption outlined in Table 2, more power will be consumed in generating the required reference voltage. A low-power reference voltage is presented in [19] that features MOSFETs operating in the subthreshold region. Simulation results for this reference voltage show the power consumption to be $1.84\mu\text{W}$ at room temperature. Another low-power reference voltage is presented in [20] that is fabricated in a $1.2\mu\text{m}$ CMOS process. The measured power consumption for this reference is $4.32\mu\text{W}$ at room temperature.

A new topology for a wake-up circuit that operates as a latched comparator but consumes orders of magnitude less power and has orders of magnitude lower offset voltage is presented in this thesis. The current consumed by the new latched comparator never exceeds off-state leakage currents, and the offset voltage is determined by the inherent characteristics of MOS devices operating in the deep-subthreshold region.

The second stage includes an even number of inverters and serves two purposes. First, toggling V_{RESET} resets the entire circuit to a known state. Second, S_2 level-shifts the logical-high voltage from the low voltage sourced by S_1 to a greater voltage required for the output, V_{OUT} , as described in Section 2.3. Of the even number of inverters in S_2 , all but the last inverter are powered by the intermediate voltages in a voltage divider. The last inverter in the second stage, the reset inverter, is directly powered by V_{RESET} .



The third stage, S_3 , provides the latching behavior of the circuit. As long as the circuit's output voltage is low, S_3 sources power to the previous stages $V_{DD1}, V_{DD2}, \dots, V_{DDn}$ via a voltage dividing string of resistors. When V_{IN} decreases to a voltage less than the internal reference voltage of S_1 , the odd number of intermediate inverters (S_1 and the even number of inverters in S_2) causes V_{OUT} to increase to a logical high voltage. A high voltage at V_{OUT} causes V_{LATCH} to decrease to a logical

low voltage of zero volts, whereby $V_{DD1}, V_{DD2}, \dots, V_{DDn}$ are zero volts. Thus the supply voltage for all inverters is zero except for the reset inverter. The circuit stays in this state, and does not respond to V_{IN} , until V_{RESET} toggles and V_{IN} is high.

With an overview of the circuit provided, the following sections describe the subcircuits in more detail. Sections 3.2 and 3.3 describe the design and operation of the input comparator stage. Sections 3.4 and 3.5 describe the process for choosing the number of inverters to use in the second stage, S_2 . Section 3.6 covers the design of the third stage and the behavior of the latch.

3.2. Topology Design of the First Stage

For a sensor at the maximum operable distance from the central hub (10-15m), a recognizable logical ‘high’ value of V_{IN} can be as low as 58mV, $V_{IH,min}$, and as high as 250mV, $V_{IH,max}$. The logical ‘low’ value, V_{IL} , will always be within a few microvolts of ground. The comparator stage of the wake-up circuit must discern between these two states without wasting current on a PTAT-generated reference voltage and output a voltage large enough to surpass the switching voltage of the first inverter in S_2 , shown in Figure 3.1.

A traditional way to amplify a voltage is to use a common-source amplifier, as shown in Figure 3.2(a). The current through such a branch can be greatly reduced by replacing the load resistor, ‘R’, with a current limiting active load. The active load shown in Figure 3.2(b) is an off-state NMOS device. In Figure 3.2(c), the NMOS devices have been changed to PMOS devices because the charge carriers in PMOS devices have a lower mobility than in NMOS devices [21], reducing the leakage current and power consumption.

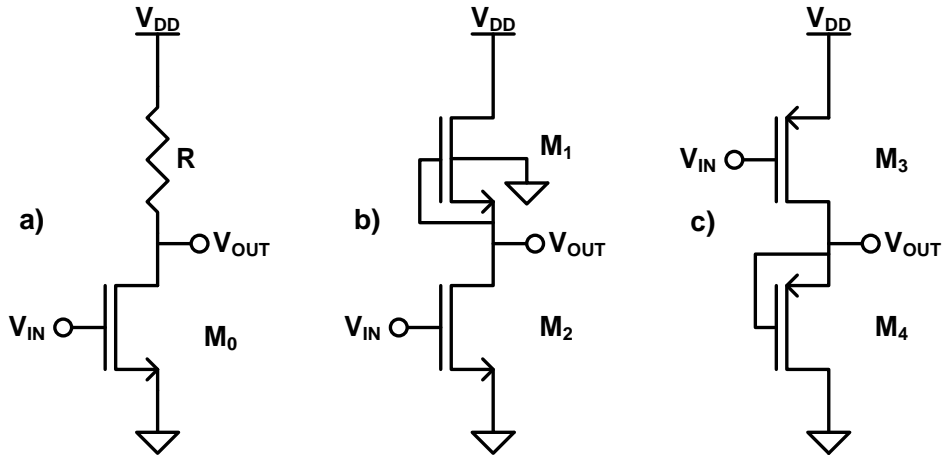


Figure 3.2 – Common source amplifiers with a) resistive load, b) off-state NMOS active load, c) off-state PMOS active load.

The topologies shown in Figure 3.2 use a built-in switching voltage as the reference voltage. The output of the circuits shown in Figure 3.2 switch from rail-to-rail as the input passes the switching voltage, which is set by the physical parameters of the devices and the supply voltage, V_{DD} .

Previously, comparators have been presented that use the inherent properties of MOS devices instead of a reference voltage [22]. These comparators use the difference between the threshold voltage of NMOS devices and the threshold voltage of a PMOS device to generate a stable reference. However, by operating near the threshold voltage of the MOS devices, the topology in [22] sinks milliamperes of current. The topology of Figure 3.2(c) uses the high resistance of M_4 to limit the current in the branch to tens of picoamperes.

3.3. Device Sizing in the First Stage

The sizes of the devices and the supply voltage of the first stage determine the switching-voltage-generated reference voltage for the first stage. The absolute value of the switching is not as important as the range in which it lies. In this application, the switching voltage must be greater than zero and less than 58mV. A switching voltage of 30mV should reduce the possibility of the first stage not switching due to process variations. The first stage can fail if V_{IN} is greater than 58mV and the output remains near V_{DD1} or if V_{IN} is less than or equal to zero and the output remains near ground.

Figure 3.3 illustrates the DC operating point when V_{OUT} and V_{IN} are held at the desired switching voltage, $V_{OUT} = V_{IN} = V_{SW}$. To determine the device sizes that yield a switching voltage of $\sim 30\text{mV}$, I_{M1} is set equal to I_{M0} and one solves for the device sizes for a given V_{DD} .

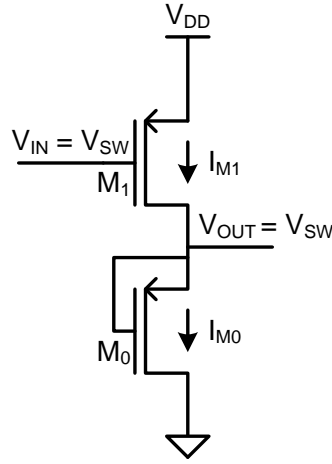


Figure 3.3 – DC operating point when the input and output voltages are at the switching voltage.

The basic equation for modeling the drain current of a device operating in the subthreshold region ($|V_{GS}| < V_T$) is shown in Eq. (6) [23], [24], assuming that $V_{BS} = 0$, $V_{DS} \gtrsim 2v_{th}$, and the channel length is sufficiently long,

$$I_D = \mu_0 C_{ox} S_M \cdot (n - 1) \cdot v_{th}^2 \cdot e^{\frac{(|V_{GS}| - |V_T|)}{n \cdot v_{th}}} \quad (6)$$

$$n = 1 + \frac{\sqrt{q N_b \epsilon_{si}}}{C_{ox} \sqrt{2\psi_s}} \cong 1 + \frac{C_d}{C_{ox}}$$

where S_M is the W/L of the device; n is the subthreshold slope factor; v_{th} is the thermal voltage, kT/q ; q is the unit charge of an electron; N_b is the doping concentration of the substrate; ϵ_{si} is the permittivity of silicon; C_{ox} is the oxide capacitance per unit area; ψ_s is the surface potential; and C_d is the depletion capacitance per unit area.

Eq. (6) shows that the drain current has no dependence on V_{DS} as long as $V_{DS} > 2v_{th}$. Since $V_{GS} = 0$ for M_0 , I_{M0} will only depend upon V_T and the device sizes. The drain current of the input device, I_{M1} , varies exponentially with its gate-source voltage. Setting the drain currents equal to each other yields Eq. (7).

$$I_{M0} = I_{M1}$$

$$\mu_o C_{ox} S_{M0} (n-1) v_{th}^2 e^{\frac{-|V_T|}{n \cdot v_{th}}} = \mu_o C_{ox} S_{M1} (n-1) v_{th}^2 e^{\frac{(V_{DD} - V_{SW} - |V_T|)}{n \cdot v_{th}}} \quad (7)$$

or,

$$S_{M0} e^{\frac{-|V_T|}{n \cdot v_{th}}} = S_{M1} e^{\frac{(V_{DD} - V_{SW} - |V_T|)}{n \cdot v_{th}}} \quad (8)$$

For a given supply voltage, Eq. (9) relates S_{M0} to S_{M1} and a switching voltage. Let $R_M = S_{M0}/S_{M1}$ then

$$R_M = e^{\frac{(V_{DD} - V_{SW})}{n \cdot v_{th}}} \quad (9)$$

The subthreshold slope is a constant in any process. For first-order calculation it can be assumed that operating in the subthreshold region $C_d/C_{ox} \cong 1$ and $n \cong 2$ [24]. For an input voltage of $V_{SW} = 30mV$ and a thermal voltage of $v_{th} \cong 25mV$ at $T = 300K$, Eq. (9) yields Eq. (10).

$$R_M = e^{\frac{(V_{DD} - 30mV)}{50mV}} \quad (10)$$

Figure 3.4 plots Eq. (10) for values of $0 < V_{DD} < 400mV$. As the supply voltage increases, the W/L ratio of the off-state device, M_0 , must increase exponentially to keep the switching voltage at 30mV. Eq. (10) indicates that the circuit in Figure 3.3 could operate from a 1.25V supply voltage, but this would require that M_0 is two million times larger than M_1 . Limiting $R_M < 1000$, yields a range of possible values for $V_{DD} < 375mV$ and their corresponding R_M values. Figure 3.5

shows the simulated voltage transfer characteristics of the circuit with, $R_M = 80$ and $V_{DD} = 250\text{mV}$. The switching voltage is $\sim 40\text{mV}$. The small inconsistency between the simulated value and the calculated value is due to the inaccuracies of the subthreshold equation when $V_{DS} < 2v_{th}$.

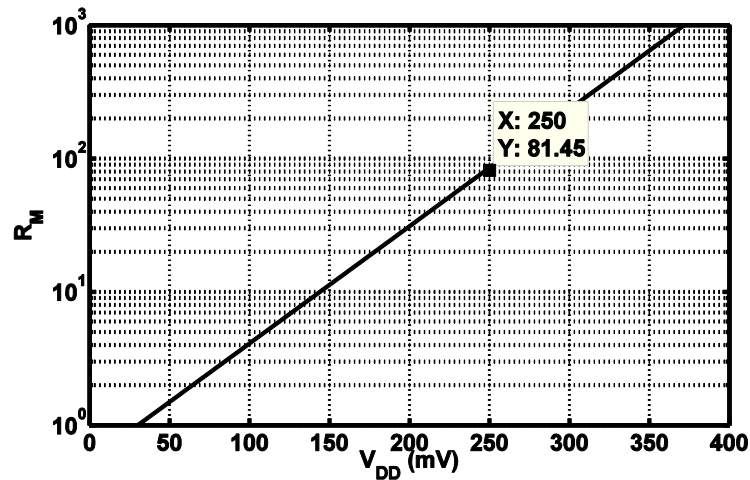


Figure 3.4 – Ratio of the active and load device sizes vs. V_{DD} for a switching voltage of 30mV.

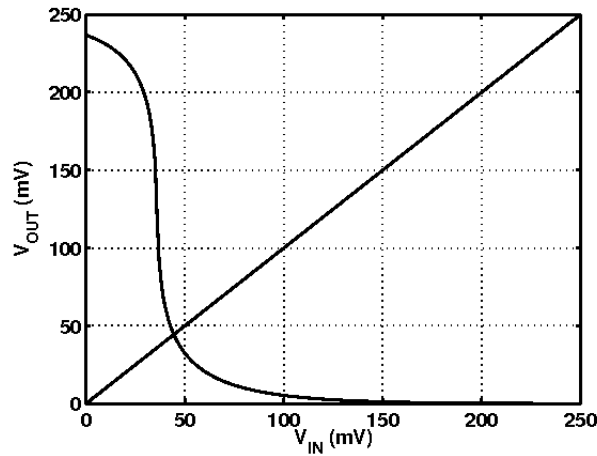


Figure 3.5 – Simulated voltage transfer characteristic for the single-stage common source amplifier.

3.4. Two-Inverter Level-Shifting Buffer

In order to satisfy the electrical constraints, a level-shifting multi-inverter stage, S_2 , buffers the low voltage output, S_1 . The output of this stage, V_{OUT} , is then large enough to turn off the top device in S_3 . The second stage must have an even number of inverters to retain the inverting behavior from V_{IN} to V_{OUT} . Figure 3.6 shows a two-inverter topology. This section will show that a two-inverter level-shifting buffer can be designed with ideal devices and resistors, but a more robust design is needed to account for process variations.

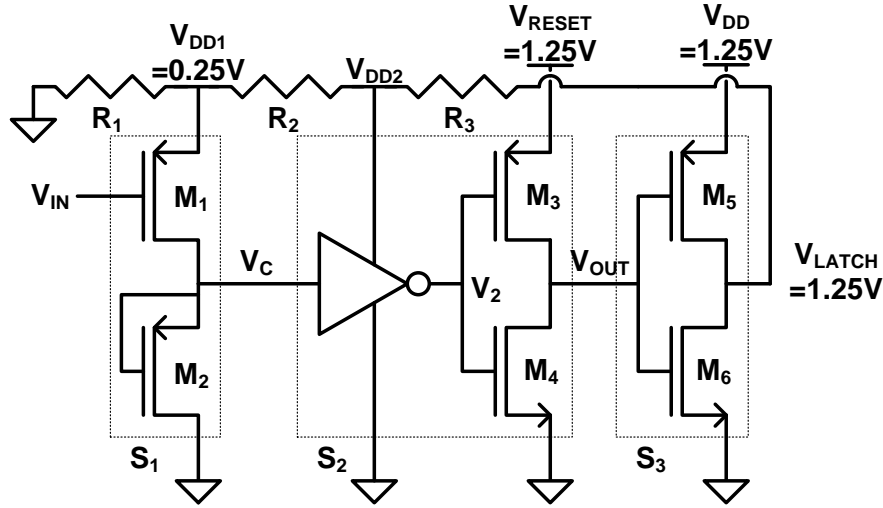


Figure 3.6 – Two inverter topology for the non-inverting level-shifting stage, S_2 .

The topology used for S_1 cannot be used for S_3 because S_3 operates well outside the subthreshold region. To operate from a 1.25V supply voltage, S_3 and the final inverter of S_2 are standard CMOS inverters. The initial inverter of S_2 must have a switching voltage less than 400mV (if $R_M < 10^3$) and a large enough output voltage to turn off M_3 ,

$$V_2 > (1250\text{mV} - |V_T|_{\min}) \quad (11)$$

where V_T is approximately 430mV but can be as low as 300mV. In the ideal case where S_2 is capable of driving its output from rail-to-rail, Eq. (11) states that V_{DD2} must be at least 950mV. However, in practice V_2 is less than V_{DD2} due to losses in the top device in the first inverter in S_2 , leading to a minimum V_{DD2} of ~1000mV. If the first inverter in S_2 had a ~1000mV supply voltage, and a maximum input voltage of

400mV, then it would need to have a switching voltage that is less than 40% of its supply voltage. This is possible, using a standard CMOS inverter, but attention must be paid to the resistor string that divides and creates the supply voltages.

The resistor string must have a total resistance of approximately $100\text{M}\Omega$ to limit the current through the string to approximately one hundred times greater than the leakage through the inverters, $\sim 10\text{nA}$. Poly resistors could be used to create the resistor string, but at $235\Omega/\square$, the resistors would have to have a size ratio of 425,000:1.

Off-state PMOS transistors can be used as resistors due to their large DC resistance, such as M_2 in Figure 3.6, but their actual resistance can vary by $\pm 10\%$ or more due to mismatch, process, and V_T variations. The ideal resistance ratios are shown in Eq. (12).

$$V_{DD2} = 1000\text{mV} = 1250\text{mV} \cdot \left(\frac{R_1 + R_2}{R_1 + R_2 + R_3} \right) \quad (12)$$

$$R_1 + R_2 = 4R, \quad R_3 = R$$

However, to ensure that Eq. (11) is always satisfied in all cases, the following equation yields the upper and lower bounds for V_{DD2} given a percentage variation in resistance, x . The worst-case scenario is defined as the case in which R_1 and R_2 are altered by $\pm 10\%$ and R_3 is altered by $\mp 10\%$.

$$V_{DD2} = 1250\text{mV} \cdot \left(\frac{(1 \pm x) \cdot (R_1 + R_2)}{(1 \pm x) \cdot (R_1 + R_2) + (1 \mp x) \cdot R_3} \right) \quad (13)$$

$$R_1 + R_2 = 4R \cdot (1 \pm x), \quad R_3 = R \cdot (1 \mp x)$$

Using the resistances in Eq. (13) for $x = 10\%$, the range of V_{DD2} becomes

$$957\text{mV} < V_{DD2} < 1037\text{mV} \quad (14)$$

However, the lower bound in Eq. (14) violates the condition set in Eq. (11) that V_{DD2} must be greater than 1000mV in all cases. Increasing the target V_{DD2} in Eq. (12) yields values of resistances that comply with the condition set in Eq. (11). After an iterative process, it was found that setting $V_{DD2} = 1037\text{mV}$ in the nominal case, sets $V_{DD2,min}$ to 1000mV, as shown in Eqs. (15) – (17).

$$V_{DD2} = 1037mV = 1250mV \cdot \left(\frac{R_1 + R_2}{R_1 + R_2 + R_3} \right) \quad (15)$$

$$R_1 + R_2 = 22R, \quad R_3 = 9R$$

$$V_{DD2} = 1250mV \cdot \left(\frac{(1 \pm x) \cdot (R_1 + R_2)}{(1 \pm x) \cdot (R_1 + R_2) + (1 \mp x) \cdot R_3} \right) \quad (16)$$

$$R_1 + R_2 = 22R \cdot (1 \pm x), \quad R_3 = 7R \cdot (1 \mp x)$$

$$1000mV < V_{DD2} < 1070mV \quad (17)$$

Since S_2 must operate from a supply voltage that is greater than $2V_T$, V_1 must swing to at least within a V_T of V_{DD2} in order to shut off the top device in S_2 , as shown in Eq. (18).

$$V_{DD1} > V_1 > (1070mV - |V_T|_{min}) \quad (18)$$

However, Eq. (10) and the design limit on the size of the devices in S_1 , set an upper limit on the range of V_{DD1} .

$$V_{DD1} < 375mV \quad (19)$$

The condition in Eq. (18) cannot be met with a supply voltage for S_1 set at 375mV. Furthermore, the reset inverter in S_2 cannot use the same topology as S_1 , because its devices operate outside the subthreshold region.

The concerns described in this section rule out the possibility of using a two-inverter level-shifting buffer for the second stage shown in Figure 3.1. The variability of off-state MOS resistors lead to excessive variations in V_{DD1} and V_{DD2} . At the extremes of variations in the resistor string, the lower boundary of V_{DD2} violates Eq. (11), and the upper boundary of V_{DD1} violates Eq. (19), motivating the decision to use a four-inverter level-shifting buffer.

3.5. Four-Inverter Level-Shifting Buffer

The cascaded two-inverter level-shifting buffer described in the previous section could not reliably amplify the input signal. Reliable up-translation of the 58mV input signal requires additional inverters. Each stage shown in Figure 3.7 increases the digital high voltage of the following stage by 250mV. Limiting the step between any two stages to less than a $|V_T|_{min}$ ensures that each inverter is capable of turning off the next inverter.

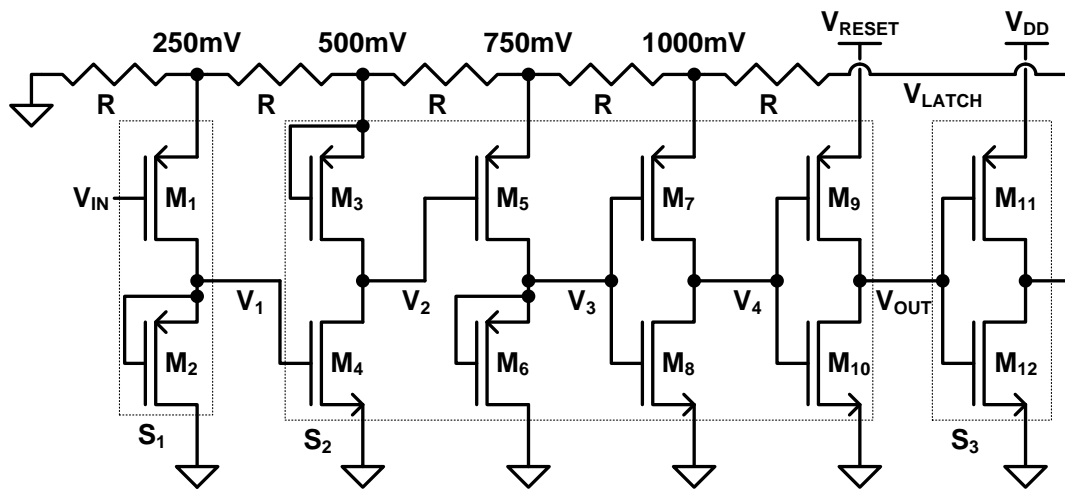


Figure 3.7 – Four inverter topology for the non-inverting level-shifting stage, S_2 .

In the first three inverters, the supply voltage is less than $2 \cdot |V_T|_{min}$, allowing use of the topology described in Section 3.2. The last three inverters in Figure 3.7 are traditional CMOS inverters. As nodes V_3 , V_4 , and V_{OUT} increase or decrease past the switching voltage for the next stage, the node voltage will pass a point at which both devices in the inverter have $|V_{GS}| > |V_T|_{min}$. The devices in the last three inverters have increased lengths, reducing the drive strength of the device when V_3 , V_4 , and V_{OUT} are approximately equal to their respective V_{SW} , reducing the energy consumed per switching event of each inverter.

3.6. Latch Design

The discussion so far has been only on the comparator and voltage translator. The other part of the circuit is its latching method. A latch is a system with two possible stable states that can be used to store information [25]. In this case, the two stable states are ‘Output High’ and ‘Output Low.’ The truth table for the wake-up latch in Figure 3.7 is shown in Table 3.

Table 3 – Latch truth table.

V_{RESET}	V_{IN}	Action
0	-	$V_{\text{OUT}} = 0$
1	0	$V_{\text{OUT}} = 1$
1	1	Keep State

The sensor also has an active-low reset command to place the wake-up latch into the “0” state. When V_{RESET} is high, the latch output is held until the input goes low, forcing V_{OUT} high.

To achieve the behavior shown in Table 3, the output of the voltage translator gates its own power supply via an additional inverter, I_6 , as described in Section 3.1. This configuration is shown in Figure 3.8. Inverters I_2 - I_5 are the four inverters in S_2 .

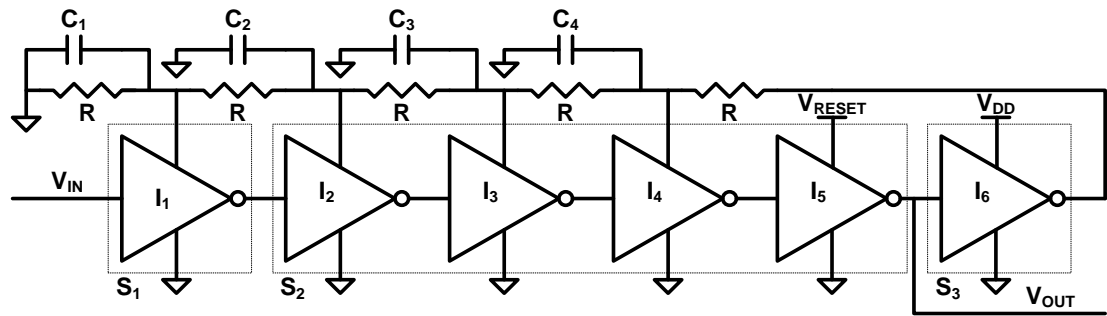


Figure 3.8 – Representation of the latch as a series of inverters.

The resistor string in Figure 3.8 is realized using off-state PMOS devices. Each device was sized to be 100 times the width of the largest device in the inverters. Additional on-chip MOS-capacitors placed at each of the intermediate nodes supply the inverters with instantaneous current.

Figure 3.9 shows the ideal timing sequence for the latch for 0.1Hz operation. Following a falling edge of V_{IN} , at time t_0 , V_{OUT} will rise to V_{DD} as long as V_{RESET} remains high. The propagation delay of the wake-up circuit, t_p , shown in Figure 3.9 is the delay from the falling edge of V_{IN} to the rising edge of V_{OUT} . The falling edge of V_{OUT} will coincide with the falling edge of V_{RESET} .

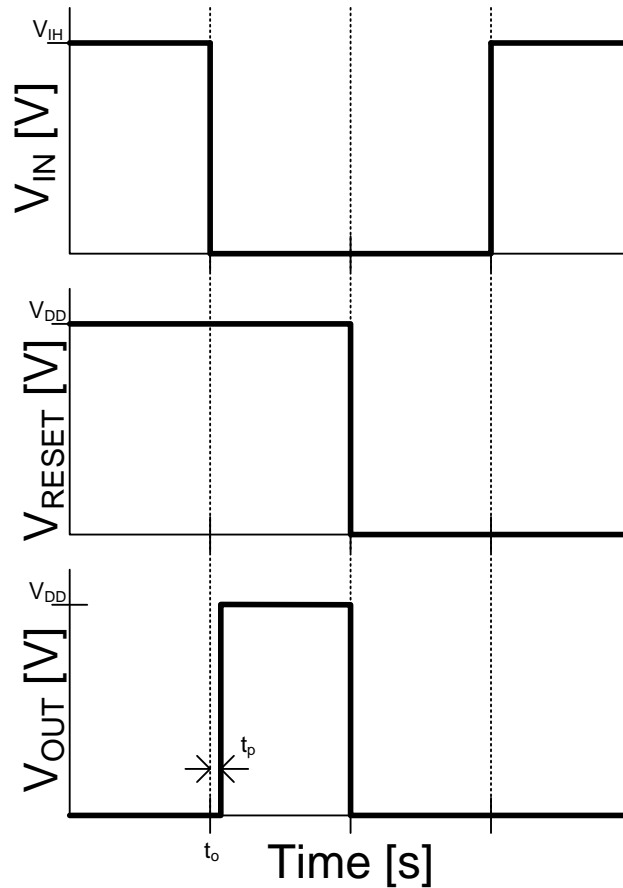


Figure 3.9 – Ideal timing sequence for the DC input circuit shown in Figure 3.8.

3.7. Variations in Propagation Delay

In the ideal case, t_p would be constant. This would result in the wake-up circuit having infinite accuracy, and the sensors waking up at exactly the same time. However, process variations affect the leakage rates of the cut-off devices causing chip-to-chip variations in t_p . In addition to chip-to-chip variations of t_p , there are also finite variations in t_p from one wake-up event to the next within the same chip.

Temperature and process-variation-induced variations in t_p are predictable for a single chip and a sophisticated communications protocol can account for them. Unpredictable event-to-event propagation delay variations lead to a loss of synchronization accuracy between RF receivers and transmitters, requiring the receiver to power up sooner and stay powered longer to ensure reception of the transmitted data. Figure 3.10 shows the variations in the simulated propagation delay for a wake-up circuit at a constant temperature with thermal and flicker noise included. The simulated 3σ range is 0.42% of the total propagation time of the wake-up circuit.

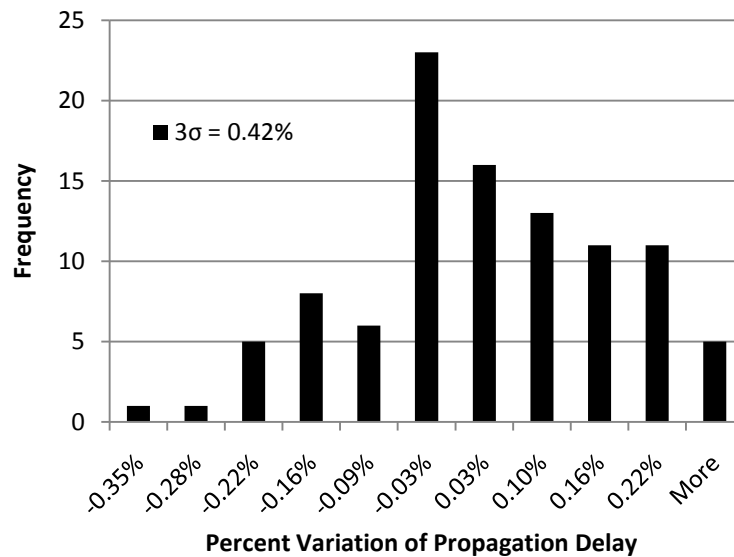


Figure 3.10 – Simulated variations in propagation delay due to transistor noise.

3.8. Latch Failures and Monte Carlo Simulations

In addition to affecting the propagation delays of separate wake-up circuits, process and temperature variations can also cause the wake-up circuit to fail. Figure 3.11 shows the failure rates of the latch over a range of temperature and V_{IN} . In the temperature range of -10 to 30 °C, the failure rate is less than 10%. Only in the hottest conditions and smallest V_{IN} does the failure rate surpass 10%.

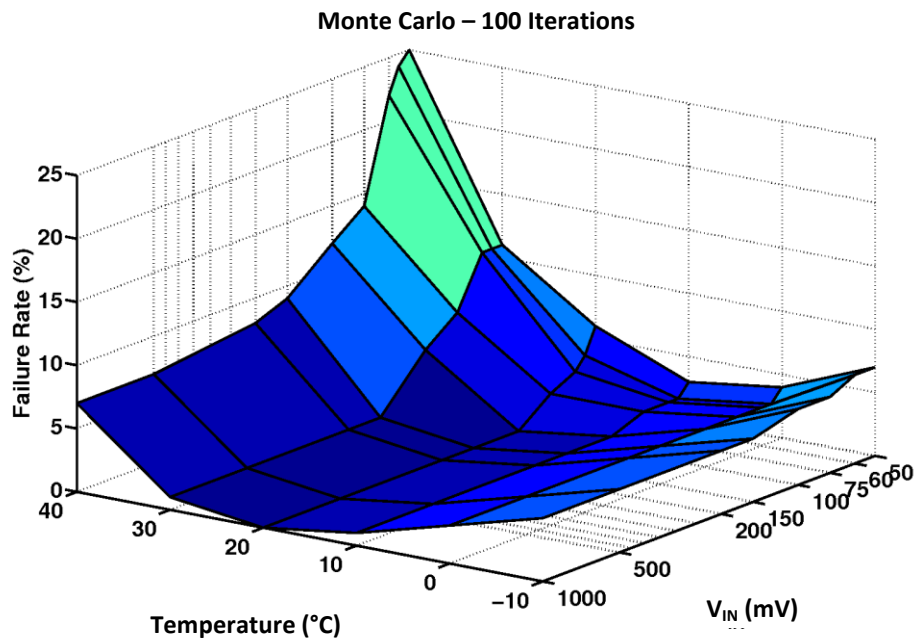


Figure 3.11 – Monte Carlo simulations showing failure rates over a range of temperature and V_{IN} .

4. EXPERIMENTAL RESULTS

4.1. Fabrication

The wake-up circuit has been fabricated in a 1P6M 0.18 μ m standard CMOS process. A die photo is shown in Figure 4.1. Three independent test circuits were fabricated. Only the DC input circuit (0.3mm x 0.2mm) is discussed in Chapter 3. The RF input circuit (0.3mm x 0.3mm) is the DC input circuit with a single-stage of the 36-stage RF energy harvester attached to its input. The third circuit is the DC input circuit attached to the full 36-stage RF energy harvester and voltage regulator (0.7mm x 0.5mm), as shown in Figure 2.3; it was fabricated for later, system-wide testing. The perimeter of the design is a conventional pad ring and each pad is fully ESD protected. The wafer was bonded in a MLF48 package (standard QFN package).

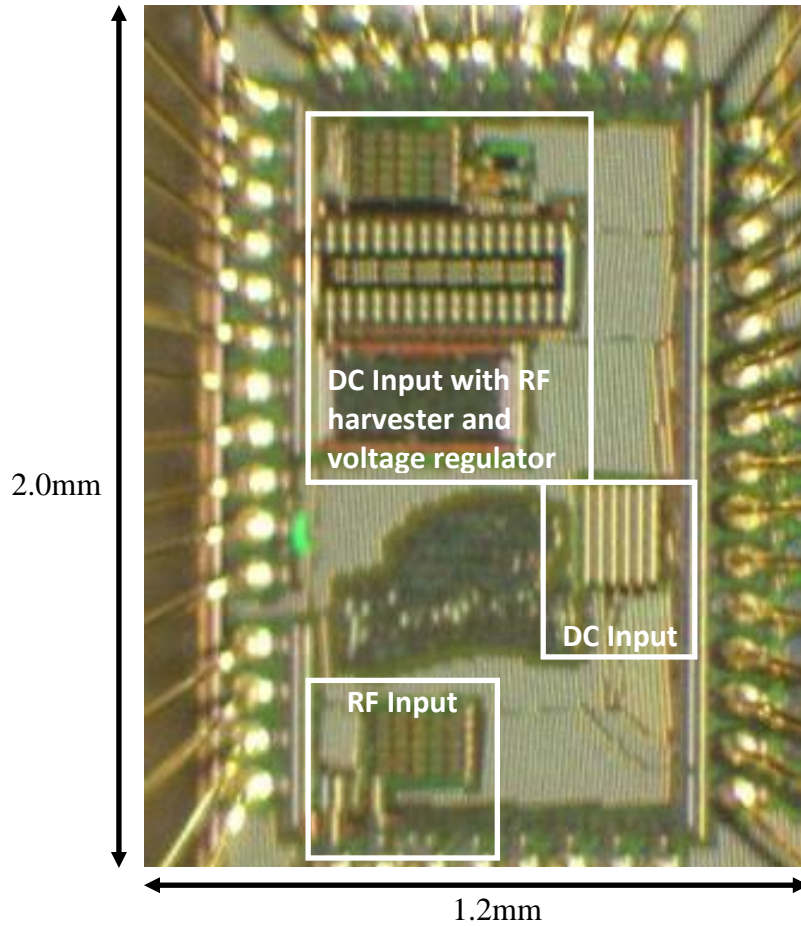


Figure 4.1 – Die photo of the test chip.

4.2. Test Board

The QFN package is mounted on a standard FR4 printed circuit board. A 120V/60Hz to 6.1V AC/DC converter supplies power to the test board. A 5V regulator and a 1.8V regulator provide the supply voltages required to verify the functionality of the design. The 5V regulator supplies the on-board buffers and amplifiers. The 1.8V regulator supplies a variable voltage divider that in turn powers the chip's ESD. Two-pin jumpers can then route power to each of the three test circuits' power pins on the chip independently by adding or removing their headers. All inputs and outputs have SMA connectors for improved signal quality and ease of use with the test equipment.

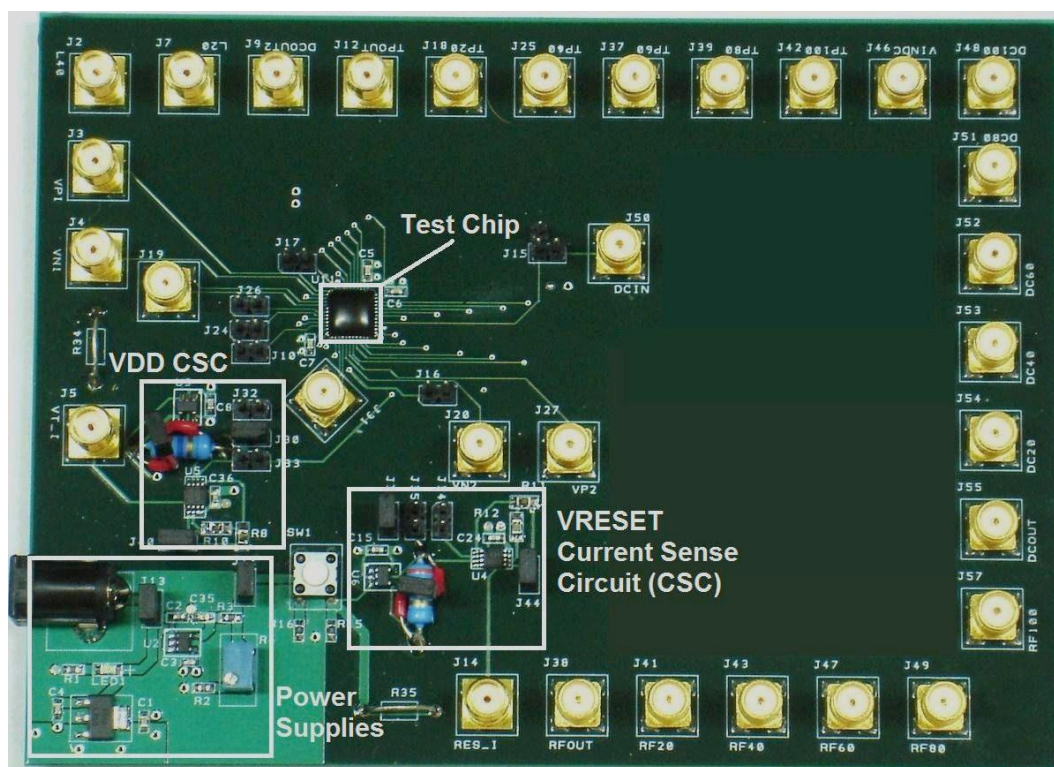


Figure 4.2 – Photo of the test board.

In each of the three test circuits, all test-point outputs are buffered with the EL5427 2.5MHz rail-to-rail buffers. This buffer offers multi-channel packages and has a 1pF input capacitance. Each power supply pin is buffered with a current sense resistor in the feedback loop.

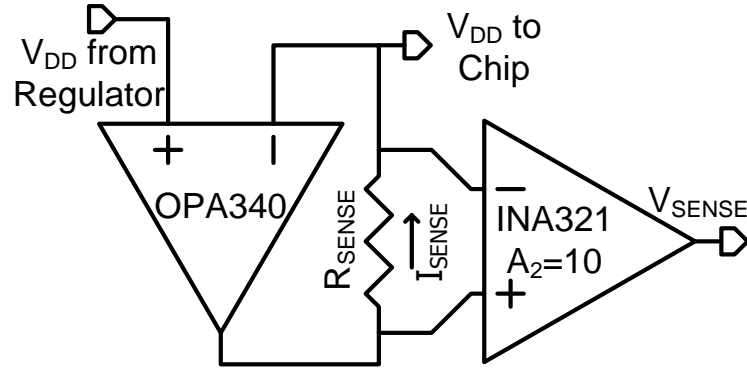


Figure 4.3 – An operational amplifier (OPA340) and an instrumentation amplifier (INA321) in a current sense configuration.

Figure 4.3 shows an operational amplifier (OPA340) and an instrumentation amplifier (INA321) in a current sense configuration. General-purpose operational amplifiers and instrumentation amplifiers tend to have BJT input devices that have non-negligible input-bias currents. In order to detect currents as low as 1nA accurately, the OPA340 and INA321 were selected for their low input-bias currents. These parts have CMOS input devices that sink or source currents from their inputs that are no more than 10pA. The OPA340 keeps the V_{DD} from the regulator and the V_{DD} to the chip at the same voltage. All the current flowing to the chip is sourced by the OPA340 and flows through R_{SENSE} . The INA321 amplifies the voltage potential across R_{SENSE} . Eq. (20) relates the output voltage, V_{SENSE} , to the measured current, I_{SENSE} .

$$I_{SENSE} = \frac{V_{SENSE}}{A_2 \cdot R_{SENSE}} \quad (20)$$

The resistor, R_{SENSE} , is a 133k Ω resistor, correlating to the desired range of V_{SENSE} , 1mV-1V, to the expected possible supply current, 750pA-750nA. Each resistor was independently measured and recorded prior to installation on the PCB.

4.3. Test Set Up

A Tektronix AWG2005 Arbitrary Waveform Generator (AWG) supplied the input stimulus in each test case, and a Tektronix TDS7401 Digital Storage Oscilloscope (DSO) with $10\text{M}\Omega$ input impedance recorded the results. A 50Ω -terminated oscilloscope would have excessively loaded the high-impedance signals and could not have probed them.

To test the DC input circuit, the AWG was used to drive V_{IN} with 200mV , 0.1Hz and the Reset line with 1V , 0.1Hz square-waves in quadrature with the timing shown in Figure 3.9.

4.4. Propagation Delay of the DC Circuit

The measured operation of the DC input circuit is illustrated in Figure 4.4. This plot shows the results of 40 transitions and illustrates the range of propagation times (t_p) measured from where the falling edge of the input crosses V_{SW} to the mid-point on the rising edge of the output for various amplitudes of V_{IN} . The average value for t_p is $418\mu\text{s}$ with a Δt_p of $33\mu\text{s}$.

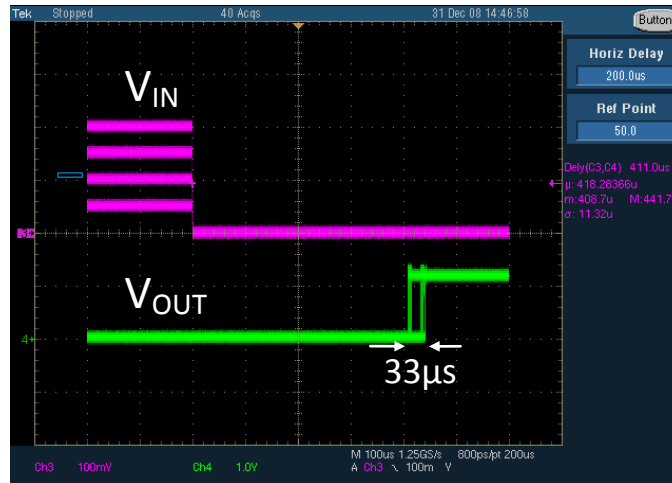


Figure 4.4 – Measured V_{IN} and V_{OUT} for amplitudes of $V_{\text{IN}} = \{50, 100, 150, 200\}$ mV.

Figure 4.5 illustrates the measured propagation delays of a single wake-up circuit versus a range of V_{IN} over 100 iterations. The range of the variation due to V_{IN} is $33\mu s$. The variation in propagation delay from one wake-up event to the next at the same V_{IN} is indicated by the vertical 6σ error bars. The 3σ variation is approximately 0.9% of the total propagation delay. This variation in the propagation delay is approximately twice the simulated results of Section 3.7.

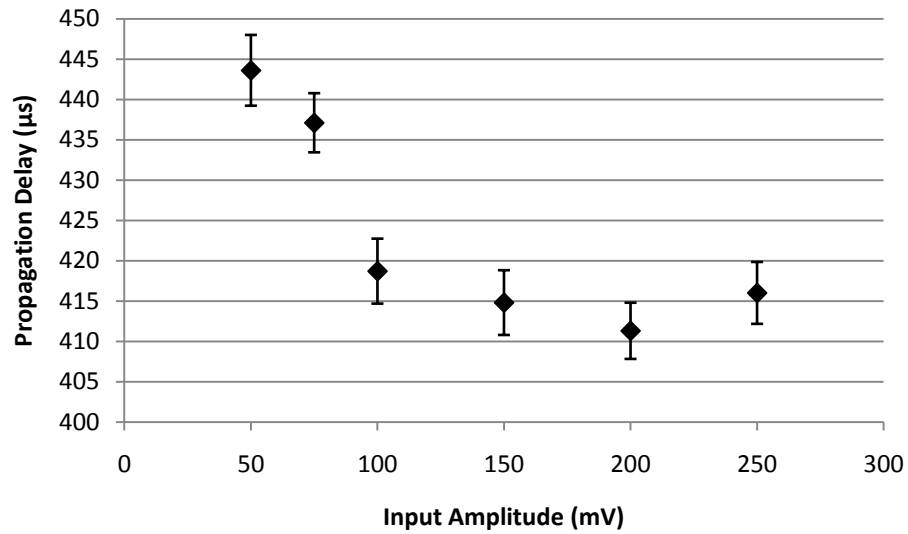


Figure 4.5 – Measured propagation delays for various input amplitudes. The bars indicate 6σ variations. The 3σ variation is approximately 0.9% of the total propagation delay.

4.5. Power Consumption of DC Circuit

Figure 4.6 is a close up of the rising edge of V_{OUT} , occurring approximately $400\mu s$ after the falling edge of V_{IN} . The first rising edge in Figure 4.6 is the switching transient of V_{SENSE} , shown in Figure 4.3. The second rising edge is V_{OUT} . The value of V_{SENSE} on the left side of the figure shows the level of the static current. This value of $120mV$ translates to a static current of $36nA$ using Eq. (20). The circuit consumes $45nW$ of static power from a $1.25V$ supply at $20^\circ C$.

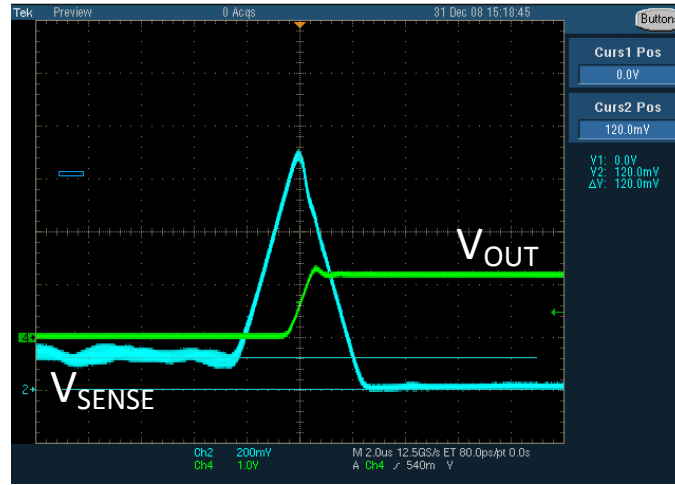


Figure 4.6 – Measured static current and switching transient.

The area under the V_{SENSE} curve shown in Figure 4.7 is proportional to the total energy consumed during a single switching event. Eq. (21) uses Eq. (20) to relate the area under the V_{SENSE} curve to the energy consumed per switching transient.

$$E_{sw} = \int_t V_{DD} \cdot I_{SENSE} dt = V_{DD} \int_t \frac{V_{SENSE}}{A_2 \cdot R_{SENSE}} dt = \frac{V_{DD}}{A_2 \cdot R_{SENSE}} \int_t V_{SENSE} dt \quad (21)$$

The integral of V_{SENSE} over time is the area under the V_{SENSE} curve in Figure 4.7. The area can be approximated as the area of a triangle shown in Eq. (22). Eq. (23) uses Eq. (21) and Eq. (22) to calculate an approximate value for the total energy consumed.

$$\int_t V_{SENSE} dt \simeq A_{\Delta} = \frac{base \cdot height}{2} = \frac{t_{sw} \cdot V_{SENSE,PK}}{2} = \frac{5\mu s \cdot 870mV}{2} \quad (22)$$

$$E_{sw} = \frac{1.2V}{10 \cdot 133k\Omega} \cdot \frac{5\mu s \cdot 870mV}{2} = 2pJ \quad (23)$$

Each switching event consumes approximately 2pJ of energy.

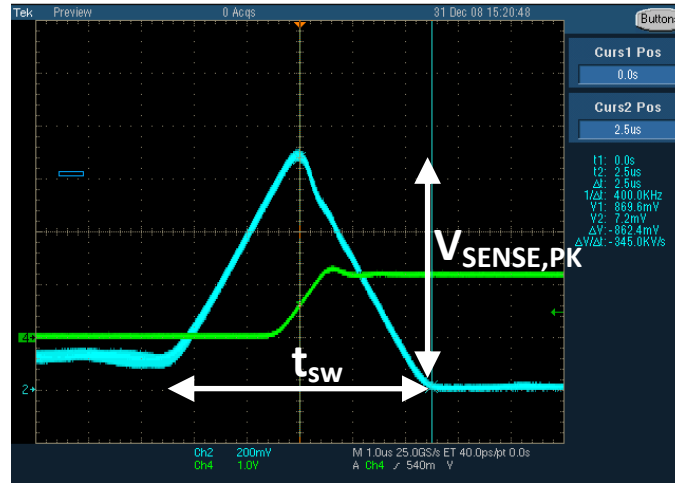


Figure 4.7 – Measured current consumed per switching transient.

4.6. Temperature Response

Implicit in this design has been the assumption that the wake-up circuit will work across a range of temperatures and that the propagation delays of the wake-up circuits is a predictable function of temperature. Figure 4.8 shows the propagation delays of a wake-up circuit as its temperature changes from -10C to 40C. Each successive rising edge of the output was observed to have a propagation delay greater than the previous rising edge. This is empirical evidence that the propagation delay is a monotonically increasing function of temperature.

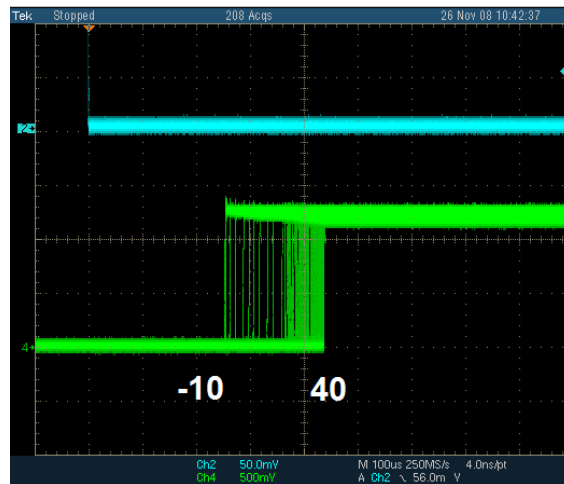


Figure 4.8 – Temperature response of the wake-up circuit with constant V_{IN} value showing t_p to be a monotonically increasing function of temperature.

4.7. RF Circuit Response

The only difference between the DC input circuit and the RF input circuit is the presence of a single stage full-wave floating-gate rectifier at the input. The rectifier converts the 900MHz RF input into the DC level used to test the DC input circuit. The behavior of this floating-gate rectifier is documented in [7]. Figure 4.9 illustrates how the loss of the RF power signal triggers the output to toggle just as the loss of a DC signal triggers the output to toggle in the DC input circuit. The rest of the circuit behaves identically to the DC input circuit.

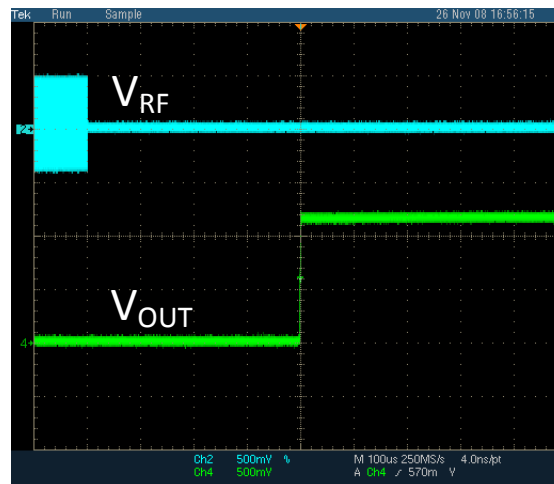


Figure 4.9 – Measured output response to an RF input.

4.8. Comparison to Prior Work

Table 4 compares the work presented in this thesis to other wireless sensor network synchronization methods. None of these has been fabricated in silicon and all consume more power than is available from the RF energy harvester. Table 4 shows that only the wake-up circuit consumes less than 100nW and no other wireless sensor network synchronization method consumes less than 1 μ W. The synchronization limiting factor, listed in the table, refer to the accuracy with which each system can predict when any given sensor will wake up. The worst case asynchronization of the wake-up circuit is less than 8 μ s, more than an order of magnitude better than the next best system.

Table 4 – Comparison of the wireless sensor network synchronization methods.

Method	Low Power Mode [26]	Continuous Timestamp [14]	Interrupt Timer [13]	Wake-up Circuit (this work)
Continuous Power	100 μ W	1-10 μ W*	5.68 μ W*	44nW
Synchronization Limiting Factor	Accuracy of external interrupt.	1ms – Data rate of 1kbps data stream. Requires line-of-sight.	100 μ s – Period of 10kHz clock.	8 μ s – $\pm 3\sigma$ uncertainty of the propagation delay

*Simulated

Table 5 compares the latched comparators presented in this thesis to prior latched comparators. The values reported for all these comparators were measured at much higher frequencies than this design requires and no static power values were reported. However, all four require a 3-3.3V supply. Additionally, the three that consume the least power have offset voltages that disqualify them from this application where the comparator must register a difference between 0mV and 58mV. Each of the comparators would also have to work in conjunction with a reference voltage, increasing their power requirements by several microwatts. The minimum power used by a latched comparator and a reference voltage combination is orders of magnitude greater than the total power used by the design presented in this thesis.

Table 5 – Comparison of the latched comparator to prior work

Method	Variable Load Comparator [17]	Low Power Differential Current [18]	Resistive Divider [18]	Charge Sharing [18]	Threshold Based Reference Latched Comparator (this thesis)
Continuous Power	340 μ W*	138 μ W*	114 μ W*	88.2 μ W*	44nW
Supply Voltage	3V	3.3V	3.3V	3.3V	1.2V
Max Offset Voltage	3mV	164mV	32mV	32mV	10mV

*Requires additional reference voltage

5. CONCLUSION

A new low-power latched comparator has been presented as a part of a battery-free, RF energy harvesting wireless sensor network. It uses multiple common-source amplifiers to amplify the DC input signal to control the power to the system. Combined with a feedback latching circuit, the latching comparator has a threshold voltage less than 58mV. The design presented in this thesis draws less than 45nW of static power at 20 °C. Finally, it provides a synchronization method that consumes two orders of magnitude less power with increased synchronization accuracy.

6. REFERENCES

- [1] M. Philipose, J. R. Smith, B. Jiang, A. Mamishev, and S. Roy, "Battery-free wireless identification and sensing," *IEEE Pervasive Computing*, vol. 4, no. 1, pp. 37-45, Jan. 2005.
- [2] Q. Tang, L. Yang, G. B. Giannakis, and T. Qin, "Battery power efficiency of PPM and FSK in wireless sensor networks," *IEEE Transactions on Wireless Communications*, vol. 6, no. 4, pp. 1308-1319, Apr. 2007.
- [3] F. Kocer, P. M. Walsh, and M. P. Flynn, "Wireless, remotely powered telemetry in 0.25 μ m CMOS," in *2004 IEEE Radio Frequency Integrated Circuits (RFIC) Systems Dig. Papers*, Forth Worth, TX, Jun. 2004, pp. 339-342.
- [4] FCC 47 CFR Part 15.247(a)(3), "Radio frequency devices: Operation within the bands 902–928 MHz, 2400–2483.5 MHz, and 5725–5850 MHz.," Oct. 2007.
- [5] D. K. Cheng, *Field and Wave Electromagnetics*, 2nd ed., Addison-Wesley Publishing Company, 1992.
- [6] T. Ugan and L. M. Reindl, "Harvesting low ambient RF-sources for autonomous measurement systems," in *IEEE Instrumentation and Measurement Technology Conference Proceedings*, May 2008, pp. 62-65.
- [7] T. Le, K. Mayaram, and T. S. Fiez, "Efficient Far-Field Radio Frequency Energy Harvesting for Passively Powered Sensor Networks," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1287-1302, May 2008.
- [8] B. Otis, Y. H. Chee, and J. Rabaey, "A 400 μ W-RX, 1.6mW-TX super-regenerative transceiver for wireless sensor networks," in *IEEE International Solid-State Circuits Conference*, Feb. 2005, pp. 396-606.
- [9] B. W. Cook, A. Berny, A. Molnar, S. Lanzisera, and K. S. J. Pister, "Low-Power 2.4-GHz Transceiver With Passive RX Front-End and 400-mV Supply," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2757-2766, Dec. 2006.
- [10] N. Panitantom, K. Mayaram, and T. S. Fiez, "A 900-MHz low-power transmitter with fast frequency calibration for wireless sensor networks," in *IEEE Custom Integrated Circuits Conference*, Sep. 2008, pp. 595-598.
- [11] J. Ayers, K. Mayaram, and T. S. Fiez, "A 0.4 nJ/b 900MHz CMOS BFSK super-regenerative receiver," in *IEEE Custom Integrated Circuits Conference*, Sep. 2008, pp. 591-594.
- [12] H. W. Johnson and M. Graham, *High Speed Digital Circuits*. Prentice Hall, 1993.
- [13] M. Hempstead, N. Tripathi, P. Mauro, G.-Y. Wei, and D. Brooks, "An ultra low power system architecture for sensor network applications," in *32nd International Symposium on Computer Architecture*, Jun. 2005, pp. 208-219.
- [14] J. M. Kahn, R. H. Katz, and K. S. J. Pister, "Next century challenges: Mobile networking for "Smart Dust",," in *The Fifth Annual ACM/IEEE International Conference on Mobile Computing and Networking*, Aug. 1999, pp. 271-278.

- [15] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proceedings of the IEEE*, vol. 91, no. 2, pp. 305-327, Feb. 2003.
- [16] T. Le, "Efficient power conversion interface circuits for energy harvesting applications," Ph.D. dissertation, Oregon State University, Corvallis, Oregon, USA, Apr. 2008.
- [17] A. Boni and C. Morandi, "High-speed, low-power BiCMOS comparator using a pMOS variable load," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 1, pp. 143-146, Jan. 1998.
- [18] P. Uthaichana and E. Leelarasmee, "Low power CMOS dynamic latch comparators," in *Conference on Convergent Technologies for Asia-Pacific Region*, Oct. 2003, pp. 605-608.
- [19] T. Shihabudheen, S. Babu, and M. Baiju, "A low power sub 1V 3.5-ppm/°C voltage reference featuring subthreshold MOSFETs," in *15th IEEE International Conference on Electronics, Circuits and Systems*, Sep. 2008, pp. 442-445.
- [20] G. Giustolisi, G. Palumbo, M. Criscione, and F. Cutri, "A low-voltage low-power voltage reference based on subthreshold MOSFETs," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 1, pp. 151-154, Jan. 2002.
- [21] R. F. Pierret, *Semiconductor Device Fundamentals*. Addison Wesley Longman, 1996.
- [22] Y. Dai, D. T. Comer, D. J. Comer, and C. S. Petrie, "Threshold voltage based CMOS voltage reference," *IEE Proceedings - Circuits, Devices and Systems*, vol. 151, no. 1, pp. 58-62, Feb. 2004.
- [23] B. H. Calhoun, A. Wang, and A. Chandrakasan, "Modeling and sizing for minimum energy operation in subthreshold circuits," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 9, pp. 1778-1786, Sep. 2005.
- [24] C. A. Enz and E. A. Vittoz, *Charge-based MOS Transistor Modeling*. Chichester, England: John Wiley & Sons Ltd., 2006.
- [25] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits*, 2nd ed., Prentice Hall, 2003.
- [26] V. Shnayder, M. Hempstead, B. Chen, G. W. Allen, and M. Welsh, "Simulating the power consumption of large-scale sensor network applications," in *Proceedings of the 2nd international conference on embedded networked sensor systems*, Nov. 2004, pp. 188-200.
- [27] F. X. Moncunill-Geniz, P. Pala-Schonwalder, C. Dehollain, N. Joehl, and M. Declercq, "An 11-Mb/s 2.1-mW Synchronous Superregenerative Receiver at 2.4 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 6, pp. 1355-1362, Jun. 2007.

