AN ABSTRACT OF THE THESIS OF

SHAH CHAMPAKLAL C. (Name) for the MASTER OF SCIENCE (Degree)

in Electrical and Electronics Engineering (Major) presented on Dec 15, 1972 (Date)

Title: AN INTERFACE OF A MAGNETIC DISC FOR A PDP-8/L COMPUTER SYSTEM

Abstract approved: Redacted for Privacy
Donald L. Amort

This thesis is concerned with the design of the interface--Read, Write and control circuits--of the magnetic disc with the PDP-8/L Computer system. The interface was designed to operate under the Data Break transfer mode of the computer and is compatible with the computer manufacturer's system.

The Data Break option was built. The circuit components for writing and reading were experimentally determined for the best performance and, the cost of the major units of the system, excluding the labor cost, was estimated. The interface was constructed on eight printed circuit cards, using standard TTL IC chips, transistors, resistors and operational amplifiers.

Since data is being stored and retrieved in parallel this storage system is faster than the conventional serial transfer. The interface has been constructed such that DEC's software for a single disc and

diagnostic software can be used. This paper indicates how a simple, inexpensive and reliable interface can be developed by using commercially available integrated circuits.

An Interface of a Magnetic Disc for a PDP-8/L Computer System

by

Shah Champaklal C

A THESIS

submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

June 1973

APPROVED:

Redacted for Privacy

Associate Professor of Electrical and Electronics Engineering
in charge of major

Redacted for Privacy

Head of Department of Electrical and Electronics Engineering

Redacted for Privacy

Dean of Graduate School

Date thesis is presented 15 December 1972

Typed by Clover Redfern for Shah Champaklal C.

ACKNOWLEDGMENT

The author wishes to express gratitude to Professor D. L. Amort for his patience, advice, suggestion, and assistance in directing the design and writing of this thesis.

TABLE OF CONTENTS

LIST OF FIGURES

AN INTERFACE OF A MAGNETIC DISC FOR A PDP-8/L COMPUTER SYSTEM

I. INTRODUCTION

The magnetic disc file and the interface is a fast parallel access bulk storage device used with the PDP-8/L computer for memory expansion. It provides a capacity of 24,576 13 bit words which are stored on a rotating disc.

The disc file is a program initiated device used in conjunction with the PDP-8/L and operates through 3-cycle data break facility of the computer.

The cost of the system was to be minimized by making use of the existing unused magnetic disc and some interface material. The interface was to be designed to keep the transfer rate maximum and to realize full benefit of the built-in features of the PDP-8/L computer data break input-output transfer. All the requirements imposed by the computer bussed system are met. The magnetic disc and interface which have been commercially available are expensive. Therefore the development of this system is based on low cost as well as reliability and simplicity.

System Specification

Storage capacity	24,576. 13 bits word. (60 hz power).
Data transfer rate	6 us/word.
Average access time	25 milliseconds.
Addressing scheme	Random or Sequential addressing from 0 to 24,576 words with variable block size from one word to 4096 words.
Data assembly	Read/Write to and from disc is in parallel with external transfer also in parallel by word.
Timing track	One, with three spare (Addressing Track).
Data tracks	39 with 1 spare.
Words per track	8192.
Recording method	RZ-Return to Zero (Modified).
Operating environment	0 to 70°C.
Heat dissipation	Since heat dissipation is small extra cooling is not required.
Power requirements	110 V 60 hz for disc, ±5 V DC for the interface.

Physical Description

The printed circuit boards containing interface and control logic are mounted on a standard rack. All the data break signals are

obtained through a cable connector from the computer and the programmed transfer signals which are available on the existing rack are connected to the back of the disc rack by a P. C. board and cables. Timing and data signals to and from the disc are connected to the back wiring by ribbon connector. For operational flexibility and maintenance the connections going from the interface rack to the computer and disc can be disconnected very easily. Since heat dissipation of the interface is very small and there is a good circulation of air an extra cooling is not required.

II. OPERATION AND PROGRAMMING

The block diagram of the system interface is shown in Figure 1. Since it uses the 3-cycle data break facility of the computer some information regarding the data break system is in order. The block diagram of the data break facility (Figure 2), the three cycle data break flow chart showing the sequences of the events (Figure 3) and the timing diagram (Figure 4) are given.

Data breaks are of two basic types: (1) Single cycle and (2) Three cycle data break.

In the Single cycle data break, registers in the device (or device interface) specify the core memory address of each transfer and count the number of transfers to determine the end of data blocks requiring more hardware than in 3-cycle data break, in which two memory locations (7750 and 7751) perform these functions and do not require hardware registers. The data break facility works according to the timing and logic levels shown in Figure 4 regarding Break Request, Cycle Select, Transfer Direction, Increment CA Inhibit, Increment MB, WC Overflow, Add-Accepted, B-Break, Address and Data signals. The Address, Cycle Select, Increment CA Inhibit, Increment MB are permanently hard wired for the disc.

In general to initiate a data break transfer of information the interface control must do the following: (see Figures 2, 3, and 4)

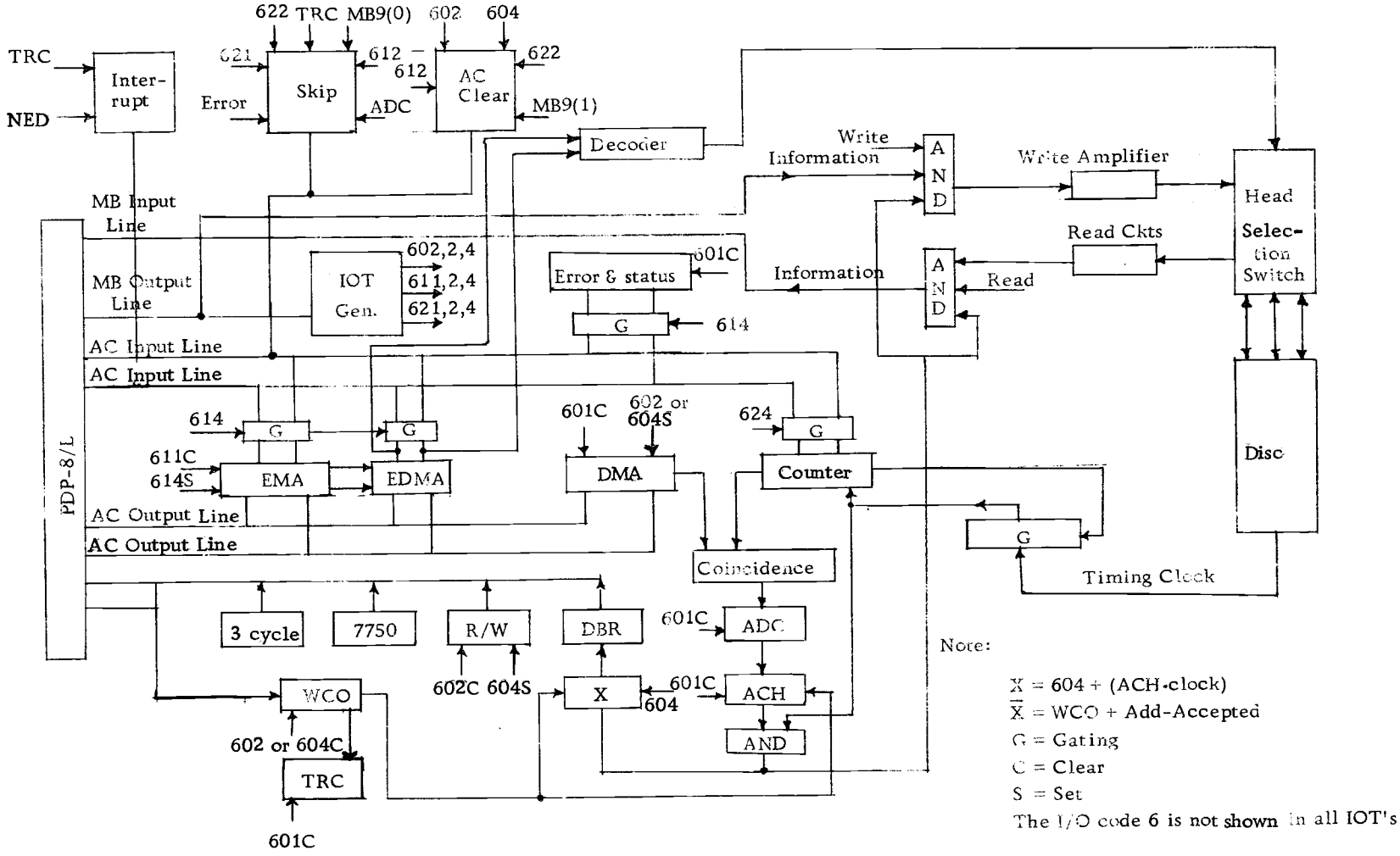


Figure 1. Block diagram of the system interface.

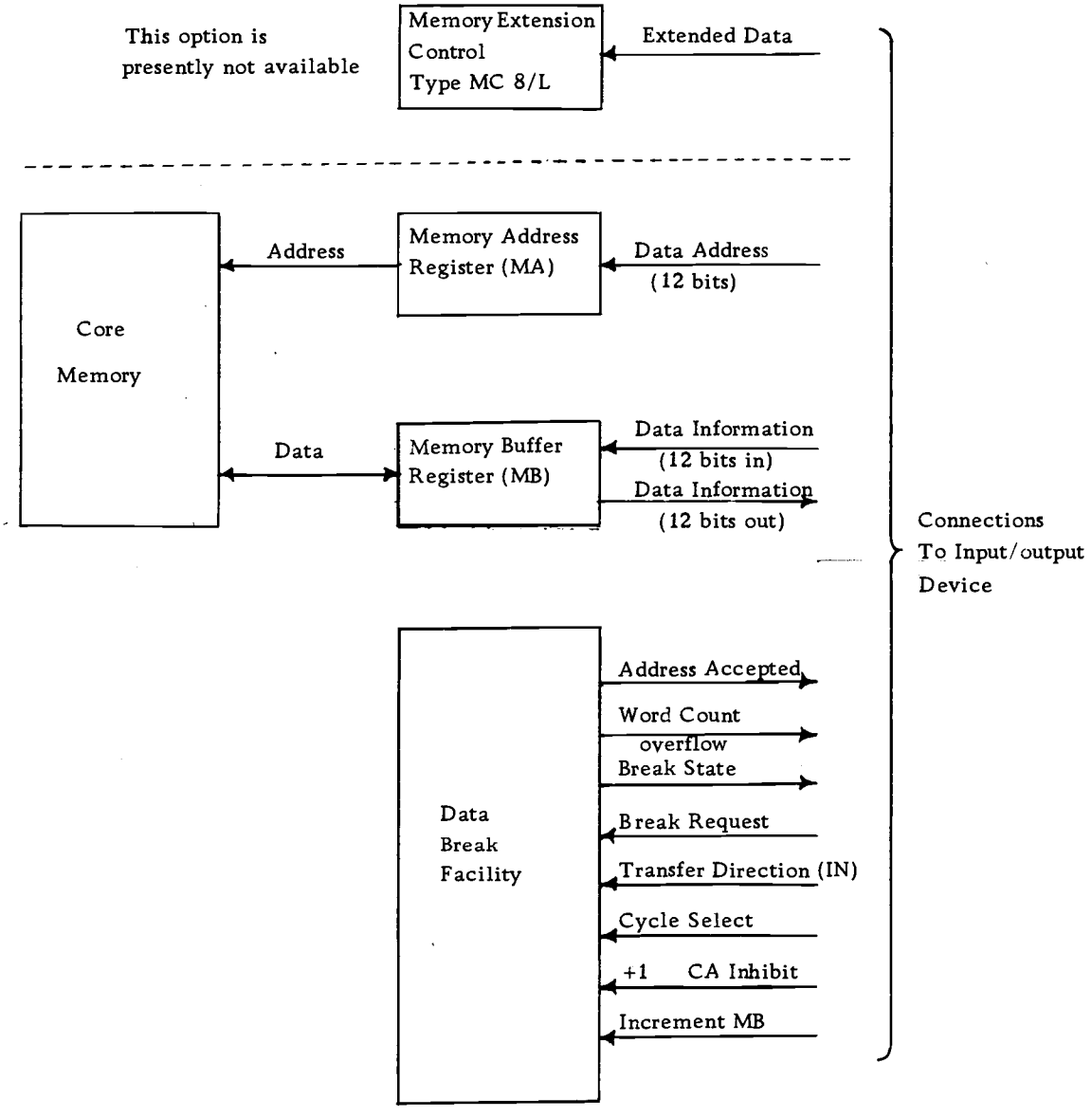


Figure 2. Block diagram of the Data Break Facility.

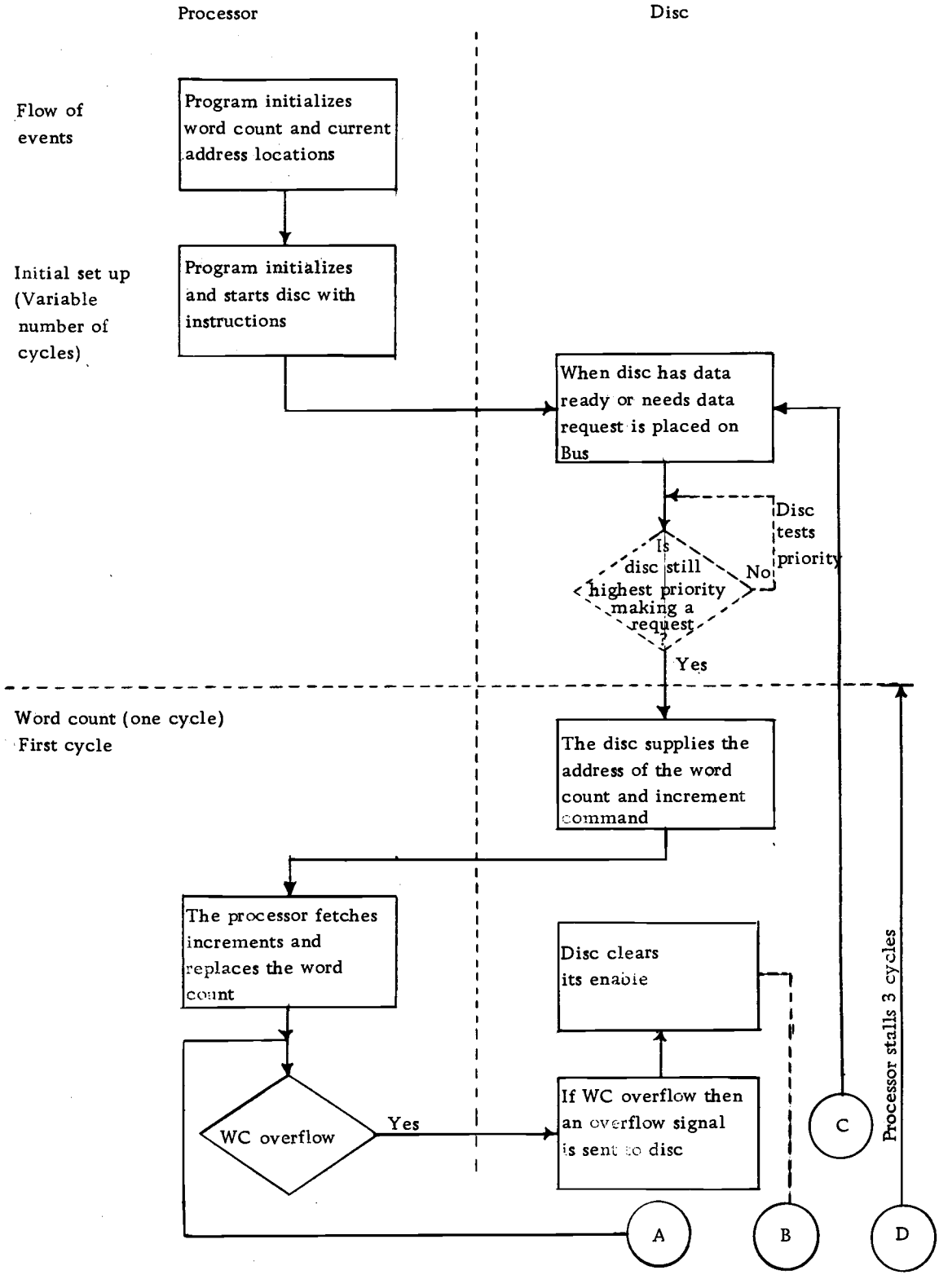
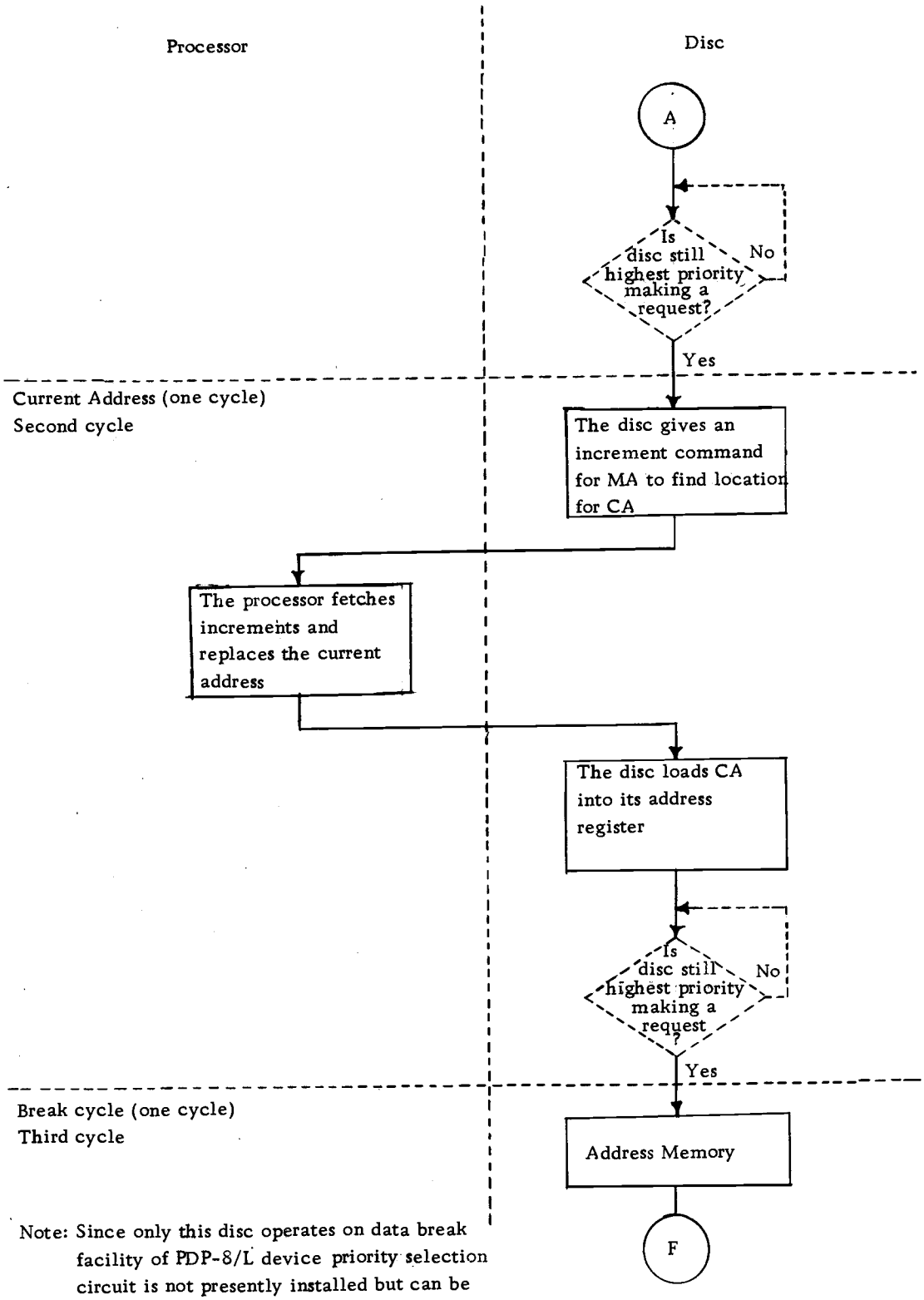


Figure 3. 3-cycle Data Break flow chart.



Note: Since only this disc operates on data break facility of PDP-8/L device priority selection circuit is not presently installed but can be installed in future.

Figure 3. Continued.

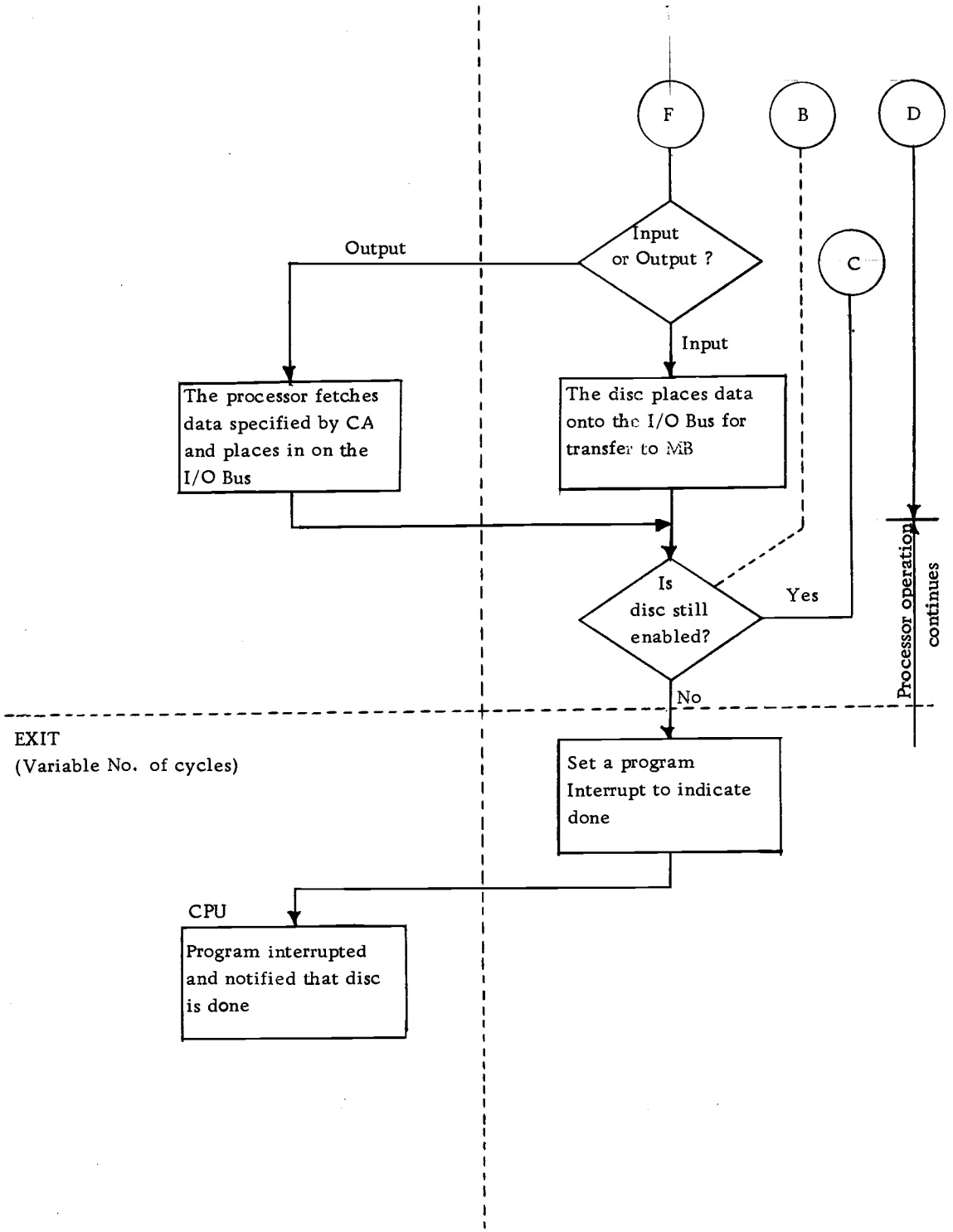


Figure 3. Continued.

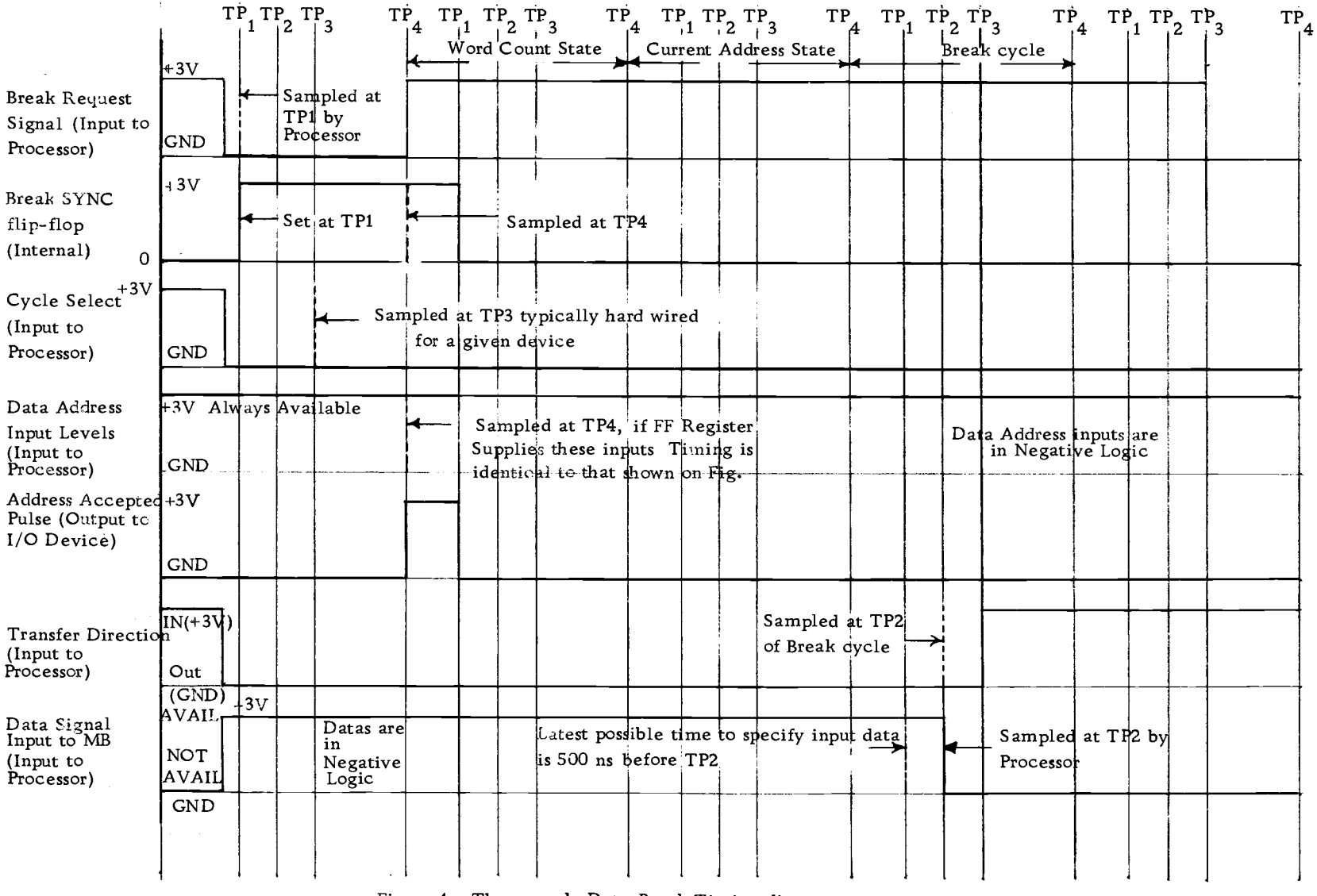


Figure 4. Three-cycle Data-Break Timing diagram.

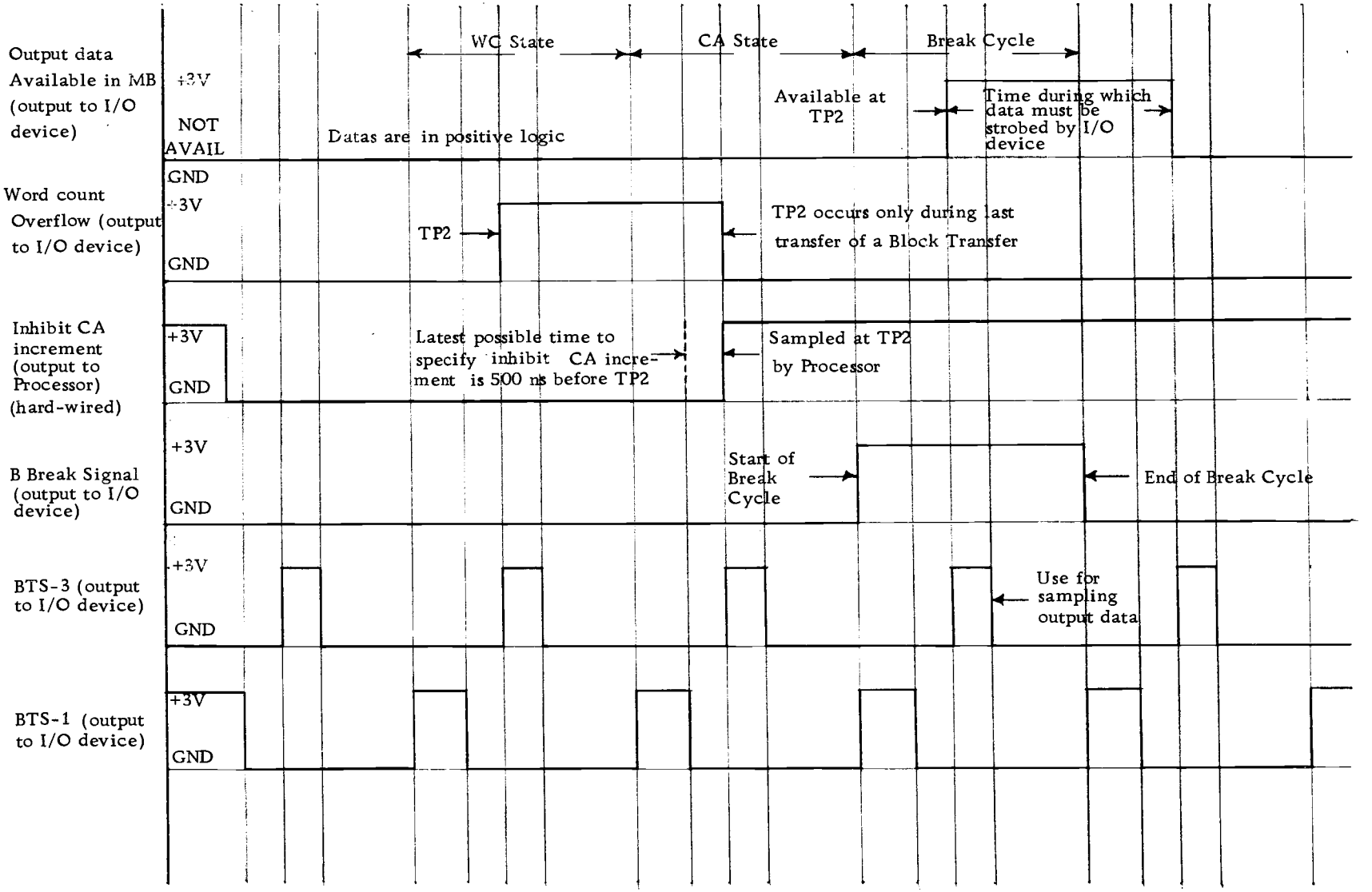


Figure 4. Continued.

(1) Request a data break by supplying a proper signal to the computer data break facility. Break Request signal sets the internal BRK-SYNC flipflop in the major state generator to control entry into the data break states (Word Count for a 3-cycle or Break for a Single cycle).

(2) A Transfer Direction signal supplied to the MB control element to allow data to be strobed into the MB from the peripheral equipment to inhibit reading from the core memory.

(3) A Cycle select signal which controls gating in the major state generator to determine if one cycle or three cycle data break is to be selected.

(4) Core memory address of the transfer which is supplied to the input of the MA.

At TP4 time of each machine cycle the major state generator is set to establish the state for the cycle. At this time the status of the BRK-SYNC flip-flop is sampled and if in one state (because of Break Request signal) the word count state (cycle select signal is permanently grounded for the disc- 3-cycle) is set into the major state generator and a data break commences. At the beginning of the Word Count cycle of the three cycle data break, the hard wired address supplied by the disc to the input of the MA is strobed into the MA and computer supplies an Address-Accepted pulse. The content of the

specified address (7750) is read from memory and 1 is added to it before rewriting. If the content of this register becomes 0 as a result of the addition, a WC Overflow pulse will be transmitted to the device. To transfer a block of N words, this register is loaded with -N during programmed initialization of the device. After the block has been fully transferred this pulse is generated to signify completion of the operation. During TS3 and TS4 times, the incremented word count is rewritten, the contents of MA is incremented by 1 to establish the next location as the address for the following second cycle of the three cycle data break and the major state generator is set to the Current Address State.

In this second cycle the content of the location (7751) is incremented before rewriting. (Increment CA Inhibit signal can prevent incrementation but in the case of the disc it is incremented.) To transfer a block of data beginning at location A this register is program initialized by loading with A-1. During TS3 and TS4 times the contents of the MB is rewritten into core memory. The address word in the MB is transferred into the MA to designate the address to be used in the succeeding memory cycle (third and the last cycle) and the major state generator is set to Break State.

The actual transfer of data between the external device and the core memory through MB occurs during the Break State. If the Transfer Direction signal establishes the direction as out of the

computer, the content of the core memory register at the address specified is transferred into the MB and is immediately available for strobing by the peripheral equipment. If the transfer direction into the PDP-8/L is specified reading from core memory is inhibitted and data is transferred into the MB from the disc register. The status of the BRK-SYNC flip-flop is sensed at the beginning of a break cycle to determine if an additional break is required. If a Break Request signal has been received since TP4 the three cycles follow, otherwise the Fetch state is set into the major state generator to continue the main program.

The complete analysis of the IOT Instructions appears in Appendix A and the mnemonics appearing on the block diagram of the system interface (Figure 1) are explained in Appendix B. In the block diagram:

1. DMA - 13 bits register, loaded from Accumulator by an IOT Instruction.
2. EDMA - 2 bits register, loaded from Accumulator by an IOT Instruction.
3. EMA - 3 bits register, loaded from Accumulator by an IOT Instruction.
4. Counter - 13 bits long activated by clock pulses from Timing Track.

5. Coincidence Unit - 13 bits long, bit by bit comparator between Counter and DMA.
6. IOT Generator - Standard Generator to generate IOT Instructions.
7. Read Ckts. - Reads data from the disc heads.
8. Write Amplifiers - Writes data on the disc.
9. ADC, ACH, WCO, TRC, DBR, R/W - Various Control Flip-flops.
10. Error and Status Register.

Interrupt Flags

There are two flags that generate an interrupt: the NED--Non Existent Disc and TRC--Transfer Complete flags. The NED flag is set when the program selects via EDMA a word track which does not exist. The TRC flag signifies the end of the data transfer. It is set at the completion of the last word transfer by the disc, following a word count overflow of the WC register. The completion flag can be sensed by DFSC instruction.

Error Flags

The error flags can be sensed by the IOT 6621 DFSE instruction. The program skips when no error exists. The error flags are described in the following paragraphs.

DRL Flag. The DRL (Data request late) flag signifies that a data transfer operation occurred between the disc buffer and the disc before the previous transfer was handled by the data break facility.

PER Flag. The PER (Parity error) signifies that a parity error occurred before the read operation.

NED Flag. As described in the interrupt flags, NED flag is set when the program selects the wrong word track.

ADC Flag. The Address Confirmed ADC Flag is used in diagnostic programming and also to signify that the DMA corresponds to the track address currently passing under the read/write heads. It can be sensed by IOT 6612 DSAC instruction which skips if the flag is set.

Status Evaluation

The status of certain conditions can be evaluated by using the IOT 6614 which loads the Accumulator with the status as shown below:

AC 0 Which specify that the physical position of the disc corresponds to either lower 2k or upper 2k of 4k locations.

AC 1-2 Permanently high to signify binary '0' because of disc capacity and software limitation.

AC 3-5 Respectively EDMA 2 through EDMA 1 and DMA_{13}.

AC 6-8 Respectively EMA 3 through EMA 1.

AC 9 DRL (1)

AC 10 NED (1)

AC 11 PER (1).

Programming Example

A programming example that writes a block of data (corresponding to the contents of locations 200-374) is shown in Appendix C. For simplicity the example assumes that all the data and instructions are within the same page but in actual practice this may not be so.

Description

The JMS WRT instruction causes a subroutine jump to location WRT with the contents of the PC+1, which contains symbolic address SUB+ 1 deposited into location WRT. Since location WRT now contains Word Count, the first instruction of the subroutine (TAD I WRT) loads the AC with the contents of WC. The WC is then deposited into WC register (location 7750). Similarly the initial address is deposited into the CA register. The program then proceeds to set up EDMA and DMA registers and start the write operation. After the DMAW instruction is issued, the data transfer operation begins and continues independently of the program. It operates under the control of the data break facility to transfer data. Computer stays in DFSC and JMP. -1 loop until the TRC is set and then DFSC passes control to DFSE which senses for error and if any, control jumps to an error or diagnostic

routine which in the example given starts at 0022 and will print a question mark on the teletype printer. If there is no error, control exits from the subroutine back to the main program to resume main processing.

III. PRINCIPLES OF OPERATION

This chapter describes the principles of operation of the disc file system.

The disc system uses the three cycle data break facility of the PDP-8/L to transfer data. The WC (Word Count) and CA (Current Address) registers in memory are used to specify the number located in the memory core of the computer and the core memory address, respectively, of the data transfer. Initially, the program loads the WC register with 2's complement of the number of the word transfers and the CA register with the initial core memory address-1. Thereafter, the CA and WC are incremented after each data transfer.

After the program sets up the WC and CA registers, it issues a DEAL instruction to load the EDMA which specifies the word track number. If a write operation is specified, the DMAW instruction is issued to load the DMA register to specify the track word address that is to receive the word transfer. The DMAW also initiates a data break request so that the first word to be recorded is loaded into the DMBW. The write operation then transfers the contents of the DMBW to the addressed word track. After each transfer the counter is incremented to address the next sequential track address. Operation continues until the WC register is reduced to zero. When this occurs a WCO (Word Count Overflow) signal is sent to interface to terminate the operation.

Disc Format

The disc format is shown in Figure 5. There are 39 data tracks (one spare) and one timing track (with three spare). The timing track contains permanently recorded clock signal and provide the control circuits the track address information presently passing under the track heads.

RZ Recording (Modified)

In Return to Zero method of recording a pulse of current is applied in one direction through the magnetic head for a '0' and the current pulse in the opposite direction for a binary '1'. This method is called Return to Zero because the writing current returns to zero inbetween the consecutive element length. The method that has been used with the disc is modified RZ or Return to Saturation recording in which the magnetic medium is magnetized to one state of remanence, except in elements where a '1' is stored when the magnetization is reversed for part of the element length. Figure 6 shows the waveforms for the RS Recording. It can be seen from the waveforms of the writing current, readback signal and the clock signal shown in Figure 6, that in RS Recording the clock and the digit frequency are the same. In Figure 6 the distance allotted to the storage of one bit is called a 'cell' or element length. The individual cells are indicated in the figure along with the binary value stored in each cell. As far as the read

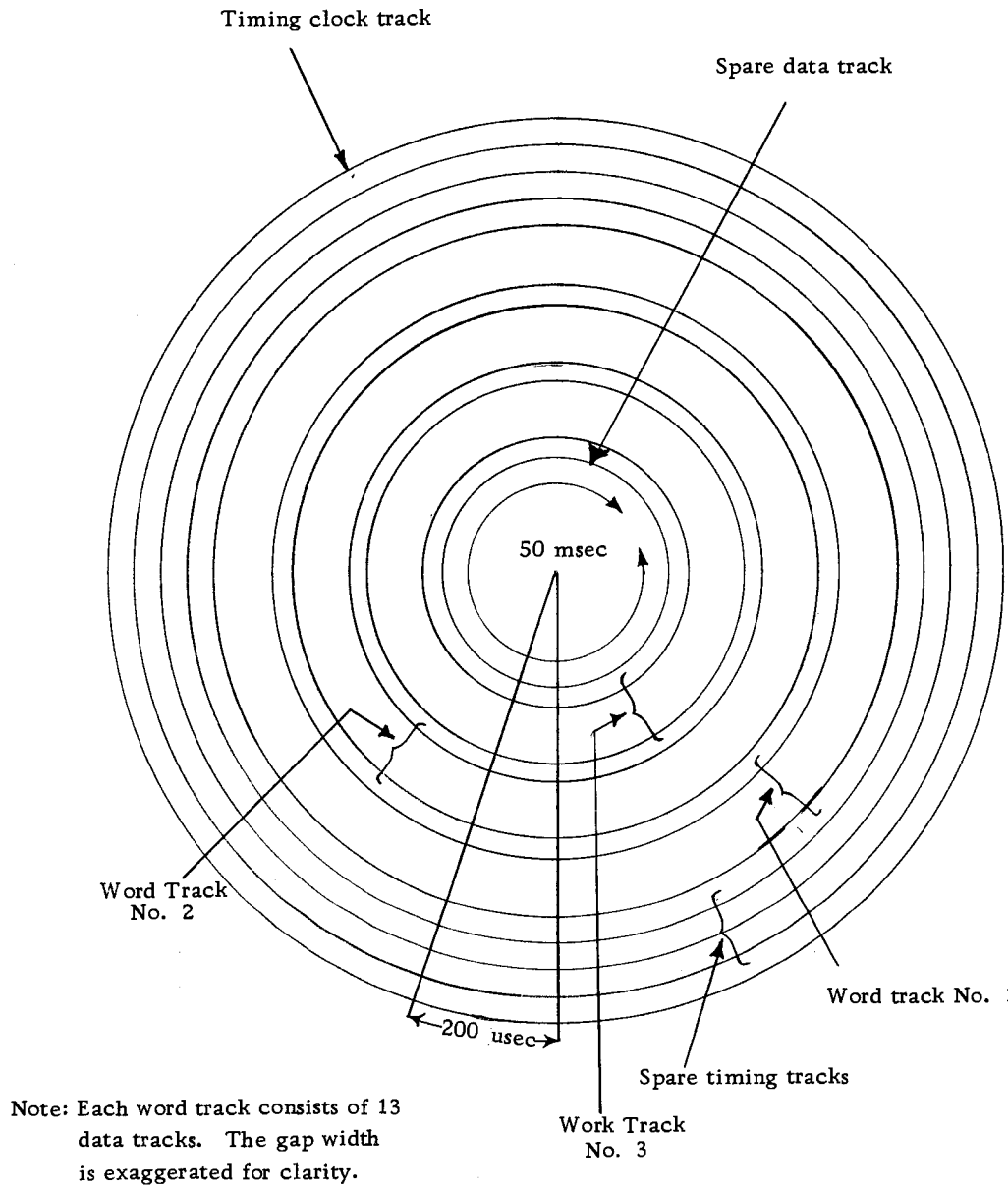


Figure 5. The disc format.

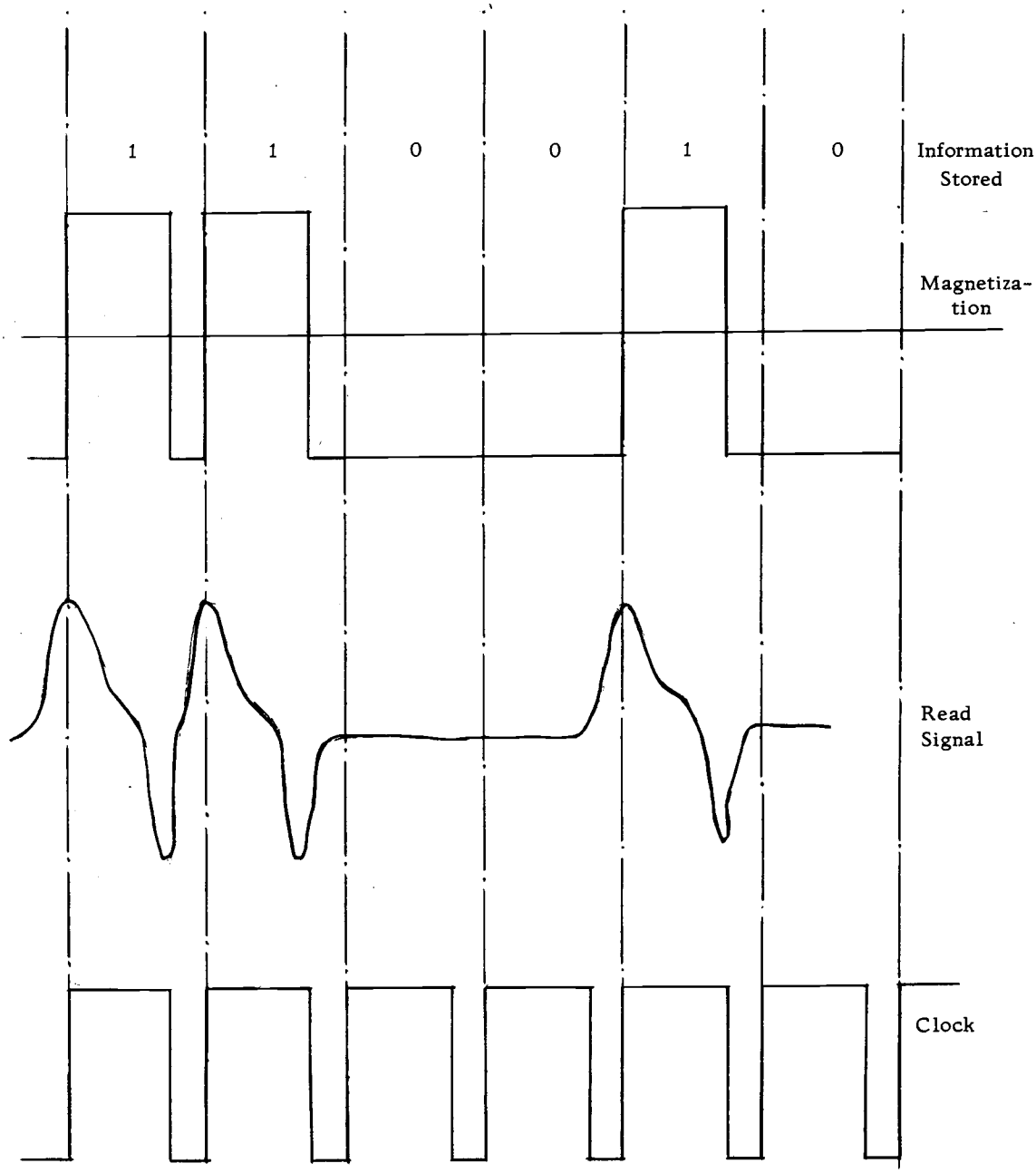


Figure 6. Wave forms for the RS recording.

back signal is concerned RS method is better than RZ because in RZ method the writing current reduces to zero so the flux change is from 0 to +Bmax, while in case of RS it is from -Bmax to +Bmax for a stored binary '1'. Since it is difficult to produce and maintain totally demagnetized state for a part of element length the output voltages produced by different recordings will not be equal for RZ method.

The rate at which information can be transferred to or from a magnetic surface depends on the density with which digits are packed along the surface and the velocity of the surface relative to the fixed heads. In addition to increasing the digit transfer rate an increase in packing density reduces the area of surface required to store a given amount of information, i.e., reduces the element length. There are two primary reasons which limit the packing density; element demagnetization and read head resolution. Both of these reduce the signal to noise ratio. As the elements are reduced in length and packed closer together the signal output is reduced by the interaction between adjacent digits. The major factor determining the resolution of the read head is the effective gap width. Obviously unless the gap width is less than the distance between two adjacent flux reversals on the surface the recorded information cannot be resolved. A head with a narrow gap has the disadvantages of decreased signal output and increased sensitivity to variations in head to surface spacing. Since in RZ method digit frequency is same as clock frequency while in NRZ method clock frequency is half the digit frequency NRZ recording

gives twice the digit transfer rate for the same density of flux reversals on the surface, requiring the response from the amplifiers extending from zero frequency up to half the digit frequency.

The Operation of Selection, Read and Write

The partial read, write and selection circuits are shown in Figure 7. All electronic selection systems are confined to making connections between a set of read-write heads and a single or smaller set of read-write amplifiers. In general these systems may be described as requiring the association of some addressing logic with each head. The system implemented as depicted in Figure 7 shows that for each transfer a set of 13 heads are to be selected. The selection logic, arranged on an x-y basis is a coincident in nature (two input decisions). One of the selection co-ordinates is the time axis and the other is chosen by appropriate word-track selection. In Figure 7 row selection is done by an appropriate clock signal and the column selection is made by selecting an appropriate word track PNP power transistor driver. The system operates as follows:

When the addressing current passes out of the base of one of the three PNP word track driver transistors, all the center points of the heads in that row are pulled to near ground. Since the driver PNP goes to saturation, current can now flow from ground through the transistor and through both legs of all the heads in that row and thence to

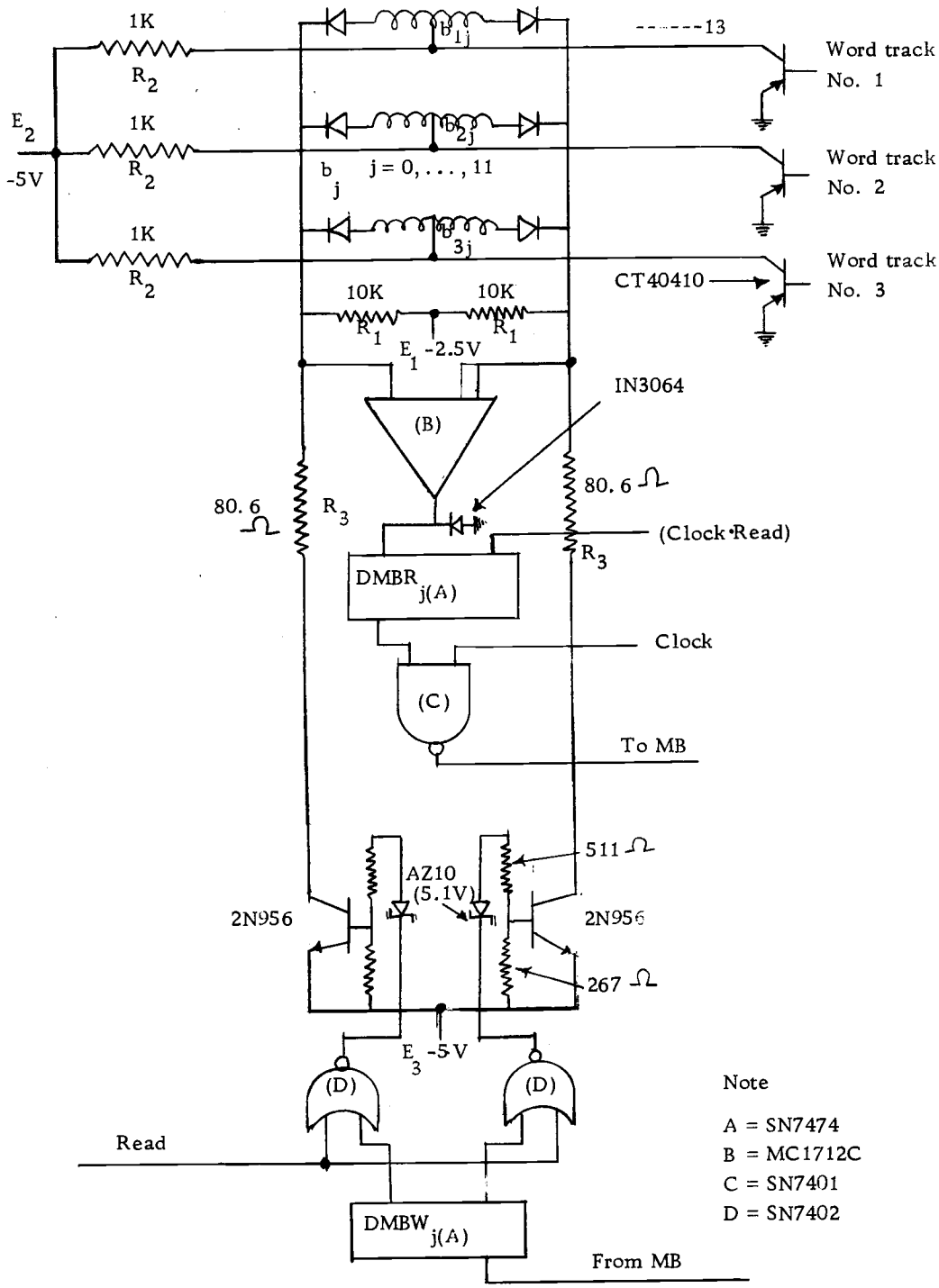


Figure 7. The partial read write and selection circuits.

the negative supply E1 through the resistor R1. Since both the diodes in the legs of the heads are forward biased any signal appearing across the heads will also appear across the corresponding R1 and so at the input of the read amplifier. Since bias source E2 is more negative than E1, the diodes in the legs of heads in other (not selected) rows are reverse biased and cannot transmit head signals to the read bus. Since R1 is very high it provides a small symmetrical biasing current source in the legs of the head to be read. Because approximately equal and opposite, but small, currents flow in the two legs of the head the net field produced is nearly zero and does not affect the recorded magnetization. In the element length where a binary '0' is stored there is no flux change and hence op amp senses no input voltage and output is clamped at near ground level by diode. In the element length where a binary '1' is stored there is a flux change in positive direction and so the op amp senses the positive voltage and output goes to the logic level of approximately 2.3 volts.

In order to write information on the medium one or the other write amplifier transistor is driven into saturation according to the state of the DMBW flipflop. This is achieved by a level shifter consisting of a Zener diode and resistors which change the TTL levels at the output of NOR gates into the excursions required at the base of the write amplifier to make it ON and OFF. This places the voltage E3 in series with R3 in one or the other leg of the head depending upon the

required binary '0' or '1' to be stored. Current passing from ground through one of the diodes via center point of the head and then through R3 and one of the saturated write amplifier transistors goes back to negative supply E3. The writing current passing through the head is controlled by R3 and E3 and is set to that value which gives the maximum read back signal. Both the write amplifier transistors remain off during read operation. The diode at the output of the reading op-amp is for the protection of the flipflop since negative excursion at the input of the flipflop must be limited.

General Operation

This paragraph will describe the general reading and writing process. To write on the disc file the DMA is loaded with the track address and EDMA is loaded with the word track No. from the accumulator. This is accomplished by the DEAL and the DMAW instructions. The DMAW instruction, which specifies the write mode also initiates the operation, enables the write amplifiers, inhibits the reading and generates the break request so that the first data word to be written is loaded into the DMBW.

A search process then begins whereby the track addresses are examined to determine when the track address passing under the write head is the correct address. This is accomplished in bit by bit comparison between DMA and the counter in the coincidence unit. When

the two addresses compare identically a signal is generated to enable the write operation and write amplifiers write the data held in DMBW in RS method of recording.

After the word is written the counter is incremented to the next sequential address and again break request is generated to fetch the next word from the memory and then similar process repeats until WCO is enabled which terminates the operation.

The read operation is similar to the write operation in that DMA and EDMA are loaded to specify the track address and word track No. by DEAL and DMAR instructions respectively from the accumulator. DMAR inhibits the writing and then search operation for correct address starts as before in writing case. When the correct address is found the track data is read in parallel into the DMBR and a break request is generated so that the data in the DMBR can be transferred to the computer memory. The operation thereafter is similar to the write mode except for the data transfer direction.

Timing Pulses

There is one timing track used by the interface to control the operation of the disc. On this track there are permanently recorded 6 microseconds wide pulses throughout the circumference except for a gap of approximately 200 microseconds. The gap provides physical reference for the starting of the track. The pulses though recorded

symmetrically are reshaped by a one-shot to be periodic but not symmetrical.

Detailed Logic Discussion

This section provides a complete logic discussion of the operation of the disc file. As a supplement to this discussion the reader is referred to Appendix A which gives an analysis of each IOT instruction and Appendix B which provides the mnemonic list.

Address Searching

The read or write operation is initiated upon the occurrence of the DEAL and the DMAW for writing or the DMAR for reading. The DEAL IOT instruction is decoded by the device selector to produce the IOT 6611 and 6614 pulses. The IOT 6611 pulse clears the EDMA and EMA and IOT 6614 pulse loads these registers from the PDP-8/L accumulator. The EDMA bits are decoded to provide the word track No. selected by the program.

Assuming that there is a read operation the DMAR instruction is issued to start the operation. DMAR generates IOT 6601 and IOT 6602 which loads DMA with the track address to initiate search operation. After this DMA and the contents of the counter are compared by an exclusive NOR operation. When both are identical ADC is set by a pulse of one clock width out of the coincidence unit. ADC sets the

ACH flipflop. ACH(1) is ANDed with clock pulses to generate break request and at the same time the information read in DMBR is allowed to pass through to the MB. At the same time the parity bit generated by the 12 bits of information is checked with the parity bit stored for the particular word for the PER flipflop, in an exclusive NOR circuit. After the transfer counter is incremented by the next sequential pulse from the clock track. Before this DBR is already reset by Add-Accepted pulse from the computer so once again it is set by the ACH(1) ANDed with clock pulse and from then on the procedure repeates.

The read operation continues in this manner until all words specified by WC register have been written in memory. When this occurs WCO flipflop is set which sets the TRC and disables the DBR. Thus no further data break occurs. The TRC signal then generates an interrupt to notify the program that the transfer is complete.

Write

The DMAW instruction initiates the write mode by starting the address search operation as previously described, it also sets R/W flipflop to signify the write mode to the data break facility. The DMAW instruction also sets the DBR flipflop to generate a break request to load DMBW with the first word to be written. The PDP-8/L data break facility responds by generating B-Break signal in the Break cycle, which enables the Break enable flipflop with the signal BTS-3

in break cycle. Break enable flipflop when in set state enables the writing of the data. The parity is generated by the parity generator if odd number of 1's are present in the data and stored in the same manner and at the same time as the data is stored. By this time Add-Accepted pulse from the computer resets DBR, and the next transfer is done when the next clock comes up in the same way as in reading case.

The write operation continues in this manner until all words specified by the WC register have been written. When this occurs the WCO is set which resets the DBR. Thus no further data break occurs. WCO also sets the TRC flipflop which generates a skip condition or interrupt to notify the program that the write operation is completed.

IV. SYSTEM OPERATION AND EVALUATION

The power supplies for the disc and the interface should be turned on before the 'START' key of the computer is pressed to start the operation of the disc in order to enable the Initialize pulse to clear the registers and different flags.

The program initiates the operation of the designed disc system but once it is initiated the disc takes over the complete control. The designed system is compatible with the software provided by the computer manufacturer for their DF-32 disc system. The Appendix C shows one example of programming the disc and more information about programming the disc can be obtained from the PDP-8/L Computer manuals. One of the capabilities of the disc, which can be utilized in our department by the students is that the complete operating software (FOCAL, ODT, DDT . . . etc.) can be permanently stored on one of the word tracks so that the time consumed to load the memory with any software package by teletype, will be reduced because then all one has to do is call back the software from the disc into the core which consumes much less time than loading by teletype. If the PDP-8/L is equipped in future by another 4K of memory the interface does not require any additional hardware but slight modification.

Future Developments

1. Write lockout switches can be installed to store the datas or the software packages permanently.
2. Indicator lights can be installed for any error signal.
3. By providing another Device Selector and IOT generator (6631, 6632, 6634) and appropriate logic the disc interface can be made to handle the maintenance software, discless logic test and interface testing etc. of the manufacturer.
4. Since the data break option is now installed high speed tapes, drums or any peripheral equipment requiring high speed transfer could be connected.
5. The priority selection circuits for the devices connected with PDP-8/L can be installed in future.

Cost Estimation

The cost of the electronic components of the system is very low compared with the similar commercially available system. The cost of the major units excluding labor cost are:

Interface	Price $
Logic Circuits	100.00
Connector Boards	40.00
Miscellaneous	10.00
Total	150.00

BIBLIOGRAPHY

1. Digital Equipment Corporation. PDP-8/L User's Handbook. Maynard, Massachusetts, 1968. 206 p.

2. Digital Equipment Corporation. Introduction to Programming. PDP-8 Family. Maynard, Massachusetts, 1971.

3. Digital Equipment Corporation. Instruction Manual for DF-32. Maynard, Massachusetts, 1969.

4. Digital Equipment Corporation. PDP-8/L Maintenance Manual. Maynard, Massachusetts, 1968. Vol. I & II.

5. Digital Equipment Corporation. PDP-8/L Replacement Schematics. Maynard, Massachusetts, 1968.

6. Joseph K. Hawkins. Circuit Design of Digital Computer. John Wiley & Sons, Inc., New York 1968.

7. William Renwick. Digital Storage Systems. John Wiley & Sons, Inc., New York 1964.

8. R.K. Richards. Digital Computer Components and Circuits. D. Van Nostrand Company, Inc., Princeton, New Jersey. 1957.

9. Texas Instruments Incorporated. IC Catalog for Design Engineers.

APPENDICES

APPENDIX A

IOT INSTRUCTION ANALYSIS

Octal	Mnemonics	Operation
6601	DCMA	ORed with B-Initialize. (1) Clears TRC Flipflop. NED Flipflop. ADC Flipflop. ACH Flipflop. DRL Flipflop. PER Flipflop. (2) Clears the DMA disc memory Address Register.
6602		(1) Clears the Accumulator. (2) Clears the R/W Flipflop setting transfer direction to read. (3) Does ones transfer from the Accumulator to the DMA. (4) Clears WCO flipflop.
6604		(1) Clears the Accumulator. (2) Sets the R/W flipflop setting transfer direction to write.

Octal	Mnemonics	Operation
		(3) Does ones transfer from the Accumulator to the DMA.
		(4) Clears WCO flipflop.
		(5) Sets DBR flipflop.
6611	DCEA	(1) Clears disc extended memory address register. EDMA.
		(2) Clears extended address register EMA.
6612	DSAC	(1) Enables skip bus if ADC flipflop is set (used primarily in diagnostic programming).
		(2) Clears the Accumulator.
6614		(1) Does ones transfer from Accumulator bits 3 through 5 to the EDMA and DMA_{13}.
		(2) Does ones transfer from disc 'Status Register' to Accumulator bits 0 through 11.
6621	DFSE	(1) Enables skip bus if no error flags are up (Skip on no error).
6622	DFSC	(1) Enables skip bus if the TRC flipflop is set and computer MB bit 9 is a zero. (IOT 6622 used alone).
		(2) Enables clear bus if computer MB bit 9 is a one. (IOT 6622 used with IOT 6624).

Octal	Mnemonics	Operation
6624		(1) Does a ones transfer of current passing address in counter to Accumulator bits 0 through 11.

Microprogrammed IOT's.

6603	DMAR	Read Operation.
6605	DMAW	Write Operation.
6615	DEAL	Clears and loads EDMA.
6616	DEAC	Clears Accumulator, loads Accumulator with EMA.
6626	DMAC	Clears the Accumulator and loads it with the current passing address in the counter.

APPENDIX B

MNEMONICS CODES FOR THE DISC SYSTEM

Mnemonic	Name and Description
ACH	Address Compare and Hold Flipflop. (1) Cleared by IOT 6601 and also by WCO signal from PDP-8/L When cleared it a. Disables reading or writing on the disc, b. Signifies that the correct address has not yet been found, c. Does not allow the clock pulses to go beyond the counter, d. Does not allow DBR to set in read mode, e. Does not allow DBR to set after initiation in write mode (2) Set by ADC When set it signifies that after correct initial address each clock pulse is a valid sequential address and allows DBR to set in read or write mode operation.
ADC	Address Confirmed Flipflop. Cleared by IOT 6601, when set it indicates that the address search has been

completed and sets ACH.

DBR — Data Break Request flipflop. It signals PDP-8/L that the disc is ready to transfer data. Functionally,

(1) It is cleared by Add-Accepted pulse from PDP-8/L.

(2) In write mode initially set by IOT 6604 and thereafter by (ACH. Clock).

(3) In read mode it is set by (ACH. Clock).

(4) WCO signal clears it.

DMA — Disc Memory Address, Disc memory address register 13 bits long.

DMBW — Disc Memory Buffer-Write, Disc memory buffer writing register. 12 bits long.

DMBR — Disc Memory Buffer-Read, Disc memory buffer reading register. 12 bits long.

DRL — Data Request Late. This error flag indicates a timing problem between the disc and the computer.

EDMA — Extended Disc Memory Address Register (Word Track Selector).

EMA — Extended Memory Address Register. (for the extended memory for computer)

NED — Non-Existent Disc Flipflop. Cleared by IOT 6601 and set when program selects the wrong word track via

Accumulator.

PER — Parity Error Flipflop. Cleared by IOT 6601 and set when an odd number of ones are read in one word (13 bits--12 bits of data and a parity bit).

R/W — Read/Write, Transfer Direction Flipflop. Cleared by IOT 6602 for the Read mode. Set by IOT 6604 for the Write mode.

TRC — Transfer Complete Flipflop. It is cleared by IOT 6601 and set,when WCO is set,signifies that the last transfer of a block is completed.

WCO — Word Count Overflow Flipflop. It is cleared by IOT 6602 or 6604 and set by WCO signal from PDP-8/L.

APPENDIX C

The following program will write the contents of locations 0200-0374 on the disc and if there is any hardware error it will print out a question mark (?) on teletype.

Assembly Language Location	Octal Debugging Location	Content	Assembly Language Content
SUB	7600	4210	JMS WRT
	7601	7604	
	7602	0177	
	7603	0200	
	7604	0200	
/WRITE SUBROUTINE			
WRT	7610	0000	
	7611	1610	TAD I WRT
	7612	3350	DCA WC (7750)
	7613	2210	ISZ WRT
	7614	1610	TAD I WRT
	7615	3351	DCA CA (7751)
	7616	2210	ISZ WRT
	7617	1610	TAD I WRT
	7620	6615	DEAL
	7621	7200	CLA

Assembly Language Location	Octal Debugging Location	Content	Assembly Language Content
	7622	2210	ISZ WRT
	7623	1610	TAD I WRT
	7624	6605	DMAW
	7625	6622	DFSC
	7626	5225	JMP. -1
	7627	6621	DFSE
	7630	5022	JMP ERR (0022)
	7631	2210	ISZ WRT
	7632	5610	JMP I WRT
/ERR SUBROUTINE			
	0022	0000	AND 0000
	0023	7200	CLA
	0024	6046	TLS
	0025	1032	TAD 0032
	0026	6041	TSF
	0027	5026	JMP 0026
	0030	6046	TLS
	0031	7402	HLT
	0032	0277	?

Note: An identical program could handle data transfers for a read operation except that the DMAW instruction is replaced by the DMAR instruction.