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Zhiqing Zhang for the degree of Master of Science in Electrical and Computer Engineering presented on November 21, 2007.

Title: Architecture Design of Multiplexed Incremental Analog-to-Digital Converters

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Gabor C. Temes

Analog-to-Digital Data Converters (ADCs) used in instrumentation and measurements often require high absolute accuracy, including excellent linearity and negligible dc offset. Incremental data converters (IDCs) provide a solution for such measurement applications. Since IDCs are essentially delta-sigma ($\Delta\Sigma$) converters with reset operation before each conversion, they retain most of the advantages of conventional $\Delta\Sigma$ converters, and yet they are capable of offset-free and accurate conversion.

Most of the previous research on incremental converters is for single-channel and dc signal applications, where they can perform extremely accurate data conversion with more than 20-bit resolution. In this thesis, the operation and the performance of IDCs in both frequency and time domain is analyzed. Design techniques for implementing multiplexed IDCs to convert narrow bandwidth ac signals are discussed too. It incorporates the operation principles, modulator topologies, digital filter design and signal-to-noise ratio optimization methodology. The theoretical analysis is verified by simulation results.

Architecture Design of Multiplexed Incremental Analog-to-Digital Converters

by
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Director of the School of Electrical Engineering and Computer Science

Dean of the Graduate School

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Zhiqing Zhang, Author

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1 Introduction

1.1 Motivation

In today's industry and consumer electronic products, most of the computational and signal processing operations are based on digital forms. Since the signal from the physical world remains analog, data converters are needed both at the input and output ends of these systems in order to interface them with the internal digital signal processing (DSP) core. Typically, in such a system, an analog-to-digital converter (ADC) is used at the input node to convert the analog signal into a digital data stream, while at the output node, a digital-to-analog converter (DAC) transforms a digital output signal from the DSP into analog form. With the development of CMOS technology, the speed, accuracy and capability of digital integrated circuits is increasing each year, which requires the corresponding improvement of the converters associated with them.

Different types of ADCs are available covering a wide range of bandwidth and resolution requirements. Fig. 1.1 shows the most recent breakthrough on ADC performance in terms of resolution and bandwidth from 1997 to 2007. Oversampling delta-sigma ($\Delta\Sigma$) ADCs are the most popular architectures among various ADCs. Unlike Nyquist-rate converters, they can achieve very high resolution and linearity without putting priming the requirements on the element matching in analog circuitry.

ADCs used in instrumentation and measurements often require high absolute accuracy, including excellent linearity and negligible dc offset.

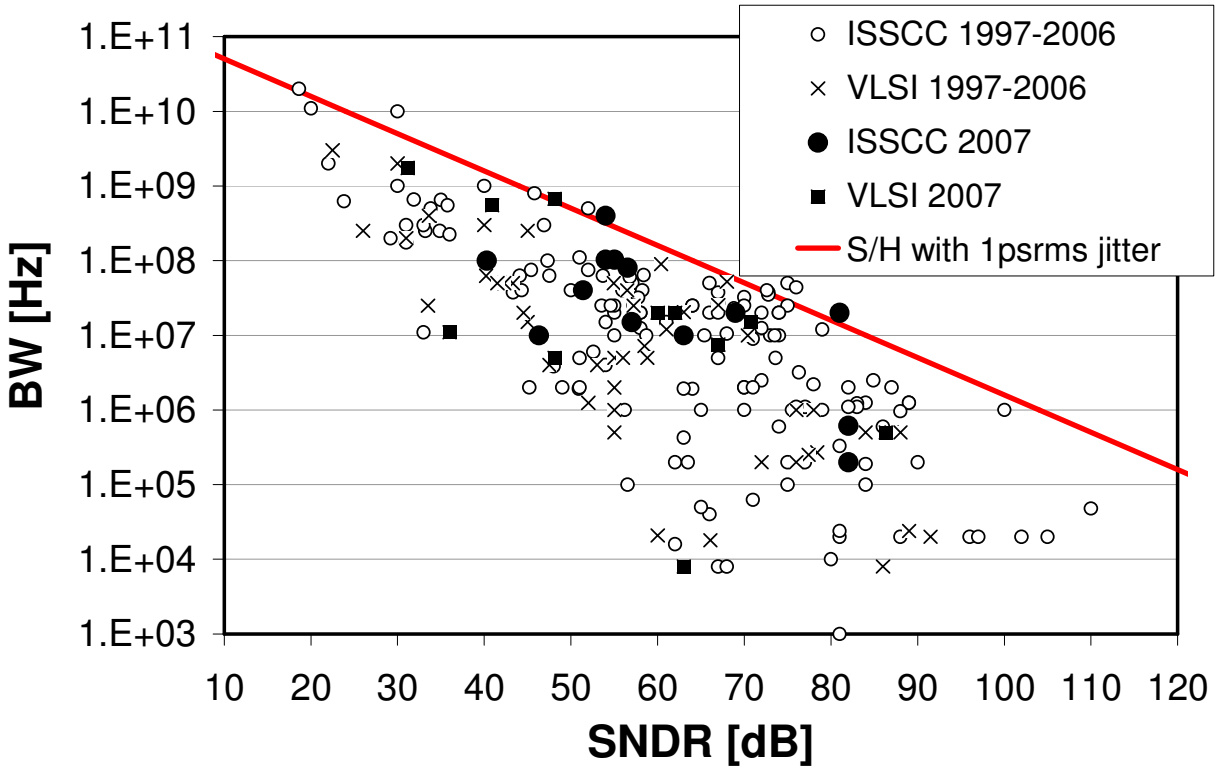


Figure 1.1. ADC Performance in terms of BW and SNDR [1].

Incremental data converters (IDCs) provide a solution for such measurement applications. Since IDCs are essentially ΔΣ converters with reset operation before each conversion, they retain most of the advantages of conventional ΔΣ converters, and yet they are capable of offset-free and accurate conversion.

1.2 Contribution

Most of the research to date on incremental converters deals with single-channel and dc signal applications, where they can perform extremely accurate

data conversion with more than 20-bit resolution. In this thesis, the operation and the performance of IDCs both in the frequency and in the time domain are analyzed. Design techniques for implementing multiplexed IDCs to convert narrow bandwidth ac signals are discussed too. This thesis incorporates the operation principles, modulator topologies, digital filter design and noise optimization methodology. The theoretical analysis is verified by simulation results.

1.3 Thesis Organization

Chapter 2 briefly compares different data converter architectures for instrumentation and measurement applications. The fundamentals of incremental converters, first-order and higher-order architectures and their operations are discussed in detail.

Chapter 3 prescribes a design technique for multiplexed IDCs in terms of quantization noise shaping. The modulator architecture design, the decimation filter design, and the simulation results are presented.

Chapter 4 introduces a design methodology which provides the best possible signal-to-noise performance for the complete data converter system.

Finally, Chapter 5 concludes the thesis and summarizes the research work discussed in the previous chapters.

2 Overview of Incremental Data Converters (IDCs)

2.1 Comparison of Different Types of ADCs

Analog-to-Digital converters (ADCs) used in instrumentation, measurement and sensor applications often require high dynamic range. For example, a photodiode produces signal currents between 1pA and 1μA, spreading across 6 decades of dynamic range. Power management and biomedical signal measurement applications may require a similar dynamic range. In addition to the high resolution demand, these converts also require high absolute accuracy, including excellent linearity and negligible dc offset. In portable and battery-powered systems, power dissipation and IC area-consumption are also very important. However, in most of these applications the converters operate in a typically low bandwidth (no more than a few kHz), which allows a flexible trade-off between bandwidth and power consumption.

A possible solution for such measurement applications is to use Nyquist-rate ADCs. However, these converters have some disadvantages. One of them is that the linearity and accuracy of Nyquist-rate converters relies on precise and large analog components used in the implementations, which take a lot of layout area and are not suitable for low-voltage analog circuits. Another disadvantage is that they usually require a very small element mismatch. For example, for an *N*-bit resistor string converter, to achieve an effective number of bits of about 16, the matching accuracy is restricted to about 0.002%, which is almost unachievable in

practical conditions [2]. The third disadvantage of such converters is the long conversion time. When a resolution of more than 16bits is required, the integrating one may be the only viable solution among Nyquist-rate converters. However, this type of converter requires at least $2^{n_{bit}}$ clock periods to complete one conversion in order to reach an n_{bit}-bit resolution, and hence it is too slow for most applications.

A ΔΣ ADC is another possible candidate for high accuracy measurements, since it can achieve high-resolution and high dynamic range conversion. Classical ΔΣ ADC is operating continuously to convert a running analog waveform to a digital waveform with a sampling frequency much higher than the Nyquist rate. Each output utilizes all preceding input values, which needs memory elements in its structure. Compared to a Nyquist-rate converter, such a converter does not have high matching accuracy requirements on analog components. It can tolerate offset and gain errors as well.

Since there is no one-to-one correspondence between the input and output samples, ΔΣ ADC's performance can only be evaluated through the comparison between the input and output wave forms either in the time domain or in the frequency domain. On the contrary, a high absolute accuracy is needed in dc or low frequency signal measurements. It is very important for such converters to be capable of carrying out sample-by-sample conversion with very low linearity, offset and gain error.

As a third option, in incremental converter provides the most feasible solution for high-precision dc measurement applications. As they retain most of the advantages of conventional ΔΣ converters, they are capable of offset-free and accurate conversion. In the following sections in this chapter, we will analyze the properties of the incremental converter in detail.

2.2 First-Order IDCs

2.2.1 Time Domain Analysis

The first CMOS incremental converter has been introduced in [3] in 1987, and was named "incremental ΔΣ converter". This converter can be implemented with 4μm CMOS technology. The block diagram of this converter is illustrated in Fig. 2.1. The circuit is relatively simple: it mainly contains an integrator, a comparator, and a counter.

The operation of the converter is described in the following steps:

1. At the beginning of each conversion in the cycle, all the memory elements

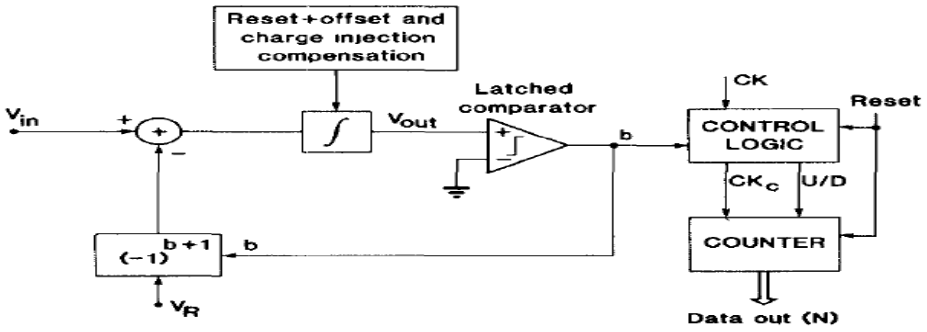


Figure 2.1. The block diagram of the first-order IDC [3].

are reset, including the integrator and the counter.

2. The converter performs the integrating operation for a fixed number N ($N = 2^{n_{bit}}$) clock periods. Here, n_{bit} is the required resolution in bits. Once the integration of the analog input signal exceeds zero, the comparator output becomes 1, then $-V_{ref}$ will be added to the input of the integrator.

3. After one conversion cycle, the whole system is reset again and repeats the above steps for the next one.

As described in [4], in step 2, after N clock periods, the output from the analog integrator would become

$$V = NV_{in} - N_{out}V_{ref} \ . \qquad (2.1)$$

Here, N_{out} is the number of clock periods when feedback is applied. In order to keep the stability of the ΔΣ loop, output V has to satisfy $-V_{ref}/2 < V < V_{in} \leq V_{ref}/2$. From the above relationships, it is

$$N_{out} = 2^{n_{bit}} (V_{in}/V_{ref}) + \varepsilon \ , \qquad (2.2)$$

where $\varepsilon \in [-V_{ref}, V_{ref}]$. Clearly the digital form of the input analog signal is simply $N_{out}/2^{n_{bit}}$, and the quantization error is $\varepsilon / 2^{n_{bit}}$.

2.2.2 Z–Domain Analysis

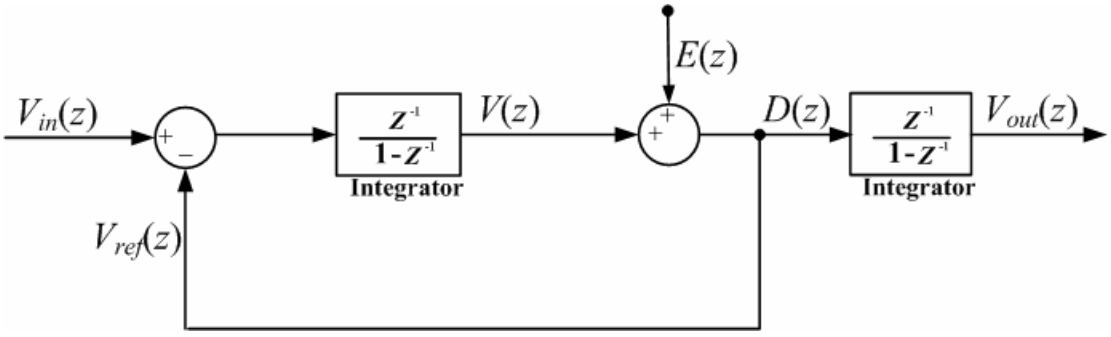


Figure 2.2. The block diagram of the first-order IDC [3].

The discrete-time model for a first-order IDC is illustrated in Fig. 2.2. Here, $V_{in}(z)$ is the analog input, $V(z)$ is the output of the integrator, $D(z)$ is the output of the quantizer, $E(z)$ is the quantization noise and $V_{out}(z)$ is the output after the digital counter. To simplify the analysis, V_{ref} is assumed to be equal to 1 and the quantization noise $e(n)$ in the range of [-1,1].

In the z domain, V_{in}, D and V have the following relationships:

$$V_{in}(z) - D(z)V_{ref}\left(\frac{z^{-1}}{1-z^{-1}}\right) = V(z),$$

$$V(z) + E(z) = D(z) \ .$$

Then, $D(z)$ follows as

$$D(z) = V_{in}(z)z^{-1} + E(z)(1-z^{-1}).$$

Without the reset section, such an IDC works like a classic first-order ΔΣ ADC. The signal transfer function (STF) is nothing but a clock period delay:

$$STF(z) = z^{-1},$$

and the noise transfer function (NTF) is a high-pass filter:

$$NTF(z) = 1 - z^{-1}.$$

One can easily find the relationship between the signals of the overall system:

$$V_{out}(z) = V_{in}(z)(\frac{kz^{-1}}{1 - z^{-1}}) + kE(z).$$

The above equation can be expanded as

$$V_{out}(z) = kV_{in}(z)(z^{-1} + z^{-2} + z^{-3} + ...) + kE(z). \qquad (2.3)$$

Since this converter is only active for N clock periods because of the reset operation, Eq. (2.3) can be simplified as

$$V_{out}(z) = kV_{in}(z)\sum_{s=1}^{N} z^{-s} + kE(z). \qquad (2.5)$$

In the time domain, $v_{out}(n)$ can be expressed as

$$v_{out}(n) = k\sum_{t=1}^{N} v_{in}(n-t) + ke(n) = kN \cdot v_{in} + ke(n). \qquad (2.6)$$

If the constant gain k is equal to $1/N$, then it is easy to conclude that after N integration steps, the quantization error at the end of each conversion cycle is $e(n)/N \in [-1/N, 1/N]$, which matches the results in Eq. (2.2) from the time domain analysis.

Eq. (2.6) shows that a first-order incremental ΔΣ ADC has to run for at least $2^{n_{bit}}$ clock cycles to achieve in n_{bit}-bit resolution. Thus the conversion rate is much slower than the system clock frequency, which is the fundamental drawback of the IDCs compared to conventional ΔΣ converters.

As mentioned above, the IDC has a structure similar to that of a conventional ΔΣ converter, but it operates differently. The differences are listed next:

- The conversion does not operate continuously. All the memory elements are reset after each conversion.
- To gain an n_{bit}-bit resolution, the converter needs to operate for at least $2^{n_{bit}}$ clock periods.
- The structure of the decimation filter is simpler. For the first-order ΔΣ incremental converter, the filter can be realized with a counter.

The successful development of the first CMOS incremental converters reveals their capability in instrumentation and measurement applications. Based on the design of [3], a lot of research has been done to improve the performance of IDC. The improvements include higher resolution, higher conversion rate and lower power consumption and smaller layout area.

2.3 Extension to Higher-Order IDCs

In [5], a second-order IDC has been introduced. The structure of this IDC incorporates a second-order ΔΣ modulator and the operation of this IDC is similar to the first-order one. The most significant improvement over previous designs is that this IDC reduces the conversion time to approximately $2^{n_{bit}/2}$ clock cycles instead of $2^{n_{bit}}$ while still achieving an n_{bit}-bit resolution.

The design theory of higher-order IDCs was discussed in [4]. In order to improve the performance, the possibility to extend the IDC's architecture from first-order to higher-order was discussed in terms of design complexity, resolution, conversion time and so on. The authors of [4] analyzed a third-order IDC's operation in the time domain. The basic block diagram of this converter is shown in Fig. 2.3, which contains a third order cascade-of-integrator-with-feedforward (CIFF) ΔΣ modulator (shown in Fig. 2.4) a digital decimation filter, and a control circuit.

After all the memory elements in the modulator and the digital filter are reset, the input signal V_{in} is applied to the input of the first integrator to start one conversion. Then the output of the first integrator after N clock periods can be found as

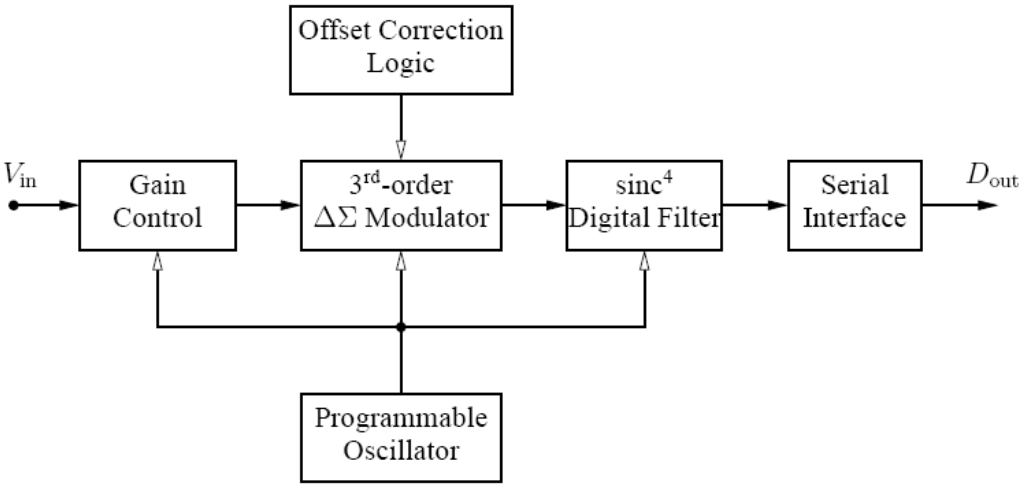


Figure 2. 3. Block diagram of a third-order IDC.

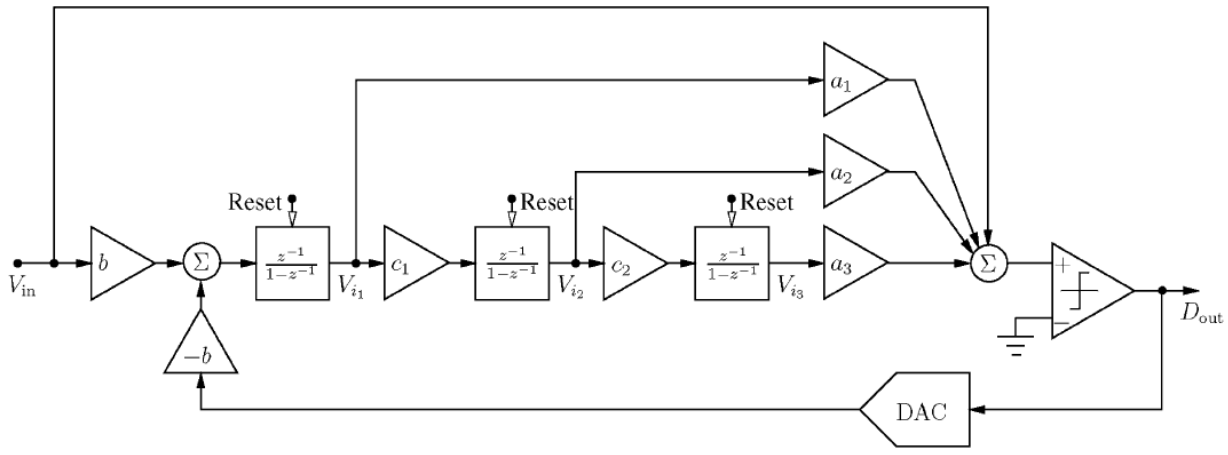


Figure 2.4. Third-order CIFF architecture.

$V_{i1}[0] = 0$

$V_{i1}[1] = b(V_{in}[0] - d_0 V_{ref})$

$V_{i1}[2] = V_{i1}[1] + b(V_{in}[0] - d_1 V_{ref})$

$= b(V_{in}[0] + V_{in}[1] - d_0 V_{ref} - d_1 V_{ref})$

…

$$V_{i1}(N) = b\sum_{k=0}^{N-1}(V_{in}[k] - d_k V_{ref}),$$

where $d_k = \pm 1$ is the output from the quantizer.

It is easy to follow the above steps to find the output signals at the second and the third integrators are, respectively

$$V_{i2}(N) = c_1 b\sum_{L=0}^{N-1}\sum_{k=0}^{L-1}(V_{in}[k] - d_k V_{ref}),$$

$$V_{i3}(N) = c_2 c_1 b\sum_{M=0}^{N-1}\sum_{L=0}^{M-1}\sum_{k=0}^{L-1}(V_{in}[k] - d_k V_{ref}). \qquad (2.7)$$

Since there is one clock cycle delay between each integrator, N, M and L have to satisfy $L = M - 1$, and $M = N - 1$.

If V_{in} is a constant, after rearranging Eq. (2.7), one can get

$$V_{i3}(N) = c_2 c_1 b(\frac{N(N-1)(N-2)}{3!}V_{in} - \sum_{M=0}^{N-1}\sum_{L=0}^{M-1}\sum_{k=0}^{L-1} d_k V_{ref}). \qquad (2.8)$$

Since the input of the quantizer, $V_{i3}(N)$, must be limited by $\pm V_{ref}$ to stabilize the $\Delta\Sigma$ loop, we have

$$-V_{ref} \le c_2 c_1 b(\frac{N(N-1)(N-2)}{3!}V_{in} - \sum_{M=0}^{N-1}\sum_{L=0}^{M-1}\sum_{k=0}^{L-1} d_k V_{ref}) \le V_{ref} \,. \quad (2.9)$$

Eq (2.9) can be simplified as

$$-\frac{3!}{c_2 c_1 b \cdot N(N-1)(N-2)}V_{ref} \le V_{in} - \frac{3!}{N(N-1)(N-2)}\sum_{M=0}^{N-1}\sum_{L=0}^{M-1}\sum_{k=0}^{L-1} d_k V_{ref} \le \frac{3!}{c_2 c_1 b \cdot N(N-1)(N-2)}V_{ref}$$

Since N is usually a large number ($N > 100$), then after N clock period, the digital representation of V_{in} is

$$D_{out} = \frac{V_{in}}{V_{ref}} \approx \frac{3!}{N(N-1)(N-2)}\sum_{M=0}^{N-1}\sum_{L=0}^{M-1}\sum_{k=0}^{L-1} d_k V_{ref} \,. \quad (2.10)$$

In an ideal ADC, the least significant bit (LSB) voltage can be defined as

$$| D_{out} - V_{in} | \le \frac{V_{lsb}}{2} \,. \quad (2.11)$$

One can derive the equivalent VLB voltage and the equivalent number of bits (ENOB) from Eqs. (2.10) and (2.11) as

$$V_{lsb} = \frac{2 \cdot 3!}{c_2 c_1 b \cdot N(N-1)(N-2)}V_{ref} \,, \quad (2.12)$$

$$n_{bit} = \log_2(\frac{2V_{ref}}{V_{lsb}}) = \log_2(c_2 c_1 b \frac{N(N-1)(N-2)}{3!}) \,. \quad (2.13)$$

Compared to first-order IDCs, the most important progress of higher-order IDC is that it reduces the conversion time significantly. For example, in order to achieve 16-bit resolution, third-order IDCs only need to be active for approximately 100 clock cycles for one conversion, while first-order IDC's have

to be on for approximately 2^{16} = 65536 clock cycles. Such an amount of time reduction also implies that the power consumption of third-order IDCs will be greatly decreased with respect to first-order IDC's.

It is also possible to analyze the performance of third-order IDCs in the z domain with a technique similar to that we used for the analysis of first-order IDCs. We will describe the analysis of higher-order IDCs in z domain in the following chapter.

The authors of [6] presented a low-power high accuracy IDC based on the design technique described above. The measurement shows that this IDC can achieve more than 22-bit resolution, which confirms the theory developed in [4].

3 Multiplexed IDCs

The research on IDCs so far has proved their feasibility for DC signal conversion. However, their potential for low-frequency ac signal conversion is still under investigation. Moreover, since IDCs are active only for a fixed number of clock periods during each data conversion, they can be easily multiplexed. In this chapter, we will discuss design issues for multiplexed IDCs. The modulator architecture, digital decimation filter and some simulation results will be presented.

3.1 Need for Multiplexed IDCs

There are some applications which require the ADCs to be able to perform multi-channel data acquisition where many (N) low frequency analog signals have to be converted into a digital form. These analog signals have narrow bandwidths (typically, $f_B < 3$ kHz).

The parallel analog-to-digital conversion of several channels carrying low frequency signals can be performed in various ways:

- Through parallel ADCs with a shared decimation filter. However, this architecture requires replicating all memory elements, which consumes a large chip area and large power consumption.

•Through multiplexed ADCs and filters using replicated storage elements (capacitors and registers). Also in this case, the chip area is large and the structure is subject to inter-channel interference.

•Through multiplexed and reset incremental converters and decimation filters. With this option, all the data conversions are operated in one ADC, which takes much less power consumption and chip area. Then this is the optimal choice.

Multiplexed IDCs can be utilized in power management (voltages, currents, temperatures, etc.), engine control (speed, fuel mix, etc.) and biomedical signal processing (EKG, EEG, etc.). Desirable requirements of the IDC architecture are:

1) large signal-to-quantization noise ratio (SQNR＞90 dB).

2) small chip area (e.g., 0.5 mm^2 for the complete ADCs).

3) low power consumption (＜2 mW).

3.2 Operation of Multiplexed IDC

As being described in Chapter 2, an IDC is essentially a ΔΣ ADC which is initially reset and then operated for a predetermined number *M* of clock cycles. The *N*thoutput is available after the *M*th clock cycle of the *N*th conversion cycle. A new cycle may start either immediately after the reset, or after an inactive (dormant) period. This reset operation makes it possible to share a single IDC

among several channels, without the need to replicate all memory elements, which is required when multiplexing a traditional ΔΣ ADC.

Fig. 3.1 shows the system diagram of the multiplexed IDC, in which all the channels share the same ΔΣ modulator and decimation filter. Fig. 3.2 shows instead the k^{th} channel of such structure. When phase F_k is high, the k^{th} channel is active for the data conversion. The input signal u_k is applied to the ΔΣ modulator first and then is converted to a bit stream as y_k, which goes into the decimation filter next. The last sample from the decimation filter output is the desired digital equivalent of u_k. After one conversion is completed, both the ΔΣ modulator and the decimation filter are reset to be ready for the next new conversion. Fig. 3.3 schematically shows the five signals u_k, x_k, y_k, w_k, v_k indicated in Fig. 3.2 for the k^{th} channel of the multiplexed IDC architecture.

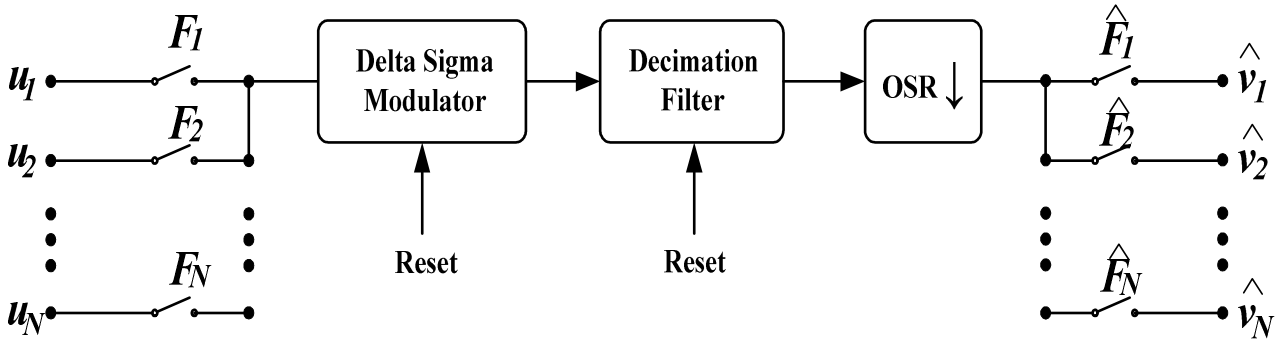


Figure 3.1. Block diagram of a third-order IDC.

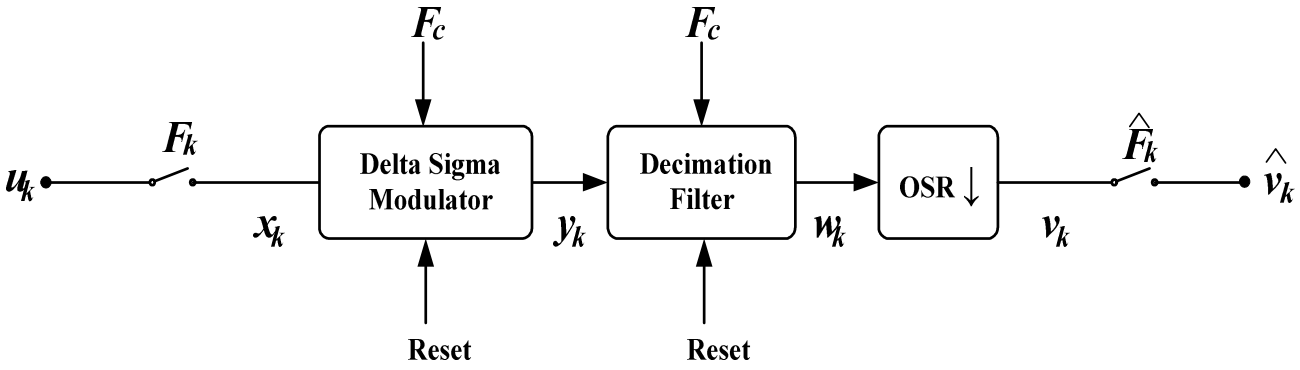


Figure 3.2. Block diagram of a third-order IDC.

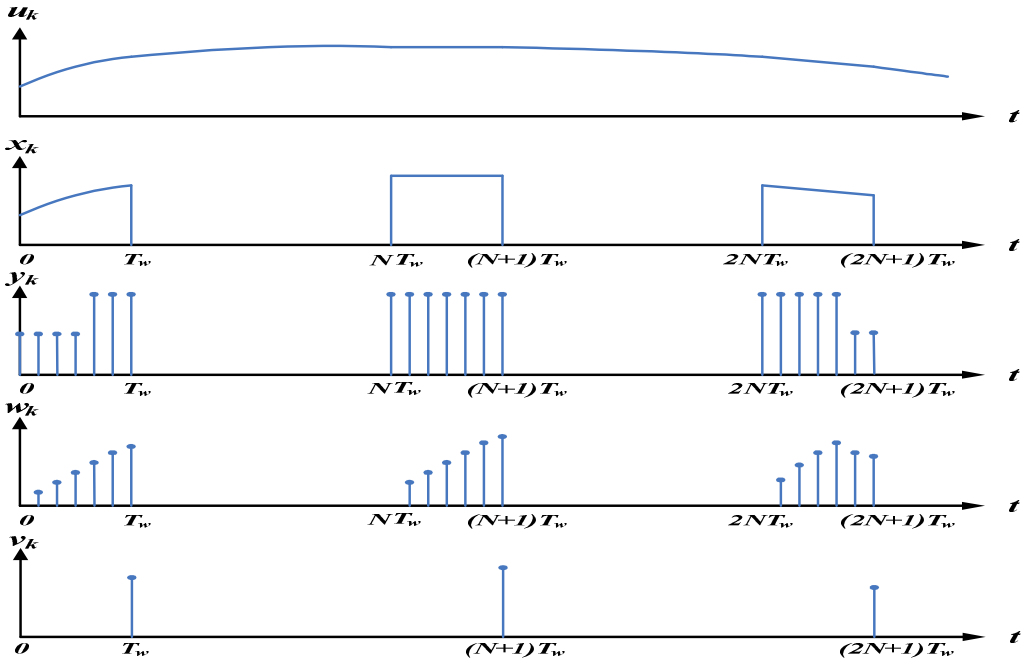


Figure 3.3. Schematical plot of the signals in the k^{th} channel.

In this N-channel structure, each channel carries a signal with a bandwidth f_B, which typically does not exceed a few kHz. The time slot devoted by the ADC to each channel is denoted by T_w, which can be considered as the duration time of

a temporal window multiplying the input analog signal in each conversion cycle. The Nyquist theorem thus requires that the following constraint be met: $NT_w < 1/2\, f_B$.

During each conversion cycle, the ΔΣ modulator and the decimation filter are functional for n clock periods. For an L^{th} order IDC, at low frequencies, the SQNR is proportional to n^L, where n is the number of clock periods in the window defined above [4]. Thus, $n = f_C T_w$, f_C is the clock frequency, must be sufficiently large in order to achieve the desired SQNR.

3.3 Architecture Consideration

There are four main types of ΔΣ architectures: cascade-of-integrator-with-feedback (CIFB), cascade-of-resonator-with-feedback (CRFB), cascade-of-resonator-with-feedforward (CRFF), and cascade-of-integrator-with-feedforward (CIFF), which is of particular interest. Fig. 3.4 shows the block diagram of a second-order CIFF architecture. It contains a series of cascaded integrators with adjustable coefficients, and the output of each integrator feeds to the input of the quantizer. It is also important to notice that there is a single path existing between the input signal and the input of the quantizer. Moreover, there is only one feedback path from the quantizer, which connects the input of the first integrator and the output of the ΔΣ modulator. The small number the feedback paths makes it easy to realize this particular structure.

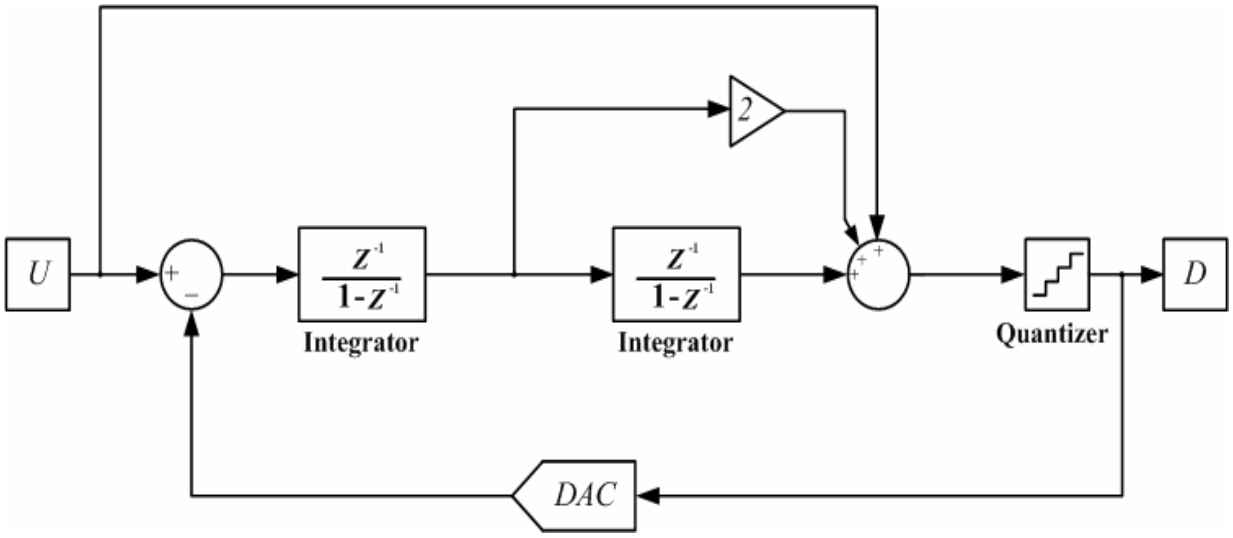


Figure 3.4. Block diagram of a second-order IDC.

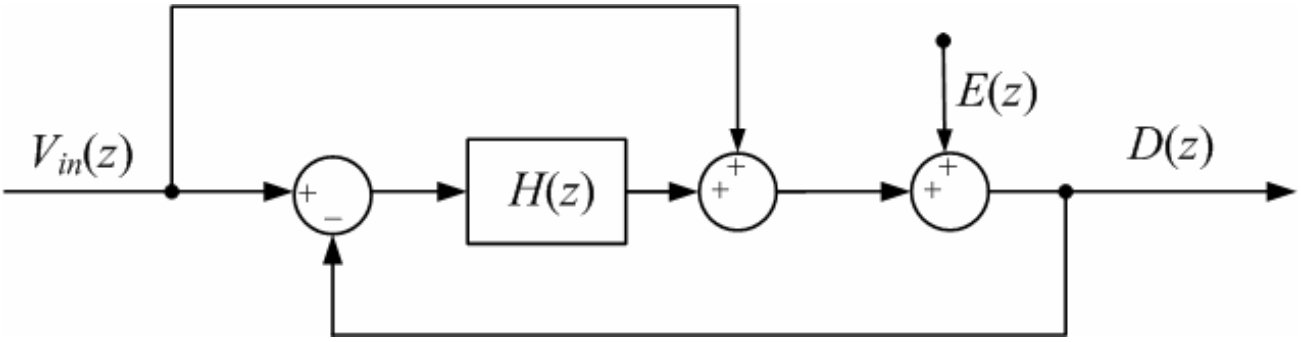


Figure 3.5. Simplified discrete time model of CIFF structure.

With careful coefficient scaling, the coefficient on the path between the input signal and the input quantizer can be normalized to 1. Because of this feed-forward path, then the discrete model of the CIFF architecture can be simplified as in Fig. 3.5. It is easy to obtain the relationship between the signals at the input $V_{in}(z)$, the quantization noise $E(z)$ and the output $D(z)$:

$$V_{in}(z)+[V_{in}(z)-D(z)]H(z)+E(z)=D(z). \tag{3.1}$$

Eq. (3.1) can be simplified as

$$V_{in}(z)+E(z)/(1+H(z))=D(z), \tag{3.2}$$

where $H(z)$ is the loop filter transfer function, which normally writes $H(z)=1-\frac{1}{(1-z^{-1})^{La}}$. L_a is the order of the modulator.

Then the STF and NTF of the modulator are, respectively,

$$STF(z)=1, \tag{3.3}$$

and

$$NTF(z)=1/(1+H(z))=(1-z^{-1})^{La}. \tag{3.4}$$

From the equations above, one can find that the loop filter in the CIFF structure shapes the quantization noise from the quantizer but does not alter the input signal. The direct path between the input signal and the quantizer minimizes the non-ideal effects of the integrators, such as: nonlinearity, limited output swing [7] [8]. For our specifications, the third-order CIFF modulator

shown in Fig. 2.4 may be used with the coefficients a = [1. 0398 0.4870 0.0967], b = 1, c = [1 1]. In order to increase the signal to noise ratio and also to improve the stability of the loop, a 5-level quantizer is adopted. The STF is 1, and the NTF is given by equation

$$NTF(z) = \frac{(1-z^{-1})^3}{1-1.9062z^{-1}+1.4074z^{-2}-0.3506z^{-3}}. \qquad (3.5)$$

Fig. 3.6 shows the power density spectrum of its NTF.

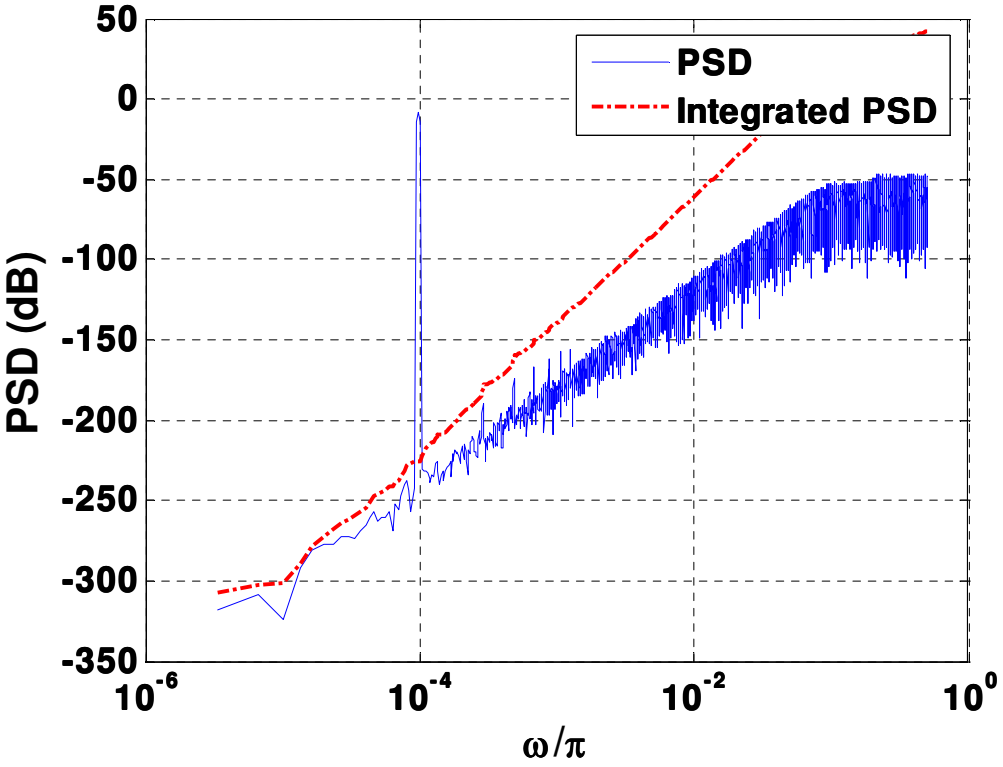


Figure 3.6. PSD of the delta-sigma loop output.

3.4 Digital Filter Design

With the reset operation, the IIR decimation filter $H_f(z)$ is only active for n clock periods, becoming an FIR digital filter $H_f(z) = h_0 + h_1 z^{-1} + h_2 z^{-2} + \ldots + h_n z^{-n}$ [9], which has been illustrated in the previous chapters. Since the modulator with CIFF structure has a signal transfer function (STF) equal to 1, the gain of the digital filter must be sufficiently flat up to signal bandwidth to minimize the distortion of the input signal. This requires $H_f(z) = 1$ for $z \cong 1$.

In addition, this filter must suppress the quantization noise introduced by the ADC and the replicas around $f_w = 1/T_w$. The noise-shaping of the ΔΣ modulator high-pass filters the quantization noise and keeps most of the quantization noise out of the signal band, which is much lower than the sampling rate of the system. This requires $H_f(z)$ to be a selective low-pass filter in order to remove the residual quantization noise at higher frequencies after noise-shaping. Also n should be large enough to achieve the specified SQNR.

The decimation filter can be realized in various ways. In [3], a counter was used as the digital filter, rather than a decimating low-pass filter, as is typical in the over-sampling converter. A 3rd-order digital Sinc filter was adopted in [6]. In [4], digital decimation filter design techniques for DC measurement were discussed.

3.4.1 Cascaded Digital Integrators

For the conversion of a low frequency signal the decimation filter could be simply implemented by cascading four accumulators. As already discussed in the previous chapters, if the IDC incorporates an L_ath CIFF structure as the modulator, then the converter has a transfer function:

$$D(z) = V_{in}(z) + E(z)(1 - z^{-1})^{La}.$$

Then $V_{out}(z)$, the output of the digital filter, can be expressed as

$$V_{out}(z) = V_{in}(z)H_f(z) + E(z)(1 - z^{-1})^{La} H_f(z). \qquad (3.6)$$

For a third-order IDC with CIFF structure, the digital filter can be simply implemented using three cascaded digital integrators, with a transfer function $H_f(z) = (\frac{1}{1 - z^{-1}})^3$. Then the overall transfer function of such an IDC is

$$V_{out}(z) = V_{in}(z)(\frac{1}{1 - z^{-1}})^3 + E(z). \qquad (3.7)$$

If the cascaded integrators operate continuously, their multiple poles at $z = 1$ will introduce infinite dc gain on the input signal and force the system to become unstable. However, in IDCs, the IIR decimation filters only operate for a finite number n of clock cycles, essentially becoming an FIR filter. Then $H_f(z) = (\frac{1}{1 - z^{-1}})^3$ can be expanded as

$$H_f(z) = \sum_{m=0}^{n-1} C_m z^{-m},\ C_m = \frac{1}{2}(m+1)(m+2). \qquad (3.8)$$

From Eq. (3.8), the dc gain of $H_f(z)$ is $\sum_{m=0}^{n-1}\frac{1}{2}(m+1)(m+2)$, which can be simplified as $\frac{(n+2)(n+2)n}{3!}$. To cancel the distortion on the input signal from this dc gain, a coefficient *k* would be introduced with the value of $\frac{3!}{(n+2)(n+2)n}$. Eq. (3.7) then becomes:

$$V_{out}(z) = V_{in}(z) + E(z)k \text{ , where } k = \frac{3!}{(n+2)(n+2)n}.$$

This equation indicates that after *n* clock cycles, the equivalent value of the LSB can be found as

$$V_{lsb} = \frac{(n+2)(n+2)n}{2 \cdot 3!} V_{ref}, \qquad (3.9)$$

which is similar to the results in Chapter 2.

However, the analysis above has only taken the dc signal into consideration. If the input signal is a low frequency signal, then with the poles at $z = 1$, such a filter design would be sensitive to any dc offset. This problem can be overcome by pushing the poles inside the unit circle rather than on the unit circle in z domain. By setting the poles at $z_p = 0.95$, this design is much more stable than the cascade of three accumulators without any damping factor.

To cancel the out of band quantization noise, the zeros at $z_z = -1$ can be introduced into the filter as well. Then the transfer function $H_f(z)$ is as

$$H_f(z) = (k\frac{1+z^{-1}}{1-z_p^{-1}})^3, \tag{3.10}$$

where k is the coefficient making $H_f(z)$ equal to 1 at $z=1$.

3.4.2 Other Digital Decimation Filters

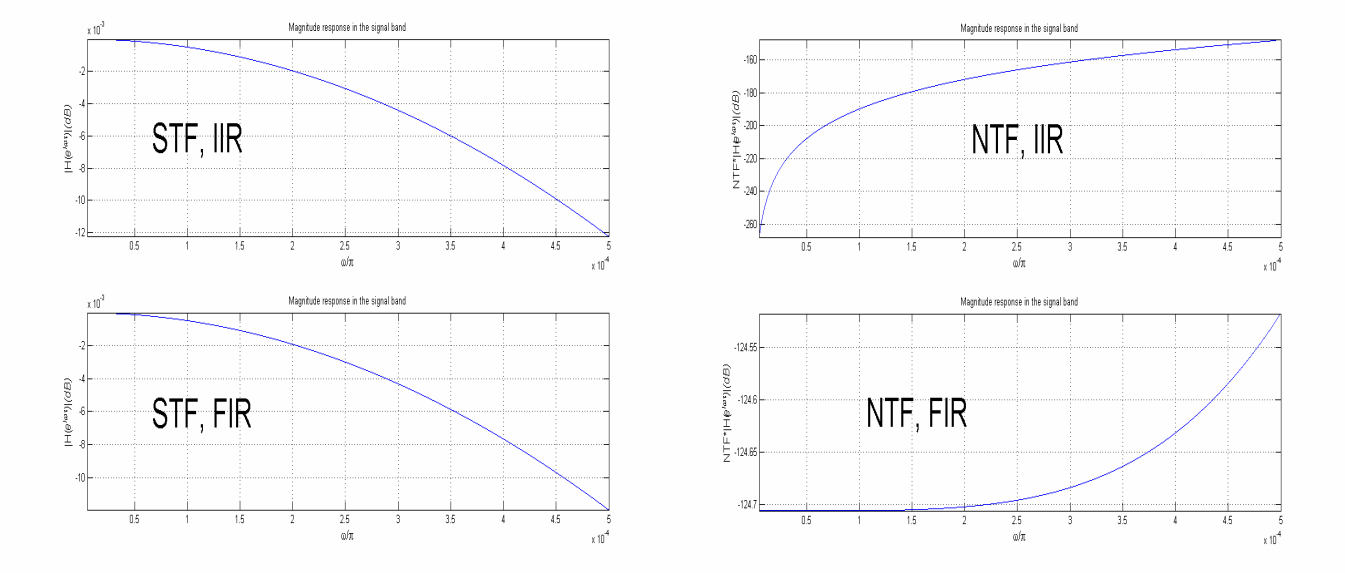
A Butterworth filter is designed to have a frequency response which is as flat as mathematically possible in the passband. Since maximum flatness of the decimation for IDC in the signal band is desirable, a Butterworth filter is able to be adopted as the second option. For our specifications, a fourth-order Butterworth filter may be used with a transfer function

$$H(z) = 10^{-6}\frac{0.065+0.26z^{-1}+0.39z^{-2}+0.26z^{-3}+0.065z^{-4}}{1-3.92z^{-1}+5.75z^{-2}-3.75z^{-3}+0.92z^{-4}} \tag{3.11}$$

An L_ath-order Sinc filter is another option (L_a is the order of the modulator), which was illustrated in [6]. However, the droop in the passband of this type filter fails to satisfy the requirements explained at the beginning of this section, which will introduce great distortion on the input signal.

Some simulations have been done to compare the performance between cascaded-damped integrators and Butterworth filter, which has the transfer function in Eq. (3.10) and Eq. (3.11). Here, STF represents the overall signal transfer function $STF(z)H_f(z)$, NTF represents the overall noise transfer function $NTF(z)H_f(z)$ and IIR represents the impulse response of the transfer function. From Fig. 3.7 and Fig 3.8, we can notice that, at low frequency, cascaded-damped

integrators shape the quantization noise more aggressively than a Butterworth filter, while the Butterworth filter has much less droop in the signal band.

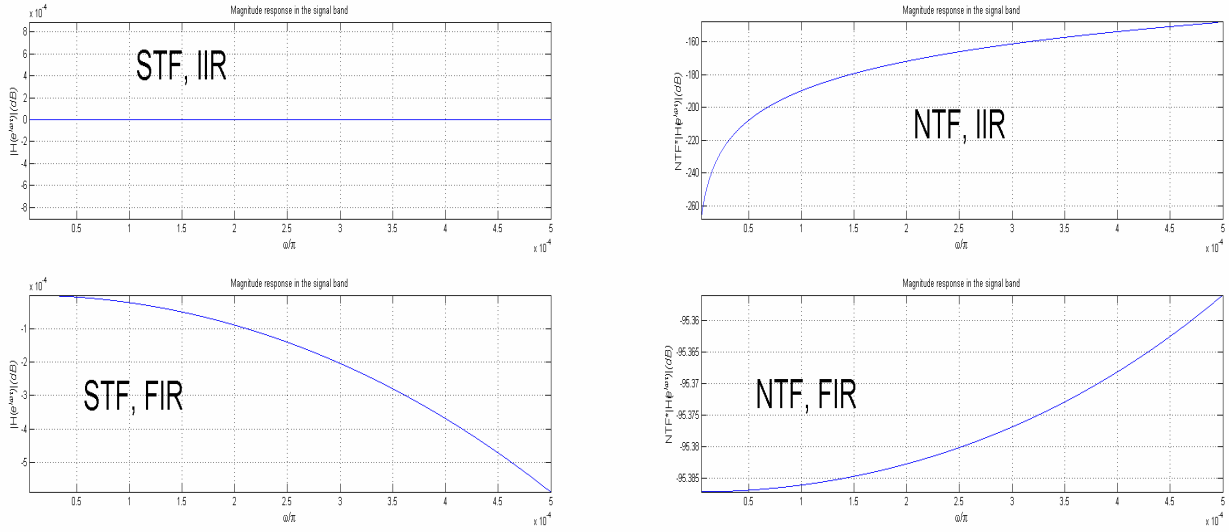


(a) (b)

Figure 3.7. Frequency response of cascaded-damped integrators.

(a) Frequency response of STF and its FIR equivalent.

(b) Frequency response of NTF and its FIR equivalent.



(a) (b)

Figure 3.8. Frequency response of Butterworth filter.

(a) Frequency response of STF and its FIR equivalent.

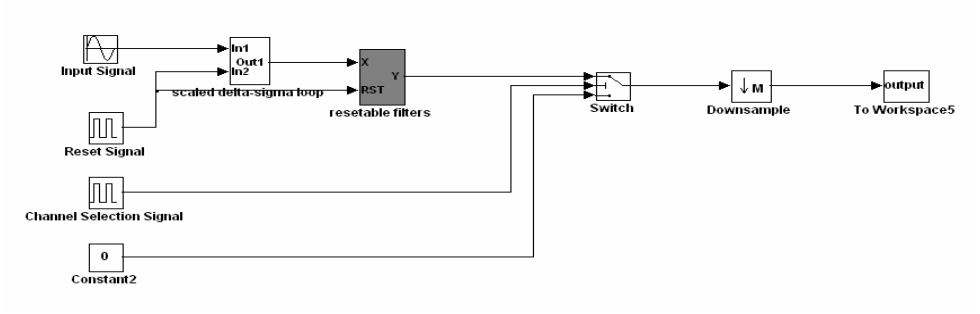
(b) Frequency response of STF and its FIR equivalent.

3.4 Simulation

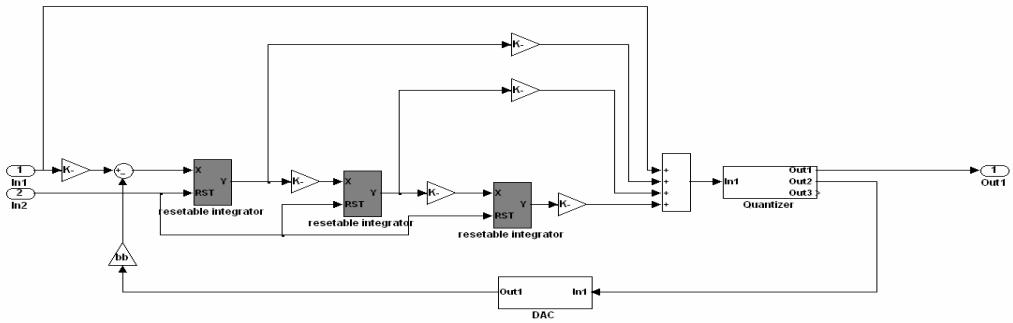
To verify the design techniques discussed in this chapter, Simulink and Matlab simulations of a typical design example will be illustrated next, These are the specifications:

- Number of channels: $N = 20$;
- Signal bandwidth: $f_B = 3$ kHz;
- Signal-to-quantization noise ratio: SQNR > 90 dB;
- Maximum sampling frequency in the modulator: $f_C = 30$MHz.

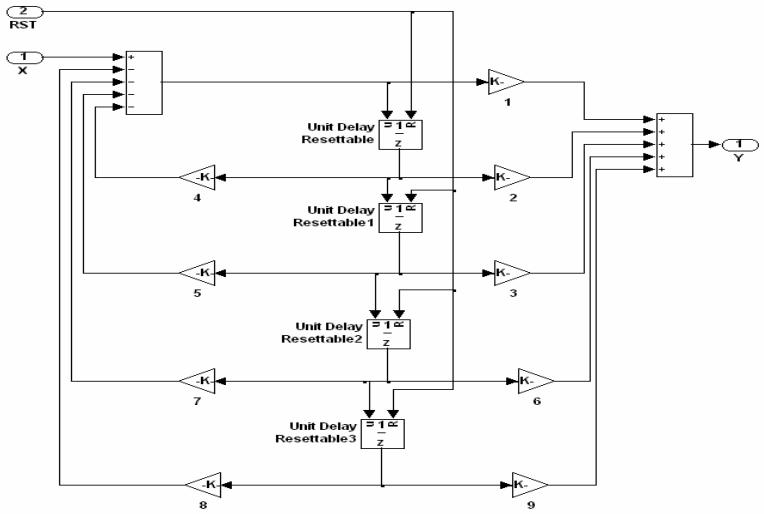
Fig. 3.9 (a) is the Simulink model of a multiplexed IDC, (b) and (c) shows the implementation of resettable ΔΣ modulator and Butterworth filter.



(a)



(b)



(c)

Figure 3.9. Simulink Model for a Multiplexed IDC.

(a) Overall System. (b) Resetable Delta-Sigma Modulator.

(c) Resettable Butterworth Filter

After the decimation filter, as shown in Fig. 3.10(a), the quantization noise is below -105 dB in the signal band in the range from 0 kHz to 3 kHz. The overall error considering the droop of the frequency response of the decimation filter over signal frequency is shown in Fig. 3.10(b). The conversion error versus the DC input is shown in Fig. 3.10(c).

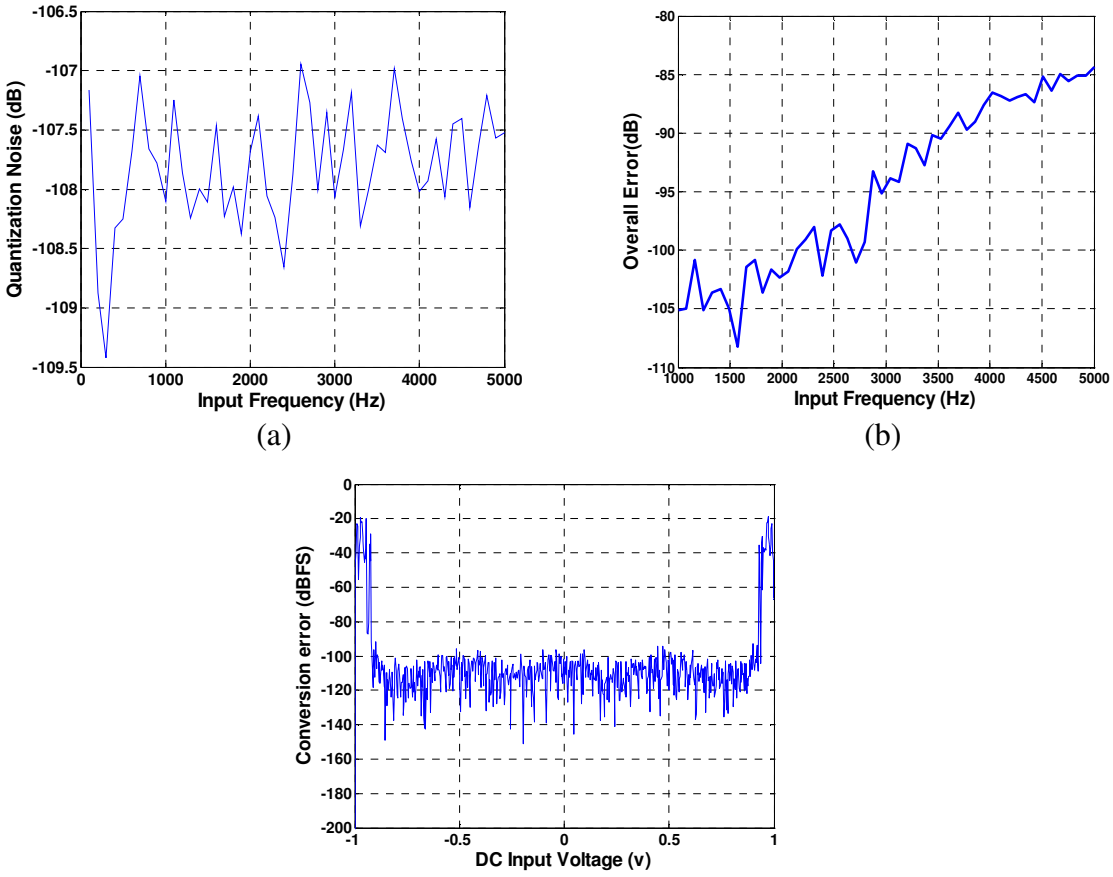


Figure 3.10. Simulation Result of a Multiplexed IDC.

(a) Quantization noise versus input frequency.

(b) Overall error versus input frequency.

(c) Conversion error versus DC input voltage

4 Signal-to-Noise Ratio Optimization

4.1 Introduction

In the previous chapters, the investigation of IDC's noise has been only focused on the quantization noise which is generated from the quantizer and shaped by the modulator loop and the decimation filter. However, there are some other noise sources including the intrinsic noise generated in the MOS transistors, as well as the extrinsic (interference) noise from the on-chip digital circuitry. In Appendix C of [2], the author discussed all the mainly intrinsic noise effects associated with delta-sigma converters using switched-capacitor (SC) circuits. To implement an ADC economically, it is important to balance the contributions of all noise sources. The author indicated that usually the thermal noise takes up the highest share as above 75% of the overall noise budget. For high-performance/low-noise systems, it is typically much easier and cheaper to suppress the quantization noise than it is to suppress the thermal noise. It is obviously the system's overall/accumulated noise performance that is of interest to the customer. It is important to consider the thermal noise properties early in the design flow, because the only way to lower the thermal noise level is to increase the power consumption. A 3dB reduction of the thermal noise level generally implies that the power consumption will have to be doubled. To illustrate the significant implications of this relationship, we may point out that in order to improve an ADC's thermal noise performance from the "16-bit" level to

the "19-bit" level, the power consumption will have to be increased by approximately 32 times.

Then especially for all IDC, which requires high absolute resolution, it is important to find out a design methodology to optimize the converters' signal-to-noise ratio (SNR) with respect to thermal noise and/or quantization noise. In this chapter, such a design technique will be described, based on time-domain considerations, and can be applied to any practical modulator structure.

4.2 Signal and Noise Analysis of the IDC

The block diagram of a typical IDC is shown in Fig. 4.1. From this figure, the single output value after M clock periods in the nth conversion cycle can be found using the finite-length convolution operation, defined as

$$v(n) = [h(k) * d(k)]_{M,n} = \sum_{k=nNM}^{[nN+1]M-1} h([nN+1]M - 1 - k)d(k). \qquad (4.1)$$

Here, $h(k)$ is the impulse response of the digital decimation filter, and $d(k)$ is the output data sequence of the ΔΣ loop, given by

$$d(k) = stf(k) * [u(k) + t(k)] + ntf(k) * q(k) \qquad (4.2)$$

Here, $stf(k)$ is the impulse response of the signal transfer function $STF(z)$ of the loop, and $ntf(k)$ is that of the noise transfer function $NTF(z)$. Also, $u(k)$ is the input signal, $t(k)$ is the input-referred thermal noise, and $q(k)$ is the quantization noise.

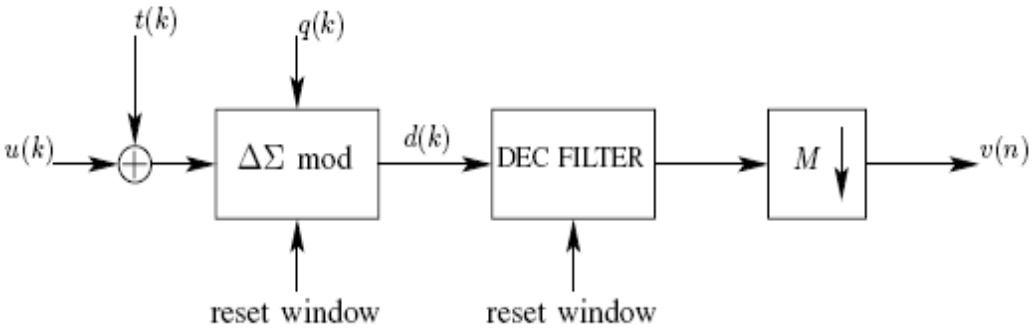


Figure 4.1. The block diagram of a typical IDC.

From Eq. (4.1) (4.2),

$$v(n) = [stf'(k) * u(k)]_{M,n} + [stf'(k) * t(k)]_{M,n} + [ntf'(k) * q(k)]_{M,n} \quad (4.3)$$

In (4.3), *stf´(k)* is the impulse response of *STF*(*z*)*H*(*z*), and *ntf´(k)* is that of *NTF*(*z*)*H*(*z*), where *H*(*z*) is the transfer function of the decimation filter. Since all blocks have nonzero outputs only for *M* periods, all convolutions contain only *M* terms. The input-referred thermal noise *t*(*k*) can be estimated from the *kT/C* noise introduced by the input branch of the loop, which can be regarded as a zero-mean noise, with power (i.e. variance or mean-square value) given by $\gamma kT/C_{in}$. Here, *k* is the Boltzmann constant, *T is* the absolute temperature in degrees, C_{in} is the capacitance of the input capacitor(s), and γ is a constant which can be estimated from the input circuitry [10]. Usually, $\gamma = 5$ is a good choice, and will be used from here on.

If we assume that the reference voltage is 1 V, so the quantization noise sequence *q*(*k*) is simply the difference between the input and the output of the quantizer. The quantization error *q*(*k*) is a white zero-mean noise, with a

probability density function (PDF) uniform within $-\Delta/2 \le q(k) \le -\Delta/2$ and zero outside this range. Here, Δ is the step size of the quantizer. The power of $q(k)$ is then $\Delta^2/12$.

Let the transfer function impulse responses be described by

$$\begin{aligned} stf[k] &= \{s_0, s_1, \cdots, s_{M-1}\} \\ ntf[k] &= \{n_0, n_1, \cdots, n_{M-1}\} \\ stf'[k] &= \{s_0', s_1', \cdots, s_{M-1}'\} \\ ntf'[k] &= \{n_0', n_1', \cdots, n_{M-1}'\} \end{aligned} \tag{4.4}$$

Since $stf'[k] = stf(k) * h(k)$ and $ntf'[k] = ntf(k) * h(k)$, the vector relations are

$$\begin{aligned} \mathrm{s}' &= \mathrm{S} \cdot \mathrm{h} \\ \mathrm{n}' &= \mathrm{N} \cdot \mathrm{h}\,, \end{aligned} \tag{4.5}$$

where

$$\begin{aligned} \mathbf{s}' &= [s_0', s_1', \cdots, s_{M-1}']^T \\ \mathbf{n}' &= [n_0', n_1', \cdots n_{M-1}']^T \\ \mathbf{h} &= [h_0, h_1, \cdots, h_{M-1}]^T \\ \mathbf{S} &= \begin{bmatrix} s_0 & 0 & 0 & \cdots & 0 \\ s_1 & s_0 & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ s_{M-1} & s_{M-2} & s_{M-3} & \cdots & s_0 \end{bmatrix} \\ \mathbf{N} &= \begin{bmatrix} n_0 & 0 & 0 & \cdots & 0 \\ n_1 & n_0 & 0 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ n_{M-1} & n_{M-2} & n_{M-3} & \cdots & n_0 \end{bmatrix} \end{aligned} \tag{4.6}$$

Combining with Eq. (4.3), the contribution of the input signal $u(k)$ to the output can be calculated as

$$v_u(n) = s'_{M-1}u(0) + s'_{M-2}u(1) + \cdots + s'_0 u(M-1). \qquad (4.7)$$

Thus, $v_u(n)$ is a weighted average of all samples of the input signal in the sampling window. The weight factors are the first M elements of the $STF'(z)$ impulse response, in reverse order.

The thermal noise power in $v(n)$ can be estimated as

$$\overline{v_t(n)^2} = \frac{\gamma kT}{C_{in}}\left(s'^2_0 + s'^2_1 + \cdots + s'^2_{M-1}\right) = \frac{\gamma kT}{C_{in}}\mathbf{h}^T \cdot \mathbf{S}^T \cdot \mathbf{S} \cdot \mathbf{h}. \qquad (4.8)$$

Assuming that the samples of the quantization noise are uncorrelated, the corresponding output noise power is given by

$$\overline{v_q(n)^2} = \frac{\Delta^2}{6}\left(n'^2_0 + n'^2_1 + \cdots + n'^2_{M-1}\right). = \frac{\Delta^2}{6}\mathbf{h}^T \cdot \mathbf{N}^T \cdot \mathbf{N} \cdot \mathbf{h}. \qquad (4.9)$$

We can assume that the maximum output signal power is V^2_{pp} /2 if the largest peak-to-peak sinewave amplitude V_{pp} which does not overload the quantizer.

The overall signal-to-noise ratio is, by (4.1) - (4.9),

$$SNR = 10\log\left[\frac{V^2_{pp}/2}{\overline{v_t(n)^2} + \overline{v_q(n)^2}}\right] = 10\log\left[\frac{V^2_{pp}/2}{\mathbf{h}^T \cdot \mathbf{O} \cdot \mathbf{h}}\right]. \qquad (4.10)$$

Here, **O** is the overall noise transfer matrix

$$\mathbf{O} = \frac{\gamma kT}{C_{in}}\left[\mathbf{S}^T\mathbf{S} + \rho\mathbf{N}^T\mathbf{N}\right] \qquad (4.11)$$

and

$$\rho = \frac{\Delta^2 / 6}{\gamma kT / C_{in}} \tag{4.12}$$

is the *noise power ratio NPR* between the power of the quantization noise and the thermal noise. In the next Section, we will use Eqs. (4.8)-(4.12) for SNR optimization.

4.3 SNR Optimization

4.3.1 General Considerations

An IDC's overall performance is determined by the SNR. For a given ΔΣ modulator, the task of optimizing the performance is equivalent to minimizing the noise contributions to the output $v(n)$ by choosing M, C_{in} and $H(z)$ appropriately to achieve:

1. Minimize the overall noise $\overline{v_t^2} + \overline{v_q^2}$.

2. Minimize the power dissipation for a specified SNR. Usually, reducing the quantization noise $q(k)$ requires less power than reducing the thermal noise $t(k)$, we would weigh $t(k)$ less heavily than $q(k)$.

To reduce the distortion on the input signal, the overall DC signal transfer function has to be chosen to equal 1 as

$$s_0' + s_1' + \cdots + s_{M-1}' = 1. \tag{4.13}$$

Since the *STF* of the CIFF ΔΣ modulator is 1 [8], specifying $H(z) = 1$ for $z = 1$ achieves unity gain in the signal band. This becomes the constraint

$$h_0 + h_1 + \cdots h_{M-1} = \mathbf{e}^T \mathbf{h} = 1. \qquad (4.14)$$

Here, **e** is an *M*-element column vector of 1s.

4.3.2 Thermal Noise Minimization

In this section, we will only consider the minimization of the thermal noise, while ignoring the quantization noise.

By Eq. (4.8), this requires the minimization of the expression

$$E(\mathbf{s}') = s_0'^2 + s_1'^2 + \cdots + s_{M-1}'^2 \qquad (4.15)$$

`subject to constraint Eq. (4.13). If $s_i' = 1/M$ is assigned for all *i*, then $E(s')$ simplifies to 1/*M*, and the mean square of the thermal noise in $v(n)$ is $\gamma kT/(MC_{in})$. Unfortunately, if quantization noise is taken into account, $s_i' = 1/M$ would result a large contribution from $q(k)$ in $v(n)$, as will be discussed in the next section.

4.3.3 Quantization Noise Minimization

The overall noise transfer function $NTF' = NTF \cdot H$ is the product of the $\Delta\Sigma$ loop's noise transfer function and the decimation filter's transfer function. If *NTF* is assumed to be known for a given $\Delta\Sigma$ modulator structure, thus the minimization of the quantization noise in $v(n)$ entails finding the optimal impulse response $h(k)$ of the decimation filter. Since the *NTF* is a highpass function, $H(z)$ should be a lowpass filter to cancel the inband quantization noise. As described in [4], the last output samples $d(M-L), d(M-L+1), \cdots, d(M-1)$ of the modulator

will contain large quantization errors. This requires that the first L elements of $h(k)$ will be zero, or very small for a for an Lth order *NTF*.

Under the constraint of Eq. (4.19) and (4.14), the optimum **h** can be found analytically, using the Lagrange multiplier method. The result is

$$\mathbf{h} = \frac{\mathbf{K}^{-1}\mathbf{e}}{\mathbf{e}^T\mathbf{K}^{-1}\mathbf{e}} = \frac{\left[\sum_{j=0}^{M-1} k_{1j} \quad \sum_{j=0}^{M-1} k_{2j} \quad \cdots \quad \sum_{j=0}^{M-1} k_{M-1,j}\right]^T}{\sum_{i,j=0}^{M-1} k_{ij}} \tag{4.16}$$

Here, $\mathbf{K} = \mathbf{N}^T\mathbf{N}$, **e** is an M-element column vector of 1s, and the k_{ij} the elements of $\mathbf{K}^{-1}$. Matlab function "quadprog" can be used to calculate Eq. (4.16).

4.3.4 Total Noise Minimization

As shown in Eq. (4.10), the digital filter which minimizes of the overall noise power, i.e. the sum of thermal and quantization noise powers, has an impulse response which minimizes $\mathbf{h}^T \cdot \mathbf{O} \cdot \mathbf{h}$, where **O** is given in Eq. (4.11). The solution is given as before by Eq. (4.16), where now $\mathbf{K} = \left(\mathbf{S}^T\mathbf{S} + \gamma \cdot \mathbf{N}^T\mathbf{N}\right)^{-1}$. As already mentioned, in practice the available quadratic programs (such as Matlab's "quadprog") may provide a faster solution than using the analytical approach.

5 Conclusion

In this thesis, the theoretical analysis and some design methods were described for multiplexed incremental converters, which include:

The analysis of the previous research on first-order and high-order IDCs was presented. The modulator structure, digital filter design and system level performance were discussed. The resolution/number of channels trade-off was explained and was used to derive an upper bound for the number of multiplexed channels for a specified clock frequency and accuracy. The comparison among different filter configurations shows that, although the cascaded-integrator has the lowest complexity, in high-resolution applications the use of a Butterworth filter may yield a better performance in terms of accuracy. The performance limitation of IDCs was explained in terms of both thermal noise and the quantization noise. A design methodology was introduced which achieves the best possible signal-to-noise performance for the complete data converter system.

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