AN ABSTRACT OF THE DISSERTATION OF

Brian LeRoy Young for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on June 3, 2013.

Title: Time-Based Noise-Shaping Techniques for Time-to-Digital and Analog-to-Digital Converters.

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Pavan Kumar Hanumolu

In this dissertation, time-based signal processing techniques and their applications in oversampling and noise-shaping data converters are examined. These techniques demonstrate the ability to shift the burden of high performance analog circuits from the compressed voltage-domain to the augmented time-domain. First, the potential of high order noise-shaping and phase-domain feedback in time-to-digital converters (TDCs) is explored. A prototype phase reference, second-order continuous-time delta-sigma TDC for sensor applications was fabricated in 90 nm CMOS and achieves 64 dB dynamic range in 1 MHz signal bandwidth. Second, an ultra-high performance oscillator-based delta-sigma modulator architecture is investigated. The proposed circuit is a third-order continuous-time PLL-Based Delta-Sigma Modulator with simulated 77 dB SNDR in 40 MHz signal bandwidth with OSR of 16, and is fabricated in 65 nm CMOS.

Time-Based Noise-Shaping Techniques for Time-to-Digital and Analog-to-Digital Converters

by

Brian LeRoy Young

A DISSERTATION

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APPROVED:

Major Professor, representing Electrical and Computer Engineering

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Director of the School of Electrical Engineering and Computer Science

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Dean of the Graduate School

I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Brian LeRoy Young, Author

ACKNOWLEDGMENTS

> For what shall it profit a man, if he shall gain the whole world, and lose his own soul? Or what shall a man give in exchange for his soul?
>
> Mark 8:36-37 KJV

The beginning of my graduate school adventure had its dawning many years ago during my high school days. A challenging new computer programming teacher named Tom Strong from Carnegie Mellon inspired me and my friends Tim Troutman and Brad Goodyear with talk of the vast opportunities in computers. The occasional dismantling of an old computer to understand its composition served as a catalyst. On one particular occasion, I clearly remember peering into the inward parts of an Apple Macintosh Centris 610 with a Motorola 68L040 microprocessor, and it was at that moment that I was determined to understand what was inside the little black plastic package and how it worked. Thank you Mr. Strong for helping to get this ball rolling.

At the completion of my undergraduate degree, the Dot Com era was in full expansion, and the salary offers were too good to resist. My career path led me to Arizona to work for Motorola and its Timing Solutions Operation. I met many good people that I am honored to have as friends. I would like to thank my manager Lou Spangler for bringing me on board and allowing me to get my hands dirty in transistor level design. Thank you especially Phuc Pham for your kindness toward, being my technical mentor, and introducing me to the delta-sigma modulator. Thank you Wilburn Ivy for our napkin engineering discussions. It's too bad that someone beat us to a phased array TV receiver for automotive applications. I would also like to thank my colleagues Bob Berger, Mike Riggs,

Lisa Prazak, Nate Castile, and others at TSO for their support. Thank you Mark Hunt for your wisdom and friendship. Thank you Karthik Rajagopalan for always encouraging me to pursue graduate school. I will always cherish the many meals we shared discussing HBT "birthday cakes".

My career path next turned to AMI Semiconductor. Thank you Mark Gianelle for so much that it is difficult to express here. Thank you Ron Cheponis and Jeff Witt for suffering my ignorance and being always ready to teach with patience. I would like to thank my manager Jim McGough for treating me better than I deserved. Your generosity and compassion is not lost on me. Thank you Tim Warneck for our technical discussions and your encouraging words. Thank you Erik Geissenhainer for the advice about Oregon State and encouragement throughout my years in Corvallis. Thank you to all at the Pennsylvania Design Center for making it such an interesting place to work! I will always look fondly on my time there.

After enjoying some part time graduate classes at Villanova University with Professor Mark Jupina, I decided to take the plunge and return to school full time. I would like to thank Rob Gregoire for putting me in contact with Oregon State professors. Thank you to Professors Un-Ku Moon and Karti Mayaram for serving on my committee and also allowing me to observe your teaching styles. Thank you Dr. David Hackleman for serving as my committee Graduate Council Representative and for sponsorship of senior design projects that I was able to observe and mentor. Thank you Professors Un-Ku Moon, Gabor Temes, and Pavan Kumar Hanumolu for allowing me to gain classroom lecturing experience. Thank you Professor Raviv Raich for the crash course in LaTeXwhich has helped me greatly in my academic career. Thank you Professor Gabor Temes for your humor in the classroom. I have a chuckle every time I think of poles in the right half

plane. Thank you Professors John Wager and John Conley for bringing energy and enthusiasm to the classroom and making the intricacies of semiconductor device physics engaging for mere circuit designers. Thank you Professor Pavan Kumar Hanumolu for your innovative teaching methods which fostered much growth in your students. Thank you Don Heer for allowing me to be your Senior Design Class teaching assistant for not one year but two years. I really enjoyed that time. Thank you Oregon State for making a commitment to teaching by hiring student oriented faculty.

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Words cannot fully express my humble admiration and indebtedness toward my advisor Pavan Kumar Hanumolu. You gave me the opportunity to pursue my dreams of graduate school. When trying times came, you supported me and encouraged me to press onward. Your feedback, stern at times and gentle other times, was exactly what was needed in those moments. I value your ability to attract decent human beings to your research group and to make our group meetings an inviting, open forum to discuss ideas and receive feedback. It has been my honor to have you as my advisor and friend. I wish you all the best in your future endeavors.

Thank you to the members of Calvary Baptist Church of Harrisburg, Pennsylvania and Mid Valley Baptist Church of Corvallis, Oregon for your prayerful support of me and my family. Thank you Pastor Jim Moore, Ernie Moore, Bob Bowers, Eric Gustafson, Jim Cavitt, Todd Herbster and others at CBC for your prayers and brotherly kindness. Thank you Pastor Bob Crawford and Brothers Dennis Bullock and Nick Weber for helping me to grow as a new Christian. Thank you Brothers Austin Adams, Matt Cook, Joe Crawford, and Charles Williams for your friendship and suffering my endless technical explanations. Thank you for the meals we shared together. Thank you Brothers Shawn Holes, Ken Lightsey, Jesse Boyd, Ricky Springer, Kevin Borden, and Michael Lasiter. Your bold witness for Jesus has been an inspiration to me. May God continue to bless you!

Thank you to my parents Terry and Patricia Young for your words of encouragement and support. You have always been there for me and supported my

dreams and aspirations. Thank you for showing me how to get back up after being knock down, and how to put away my selfish pride. Thank you to my sister Jonie Roberge for your encouragement in negotiating the maze of graduate school. Your strength in overcoming has inspired me. Thank you to my extended family for their love, support, and encouragement.

How fortunate and undeserving am I to have a wonderful, loving, caring wife as you Stephanie, my partner, best friend, and mother of my children Phoebe, Daniel, and Baby #3. From the beginning when I first told you I wanted to go back to graduate school, you never once hesitated. You have always encouraged me to press on — all the more so in my times of self doubt. We have struggled. But we have persevered through our walk with Christ. I would have never finished graduate school without you. I thank God for you always. I love you!

To Him who gave me life and life anew, who redeemed my soul, who directs my paths, and reigns supreme, thank you Lord Jesus!

At the beginning of the year 2007, I was faced with great turmoil in my life. Then one day a man asked me a question that would change my life for ever. He asked, "Brian, if you were to die tonight, do you know for sure that you would be in Heaven?" I had never thought of that before. I thought that church was something I would get back into when I had children, so they would be raised with morals. He then showed me from the Bible that "There is none righteous, no, not one" (Romans 3:10 KJV) "For all have sinned, and come short of the glory of God" (Romans 3:23 KJV). This was sobering news. He then read "But the fearful, and unbelieving, and the abominable, and murderers, and whoremongers, and sorcerers, and idolaters, and *all liars*, shall have their part in the lake which burneth with fire and brimstone: which is the second death." At this point I was

honest with myself and with God, and realized that for the life I had lived and all the lies I had told that I deserved to be in Hell for all eternity. Some may look at me as a good person. I never got in trouble and had a successful career, but when compared to God and his righteousness my "righteousnesses are as filthy rags" (Isaiah 64:6 KJV).

It was at this point I realized I had a big problem, and he continued to read. "For the wages of sin is death; but the gift of God is eternal life through Jesus Christ our Lord." (Romans 6:23 KJV). He spoke of the gift of God being eternal life. I had gone to church before and knew of Heaven and Hell and Jesus, but I had never heard of the gift of God. Jim preceded to analogize a Christmas present with the gift of God, and spoke of how a gift is no longer a gift if you work for it yourself. He said that to receive a gift you much reach out and take it. Now I thought this is something that I could do. I spent years trying to be a good person outwardly, but I knew in my heart that I was not.

So what could I do to receive the gift of eternal life and escape eternal punishment in Hell? That very question was asked of Paul and Silas to which they responded, "Believe on the Lord Jesus Christ, and thou shalt be saved." In other words if we believe that Jesus Christ lived a perfect, sinless life on this earth (1 Peter 2:22 KJV); died and shed his blood on the cross as payment for sin past, present, and future (Hebrews 9:26, 10:12 KJV); and rose again on the third day (1 Corinthians 15:3-4 KJV), that God would forgive us for the wrong things we have done and give us a home in Heaven. This good news or Gospel seemed too good to be true! He then continued to read, "For whosoever shall call upon the name of the Lord shall be saved" (Romans 10:13 KJV) and "That if thou shalt confess with thy mouth the Lord Jesus, and shalt believe in thine heart that God hath raised him from the dead, thou shalt be saved" (Romans 10:9 KJV).

At that point I fully realized that all the good that I had done would never outweigh the bad, and that I needed the free gift of eternal life that God offers through Jesus Christ. I bowed my head and prayed to God and told Him that I knew I was a sinful man deserving of Hell. I believed that Jesus lived the sinless life that I never could, paid the penalty for my sin, and rose again. I accepted the gift of eternal life through placing my trust and faith in Jesus Christ. This is a gift that cannot be worked for because "For by grace are ye save through faith; and that not of yourselves: it is the gift of God: not of works, lest any man should boast" (Ephesians 2:8-9 KJV).

I implore you reader and friend to examine yourself in the light of God's righteousness and call upon Jesus for forgiveness today. For the believer, I encourage you to read your Bible, pray, and go to a church. "Be ready always to give an answer to every man that asketh you a reason of the hope that is in you with meekness and fear" (1 Peter 3:15 KJV).

I chose the versus from Mark to begin my acknowledgements because they continue to remind me of my old selfish motives for attending graduate school. With a Ph.D. I had sought the praise of men to serve my own selfishness. Now, I would trade nothing for the hope I have in Christ Jesus.

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To Him whose name shall be called Wonderful, Counsellor, The mighty God, The everlasting Father, The Prince of Peace: Jesus the Christ.

TIME-BASED NOISE-SHAPING TECHNIQUES FOR TIME-TO-DIGITAL AND ANALOG-TO-DIGITAL CONVERTERS

CHAPTER 1. INTRODUCTION

Since the first integrated circuits (ICs) were co-invented independently by Jack Kilby of Texas Instruments [1] and Robert Noyce of Fairchild Semiconductor [2], the past five decades have seen an almost unimaginable growth in their applications. These physically diminutive inventions became a major catalyst in the second industrial revolution, the Technological Revolution, and spawned a worldwide 100 billion dollar industry. Thanks to the many pioneering achievements of engineers and scientists of yesteryear, we enjoy the instant accessibility of information in the palm of our hand through ubiquitous wireless networks and smartphones.

The hand-held computing and part-time audio communication device, known in the vernacular as a smartphone, would have never come into existence without visionary science fiction writers and the miniaturization of the monolithic IC. Without belaboring the works of science fiction, the future co-founder of Intel, Gordon Moore, famously predicted in 1965 that the number of transistors in an integrated circuit would double every year [3]. He would later revise that number to be a doubling every two years [4]. Forty years ago it must have been difficult to imagine today's modern microprocessors which contain upwards of a billion transistors on

a single die the size of a fingernail, and will soon enable super computer clusters to perform at exaFLOP scale (10^{18} FLoating-point Operations Per Second).

1.1 Motivation

Most of the effort in modern nanometer-scale CMOS development has been directed at producing higher digital circuit integration, leaving the artful world of analog circuits, with a few exceptions, woefully neglected. Digital circuits have benefitted from nearly free transistors, producing digital circuit solutions reminiscent of Weimar Republic monetary policy. Specific processes optimized for analog circuit performance have not been cost competitive in the consumer market space and have been relegated to niche applications. Consumer market pressure drives the integration of analog circuits, such as the analog-to-digital converter (ADC) and phase-locked loop (PLL), onto the digital die where the analog circuit design is saddled with the burden of MOSFETs — all the negative characteristics of BJTs without the positive characteristics.

While CMOS process and supply scaling have benefitted digital circuits greatly through decreased gate delay and dynamic power, they have created two main problems in analog circuits. Firstly, transistor small signal intrinsic gain, $g_m r_o$, decreases with decrease in channel length. Small signal transconductance is proportional to $1/t_{ox}$, and output resistance is proportional to L. For technology nodes larger than 130nm, the rate of gate length and gate oxide scaling remains largely constant. However, with technology nodes less than 130nm, the rate of gate oxide scaling has slowed due to quantum mechanical tunneling which leads to significant gate current. Together they result in reduced transistor intrinsic gain, compromising analog circuit performance. Secondly, supply voltage

scaling has reduced the voltage headroom available for signal information, leading to a decrease in signal power. Without a subsequent increase in power consumption to mitigate device noise, signal-to-noise ratio, $SNR = P_{signal}/P_{noise}$, must also decrease. Analog circuits in nanometer-scale CMOS cannot continue rely on traditional techniques to mitigate low gain and high mismatch, but increasingly must depend on high power multi-stage amplifiers and complex digital calibration systems to remove analog circuit imperfections.

1.1.1 Time-Based Signal Processing Techniques

Woes of analog circuits designed in digital processes cause a subtle benefit to be often overlooked. Neglecting the impact of wire resistance and capacitance for simplicity, process scaling has directly reduced the input capacitance proportional to t_{ox}/L^2 and increased current drive proportional to $1/t_{ox}$ resulting in higher switching speeds. Thus, gate delay and rise/fall times decrease, and time uncertainty or metastability also reduces. In other words, time resolution of a given period is increasing as gate length decreases. Figure 1.1 depicts increased time resolution potential of process scaling. These properties of digital process scaling open up the possibility of processing signal in time rather than voltage.

In the analog-to-digital converter branch of analog circuits, there has been an ardent research emphasis into a class of time-based circuit generally know as the voltage-controlled oscillator-based ADC [5]. The voltage-controlled oscillator (VCO) performs ideal voltage-to-phase integration with modulus 2π. With its pole at DC, the VCO integrator circumvents finite gain error associated with traditional op-amp based integrators. Simple digital counters can track the modulo-2π phase wrapping and trade off signal dynamic range with conversion time. In other words,

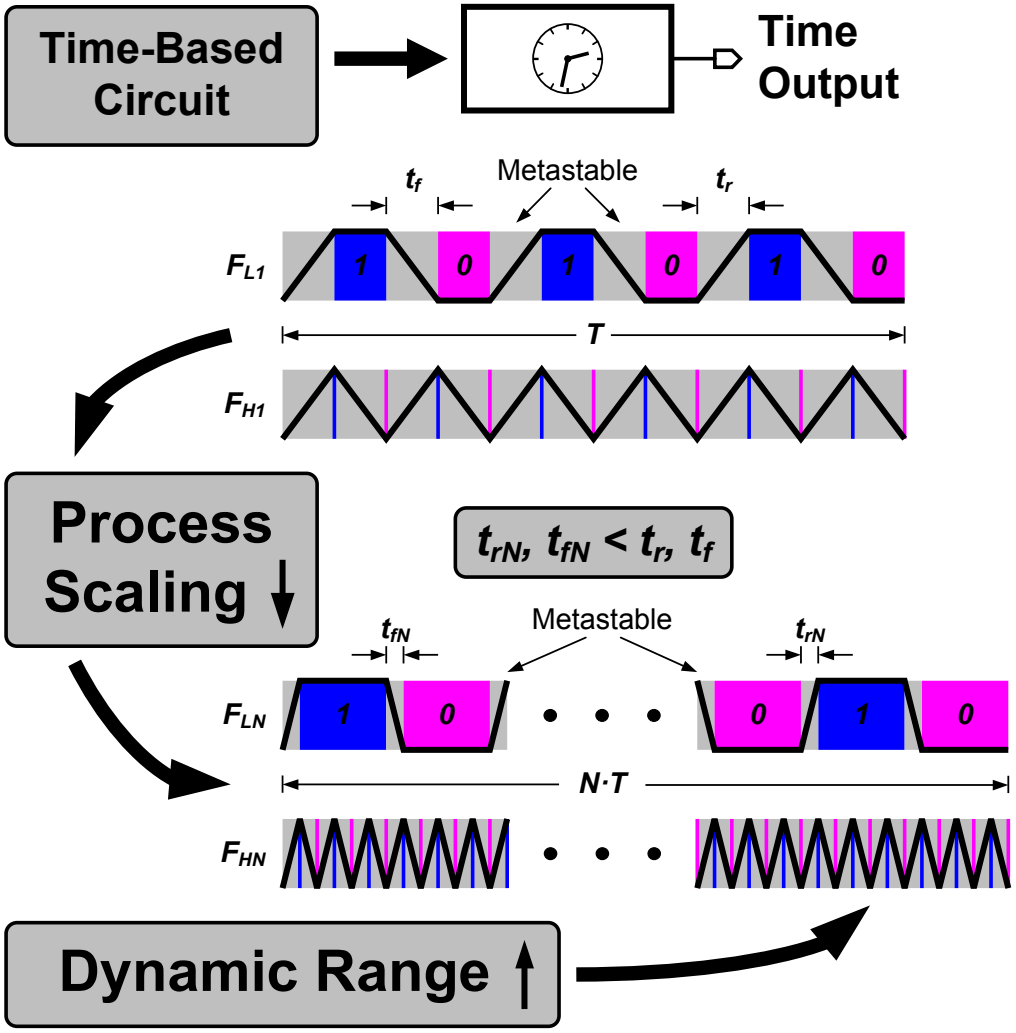


Figure 1.1: Process scaling reduces metastability and increases time resolution.

given enough time, signal range can be extended indefinitely. Phase detector circuits borrowed from phase-locked loop circuits can distinguish oscillator phase. When used as a quantizer, a VCO with multiple phase outputs increases quantizer resolution by $\log_2(M)$, where M is the number of VCO phases. Unlike traditional flash ADCs which must discriminate signals proportional to $V_{DD}/2^M$, VCO quantizers discriminate phase outputs with swings nearly rail-to-rail, reducing offset and metastability requirements of its comparators. In general, oscillator-based integrators and quantizers mitigate integrator finite gain error with ideal phase-domain integration, and comparator offset and metastability effect with large swing outputs. Additionally, this phase-domain integrator decouples signal power from supply voltage through signal conversion to time where dynamic range can be indefinitely expanded.

1.1.2 Oversampling and Noise-Shaping

In addition to time-domain signal processing, the concepts of oversampling and noise-shaping can be used to enhance ADC performance by reducing the amount of in-band quantization noise. In the case of ADCs, the delta-sigma modulator (DSM) is the pervasive architecture [6]. It exploits loop filter gain to filter quantizer noise out of the band of interest. Noise-shaping may be either high-pass (with low-pass signal) or band-stop (with band-pass signal). Continuous-time loop filter implementations have furthered development of giga-sample per second delta-sigma modulators with greater than 100 MHz signal bandwidth [7, 8].

1.2 Organization

This work seeks to outline and demonstrate time-based noise-shaping techniques with application to time-to-digital converter (TDC) and analog-to-digital converter (ADC) circuits. Chapter 2 explores background information and analysis of existing TDC architectures. Chapter 3 details the proposed Phase-Reference Continuous-Time Delta-Sigma TDC, including measurement results, which has application in time-based sensors and as a phase detector replacement in digital loop filter phase-locked loops. Next, Chapter 4 examines the intricacies of time-based analog-to-digital converters, noting their advantages and disadvantages. Chapter 5 documents the architecture and modeling of the proposed Oscillator-Based Delta-Sigma ADC. After that, Chapter 6 covers the circuit level design and simulated results of the proposed PLL-Based Delta-Sigma ADC. Lastly, this work is concluded with a summary.

CHAPTER 2. REVIEW OF TIME-TO-DIGITAL CONVERTER TECHNIQUES

A time-to-digital converter (TDC) is an electronic circuit that quantizes the analog quantity *time* or *phase* into a digital code. Historically, the TDC has been used in time-of-flight radar measurements and nuclear physics particle detection to evaluate the time interval between two events [9]. More recently, TDCs have become attractive replacements for the phase detector in a phase-locked loop (PLL), and enable analog loop filters to be digitized [10, 11]. Further, TDCs also have been used to quantized time- and phase-based sensor information for digital post processing [12, 13], and have enabled improvements in automotive and industrial sensor applications.

Time to digital converters, and all data converters for that matter, can be subdivided into two classes — those with and without memory of previous conversion — and will be discussed in the following sections.

2.1 Memoryless Architectures

Time-to-digital converters with memoryless architectures are very common and compose the vast majority TDC designs. They can be thought of as a "here and now" type of circuit because their output only depends on the current input. This allows for high conversion bandwidths and fast conversion times. However, memoryless architectures suffer from limited resolution which is on the order of a technology's minimum gate delay. To understand this architecture, some examples

will be investigated next.

2.1.1 D Flip-Flop TDC

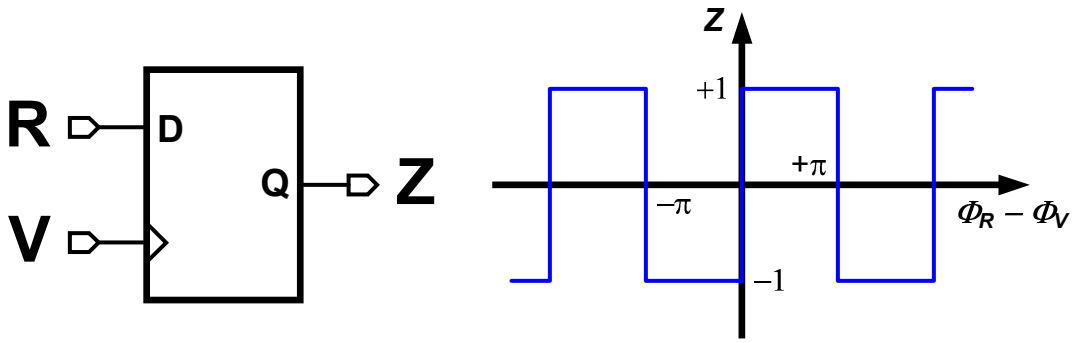


Figure 2.1: One bit D flip-flop TDC circuit and transfer function plot.

Traditionally, time-to-digital converters quantize time intervals based on a unit delay element. In fact, the simplest TDC is a D flip-flop (DFF) TDC shown in Fig. 2.1, also known as a bang-bang phase detector [14]. It finds ubiquitous application as the phase detector in digital loop filter phase-locked loop circuits. It is periodic with 2π and therefore cannot detect large frequency differences in PLL applications. The DFF TDC output resolves the early/late relationship between the first input phase, R, and second input phase, V, and is limited to one-bit resolution.

2.1.2 Flash TDC

To improve resolution of the DFF TDC, a multi-tap delay line based flash TDC, shown in Fig. 2.2 and analogous to a flash ADC, increases TDC resolution to the technology minimum unit gate delay. For a modern nanometer scale process,

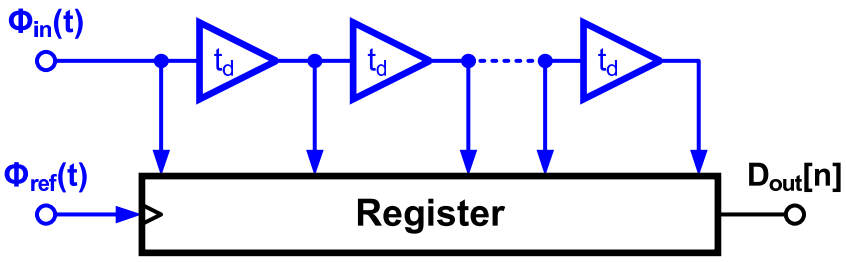


Figure 2.2: A general flash time-to-digital converter.

this can be on the order of picoseconds. The delay elements can be either linearly [10] or logarithmically weighted [15]. The former has the advantage of inherent monotonicity at the expense of chip area, while the latter has the advantage of reduced area at the expense of additional nonlinearity correction circuitry. In these approaches, resolution is limited to the minimum technology delay.

Another variation of the flash TDC is the oscillator-based TDC [9]. It utilizes a multi-phase ring oscillator in place of a delay line, and counts oscillation cycles and residual phase. This TDC has the advantage of being much smaller in area than a conventional delay line; however, it suffers from unmitigated jitter accumulation and frequency drift. Note that if a reference clock is available, a multi-phase PLL would perform the same function while canceling frequency drift and mitigating accumulated phase noise.

2.1.3 Vernier Delay Line TDC

A variation of the flash TDC is the Vernier delay line based TDC shown in Fig. 2.3 [16]. It exploits the delay element propagation delay difference, $t_2 - t_1$, between two equal element length delay lines to increase TDC resolution to a fraction of a single delay element. While this technique in principle can achieve

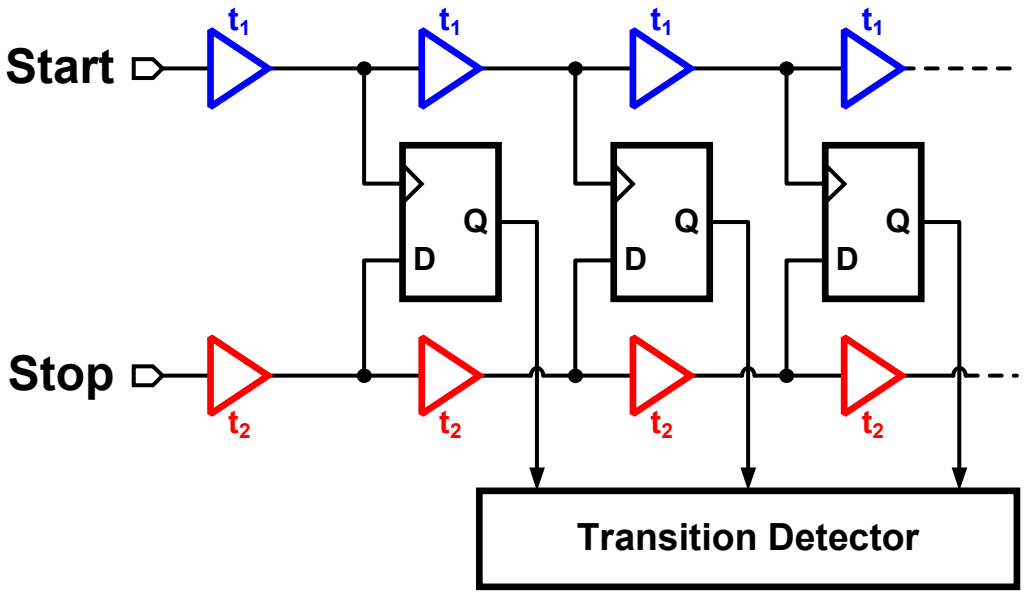


Figure 2.3: Vernier delay line based TDC with transition detector.

sub-picosecond resolution, in practice, resolution is limited by delay element propagation delay mismatch, flip-flop metastability, and delay line phase noise. Additionally, the Vernier delay line based TDC's transfer characteristic is not assured to be monotonic, and may introduce instability when used in a feedback system.

2.1.4 Stochastic TDC

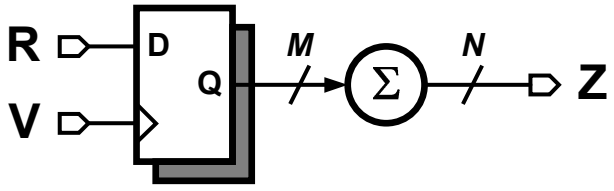


Figure 2.4: Stochastic TDC composed of DFF TDCs with uncorrelated input voltage offsets and digital summation block.

A close reexamination of the statistical behavior of the DFF TDC leads to the

stochastic TDC shown in Fig. 2.4 [17]. It takes advantage of the random mismatch characteristics of a set of latches operating around their meta-stable points. Under the influence of process variations and environmental conditions, the input offset voltage of a set of latches can be shown to have a Gaussian profile according to the central limit theorem [18]. In the Stochastic TDC, each latch receives identical input signals, and their output decisions (early/late) are summed to produce the digital output code. For a statistically significant number of latches, this TDC has a greater linear range than a DFF TDC; however, it cannot match the dynamic range of a flash TDC.

2.1.5 ADC-Based TDC

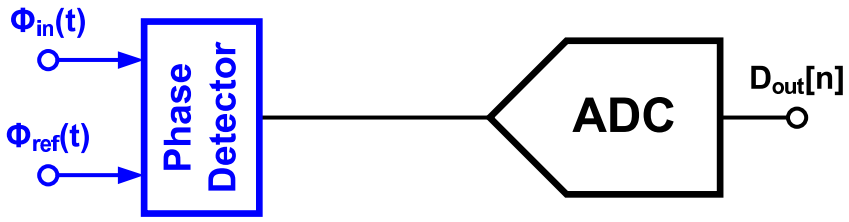


Figure 2.5: Conventional implementations of the TDC using an ADC backend.

A recent trend in TDC research is to apply analog-to-digital converter techniques to TDCs. Figure 2.5 shows one such implementation. A linear phase detector is combined with a high resolution ADC first to transform the input phase difference into a voltage, and then it is converted to digital. This TDC is limited to periodic inputs with low signal bandwidth due to the averaging nature of the phase to voltage conversion [19]. Another example is the dual-slope TDC [20]. It combines a phase/frequency detector (PFD) with a traditional dual-slope ADC to achieve high resolution. The primary drawback of this realization is that to resolve

N-bits, this TDC must operate for greater than 2^N clock cycles, which limits its use to low bandwidth systems.

2.1.6 Coarse-Fine TDC

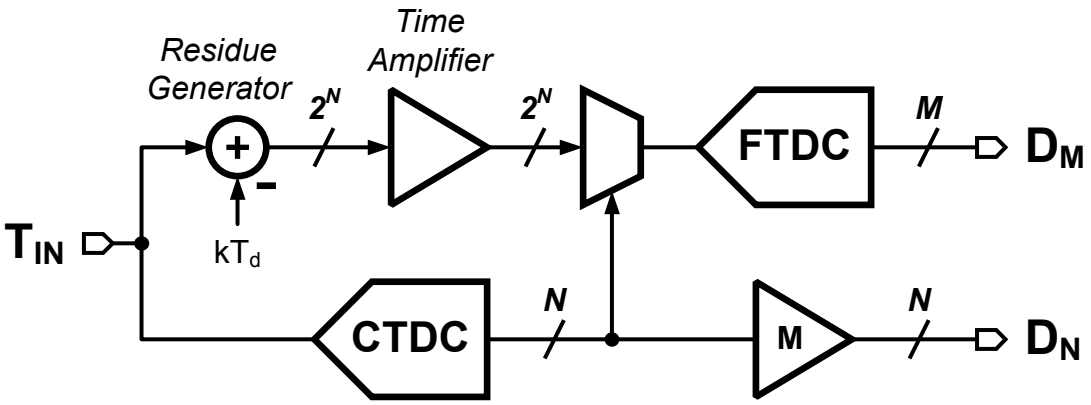


Figure 2.6: Coarse-fine, two-step TDC with time residue amplification.

Another interesting case of ADC techniques influencing TDCs is the coarse-fine TDC [21]. This TDC, shown in Fig. 2.6, resembles a two-step ADC where the first stage time residue amplification is performed by means of a time amplifier. The time amplifier consists of an SR latch operated around its meta-stable point, which provides time delay amplification of the time residue signal. The coarse and fine TDC sections can resolve N and M bits respectively, using a delay line based flash TDC architecture. Unlike classical two-step ADCs with sample-and-hold multiplying DACs, time amplifiers only function as gain stages and do not have the ability to store time in the phase domains. This limits its application to memoryless TDC architectures.

2.2 Architectures With Memory

Data converter architectures that make use of previous conversion information can increase data converter resolution. In the ADC realm, delta-sigma modulation uses memory of previous quantization noise together with oversampling to suppress in-band quantization noise. The following architectures utilize noise-shaping and oversampling to elevate TDC resolution to a higher level than is practical in memoryless architectures.

2.2.1 Continuous Time Delta-Sigma TDC

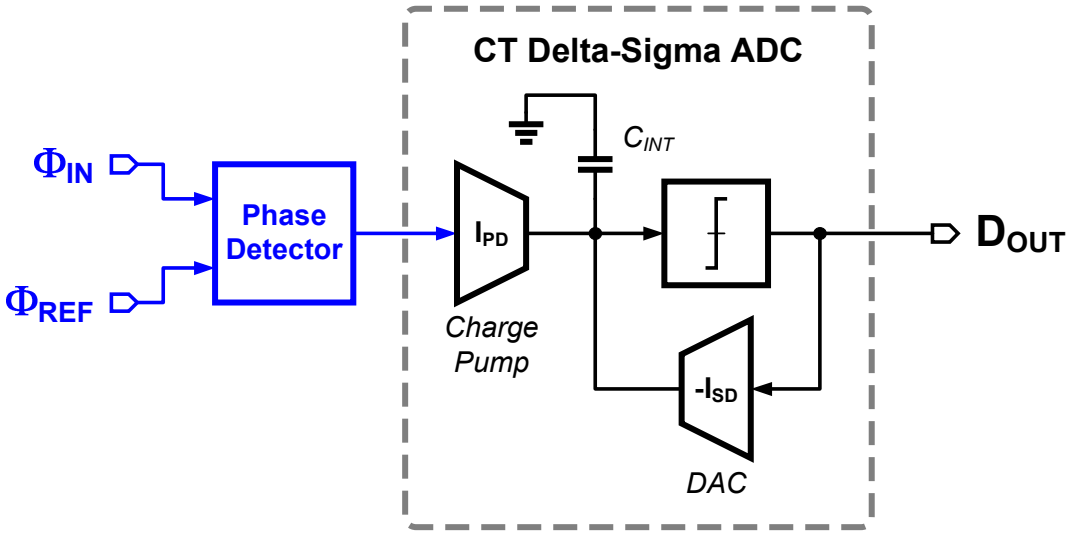


Figure 2.7: An oversampling and noise-shaping TDC utilizing a continuous-time delta-sigma ADC.

An example of oversampling and noise-shaping is the $\Delta\Sigma$-based TDC shown in Fig. 2.7 [11]. This architecture forms a first order CT$\Delta\Sigma$ TDC using a Hogge phase detector front end, phase-to-current transducer, current-domain feedback

reference, and integrating capacitor. A small open-loop gain reduces sensitivity to metastability in the one-bit quantizer. Potential mismatch in transconductance and feedback reference could alter the TDC noise transfer and signal transfer functions. However, this first order loop will remain inherently stable, within reason, with only some possible loss of resolution.

2.2.2 Gated Ring-Oscillator TDC

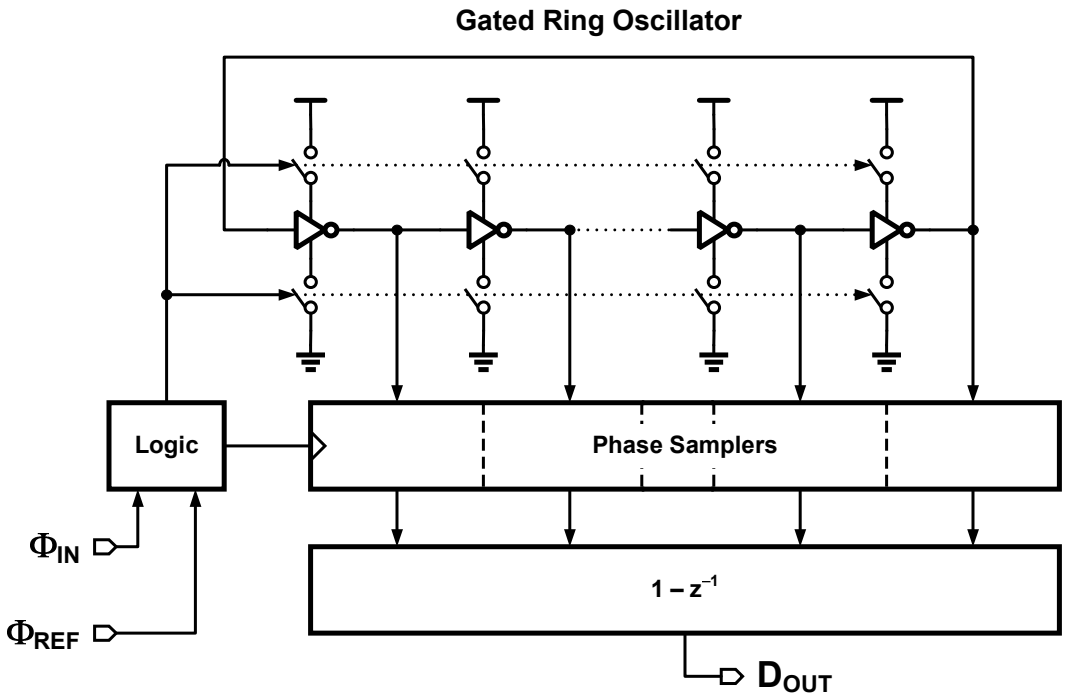


Figure 2.8: Gated ring oscillator TDC with first order quantization noise-shaping.

In a similar manner, the multi-path gated ring-oscillator (GRO) TDC, shown in Fig. 2.8, produces first-order quantization noise-shaping by storing previous time-domain quantization noise information [22]. The GRO is disabled in such a manner that its phase state is held. When enabled, the GRO begins integrating phase from the previous phase state, resulting in first-order quantization noise-

shaping. In practice, the GRO phase state is not held perfectly, introducing noise folding nonlinearity. The GRO TDC also suffers from dead zones when the measurement period is similar to an integer multiple of the GRO period. A more generalized switched ring-oscillator (SRO) TDC was introduced later [23]. The SRO mitigates the GRO deficiencies by switching between two non-zero frequencies. This obviates phase state leakage and nonlinearity.

2.3 Summary

This chapter surveyed common time-to-digital converter architectures that operate with and without memory of previous conversions. Digital process scaling into the nanometer realm greatly benefits memoryless TDC architectures with increased time resolution through reduced minimum gate delays. Vernier delay line based TDCs can improve resolution but suffer from delay mismatches that can sacrifice monotonicity. Architectures making use of memory demonstrated how quantization noise-shaping and oversampling in TDCs can improve resolution to less than the technology minimum gate delay. While these designs were limited to first order quantization noise-shaping, higher order noise-shaping has the potential to increase resolution and is explored in the next chapter.

CHAPTER 3. PHASE-REFERENCE CONTINUOUS-TIME DELTA-SIGMA TDC

This chapter describes the architecture and design details of a delta-sigma time-to-digital converter with second order quantization noise-shaping and phase domain feedback reference signals.

3.1 Proposed Architecture

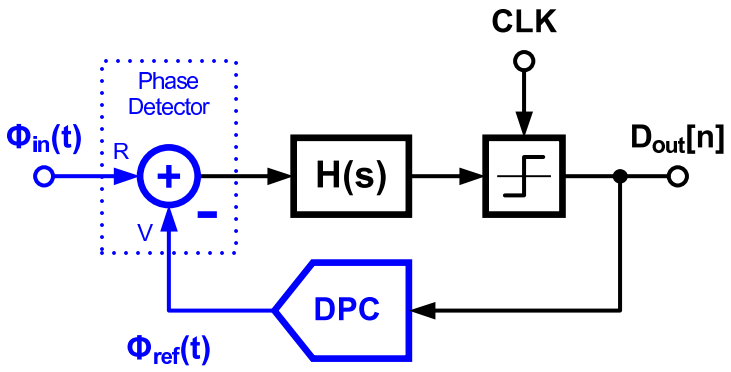


Figure 3.1: A simplified block diagram of the proposed phase-reference continuous-time delta-sigma (PR-CTΔΣ) TDC architecture.

The conceptual model of the proposed phase-reference continuous-time delta-sigma (PR-CTΔΣ) TDC is shown in Fig. 3.1 [24]. By employing noise-shaping and oversampling techniques common to voltage-domain ΔΣ ADCs, the PR-CTΔΣ TDC high-pass filters phase-domain quantization noise and greatly improves TDC resolution. Unlike [11], the phase detector is integrated into the delta-sigma loop thereby enabling the use of a digital-to-phase converter (DPC) to generate phase-domain reference signals. This significantly improves PR-CTΔΣ TDC linearity by

allowing the phase detector to operate in its most linear region, $|\Phi_R - \Phi_V| \neq 0$. After processing in the phase-domain, results are converted to the voltage-domain for further processing in the loop filter, $H(s)$, and quantizer.

The PR-CT$\Delta\Sigma$ loop filter, $H(s)$, and quantizer design trade-offs remain the same as those in the traditional CT$\Delta\Sigma$ ADC with notable exceptions. Nonuniform reference phase spacing in a multi-phase DPC would cause harmonic distortion similar to mismatch in switched-capacitor or current steering DACs, and would negate phase detector linear region operation. Implementing mismatch shaping techniques, such as dynamic element matching, are not a straightforward solution to this problem. For these reasons, a second-order CT loop filter and one-bit quantizer were chosen for implementation in this work, shown in Fig. 3.2.

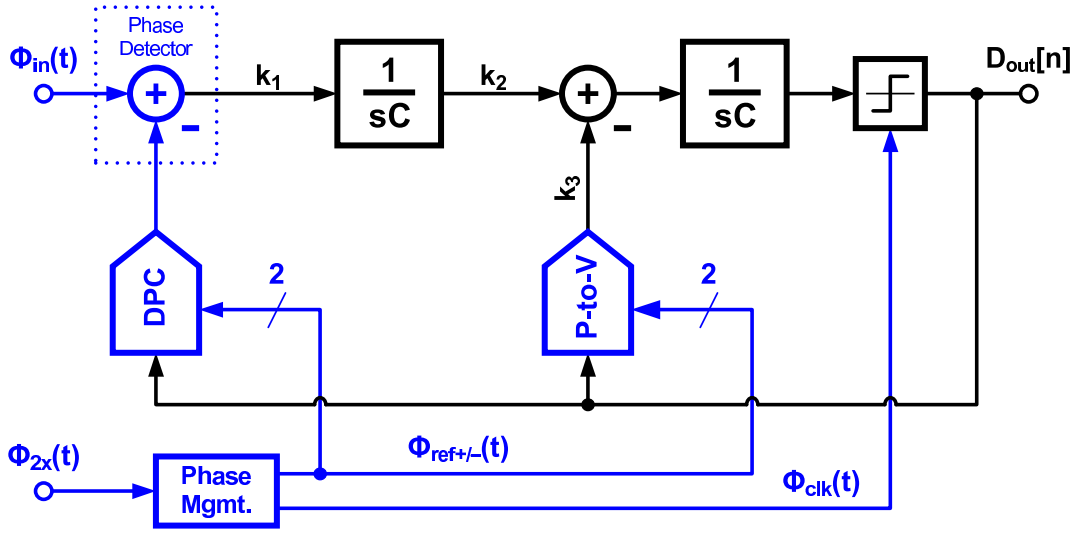


Figure 3.2: The proposed second-order PR-CT$\Delta\Sigma$ TDC block diagram.

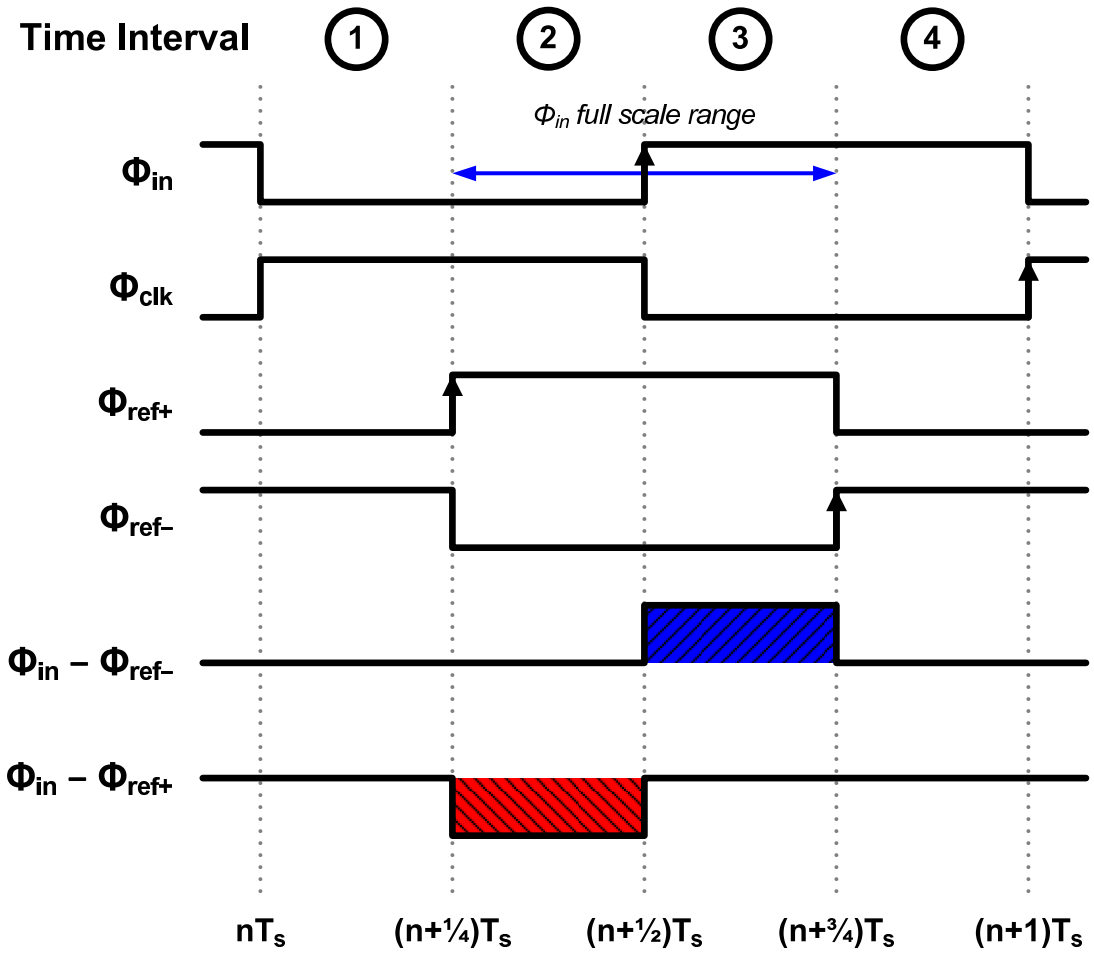


Figure 3.3: Phase timing of the proposed TDC architecture.

3.1.1 Phase Timing

A timing diagram of the input phase Φ_{in}, quantizer phase Φ_{clk}, and reference phases Φ_{ref+} and Φ_{ref-} is shown in Fig. 3.3. These signals are positive edge sensitive. Figure 3.3 is broken up into four time intervals (TI). Defined to be inclusive of TI 2 and TI 3, the TDC input full scale time range is $T_s/2$. Reference edges Φ_{ref+} and Φ_{ref-} occur at the end of TI 1 and 2, respectively. Any additional phase detector induced loop delay is absorbed during TI 4, while DPC delay and previous quantizer regeneration time are absorbed in TI 1.

3.2 Circuit Design

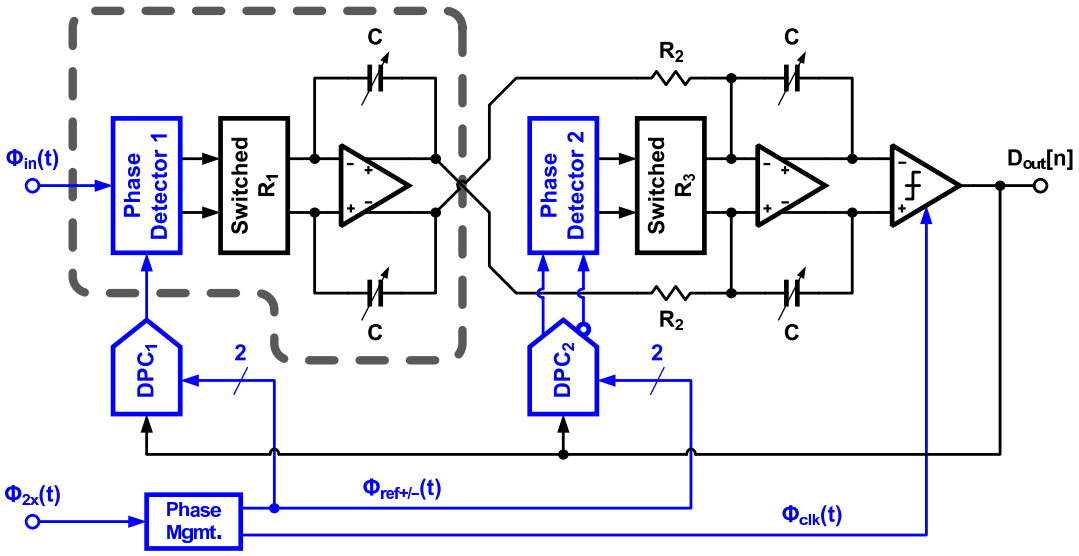


Figure 3.4: Detailed circuit block diagram.

The PR-CT$\Delta\Sigma$ TDC circuit block diagram is shown in Fig. 3.4. The following subsections detail key blocks including phase detector, digital-to-phase converter, switched resistor, operational amplifier, loop filter, and phase management.

3.2.1 Phase Detector

In order to process phase-domain signals, the PR-CT$\Delta\Sigma$ TDC uses a three-state phase/frequency detector (PFD) to measure the difference between the input signal phase, Φ_{in}, and the digital-to-phase converter phase, Φ_{ref}. Because the phase detector is placed at the modulator front end and lacks an input feed-forward path, its linearity performance, or absense thereof, will determine the overall TDC linearity performance. Simulation results show that the linearity of the PFD improves as $|\Phi_R - \Phi_V|$ increases away from zero. Figure 3.5 shows the normalized transfer characteristic of a three-state pass transistor PFD versus static phase input difference [25]. Each data point is an average of ten $U - D$ output cycles. This plot exhibits the classical asymmetric characteristic beyond $\pm 2\pi$ input phase difference.

Figure 3.6 shows pass transistor PFD static differential nonlinearity in terms of bits of accuracy. Static DNL refers to linearity measured with constant input phase difference, where each data point is the average of ten input cycles. This plot shows that in a $\pm\pi$ input range there is significant loss of linearity around zero and $\pm\pi$. The nonlinearity around zero and $\pm\pi$ input phase difference results from finite input edge rates and incomplete internal state transitions. Faster edge rates will both minimize the nonlinearity region duration and magnitude, resulting in phase detectors with wider ranges and higher linearity.

The pass transistor PFD, shown in Fig. 3.7, has benefits of fast operation and low power consumption, and functions well when used in integer-N PLLs where input phase variations are small. However, when tasked with processing widely varying input phase differences, such as those that occur in the PR-CT$\Delta\Sigma$ TDC or fractional-N PLLs, dynamic storage of state information in the pass transistor latch

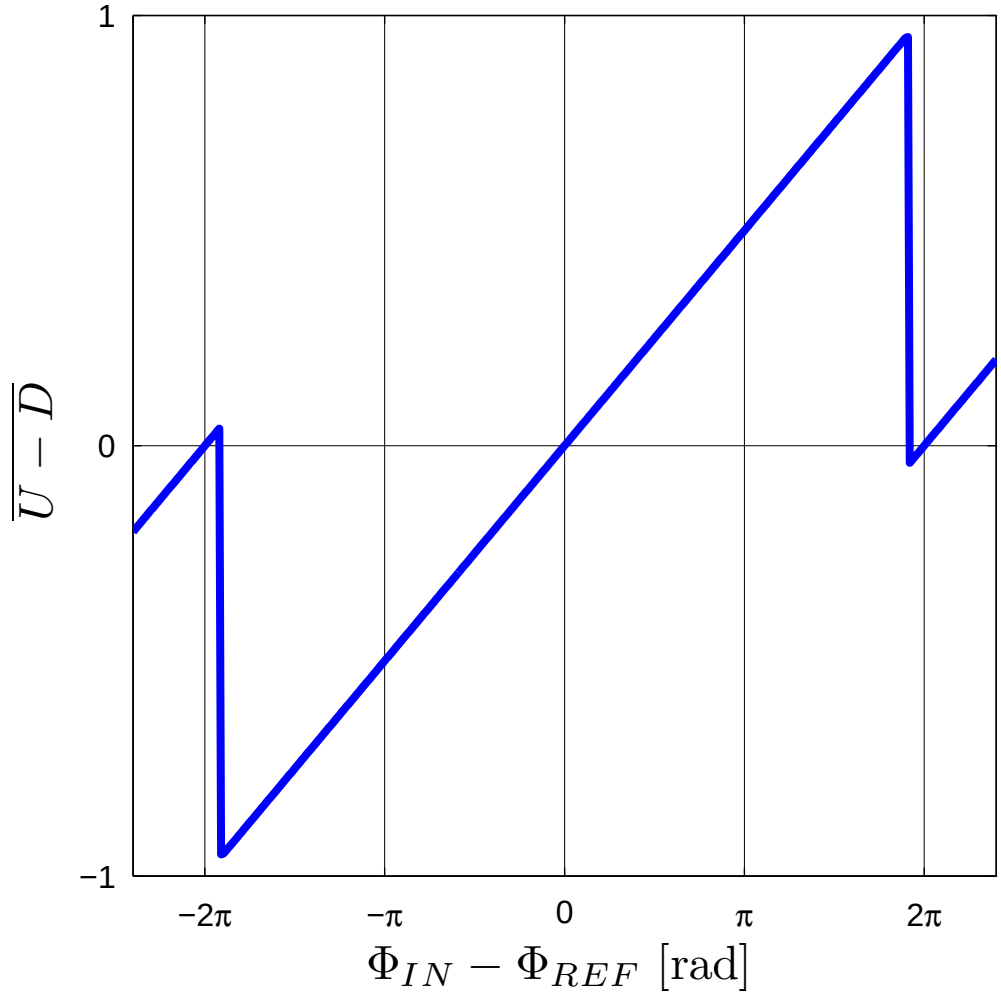


Figure 3.5: Normalized transfer characteristic of pass transistor phase/frequency detector versus input phase difference.

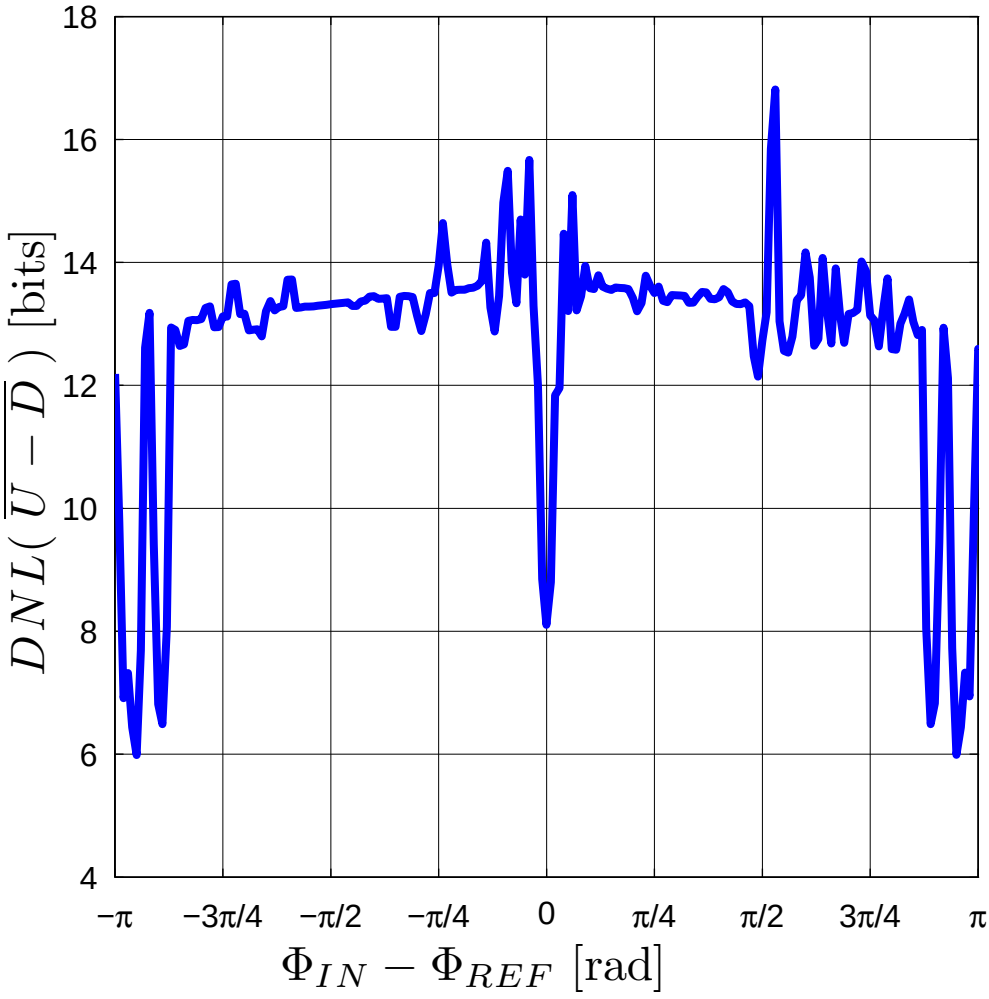


Figure 3.6: Pass transistor PFD linearity versus input phase difference expressed in bits.

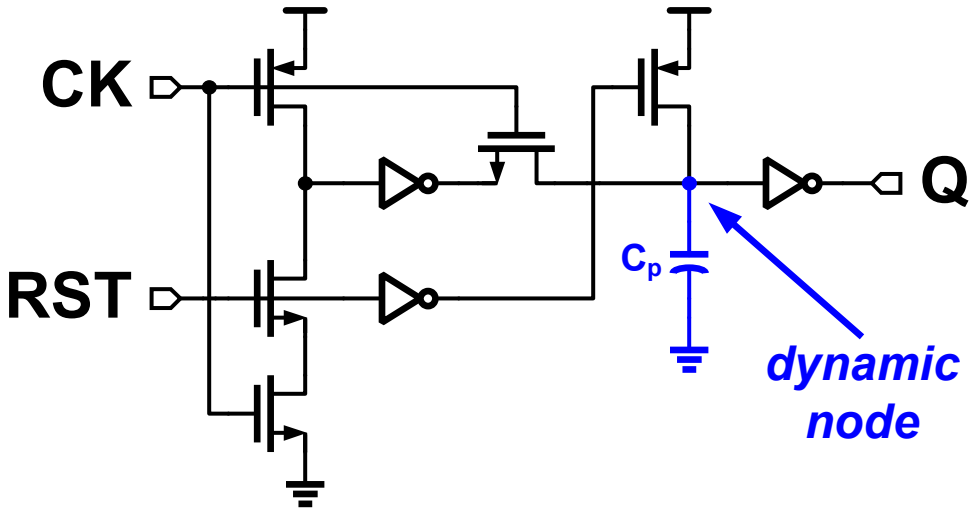


Figure 3.7: Latch circuit of pass transistor PFD showing internal dynamic node which leads to dynamic DNL.

is not consistent. The pass transistor PFD is constructed of two pass transistor latches. Their outputs are gated together to produce the reset signal. When the reset signal is asserted, the latch's high impedance dynamic node is reset to logic-1. Subsequent input signal rising edges will inject charge onto C_p prior to discharge. When the input phase difference is near $\pm\pi$, the charge coupling effect is exacerbated. Additionally, if the pull-up transistor precharging C_p is weak, voltage on C_p will retain some memory of the previous input phase processing event. The combined effect of charge coupling and previous state memory lead to significant dynamic nonlinear distortion. Therefore, it is not suitable to use the pass transistor PFD as the front end phase detector in the PR-CT$\Delta\Sigma$ TDC. Using a traditional NAND gate based PFD as the front end phase detector is preferred as it is less sensitive to previous phase processing events. Ultimately, any memory based phase detector will have reduced dynamic nonlinearity performance and should be avoided in TDC applications where linearity is important.

Fortunately, the PR-CT$\Delta\Sigma$ TDC architecture facilitates operating the PFD in its most linear regions, $-7\pi/8 < \Phi_{IN} - \Phi_{REF} < -\pi/8$ and $\pi/8 > \Phi_{IN} - \Phi_{REF} > 7\pi/8$. During DPC state transitions, the PFD output is disabled to prevent false edge transitions from affecting modulator stability. It is important to note that while the PFD can detect frequency, the PR-CT$\Delta\Sigma$ TDC architecture limits the PFD valid range to $\pm\pi$.

3.2.2 Digital-to-Phase Converter

The digital-to-phase converter uses a one-bit control signal from the quantizer to select the phase reference of the PFD. Analogous to a two level DAC, the two level DPC generates two Φ_{ref} phases, which are inherently linear. DPC_1 provides the V signal for PFD_1. With the addition of a complementary output, DPC_2 provides both R and V phases to PFD_2 to enable loop stabilization completely in the phase-domain.

A multi-bit DPC could produce increased TDC resolution proportional to $log_2(M)$, but does not have a straight forward implementation. A problem arises in generation of uniformly spaced reference phases in a delay line. While average phase spacing can be maintained through use of a delay-locked loop (DLL), device and routing mismatches lead to non-uniform phase spacing and nonlinearity. It is possible yet costly to calibrate individual phases, and mismatch shaping algorithms would introduce additional error sources in manipulating a delay line.

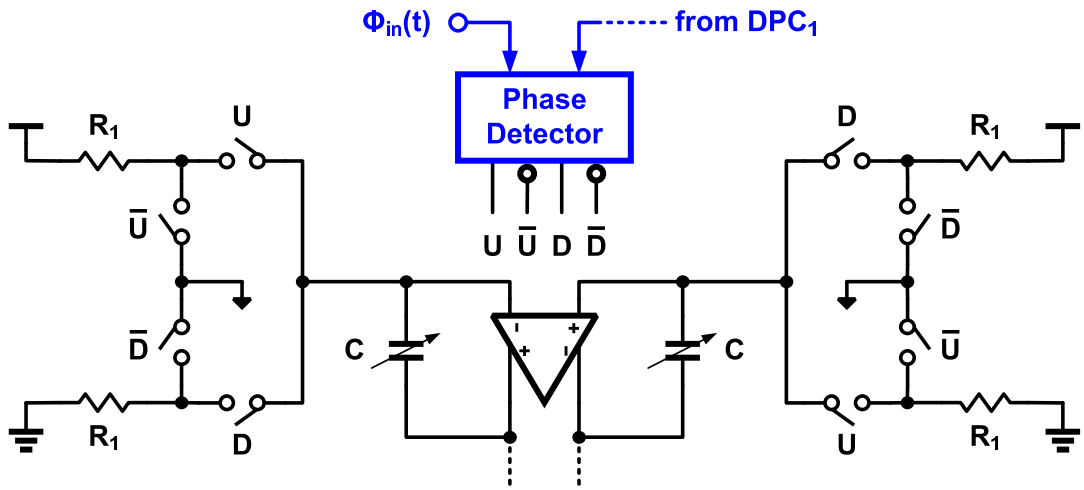


Figure 3.8: First integrator and switch-resistor circuit details.

3.2.3 Switched-R Phase-to-Current Converter

Implementation of the switched-R phase-to-current converter circuit is shown in Fig. 3.8. It linearly transforms PFD output information into current pulses of fixed amplitude and variable width. Switches connect resistors between V_{DD} or V_{SS} to either analog ground or integrator virtual ground. The U and D phase detector signals control the time duration and polarity of the switched-R current pulses. Switch ON resistance and its voltage drop, ΔV, were designed to be a fraction of the total resistance to minimize nonlinearity. Shown in Fig. 3.9, switches are placed at the virtual ground according to *Option 2* to minimize the impact of OFF state switch leakage. Switching the resistor according to *Option 1* would have resulted in error charge from C_p being injected into the integrator. Further, the PR-CT$\Delta\Sigma$ TDC architecture is designed to activate the switched-R current pulses during TI 2 or 3.

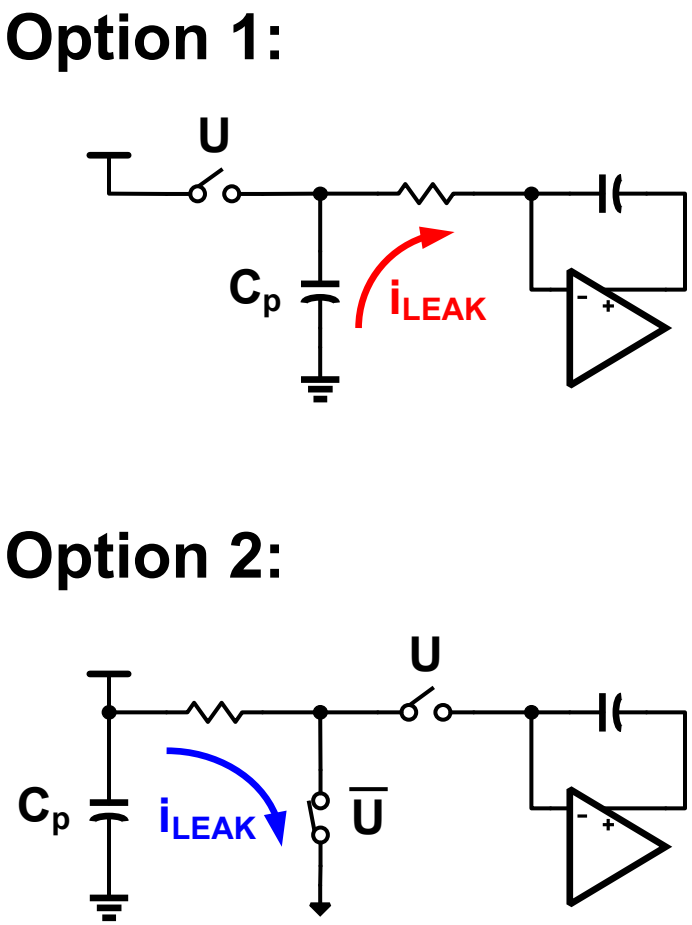


Figure 3.9: Schematic depicting the impact of parasitic capacitor charge leakage on switch location.

3.2.4 Op-amps

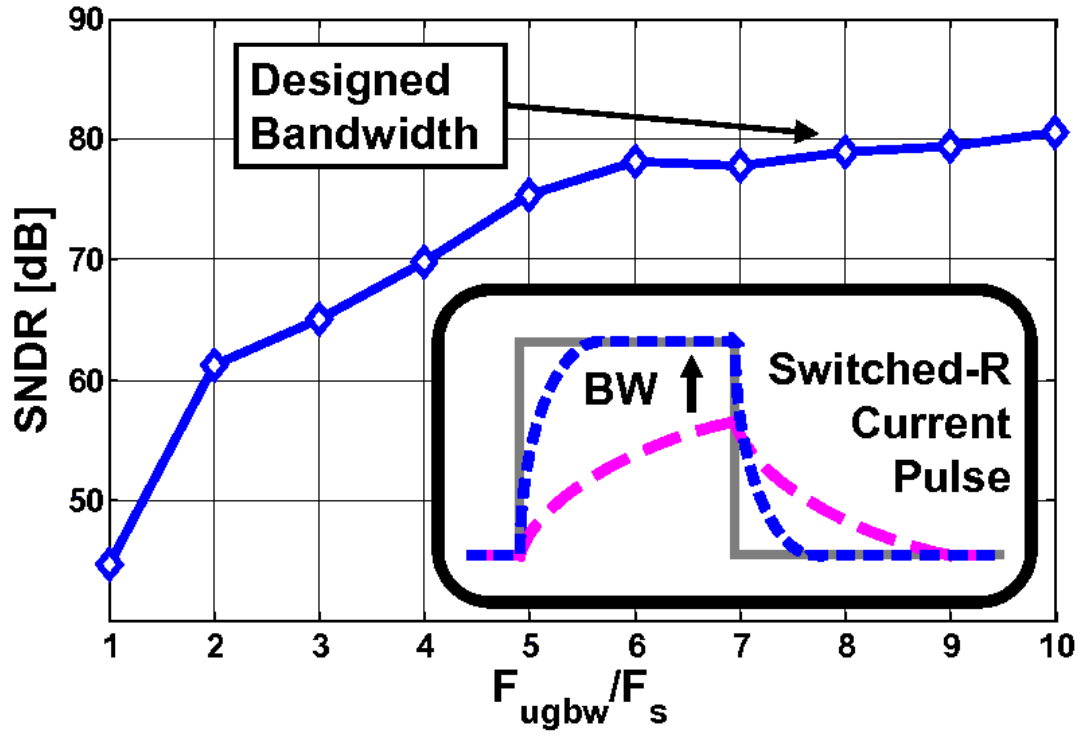


Figure 3.10: SNDR dependence on op-amp unity gain bandwidth to sampling frequency ratio.

The first and second active integrator op-amps employ a fully differential Miller compensated two-stage amplifier with telescopic cascode first stage and class-A output stage. Extracted simulations shows 60 dB DC gain for both op-amps with 1.3 GHz and 500 MHz unity gain bandwidth for the first and second op-amps, respectively. Figure 3.10 shows simulated SNDR versus first op-amp unity gain bandwidth to sampling frequency ratio, and demonstrates that high op-amp gain bandwidth is required to maintain the integrity in reconstruction of the switched-R current pulses.

3.2.5 Loop Filter

A second-order continuous-time (CT) loop filter processes the input signal and quantization noise. The impulse invariant transform converts the double integration discrete-time loop filter to CT (3.1) with DAC pulse shape parameters $(\alpha, \beta) = (0.25, 0.75)$ [26].

$$H(z) = \frac{-2z+1}{(z-1)^2} \Longrightarrow H(s) = \frac{-(3s+4)}{s^2} \tag{3.1}$$

The equivalent voltage-domain DAC pulse shape is quarter-delay return-to-zero (QRZ). The switched-R block, capacitors, and op-amp form both loop filter active-RC integrators. Externally variable voltage reference and programmable binary weighted capacitors are used to tune RC time constant variations.

3.2.6 Phase Management

An I/Q phase generator is used to create reference phases, Φ_{ref+} and Φ_{ref-}, and quantizer clock phase, Φ_{clk}, from a $2X$ clock input source. Upon startup, a separate synchronize bit controls phase detector initialization ensures that the input signal Φ_{in} lies between reference phases, Φ_{ref+} and Φ_{ref-}.

3.3 Measurement Results

A prototype IC was fabricated in a low-power 90 nm CMOS process. An arbitrary waveform generator (AWG) provided a 312.5 MHz reference clock and a 156.25 MHz phase modulated clock. The phase modulated clock was low-pass filtered by an external PLL in an attempt to suppress harmonics of the signal

generator and convert the AWG phase modulated sine waveform to a square waveform. Measurements of the AWG and PLL combination showed an input signal attenuation of ∼0.5 dB, and an insignificant contribution to AWG phase noise.

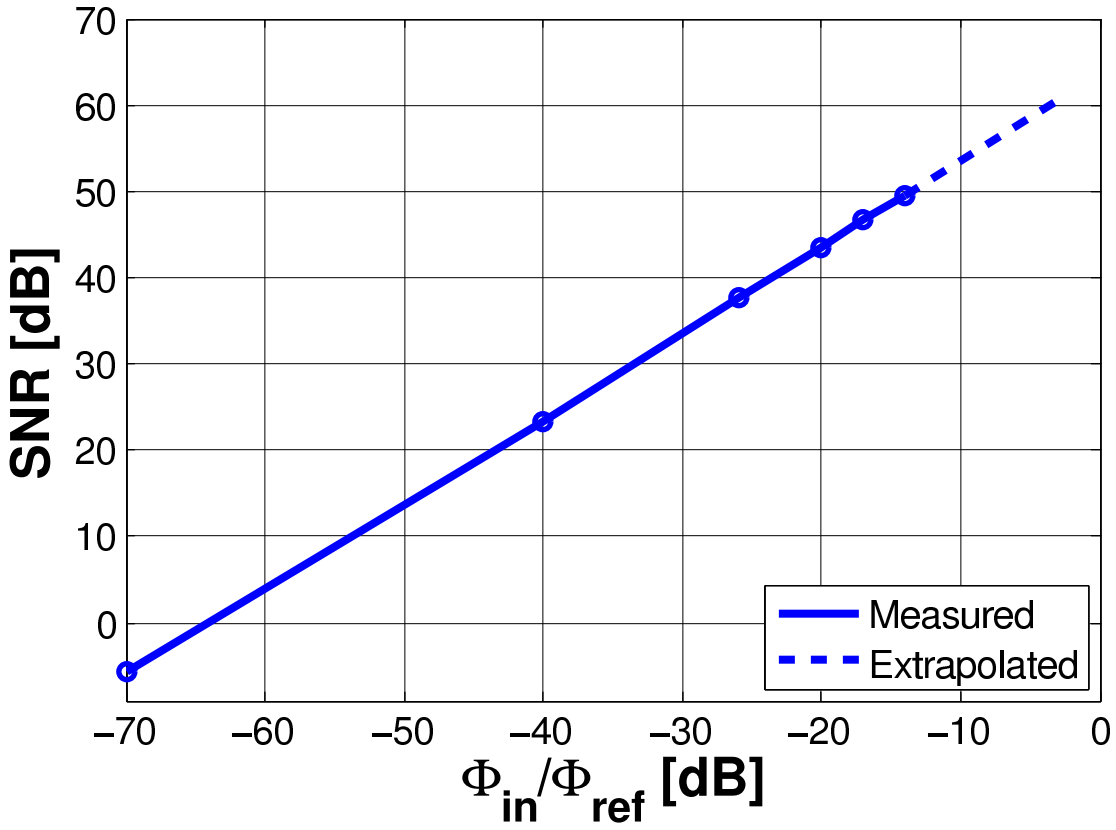


Figure 3.11: Plot of SNR versus input magnitude.

A 153 kHz sinusoidally phase modulated input signal was applied to the PR-CTΔΣ TDC. The TDC demonstrated 50 dB SNR with -14 dB input signal, and 64 dB dynamic range (limited by signal source phase noise and distortion). SNR performance versus input amplitude is plotted in Fig. 3.11. Static phase offset, harmonic distortion, and high phase noise of the signal source prevented meaningful measurement of SNR and SNDR over the full dynamic range.

The measured output spectrum with -40 dB FS input signal is plotted in Fig. 3.12. For reference, a simulated spectrum with 0.1% RMS jitter is included

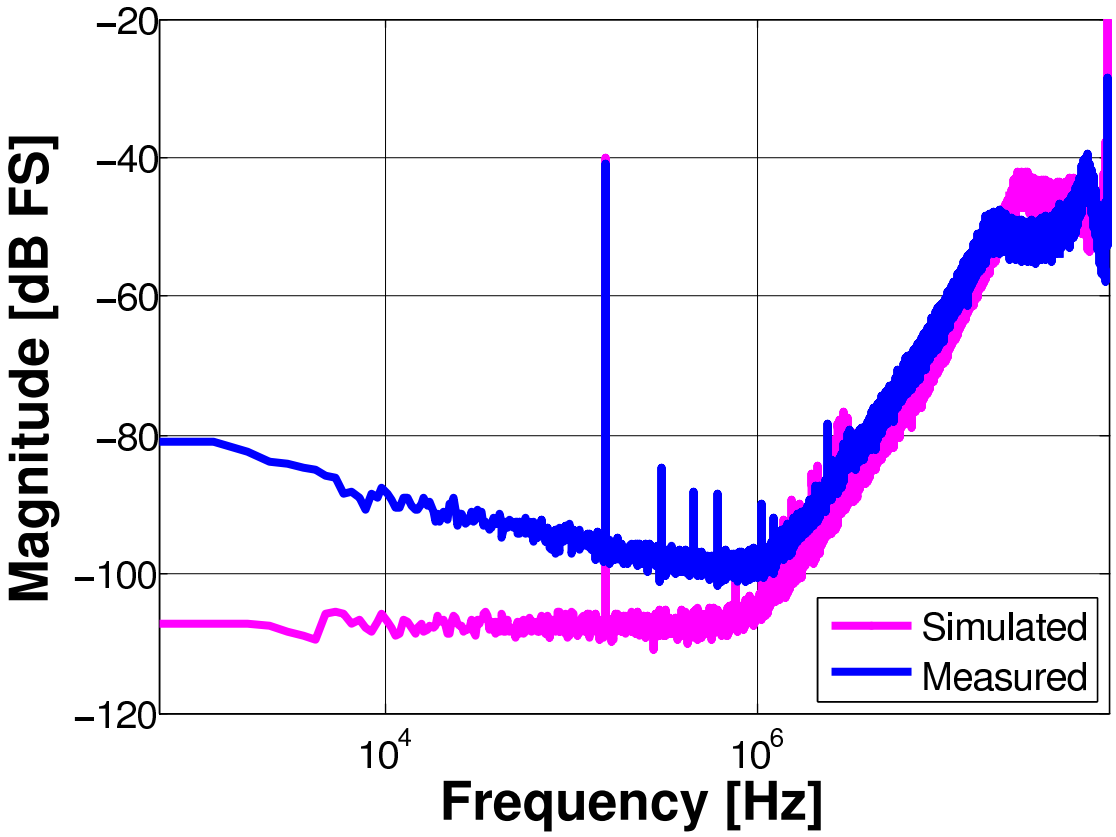


Figure 3.12: Measured spectrum of 32 ps pk-pk, 153 kHz sinusoid phase modulated input signal, and simulated spectrum with 0.1% RMS jitter.

in Fig. 3.12. As shown in Fig. 3.13, harmonic tones in the output spectrum are indistinguishable from distortion introduced by the signal source. Poor signal source phase noise also degrades TDC performance by increasing the in-band noise floor.

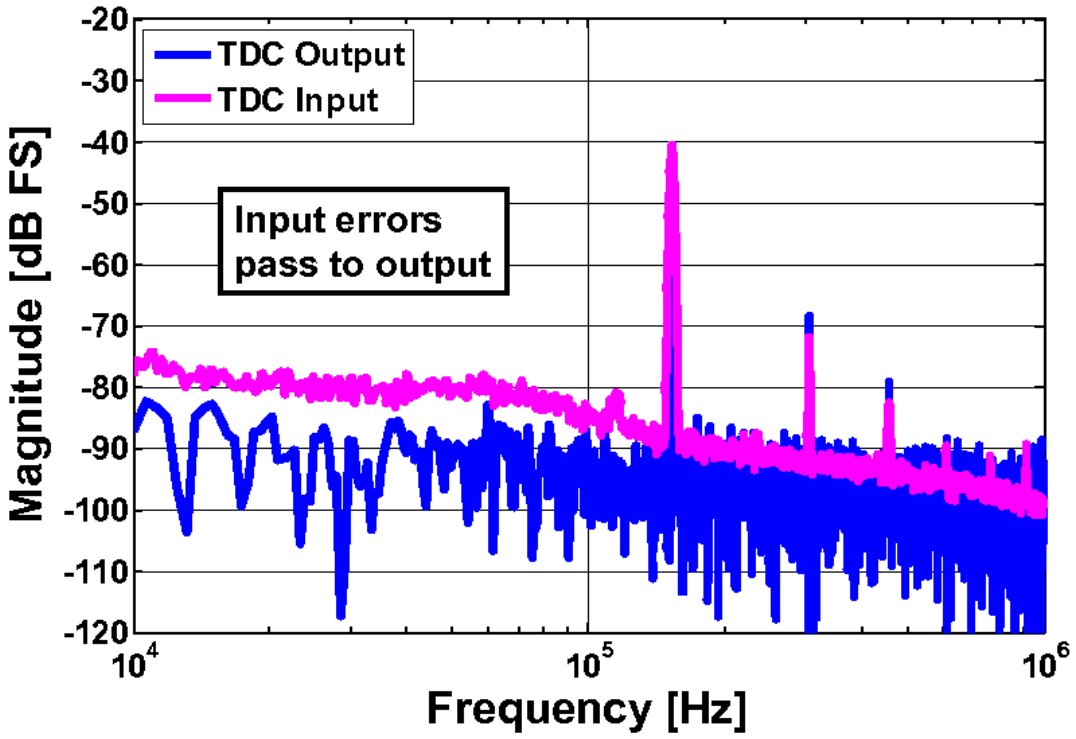


Figure 3.13: Comparison of TDC output spectrum with input signal source spectrum.

Performance of the phase-reference CT$\Delta\Sigma$ TDC is summarized in Table 3.1, and a die photograph is shown in Fig. 3.14.

3.4 Summary

A second-order continuous-time $\Delta\Sigma$ TDC using phase-domain reference signals has been proposed. This design introduced the concept of using phase as the modulator reference, and the feasibility of higher order noise-shaping in TDCs.

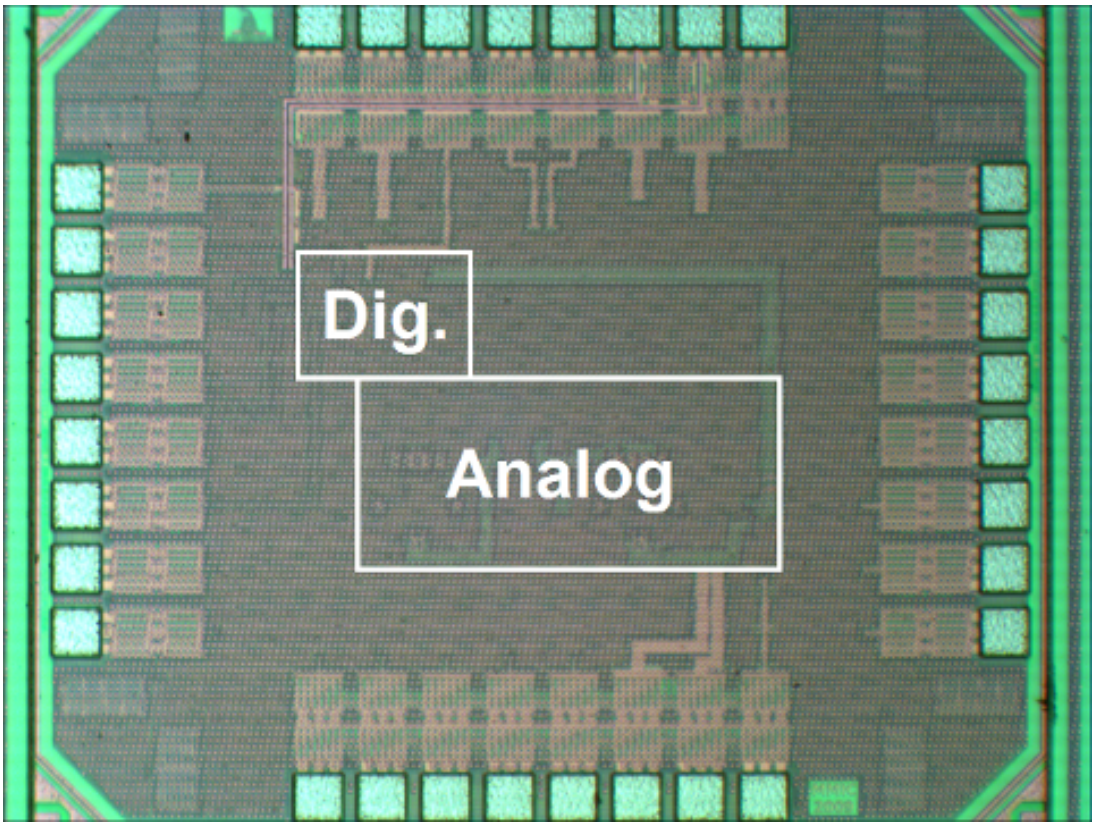


Figure 3.14: Die photograph.

Table 3.1: Performance Summary

Bandwidth / F_s (MHz)	1.0 / 156.25
Full scale range	3.2 ns
Resolution	2.4 ps*
DR (dB)	64
Power Supply	1.2 V
Power consumption	1.3 mW (A) / 0.8 mW (D)
Process	LP 1P9M 90nm CMOS
Active die area	0.12 mm^2 (0.26×0.45 mm)

*Limited by signal source.

The proposed architecture allows the PFD to operate in its most linear region, improving distortion performance. The measured results of the prototype IC fabricated in an LP 90 nm CMOS process show a resolution of 2.4 ps over a 3.2 ns range in a 1 MHz bandwidth with 2.1 mW power consumption from a 1.2 V supply.

CHAPTER 4. VCO-BASED ANALOG-TO-DIGITAL CONVERTERS

Of recent interest in the field of analog-to-digital converters research is a class of time-based, noise-shaping signal processing circuits generally referred to as the VCO-based ADC. The genesis of this *nom de plume* comes from the inclusion of one or more tuneable oscillator circuits, often voltage-controlled, within the data converter, which perform essential signal processing functions in the time-domain.

This chapter explores the two general types of noise-shaping VCO-based ADCs. The first type generates a digital output code proportional to oscillator frequency and is known as a VCO Quantizer, whereas the second type develops a digital output code proportional to oscillator phase and is known as a VCO Integrator. These tuneable oscillator based circuits have highly nonlinear transfer characteristics leading most VCO-based ADC research into improving linearity performance. Further, this chapter also discusses existing methods used to combat oscillator nonlinearity.

4.1 VCO Quantizer

The VCO Quantizer is the first iteration of VCO-based ADCs [5]. It is also known as an open-loop VCO-based ADC or a frequency delta-sigma modulator (FDSM) because it generates digital output codes proportional to oscillator frequency. It is also observed that the VCO Quantizer signal transfer function is approximately unity for signals less than the Nyquist frequency and a sinc low

pass transfer function for high frequency input signals.

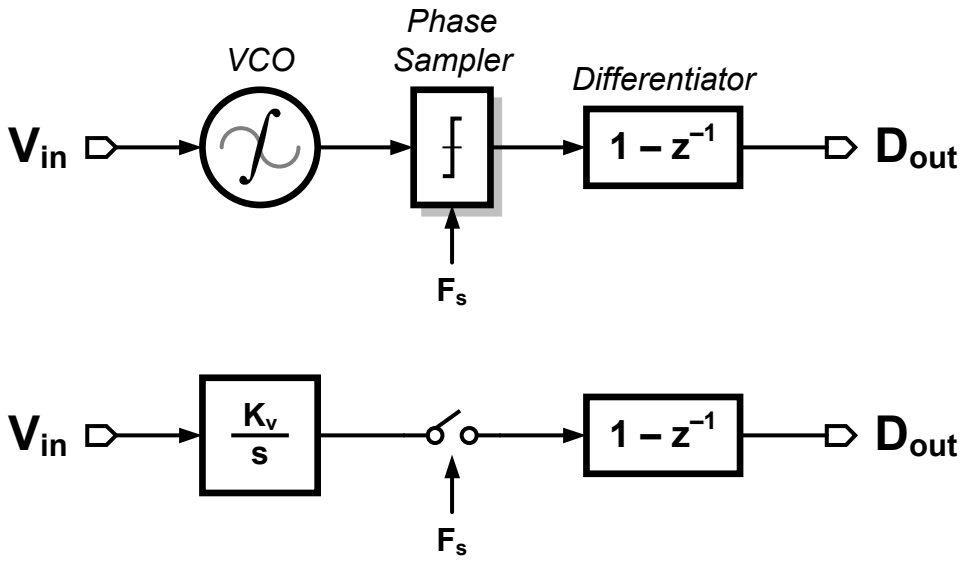


Figure 4.1: VCO Quantizer block diagram and linear model.

Figure 4.1 shows the block diagram and simplified linear model of a VCO Quantizer. It consists of a voltage-controlled oscillator, phase quantizer or counter, and first-order difference block. The voltage-controlled oscillator functions as an ideal integrator in the phase domain with linear transfer function,

$$\frac{\Phi_{out}(s)}{V_{in}(s)} = \frac{2\pi \cdot K_v}{s}, \tag{4.1}$$

where K_V has units Hz/V.

The phase quantizer/counter block can be implemented as a single-bit quantizer by sampling oscillator phase at rate F_s using a DFF phase detector. Quantizer resolution can be enhanced through use of multi-bit quantization techniques. The simplest version counts oscillator phase increments of 2π. Using this method, quantizer range can be indefinitely expanded constrained only by the maximum conversion time and counter resolution. Another method samples each phase of a multi-phase oscillator, increasing resolution to a fraction of 2π. Both methods can

be combined to further increase quantizer resolution.

To increase resolution in a traditional voltage-based Flash ADC, each comparator must discriminate between voltage intervals separated by $V_{LSB} \propto V_{DD}/2^M$. As V_{DD} continues to decrease with process technology, mismatch induced input referred offset become comparable to the quantizer LSB. This leads to missing codes and loss of quantizer monotonicity. The attractiveness of these phase quantization methods is their ability to discern between signals on the order of the full supply voltage for all oscillator phases except the output in transition, reducing quantizer metastability [27].

The final block of the VCO Quantizer follows the phase sampler and performs discrete-time differentiation, $1 - z^{-1}$, of sampled phase. In one method, this differentiation may be performed by summing the quantized phase outputs at each sampling instance followed by explicitly subtracting the present/previous binary coded decimal (BCD) numbers. Alternatively, an exclusive-OR gate can perform a one bit digital differentiation of present/previous individual quantized phases, which are then subsequently summed. Interestingly, this approach generates a rotating pattern indicating which oscillator phases have changed between samples [28]. When a VCO Quantizer with the XOR differentiation technique is used in a delta-sigma feedback loop, the VCO Quantizer's rotating pattern can shape feedback DAC mismatch errors through dynamic element matching [29].

Tracing the input signal in the linear model, shown in Fig. 4.1, the input is integrated, quantized, and differentiated. The back end z-domain differentiation negates the input integration, and the phase sampler introduces a zero-order hold function to the input signal. This zero-order hold (ZOH) function exhibits sin(x)/x filtering in the frequency domain and yields first order anti-aliasing of the input signal. The resulting digital output codes (Dout) are proportional to input voltage

and oscillator frequency with $F_{osc} = K_v \cdot V_{in}$. However, voltage-controlled oscillator gain, K_v, is a nonlinear function of V_{in} and causes significant harmonic distortion.

4.2 Non-Ideal Effects

While VCO-based ADCs have demonstrated supply voltage independent dynamic range and improved quantizer metastability, they have have two non-ideal effects which degrade ADC performance. The first one is VCO gain nonlinearity, and the second one is an in-band noise floor introduced by VCO phase noise, $S_{\Phi vco}$. Nonlinear VCO Gain creates very large harmonic terms limiting ADC resolution to as low as four to five bits. Together VCO nonlinearity and phase noise are the dominant low frequency noise sources limiting signal-to-noise plus distortion ratio (SNDR), and they must be addressed to make VCO-based ADCs a viable option in high resolution and wide bandwidth ADCs.

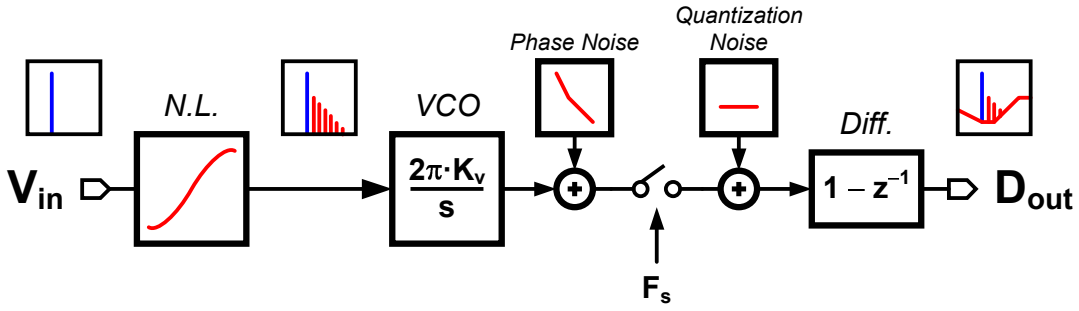


Figure 4.2: Block diagram of a VCO Quantizer showing error sources and their effect on the output spectrum.

Figure 4.2 shows the block diagram of a VCO Quantizer with error sources including K_v nonlinearity, VCO phase noise, and quantization noise. Each error source affects the ADC output in different ways depending on its insertion point in the system. Uniformly distributed, white quantization noise is added after

the phase sampler and passes through a digital differentiator. This first order differentiation selectively filters the high frequency quantization noise, and when combined with oversampling, it reduces in-band quantization noise.

Also shown in Fig. 4.2, phase noise is added at the VCO output and prior to sampling. Phase noise is a type of colored noise and is characterized by three distinct carrier frequency offset regions. The first region is close-in phase noise. It is characterized by a $1/f^3$, -30 dB/dec slope, where f is frequency, and it is composed of integrated flicker noise of the oscillator devices. The second region is mid-range phase noise. It is characterized by a $1/f^2$, -20 dB/dec slope and is composed of integrated thermal noise of the oscillator devices. The third region, not shown in Fig. 4.2, is a zero slope region with noise sources originating in VCO output buffers, which are not integrated. The succeeding phase sampler folds back phase noise from higher order harmonics of the carrier frequency, but fortunately their low relative noise powers add a negligible amount of noise. After sampling, the digital differentiator removes one order of integration and converts $1/f^3$ and $1/f^2$ to $1/f$ and white noise at the ADC output, respectively. Phase noise can alternatively be modeled as an additive VCO input noise source.

Modeling a VCO Quantizer in Matlab/SIMULINK is a straightforward exercise. Input referred phase noise and VCO nonlinearity can be modeled with existing blocks to create a fast, robust model. Figure 4.3 shows the normalized magnitude of a 16-phase VCO Quantizer with multi-phase quantization and additive phase noise. A modest -100 dBc/Hz @ 1 MHz additive phase noise with $1/f^3$ flicker noise corner of 5 MHz is applied as an input referred quantity to the VCO input. The linear VCO gain is set at a reasonable 1.067 GHz/V, and the input full scale range is ± 0.3 V.

In the output spectrum, the differentiated $1/f^3$ phase noise appears as $1/f$

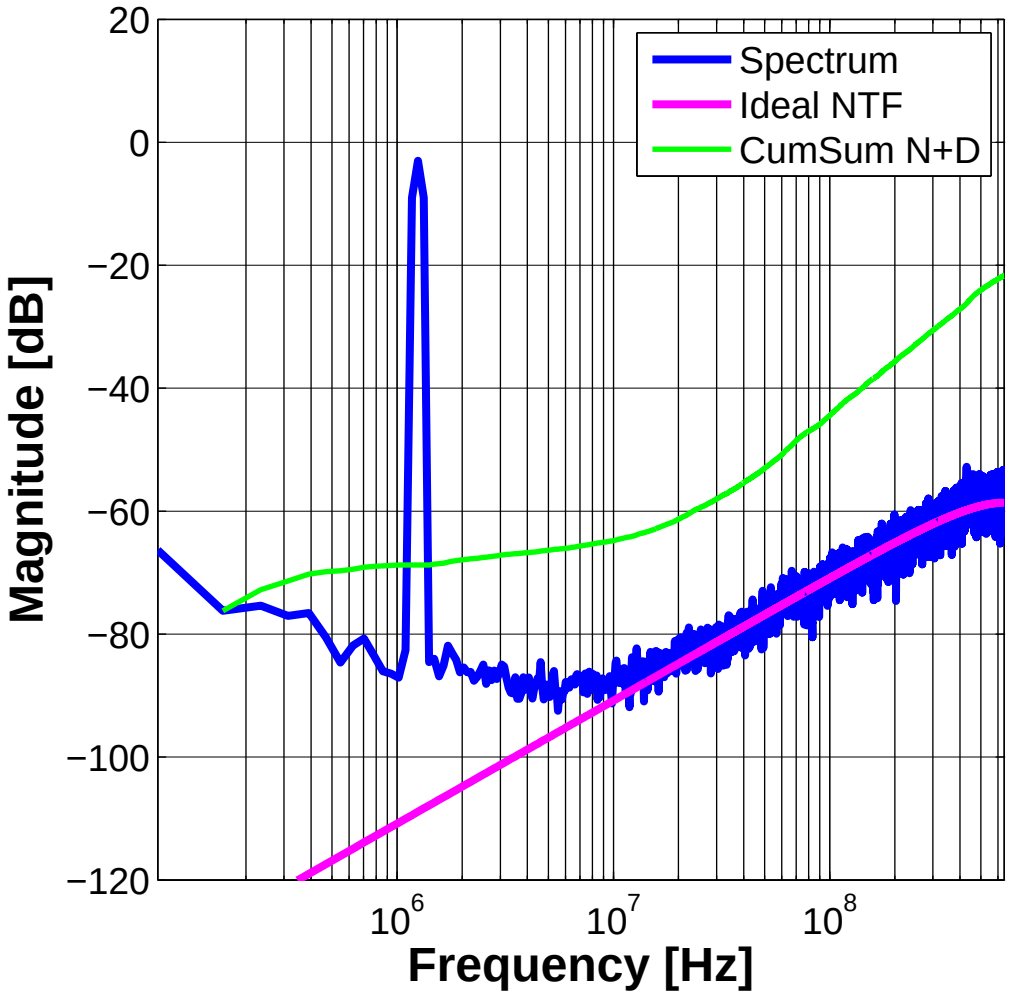


Figure 4.3: Spectrum of VCO Quantizer with VCO phase noise.

noise from low frequency to 5 MHz. Differentiated $1/f^2$ noise dominates the noise floor until about 10 MHz where the quantization noise becomes dominate. This low frequency noise floor can be decreased by dissipating more power in the VCO to reduce phase noise, increasing K_v independent of K_v, or decreasing the VCO zero input frequency, f_0. In reality, VCO phase noise is strongly coupled to system parameters, K_v and f_0, and the only practical method to decrease low frequency, in-band noise is to consume more power in the VCO.

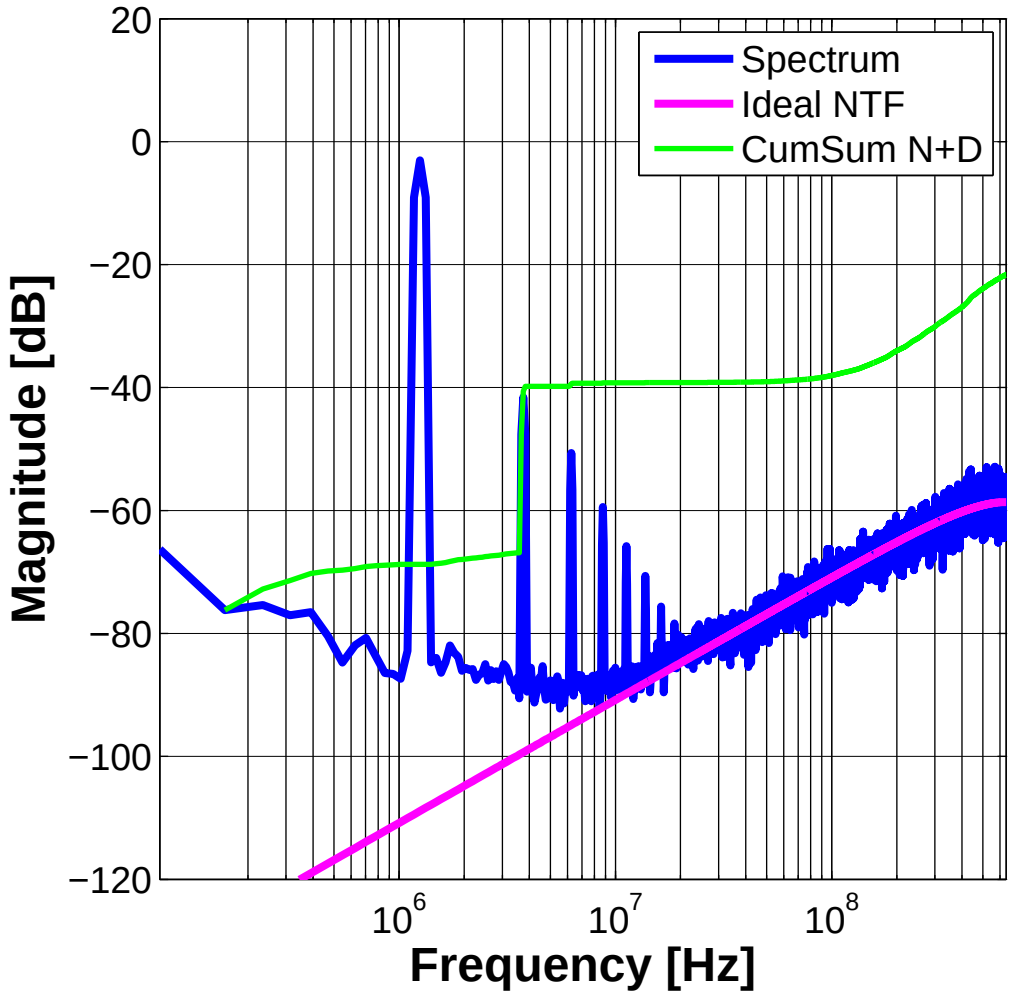


Figure 4.4: Spectrum of VCO Quantizer with nonlinear VCO gain and VCO phase noise.

Figure 4.4 shows the effect of nonlinear VCO gain on the output spectrum of a VCO Quantizer. Even and odd order harmonics are evident and degrade SNDR performance by ¿25 dB. Without nonlinearity correction, the VCO Quantizer would be left in the novelty bin with little chance of displaying its merits.

4.3 Nonlinearity Mitigation Techniques

Auspiciously, out of the smoldering heaps of failed research attempts arise new opportunities. This continues to be the case with VCO Quantizer ADCs and nonlinear VCO gain. The first measured results with $f_s = 2$ MHz and OSR = 2000 showed that for a -35 dB FS input the SFDR was 80 dB; however, with a -3 dB FS input, the SFDR decreased to 44 dB [5]. The past several years have seen several techniques developed to address this disparity in performance. Each technique has the goal of reducing harmonic distortion and promoting acceptance of VCO-based ADCs in the wide bandwidth delta-sigma universe. The following subsections highlight techniques designed to mitigate VCO gain nonlinearity.

4.3.1 Feedback

A common approach to linearize nonlinear circuits is to use negative feedback and high loop gain. Figure 4.5 shows a nonlinear element preceded by high gain, A, in a negative feedback loop. The use of negative feedback and high gain reduces input referred nonlinearity. This essential linearizing technique is foundational to delta-sigma modulators in suppressing quantizer nonlinearity.

In [30], a Gm-C integrator and VCO Quantizer ADC formed a second-order

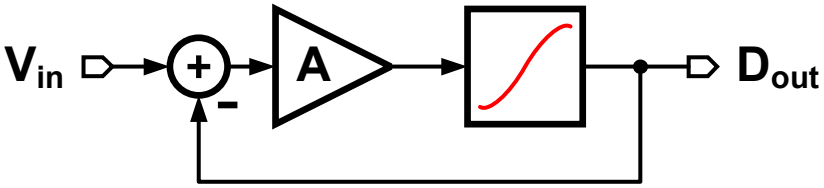


Figure 4.5: Block diagram of high gain loop filter and negative feedback used to suppress nonlinearity.

$\Delta\Sigma$ ADC in 0.6 μm CMOS. While the VCO Quantizer was described to use a counter based quantizer, the authors noted that the multi-bit VCO Quantizer output was requantized to facilitate a linear single bit feedback DAC. Unfortunately, this design was only simulated and not fabricated with simulation results indicating an ordinary 59 dB SNR in 5 MHz bandwidth.

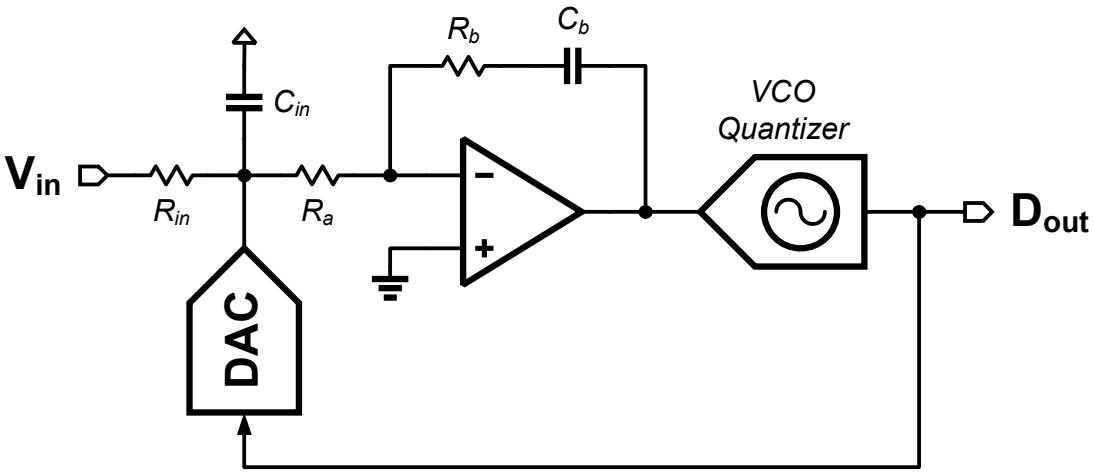


Figure 4.6: Block diagram of a third order feedback system to suppress VCO gain nonlinearity.

Expanding on ideas presented in [30], Figure 4.6 shows a second-order delta-sigma loop filter and VCO Quantizer, and they are used to produce a third-order noise shaped ADC in 0.13 μm CMOS [29]. The circuit contains three integrators: passive-RC, active-RC, and VCO. The integration of the VCO is nullified

by discrete differentiation. The loop is stabilized with a zero formed by resistor R_b and capacitor C_b. A second feedback DAC (not shown) forms a fast feedback loop around the VCO Quantizer to compensate for a full clock cycle delay created by the VCO Quantizer and primary feedback DAC. Feedback DAC mismatches are noise shaped with the implicit rotational pattern generated with exclusive-OR digital subtraction [28].

This circuit achieves third order noise-shaping with one order coming from the VCO Quantizer. The other two are derived from a passive-RC integrator and active-RC integrator. At first glance, the passive-RC integrator appears to have some attractive low power integration benefits; however, it has no gain and cannot suppress VCO gain nonlinearity. Further, its pole frequency must be set at or beyond the intended signal bandwidth in order to minimize input referred noise amplification [31]. In this approach, loop gain burden is shifted from the passive-RC integrator to the active-RC integrator which struggles to suppress loop nonlinearities, especially near the signal band edge. The prototype circuit achieved 86 dB peak SNR and 72 dB peak SNDR in a 10 MHz bandwidth consuming 40 mW.

4.3.2 Pseudo-Differential

With many implementations of VCO Quantizers having single ended inputs, their outputs contain significant even order distortion. This can be seen in the example spectrum of Fig. 4.4. A single tone sinusoid passing through a nonlinear system will produce addition terms at all harmonics according to

$$f(x) = a_0 + a_1 \cdot x + a_2 \cdot x^2 + a_3 \cdot x^3 + ... \tag{4.2}$$

Figure 4.7 shows a block diagram of two identical nonlinear ADCs operating

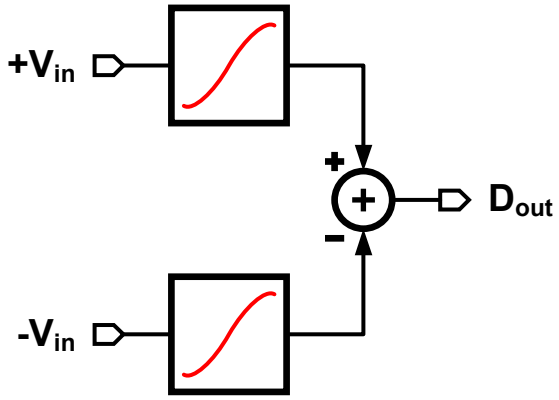


Figure 4.7: Block diagram of a pseudo differential architecture used to suppress even order harmonics.

in pseudo differential fashion. Positive input signal is applied to the top most ADC, and negative input signal is applied to the bottom ADC. Removal of the DC offset and even order harmonics follows Equation (4.3).

$$\begin{aligned} f_+(x) &= a_0 + a_1 \cdot x + a_2 \cdot x^2 + a_3 \cdot x^3 + ... \\ f_-(x) &= a_0 - a_1 \cdot x + a_2 \cdot x^2 - a_3 \cdot x^3 + ... \\ f_{out} &= f_+(x) - f_-(x) \\ &= 2a_1 \cdot x + 2a_3 \cdot x^3 + ... \end{aligned} \tag{4.3}$$

It is instructive to note that after taking the difference of the two paths, the signal power is increased by 6 dB. However, the inclusion of a second ADC and its uncorrelated noise sources, increases total noise power by 3 dB. Net SNR is improved by 3 dB, and even order harmonic distortion is eliminated at the expense of a doubling in power consumption. There is no clear benefit of the pseudo differential technique with respect to SNR improvement alone, as similar SNR increase can be obtained by doubling power consumption in a single ADC. This technique has demonstrated excellent even order harmonic rejection in recent VCO-

based ADCs [32, 33, 34, 35, 36].

4.3.3 Estimation

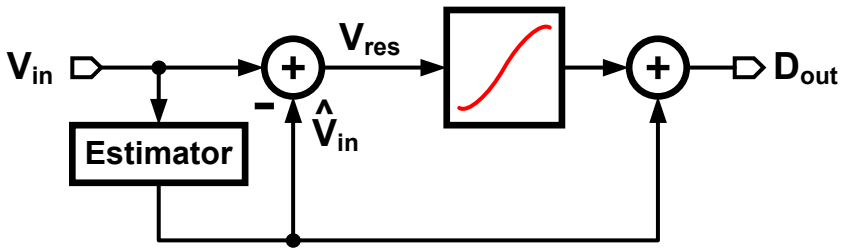


Figure 4.8: Block diagram of an estimation technique that subtracts an input signal estimate from the input in order to reduce distortion produced by the nonlinear circuit.

Figure 4.8 shows a block diagram of a nonlinearity suppression technique which uses estimation and feed forward to reduce harmonic distortion. The Estimator block generates a low latency appraisal of the input signal. This estimated value is subtracted from the input signal to produce a residue value that is processed by the nonlinear ADC. Because this residue is a small fraction of the original input signal, the nonlinear ADC generates little harmonic distortion.

A residue-cancelling VCO-based quantizer used this estimation technique together with feedback and pseudo differential VCO Quantizers to create a high resolution and width bandwidth VCO-based delta-sigma ADC [35]. The measured second order prototype results demonstrated 76.6 dB SNDR in 10 MHz signal bandwidth with an over sampling ratio of 30 and power consumption of 16 mW.

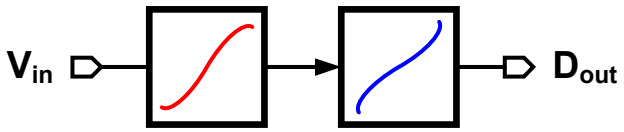


Figure 4.9: Block diagram of an error correction technique which calculates and applies an inverse nonlinear function.

4.3.4 Error Correction

Another method seeks to eliminate harmonic distortion by using calibration to generate an inverse nonlinear transfer function to undo ADC nonlinearity [32, 36]. The simple block diagram in Fig. 4.9 shows a nonlinear ADC cascaded with an inverse nonlinear transfer function. To the level of accuracy of the inverse nonlinear transfer function, the resultant system output is linear. Most implementations rely on matching a replica nonlinear ADC to the online ADC. This replica ADC can be calibrated in the background without data conversion interference, with the results begin applied to the online ADC output.

4.3.5 Two-Level Modulation

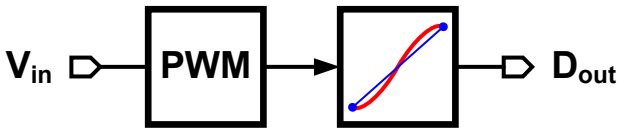


Figure 4.10: Block diagram of two level modulation technique which linearizes a nonlinear element by only operating at two distinct points.

This two-level modulation techniques relies on the time honored, stalwart principle that any two points define a straight line and is by definition linear.

Figure 4.10 shows the block diagram of a system where an input signal is linearly converted to a pulse width modulated (PWM) signal that is applied to a nonlinear ADC. Assuming rise and fall times of the PWM signal are small, the nonlinear ADC is only operated at two distinct points of its input range. This effectively

An example of two-level modulation used to reduce VCO gain nonlinearity is found in the proposed VCO-based ADC [34]. It uses naturally sampled PWM generator followed by a switched ring oscillator VCO-based ADC to bypass VCO gain nonlinearity by operating the VCO at two points. In practice, finite rise/fall times will cause the VCO to operate in the nonlinear region for short periods. The measured results of the prototype ADC demonstrated 59.1 dB SNDR in 8 MHz bandwidth with an over sampling ratio of 40 and power consumption of 4.3 mW.

4.4 VCO Integrator

Through the short history of VCO-based ADCs the VCO Quantizer has been the preferred realization of this class of time-based ADCs. The VCO Quantizer samples and differentiates VCO phase to create a digitized output. Noting that frequency is the first derivative of phase, this digital output is proportional to VCO frequency with the input to output gain being the unit-less quantity $K_v T_s$, where T_s is the sampling period. Maximizing the VCO Quantizer's full dynamic range requires exercising the full range of nonlinear VCO gain. However, if sampled VCO phase is not explicitly differentiated but instead used directly, a small input signal applied to the same K_v yields very large phase changes. This leads to the enhanced use of voltage-controlled oscillators as integrators.

Figure 4.11 shows a simplified block diagram of VCO Integrator operating within a negative feedback loop to form a first order delta-sigma modulator. The

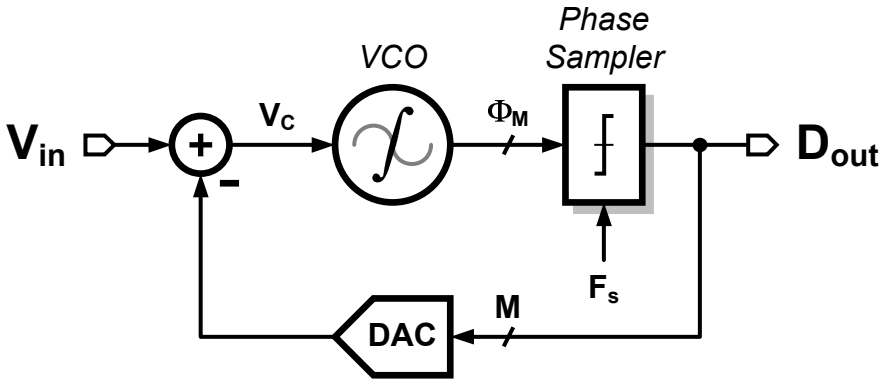


Figure 4.11: Block diagram of VCO Integrator architecture with phase sampler and negative feedback.

VCO functions as an ideal phase domain integrator with transfer function $2\pi K_v/s$. Its output phase is sampled by a phase sampler which discriminates between levels proportional to supply voltage and greatly reduces metastability errors. Note that the term VCO Integrator may refer to a VCO circuit with or without output phase sampling. Next, the feedback DAC output signal is subtracted from the input, and the residue supplied to the VCO input. This small residue, which is nothing more than the DAC quantization error, exercises only a minimal region of the nonlinear K_v characteristic helping to suppress harmonic distortion. Nonlinearity suppression can be further enhanced with the addition of a high gain loop filter preceding the VCO Integrator.

Addition of a high gain loop filter in advance of a VCO Integrator was proposed in [37]. Figure 4.12 shows the block diagram of a fourth-order noise-shaping $\Delta\Sigma$ modulator composed of a third-order feed forward analog loop filter and 15-stage VCO Integrator with phase quantizer. With the any VCO Integrator architecture, there is an important point of distinction to make. The input of the VCO Integrator is a high impedance and does not form a low impedance virtual ground.

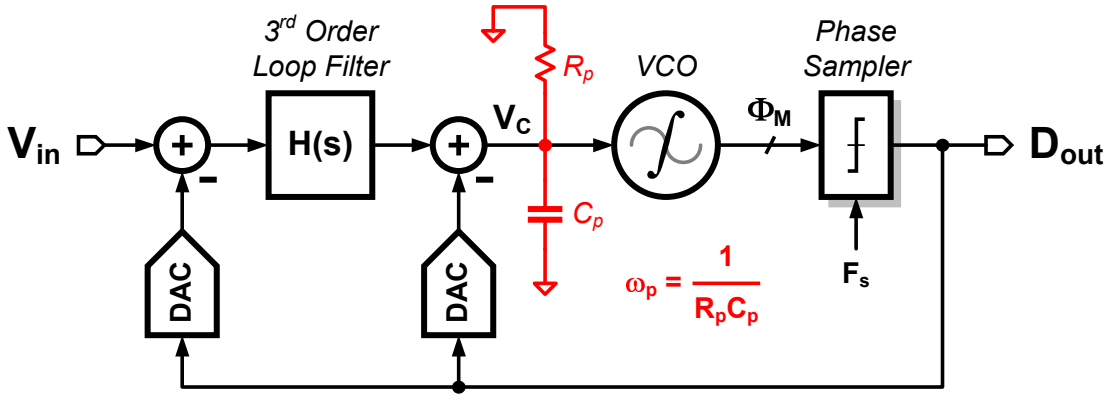


Figure 4.12: Block diagram of a delta-sigma modulator with VCO Integrator and additional parasitic loop filter pole.

In case of the ADC shown in Fig. 4.12, a low value shunt resistor, R_p, is added to the VCO Integrator input in an attempt to reduce parasitic pole introduced by C_p [38]. This pole, $1/(R_pC_p)$ introduces additional loop delay which causes the delta-sigma modulator to tend toward instability. An additional side effect of this loop delay is increased power consumption to drive R_p.

A prototype fourth-order delta-sigma modulator was designed in 0.13-μm CMOS [37]. This circuit operates with a sampling frequency of 900 MHz and signal bandwidth of 20 MHz. Operating with a 1.5 V supply and consuming 87 mW, the modulator achieves 81.2 dB peak SNR, 78.1 dB peak SNDR, and ¿85 dB dynamic range limited by ISI generated in-band tones. ISI generated tones appear through the use of explicit DWA to counteract DAC mismatch. When the number of active DAC levels exceeds half of the full scale range, one or more DAC cells remain on from the previous conversion resulting in signal dependent ISI charge injection. This design is the first high performance ADC example using a VCO Integrator with phase output to mitigate VCO gain nonlinearity. Another notable design is found in [39].

4.5 Switched Ring Oscillator Architecture

At the heart of two recent advances in time-based data converters is the Switched Ring Oscillator (SRO) [34, 23]. Prior art of the Gated Ring Oscillator [22] used the input signal to turn on/off oscillator. Preserving the oscillator phase state between conversions and sample-to-sample differentiation yielded quantization noise-shaping. In functional implementations, oscillator phase state is not accurately preserved during oscillator stoppage, leading to quantization noise leakage.

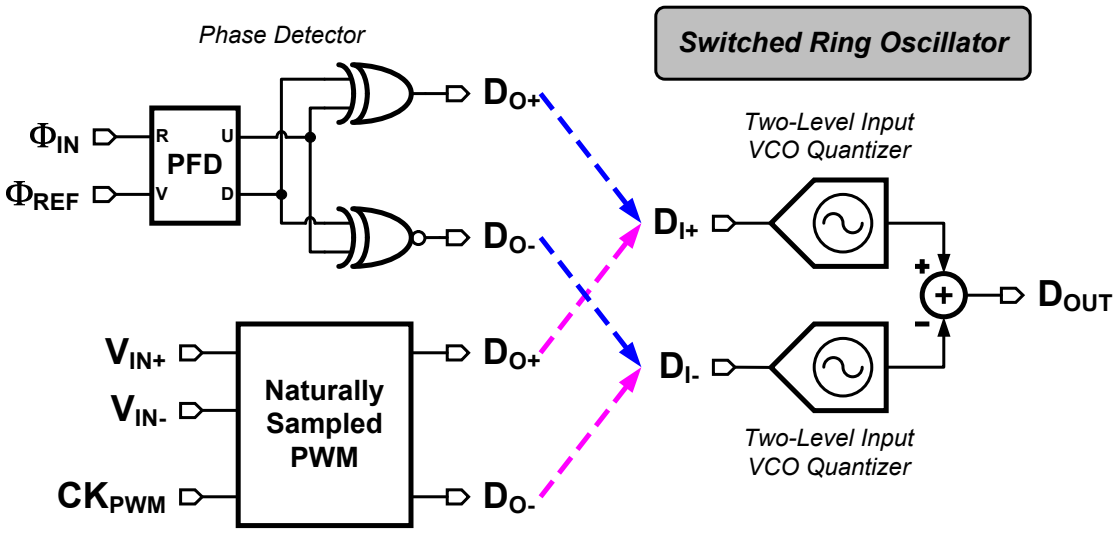


Figure 4.13: Phase detector and naturally sampled PWM front end with two-level switched ring oscillator ADC back end, implementing a TDC and ADC respectively.

To alleviate the problems of phase state preservation, the authors of [34, 23] proposed to not completely stop the oscillator, but instead operate the oscillator at two widely spaced non-zero frequencies. This eliminates phase state leakage because at low frequency the oscillator continues to accumulate phase, albeit at a

slower rate. Figure 4.13 shows the block diagram of the proposed SRO TDC and PWM VCO-based ADC. Both designs share a common two-level input Switched Ring Oscillator back end with their respective phase and voltage front ends.

Using two VCO Quantizers in a pseudo differential manner reduces even order harmonic distortion and power supply transients. While one VCO Quantizer's VCO is running at its highest frequency, the other is running at its slowest frequency. When the front end circuit switches polarity, the oscillators switch their frequency. Low impedance NMOS switches are used to switch rapidly between two voltage references to maintain near constant supply current and minimal power supply ripple.

The Switched Ring Oscillator's individual VCO Quantizer block diagram is shown in Fig. 4.14. It consists of a 4-stage pseudo differential, feed forward resistor coupled, voltage controlled ring oscillator; a phase sampler; a transition detector; a ROM encoder; and a digital differentiator. The VCO high side supply voltage is fixed at 1.2 V. A two-level digital input switches the VCO low side supply voltage from some high potential which is less than 1.2 V (for slow frequency) to a low potential which is greater than or equal to 0 V (for high frequency). The switches are constructed with NMOS transistors for high speed operation.

A phase sampler, constructed using a sense amplifier flip-flop [40], periodically samples VCO phase. Figure 4.15 shows the phaser representation of a four stage ring oscillator with eight quantized states. In the example figure, oscillator phase has transitioned from state S_0 to state S_2 after one sampling period.

Figure 4.16 details, for a four state ring oscillator, the eight possible states and the value of each phase output, Φ_n. As the oscillator state increases, the phase outputs progress through a regular pattern and is analogous to *walking* a 1 through the states followed by *walking* a zero through the states. A transition

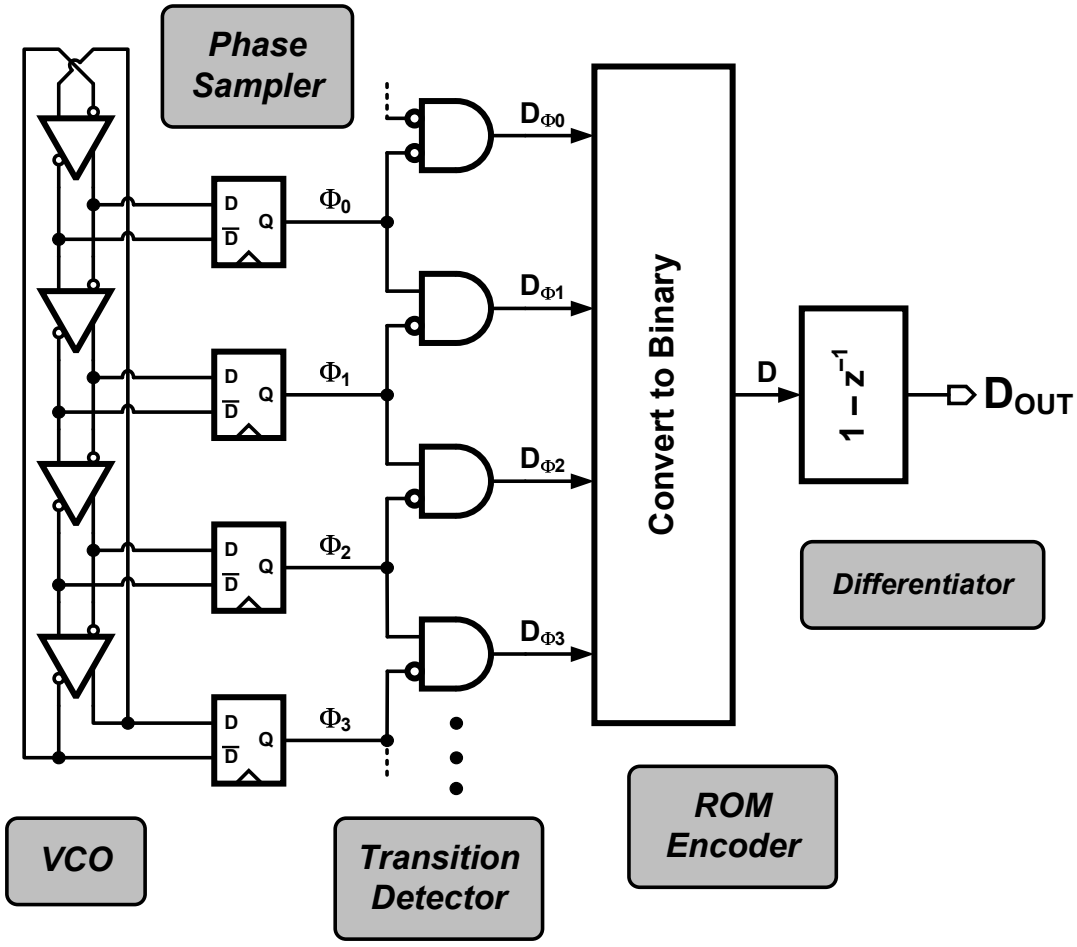


Figure 4.14: Block diagram of Switched Ring Oscillator.

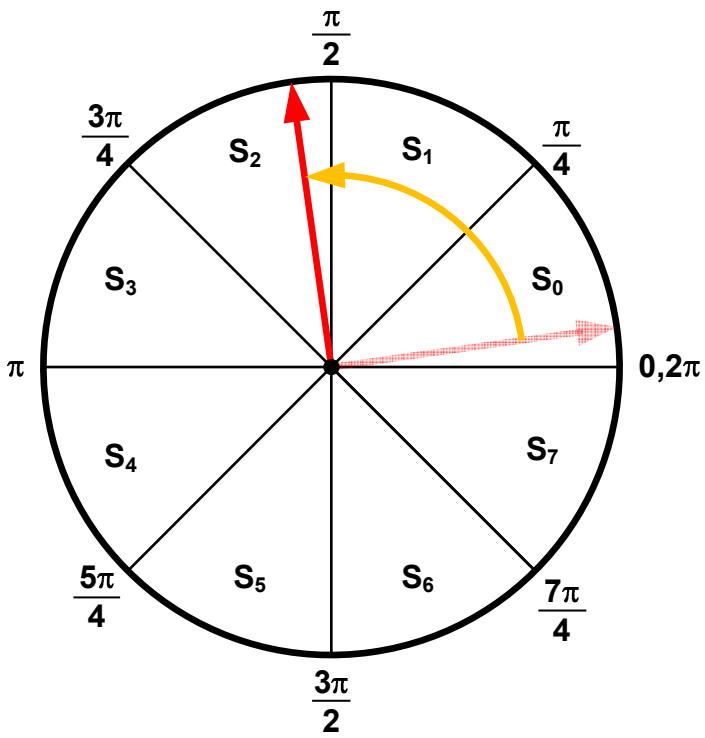


Figure 4.15: Phaser diagram showing quantized oscillator phase states of a four stage oscillator.

	Φ_0	Φ_1	Φ_2	Φ_3	D
S_0	0	0	0	0	0
S_1	1	0	0	0	1
S_2	1	1	0	0	2
S_3	1	1	1	0	3
S_4	1	1	1	1	4
S_5	0	1	1	1	5
S_6	0	0	1	1	6
S_7	0	0	0	1	7

	Φ_0	Φ_1	Φ_2	Φ_3	D
S_0	0	0	0	0	0
S_1	1	0	0	0	1
S_2	1	1	0	0	2
S_3	1	1	1	0	3
S_4	1	1	1	1	4
S_5	0	1	1	1	5
S_6	0	0	1	1	6
S_7	0	0	0	1	7

	Φ_0	Φ_1	Φ_2	Φ_3	D
S_0	0	0	0	0	0
S_1	1	0	0	0	1
S_2	1	1	0	0	2
S_3	1	1	1	0	3
S_4	1	1	1	1	4
S_5	0	1	1	1	5
S_6	0	0	1	1	6
S_7	0	0	0	1	7

	Φ_0	Φ_1	Φ_2	Φ_3	D
S_0	0	0	0	0	0
S_1	1	0	0	0	1
S_2	1	1	0	0	**2**
S_3	1	1	1	0	3
S_4	1	1	1	1	4
S_5	0	1	1	1	5
S_6	0	0	1	1	6
S_7	0	0	0	1	7

Figure 4.16: Tables illustrating oscillator phase output values and corresponding phase states.

detector circuit made from an AND gate is configured to identify in adjacent Φ_n phases the unique $0-1$ and $1-0$ boundaries. For the special cases of all Φ_n being zero or one, the first and last phases are properly gated together. Together with reduced phase quantizer metastability, only transition detector output state will be active at a time. A fast dynamic ROM encoder converts transition detector state information to a binary coded decimal. Finally, a combination of registers and two's complement adders realize the first order digital differentiation filter.

4.6 Summary

The area of VCO-based ADCs has seen tremendous growth in research interest in the last several years. Being a class of time-based signal processing circuits, the VCO-based ADC sees improved resolution as processes scale and become faster, while remaining insensitive to supply voltage scaling. Gain nonlinearity is the biggest challenge to widespread adoption of VCO-based ADCs in the commercial market. Several techniques have been introduced to mitigate nonlinearity, but more opportunities remain for nonlinearity suppression. Overall, VCO-based ADCs have a promising future in nanometer CMOS.

CHAPTER 5. MODELING OF A PLL-BASED DELTA-SIGMA MODULATOR

The name combination, PLL-Based Delta-Sigma Modulator, may seem perplexing at first. This level of confusion might be similar to that experienced by Western naturalists in Australia upon their first encounter with the platypus, an animal appearing to be the amalgamation of a beaver and a duck. Fortunately, this chapter alleviates confusion and discusses how the time-based signal processing techniques of phase-locked loops can be combined with the oversampling and noise-shaping characteristics of delta-sigma modulators to produce a high resolution, wide bandwidth ADC. A cursory examination of PLLs and delta-sigma ADCs reveals many similarities. Both use negative feedback and integrators to suppress large output noise sources — VCO phase noise in the PLL and quantization noise in the delta-sigma ADC. Just as delta-sigma techniques have been applied to PLLs in the form of fractional-N dividers, this work seeks to utilize PLL techniques and circuits to enhance delta-sigma modulator performance in nanometer scale CMOS.

This chapter focuses on creating a model for a new time-based ADC. First, a circuit architecture is developed and described. Specific implementation challenges are identified and architectural solutions are proposed. Finally, simulation results from a robust Matlab/SIMULINK model are presented to demonstrate the efficacy of the PLL-Based Delta-Sigma Modulator.

5.1 PLL-Based Delta-Sigma Modulator Architecture

Choosing a loop filter architecture of a PLL-Based delta-sigma modulator adds additional constraints not found in traditional delta-sigma modulators. VCO-based or more generally oscillator-based integrators form the bases of this delta-sigma architecture. They suffer from non-ideal effects such as an additional passive oscillator pole, phase detector nonlinearity, oscillator phase noise, and nonlinear oscillator gain. Much effort in previous research has been focused on reducing non-linear oscillator gain, primarily through the use of a high gain loop filter preceding the oscillator. A goal of this research is to demonstrate that oscillator-based integrators can replace traditional active-RC integrators at the loop filter front end where reliance on loop gain is not possible.

5.1.1 Discrete-Time Prototype

Classically, continuous-time modulators are first prototyped in discrete-time because of access to a vast knowledge base of publications and software tools. A common software program contains a set of Matlab functions and scripts for loop filter prototyping and generation of optimal loop coefficients for specified architectures [41]. Tradeoffs of important delta-sigma modulator parameters such as modulator order, oversampling ratio, out-of-band gain ($\|H_\infty\|$), and quantizer resolution can be investigated. After designing the optimized DT and determining the CT feedback DAC pulse shape, application of impulse invariance ensures the impulse response of the CT modulator matches that of the DT modulator [26].

Before determining the specifics of the loop filter architecture, a basic un-

derstanding of system performance must be gleaned. For the modulator to have greater than 74 dB SNDR (the noise term is inclusive of quantization and device noise), the SNQR should be greater than desired SNDR to insure a more power efficient, thermal noise limited design. Given a modulator with $NTF = (1-z^{-1})^L$, Equation (5.1) shows that SQNR may be increased through an increase in modulator order (L), oversampling ratio (OSR), or number of quantizer levels (M). Further reduction of in-band quantization noise may be obtained though optimized NTF zero placement. For reduced sensitivity to quantizer DC offset, at least one NTF zero should be placed at DC, and it is not recommended to optimize zeros for $L < 3$.

$$SQNR\ [dB] = 10\log_{10} M + 1.76 + (2L+1)\cdot 10\log_{10} OSR - 10\log_{10}\left(\frac{\pi^{2L}}{2L-1}\right) \quad (5.1)$$

Empirical simulation using Matlab shows that a third order modulator with an oversampling ratio of 16, sampling frequency of 1.28 GHz, and 16-level quantizer results 81.5 dB SQNR. The prototype discrete-time NTF is given by

$$NTF(z) = \frac{(1-z^{-1})(1-1.977z^{-1}+z^{-2})}{(1-0.4149z^{-1})(1-0.8707z^{-1}+0.3779z^{-2})}. \quad (5.2)$$

Figure 5.1 plots the prototype discrete-time NTF and cumulative summation of estimated quantization noise with nominal quantizer LSB step size $2V_{ref}/M = 150mV_{p-p}$.

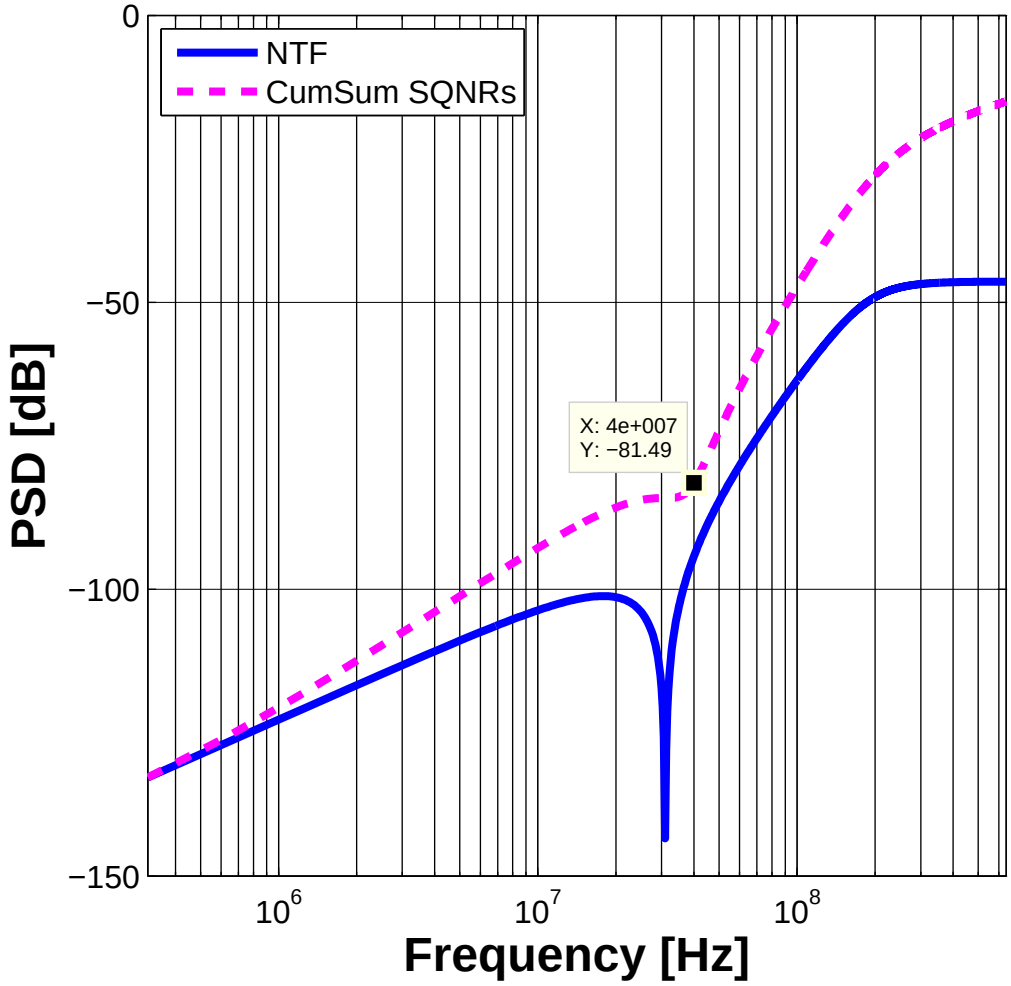


Figure 5.1: Power spectral density plot of noise transfer function and cumulative summation of estimated quantization noise versus frequency.

5.1.2 Modulator Loop Architecture

The next step after determining the prototype discrete-time is to choose a modulator loop architecture. Two common loop architectures for low-pass modulators are Cascade-of-integrators, feedback form (CIFB) and Cascade-of-integrators, feed-forward form [42]. When considering in the context of a single input tap and a continuous-time loop filter, the CIFB loop filter architecture exhibits L^{th} order anti-alias filtering of the input signal, where L is the modulator order [26]. This can be understood by noticing that in the continuous-time modulator, the sampler is preceded by L-integrators, whereas in the discrete-time modulator the sampling occurs at the modulator input. Its inherent anti-aliasing property can be used to suppress out-of-band blockers; however, this same single input tap CIFB loop architecture suffers from increased sensitivity to integrator nonlinearity. This is because all of the input signal must be directed through integrator nonlinearity. In addition, L feedback DACs are required to stabilize the loop. The CIFF architecture circumvents integrator induced nonlinearity by routing the input signal around the loop filter and directly to the quantizer input [43]. This architecture exhibits a unity signal transfer function and is stabilized with a single feedback DAC. Its primary drawback is the requirement of a summation circuit (passive or active) at the quantizer input. Typically, this leads to higher power consumption or loss of accuracy, and in the case of passive current summation, higher supply voltage for wide compliance range current steering DACs [8].

In the case of a oscillator-based delta-sigma modulator, strict implementation as either CIFB or CIFF leads to unacceptable distortion or high power consumption. The CIFB architecture would exacerbate oscillator-based integrator nonlinearity, and the inclusion of the CIFF architecture summation node would

impose strenuous requirements on charge pumps, current steering DACs, and amplifiers, depending on implementation. To alleviate these problems and find the best compromise, a partial feed-forward/feedback architecture is proposed and a block diagram is shown in Fig. 5.2. Gain coefficients are shown in Table 5.1.

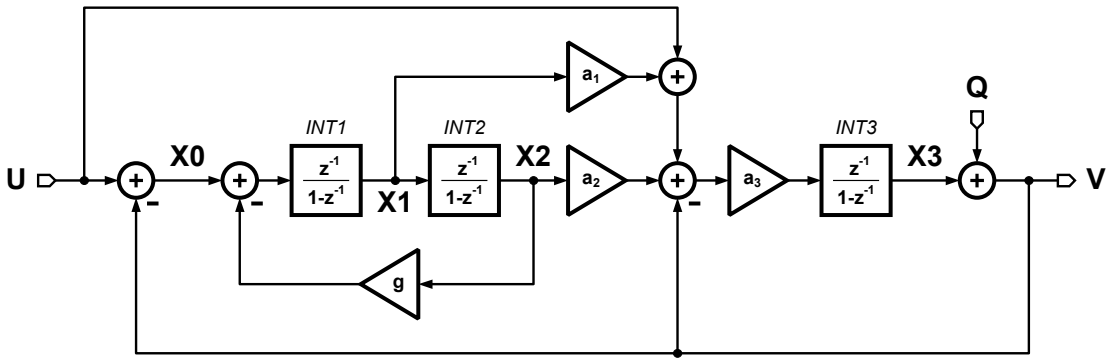


Figure 5.2: Discrete-time linear model of partial feed-forward/feedback delta-sigma modulator.

Table 5.1: Z-domain Gain Coefficients

Coefficient	Value
a_1	0.6678
a_2	0.1501
a_3	1.7144
g	0.0230

In this architecture, the input signal is directed to integrators $INT1$ and $INT3$, reducing the signal content in both $INT1$ and $INT2$. Note that $INT3$ must still process the full input signal. A resonator is formed around $INT1$ and $INT2$ to allow optimized NTF zero placement. Feedback DACs, $DAC1$ and $DAC2$, insure proper feedback stability. In this loop architecture, feed-forward summation is computed at the input of $INT3$ and signal content is minimized in $INT1$ and $INT2$. Distortion induced in $INT3$ is minimized by the preceding loop gain.

Figure 5.3 shows the input signal transfer function to each node versus input frequency without dynamic range scaling.

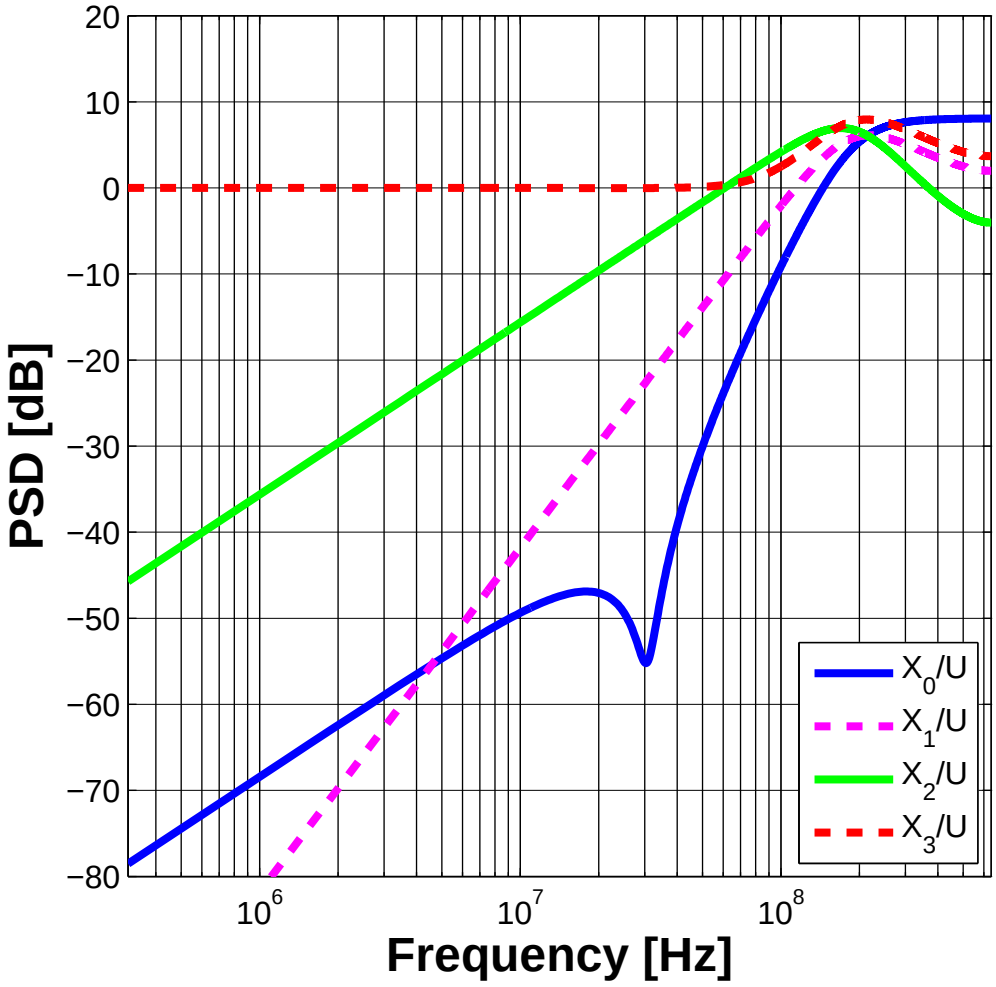


Figure 5.3: Magnitude of signal content in nodes X_0 through X_3 without dynamic range scaling in z-domain model.

Note, dynamic range scaling will be applied after conversion to the final time-domain modulator. Also note, as with any partial feed-forward/feedback architecture, the STF manifests out-of-band gain peaking (in this case $\sim 8dB$), which places a greater burden on the anti-alias filter to suppress out-of-band blockers near

the signal band edge.

5.1.3 Discrete-Time Prototype

For their continuous-time implementation, $DAC1$ and $DAC2$ feedback DACs are implemented with NRZ pulse shape. With application of the impulse invariance transformation, the prototype discrete-time NTF (5.2) is transformed to the continuous time domain NTF in software [41].

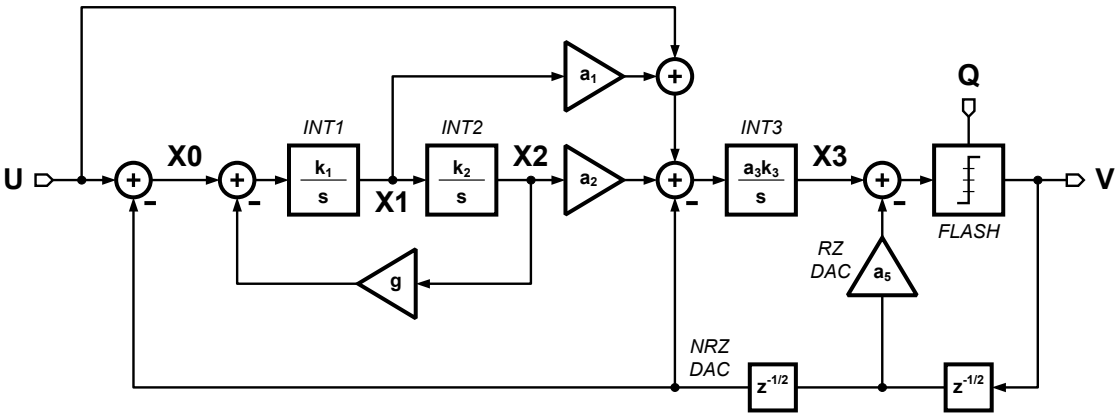


Figure 5.4: Continuous-time linear model of partial feed-forward/feedback delta-sigma modulator.

Figure 5.4 shows the continuous-time linear model. The resultant gain coefficients are tabulated in Table 5.2. An additional gain term, $a5$, feeds back to the quantizer input with a return-to-zero DAC and compensates for the one clock cycle loop delay of the two feedback DACs [44].

Each integrator is represented by the linear transfer function, k/s. In traditional continuous-time delta-sigma modulators, k/s is commonly realized as an amplifier-based active-RC integrator. The exactness of the integrator is dependant on amplifier gain and bandwidth. Modern nanometer-scale CMOS processes suffer

Table 5.2: S-domain Gain Coefficients

Coefficient	Value	Coefficient	Value
a_1	0.4973	k_1	F_s [rad]
a_2	0.1267	k_2	F_s [rad]
a_3	2.2572	k_3	F_s [rad]
g	0.0226	a_5	1.7144 [rad]

from both low supply voltages and low intrinsic transistor gain, $g_m r_o$, which limit signal power and amplifier gain. Oscillator-based integrators solve both issues with supply-voltage independent dynamic range and inherent infinite phase-domain DC gain; however, they are not void of difficulty.

5.2 Oscillator-Based Integrators

Oscillator-based integrators can be implemented as either high-Q LC tanks or low-Q ring oscillators. LC oscillators tradeoff excellent phase noise per milliwatt power for large inductor area and narrow tuning range, whereas ring oscillators occupy a small area and have wide tuning range but consume a large amount of power to have low phase noise. From the basis of power consumption and phase noise alone, the LC oscillator should be the clear choice leading to a high performance, low power design. However, the need for low phase noise must be balanced with wide tuning range.

5.2.1 Quality Factor

Quality factor, Q, is defined as the ratio of energy stored to the energy dissipated per cycle. For lossy LC oscillators, Q and bandwidth are parameters of the RLC network components and resonant frequency (5.3), (5.4), (5.5), respectively.

$$Q = \omega_o RC = \frac{R}{\sqrt{L/C}} = \frac{R}{\omega_o L} \tag{5.3}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{5.4}$$

$$\omega_b = \frac{1}{RC} \tag{5.5}$$

Integrated circuit implementations of LC oscillators can have Q values between 5 and 10. However, inductor sizes can be very large, and frequency tuning range is limited. In contrast, Equation (5.6) shows effective Q for a three stage ring oscillator [45].

$$Q_{eff} = \frac{9}{8}\sqrt{\frac{\pi |dv/dt|_{max}}{\omega_0 V_{dd}}} \tag{5.6}$$

Typical values of ring oscillator quality factor are on the order of 1. These low Q values result in higher phase noise and frequency selectivity is reduced. However, ring oscillators can be made very compact physically and have wide tune range. Both characteristics are desirable in oscillator-based data converters.

5.2.2 Oscillator Bandwidth

While ring oscillators are typically considered to be voltage controlled, they are more typically implemented as current-controlled oscillators with a transconductor input circuit. Figure 5.5 shows the circuit diagram of an inverter based current-controlled ring oscillator with PMOS V-to-I converter and equivalent VCO

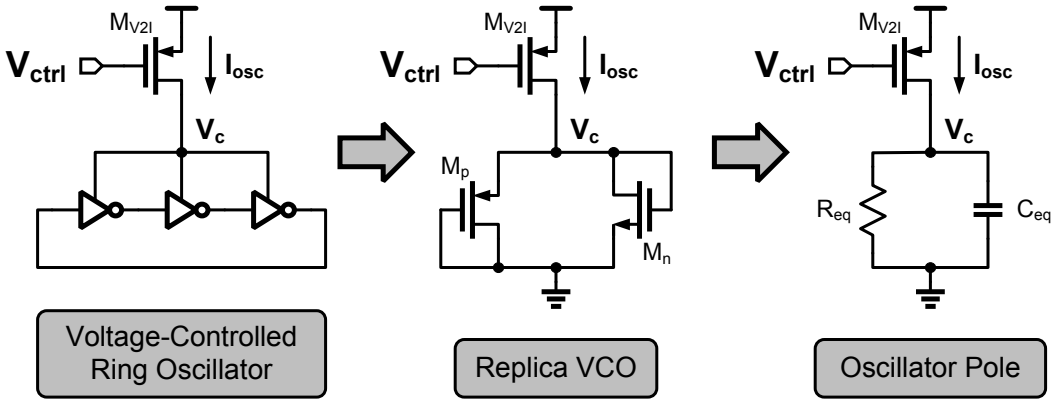


Figure 5.5: Voltage-controlled oscillator with PMOS V-to-I converter, equivalent replica VCO, and passive RC filter equivalent circuits.

replica model [46].

If node V_c of Fig. 5.5 is driven by an ideal DC voltage source with the assumption of Square Law compliant transistors, current drawn from the voltage source, I_{osc}, is given as

$$\begin{aligned} I_{D,x} &= \mu_x C_{ox} \frac{W_x}{L_x} (V_c - V_{TH,x})^2 \\ I_{osc} &= I_{D,p} + I_{D,n} \end{aligned} \tag{5.7}$$

Direct voltage control of inverter based ring oscillators results in a linear voltage-to-frequency transfer function. To this end, transistor M_{V2I} generates a quadratic drain current and supplies the quadratic current requirements of the current-controlled ring oscillator, resulting in a linear V-to-F characteristic.

An estimation of oscillator bandwidth, w_b, by considering the representative replica oscillator circuit of Fig. 5.5 as an equivalent resistance, R_{eq}, and capacitance, C_{eq}, leading to

$$w_b = 1/(R_{eq} C_{eq}) \ . \tag{5.8}$$

To a first order, R_{eq} can be estimated as V_c/I_{osc} with C_{eq} estimated as the gate

capacitance of M_p and M_n plus other metal routing capacitance internal to the oscillator.

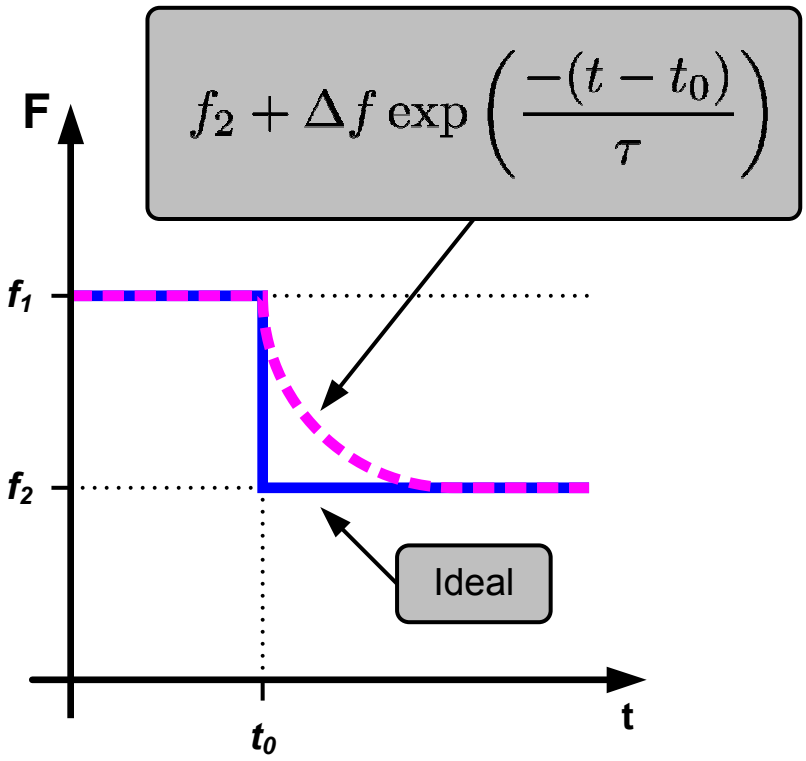


Figure 5.6: Oscillator frequency versus time for negative control voltage step.

To gain insight into (5.8), the voltage control step response of the circuit shown in Fig. 5.6 is investigated. It shows oscillator frequency as the VCO is subjected to a small control voltage step.

The ideal response is for the oscillator frequency to change instantaneously; however, oscillator bandwidth in real circuit implementations limits the rate of frequency change. For small input voltage steps, oscillator frequency versus time can be modeled as a first order pole with decaying exponential response given by

$$f_{osc} = f_2 + \Delta f \exp\left(\frac{-(t-t_0)}{\tau}\right) \tag{5.9}$$

where f_{osc} is the oscillator frequency, $\Delta f = f_1 - f_2$, and t_0 is the voltage step time

(intentionally coincident with an oscillator zero crossing).

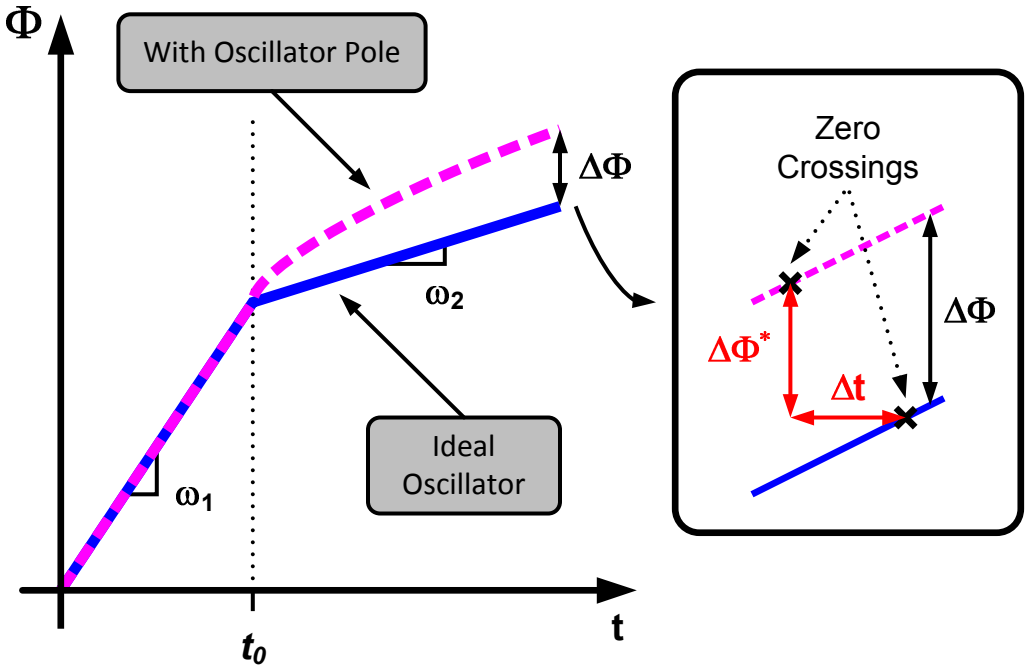


Figure 5.7: Oscillator phase versus time for negative control voltage step.

Figure 5.7 depicts the absolute phase response of an oscillator with control voltage step at t_0, which is the integral of (5.9). For time prior to t_0, both the ideal oscillator and non-ideal oscillator with first order pole accumulate phase at a constant rate, ω_1. At time t_0, a small negative voltage step is applied to the control voltage. The ideal oscillator reacts immediately and begins accumulating phase at a slower rate, ω_2. The non-ideal oscillator does not react as quickly, and its accumulated phase overshoots the ideal oscillator accumulated phase. After many time constants, the non-ideal oscillator's rate of phase accumulation decreases to the nominal w_2. At this point, some interesting observations can be made. The phase difference between the two oscillators far from t_0 will have a deterministic value, $\Delta\Phi$, proportional to the non-ideal oscillator pole time constant, τ. The

phase of each oscillator with $t_0 = 0$ is given by

$$\begin{aligned}
\omega(t) &= \omega_1 \cdot u(-t) + \{(\omega_1 - \omega_2)e^{-t/\tau} + \omega_2\} \cdot u(t) \\
\Phi(t) &= \int_0^t \omega(t)dt \\
\Phi(t) &= \{-(\omega_1 - \omega_2)\tau \cdot e^{-t/\tau}\Big|_0^t + \omega_2 t\} \\
\Phi(t) &= \{-(\omega_1 - \omega_2)\tau \cdot (e^{-t/\tau} - 1) + \omega_2 t\}, \qquad (5.10)
\end{aligned}$$

and the phase of the ideal and non-ideal oscillators (ω_{ideal} and $\omega_{non-ideal}$) and their difference ($\Delta\Phi$) are given by

$$\Phi_{ideal}(t) = \omega_2 t \qquad (5.11)$$

$$\Phi_{non-ideal}(t) = -(\omega_1 - \omega_2)\tau \cdot (e^{-t/\tau} - 1) + \omega_2 t \qquad (5.12)$$

$$\Delta\Phi(t) = -(\omega_1 - \omega_2)\tau \cdot (e^{-t/\tau} - 1). \qquad (5.13)$$

If $t \to \infty$, the exponential term dies away and the oscillator pole time constant is given by

$$\tau = \frac{\Delta\Phi}{\omega_1 - \omega_2} \qquad (5.14)$$

Now we can observe that it is difficult to inspect the phase of an inverter-based ring oscillator at an arbitrary time instant. Some insight can be gained through observation of multiple output phases, but higher phase measurement accuracy is required to evaluate (5.14). What can be observed accurately are edge crossings. Figure 5.7 shows zoomed plot of the oscillator phase far from t_0. Zero crossings are indicated for both the ideal and non-ideal oscillators, and they have an edge crossing time difference, Δt, and modified oscillator phase difference, $\Delta\Phi^*$. Accounting for the missing phase accumulation at constant rate, ω_2, for the duration of Δt, Equation (5.14) is modified for use with zero crossing information and is given by

$$\tau = \frac{\Delta\Phi^* + \omega_2\Delta t}{\omega_1 - \omega_2} = 1/\omega_b \qquad (5.15)$$

The linear phase-domain model of the voltage-controlled inverter-based ring oscillator shown in Fig. 5.5 is given by

$$H(s) = \frac{2\pi K_{vco}}{s} \cdot \frac{1}{s\tau + 1} \tag{5.16}$$

Simulation measurements show $w_b \approx f_{osc}$ yielding $Q = 1$ and confirming the assertions made in [45]. To decrease oscillator induced loop delay, f_{osc} should be maximized; however, this conflicts with phase noise minimization.

5.2.3 Phase Noise

Active-RC integrators are subjected to well-known resistor and op-amp noise. As its time-based equivalent, oscillator-based integrators are subjected to time domain noise or more commonly, phase noise. Oscillator phase noise, $\mathcal{L}(f)$ with units dBc/Hz, is defined as the random fluctuation in output phase due to upconverted device noise [47]. Phase noise is a single-sideband (SSB) power spectral density given mathematically by $\mathcal{L}(f) = \frac{1}{2}S_\phi(f)$, where $S_\phi(f)$ is the double-sideband phase noise spectrum.

Figure 5.8 shows three primary phase noise regions: 1. upconverted device flicker noise $\mathcal{L}(f) \propto 1/f^3$, 2. upconverted device thermal noise $\mathcal{L}(f) \propto 1/f^2$, and 3. wide-band Leeson noise $\mathcal{L}(f) \propto constant$. In [48], the relationship of oscillator frequency, f_{osc}, and power dissipation, P, for ring oscillators is approximated as

$$\mathcal{L}(f) \propto \left(\frac{f_{osc}}{f}\right)\frac{1}{P}. \tag{5.17}$$

For a given ring oscillator with fixed oscillation frequency (f_{osc}), doubling f_{osc} results in double power dissipation and 3 dB lower phase noise. In a second oscillator, when f_{osc} is doubled and power dissipation is held fixed, phase noise increases

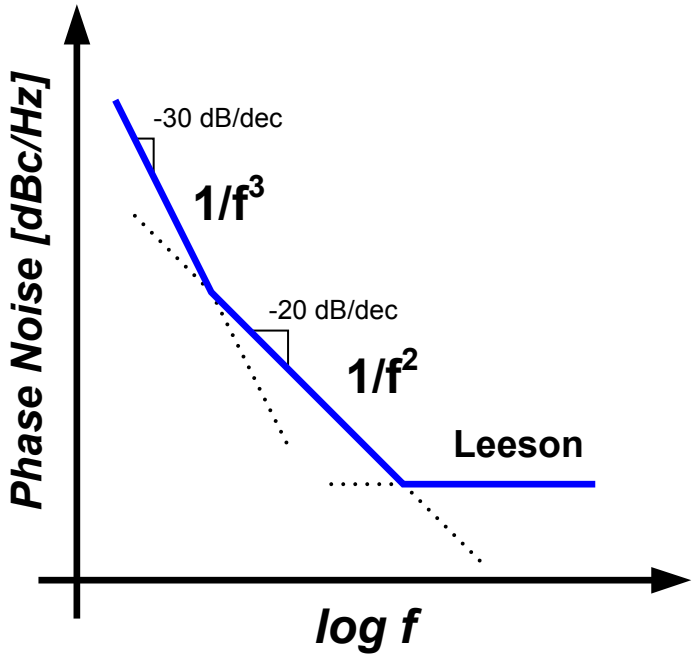


Figure 5.8: Plot of single sideband phase noise, $\mathcal{L}(f)$, versus log frequency.

by $6dB$. Doubling both oscillation frequency and power generates a net $3dB$ increased in phase noise. This result is in conflict with maximizing f_{osc} to maximize the oscillator pole frequency.

Modeling oscillator phase noise can be easily accomplished by passing phase noise through the inverse of the oscillator linear phase domain transfer function (5.16). The input referred voltage noise is given by

$$\overline{v_n^2} = 10^{\,\mathcal{L}(f_0)/10} \cdot \left(\frac{f_0}{K_{vco}}\right)^2 \cdot 2 \tag{5.18}$$

where f_0 is the spot frequency, K_{vco} has units Hz/V, and applied to the control voltage input using a zero-order hold function with period $1/f_{osc}$. For signal bandwidth much less than f_{osc}, the *sinc* frequency response of the zero-order hold function will have negligible impact on signal band edge noise.

With a voltage mode, input referred phase noise given by (5.18), a model of

flicker noise with a -10 dB/dec slope can be generated according to [49, 50]. In this approach, an alternating cascade of left half plane pole/zero pairs approximates a 1/f characteristic. Each successive pole or zero is placed an octave higher in frequency than its predecessor with the last element being a zero. Note that the flicker noise corner frequency is +2.5 dB higher than the thermal noise floor.

5.2.4 Oscillator Nonlinearity

Linear frequency, supply voltage-controlled ring oscillator circuits are impractical to implement due to the need for a low power, low impedance, high dynamic range voltage buffer circuit. In the search for an alternative, first the VCO with PMOS V-to-I converter, shown in Fig. 5.5, is considered because of its linear V_{ctrl} to f_{osc} characteristic. A simplified analysis models the periodic steady state ring oscillator as a replica VCO load, which is a parallel combination of PMOS and NMOS diode connected transistors [46].

All transistors in the replica VCO shown in Fig. 5.5 are assumed to operating in saturation with Square Law drain current characteristics. The drain current, I_{osc}, is proportional to V_{ctrl}^2 leading to $f_{osc} = \sqrt{I_{osc}}$. Difficulty arises in attempting to generate a current with square root characteristics; however, if two current controlled oscillators operating with a small-signal linear differential input current are considered, then some interesting properties develop.

Figure 5.9 shows the circuit diagram for a pseudo differential linear current-controlled oscillator. It consists of two ring oscillators, $OSCP$ and $OSCN$, driven by current sources, I_p and I_n. Each current source is summation of standby current, I_0, and a small input signal current, ΔI. The current to f_{soc} relationship of a single current-controlled ring oscillator can be extended to the pseudo-differential case

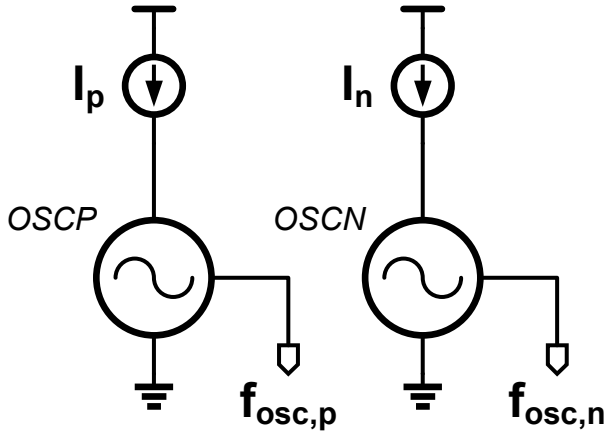


Figure 5.9: Block diagram of pseudo differential current controlled ring oscillator.

where $\Delta f_{osc} = f_{osc,p} - f_{osc,n} = \sqrt{I_p} - \sqrt{I_n}$. Use of binomial expansion results in following theorem.

$$\begin{aligned} \Delta f_{osc} &= \sqrt{I_p} - \sqrt{I_n} \\ &= I_0 \cdot \left\{ \left(1 + \frac{\Delta I/2}{I_0}\right)^{\frac{1}{2}} - \left(1 - \frac{\Delta I/2}{I_0}\right)^{\frac{1}{2}} \right\} \end{aligned} \tag{5.19}$$

Expanding the square root terms of (5.20) with binomial theorem under the approximation that $|\Delta I/I_0|$ yields

$$\left(1 + \frac{\Delta I/2}{I_0}\right)^{\frac{1}{2}} = 1 + \frac{1}{2}\left(\frac{\Delta I/2}{I_0}\right) + \frac{1}{2}\left(\frac{1}{2} - 1\right)\left(\frac{\Delta I/2}{I_0}\right)^2 \frac{1}{2!} + \ldots \tag{5.20}$$

$$\left(1 - \frac{\Delta I/2}{I_0}\right)^{\frac{1}{2}} = 1 + \frac{1}{2}\left(-\frac{\Delta I/2}{I_0}\right) + \frac{1}{2}\left(\frac{1}{2} - 1\right)\left(-\frac{\Delta I/2}{I_0}\right)^2 \frac{1}{2!} + \ldots \tag{5.21}$$

With the assumption that $(\Delta I/2)/I_0$ is small, high order terms can be ignored. Equations (5.21) and (5.22) are substituted into (5.20) to produce

$$\Delta f_{osc} = \Delta I \tag{5.22}$$

This interesting result affirms that a small linear differential current applied to two current-controlled ring oscillators gives rise to a linear frequency difference. Linear differential input/output transconductor circuits may be used to translate differential voltage inputs while rejecting common-mode perturbations. Another option is to use pulse width modulated, two-level current inputs [23, 34]. Current pulses of magnitude, $\Delta I/2$ and $-\Delta I/2$, and duty cycle, D, are periodically switched between two oscillators, producing a frequency difference of Δf_{osc} for $D \cdot T$, and $-\Delta f_{osc}$ for $(1 - D) \cdot T$.

5.3 Phase Detector and Charge Pump

In phase-locked loop circuits, input reference and fed back VCO phase signals must be interfaced with an analog loop filter. This is routinely handled by a phase difference detector (i.e. phase detector) and phase-to-current converter (i.e. charge pump).

5.3.1 Three-State Phase Frequency Detector

The three-state phase/frequency detector (PFD) architecture is among the most common linear phase detector architectures. Its name portends the underlying architecture depicted in Fig. 5.10, which is comprised of two positive edge triggered flip-flops and a NAND logic gate. Each flip-flop data input is set to constant logic-1. From state RST, a positive edge on R will cause the state machine to enter state U and generate a corresponding U signal. A subsequent positive edge on V will momentarily activate D, and the NAND combination of U and D

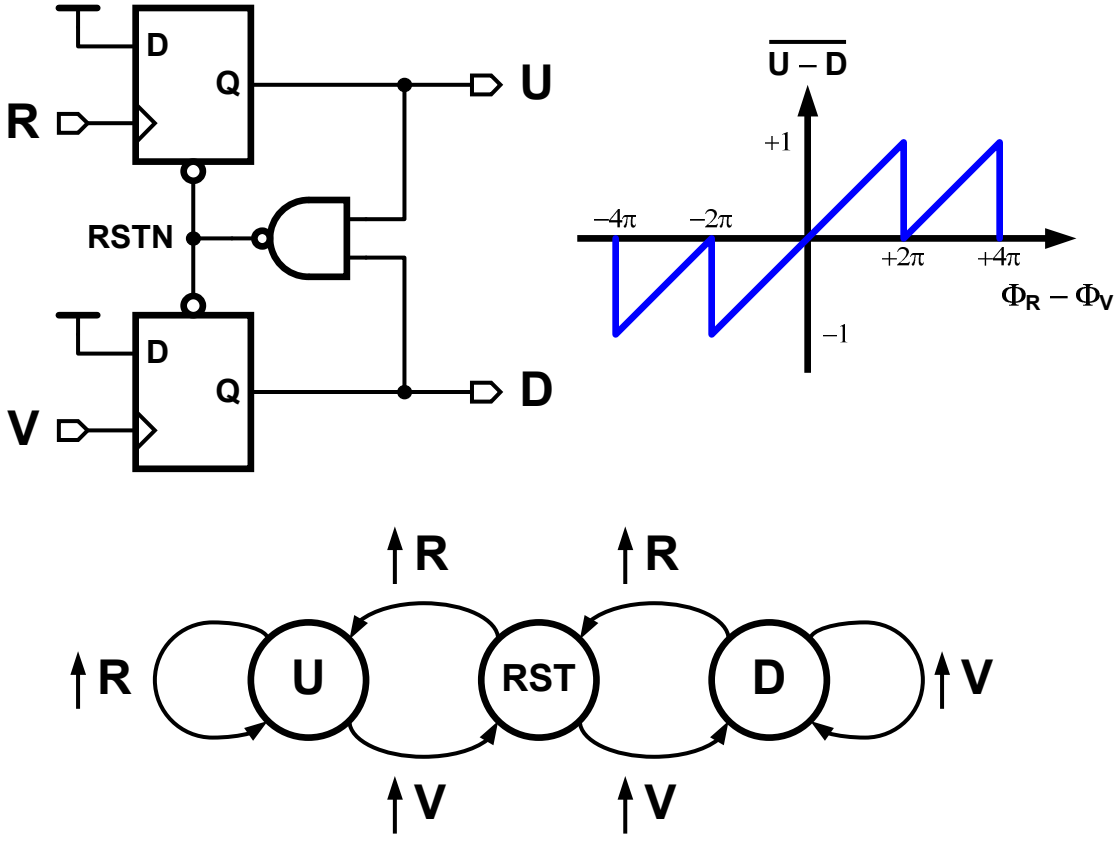


Figure 5.10: Three state phase/frequency detector block diagram, transfer function, and state diagram.

reset both flip-flops to their default RST state. Correspondingly, if a V positive edge occurs first while in state RST, the state machine will enter state D and will reset to state RST after an R positive edge. Dead zone behavior can be mitigated by delaying the NAND reset signal to have finite U and D signal overlap, which allows charge pump switches enough time to turn on before both are turned off. Positive phase difference between R and V greater than 2π will consistently produce positive average output signals, with the converse also being true. This aperiodicity allows the three-state PFD to detect frequency as well.

While the three-state PFD theoretically has a linear operating region of $-2\pi \leq \Phi_R - \Phi_V \leq +2\pi$, there are some circuit effects that reduce its performance. The first results from delay in the NAND reset path designed to eliminate dead zone in charge pump switches. This delay reduces the linear range to $-2\pi(1 - t_d/T) \leq \Phi_R - \Phi_V \leq +2\pi(1 - t_d/T)$. As process nodes scale, switch rise/fall times decrease. Proportional scaling of clock period, T, maintain constant dynamic range. The second effect is much more menacing and involves the internal construction of all memory storage elements used to store PFD state information.

At the highest level, flip-flops are considered purely digital circuits storing only ones and zeros. The reality is that transistor-level circuit architecture and sizing contribute to finite setup and hold time, and clock-to-Q delay. The flip-flop in the three-state PFD operates as a one-shot with reset. This reset action is often slow and incomplete, leading to the internal nodes retain time dependent memory of its previous state. Additionally, input phase difference around $\pm\pi$ cause additional nonlinearity due to opposing edge transitions of R and V. Certain architectures, such as the true single phase and pass transistor architecture, are more susceptible than others to these variations.

In typical integer-N PLL applications of even modest jitter performance,

cycle-to-cycle variations of phase detector inputs are small and lead to reduced signal dependent variations. In contrast, oscillator-based ADCs which employ phase detectors and fractional-N PLLs can have widely varying phase detector inputs, and they are predisposed to this time dependent memory. The nonlinearity problems of three-state PFDs preclude their use in high linearity systems.

5.3.2 Exclusive-OR Phase Detector

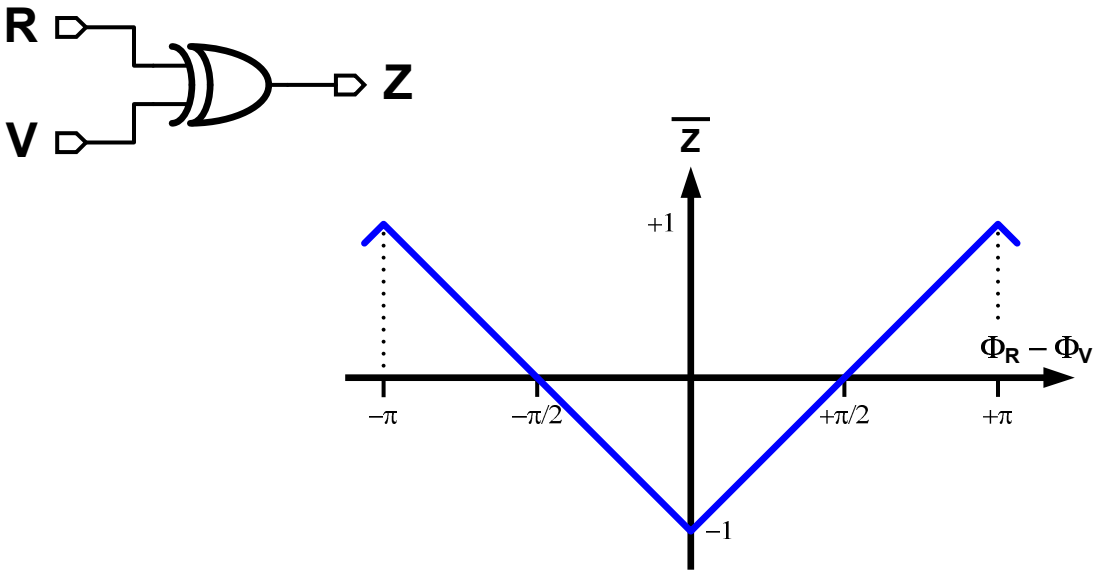


Figure 5.11: Exclusive-OR phase detector block diagram and transfer function.

A simpler, less problematic phase detector is the XOR logic gate. Figure 5.11 shows the transfer characteristic of the XOR phase detector. It has a symmetric transfer characteristic that is periodic with 2π with twice the gain and half the dynamic range of the three-state PFD. The linear range is from $0 \leq \Phi_R - \Phi_V \leq \pi$ where gain is positive, but changes sign between $\pi \leq \Phi_R - \Phi_V \leq 2\pi$. Fortunately in this application, the phase detector is not required to perform frequency detec-

tion, and modulator negative feedback maintains phase detector operation in its positive gain region. The XOR phase detector has neither state memory nor reset dependent operation, and has none of the associated problems.

5.3.3 Charge Pump Linearity

The phase-to-current conversion operation performed by the charge pump (CP) circuit is the final step to interface the VCO's time-based integration with an analog loop filter. Ideally, the charge pump should convert the phase detector's variable pulse width information to current pulses with zero rise/fall time. While this is an unrealistic goal, practical circuit implementations can achieve rise/fall times of about 10 ps in 65nm CMOS.

Figure 5.12 plots both the XOR phase detector plus charge pump output timing diagram versus time, and XOR phase detector plus charge pump transfer characteristic versus input phase difference. In the region away from 0 and π, the transfer characteristic is linear due to time integration of a trapezoidal CP current pulses being equal to that of a square CP current pulse. In the input phase difference regions between $0 \leq \Phi_R - \Phi_V \leq \pi(t_r + t_f)/T$ and $\pi(1 - t_r - t_f)/T \leq \Phi_R - \Phi_V \leq \pi$, charge pump current pulses become triangular and are no longer linearly dependent on input phase difference. Careful dynamic range scaling of oscillator-based integrator gain can limit signal excursions into these nonlinear regions and maximize composite oscillator-based integrator linearity.

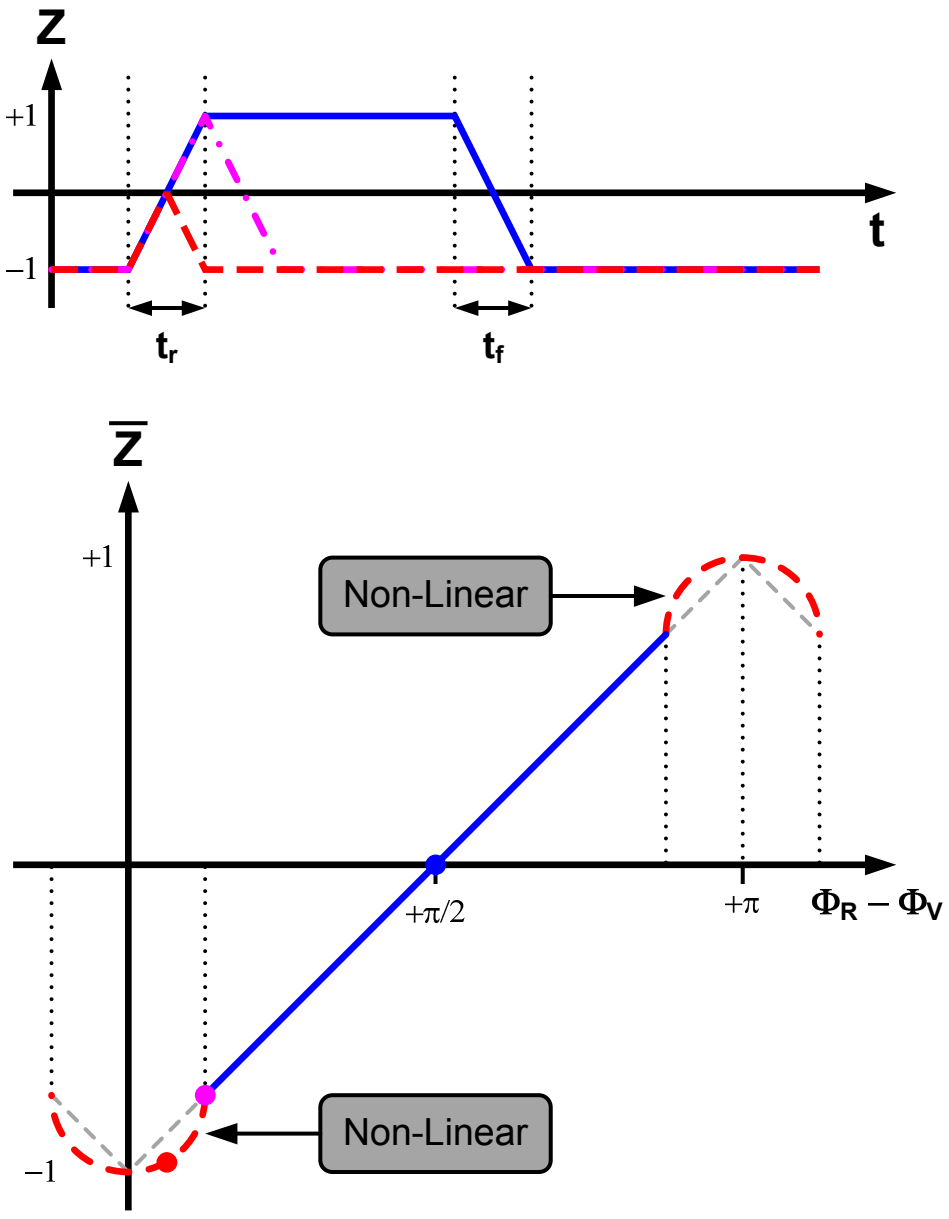


Figure 5.12: Exclusive-OR phase detector and charge pump with finite rise/fall time induced non linearity.

5.4 Feedback DAC

The oversampling and noise-shaping benefits of delta-sigma modulation that can easily suppress quantization noise do little in themselves to reduce errors in the primary feedback. Examination of Fig. 5.13 errors such as inter-symbol interference, jitter, device mismatch and noise see the same transfer function (5.23) to the output as the signal transfer function (STF). In other words, errors in the primary feedback DAC are not suppressed by the loop filter gain within the signal band.

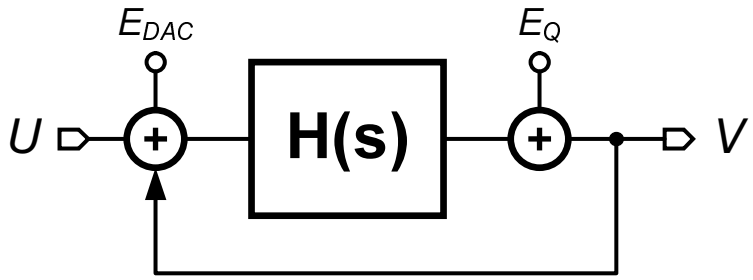


Figure 5.13: Linear model of continuous-time delta-sigma modulator with DAC and quantization noise.

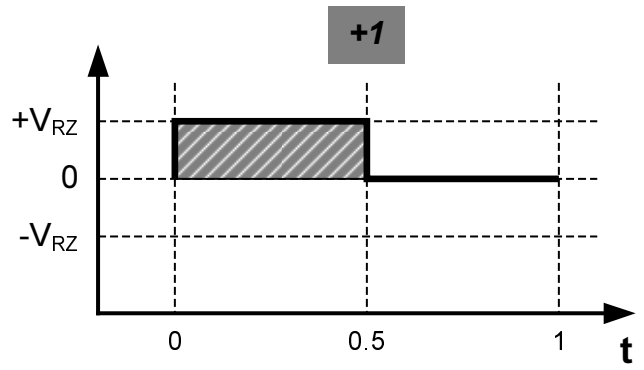
$$STF = \frac{V}{U} = \frac{V}{-E_{DAC}} = \frac{H(s)}{1 + H(s)} \tag{5.23}$$

This can have catastrophic effects on the modulator output, as the quality of the feedback DAC dictates overall modulator performance. Effects such as inter-symbol interference (ISI), device mismatch, device noise, and clock jitter, must be thoughtfully considered and care is taken to reduce their effects through architecture and circuit design techniques.

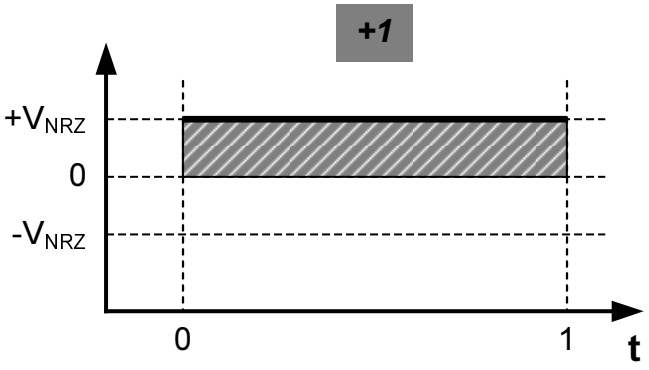
Choice of the feedback DAC architecture for a continuous-time delta-sigma modulator essentially has been relegated to the ubiquitous non-return-to-zero.

Why is this the case? To understand this, two common feedback DAC architectures are studied: return-to-zero, and non-return-to-zero.

In continuous-time delta-sigma modulators, negative feedback is often created with a rectangular pulse shape DAC commonly implemented with current steering circuits [26, 51]. The pulse interval diagram for both return-to-zero (RZ) and non-return-to-zero NRZ are shown in Figures 5.14(a) and 5.14(b), respectively. Each pulse shape is defined by parameters (α,β), which correspond the the normalized pulse start/stop times, respectively. The RZ and NRZ pulse shapes are the most common forms.



(a) Return-to-zero (0,0.5).



(b) Non-return-to-zero (0,1).

Figure 5.14: DAC pulse diagram with interval (α,β).

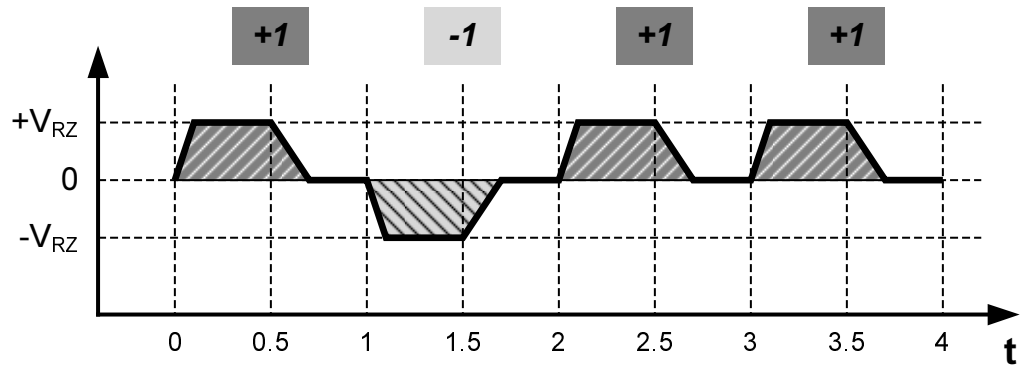
The advantages and disadvantages of the RZ and NRZ pulse shapes complement one other. An RZ pulse exhibits superior inter-symbol interference (ISI) immunity, but suffers from increased clock jitter sensitivity. Conversely, an NRZ pulse exhibits poor inter-symbol interference immunity, but is less sensitive to clock jitter.

5.4.1 Inter-Symbol Interference

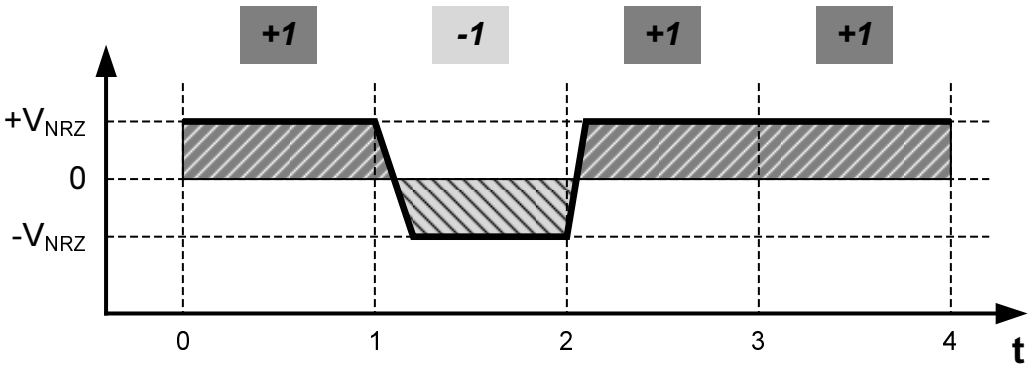
The aptly named inter-symbol interference is a phenomena associated with sampled data converter circuits, including clock and data recovery (CDR) circuits [52]. ISI causes the present data sample output to be a function of its prior, current, and following inputs. An ideal DAC which can produce perfectly rectangular pulses will have zero ISI. Figure 5.15 shows an illustrative example of practical 1-bit RZ and NRZ pulse shapes with finite rise and fall times. Note that these rise/fall times may not be matched.

In Figure 5.15, the DAC input impulse sequence is $[+1, -1, +1, +1]$. Integrating the RZ waveform over each sample period results in quantity that is independent of the previous or next sample period value. However, when the NRZ integrated over each sample period, the resultant quantity is highly dependent on its nearest neighbors. If both rise and fall times are matched, the integration magnitude of the sample period beginning with a $+1 \rightarrow -1$ transition will be the same a $-1 \rightarrow +1$ transition. Note this does not remain true when consecutive sample period values are identical, (i.e., $+1 \rightarrow +1$ or $-1 \rightarrow -1$).

While rise/fall asymmetry can be reduced with differential circuit topologies, it cannot be completely eliminated. This nonlinearity will lead to in-band noise folding of high frequency quantization noise [53]. Fast switching speeds of modern



(a) RZ pulse train.



(b) NRZ pulse response.

Figure 5.15: DAC pulse train with finite, unmatched rise/fall times.

nanometer-scale CMOS process help reduce this effect.

5.4.2 Clock Jitter

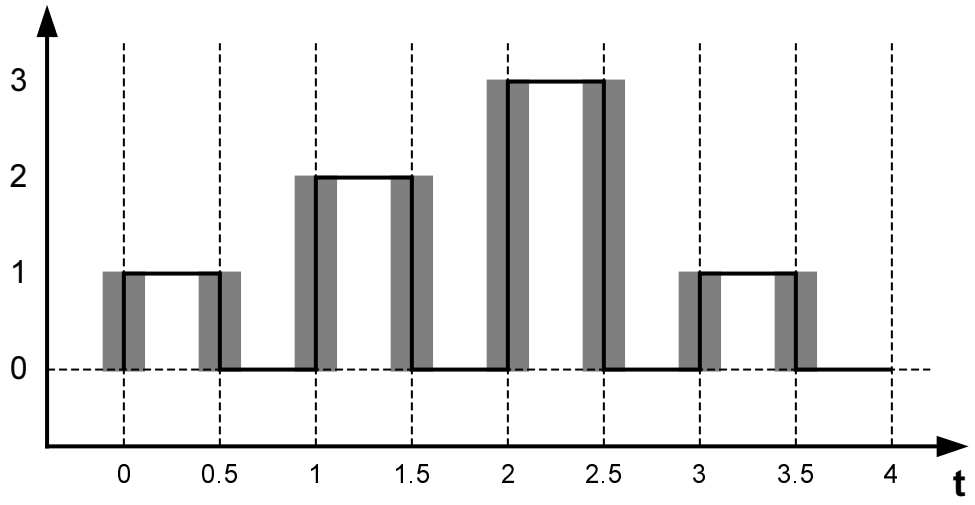
Market pressure to increase signal bandwidth juxtaposed with minimum OSR reduction has necessitated increase in sampling clock frequencies. This places a heavy burden on the clock generator to meet ADC timing requirements. Prior art has documented the detrimental effects of clock jitter [26, 44, 54]. Figure 5.16 shows the DAC pulse edge uncertainty for both an RZ and NRZ pulse shape. An intuitive inspection of both waveforms shows that because the RZ pulse shape has more transitions, it is also more sensitive to clock jitter. It is also interesting to note the NRZ pulse is sensitive to jitter only when the DAC code changes.

For a current DAC with NRZ pulse shape in the presence of white clock jitter, the estimated SNR is given by (5.24), where σ_{jitter} is the RMS long term jitter, OSR is the oversampling ratio, $\sigma^2_{I_{DAC,NRZ}}$ is the variance of the DAC code, $\sigma^2_{\Delta I_{DAC,NRZ}}$ is the variance of the first order difference of the DAC code, $\Delta I_{DAC,NRZ}$ [38].

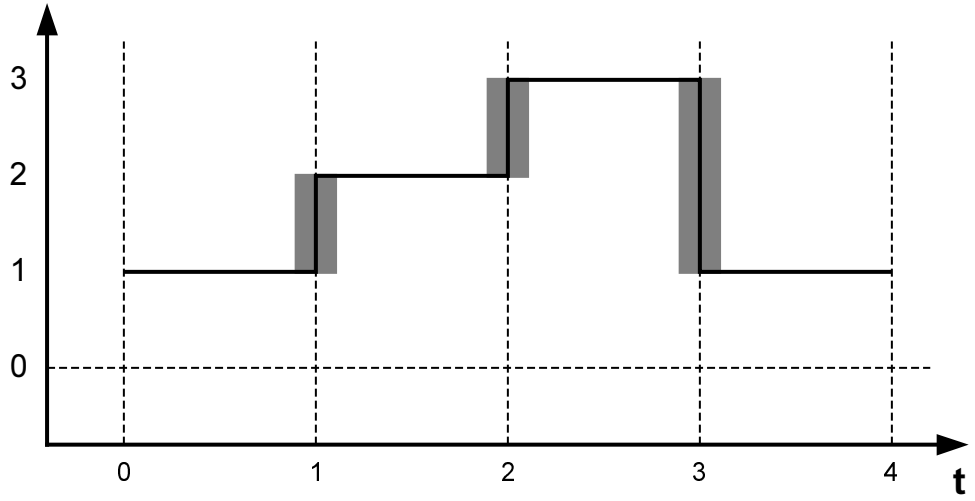
$$SNR_{jitter}\left(\sigma_{jitter}\right) = 10\log\left(OSR \cdot \frac{\sigma^2_{I_{DAC,NRZ}}}{\sigma^2_{\Delta I_{DAC,NRZ}}} \cdot \frac{T_s^2}{\sigma^2_{jitter}}\right) \tag{5.24}$$

5.4.3 Mismatch

Leaving the two-level DAC in the quest for higher resolution and more linear loop dynamics, delta-sigma modulators have been employing multi-bit feedback [55]. While a two-level DAC is inherently linear regardless of the end point values, multi-level DAC linearity is degraded by systematic and random mismatch errors



(a) RZ jitter response.



(b) NRZ jitter response.

Figure 5.16: DAC jitter response for RZ and NRZ pulse shapes.

between bit cells. Figure 5.17 shows an NMOS cascode current steering DAC cell. Low frequency mismatch is dominated by transistor M_{CS}. Transistor V_{th} matching is given by (5.25).

$$\Delta V_{th} = \frac{A_{VTH}}{\sqrt{WL}} \tag{5.25}$$

Systematic mismatch can be reduced primarily through careful layout techniques that consider well proximity effect, physical orientation, current flow, metallization, etc. The impact of random mismatch can be decreased by increasing device area according to (5.25) and increasing the small signal saturation voltage, v_{dsat}. Care should be taken with nanometer scale processes less than 130nm, as gate tunneling currents have become significant, which can alter dynamic logic and current mirror bias circuits [56].

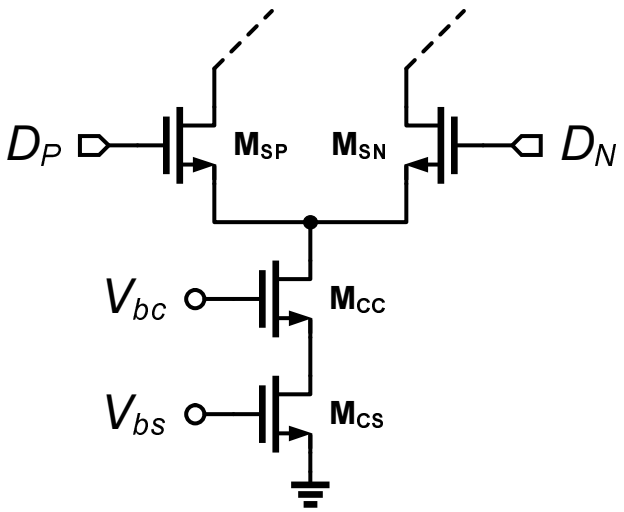


Figure 5.17: A NMOS current steering DAC cell.

5.4.4 Noise

A current steering DAC bit cell with additive noise sources is shown in Fig. 5.18. Current is steered through switch, M_{Sp}, for analysis purposes. At low fre-

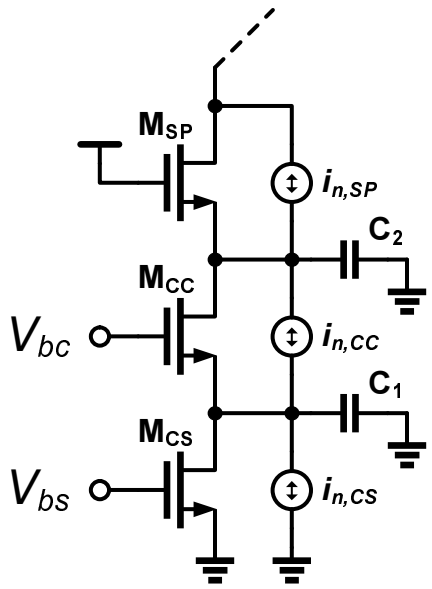


Figure 5.18: The simplified AC noise model for an NMOS current steering DAC cell.

quency, current noise from M_{CS} dominates. At moderate frequency, which could be within the signal bandwidth, parasitic capacitor C_1 forms a low impedance connection to ground, bypassing $i_{n,CS}$ and making $i_{n,CC}$ a significant source of noise. At very high frequencies, parasitic capacitance, C_2, shorts to ground allowing switch, M_Sp to dominate the output current noise. In an oversampled system, M_Sp noise is out of band; however, the pole formed with C_1 can reside within or near the signal band edge leading to significant noise contribution. Care should be taken when designing the cascode bias network for transistor M_{CC}.

5.5 Excess Loop Delay Compensation

Traditionally, quantizer delay and feedback DAC delay have dominated excess loop delay, but with the movement toward high sampling rate modulators, the effect of finite op-amp bandwidth also must be carefully considered. Many techniques have been published that can be used to compensate excess loop delay (ELD) [57]. Additionally, a nonlinear search algorithm and root mean square fit of the continuous time impulse response to the discrete time impulse response can optimize loop coefficients and accurately compensate for ELD [58].

One such method is shown in Fig. 5.19, where excess loop delay is compensated by adding a fast gain, negative feedback path from the quantizer output to its input [59].

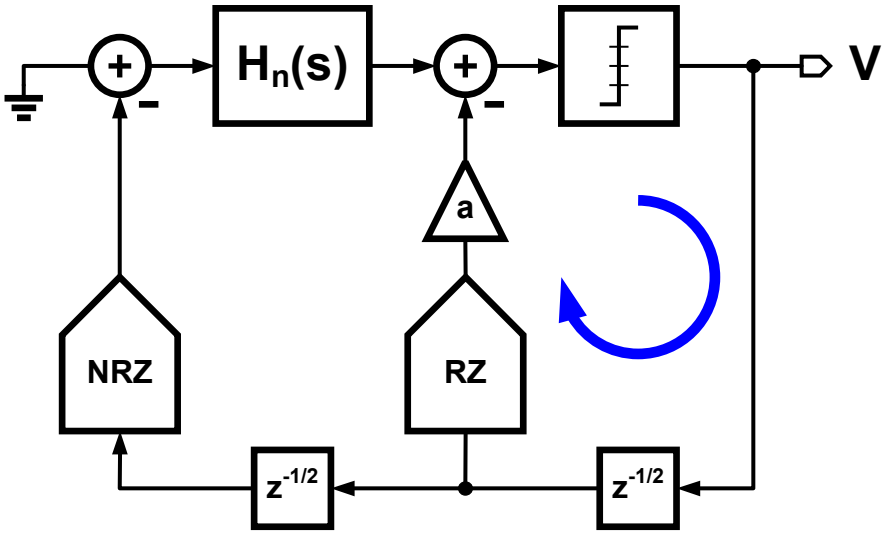


Figure 5.19: A block diagram of excess feedback delay compensation using a fast feedback path around the quantizer.

This seeks to make the continuous time impulse response observed at the quantizer input match that of the discrete time prototype at every sampling instant. In other words, if the open loop impulse responses of both the DT and

CT loop filters match at quantizer sampling instances, then the result is impulse invariant. Compensation DAC gain, a, is equal to the impulse response value after one clock period for the zero excess loop delay system, and can be calculated by hand [26] or using software tools [41]. A fast feedback path around the quantizer requires a wide compliance range current DAC as to not severely limit quantizer input range or high gain bandwidth summing amplifier with associated power increase. The DAC is commonly implemented as a half delay return-to-zero current steering DAC.

In another common method shown in Fig. 5.20, the quantizer output is differentiated and fed back to the last integrator input [60, 37]. This obviates the need for a summing amplifier or wide compliance range DAC, as summation is performed in current at a virtual ground. This differentiated quantizer signal is reintegrated by the last integrator to produce the correct compensation of the quantizer input Low frequency systems may employ explicit digital differentiation of the quantizer output, but the additional delay penalty inhibits application in high frequency modulators.

Figure 5.20 diagrams the process of differentiation using non-return-to-zero DACs separated by a half clock cycle delay [60]. The timing diagram of current mode differentiation using NRZ DACs is show in Fig. 5.21 with transfer function $a'(z^{-1/2} - z^{-1})$. Providing the fast feedback path through the last integrator modifies the gain coefficient to be $a' = a/k_n$. Additionally, it can be seen in Fig. 5.20 that DACs NRZ_2 and NRZ_4 have the same input delay time, and can be merged into one DAC with gain $1 - a'$ to save power and reduce noise. It should be noted that the bandwidth of the op-amp (or second pole of the integrator) should be high enough to not introduce added delay to the fast feedback loop.

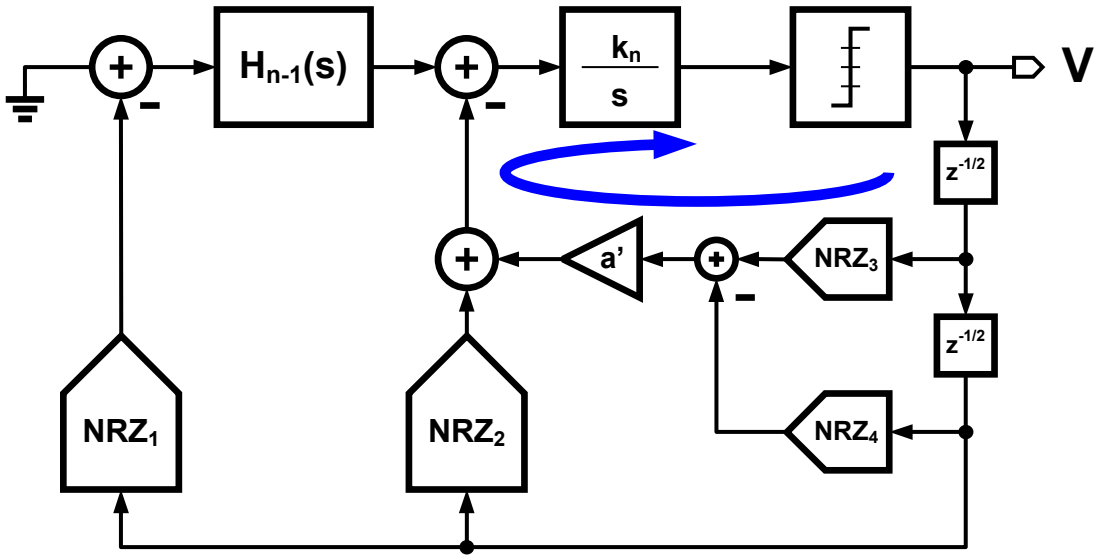


Figure 5.20: A block diagram of excess feedback delay compensation using a differentiated fast feedback path around the last integrator and quantizer.

5.5.1 The Not So Virtual, Virtual Ground

Implementing $INT1$ of Fig. 5.4 as a voltage-controlled oscillator-based integrator introduces some unique challenges in loop stability. Traditional active-RC integrators benefit from a virtual ground summation with looking in impedance $Z_{in} \approx 1/(sC \cdot A(s))$. The impact of stray capacitance on the virtual ground node due to DAC output, op-amp input, or metal routing capacitance is mitigated by high op-amp gain and bandwidth.

When an active-RC integrator is replaced by a voltage-controlled oscillator-based integrator, the assumption of a virtual ground for current summation is made void. As depicted in Fig. 5.22, the looking in impedance of the VCO integrator is nearly infinite. A pole is formed by input resistor, R, and the sum of stray capacitors, C_p, on node PVG. With additional capacitor, C_{LPF}, the impedance

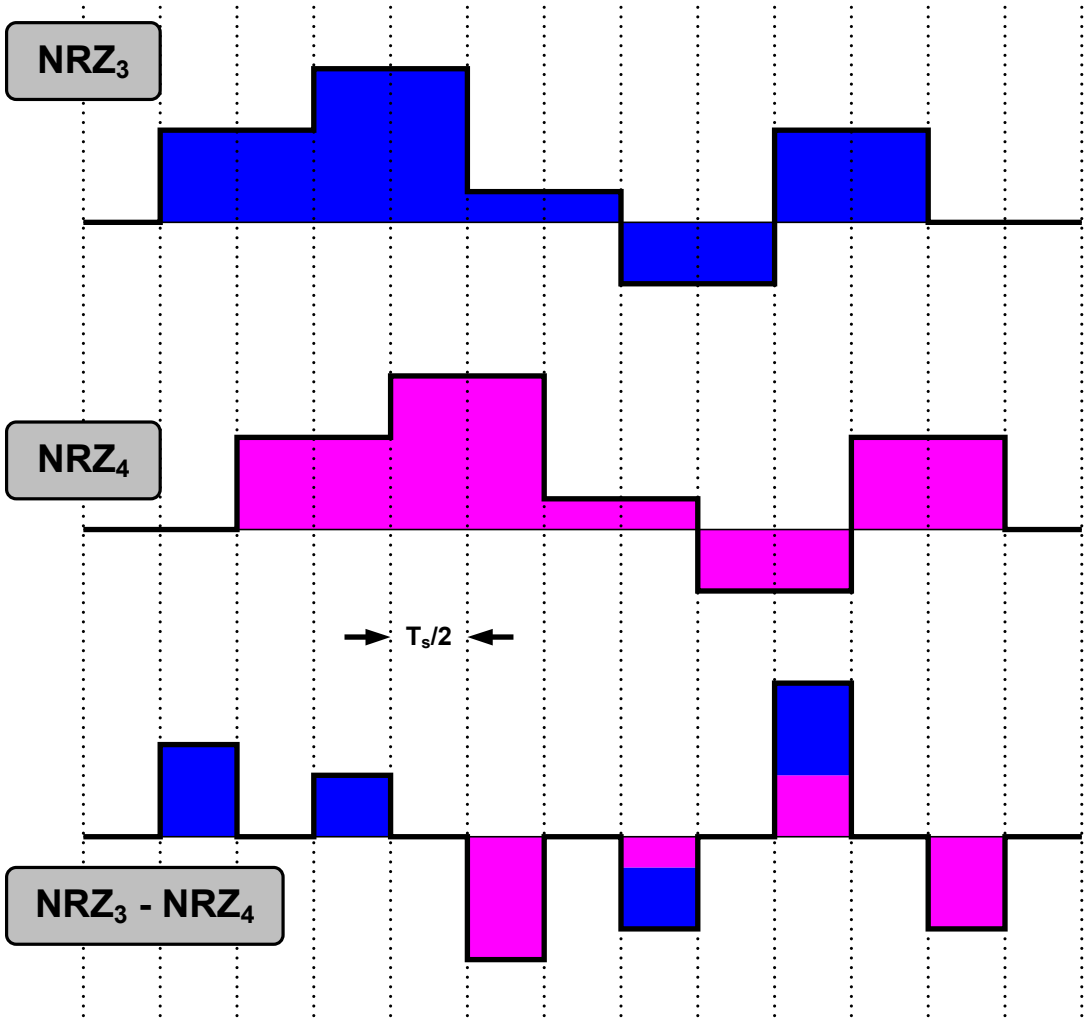


Figure 5.21: Timing diagram showing the formation of differentiated RZ pulse for excess loop delay compensation.

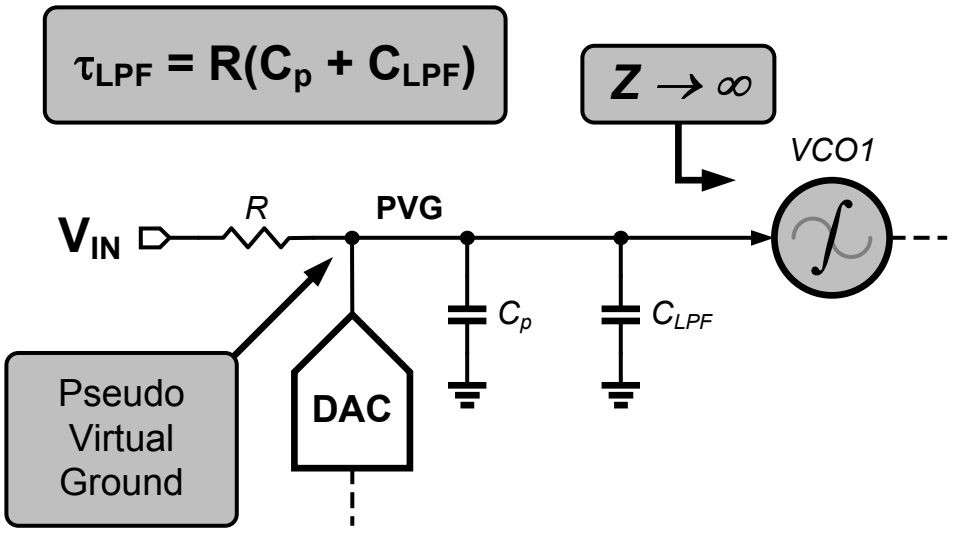


Figure 5.22: A schematic drawing illustrating the absence of a true virtual ground with VCO based integrators.

of PVG can be lowered causing the formation of a weak virtual ground, or *pseudo virtual ground*. Intentionally lowering the pole frequency to 2.5 times the signal bandwidth can also suppress DAC current pulse induced pseudo virtual ground ripple without increasing in-band input referred noise. However, this additional pole degrades loop gain phase margin massively leading to loop instability. Traditional fast feedback methods are not sufficient to abate the pseudo virtual ground pole.

To circumvent this unwanted loop delay, a linear proportional path, $A4$, shown in Fig. 5.23 adds a fast path around oscillator-based integrators $INT1$ and $INT2$ creating an additional zero in the loop. This zero is optimized to compensate for pseudo virtual ground and oscillator imperfections, and permit impulse response congruency.

Replacing the final integrator with an oscillator-based integrator/quantizer proves to be an impractical solution. While implementing $INT3$ as a VCO-based

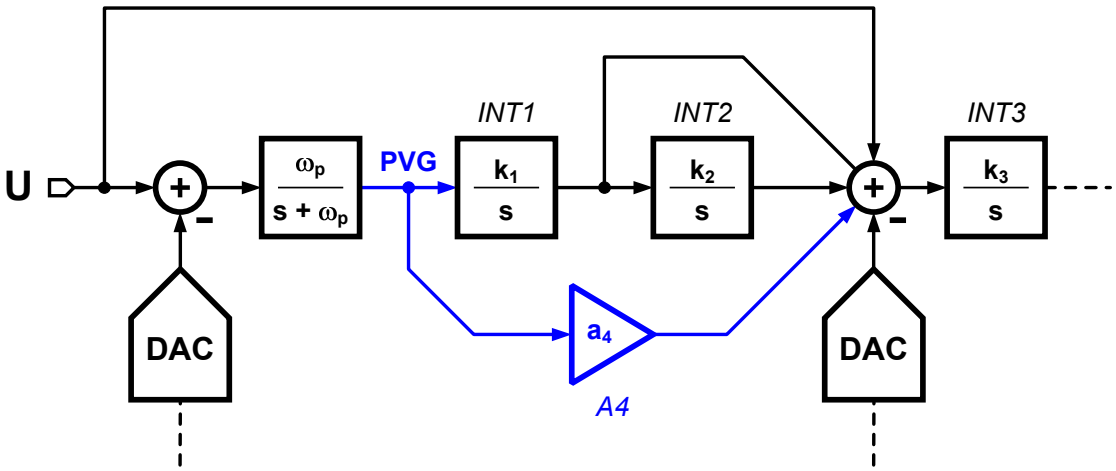


Figure 5.23: Linear proportional path $A4$ to compensate pseudo virtual ground and oscillator poles.

phase quantizer would create a completely active-RC integrator free design, its pseudo virtual ground pole exacerbates loop delay problems. Because the integrator's output is a phase-domain signal, a feed-forward branch solution would first require proportional voltage-to-phase conversion (i.e. a voltage-controlled delay line, VCDL) and summation in the phase domain. A VCDL-based proportional path would add additional intrinsic delay, and would be difficult to compensate for this added excess loop delay. In [37], a VCO-based integrator/quantizer overcame this problem by using a small load resistor at the VCO input to artificially lower the pseudo virtual ground impedance at the expense of large power consumption. This added power consumption was deemed unsatisfactory for this design, and $INT3$ is implemented with a traditional active-RC integrator followed by a flash-based quantizer.

5.6 Loop Gain Optimization

Discussion of loop gain optimization begin with excess loop delay compensation. Traditional ELD compensation begins with a discrete time loop gain prototype, knowledge of the feedback DAC pulse shape, and sampling clock period [26]. The loop gain of the discrete time prototype, shown in Fig. 5.2, is given by (5.26). Applying the zero order hold discrete time to continuous time mapping to (5.26) produces the ideal continuous time loop gain (5.29).

$$LG(z) = -\left(\frac{a_1 I_z}{1+gI_z^2} + \frac{a_2 I_z^2}{1+gI_z^2} + 1\right) \tag{5.26}$$

$$I_z = \frac{z^{-1}}{1-z^{-1}} \tag{5.27}$$

$$LG(s) = d2c_{ZOH}\{LG(z)\} \tag{5.28}$$

$$I = \frac{k}{s} \tag{5.29}$$

Equation (5.26) lacks consideration of quantizer and feedback DAC delay. This delay is chosen to be fixed at one clock period. An excess loop delay compensation path with gain a_5 is added around the quantizer yielding

$$LG_{ELD}(z) = z^{-1}\big\{LG(z) - a_5\big\}. \tag{5.30}$$

Equation (5.30) fails to account for additional poles associated with oscillator-based integrators. For this reason, the loop gain is constructed first in the s-domain and then back converted to discrete time for impulse response evaluation. Equation (5.31) is the transfer function associated with the pseudo virtual ground pole, and Eqs. (5.32) through (5.34) show the integrator transfer functions with

additional poles and finite gain limitations.

$$P = \frac{1}{s/\omega_0 + 1} \tag{5.31}$$

$$I_{P1} = I \cdot \frac{1}{s/\omega_1 + 1} \tag{5.32}$$

$$I_{P2} = I \cdot \frac{1}{s/\omega_2 + 1} \tag{5.33}$$

$$I_{P3} = \frac{A_0}{s^2\left(\frac{1}{\gamma k_3 \omega_a}\right) + s\left(\frac{A_0+1}{\gamma k_3} + \frac{1}{\omega_a}\right) + 1} \tag{5.34}$$

Next, the optimized loop gain transfer function is constructed in stages given by

$$LG_{OPT1}(s) = -\left(\frac{a_1' P \cdot I_{P1}}{1 + g' I_{P1} \cdot I_{P2}} + \frac{a_2' P \cdot I_{P1} \cdot I_{P2}}{1 + g' I_{P1} \cdot I_{P2}} + a_4' P + \frac{1}{\alpha}\right) \tag{5.35}$$

$$LG_{OPT2}(s) = \frac{I_{P3}}{\alpha}, \tag{5.36}$$

where α is the inverse quantizer gain. Each of the *prime* gain coefficients are tuned versions of the original coefficients. Converting from continuous time to discrete time results in

$$LG_{OPT1}(z) = \text{c2d}\{LG_{OPT1}(s)\} \tag{5.37}$$

$$LG_{OPT2}(z) = \text{c2d}\{LG_{OPT2}(s)\}. \tag{5.38}$$

Finally, excess loop delay compensation is accomplished by applying a differentiated quantizer output to the input of the final integrator. The final optimized discrete time loop gain equation is given by

$$LG_{OPT}(z) = \left\{z^{-1} \cdot (LG_{OPT1}(z) - 1) - a_5'(z^{-1/2} - z^{-1})\right\} \cdot LG_{OPT2}(z). \tag{5.39}$$

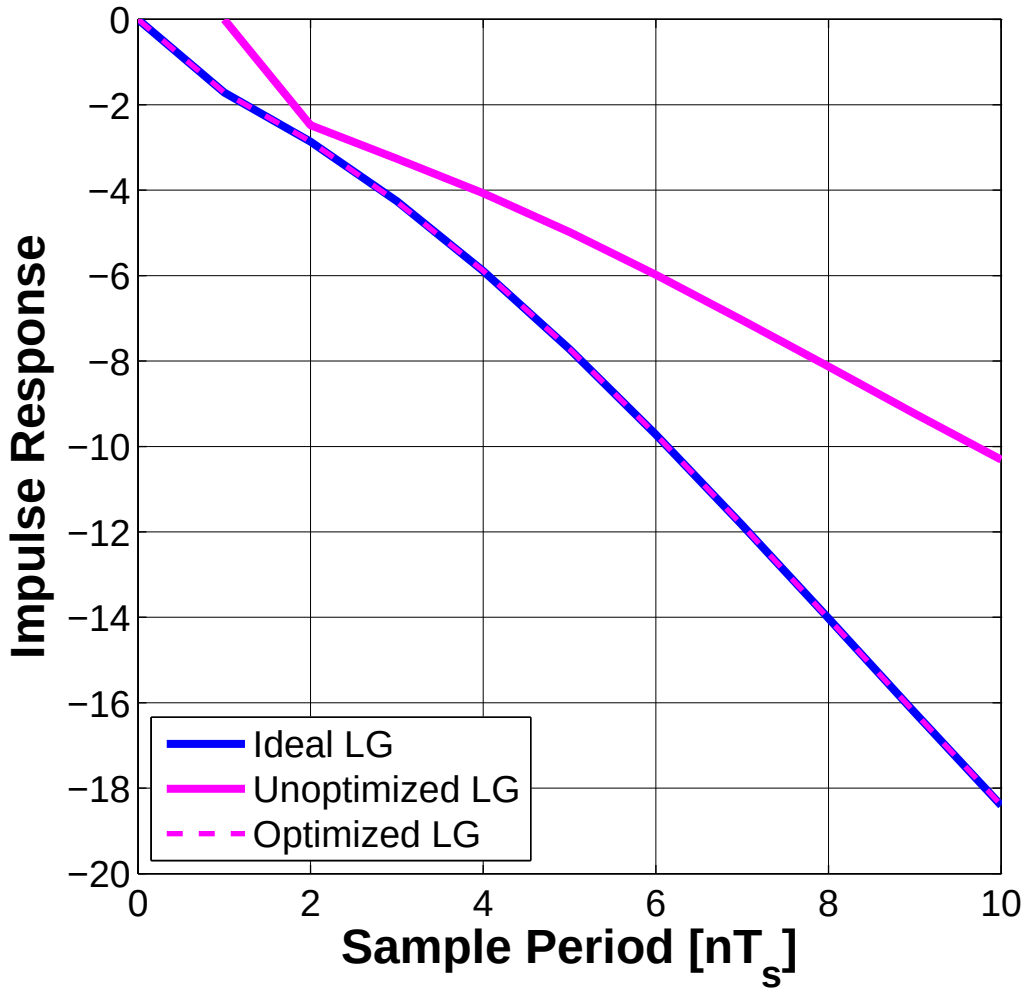


Figure 5.24: Loop gain impulse response.

5.6.1 Impulse Response Matching

After obtaining discrete time equations for both the ideal loop gain (5.30) and optimized loop gain (5.39), the process of optimization can begin. First, the *prime* gain coefficients of (5.39) are initialized to those found in (5.30). Next, the impulse response for each for each transfer function is calculated for ten samples. The RMS error $\|LG(n) - LG_{OPT}(n)\|_2$ is calculated, and a Matlab nonlinear search algorithm, *fminsearch*, iteratively seeks to minimize this error [58].

Figure 5.24 shows the impulse response for the ideal loop gain, and the optimized loop gain before and after optimization. The ideal and post optimized loop gain magnitude responses are plotted in Fig. 5.25. This method of loop optimization results in good matching of high frequency loop gain.

Figure 5.26 shows the magnitude response of the ideal and optimized noise transfer functions. Once again, there is good agreement in high frequency response except for a small ripple in the optimized NTF. Due to the limited number of samples used in the impulse response and finite gain bandwidth errors in the third integrator, optimized low frequency loop gain deviates significantly from the ideal loop gain. Fortunately, reduced ability of quantization noise suppression is negligible because device thermal noise is the dominate noise source below 40 MHz.

5.7 Simulation Results

Nanometer scale silicon production times are on the order of several months and have justified the use and cost of advanced EDA tools for design verification. Differing from their voltage-based affiliates, verification of time-based data

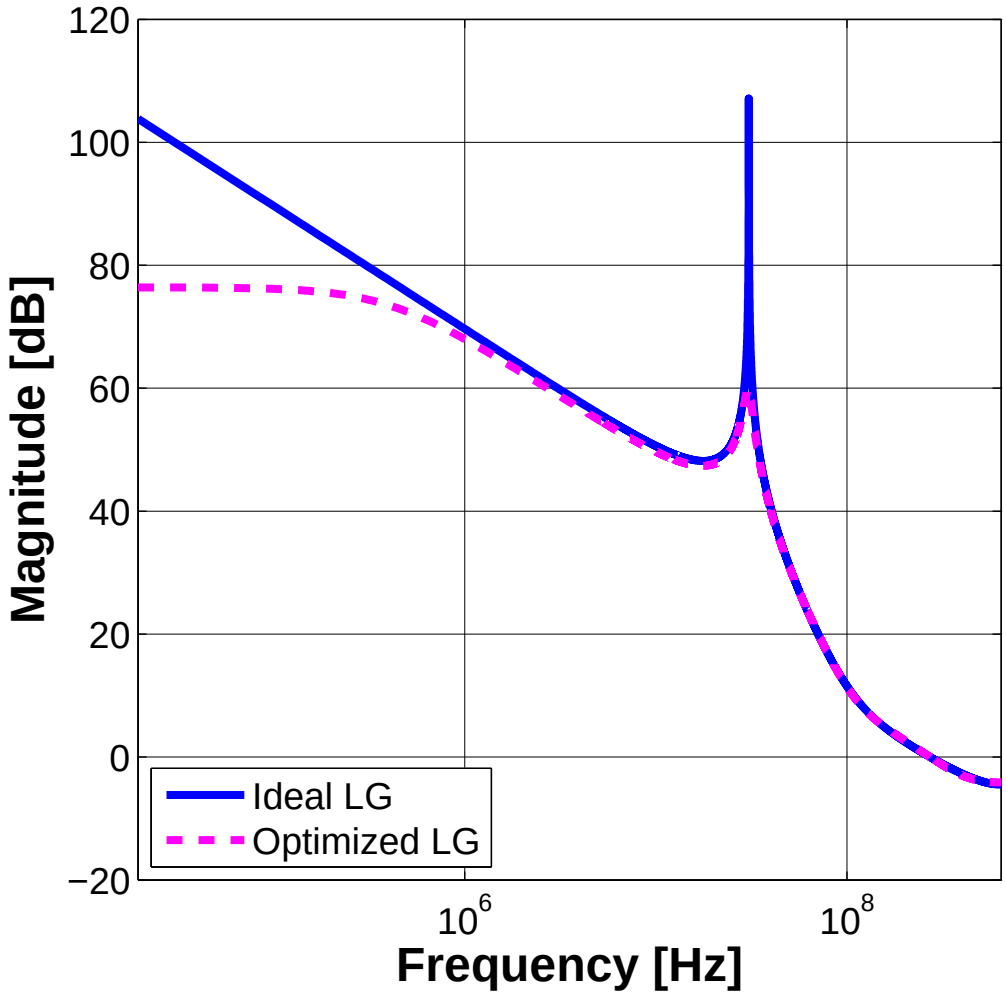


Figure 5.25: Loop gain magnitude response.

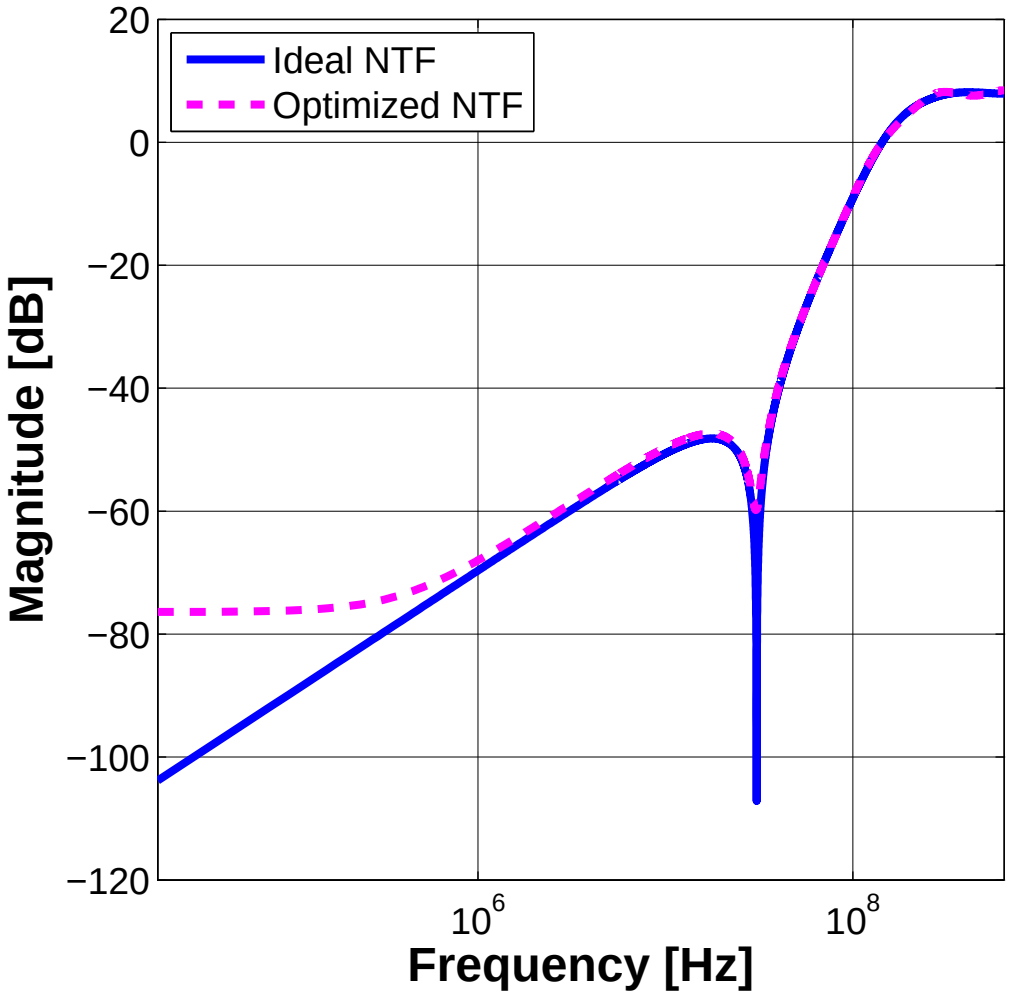


Figure 5.26: Noise transfer function magnitude response.

converter circuit designs requires small time steps in order to ensure simulation accuracy. This requirement of increased simulation accuracy necessarily increases simulation time, which can be on the order of weeks. With much of a designer's time spent verifying a design, it becomes more efficient to develop an accurate, robust mathematical model to cut initial verification time from weeks to minutes.

To this end, a SIMULINK model of the proposed PLL-Based Delta-Sigma Modulator was developed to allow exploration of various circuit non-ideal effects. These effects include thermal and flicker noise sources, VCO phase noise and number of phase outputs, DAC mismatch and jitter, op-amp finite gain and bandwidth, quantizer delay and bandwidth, and gain coefficients. While other high level modeling tools are available such as Verilog-A, Verilog-AMS, and CppSim, SIMULINK was found to have the rapid prototyping benefit afforded by its GUI interface and access to an interpolating zero-crossing detection feature. This interpolating zero-crossing detection feature proves invaluable in time-based circuit modeling. Unlink the *cross* function in Verilog-A, SIMULINK's variable step simulation engine will pause after a zero-crossing event. Through interpolation, SIMULINK estimates the zero-crossing time and evaluates the system at that time point. This greatly improves time resolution without forcing the simulation engine to run with very small maximum time steps. A 4096-point simulation takes less than a minute on an aging PC.

Figure 5.27 plots the power spectral density (PSD) of the PLL-Based Delta-Sigma Modulator SIMULINK model for 4096 points. A small random noise source with variance less than the quantization noise ensures disassociation between simulation runs and allows spectrum averaging. Thermal noise sources are not included to allow comparison of the ideal NTF envelope and simulated shaped quantization noise spectrum. Op-amp finite gain limits low frequency quantization noise sup-

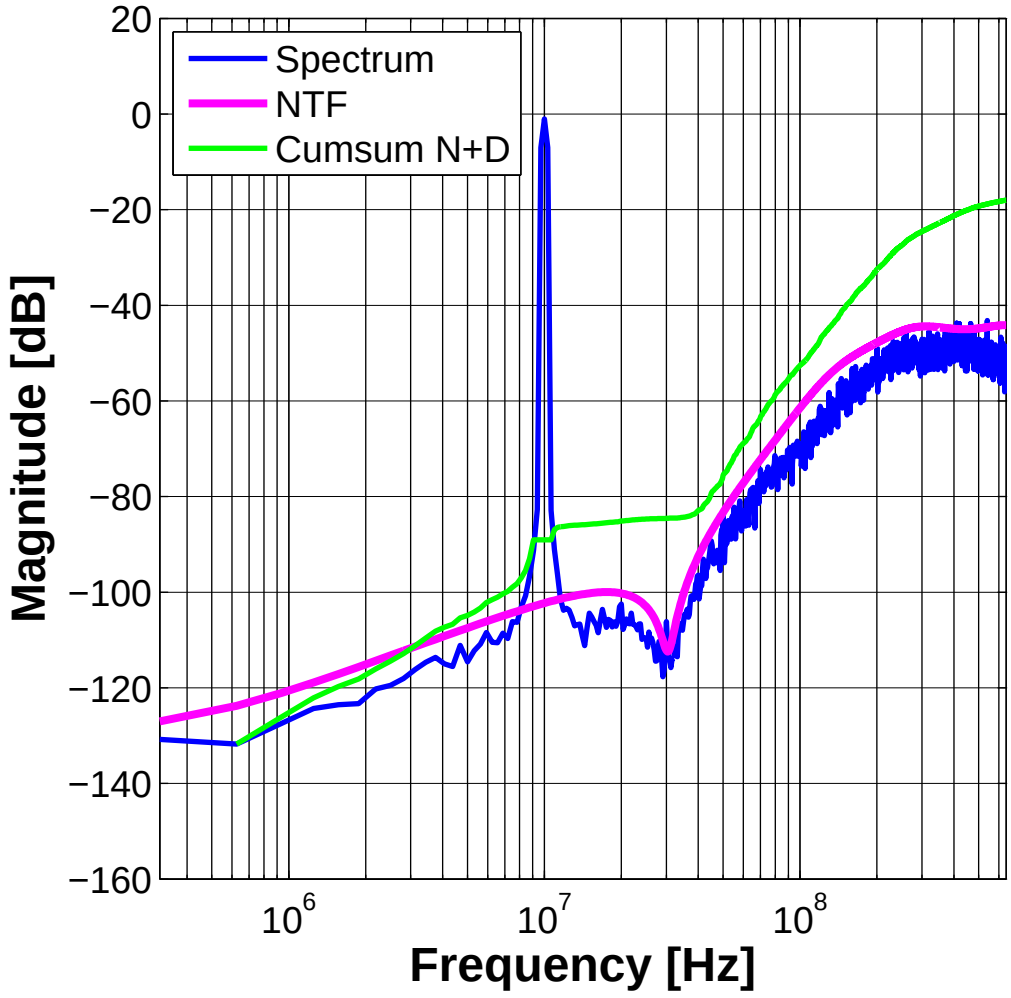


Figure 5.27: SIMULINK model without thermal noise sources simulated output spectrum with 8x averaging, NTF magnitude response, and cumulative sum noise.

pression, while phase detector delay and finite flash ADC bandwidth cause some small peaking in high frequency quantization noise. Modeled $VCO1$ nonlinearity generates an insignificant third harmonic tone.

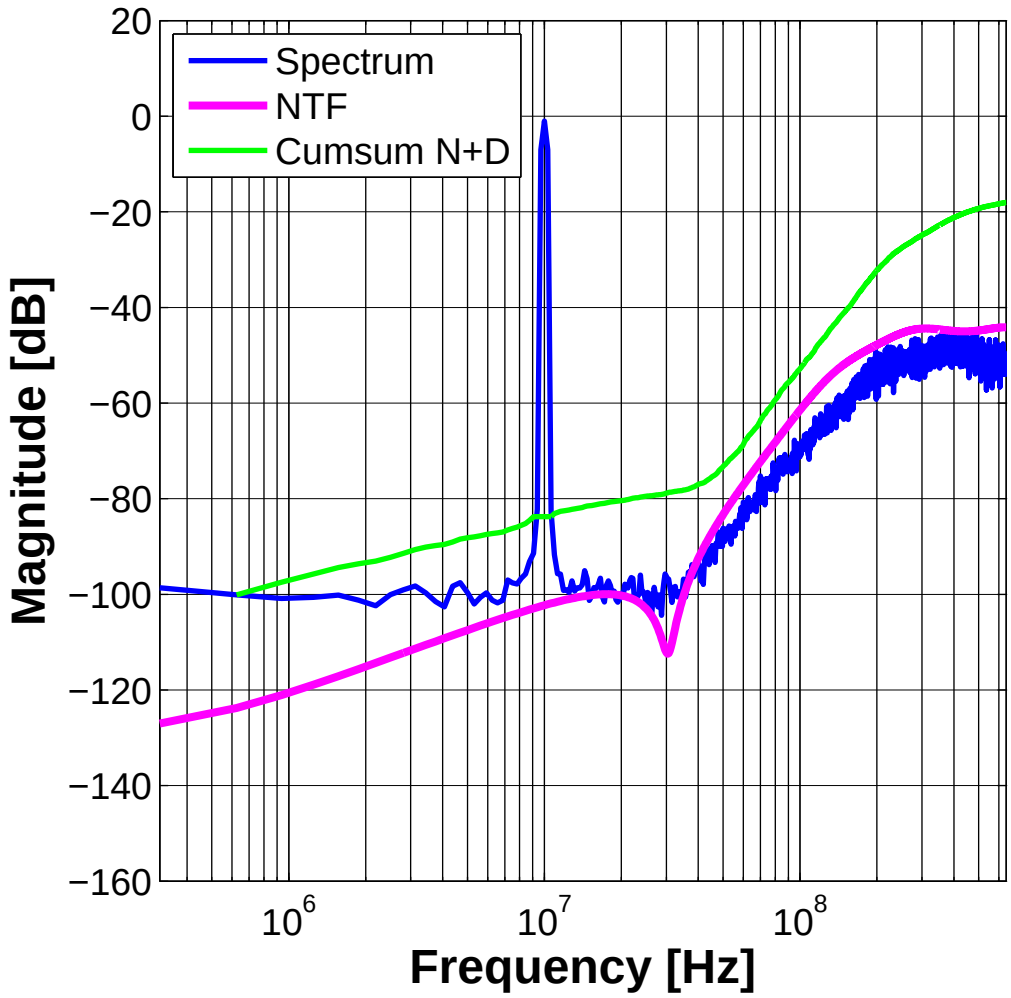


Figure 5.28: SIMULINK model simulated output spectrum 8x averaging with NTF magnitude response and cumulative sum noise.

Figure 5.28 shows the 8x averaged, 4096 point power spectral density (PSD) of the SIMULINK model. Estimated thermal and flicker noise sources from the input resistors, feedback DACs, VCOs, op-amp, and transconductors are included.

A 10 MHz input tone with magnitude -1 dB full-scale produces 77.6 dB SNDR and 12.6 bits ENOB in a 40 MHz bandwidth. Modulator overload occurs with input magnitude exceeding ≈0.5 dB FS. Note that effects of DAC mismatch are not included in this simulation result.

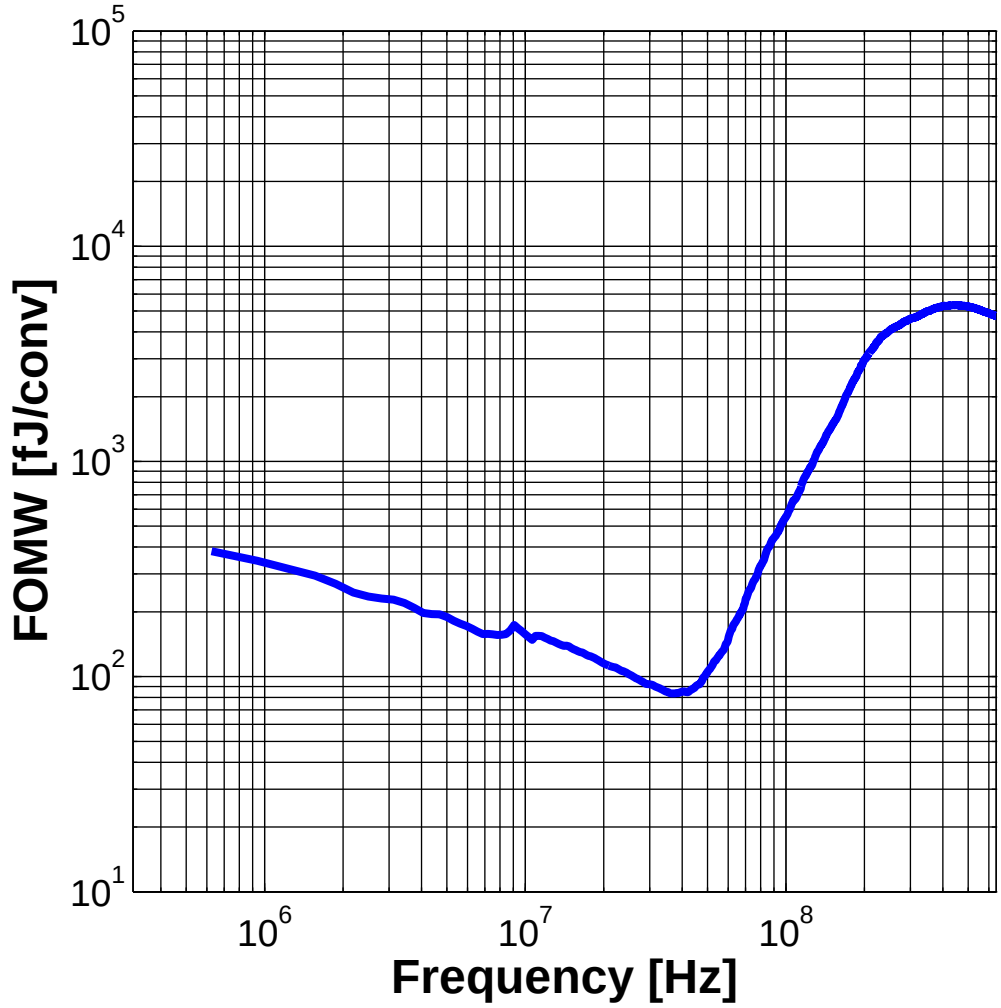


Figure 5.29: SIMULINK model simulated Walden figure of merit.

Figure 5.29 plots the Walden Figure of Merit versus frequency for the cumulative summed noise in Fig. 5.28 [61]. Future top-level circuit simulations produce the conservative power consumption estimate of 43 mW, which is used to calculate

this plot. The minimum figure of merit occurs at approximately at the specified signal bandwidth of 40 MHz. At less than 40 MHz, thermal noise dominates SNDR, and at above 40 MHz, quantization noise dominates SNDR. In most cases it is more power efficient to suppress quantization noise by increasing $\|H(\infty)\|$; however, in the case of this architecture, increasing $\|H(\infty)\|$ beyond 2.5 met with increased risk of instability.

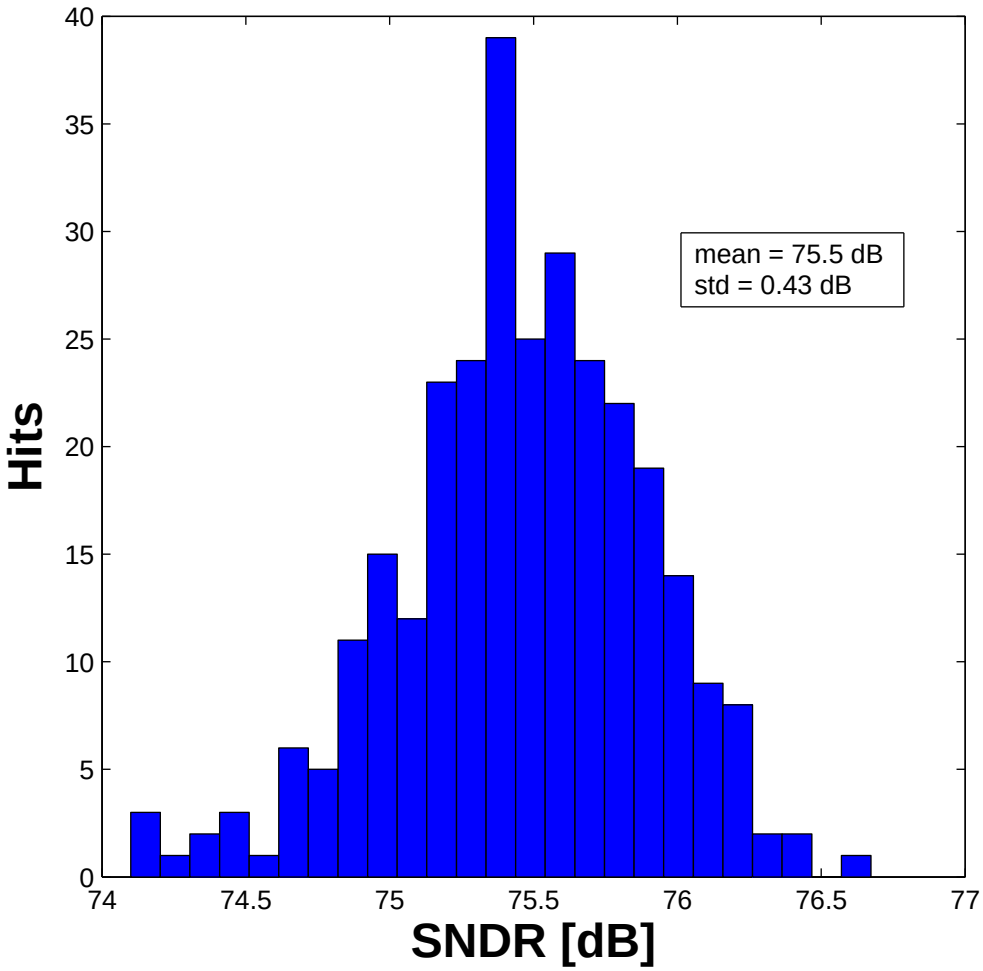


Figure 5.30: Histogram of DAC1FD, DAC2FD, and DAC2HD mismatch for 300 Monte Carlo simulations.

To this point the effect of DAC mismatch has not been included. All three

DACs (DAC1FD, DAC2FD, and DAC2HD) are implemented with current steering non-return-to-zero pulse shapes switching at a rate of 1.28 GHz. It has been noted in previous research that common rotational algorithms used to shape DAC mismatch cause continuous-time current steering DACs to suffer from increased inter-symbol interference (ISI) when DAC codes exceed -6 dB FS [38]. An ISI and mismatch shaping technique solves this problem, but it operates at frequencies an order of magnitude slower than the PLL-Based Delta-Sigma Modulator design requires [62]. Therefore, in order to meet 12 bit ENOB performance, the DACs rely on intrinsic matching. Specifically, the $1-\sigma$ mismatch of DAC1FD, DAC2FD, and DAC2HD are 11.4, 9.1, and 10.4 bits respectively. Figure 5.30 shows a histogram plot of SNDR of a 300 run Monte Carlo simulation with the aforementioned DAC mismatch parameters and other thermal/flicker noise sources. The mean is 75.5 dB, and the standard deviation is 0.43 dB. Mismatch performance is limited by DAC1FD mismatch yet further mismatch reduction would result a DAC with physical size that rapidly becomes unwieldy.

5.8 Summary

This chapter has introduced the PLL-Based Delta-Sigma Modulator architecture which makes use of ring oscillators as ideal integrators. Following the traditional design flow, the modulator was first prototyped in discrete time. The process of substituting time-based signal processing circuits revealed two additional challenges: a bandwidth limiting oscillator pole and a virtual ground destroyed by a high impedance VCO input. The inclusion of a fast feed forward gain around the oscillator-based integrators mitigated both issues simultaneously. A robust time-domain PLL-Based Delta-Sigma Modulator model developed in Mat-

lab/SIMULINK allows the exploration of non-ideal circuit effects. Such effects include noise, mismatch, nonlinearity, delay, and gain coefficients. A similar time-domain Verilog-A model takes approximately two orders of magnitude longer to run, yet is less complete and accurate. In a symbiotic manner, the SIMULINK model is used to predict circuit performance and requirements, and circuit block simulation results can be added back into the SIMULINK model to further refine the model. The end result is a rugged model that accurately and quickly predicts circuit performance.

CHAPTER 6. DESIGN OF A PLL-BASED DELTA-SIGMA MODULATOR

This chapter describes the PLL-Based Delta-Sigma Modulator specification and circuit design of principle building blocks. The top level circuit block diagram is illustrated in Fig. 6.1. This third order modulator is constructed with

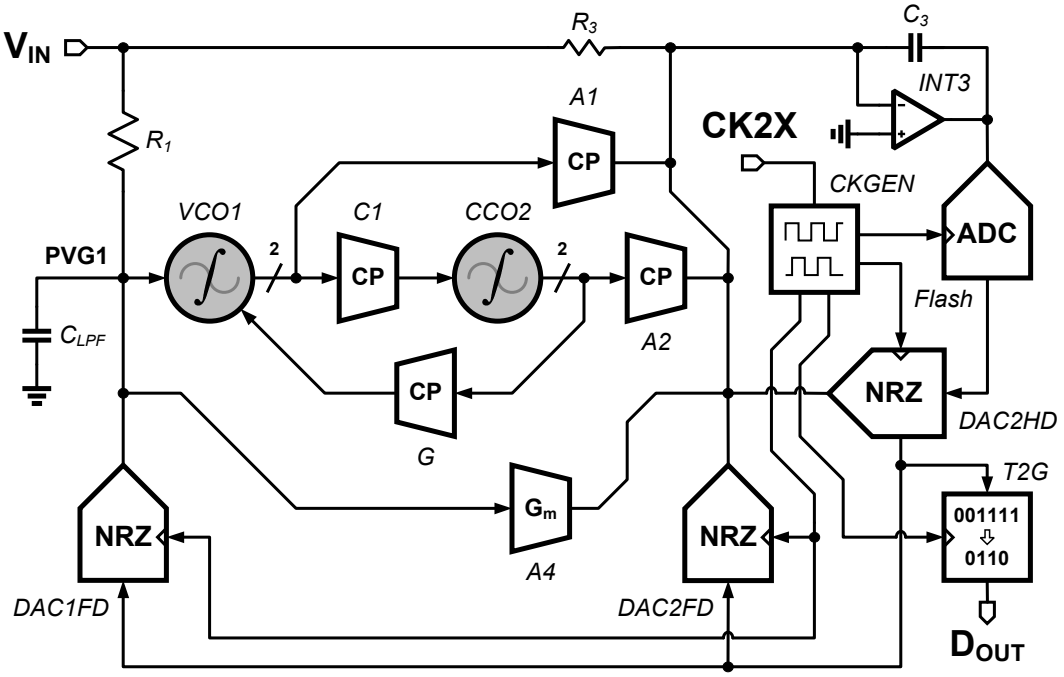


Figure 6.1: Block diagram of the proposed third order PLL-Based Delta-Sigma Modulator.

input resistors, R_1 and R_3; passive low-pass filter on net $PVG1$; voltage-controlled oscillator-based integrator, $VCO1$; current-controlled oscillator-based integrator, $CCO2$; two-phase source-switched charge pumps, $A1$, $A2$, $C1$, and G; active-RC integrator, $INT3$; flash-based ADC, $FLASH$; linear transconductor, $A4$; primary full-delay NRZ feedback DAC, $DAC1FD$; secondary full-delay NRZ feed-

back DAC, $DAC2FD$; loop-delay compensating half-delay NRZ feedback DAC, $DAC2HD$; clock generator circuit, $CKGEN$; and thermometer-to-Gray coder, $T2G$.

Table 6.1 lists the target specifications for the prototype delta-sigma modulator with goal of creating a circuit to exceed the requirements of a typical 802.11n wireless receiver [63, 64].

Table 6.1: ADC Target Specifications

Order	3
OSR	16
R_1	400 ohms
ENOB	>12 bits
Signal Bandwidth	40 MHz
Sampling Frequency	1.28 GHz
Technology	65 nm CMOS

6.1 Oscillator Based Integrator

Central to the PLL-Based Delta-Sigma Modulator architecture is the ring oscillator-based integrator, which can be implemented with either voltage or current input control. It is the time-domain circuit equivalent of the active-RC integrator. The mathematical integration function is performed in the phase-domain with a linear equation model of $2\pi K_V/s$. The oscillator-based integrator can maintain high dynamic range independent of supply voltage, and achieve infinite DC gain. Figure 6.2 shows the block diagram of VCO integrator, $VCO1$. It is comprised of a PMOS input fully-differential transconductor connected to current-controlled ring

oscillator loads, operating at zero-input frequency, $f_{osc,0} = F_s/2$. The transconduc-

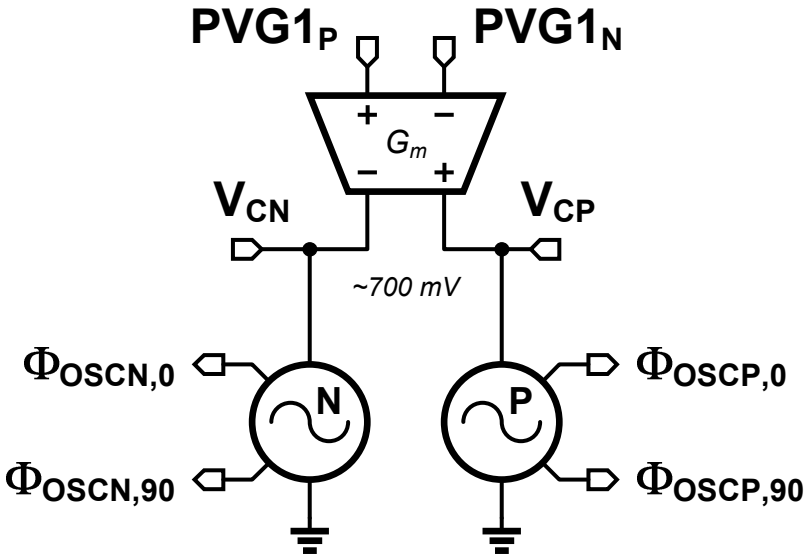


Figure 6.2: Two phase voltage-controlled oscillator-based integrator with differential linearized transconductor and separate current-controlled ring oscillator loads.

tor input common-mode voltage is 600 mV, and the nominal voltage drop across the current-controlled oscillators is ∼700 mV. Inputs V_{CP} and V_{CN} are oscillator virtual supply nodes, and serve as input points for resonator gain block, G. Both ring oscillator loads generate 0° and 90° phase outputs, which lessen the sensitivity to the highly probable scenario of $f_{osc,0} \neq F_s/2$. Two oscillator phases were found to be sufficient; however, using more phases would continue to reduce this sensitivity at the expense of additional power and layout complexity. The modulator's second integrator, $CCO2$, is identical to $VCO1$ with the exception of the absence of a linear transconductor circuit.

6.1.1 Ring Oscillator

The circuit diagrams of the ring oscillator and its delay cell and output buffer are shown in Fig. 6.3. The ring oscillator is constructed with eight pseudo-differential resistive feed-forward delay cells and two pairs of inverter-based AC coupled output buffers. Delay cell interconnect lengths are matched, and supply bus connection are tree connected. The pseudo-differential delay cell architecture reduces virtual supply voltage ripple and thus self-induced deterministic jitter. Using eight delay cells facilitates sharper oscillator rise/fall times, which contributes to low phase noise [65]. The delay cell's feed-forward resistors maintain the desired 180° relationship between two oscillator halves without compromising oscillator startup integrity. The low frequency zero of the AC-coupled output buffer causes minimal phase variation over full-scale range of oscillator frequencies.

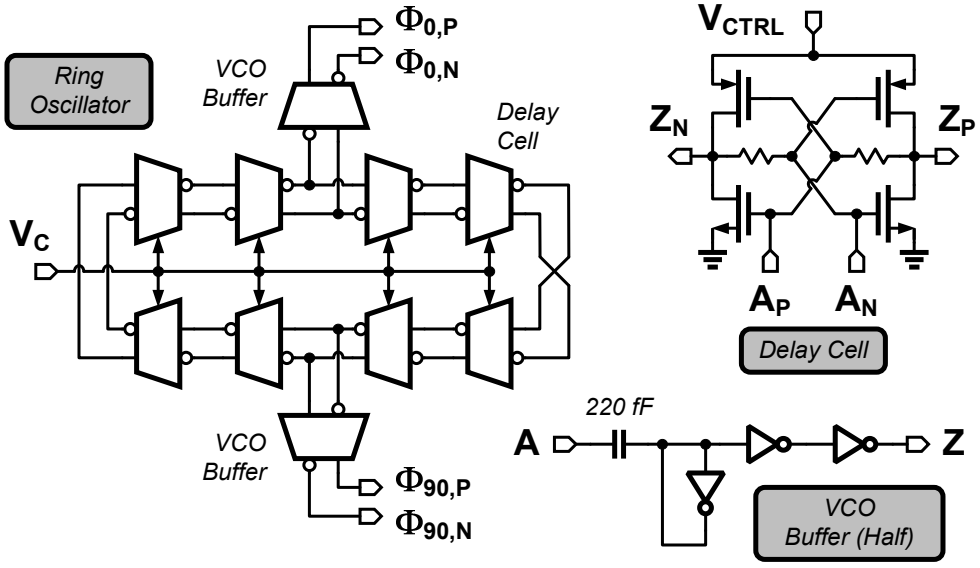


Figure 6.3: Pseudo-differential resistive feed-forward ring oscillator with AC-coupled output buffer.

6.1.2 Linearized Transconductor

Figure 6.4 depicts the linearized transconductor circuit of $VCO1$. Transistors M_1 and M_2 constitute the input differential pair and tail current sources, respectively. Segmented transistor M_{TUNE} operates in deep triode and functions as a split-tail-current, source degeneration resistor according to (6.1) and (6.2).

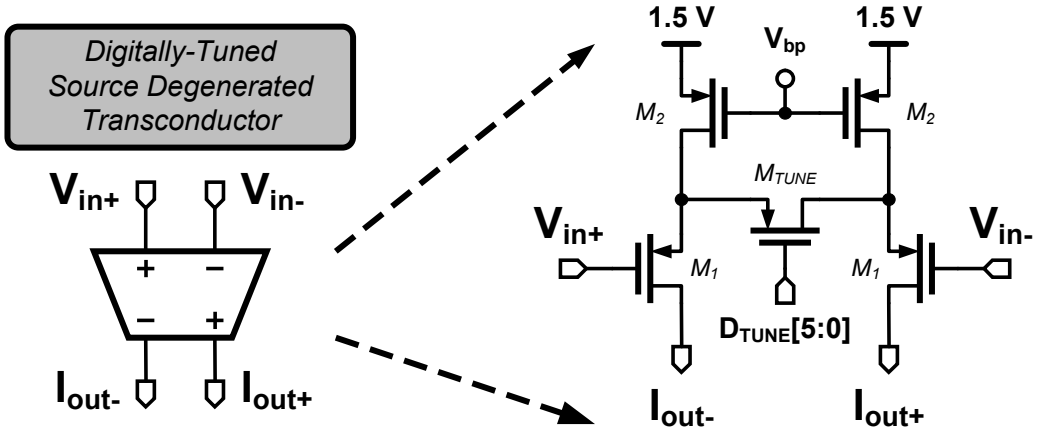


Figure 6.4: Parallel source degenerated transconductor with 6-bit VCO gain tuning and improved linearity.

$$R_{TUNE} = \frac{1}{\mu_p C_{ox} \frac{W}{L}(V_{GS} - V_{TH,p})} \tag{6.1}$$

$$G_m = \frac{g_{m,M1}}{1 + g_{m,M1} R_{TUNE}/2} \tag{6.2}$$

Tuning control signal, $D_{TUNE<5:0>}$, is switched between 1.5 V (V_{off}) and 600 mV (V_{on}) to modulate the transconductance, hence VCO gain, proportional to $1/R_{TUNE}$. The transconductor was designed to have $\pm 25\%$ tuning range to cover anticipated process variation. Additionally, the V_{on} can be adjusted at the expense

of some linearity degradation. The current-controlled ring oscillator load derives its bias current solely from $I_{D,M2}$ without the need for an additional bias current. A 1.5 V supply voltage is required to keep transistors M_1 and M_2 in saturation. While the split-tail-current method of source degeneration causes M_2 and M_{TUNE} device noises to become a significant contributor, it allows the supply voltage to remain lower than it would be with series source degeneration. Also, if care is taking during power up, the 1.5 V supply voltage will not appear fully across any transistors.

Inverter-based ring oscillators exhibit a mostly linear dependence on control voltage. Applying (6.4), ring oscillator current is quadratically dependent on V_C, when V_C exceeds $2V_{TH} + 2V_{ov}$.

$$V_{GS} = |V_C - V_{DD}| \tag{6.3}$$

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{6.4}$$

$$\tag{6.5}$$

A common source transconductor in saturation can generate a large-signal quadratic dependent current. However, this work leverages a linear transconductor shown in Fig. 6.4, leading to each current-controlled ring oscillator having a square root frequency response to linear input current. Figure 6.5 shows the frequency versus control voltage, $PVG1$, for both OSC_P and OSC_N, and their difference frequency.

It is instructive to note that the difference between f_{oscp} and f_{oscn} (performed in the system by XOR phase detectors) results in an even function of VCO gain and greatly improved linearity. Figure 6.6 illustrates the VCO gain of $VCO1$ which has a nominal VCO gain of $K_{VCO1} = 800\,\text{MHz/V}$. Resonator gain block

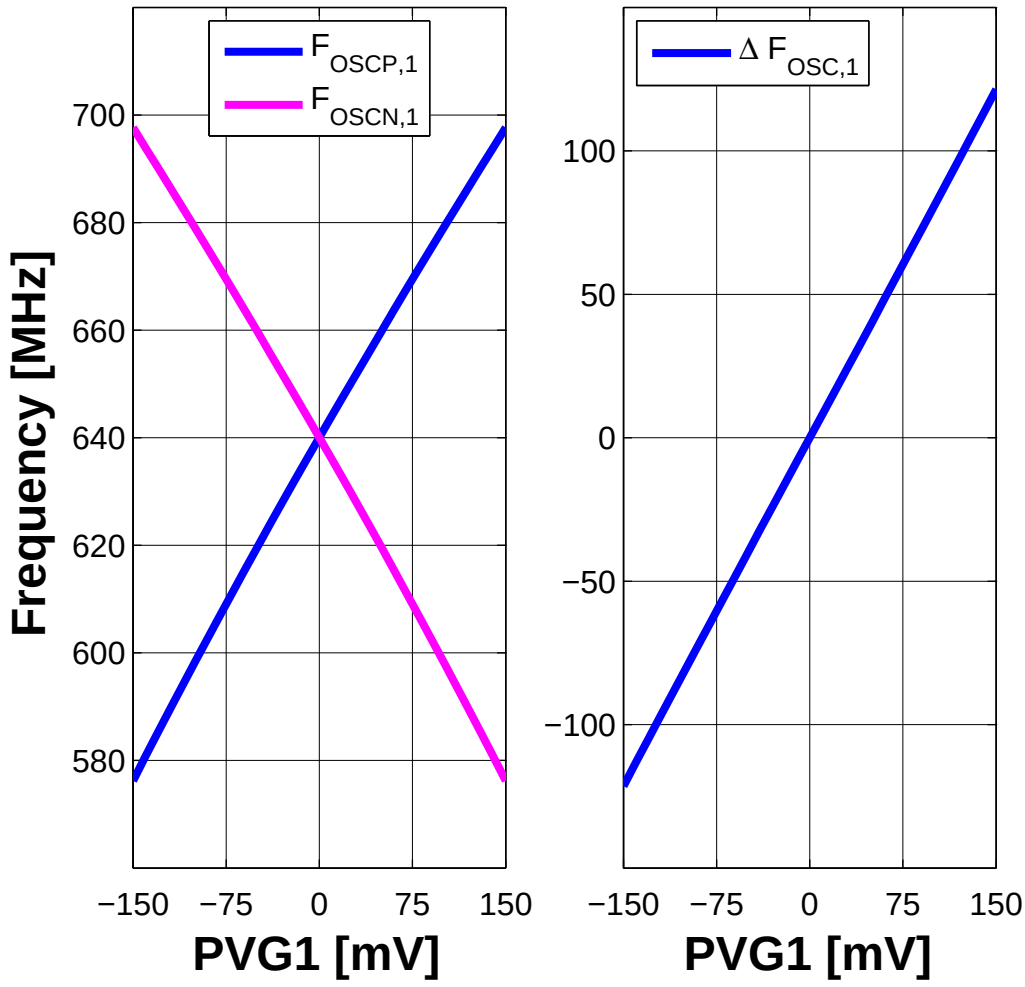


Figure 6.5: Frequency of each oscillator in $VCO1$ and their difference versus input control voltage.

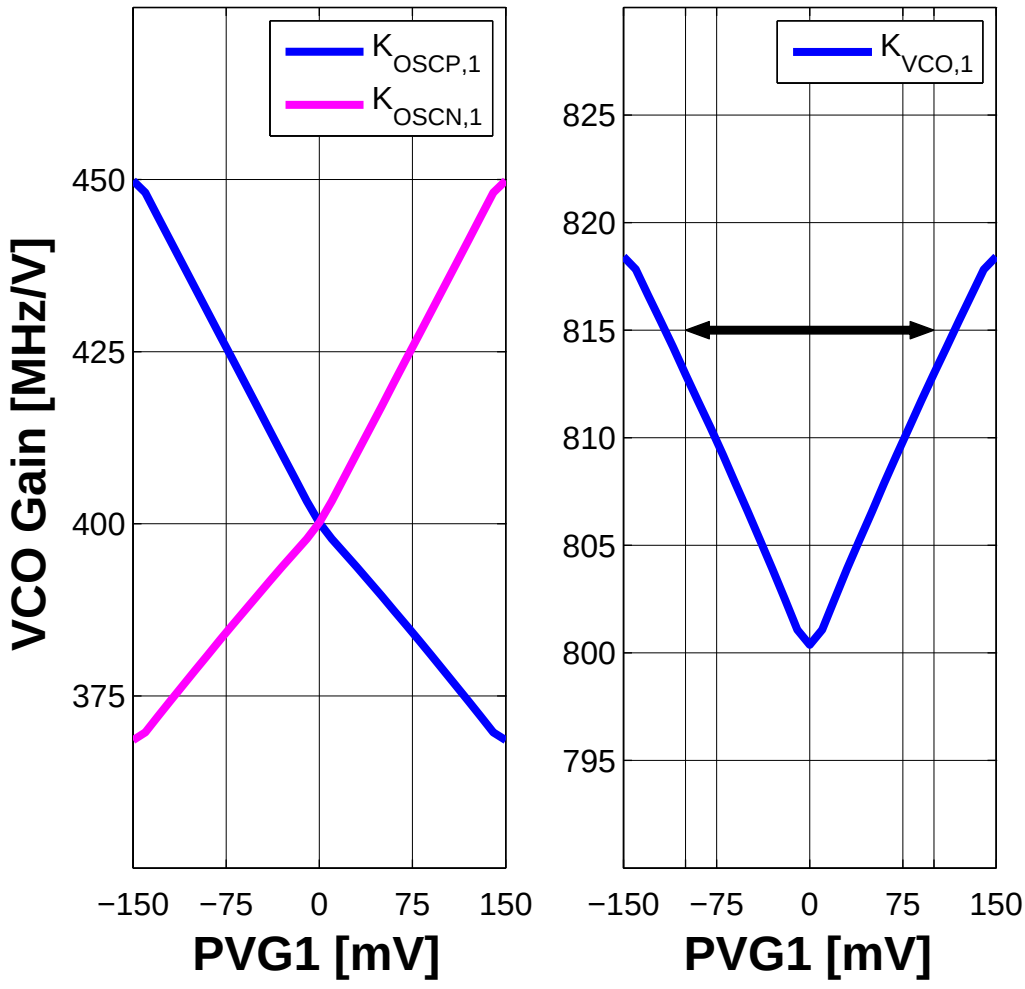


Figure 6.6: VCO gain of each oscillator in $VCO1$ and their difference versus input control voltage.

G uses a source-switched charge pump to implement a two-point modulated current pulse. This two-point method is linear by design, and has gain $K_{VCO1,G} = 27.8\,\text{MHz/V}$. Linearity performance in oscillator-based integrator $CCO2$ benefits from the same two-point modulator of $C1$. While $CCO2$ is not voltage controlled perse, an equivalent voltage gain is calculated to be $K_{CCO2,C1} = 237\,\text{MHz/V}$.

During initial foreground calibration, test circuits allow direct observation and control of oscillator gains. Setting the analog input to zero and primary feedback DAC to $\pm 1LSB$ forces a current through input resistor R_1, and creates a voltage difference given by $V_{PVG1} = R_1 \cdot \pm I_{DAC1FD,LSB}$. The second oscillator-based integrator, $CCO2$, is tuned by disabling the $C1$ phase detector, forcing its charge pump on, and adjusting the charge pump bias current. The resonator, G, is tuned in a similar manner.

6.1.3 Oscillator Phase Noise

The single-sideband phase noise of one $VCO1$ ring oscillator is shown in Fig. 6.7. The typical phase noise is -112.7 dBc/Hz and -110.8 dBc/Hz at 1 MHz carrier offset for white only and all noise sources, respectively. The $1/f^3$ noise corner frequency is ¡1 MHz.

Phase noise contributions are equally split between the transconductor and ring oscillators. It uses 2.4 mA current from a 1.5 V supply for each of the two ring oscillators. Oscillator-based integrator $CCO2$ operates from a 1.2 V supply with similar performance numbers. Through transient simulations, the oscillator parasitic pole frequency was simulated to be nominally 640 MHz.

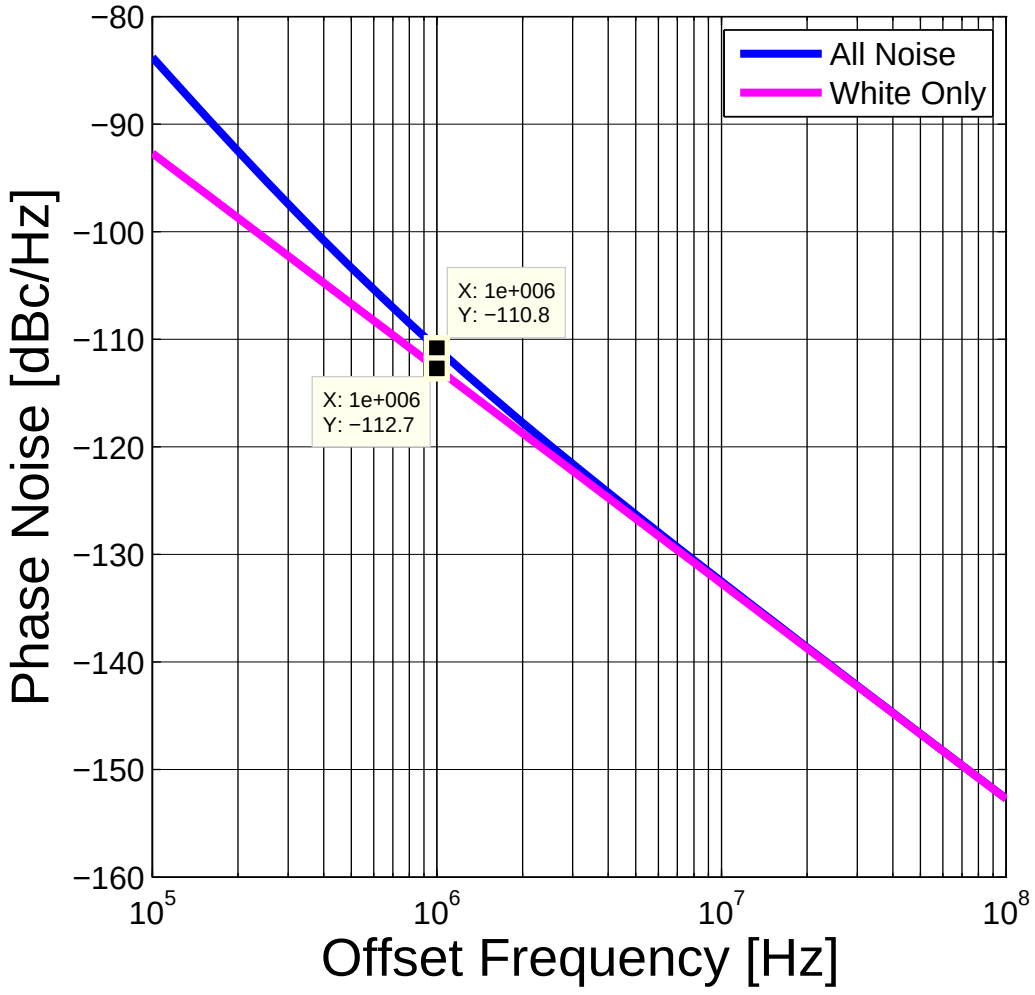


Figure 6.7: The SSB phase noise plot of one $VCO1$ ring oscillator with and without flicker noise sources.

6.2 Time-to-Analog Interface

Using time-based signal processing circuits requires interface circuitry to connect analog-domain inputs and outputs to the time-based circuit. Section 6.1 describes methods to connect analog signals to time-based circuits. The interface remaining to define is the time-to-analog interface. These circuits must extract the time-based signal information and facilitate connection to analog circuitry. Circuit techniques used in analog loop filter phase-locked loops provided inspiration. Specifically, these PLL circuits are the phase detector and charge pump. The phase detector is a time-based circuit block which can calculate the time difference between two signals. A charge pump is a circuit that converts a time-based signal into a proportional current. Described next is the circuit implementations of an exclusive-OR phase detector and a source-switched charge pump.

6.2.1 Exclusive-OR Phase Detector

A static CMOS exclusive-OR phase detector with matched pull up/down networks (depicted in Fig. 6.8), processes the time-based, phase-domain integration performed in oscillator-based integrators, $VCO1$ and $CCO2$. Use of static CMOS avoids the linearity problems associated with dynamic logic at the expense of slightly higher power.

Figure 6.10 illustrates the connections between a two-phase oscillator-based integrator and XOR phase detectors. The XOR phase detector has a linear range of π, phase offset of $\pi/2$, and normalized gain of $1/\pi$, shown in Fig. 6.9.

The XOR phase detector measures the phase difference between ring oscilla-

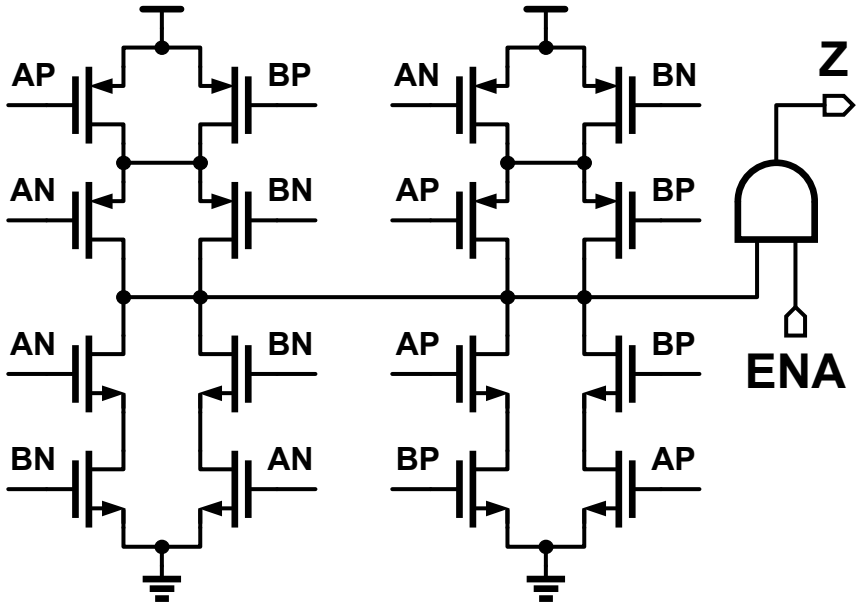


Figure 6.8: CMOS exclusive-OR phase detector with symmetric pull-up/down networks and enable signal.

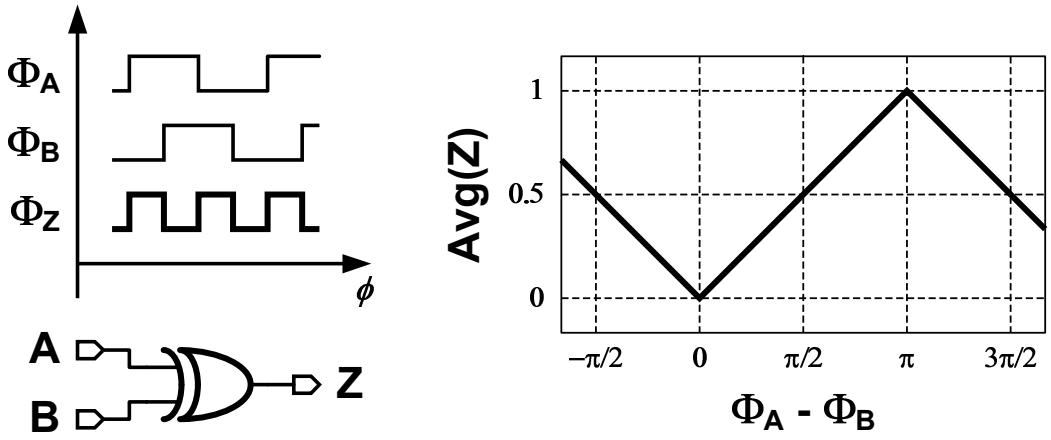


Figure 6.9: Exclusive-OR phase detector timing diagram and transfer function.

tor phases, OSC_P and OSC_N, and generates output pulses with frequency content that is on average two times $f_{osc,0}$. These output signals control downstream phase-to-current circuits more commonly known as charge pumps. An enable signal allows a predefined phase detector state during initial modulator calibration.

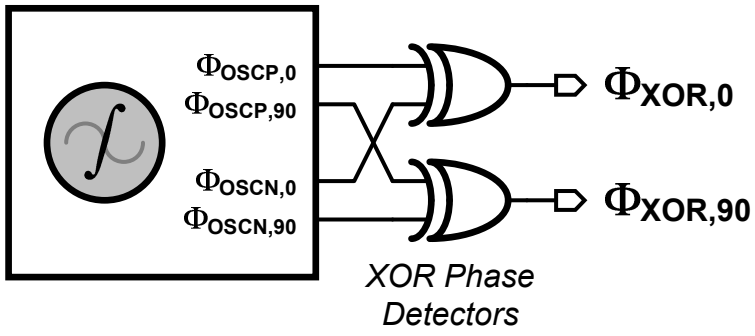


Figure 6.10: Oscillator-based integrator with exclusive-OR phase detectors.

6.2.2 Source-Switched Charge Pump

The charge pump is the second part of the time-to-analog interface circuit. It is implemented with a pseudo-differential source-switch charge pump (SSCP) shown in Fig. 6.11.

Connecting the source terminal of current source transistor M_P to V_{DD} rapidly charges $C_{gs,p}$ to V_{bp}, with complementary action occurring with transistor M_N. Decoupling capacitors on V_{bp} and V_{bn} minimize switching transients. Because M_P and M_N drain capacitors are not discharged (as is the case with the drain-switched architecture), the SSCP has faster current pulse rise/fall times and less propagation delay. Current pulse rise/fall time are important because they limit charge pump linearity full-scale range and contribute adversely to loop delay.

The exclusive-OR phase detectors and sources-switched charge pumps oper-

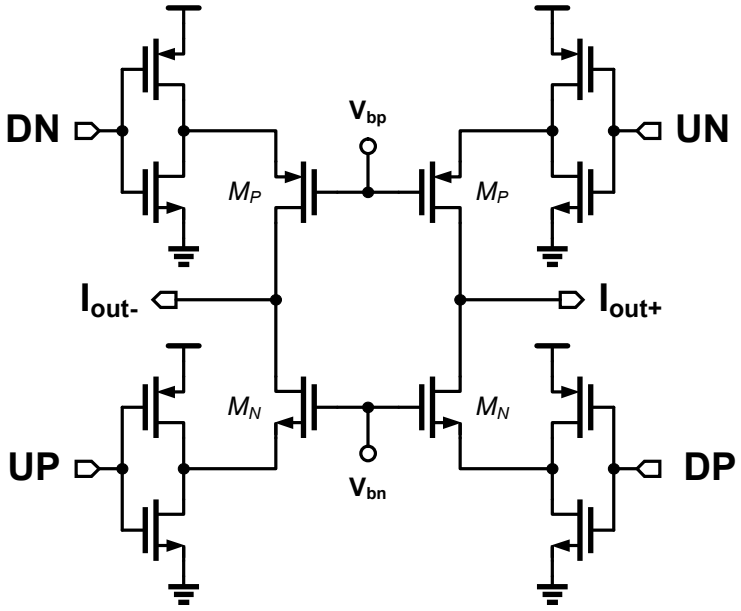


Figure 6.11: Circuit diagram of a pseudo differential source-switched charge pump.

ate from a $1.2V$ supply. They are used to implement the feed-forward gain stages, $A1$ and $A2$; inter-stage gain, $C1$, between $VCO1$ and $CCO2$; and resonator feedback gain between $CCO2$ and $VCO1$. Figure 6.12 shows the simulated transfer function of the $C1$ phase detector and the charge pump.

Circuit operation occurs in the positive gain region between 0-to-π radians. Dynamic mismatch between M_P and M_N currents cause a small differential-mode offset leading to $\overline{I_{cp}} \neq 0.5$ at $\pi/2$. Input phase differences approaching positive gain region extremes exhibit large differential nonlinearity as shown in Fig. 6.13. Dynamic range scaling limits the input range between $\pi/7$ and $6\pi/7$, where linearity is better than 5.5 bits.

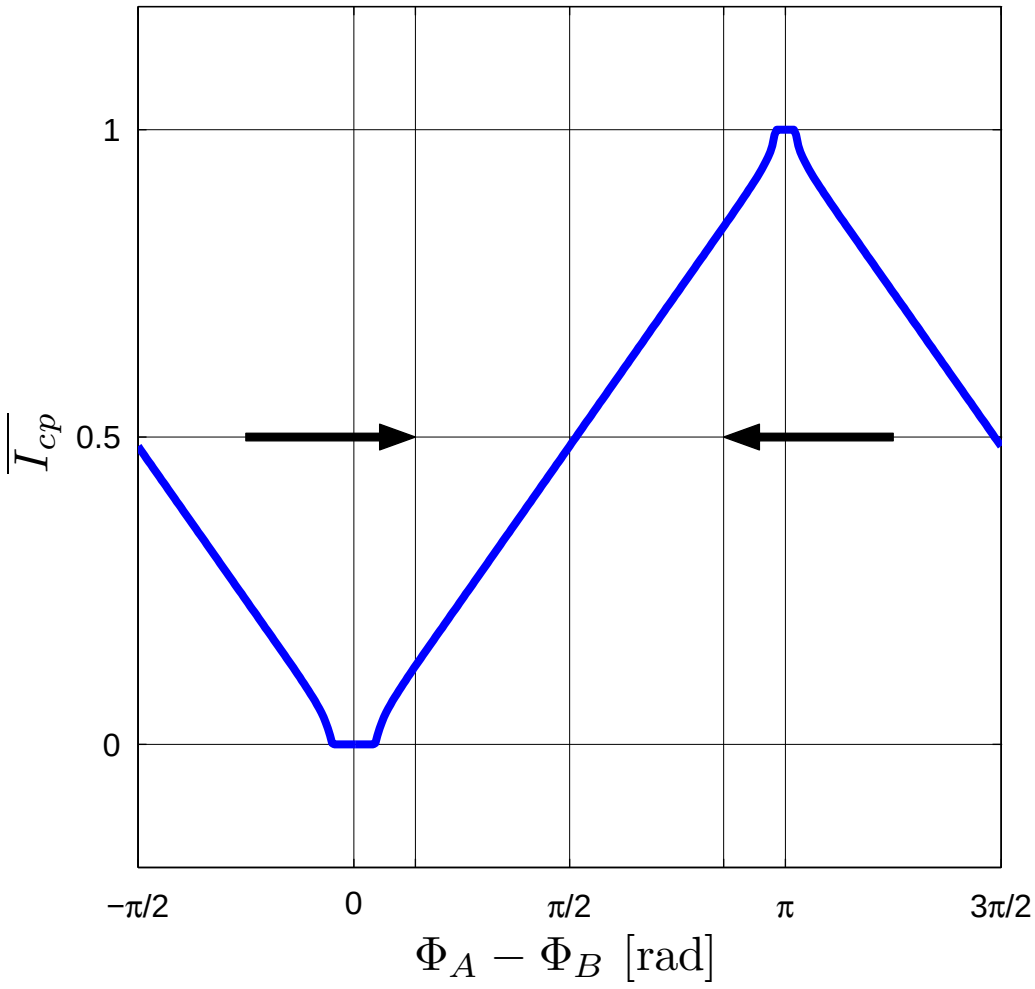


Figure 6.12: Normalized average current (I_{cp}) of $C1$ phase detector and charge pump versus input phase difference ($\Phi_A - \Phi_B$).

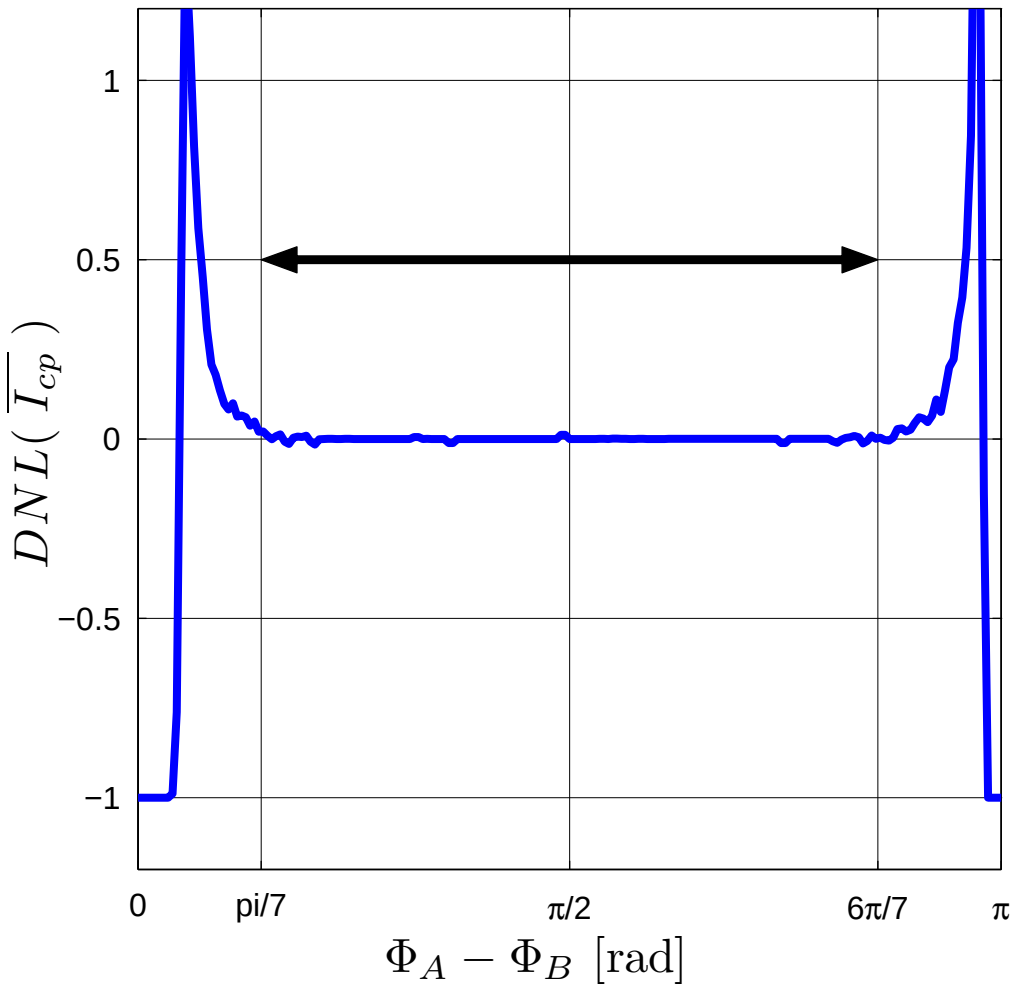


Figure 6.13: Differential nonlinearity of $C1$ average I_{cp}) versus input phase difference ($\Phi_A - \Phi_B$).

6.3 Analog Circuits

Traditional analog circuits still perform critical functions in the PLL-Based Delta-Sigma Modulator architecture. A linear transconductor, current steering DACs, active-RC integrator, and flash ADC round out the remaining analog circuitry.

6.3.1 Linear Transconductor

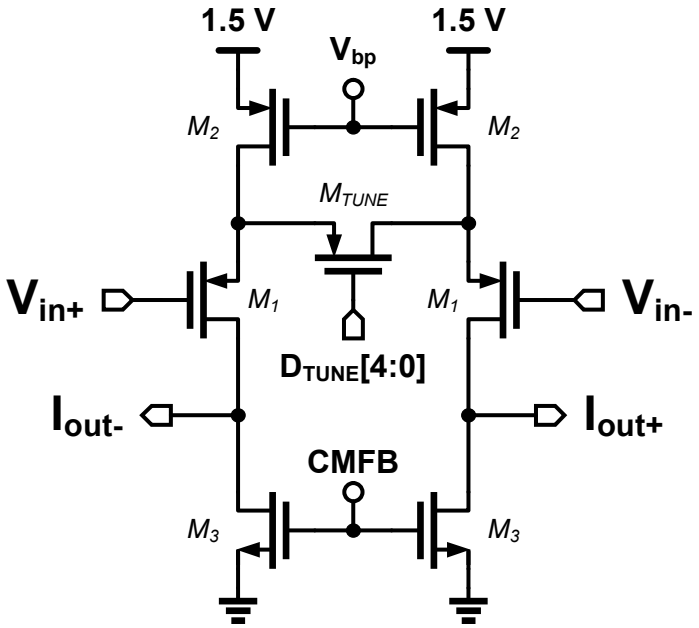


Figure 6.14: Linear transconductor with differential input/output and 5-bit digital trim.

The circuit diagram for linear transconductor $A4$ is shown in Fig. 6.14. It serves as a fast feed forward path to compensate for loop delay introduced by $VCO1$, $CCO2$, and the pseudo virtual ground $PVG1$. The transconductor input stage closely resembles that of the voltage input structure of $VCO1$. An input

common mode voltage of 600 mV necessitates a high supply voltage of 1.5 V to keep transistor M_2 in saturation. A digitally controlled split-tail-current source degeneration transistor controls transconductance while improving linearity. This method is preferable because it incurs no supply headroom penalty; however, it causes noise from tail current source transistors, M_2, to increase output current noise. Transistors M_3 are designed with high over drive voltage for minimal noise, and they are controlled by a separate common mode feedback loop which sets their drain voltage to 600 mV.

6.3.2 Feedback Digital-to-Analog Converter

The PLL-Based Delta-Sigma Modulator makes use of three non-return-to-zero (NRZ) current steering DACs. The DACs are a primary full clock delay DAC, $DAC1FD$, a secondary full clock delay DAC, $DAC2FD$, and a secondary half clock delay DAC, $DAC2HD$. $DAC1FD$ forms the primary feedback path around the entire loop, and its positioning at the modulator frontend dictates stringent linearity performance. $DAC2FD$ and $DAC2HD$ form both a secondary feedback path and loop delay compensating fast feedback path. Each DAC contains 16 individual elements.

Figure 6.15 shows the block diagram for a single DAC cell including sense-amplifier flip-flop [40], low-swing buffer, and 1-bit PMOS/NMOS current steering DAC. Sense-amplifier based flip-flops improve data input sensitivity to small swing complementary inputs which may be present in high speed signal paths. Further, they can be designed to have equal clock-to-Q and clock-to-QB propagation delays which promote glitch less current steering. Low-swing buffers are designed to have asymmetric rise and fall times to minimize current source drain voltage glitches

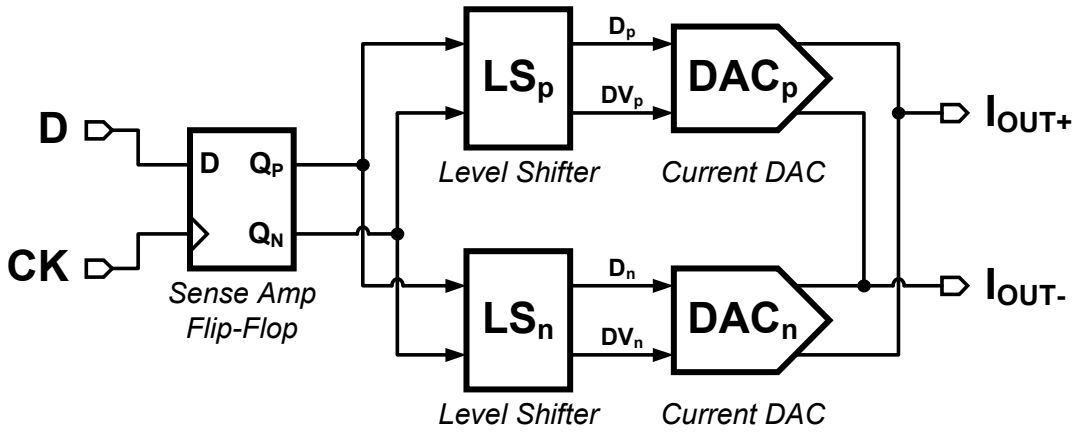


Figure 6.15: Individual DAC cell including sense-amp flip-flop, level shifting low-swing buffer, and 1-bit PMOS/NMOS current steering DAC.

[66]. Current switching of both PMOS and NMOS current sources allows reduction in power consumption and current noise. The penalty is reduction in current source overdrive voltages and double the number of current steering switches and low-swing buffers.

Figures 6.16 and 6.17 show the circuit diagrams of the NMOS and PMOS current steering DAC, respectively. Each circuit consists of a current source transistor, M_X, cascode transistor, M_{XC}, current steering transistor, M_{XS}, and charge injection removal transistor, M_{XV}. Note that X generically refers to the transistor type, either NMOS or PMOS. Each transistor is designed to work in saturation when conducting current. M_{XV} transistors are sized half that of M_{XS} and are driven with an inverted signal. They provide or remove channel charge to the M_{XS} transistor which would otherwise come from the current source and corrupt the DAC output current. With a 1.2 V power supply, 300 mV is partitioned for M_X drain-source voltage, and 150 mV each is partitioned for M_{XC} and M_{XS} drain-source voltages. Drain voltages of an offline PMOS/NMOS current source cell can be externally monitored to ensure correct biasing conditions.

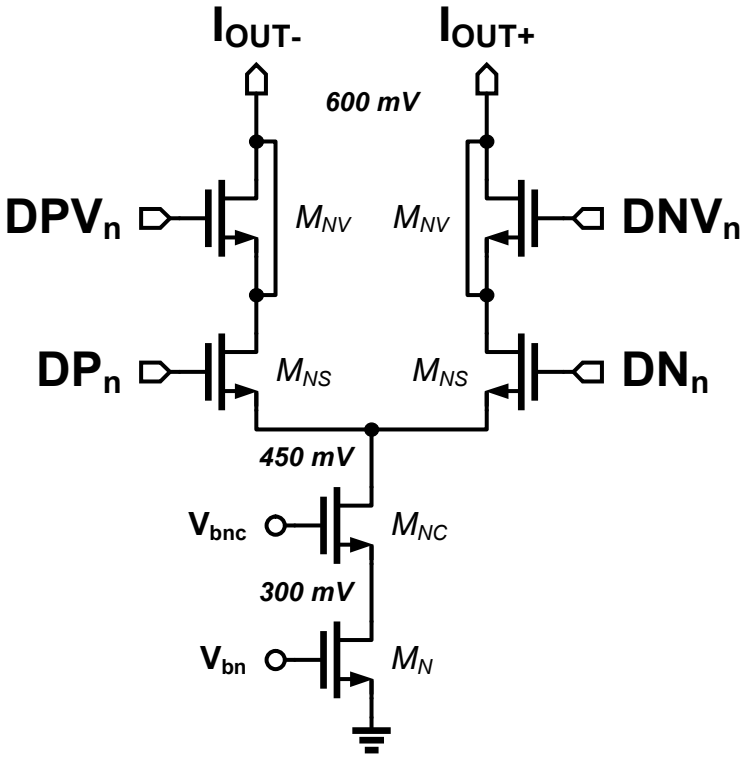


Figure 6.16: NMOS current steering DAC.

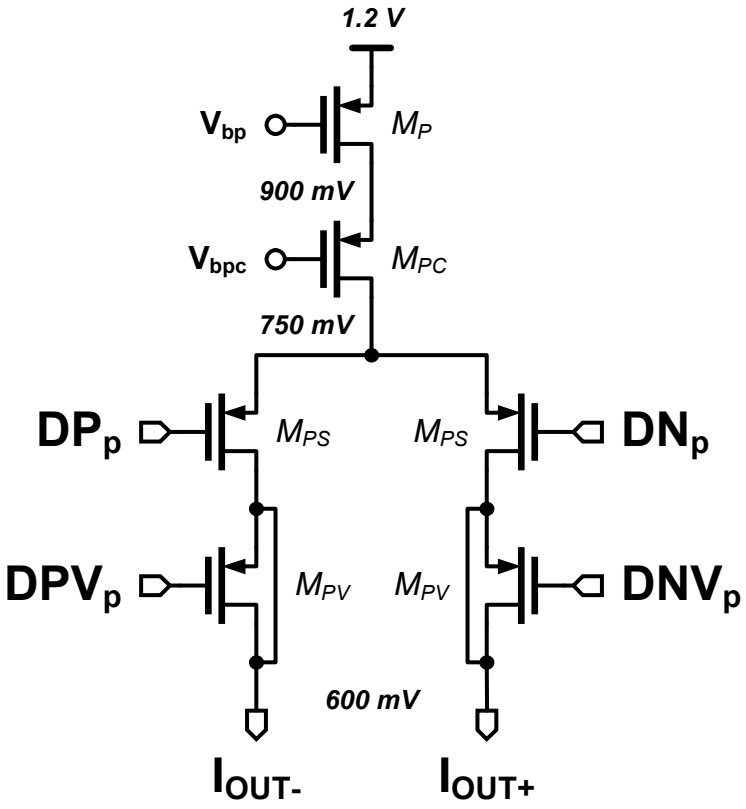


Figure 6.17: PMOS current steering DAC.

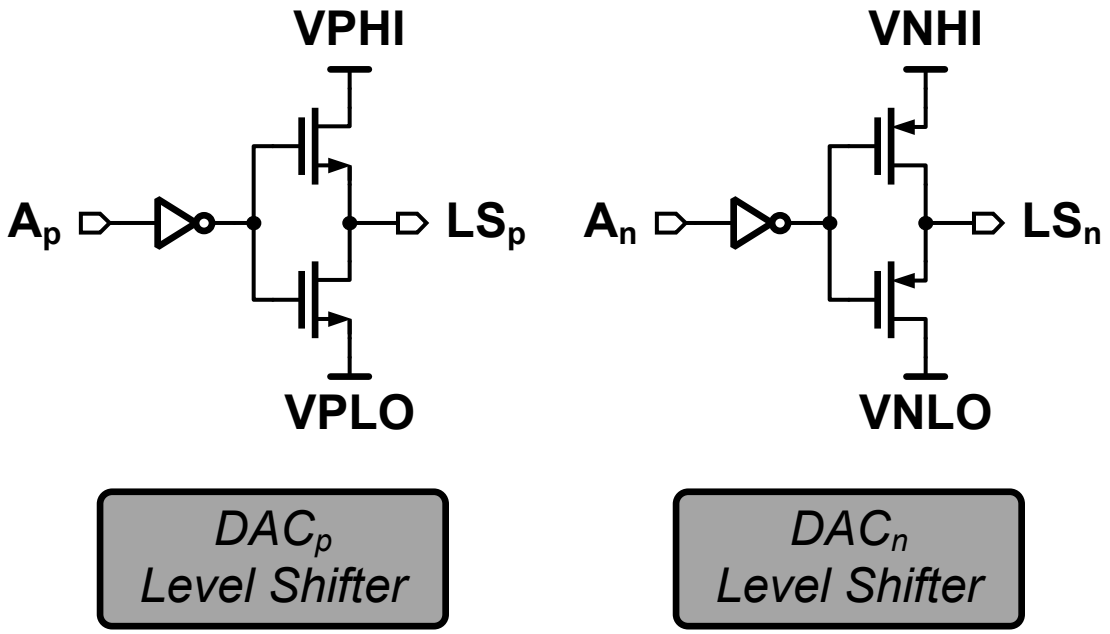


Figure 6.18: Level shifting low-swing buffer for PMOS and NMOS current steering DAC cells.

Figure 6.18 shows the circuit diagram for the level shifting low-swing buffers for both the PMOS and NMOS current steering DAC cells. The DAC_p level shifter follows a standard CMOS inverter with an NMOS pull up/down network. The pull-down NMOS transistor can rapidly discharge LS_p to $VPLO$ through saturation region operation. However the pull-up NMOS transistor can only slowly charge LS_p to $VPHI$ through its sub-threshold operation. The DAC_n level shifter has complimentary operation. It can rapidly charge LS_n to $VNHI$, but only slowly discharge to $VNLO$. This skewed crossover point causes both current source switches to conduct at the same time which ensures minimal current source transistor drain voltage perturbation.

DAC matching performance is ensured through careful layout practices including a power supply metal bus tree structure to mitigate systematic mismatch.

Random mismatch is minimized through increased transistor area [67]. No other mismatch mitigating techniques were used. At process nodes below 130 nm, transistor gate current can no longer be assumed to be zero. In fact, the $DAC1FD$ NMOS current source transistor has 93.75 μA drain current and ¿1 μA gate current under typical conditions! Current source transistor sizes for each DAC are shown in Table 6.2.

Table 6.2: DAC Current Source Transistor Dimensions

Transistor	Width [μm]	Length [μm]	Fingers
DAC1FD P	20.5	5	4
DAC1FD N	17.0	10.22	2
DAC2FD P	4.6	1.8	2
DAC2FD N	3.95	3.7	1
DAC2HD P	7.7	2.9	4
DAC2HD N	6.4	5.8	2

6.3.3 Active-RC Integrator and Flash ADC

An active-RC based integrator provides a low impedance summation node for source-switched charge pumps, linear transconductors, feedback DACs, and the feed forward input signal. A schematic of the integrators with 5 bit capacitive tuning is shown in Fig. 6.19. Resistor R_3 is 1200 ohms and capacitor C_3 is nominally 546 fF. Capacitor tuning can account for ±45% time constant variation and is adjusted manually.

The operational transconductance amplifier is constructed as a two stage amplifier and operates from a 1.2 V supply. The first stage is an fully differential

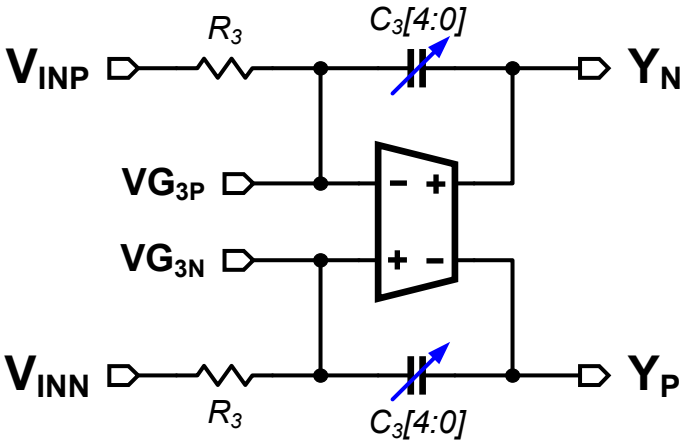


Figure 6.19: Active-RC integrator with 5 bit capacitor tuning.

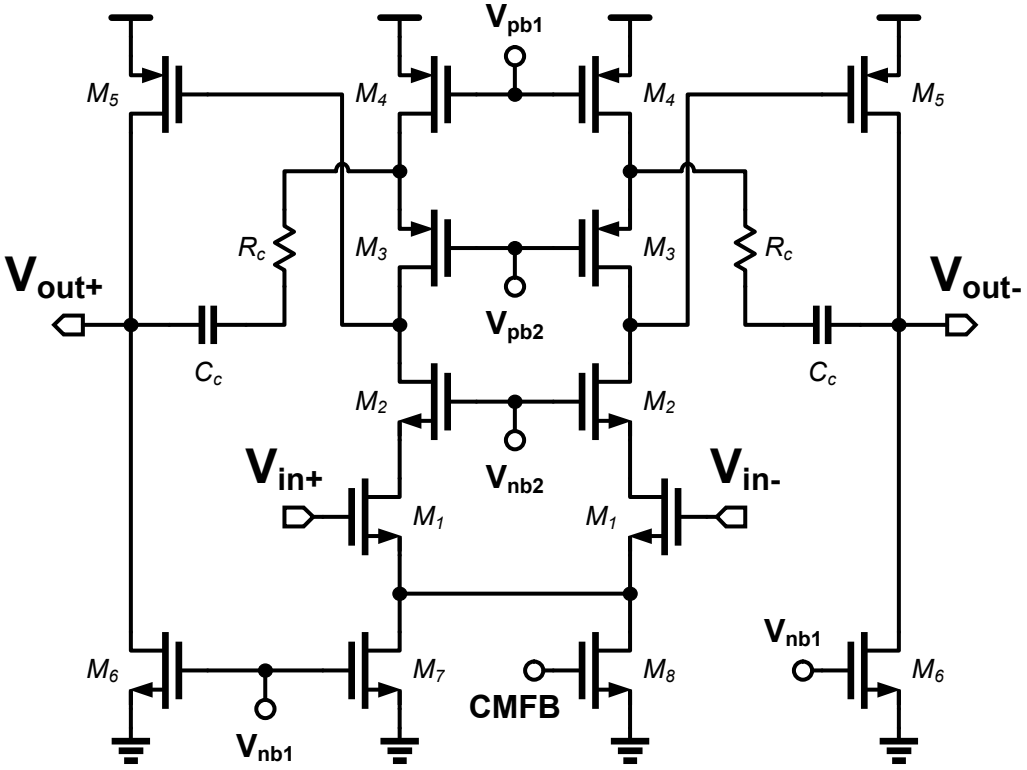


Figure 6.20: Two stage, cascode compensated operational transconductance amplifier with telescopic cascode first stage and common source second stage.

NMOS telescopic cascode amplifier. The second stage is a PMOS common source amplifier. Common mode is sensed with high impedance resistors and fed back to the first stage tail current source, M_8. Cascode compensation ensures amplifier stability [68]. All transistor except cascode transistors have length equal to 130 nm to improve their intrinsic gain while minimizing stray capacitance for high speed operation [69]. Cascode transistors have length equal to 100 nm. Post extraction simulations show 55 dB gain, ¿2.8 GHz unity gain bandwidth, and 55 degrees phase margin. The total power consumption is 6 mW.

The 16 element flash ADC is composed of a bidirectional voltage reference generating resistor string, differential preamplifier with reference subtraction, and sense-amplifier based latch. The full scale input range is 1.2 Vp-p differential resulting in an LSB size of 75 mVp-p. Monte Carlo transient simulations ensured monotonicity with input referred offset being ¡12 mVp-p 1-sigma. Sense-amplifier based latches minimized propagation delay and facilitate high speed operation.

6.4 Simulation Results

A prototype PLL-Based Delta-Sigma Modulator was designed and submitted for fabrication in TSMC 65 nm GP CMOS with 9 metal layers. A layout plot is shown in Fig. 6.21 and occupies an active area of 0.49 mm^2. Prototype dies are due to be packaged in 88 lead QFN packages with 10x10 mm body size and 0.4 mm pin pitch. An electrical package model and bond wire model are included in top level circuit simulations.

Figure 6.22 plots the 4096 point Analog FastSPICE transient noise simulation result of the C+CC extracted PLL-Based Delta-Sigma Modulator with package and bond wire models. Normalized power spectral density is plotted in blue,

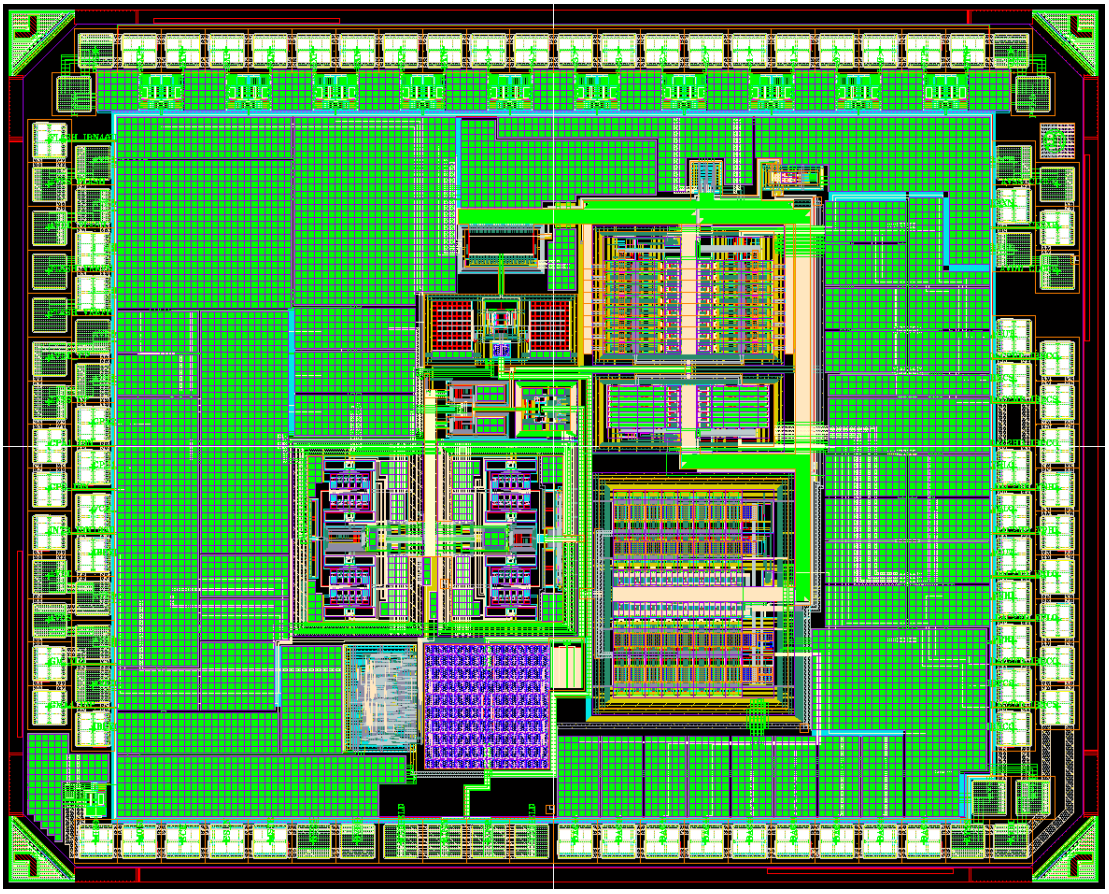


Figure 6.21: Image of oscillator-based delta-sigma modulator top-level layout with $0.49\,\mathrm{mm}^2$ active area.

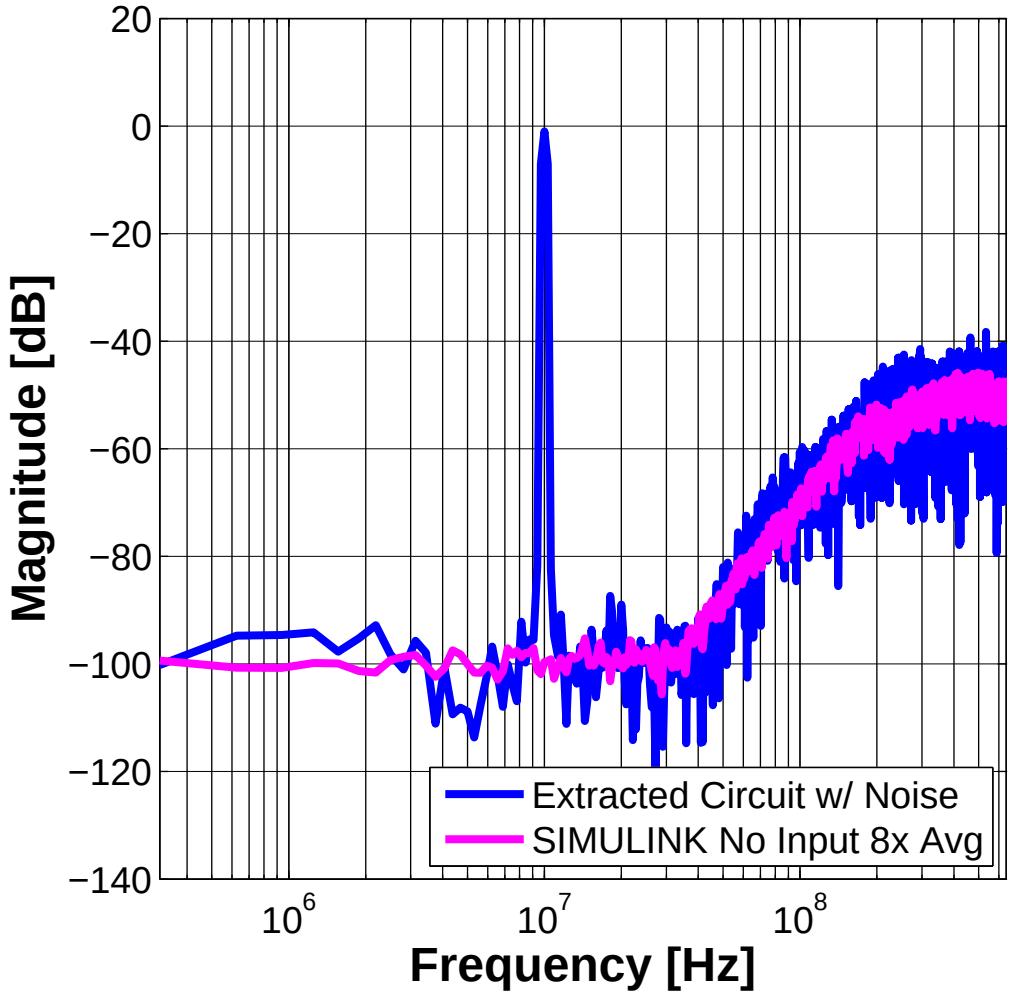


Figure 6.22: Circuit simulation PSD with C+CC extracted top-level, transient noise, and package/bond wire model. An 8x average SIMULINK model PSD demonstrates model versus circuit simulation congruency.

Table 6.3: Simulated Performance Summary

Sampling Frequency	1.28 GHz
Bandwidth	40 MHz
Full Scale Input	2.4 $V_{p-p,diff}$
SNDR	76.8 dB
SFDR	86.3 dB
Power	43 mW
Supply Voltage	1.2/1.5 V (A) 1.0 V (D)
FOMW [70]	95 fJ/conv-step
FOMS [70]	166.5 dB
Process	TSMC 65 nm GP 1P9M CMOS
Active Area	0.49 mm^2

and an 8 times averaged PSD from the SIMULINK model with zero input is plotted in magenta for comparison purposes. A -1 dB FS, 10 MHz sinusoidal tone is applied as the circuit simulation input, while no input is applied to the SIMULINK model. Good agreement between circuit simulation and SIMULINK model simulation is observed for low frequency thermal noise and high frequency quantization noise. Note that DAC mismatch was neither applied to the circuit simulation nor SIMULINK model simulation. Small spurs are observed in the circuit simulation spectrum at around 18-20 MHz and are attributed to supply noise sensitivity in the oscillator-based integrators. These tones are absent when the package and bond wire models are not included in the circuit simulation. Transistor level circuit simulation results are tabulated in Table 6.3.

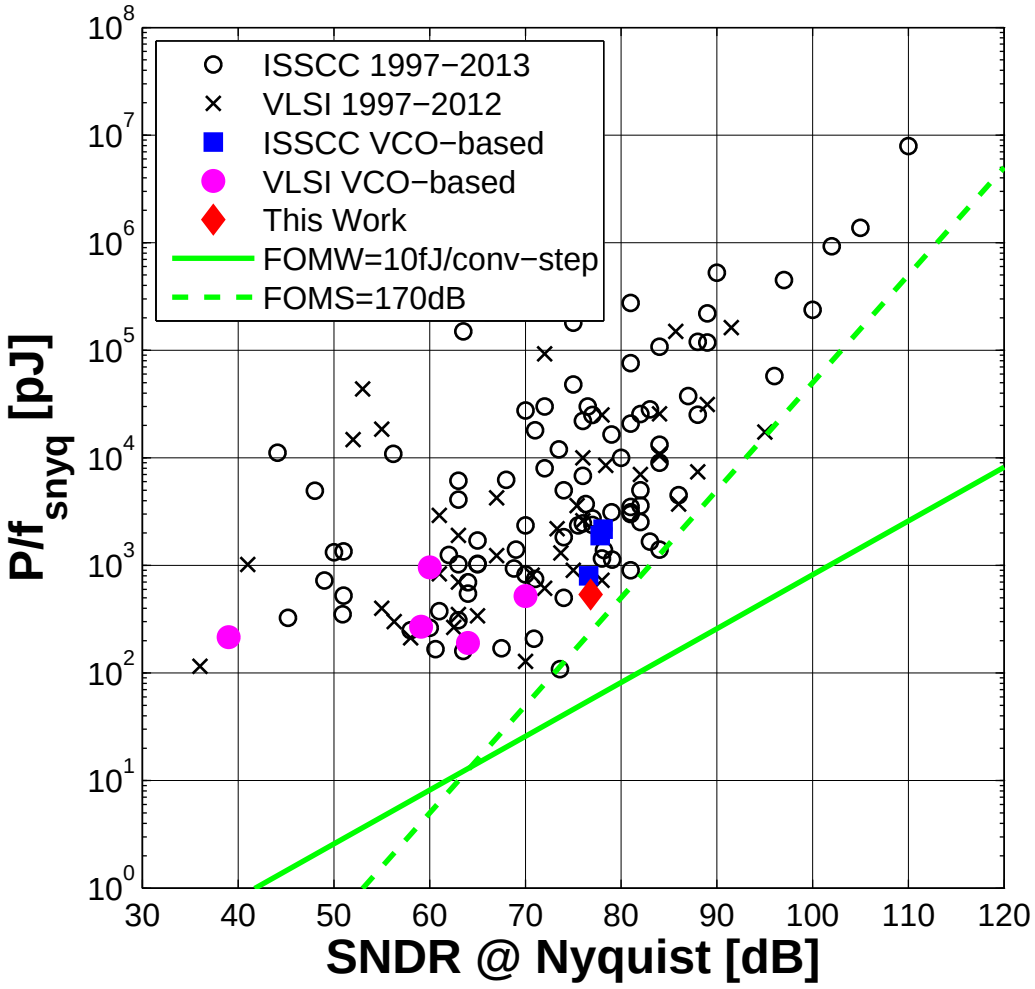


Figure 6.23: Plot of Energy versus SNDR for delta-sigma modulator, highlighting VCO-Based ADCs.

Figure 6.23 plots energy versus SNDR for comparison purposes. It consolidates performance metric data for delta-sigma modulators published at ISSCC from 1997 to 2013 and at VLSI Circuits Symposium from 1997 to 2012. Eight published VCO-based designs are highlighted for comparison. Also shown in this plot is a data point for the proposed PLL-Based Delta-Sigma Modulator. Its estimated performance compares favorably with state of the art VCO-based ADCs.

6.5 Summary

This chapter has covered the circuit design of the PLL-Based Delta-Sigma Modulator. Top level circuit architecture was detailed in Fig. 6.1. Discussion of oscillator circuit linearization techniques then followed. Due to a delay in acquiring prototype samples, top level C+CC extracted circuit level simulation results were provided. These simulations show the competitiveness of the PLL-Based Delta-Sigma Modulator when compared against state of the art VCO-based ADCs.

CHAPTER 7. CONCLUSION

Consumer demand and engineer curiosity have been major catalysts in process node scaling. CMOS transistors with their low power operation and high density integration have supplanted other transistor varieties. The orders of magnitude improvement in computing power that have occurred in nearly a century which can be largely attributed to CMOS process scaling is remarkable. While process scaling has had a significant positive impact on digital circuits, it has affected analog circuit negatively with reduced supply voltage and transistor gain.

This work has sought to further develop time-based signal processing techniques in order to compensate for the detrimental effects that process scaling into nanometer scale CMOS has had on analog circuits. By transforming the signal space into the time domain, supply voltage is no long the limiting factor in signal power. Also, the use of time domain VCO-based integrators can mitigate low intrinsic transistor gain because of its ideal phase domain integration ability.

Two prototype circuits have been developed to demonstrate time-base noise-shaping techniques. The first circuit is a time-to-digital converter with second order quantization noise-shaping. The aptly named Phase-Reference Continuous-Time Delta-Sigma (PR-CT$\Delta\Sigma$) TDC uses a digital-to-phase converter (DPC) circuit to close the feedback loop. This allows supply voltage independent, time domain signal processing. A switched-resistor interface circuit joins the time domain block to a voltage domain integrator. The circuit has potential for sub-picosecond resolution using high quality references.

The second circuit is an oversampling and noise-shaping analog-to-digital

converter which uses time domain oscillator-based integrators. This third order PLL-Based Delta-Sigma Modulator uses common phase-locked loop circuit blocks, such as phase detectors, charge pumps, and voltage-controlled oscillators, together with traditional delta-sigma modulator building blocks to create a low power, high resolution, and wide bandwidth ADC. Both architecture and circuit techniques are used to overcome the limitations of oscillator-based integrators. The PLL-Based Delta-Sigma Modulator demonstrates further advancement of time-based signal processing techniques in analog-to-digital converters.

7.1 Future Work

The PR-CT$\Delta\Sigma$ TDC resolution was partially limited by a single-bit quantizer and feedback DPC. The primary reason for not pursuing a multi-bit implementation is nonlinear phase spacing in a multi-bit DPC. However, it may be possible to create a multiple input delay line where the input point is selected through an algorithm designed to shape phase spacing errors. Inclusion of oscillator-based integrators could produce a completely time domain TDC.

Another possible idea with regard to the PLL-Based Delta-Sigma Modulator would be to replace the final active-RC integrator and flash ADC with a VCO Integrator and phase quantizer. A voltage-controlled delay line following a single phase VCO could provide multiple phase outputs for the phase quantizer and allow the addition of a fast path around the VCO to compensate for its high impedance control input. The additional static delay of the delay line would add to loop delay and complicate stability. Creative partitioning of feedback delay or the addition of a digital fast feedback around the quantizer could mitigate delay.

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