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Tawfiq Musah for the degree of Doctor of Philosophy in

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Title:

Low Power Design Techniques for Analog-to-Digital Converters in Submicron CMOS

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Abstract approved: _____

Un-Ku Moon

Advances in process technologies have led to the development of low-power high speed digital signal processing blocks that occupy small areas. These advances are critical in the development of portable electronic devices with small feature size and long battery life. However, the design of analog and mixed-signal building blocks, especially analog-to-digital converters (ADCs), becomes complex and power-inefficient with each advance in process node. This is because of decreased headroom and low intrinsic gain.

In this thesis, circuit techniques that enable the design of low-complexity power-efficient ADCs in submicron CMOS are introduced. The techniques include improved correlated level shifting that allow the use of simple low gain amplifiers to realize high performance pipelined and delta-sigma ADCs. Also included is an investigation of the possibility of replacing the power-hungry amplifier in integrators, used in delta-sigma modulators, with low power zero-crossing-based ones. Simulation results of a correlated level shifting pipelined ADC and measure-

ment results of a fabricated prototype of a zero-crossing-based delta-sigma ADC are employed to discuss the effectiveness of the techniques in achieving compact low-power designs.

Low Power Design Techniques for Analog-to-Digital Converters in Submicron CMOS

by

Tawfiq Musah

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September 15, 2010

APPROVED:

Major Professor, representing Electrical and Computer Engineering

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Director of the School of Electrical Engineering and Computer Science

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Dean of the Graduate School

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Tawfiq Musah, Author

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CHAPTER 1. INTRODUCTION

1.1 Motivation

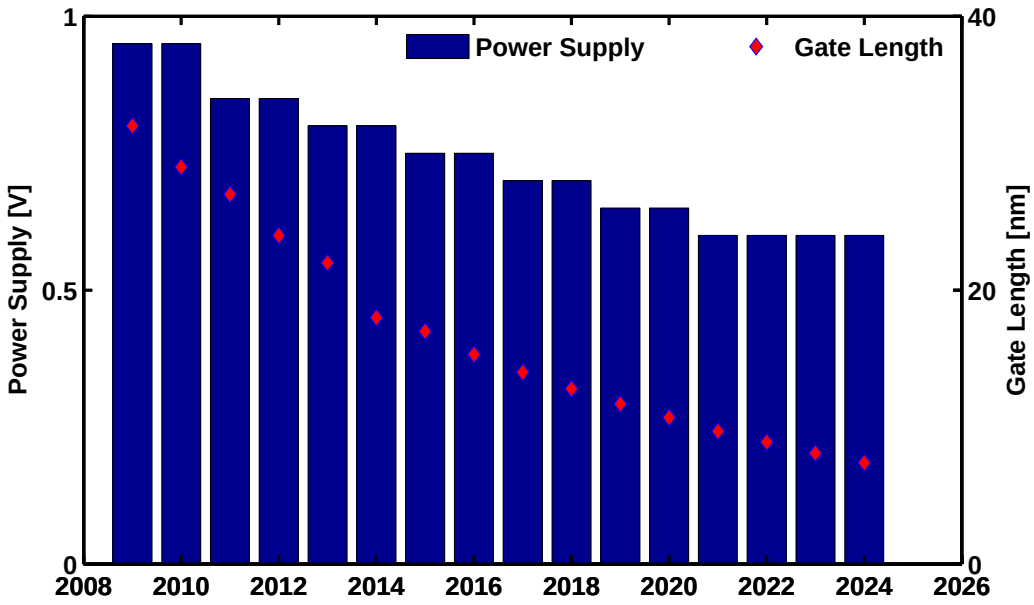

Figure 1.1: 2009 International Technology Roadmap for Semiconductors.

In 1965, Gordon Moore predicted that the number of transistors that can be placed in an integrated circuit will increase at a rate of roughly a factor of two

per year [1]. Ten years later, he modified his prediction to forecast doubling of the number of transistors every two years. This prediction became more of a guideline for driving the cost of electronics down [2] and the semiconductor industry has been adhering to it since. To achieve the steep increase in density, the dimensions of the transistor have to be scaled down accordingly. This has to accompanied with a reduction in supply voltages to reduce the stress on the transistors and improve reliability. The 2009 International Technology Roadmap for Semiconductors [3] forecast of the transistor gate length and corresponding power supply is shown in Fig. 1.1. It predicts that the supply voltage for low operating power processes will decrease to 0.6V with a gate length of about 10nm by 2021 .

While this decrease in size and lower supply voltage lead to faster and lower power digital circuit blocks, their analog counterparts do not see the same benefits [4]. This is because the decrease in supply voltages results in limited signal swing and for that matter signal-to-noise ratio. Moreover, the intrinsic gain as well as transistor matching, decreases with each technology scaling . As a result complex design techniques have to be employed to design high performance analog and mixed-signal circuits in advanced processes.

To design low power analog-to-digital (ADC) circuits in submicron CMOS, the goal is to be able to achieve high performance while using simple building blocks. The most power-consuming building block in switched-capacitor ADC circuits is the amplifier. High performance ADCs require amplifiers with high DC gain and bandwidth, which are difficult to achieve in submicron processes without sacrificing power efficiency. There have been several techniques proposed to realize high effective amplifier gain using low gain amplifier circuits, but their susceptibility to noise makes them unattractive for high performance ADCs.

1.2 Contribution

This work is aimed at developing design techniques that realize low power switch-capacitor circuits without increasing noise. The techniques include:

a) An improved Correlated Level Shifting (CLS) technique that allows the use of low gain single stage amplifiers to realize very high effective loop gain.

b) A CLS integrator that needs only two phases for its operation and offers the possibility of removing the phase error of the integrator.

c) A zero-crossing-based integrator that has the promise of becoming a low power alternative to traditional amplifiers, especially in deep submicron processes.

1.3 Organization

The rest of this thesis is organized as follows. Chapter 2 discusses the effect finite amplifier DC gain has on major switched-capacitor building blocks and how these effects limit the performance of several ADC structures. Chapter 3 surveys past techniques and proposes new ones to achieve gain enhancement in switched-capacitor building blocks. The design of a pipelined ADC using the improved CLS technique and a low phase error CLS integrator are presented in Chapters 4 and 5 respectively. The design of a zero-crossing based delta-sigma ADC is explored in Chapter 6. A summary of the research accomplishments concludes the thesis as Chapter 7.

CHAPTER 2. AMPLIFIERS IN SWITCHED-CAPACITOR ANALOG-TO-DIGITAL CONVERTERS

2.1 Effect of Finite Amplifier Gain

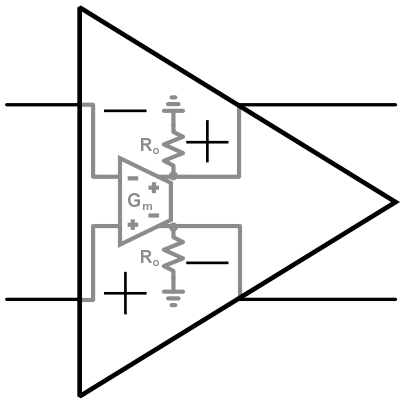

Figure 2.1: Representation of operational transconductance amplifier

Switched-capacitor circuits are notable for their insensitivity to absolute capacitor values. The simplest realization of the circuits involve a set of capacitors that are charged to a particular voltage, then the charge is transferred to another set of capacitors. Gain or attenuation is achieved by appropriately sizing the two sets of capacitors. For accurate charge transfer, an operational amplifier is used to force a virtual ground. For switched-capacitor stages, the amplifier is required to have high input and output impedance, hence an operational transconductance amplifier (OTA) is used. The accuracy of the virtual ground limits the accuracy

of the charge transfer since capacitor matching is high enough, especially in submicron processes. For the purposes of this thesis, the OTA will be represented by the symbol shown in Fig. 2.1, and will be assumed to have infinite bandwidth.

2.1.1 Sample-and-Hold

A sample-and-hold (SAH) circuit is commonly used as a front-end of switched-capacitor ADCs. It relaxes the design requirement of the stages immediately succeeding it. However, the accuracy of the SAH limits the accuracy of the ADC. A flip-around SAH is shown in Fig. 2.2. It consists of clocked switches, capacitors and an amplifier. The two phase clock signals ϕ_1 and ϕ_2 are realized as non-overlapping phases. The input signal V_S is sampled on the C_f capacitors at the end of ϕ_1. During ϕ_2, the capacitors are flipped-around to feedback around the amplifier. The next stage samples the output at the end of ϕ_2. If the amplifier is ideal, the capacitors maintain the charge sampled on them during ϕ_1, yielding an output voltage equal to the input. However, if the amplifier has a finite DC gain, A, the differential output voltage becomes

$$V_O = \Big[\frac{A}{1+A}\Big]V_S = \Big[1 - \frac{1}{1+A}\Big]V_S. \tag{2.1}$$

For high dynamic range, the amplifier gain error and its nonlinearity has to be lower than the accuracy of the ADC. Another significant design problem of the SAH is the noise requirement. The noise from the sampling switches and the amplifier has to be below the quantization noise of the ADC. This requirement makes the SAH the most power consuming block in an ADC.

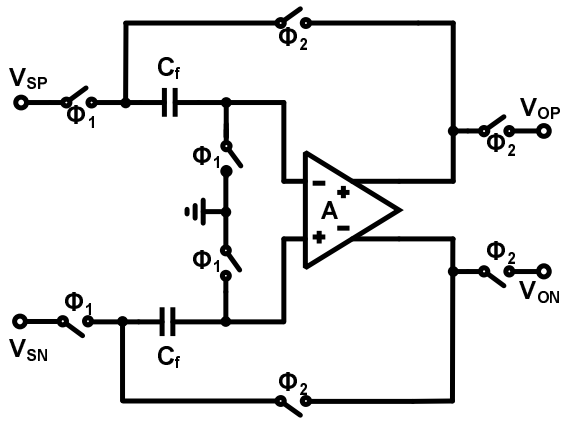

Figure 2.2: Flip-around sample-and-hold

2.1.2 Multiplying Digital-to-Analog Converter

The multiplying digital-to-analog converter (MDAC) is a switched-capacitor block that acts as a digital-to-analog converter (DAC), a subtractor and a gain stage. The MDAC is most commonly used in residue-generating ADC structures, including sub-ranging, pipelined and algorithmic ADCs. A flip-around realization of an MDAC is shown in Fig. 2.3. As in the case of the SAH, the input signal is sampled on the capacitors at the end of ϕ_1. One terminal of each capacitor is connected to the input of the amplifier. The other terminal of the feedback capacitor C_f is connected to the output of the MDAC while that of C_s is connected to the DAC references during ϕ_2. At the end of ϕ_2, the output of the MDAC, assuming an ideal amplifier, can be expressed as

$$V_{Oideal} = \frac{C_s + C_f}{C_f} V_S - \frac{C_s}{C_f} D V_R. \tag{2.2}$$

Incorporating the finite amplifier gain results in an MDAC output that is less than the ideal output, and can be expressed as

$$V_O = \Big[\frac{A\beta}{1+A\beta}\Big]V_{Oideal} = \Big[1 - \frac{1}{1+A\beta}\Big]V_{Oideal}. \tag{2.3}$$

where β is $\frac{C_f}{C_s+C_f}$ and represents the feedback factor of the MDAC. The output error is inversely proportional to the loop gain of the MDAC, and has to be low enough to meet the accuracy requirement of the next MDAC stage.

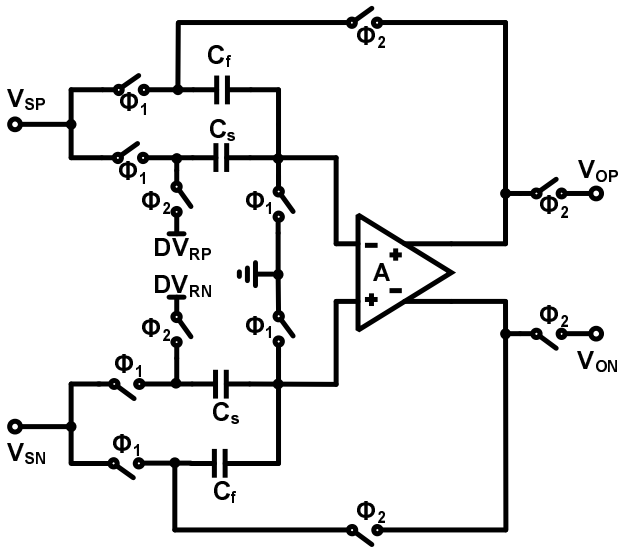

Figure 2.3: Flip-around multiplying digital-to-analog converter

2.1.3 Integrator

The integrator is used in switched-capacitor blocks with memory, like filters. It is commonly used in the loop filter of delta-sigma modulators. Fig. 2.4 shows the schematic of a switched-capacitor integrator where the same capacitor is used for both the input sampling and the DAC references. The input signal is sampled on C_s at the end of ϕ_1. The charge on C_s is then transferred to the integrating

capacitor C_f during ϕ_2. At the end of the charge transfer, the output of the integrator, assuming ideal amplifier, can be expressed as

$$V_O = \frac{C_s}{C_f}\frac{z^{-1}}{1-z^{-1}}[V_S - DV_R]. \tag{2.4}$$

The finite amplifier gain adds a magnitude and phase error to the integrator output, yielding

$$V_O = \frac{C_s}{C_f}\Big[1 - \frac{1}{1+A\beta}\Big]\frac{z^{-1}}{1-[1-\frac{1-\beta}{1+A\beta}]z^{-1}}[V_S - DV_R]. \tag{2.5}$$

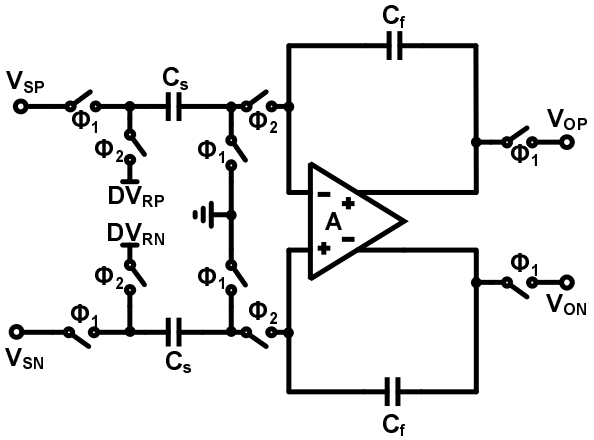

Figure 2.4: Integrator with shared input and DAC capacitor

The phase error determines the low frequency magnitude of the integrator transfer function. Ideally, the integrator transfer function approaches infinity at DC. This property makes the integrator the block of choice for applications where suppression of slow moving signals is desired. In such applications, the lower the phase error, the better the low frequency suppression.

2.2 ADC Architectures

Amplifier finite gain deteriorates the performance of switched-capacitor circuits, and for that matter switched-capacitor ADC. While high amplifier gain is desirable, it comes with the cost of high power consumption. Understanding how finite amplifier gain error affects an ADC performance could therefore be helpful in defining the minimum gain required for a given accuracy.

2.2.1 Flash ADC

The flash is the simplest analog to digital converter structure. In this ADC, an input signal is connected to a set of comparators. Each comparator is also connected to a different threshold voltage. For the flash ADC in Fig. 2.5, the threshold voltages are determined by a resistor string. The outputs of the comparators give a digital representation of the analog input signal.

The comparator thresholds are designed such that the outputs of the comparator give a thermometer code representation of the signal. For the three-comparator flash ADC of Fig. 2.5, the threshold voltages are ($\frac{-V_{REF}}{2}$,0,$\frac{V_{REF}}{2}$). The possible set of comparator outputs are 000, 001,011 and 111 depending on the region the input voltage falls. This output can then be decoded to a 2-bit word representation of the input signal. The ADC digital output can be written as

$$D_{out} \cdot V_{REF} = V_{IN} + \frac{V_{REF}}{2^2}. \tag{2.6}$$

The second term on the right-hand side of Eq. (2.6) is the quantization error of the 2-bit flash. For higher resolution, the number of bits used to represent the signal has to be increased. This results in lower quantization error. For an N-bit

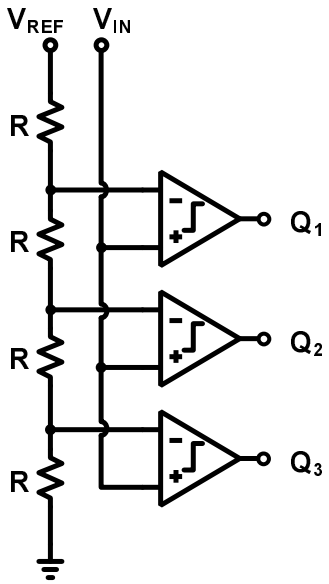

Figure 2.5: 2-bit flash ADC

flash, the digital output becomes

$$D_{OUT} \cdot V_{REF} = V_{IN} + \frac{V_{REF}}{2^N}. \tag{2.7}$$

While the quantization error is significantly reduced with higher number of bits, the number of comparators required to digitize the input signal increases exponentially. For instance, a 3-bit flash requires 7 comparators while a 4-bit one requires 15 comparators. The number of comparators required for an N-bit flash ADC is 2^N-1. The large number of comparators required for higher resolution flash ADCs makes them power- and area-inefficient. However, they can operate at very high conversion speeds since all the comparators are strobed at the same time. For high resolution, other ADC architectures are used.

2.2.2 Two-step ADC

A more power- and area-efficient way of increasing the resolution of flash ADC, is to break the conversion into two separate steps. The number of bits resolved in each step is low so the number of comparator used is small. A block diagram of a two-step ADC is shown in Fig. 2.6, where delays are omitted for clarity. The input signal is fed to the first flash ADC, which digitizes it with quantization error E_1. This error is extracted by and MDAC and is digitized by the flash ADC with an error E_2. The final output of the two-step ADC is obtained by summing the weighted digital outputs of the two flash ADCs. For the ADC of

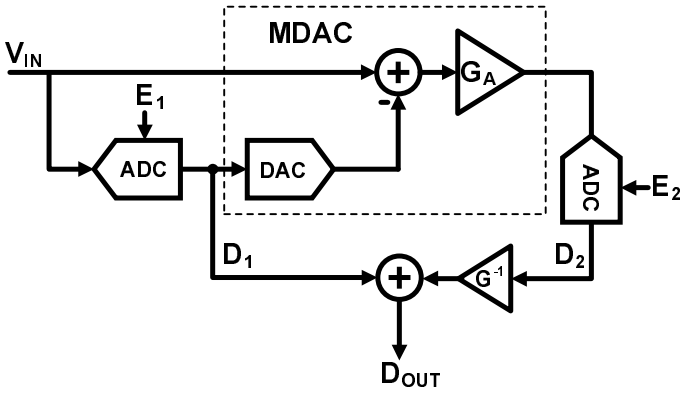

Figure 2.6: Two-step ADC

Fig. 2.6, the digital out is

$$D_{OUT} \cdot V_{REF} = D_1 + \frac{D_2}{G}. \tag{2.8}$$

$$D_{OUT} \cdot V_{REF} = V_{IN} + E_1 + \frac{1}{G}(-G_A E_1 + E_2). \tag{2.9}$$

$$D_{OUT} \cdot V_{REF} = V_{IN} + \left(1 - \frac{G_A}{G}\right) E_1 + \frac{1}{G} E_2. \tag{2.10}$$

If the closed loop gain of the MDAC (G_A) matches the digital gain (G), the quantization error from the first stage of the ADC is completely canceled. The

remaining noise will be solely from the quantization error of the second stage, which is suppressed by the interstage gain. While it is easy to realize accurate digital gain, accurate analog gain is difficult to achieve due to finite amplifier gain. Using the MDAC gain expression derived from Eq. (2.3) and Eq. (2.10), the ADC output can be rewritten as

$$D_{OUT} \cdot V_{REF} = V_{IN} + \frac{E_1}{1 + A\beta} + \frac{1}{G} E_2. \tag{2.11}$$

$$D_{OUT} \cdot V_{REF1} = V_{IN} + \frac{1}{1 + A\beta} \frac{V_{REF1}}{2^{N1}} + \frac{1}{G} \frac{V_{REF2}}{V_{REF1} 2^{N2}}. \tag{2.12}$$

Equation (2.12) defines the amplifier gain requirement for a two-step ADC with a resolution of N_1+N_2 bits. The matching between the references for the two stages could pose a problem since any mismatch will add to the gain error in the second term on the RHS of Eq. (2.12). To avoid this matching constraint, the MDAC could be designed such that G_A=2^{N1}. This allows the use of the same reference voltage for two subADCs. For example, a two-step ADC with a 4-bit flash subADC will require an MDAC gain of 16 to use the same reference in both stages.

2.2.3 Pipelined ADC

The pipelined ADC is a multiple stage extension of the two-step ADC. It has several stages that resolve only a few bits each. The sampling speed of the ADC is limited by the speed of just one stage, making the throughput of pipelined ADC very high. The latency associated with the pipelined conversion is not a problem in most applications, so a large number of stages could be used. Moreover, the small number of bits per stage results in an ADC with small area and low power operation. A block diagram of an n-stage pipelined ADC is shown in Fig. 2.7. It consists of n-1 MDAC stages with a flash subADC at the end.

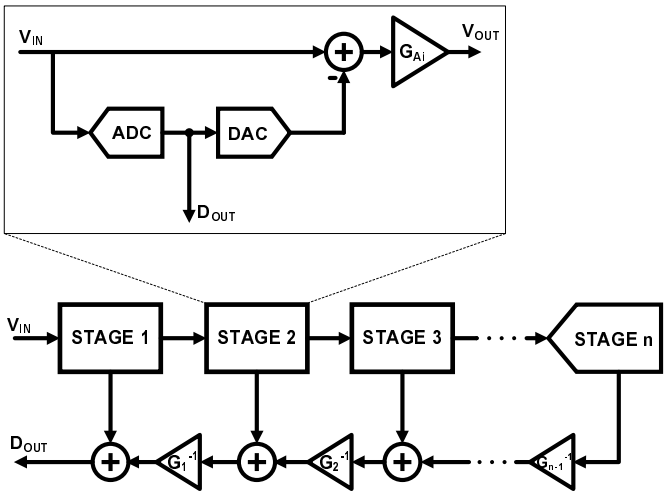

Figure 2.7: Pipelined ADC

The digital output of the ADC is the weighted sum of all the outputs of the subADCs after taking care of the latency. The output can be written as

$$D_{OUT} \cdot V_{REF} = D_1 + \frac{D_2}{G_1} + \frac{D_3}{G_1 G_2} + \frac{D_n}{G_1 G_2 G_3 ... G_n}. \tag{2.13}$$

$$D_{OUT} \cdot V_{REF} = V_{IN} + \left(1 - \frac{G_{A1}}{G_1}\right) E_1 + \left(1 - \frac{G_{A2}}{G_2}\right) E_2 + ... + \frac{1}{G_1 G_2 G_3 ... G_{n-1}} E_n. \tag{2.14}$$

If $G_{Ai} = G_i$, the ADC output reduces to

$$D_{OUT} \cdot V_{REF} = V_{IN} + \frac{1}{G_1 G_2 G_3 ... G_{n-1}} E_n = V_{IN} + \frac{1}{G_1 G_2 G_3 ... G_{n-1}} \frac{V_{REF}}{2^{Nn}}. \tag{2.15}$$

Equation (2.15) indicates that the accuracy of the pipelined ADC depends on the resolution of the back-end flash ADC and the product of the gains of the stages. Finite amplifier gain causes the quantization noise of the earlier stages to leak through to the output. The digital output of the pipelined ADC with a non-ideal amplifier gain is

$$D_{OUT} \cdot V_{REF} = V_{IN} + \frac{1}{(1 + A\beta)_1} E_1 + \frac{1}{G_1} \frac{1}{(1 + A\beta)_2} E_2 + ... + \frac{1}{G_1 G_2 ... G_{n-1}} E_n. \tag{2.16}$$

Equation (2.16) gives the effect each MDAC gain error has on the entire ADC performance. The loop gain requirement gets relaxed down the pipeline since the accuracy requirement tapers down the pipeline too. It might seem from the above expression that a straightforward way of reducing the loop gain requirement is to resolve more bits in the first stage. However, the higher the number of bits resolved, the higher the required MDAC gain, which implies lower feedback factor. Thus, the reduction in the loop gain requirement is offset by the reduction in feedback factor, leaving the amplifier gain requirement unchanged.

One important consideration in designing pipelined ADCs is the offset in the subADCs. If the subADC offset is too high, the residue voltage will exceed the range of the next subADC leading to lost information. If the MDAC gain is chosen to be 2^{M-1} instead of 2^M for an M-bit stage, the effect of the subADC offset and nonlinearity is reduced [5]. However, this reduces the effective number of bits per stage and hence requires more stages to resolve a given number of bits. The redundancy does not complicate the digital output summation or, as it popularly called, digital error correction.

The transfer curve of a 10-bit pipelined ADC is shown in Fig. 2.8. The pipeline has four stages resolving 2.5 effective bits each and a 2-bit flash in the back-end. The 2.5bit stage has six comparators in the subADC (7 levels) and an MDAC with a gain of 4. A 20-dB loop gain is used in the first MDAC while the remaining stages remain ideal. As is evident from the Fig. 2.8, the gain error causes vertical jumps in the ADC transfer curve when the input transitions from one region of the subADC to another. This will cause nonlinearities in the ADC spectrum and degrade signal to noise and distortion ratio (SNDR).

Another way of decreasing the quantization noise in a pipelined ADC is to oversample the input signal. The quantization noise of the pipelined ADC is spread

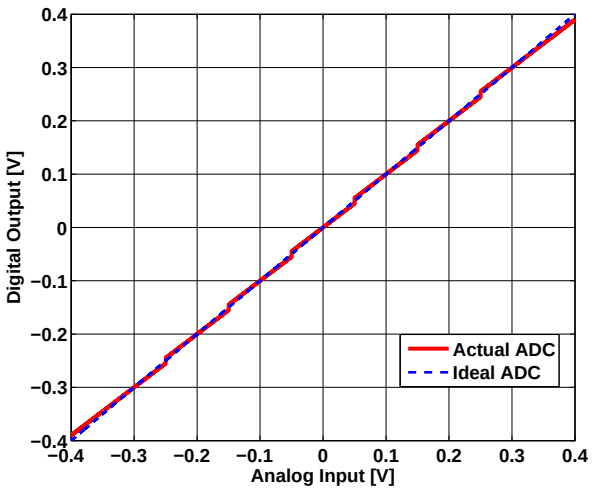

Figure 2.8: Effect of gain error in pipelined ADC linearity

evenly in the Nyquist band due to aliasing. If the signal bandwidth is less than Nyquist, the amount of quantization noise in the signal band is reduced. The signal to quantization noise ratio (SQNR) of the ADC increases by 3dB for every doubling of the oversampling ratio.

2.2.4 Delta-Sigma ADC

The delta-sigma ADC improves on the idea of oversampling to realize high accuracy ADCs. A loop filter is used to suppress the inband quantization noise of the delta-sigma modulator. While the oversampling and noise shaping are instrumental in the achieving high accuracy, the signal bandwidth is limited to a few MHz especially for resolutions beyond 12bits. The loop filter that determines the noise shaping could be either lowpass (quantization noise is high-pass filtered) or bandpass (quantization noise is notch filtered), and could be of any order.

The block diagram of a lowpass delta-sigma modulator is shown in Fig. 2.9. A 2nd order low-distortion topology [6] is used in this example. There are two full delay integrators in the loop, and parameters δ and α in their transfer functions are ideally unity.

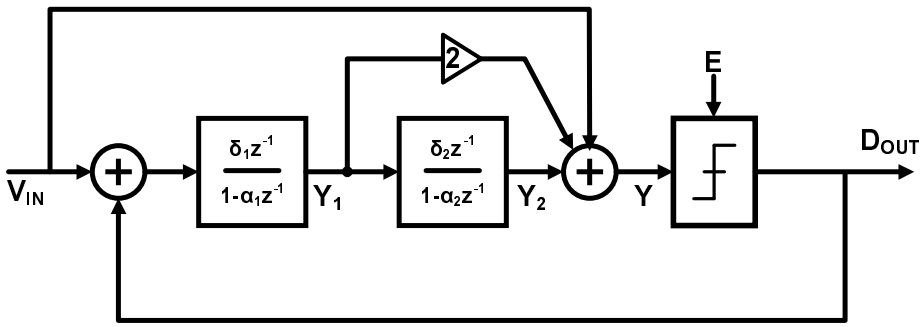

Figure 2.9: Delta-sigma ADC

The signal transfer function (STF) from V_{IN} to D_{OUT} and the noise transfer function (NTF) from E to D_{OUT} can be written as

$$STF = \frac{1 + 2I + I^2}{1 + 2I + I^2} = 1. \tag{2.17}$$

$$NTF = \frac{1}{1 + 2I + I^2} = \frac{(1 - \alpha z^{-1})^2}{1 - 2(\alpha - \delta)z^{-1} + (\alpha^2 - 2\alpha\delta + \delta^2)z^{-2}}. \tag{2.18}$$

where the integrator transfer functions are assumed to be identical and represented by I. If the magnitude and phase errors are zero, the NTF reduces to a 2nd order highpass filter with both of its zeroes at DC, as shown in Eq. (2.19)

$$NTF = (1 - z^{-1})^2. \tag{2.19}$$

However, in the presence of finite amplifier gain, the NTF becomes

$$NTF = \frac{\left[1 - \left(1 - \frac{1-\beta}{1+A\beta}\right)z^{-1}\right]^2}{\left[1 - \frac{\beta}{1+A\beta}z^{-1}\right]^2}. \tag{2.20}$$

This limits the low frequency attenuation of the loop and degrades inband quantization noise suppression. From Eq. (2.20), the magnitude of the NTF at DC can be derived as

$$NTF(z=1) = \frac{1}{[1+A]^2}. \tag{2.21}$$

For an amplifier with a 40-dB gain, the attenuation of the NTF at DC is 80-dB. This is illustrated in Fig. 2.10. For higher suppression, the amplifier gain has to be increased accordingly.

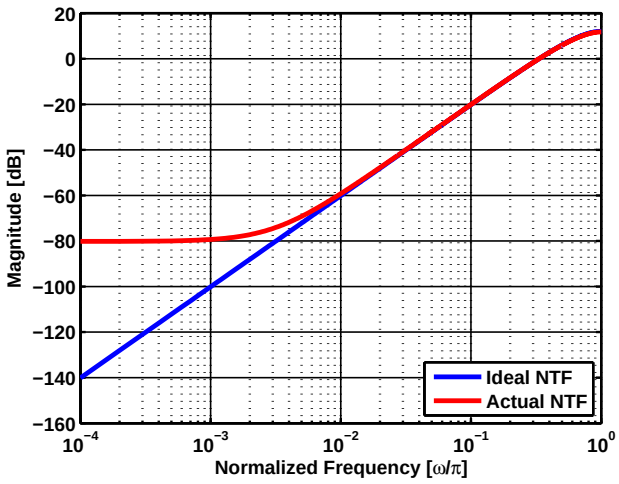

Figure 2.10: Effect of amplifier gain on noise shaping

An alternate way of achieving better inband suppression is increase the modulator order. For instance, a 3rd order modulator would achieve 120-dB attenuation at DC. However, increasing the modulator order degrades the stability of the modulator and decreases the maximum input signal that can be applied to the modulator. A more stable way of increasing the order of the noise shaping is to use cascaded or MASH modulators. Several low order modulators are pipelined to realize a delta-sigma modulator of a higher order. A block diagram of a two-stage MASH modulator is shown in Fig. 2.11. Each stage is made up of the feedforward

modulator of Fig. 2.9. The modulator has a unique property where the output of the second integrator is just a delayed version of the quantization noise.

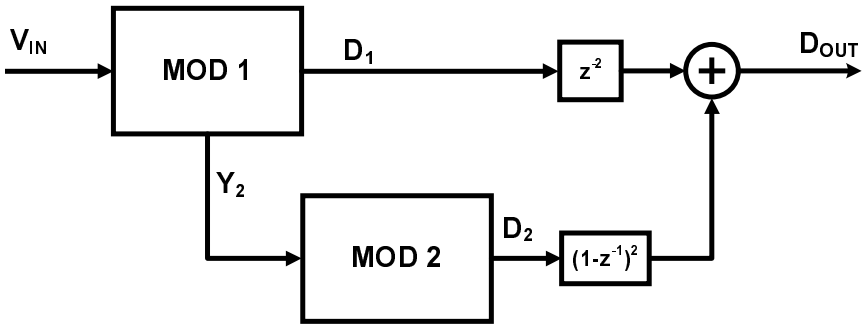

Figure 2.11: Two-stage MASH ADC

The final output of the MASH modulator assuming ideal amplifier gain is

$$D_{OUT} = z^{-2}D_1 + (1 - z^{-1})^2 D_2. \tag{2.22}$$

$$D_{OUT} = z^{-2}V_{IN} + z^{-2}(1 - z^{-1})^2 E_1 + (1 - z^{-1})^2[Y_2 + (1 - z^{-1})^2 E_2]. \tag{2.23}$$

Since $Y_2 = -z^{-2}E_1$, Eq. (2.23) simplifies to

$$D_{OUT} = z^{-2}V_{IN} + (1 - z^{-1})^4 E_2. \tag{2.24}$$

The cancelation of E_1 will not be prefect when the loop filter is not ideal. The maximum attenuation achieved in this situation is no better than Eq. (2.21) due to E_1 leakage. Thus, very high amplifier gain is required in MASH modulators. A possible low power solution is to modify the digital NTF such that it matches the analog NTF. This can be accomplished with an adaptive filter [7].

CHAPTER 3. LOW POWER GAIN-ENHANCEMENT TECHNIQUES

3.1 Introduction

The effect amplifier gain on the performance of ADCs was extensively explored in the previous chapter. While the gain requirement depends on the architecture and resolution of the ADC, the general trend is that high amplifier gain is needed for high accuracy conversion. There are several direct ways of designing high gain amplifiers, including cascading of several low gain stages, cascoding and active cascoding [8]. While these approaches increase gain, they also increase the power consumption and degrade the amplifier stability, necessitating complicated compensation techniques. There are numerous techniques proposed to enhance the effective amplifier gain without degrading stability or complicating the amplifier design. These techniques leverage properties of switched-capacitor circuits at the system level to simulate high effective amplifier gain.

The bandwidth of the amplifiers used in the circuits below are assumed to be infinite to simplify discussions. However, some of the techniques that may offer the same gain enhancement might have different effects on the closed loop bandwidth of the circuit, and should be taken into consideration when shopping for a gain enhancement technique. A summary of the gain enhancement achieved by each of the techniques presented below is tabulated in the Appendix.

3.2 Precise Op-amp Gain Technique

The closed loop gain of switched-capacitor gain stage is determined by the ratio of capacitors and the amplifier gain. The precise op-amp gain (POG) technique seeks to improve the accuracy of a gain stage by skewing the capacitor values to account for the loss due to amplifier gain [9, 10]. This requires that the op-amp gain to be known precisely. Consider the gain stage of Fig. 3.1. The gain stage, with a feedback factor $\beta = \frac{C_f}{C_s+C_f}$, has an ideal output voltage that was derived in the previous chapter to be

$$V_O = \frac{C_s + C_f}{C_f} V_S. \tag{3.1}$$

Incorporating the finite amplifier gain and the modified capacitor values gives

$$V_O = \frac{C_{sPOG} + C_{fPOG}}{C_{fPOG}} \Big[\frac{A\beta}{1 + A\beta}\Big] V_S. \tag{3.2}$$

Choosing $C_{fPOG} = C_f$ and $C_{sPOG} = C_s \frac{A\beta}{A\beta-1} + C_f \frac{1}{A\beta-1}$, ensures that Eq. (3.2) is always equal to Eq. (3.1).

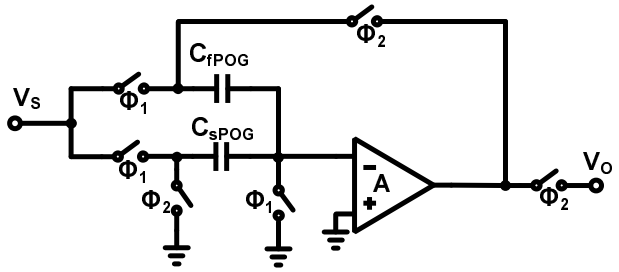

Figure 3.1: POG flip-around MDAC

For the integrator in Fig. 3.2, the effect of magnitude and phase errors are removed by choosing $C_{fPOG} = C_f\big(1+\frac{1}{A}\big)$, $C_{sPOG} = C_s$ and $C_{dPOG} = C_d\big(1+\frac{1}{A}\big) + \frac{C_s}{A}$. In the presence gain variation, the effective amplifier gain is the nominal gain, A divided by mismatch factor. This technique is quite challenging to implement, especially in submicron technologies as variations in gain are more severe. Moreover,

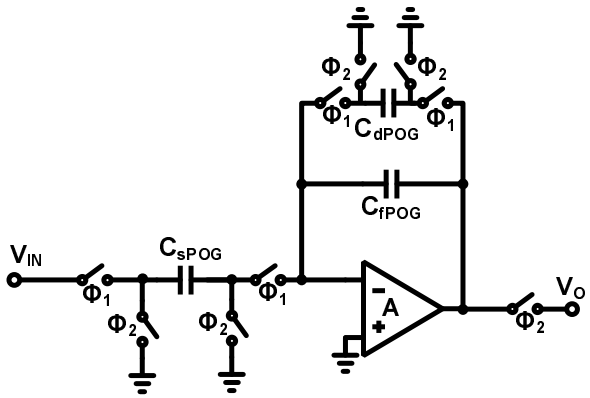

Figure 3.2: POG integrator

there is still significant variations at the virtual ground which worsens distortion. Thus, designing an amplifier that is very linear and has low sensitivity to PVT variations is the only way to get the benefit of gain enhancement using the POG technique.

The POG technique does not perform offset or $\frac{1}{f}$ noise cancelation, but it is compatible with several offset canceling techniques. Moreover, there is no additional thermal noise since the capacitor values do not change appreciably.

3.3 Replica Gain Enhancement

This technique uses a replica amplifier to provide an estimate of the output voltage, so that the main amplifier has to settle to only the difference between the estimated and actual output voltage. This significantly reduces the error voltage at the virtual ground and increases the loop gain.

Fig. 3.3 show a switched-capacitor sample-and-hold using replica gain enhancement [11]. The main loop is the loop formed by C_s and G_{m1} and R_{o1} while

C_A, C_B, G_{m2} and R_{o2} forms the replica loop. During ϕ_1, the input signal is sampled on C_s and the output is estimated by the replica loop. During ϕ_2, the voltage is held on C_s, and since the replica loop maintains the estimated output voltage, the main loop does not need a large error voltage to hold V_o. The output of the sample-and-hold at the end of ϕ_2 can be expressed as

$$V_{OUT} = \Big[1 - \frac{1}{\big(1 + G_{m1}R_o\big)\big(1 + G_{m2}R_o\big)}\Big]V_{IN}. \tag{3.3}$$

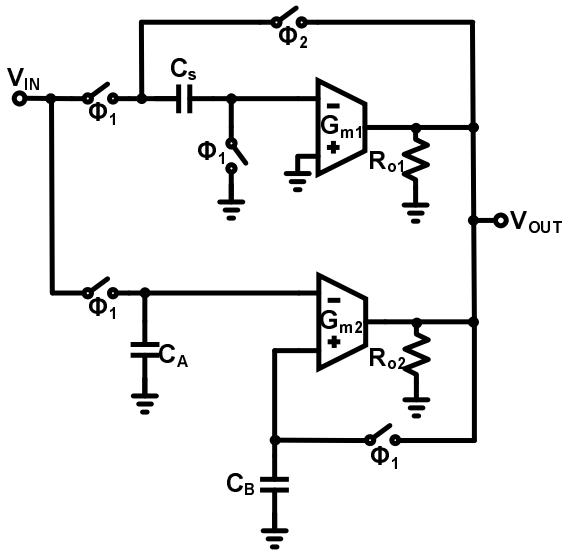

Figure 3.3: Replica gain enhanced SAH

From Eq. (3.3), the sample-and-hold achieves a lop gain that is the product of the loop gains of the main and replica paths. Also, the offset of the either the main or replica amplifiers are attenuated by the gain of the other. However, the addition of C_A loads the input. A gain stage realization [12] of the replica gain enhancement technique is shown in Fig. 3.4. An amplifier stage is used to isolate the holding capacitor from the virtual ground. This ensures that feedback factor of the gain stage is not affected by the holding capacitor. The gain stage requires

three phases to operate. The input voltage is sampled on the capacitors C_S and C_F at the end ϕ_1. The output is estimated in ϕ_{21}, and the charge needed maintain the estimate is stored on C_H. At the amplification in ϕ_{22}, the output voltage settles to

$$V_{OUT} = \Big[1 - \frac{1}{\big(1 + A_1 G_{m2} R_o \beta\big)^2}\Big] V_{IN}. \tag{3.4}$$

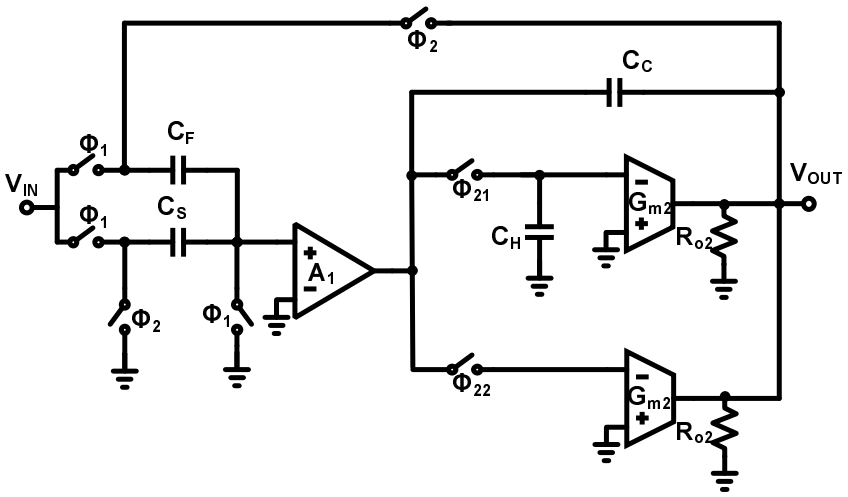

Figure 3.4: Replica gain enhanced gain stage

The gain stage achieves an effective loop gain that is the product of the loop gains of the main and replica loops. The use of a two stage amplifier reduces the effect of sampled noise due to the holding capacitor and the offset. It is worth noting that the use of replica stages causes the technique to suffer from output impedance degradation since the two transconductance amplifier outputs are tied together ($R_o = R_{o1}//R_{o2}$).

3.4 Correlated Double Sampling

Correlated double sampling (CDS) encompasses a number of gain enhancement techniques that achieve gain enhancement by using a voltage that is corre-

lated to the one being amplified to correct for the effect of gain error. The same input voltage is used in gain stages for both the estimation and the correction to ensure good correlation. In integrator realizations, the previous output voltage, which is typically strongly correlated to the current output voltage due to over-sampling, could be used for gain error correction. The technique was initially used to remove just the offset voltage and $\frac{1}{f}$ noise of amplifiers, before its gain enhancement property was realized. The CDS technique has been extensively studied and improved over the years, so the discussion below is limited to a few representative circuit realizations. The operation of the gain stages and integrators are described and the effective gain enhancement are shown. An exhaustive list of the techniques, their operation and effective gains can be found in [13, 14, 15].

3.4.1 Predictive Correlated Double Sampling

An earlier CDS integrator presented in [16] is shown in Fig. 3.5(b). A gain stage obtained by modifying a version of the integrator is also shown as Fig. 3.5(a). For the gain stage, the output is estimated by connecting C_1 and the bottom C_2 in an inverting amplifier configuration. The capacitor C_1 samples the input with respect to the error voltage at the input of the amplifier, while the top C_2 also samples the error voltage. Therefore, at the beginning of the amplification phase in ϕ_2, the negative of the estimated error is already pre-charged on the capacitors. The effective loop gain achieved using this techniques becomes extremely frequency dependent due to the use of the previous output sample. This technique assumes strong correlation in successive samples, hence can only be used in narrowband applications. The effective gain enhancement is highest at DC and degrades with frequency. The output voltage with the gain error at DC and Nyquist are

$$V_{OUT} = \begin{cases} \frac{C_1}{C_2}\left[1 - \frac{1}{1+A\beta_1+A^2\beta_2}\right]V_{IN} & \text{if } z = 1, \\ \frac{C_1}{C_2}\left[1 - \frac{1+\frac{\beta_2}{\beta_1}+A\beta_2}{1+\frac{\beta_2}{\beta_1}+A\beta_2(4-\beta_2)+A^2\beta_2}\right]V_{IN} & \text{if } z = -1, \end{cases} \tag{3.5}$$

Approximation of Eq. (3.5) shows that the loop gain is proportional to A^2 at DC but falls to A at the Nyquist frequency. The change of effective loop from DC to Nyquist has a first order dependence on frequency.

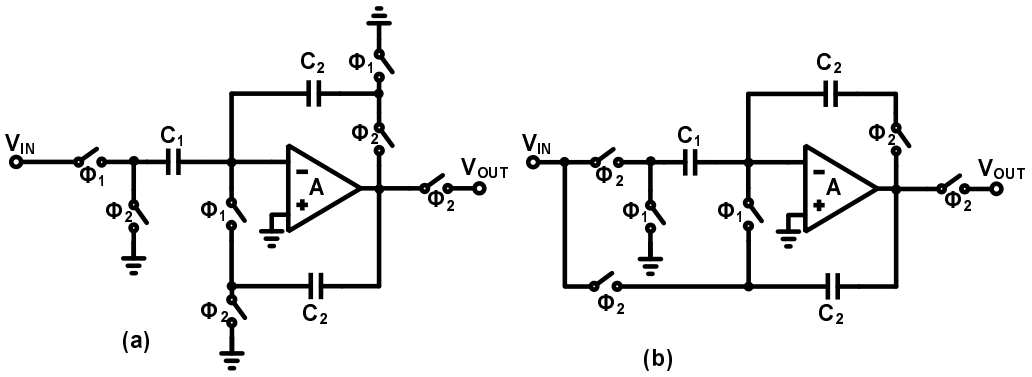

Figure 3.5: Haug CDS (a)gain stage and (b)integrator

The integrator of Fig. 3.5(b) is an inverting delay-free integrator. The error voltage at the virtual ground due to finite gain is estimated in ϕ_1 using the previous input and output voltages sampled on C_1 and C_2. The estimated error voltage is sampled on C_1 and it is used to correct for the gain error in ϕ_2. The output voltage at the end of ϕ_2 is

$$V_{OUT} = \frac{C_1}{C_2}\left[1 - \frac{1}{1+A\beta}\right]\frac{1}{1 - \left[1 - \frac{1-\beta}{(1+A\beta)(2+A)}\right]z^{-1}}V_{IN}. \tag{3.6}$$

The magnitude error of the integrator is unchanged compared to the conventional integrator, but the phase error is suppressed by a factor of $(2 + A)$. Since the effective of magnitude error is not as detrimental to circuit performance as the phase error, this integrator could be used in high performance applications.

An improvement on the gain stage of Fig. 3.5(a) presented in [17] is shown in Fig. 3.6(a). The integrator realization of the same technique is shown in Fig. 3.6(b). The two circuits operate in a similar fashion, but for the reset switches added at the output terminal of the C_2 capacitors.

For the gain stage, the output is estimated during ϕ_2, and the estimated error sampled on the top C_1 and C_2. This estimated error subtracts the gain error during amplification, leading to a better virtual ground. The output voltage at the end of ϕ_1 is

$$V_{OUT} = \frac{C_1}{C_2}\Big[1 - \frac{z^{-1}}{z^{-1} + 2A\beta_1 + (A\beta)^2}\Big]V_{IN}. \tag{3.7}$$

The loop gain from Eq. (3.7) is the square of the nominal loop gain and does not degrade appreciably even at the Nyquist frequency. Therefore, the gain stage can achieve gain enhancement even in wideband applications. The wideband operation is due to the fact that the same input voltage sample is used in both ϕ_1 and ϕ_2.

The fixed input in both ϕ_1 and ϕ_2 is used in the integrator to ensure that the estimation of the error voltage is independent of the input voltage. However, different feedback factors in ϕ_1 and ϕ_2 makes the gain enhancement slightly less than square of the nominal loop gain. The integrator is also delay-free and inverting and its output voltage at the end of ϕ_1 is

$$V_{OUT} = \frac{C_1}{C_2}\Big[1 - \frac{1}{1 + A\beta}\Big]\frac{1}{1 - \Big[1 - \frac{(1-\beta)(1-\beta_2 k)}{(1+A\beta)(1+A\beta_2)}\Big]z^{-1}}V_{IN}. \tag{3.8}$$

The phase error for this integrator is suppressed by a factor of $\frac{1+A\beta_2}{1-\beta_2 k} \approx \frac{A}{1+2k}$.

Another wideband CDS implementation is shown in Fig. 3.7. This realization was proposed in [18, 19] and uses a holding capacitor to store the error voltage to be used for correction, making the gain enhancement frequency independent. However, the additional capacitor (C_I) degrades the feedback factor ($\beta_I < \beta$) and

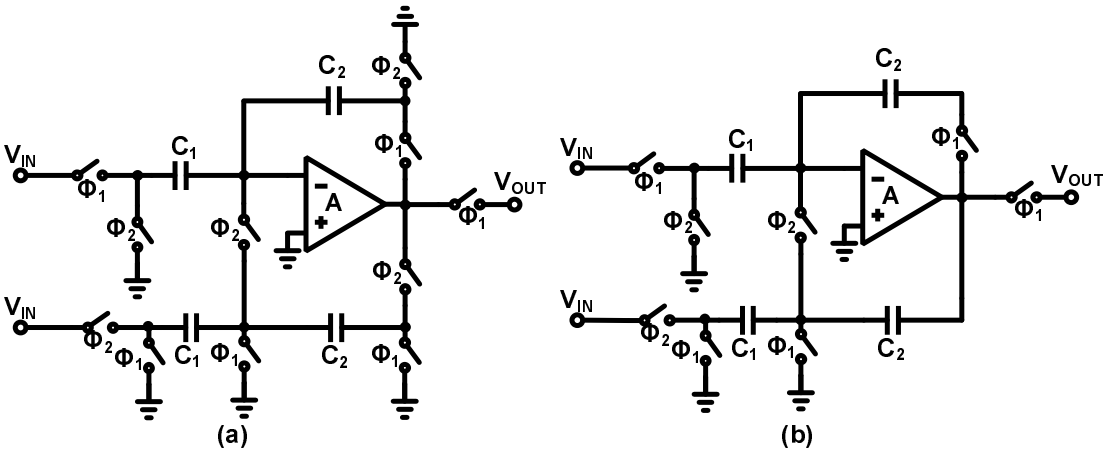

Figure 3.6: Larson CDS (a)gain stage and (b)integrator

worsens $\frac{kT}{C}$ noise. The output voltage of the gain stage at the end of ϕ_2 is

$$V_{OUT} = \frac{C_1}{C_2}\Big[1 - \frac{1}{(1+A\beta)(1+A\beta_I)}\Big]V_{IN}. \tag{3.9}$$

Equation (3.9) shows that the loop gain is the product of the loop gains in ϕ_1 and ϕ_2, where $\beta_I = \frac{C_f}{C_s+C_f+C_I}$.

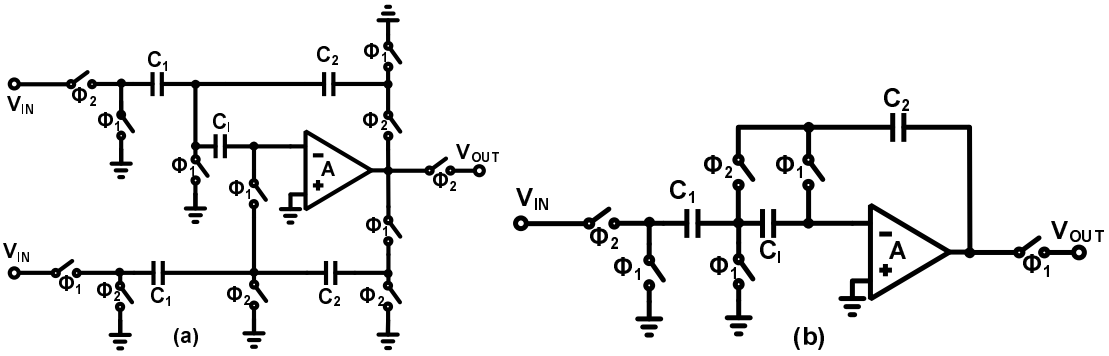

Figure 3.7: Nagaraj CDS (a)gain stage and (b)integrator

The integrator of Fig. 3.7(b) can boast of the least number of additional switches needed to implement the technique. In the switching option shown, the input charge transfer occurs in ϕ_2, with C_I level shifting the virtual ground with

the previous error voltage to provide a more accurate virtual ground. The output is sampled at the end of ϕ_1, the same phase where the charge for level shifting on C_I is refreshed. The output voltage at the end of ϕ_1 can be expressed as

$$V_{OUT} = \frac{C_1}{C_2}\Big[1 - \frac{1 + A(\beta + \beta_1 k)}{(1 + A\beta)(1 + A\beta_1)}\Big]\frac{z^{-1}}{1 - \Big[1 - \frac{\beta_1(1-\beta)}{(1+A\beta)(1+A\beta_1)}\Big]z^{-1}}V_{IN}. \qquad (3.10)$$

The magnitude error in Eq. (3.10) is slightly less that of the conventional one. It was pointed out in [13] that sampling the output at the end of ϕ_2 brings the magnitude error back to that of the conventional integrator. The phase error is suppressed by a factor of $(1 + A\beta)/\beta_1 \approx A$.

The input voltage in both Fig. 3.6 and Fig. 3.7(a) is assumed to remain unchanged in both the prediction and amplification phase, to achieve wideband operation. This will require either a sample-and-hold or additional phase to realize, thus reducing speed of operation or increasing power consumption.

3.4.2 Time-Shifted Correlated Double Sampling

The time-shifted CDS technique [20], a gain stage realization of which is shown in Fig. 3.8 sought to remove the extra clock phase requirement by passing the predicted output to the next stage's prediction network at the end of ϕ_1 . This way, when the amplification is been performed in the current stage, the next stage is in prediction mode. In a pipelined ADC implementation, a sample-and-hold stage is needed in front of the first stage to make this technique effective. Also, since the predicted rather than the accurate output is used for estimation in the subsequent stages, the gain enhancement degrades down the pipeline.

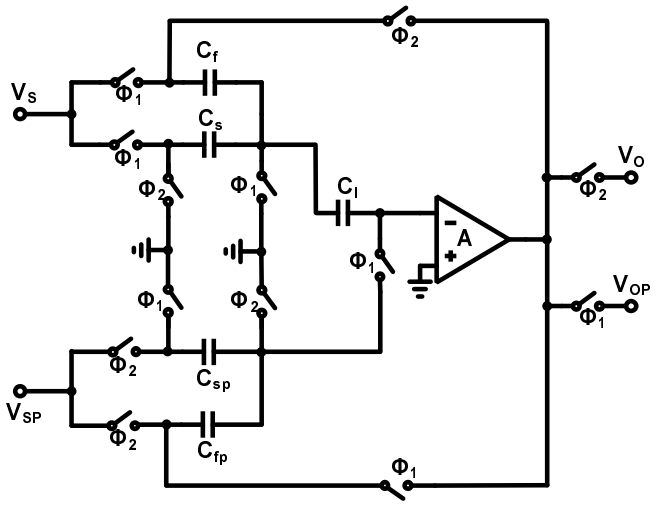

Figure 3.8: Time-shifted CDS

3.4.3 Time-Aligned/Split-Capacitor Correlated Double Sampling

The time-aligned variant of [20] presented in [21] obviates the need for a sample-and-hold by sampling the input for both prediction and amplification at the same time. This necessitates an extra set of sampling capacitors to maintain the same sampling frequency. Also, the large loading of the previous stage slows down settling and thus increasing power consumption. To speed up the pipeline time-shifted CDS stages where used after the first stage, with a time-aligned stage inserted in the fourth to reset the error accumulation.

The extra loading that prevents the use of time-aligned CDS stages in all the pipelined stages was avoided in the split capacitor CDS of [22]. The split capacitor CDS employs the loading-free MDAC stage of [23] and [24] in time-aligned CDS stages obviating the need for extra load capacitors. Due to the nature of the loading-free MDAC, the split-capacitor CDS could be applied to only the first four stages of the pipeline.

3.5 Correlated Level Shifting

Correlated Double Sampling (CDS) technique has been proven to be an effective way of enhancing the effective loop gain of switch-capacitor gain stages. The technique makes it possible to use simple low gain amplifiers to realize high accuracy data converters. However, most realizations of the CDS technique suffer from increased thermal noise, and limited gain enhancement due to mismatch between predictive and corrective phases. This limitations will reduce the effectiveness of CDS techniques in deep submicron technologies where the intrinsic gain and available signal swing are low. Correlated Level Shifting (CLS) was proposed recently to offer a more power-efficient alternative to CDS even in deep submicron technologies. It achieves high effective loop gain and true rail-to-rail operation [25]. Moreover, the additional thermal noise due to the CLS scheme is very small, almost negligible.

The circuit in Fig. 3.9 shows a Correlated Level Shifting gain stage. The input is sampled at the end of ϕ_1. The amplification phase (ϕ_2) is divided into ϕ_{21} for estimation and ϕ_{22} for level-shifting. The level-shifting capacitor, C_{LS}, samples the estimated output at the end of ϕ_{21} and is placed in series with the amplifier output in ϕ_{22}. This always brings the amplifier output back to the mid-rail at the beginning of ϕ_{22} forcing a more accurate virtual ground. The final output voltage at the end of ϕ_{22} is

$$V_O = \frac{C_s + C_f}{C_f}\Big[1 - \frac{1+\lambda}{\big(1+A\beta\big)\big(1+A\beta+\lambda\big)}\Big]V_S. \tag{3.11}$$

During the level shifting phase, there is charge sharing between C_{LS} and the total load capacitance at the output, C_{LD}. This degrades the gain enhancement and increases the swing at the output of the amplifier. The ratio of C_{LD} to C_{LS}

is denoted as λ. For $\lambda = 1$ (or $C_{LS} = C_{LD}$), there is about 6dB loss in gain enhancement. However, increasing the C_{LS} capacitor is not a desirable approach due to power constraints. The charge sharing could be mitigated in a two-stage amplifier configuration as shown in Fig. 3.10. This is because the compensation capacitor in the second stage contributes some of the charge needed at the output of the amplifier [25]. However, a two-stage amplifier may not be always desirable, and the compensation capacitor is designed for stability rather than gain enhancement.

Since the level-shifting is done at the output of the MDAC, noise sampled on C_{LS} capacitor is attenuated by the loop gain. The only disadvantage of the CLS is that it does not cancel offset and $\frac{1}{f}$ noise.

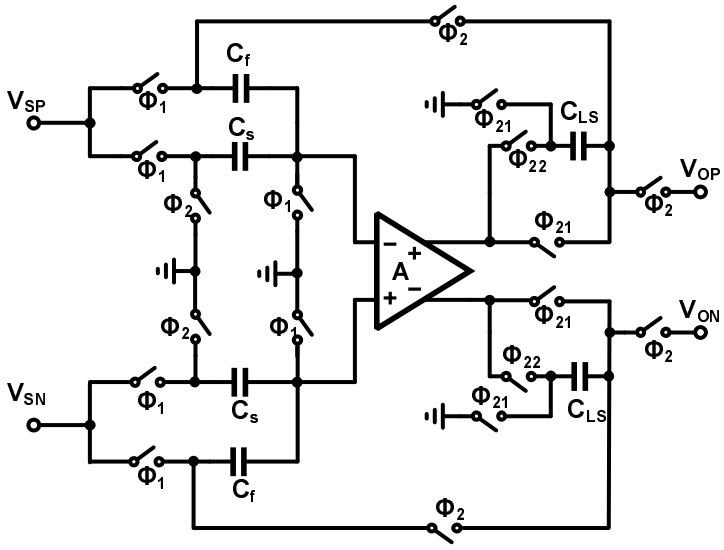

Figure 3.9: Correlated Level Shifting MDAC

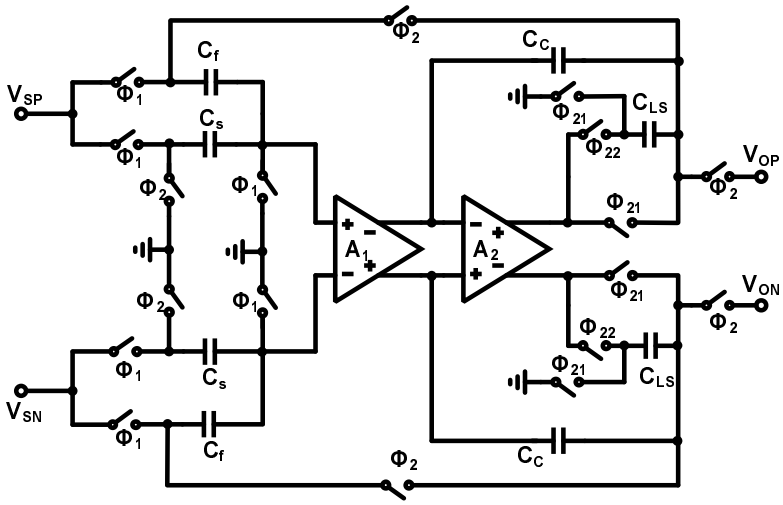

Figure 3.10: CLS MDAC with two-stage amplifier

CHAPTER 4. CROSS-COUPLED CORRELATED LEVEL SHIFTING PIPELINED ADC

4.1 Introduction

The Correlated Level Shifting (CLS) technique offers a power-efficient way of realizing high effective amplifier gain in switched-capacitor circuits. The gain enhancement is achieved without adding to the thermal noise of the circuit. Moreover, level shifting the amplifier output allows the use of large signal swings, even beyond the power rails. The increased signal swing results in higher signal-to-noise ratio (SNR), or lower analog power if capacitors are scaled down accordingly. This makes the technique extremely useful in deep submicron processes where the supply voltage is around 1V.

However, the use of capacitors to implement the level shifting in switched-capacitor circuits causes charge sharing and makes it difficult for the level shifting capacitor to hold the charge sampled on it. As the level shifting capacitor loses the charge sampled on it, the amplifier swing increases raising the error voltage at the virtual ground in the process. Thus, the charge-sharing between the level shifting capacitor and other capacitors connected to it in the circuit reduces the amount of gain enhancement achieved. Another way to think about this problem is that the use of a capacitor in series with the amplifier in a switched-capacitor circuit forms a voltage divider with the load capacitor, and reduces the loop gain.

One direct way of reducing the amount of charge lost by the level shifting

capacitor is to make it large relative to the load capacitor. However, the amplifier will have to drive the large capacitor in the estimation phase of the technique resulting in higher power consumption. Instead of increasing the level shifting capacitor, the charge sharing could be alleviated by reducing the amount of load capacitance seen by the level shifting capacitor. This will also reduce the voltage division at the output and increases the loop gain.

4.2 Cross-Coupled CLS Technique

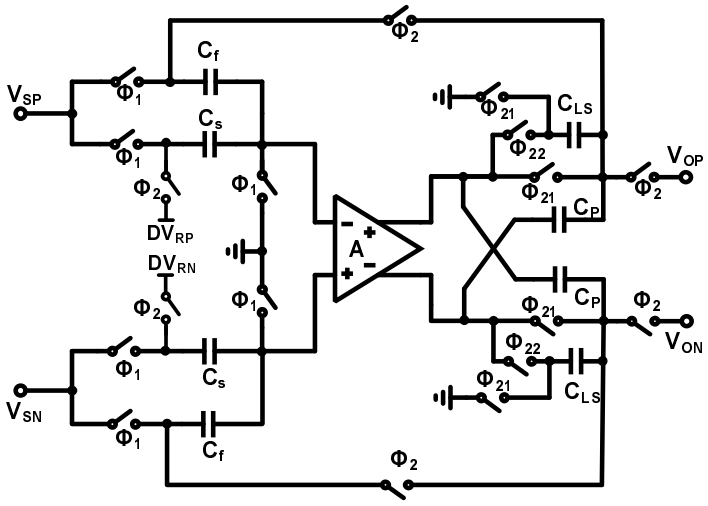

Figure 4.1: Cross-Coupled CLS MDAC

A CLS MDAC that avoids loop gain degradation by using two cross-coupled capacitors is shown in Fig. 4.1. Like the regular CLS MDAC, sampling, estimation and level-shifting occur in ϕ_1, ϕ_{21} and ϕ_{22} respectively. The C_s and C_f capacitors sample the input in ϕ_1. The level shifting network at the output is reset during this phase. During the estimation phase in ϕ_{21} (shown in Fig. 4.2), C_f is flipped around to the output and the C_P capacitors are connected across the differential output. At the end of ϕ_{21}, the estimated output voltage is sampled on C_{LS} and the

differential output voltage is sampled across C_P. The load seen by the amplifier in this phase is larger than in the regular CLS due to the addition of the two C_P capacitors. However, as it will be shown later, the value of C_P can be quite small, so the extra power needed to settle in this phase negligible.

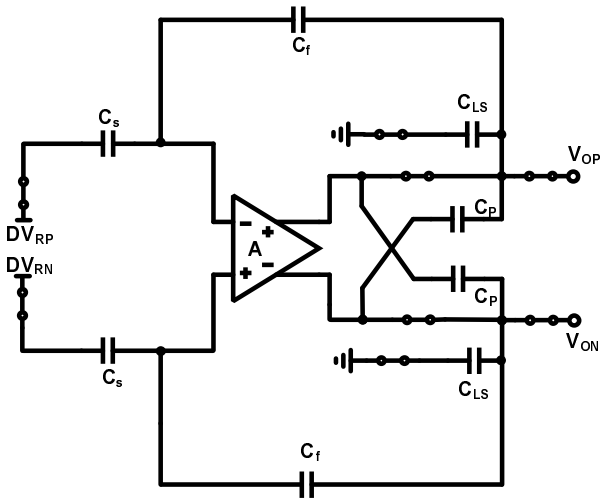

Figure 4.2: Cross-Coupled CLS MDAC - Estimation

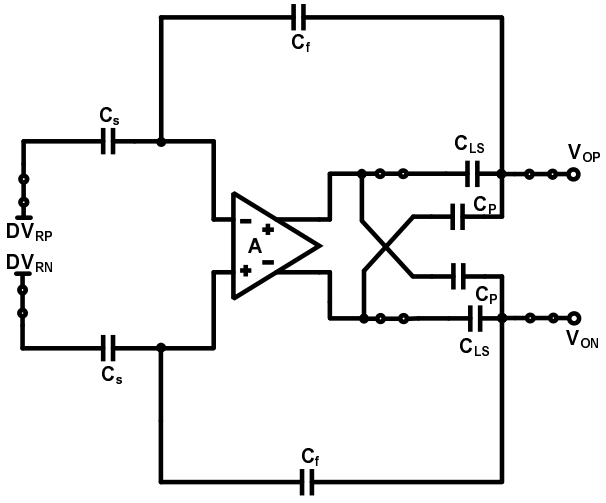

Figure 4.3: Cross-Coupled CLS MDAC - Level Shifting

At the beginning of ϕ_{22}, the C_{LS} capacitors are used to bring the amplifier output back to the common-mode level. This action forces the charge that can be

held across C_P to just a single-ended output voltage. The excess (deficient) charge on C_P is sourced to (sank from) the load capacitor. Proper sizing of C_P could make it provide exactly the same amount of charge lost by C_{LS} and thus remove the effect of charge sharing. In other words, C_P realizes a negative capacitance because it forms a positive feedback loop with the amplifier (as can be seen in Fig. 4.3), and the value of the capacitance could be chosen such that it neutralizes the load capacitance. Removing the effect of the load capacitor will prevent charge sharing and avoid the loop gain degradation prevalent in the regular CLS.

The output voltage of the MDAC at the end of ϕ_{22} can be expressed in a similar way to the regular CLS as

$$V_O = \frac{C_s + C_f}{C_f}\Big[1 - \frac{1+\lambda}{\big(1+A\beta\big)\big(1+A\beta+\lambda\big)}\Big]\Big[V_S - \frac{C_s}{C_f}DV_R\Big]. \tag{4.1}$$

However, the λ that limited the gain enhancement in the regular CLS is modified by C_P and becomes

$$\lambda = \frac{C_{LD} - C_P(A\beta - 1)}{C_{LS}} \tag{4.2}$$

It can be observed from Eq. (4.2) that if the DC gain of the amplifier (A) is precisely known, C_P could be chosen to eliminate the gain error of the MDAC. In other words, designing for a λ = -1 will result in an MDAC with infinite effective loop gain.

4.2.1 Sensitivity to DC gain variations

The value of C_P used depends on the nominal amplifier gain, which is difficult to predict accurately. The effective loop gain will therefore be sensitive to variations in the amplifier gain. The sensitivity of the effective loop gain to DC gain deviations from its nominal value due to process and device mismatch is shown in Fig. 4.4.

For the plot, a nominal loop gain of 20dB is used, and it is assumed that the open loop DC gain does not change between ϕ_{21} and ϕ_{22} for both the regular and cross-coupled CLS. Also, $C_{LD} = 455$fF, $C_{LS} = 200$fF and $C_P = 72$fF. The effective loop gain of the cross-coupled CLS is much larger than that of the regular CLS for most of the range of variations. It falls below the effective loop gain of the regular CLS when the actual initial loop gain is much larger than the nominal, because of over compensation. For lower actual amplifier gain values, the effective loop gain of the cross-coupled CLS will at worst be the same as that of the regular CLS.

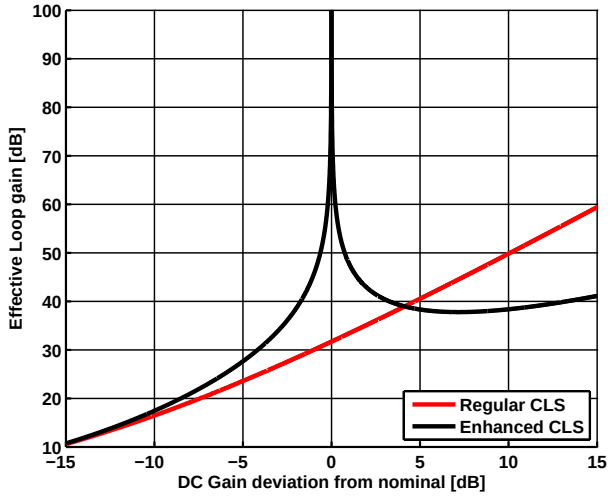

Figure 4.4: Sensitivity of loop gain to DC gain variation

The sensitivity of the effective loop gain reduces with larger C_P (and corresponding large C_{LS}). Fig. 4.5 shows a 3D plot of the sensitivity of the effective loop gain to gain variations and cross-coupling capacitance. A loop gain of 30dB and a load capacitance of 600fF was used for this plot. It is evident that the sensitivity of the effective loop gain to DC gain variations worsens at lower values of C_P. However, larger C_P values require large C_{LS} values, increasing the load the amplifier drives during the estimation phase.

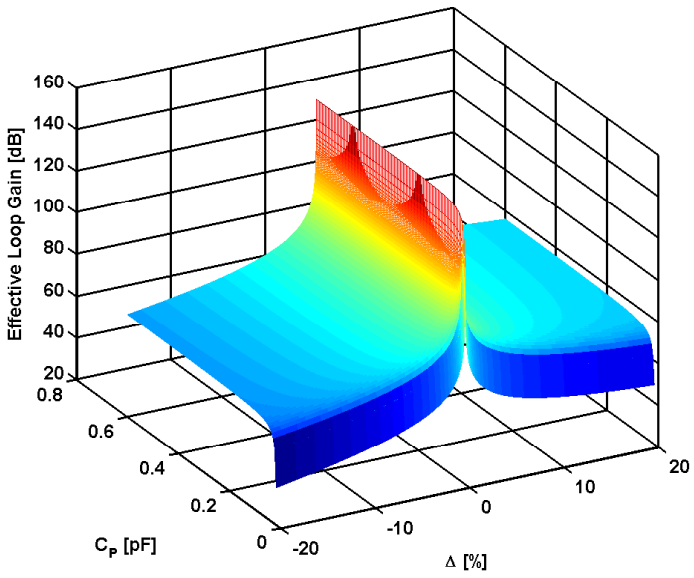

Figure 4.5: Effect of C_P on Accuracy

It is important to note that any parasitic capacitors at the output of the MDAC will increase the load capacitance and further degrade loop gain. Moreover, parasitic capacitors at the input of the amplifier, known to reduce loop gain, will reduce the amount of the effective cross-coupled capacitance and hence the compensation. Therefore, care must be taken to minimize parasitic capacitances. In processes that predict these parasitic capacitors with some degree of accuracy, their values could be accounted for while designing the MDAC to ensure that their adverse effect is reduced.

To ensure high effective loop gain over wider PVT variations, the capacitors C_P could be made trimmable. A few trimming bits or fuses will be enough to ensure high performance over all PVT variations.

4.2.2 Loop characteristics and settling

The loop behavior during the estimation phase (Fig. 4.2) is similar to that of a regular MDAC. Assuming the amplifier has a single pole roll-off with DC gain A_0 and unity gain bandwidth ω_t, the loop gain, L, and time constant, τ, are given by

$$L_{21} = A\beta \tag{4.3}$$

$$\tau_{21} = \frac{1}{\beta\,\omega_t}. \tag{4.4}$$

The unity gain bandwidth in ϕ_{21} is determined by the g_m of the input pair of the amplifier and the load capacitor.

$$\omega_t = \frac{g_m}{C_{LD}} \frac{C_{LD}}{C_{LD} + C_{LS} + 4C_P} \tag{4.5}$$

From Eq. (4.5), the unity gain bandwidth of the CLS MDAC in ϕ_{21} is slightly less than that of the regular MDAC ($\omega_{t0} = g_m/C_{LD}$). The time domain expression for the output of the CLS MDAC in ϕ_{21} becomes

$$V_{O21} = \Big[1 - \frac{1}{1 + A_0\beta}\Big]\Big[1 - e^{-\frac{t}{\tau_{21}}}\Big] V_{Oideal}. \tag{4.6}$$

The MDAC behavior in ϕ_{22} (Fig. 4.3) is more interesting. In this phase, the loop gain and time constant are given by

$$L_{22} = \frac{A\beta}{1 + \lambda} \tag{4.7}$$

$$\tau_{22} = \frac{1}{\beta\,\omega_{t0}} \frac{|C_{LD} - C_P(A\beta - 1)|}{C_{LD}}. \tag{4.8}$$

Consequently, the time domain expression for the output voltage during this phase can be expressed as

$$V_{O22} = V_{O21}(Ts/4) + \Big[1 - \frac{1 + \lambda}{1 + \lambda + A_0\beta}\Big]\Big[1 - e^{-\frac{t}{\tau_{22}}}\Big]\big(V_{Oideal} - V_{O21}(Ts/4)\big). \tag{4.9}$$

It can be observed from Eq. (4.9) and Eq. (4.8) that the time constant could be designed to be very small, essentially removing any settling error in this phase. This benefit comes automatically when the loop degradation due to charge sharing is perfectly compensated by choosing $\lambda = -1$ in Eq. (4.2).

One settling effect not captured by Eq. (4.9) is the charge injection of C_P into the load capacitors at the beginning of ϕ_{22}. This causes an overshoot in the output voltage, that eventually settles out. The magnitude of the overshoot is proportional to the ratio of the effective cross-coupling capacitor, $C_P(A\beta - 1)$, to the total load capacitor, C_{LD}. The overshoot does not adversely affect settling since it is associated with very low output settling time constant.

The output waveform of the CLS MDAC is shown in Fig. 4.6, where ϕ_{21} is between 5ns and 7.5ns, and ϕ_{22} is between 7.5ns and 10ns. As can be seen from the settling response at the beginning of ϕ_{22}, the larger the value of C_P (degree of compensation), the larger the overshoot. There is an overshoot in the case of perfect compensation because for $\lambda = -1$, $C_P(A\beta - 1)$ has to be greater than C_{LD}.

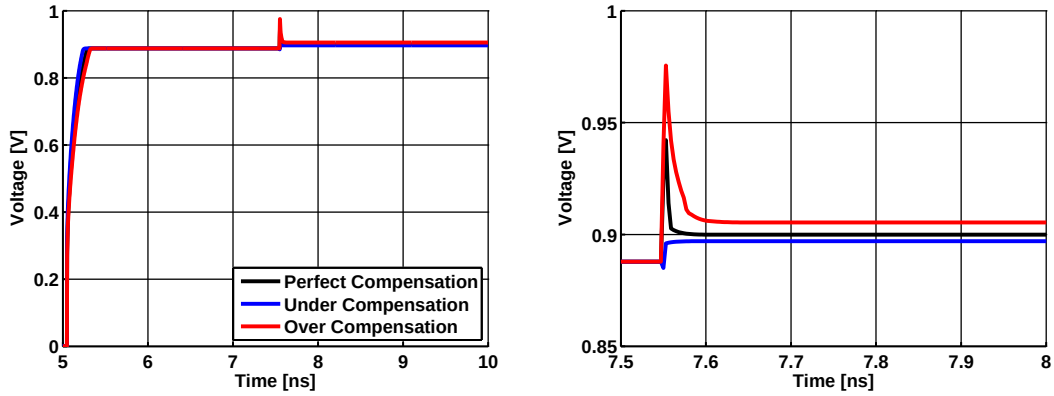

Figure 4.6: Settling response of CLS MDAC

4.3 Architecture

The improved CLS technique is used to design a 10-bit pipelined ADC. The block diagram of the pipelined ADC is shown in Fig. 4.7. The optimum number of bits per stage in a pipelined ADC has been shown to be minimum for low resolution applications [26]. For high resolution applications, higher number of bits is more desirable [27]. One reason why higher number of bits per stage are avoided, especially for low resolution applications, is that the capacitive loading does not easily scale down the pipeline. This is because although the sampling capacitors of the MDACs could be scaled down aggressively, the sampling capacitors from the quantizers are limited by matching. This slowed rate at which the load capacitor of each stage reduces down the pipeline makes reduces the power benefits that could be achieved from capacitor scaling.

The cross-coupled CLS MDAC allows the use of multiple bits per stage. This is because the load neutralization in the level-shifting phase isolates the amplifier from the load and minimizes the power penalty incurred in using multi-bit stages. A 2.5bit per stage was therefore chosen for this design. The pipeline has four stages resolving 2.5bits each and a 2-bit flash at the end. The total sampling capacitance is 400fF for the first stage, 200fF for the second, and 120fF for the third and fourth stages.

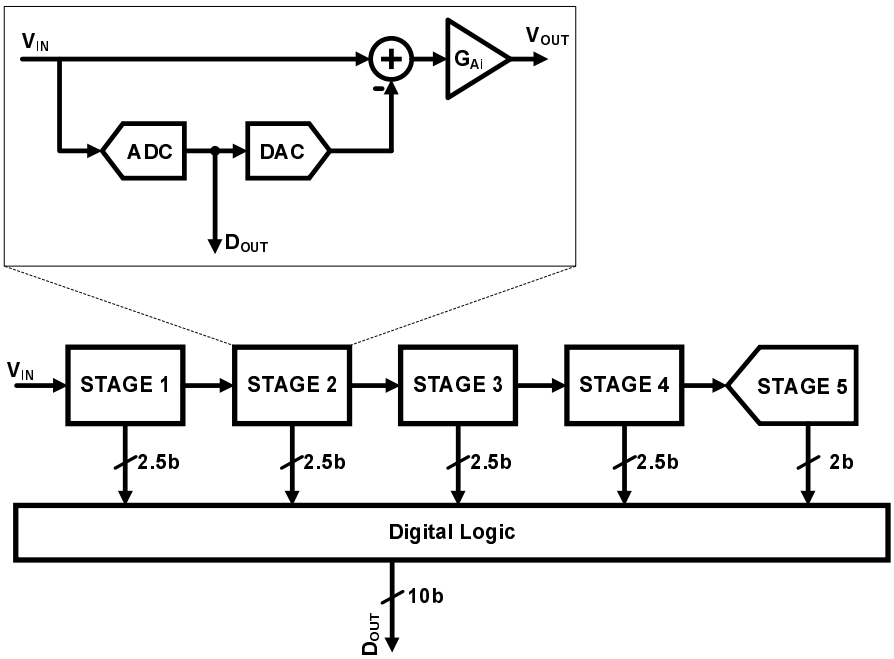

Figure 4.7: Pipelined ADC block diagram

4.4 Circuit Implementation

4.4.1 No SAH Input Stage

To save power, no dedicated S/H stage is used and an input sampling scheme akin to the one reported in [28] is adopted to minimize aperture error and alleviate kickback. The SAH-less front-end implementation is shown in Fig. 4.8. Since the CLS scheme requires a four phase clock to operate, no extra hardware is required to generate an early sampling edge. The input is sampled at the end of ϕ_{11} to a fixed voltage for both the sampling capacitors in the MDAC and subADC.

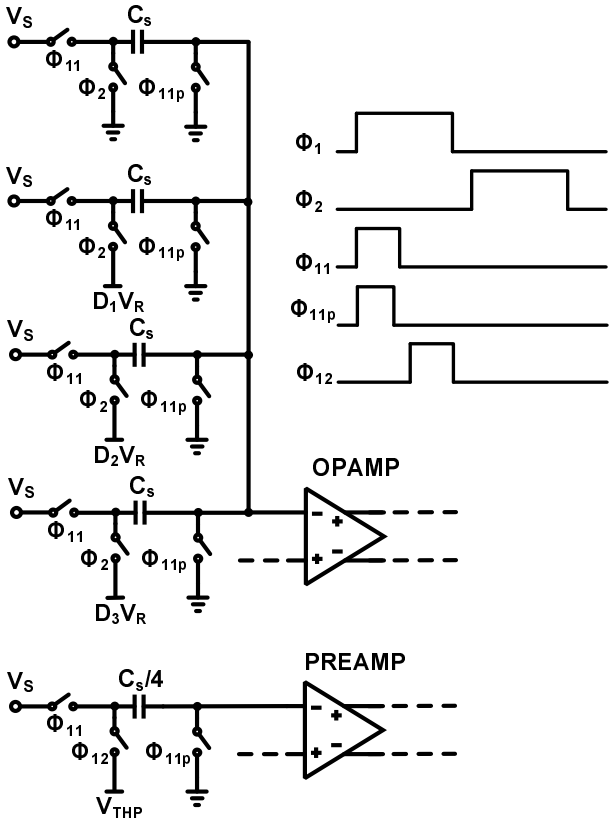

Figure 4.8: SAH-less sampling configuration

4.4.2 2.5bit/stage MDAC

In the absence of a SAH, the first MDAC becomes the most power consuming block in the pipelined ADC. There are numerous configurations of the MDAC, each more suited to a particular technique or application. An MDAC with a dedicated feedback capacitor is preferred to the flip-around MDAC in applications where low kickback is needed. However, the flip-around MDAC gives better power/speed trade-off. The DAC capacitors could either be separate from the input sampling capacitor for better spurious-free dynamic range or same for less $\frac{kT}{C}$ noise. The DAC switching could either be thermometer, binary or merged [29].

The flip-around MDAC configuration is chosen for this design. The DAC capacitors are shared with the input sampling, with merged capacitor switching to guarantee monotonicity. The 2.5bit/stage MDAC is shown in Fig. 4.9, with $C_s = C_f$ to realize a multiply by four stage. The level shifting and cross-coupled capacitors, C_{LS} and C_P respectively, are reset during ϕ_1. The load capacitor, not shown here, consist of the sampling capacitors of the succeeding stage's MDAC and subADC and are connected to the output for the entire amplification phase, ϕ_2.

4.4.3 Opamp

A telescopic op-amp with just and NMOS cascode was used in the MDAC and is shown in Fig. 4.10. M_6 an M_7 are designed to have longer lengths for gain. Continuous-time common-mode feedback was used as switch-capacitor circuits at the output tend to interfere with the level-shifting and thus the gain enhancement.

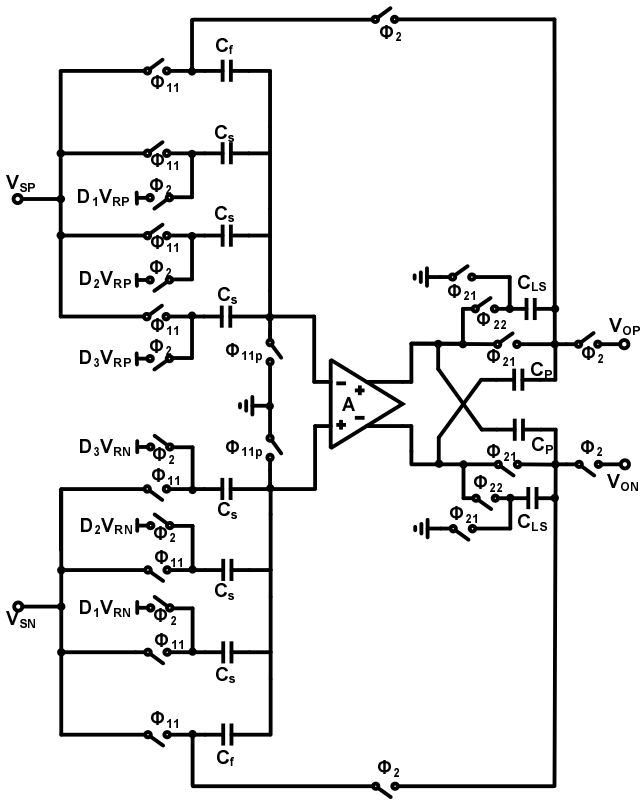

Figure 4.9: 2.5bit MDAC

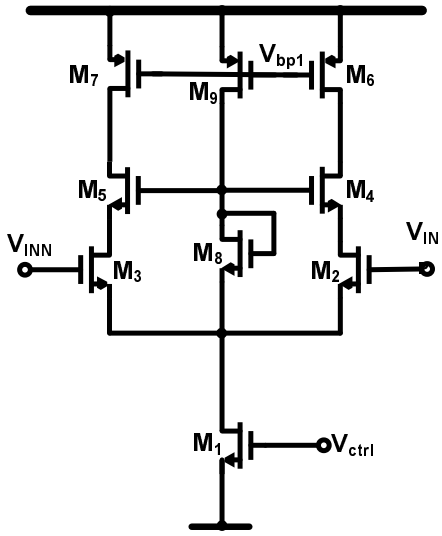

Figure 4.10: Opamp Schematic

The op-amp is designed to have an open loop DC gain of 32dB and a unity gain bandwidth of 850MHz with a tail current of 1.4mA using 1.2V supply in the first stage. The device sizes and tail currents are scaled down for the rest of the stages.

4.4.4 Sampling Switch

For linearity considerations when using rail-to-rail input at low voltage supply, a bootstrapped switch was used for input sampling. The switch reported in [30] (Fig. 4.11) is used and shows over 80dB THD at 1.2V supply. Transmission gates are used for the DACs and other noncritical sampling.

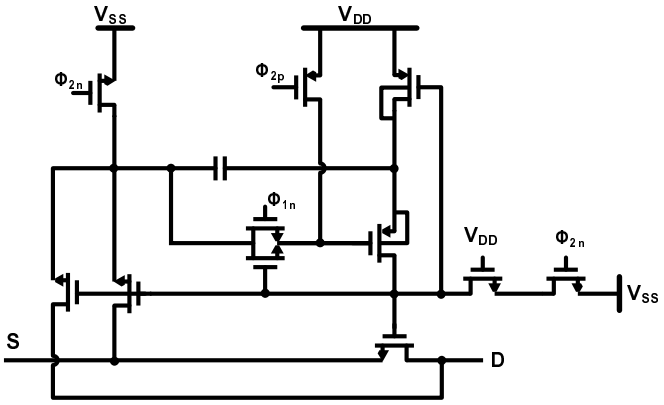

Figure 4.11: Bootstrapped switch

4.4.5 SubADC

The subADC for each stage has a dedicated resistor reference string for generating the comparator thresholds and six comparators. The 7 level DAC is realized as a combination of three 1.5bit DACs, by specific pairing of the six comparator outputs. Several combinations of the comparator output pairs are possible to realize the DAC (three were investigated) but the one presented in Fig. 4.12 was observed to have the least sensitivity to routing mismatch after layout. The three reference DAC circuit used is similar to the one reported in [31] and is shown in Fig. 4.13. The decoded comparator outputs are gated with the amplification phase clock to ensure that the reference are disconnected from the sampling capacitors during the sampling phase.

The decoded digital signals used to drive the DAC switches in each 1.5bit DAC are combined to generate the 3bit binary code. The digital circuit used to perform the decoding is shown in Fig. 4.14. The use of intermediary output of the DAC to generate the binary digital code is simplifies the decoder design.

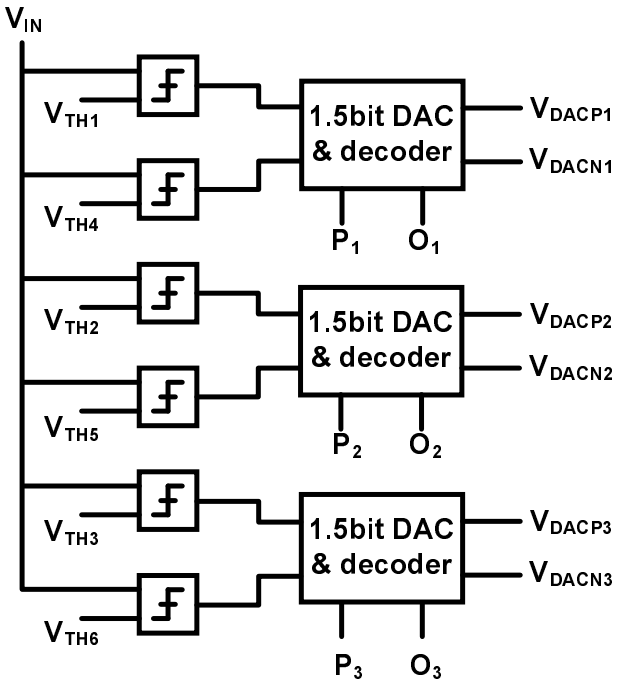

Figure 4.12: 7 level quantizer

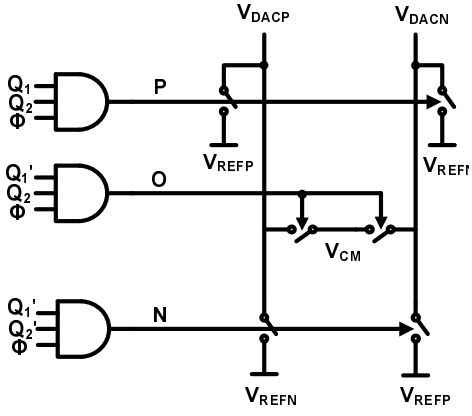

Figure 4.13: 3 level DAC

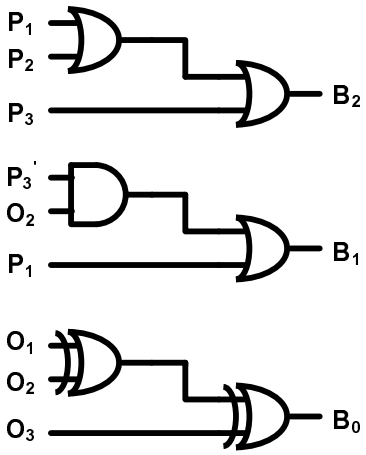

Figure 4.14: 2.5bit decoder

Each of the comparators used in the subADC consists of a preamp, regenerative latch and an SR latch, as shown in Fig. 4.15. The preamp is used to ensure that the latch offset is suppressed. The preamp also reduces the effect of kickback from the latches. Each comparator input has a capacitor that is used to realize the difference between the input voltage and reference thresholds. For the first stage, input is sampled in ϕ_{11} and the threshold voltage is subtracted in ϕ_{12}. The comparator is strobed at the end of ϕ_{21}. For all other stages, the threshold voltages are sampled first on the capacitor during amplification, then the input is subtracted from it in the sampling phase.

4.4.6 Clock Generator

The four phases needed for the MDAC operation are generated using the schematic shown in Fig. 4.16. A fast clock input is brought in off-chip, and is divided down to generate the slow non-overlapping clocks ϕ_1 and ϕ_2. Two non-overlapping clock phases are also generated with fast clock, and these phases are

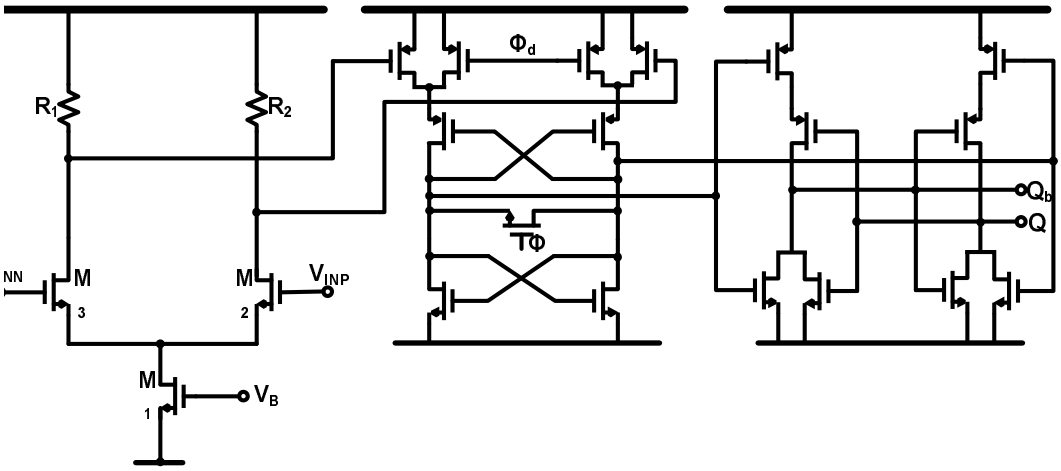

Figure 4.15: Comparator schematics

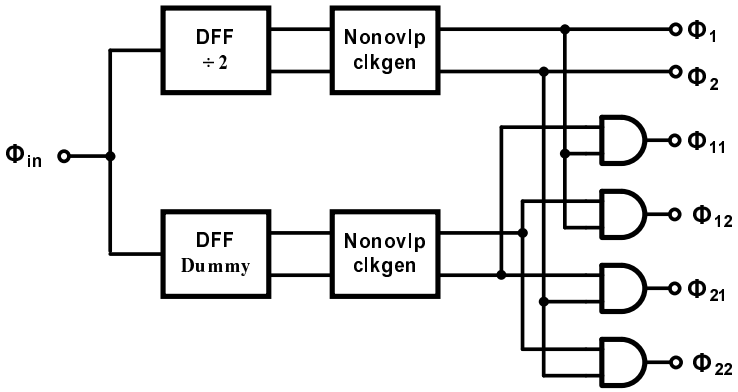

Figure 4.16: Four phase clock generator

gated with the slow clocks to generate ϕ_{11}, ϕ_{12}, ϕ_{21} and ϕ_{22}. The total of six clock phases generated in the circuit are shown in Fig. 4.17. A conventional non-overlapping clock generator is used and is shown in Fig. 4.18.

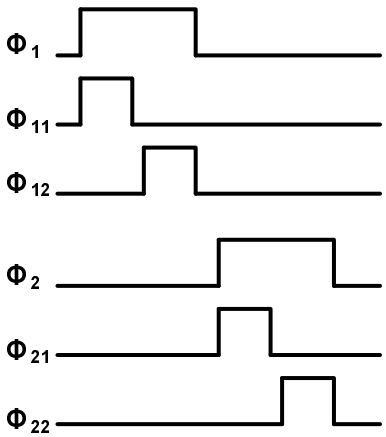

Figure 4.17: Clock phases

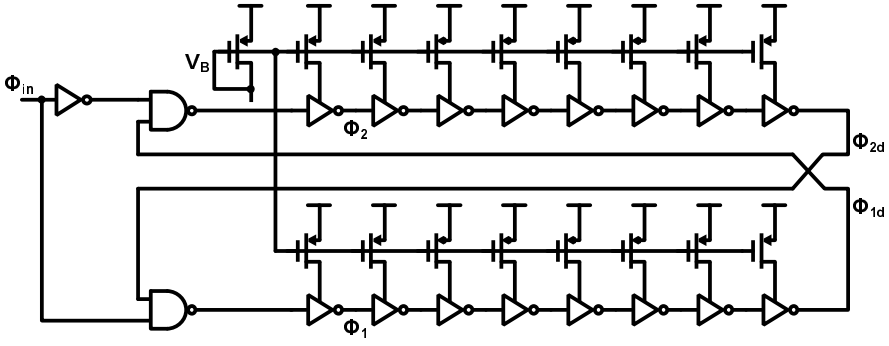

Figure 4.18: Non-overlapping clock generator

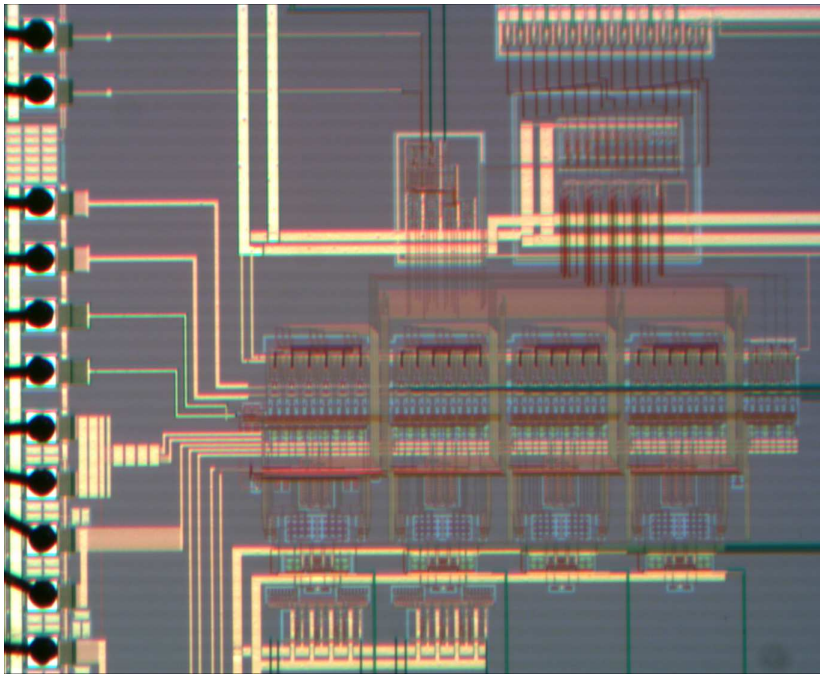

Figure 4.19: Chip Micrograph

4.5 Simulation Results

The pipelined ADC is designed in a 0.18μm 2-poly 4-metal CMOS process. The capacitors are designed as poly-poly capacitor for linearity. The active die area is 1.5mm x 0.9mm. As can be seen in the captured chip micrograph of Fig. 4.19, and it is dominated by the subADC blocks. Optimization of the subADC design will significantly reduce the total are occupied by the chip. The total power consumption is expected to be about 6mW with the analog power consumption estimated at 4mW. The simulated output spectrum of the pipelined ADC at 50MHz clock frequency is shown in Fig. 4.20. For a reference voltage of 1.6V$_{PP}$, the SNDR and SFDR are 61dB and 74dB respectively. The prototype is under testing, so just the expected performance summary is presented in Table 4.1.

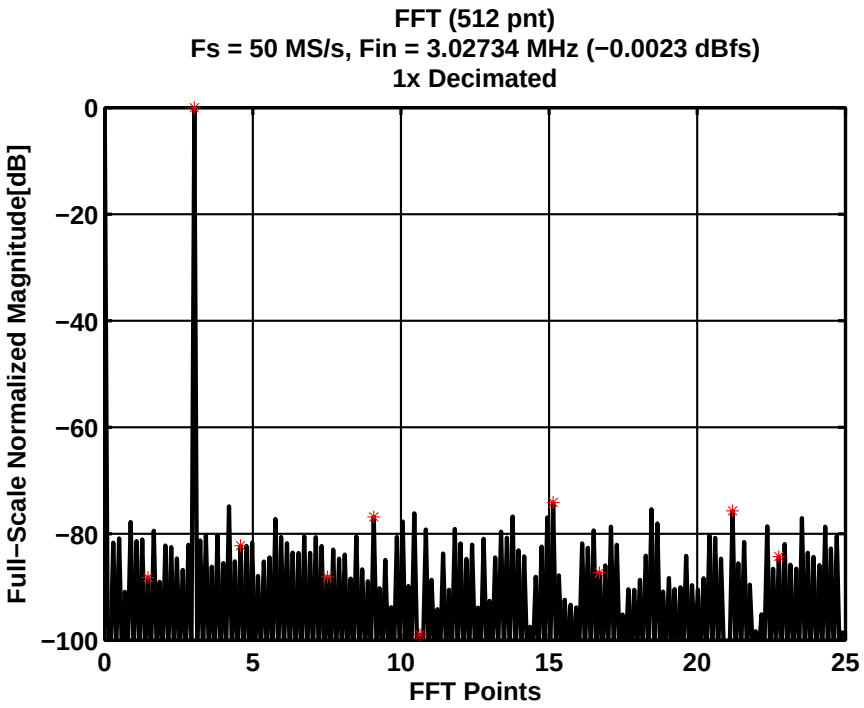

Figure 4.20: ADC output spectrum

Table 4.1: Performance summary

Technology	0.18μm CMOS
Supply voltage	1.2V
Clock Frequency	50MHz
Input range	2.4V$_{PP}$
ENOB	9.0 bits
SFDR	74.0dB
Power consumption	6mW
Active die area	1.5μm x 0.9μm

CHAPTER 5. CORRELATED LEVEL SHIFTING INTEGRATOR

5.1 Correlated Level Shifting Integrator

The CLS technique could be applied directly to an integrator. A three-phase CLS integrator realization is shown in Fig. 5.1 [32]. Like the MDAC version, the input voltage is sampled in ϕ_1. The estimate of the output is obtained in ϕ_{21} and it used to level shift the amplifier output in ϕ_{22}. The output voltage at the end of ϕ_{22} is can be expressed as

$$V_{OUT} = \frac{C_s}{C_f}\Big[1 - \frac{1+\lambda}{A\beta(1+\lambda+A\beta)}\Big]\frac{z^{-1}}{1-\Big[1-\frac{(1+\lambda)(1-\beta)}{1+\lambda+A\beta(1+\lambda+A\beta)}\Big]z^{-1}}V_S. \qquad (5.1)$$

From Eq. 5.1, both the magnitude and phase errors are proportional to $1/A^2$, approximately a factor of A improvement from the regular integrator. The CLS integrator, like its MDAC counterpart, has few advantages over the CDS integrators. The level shifting at the output of the amplifier allows rail-to-rail swing and curbs distortion. Moreover, moving the level-shifting network to the output of the integrator ensures that any additional thermal noise due to the extra switching is attenuated by the loop gain.

In spite of the benefits of CLS integrator over the CDS integrator, there are a few issues with it that need to addressed. One of the issues is that the extent of gain enhancement is determined by λ, which as explained earlier is the ratio of the load capacitance to the level shifting capacitance. Small C_{LS} capacitance

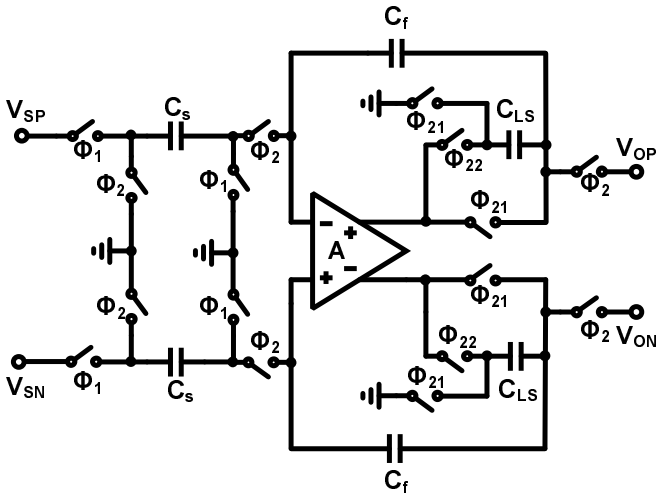

Figure 5.1: CLS Integrator

compared to the total load capacitance results in only marginal gain enhancement. Also, unlike the CDS integrators explored earlier, the offset and $\frac{1}{f}$ noise is not suppressed. Furthermore, the three-phase operation is not usually desirable in high speed applications.

If instead of estimating the current integrator output, we use the previous integrator output for level shifting, we avoid the extra phase required for estimation. This allows a two-phase realization of the CLS integrator. While this may increase the amplifier swing compared to regular CLS, the error at the op-amp virtual ground will depend only on the current input. Fig. 5.2 shows the proposed CLS integrator. The operation is similar to that of the conventional integrator with an additional switched-capacitor network at the output to implement the level shifting. As the next stage's sampling capacitors sample the output during ϕ_1, the level-shifting capacitors (CLS) also sample the output voltage. The CLS capacitors are then used to level-shift the output of the op-amp during the charge transfer phase, ϕ_2. If the voltage sampled across C_{LS} at the end of ϕ_1 matches

the previous output voltage, then the settling error at the virtual ground will be due to only the new charge, driving the phase error to zero. However, the voltage sampled on CLS is less than the output voltage at the end of ϕ_2 due to the finite loop gain in the hold phase (ϕ_1). The use of the previous output voltage for level shifting makes the magnitude and phase errors frequency-dependent. Resolving the magnitude and phase errors at DC yields an integrator output that can be expressed as

$$V_{OUT} = \frac{C_s}{C_f}\Big[1 - \frac{1}{1 + A\beta(1+A)}\Big]\frac{z^{-1}}{1 - \Big[1 - \frac{1-\beta}{1+A\beta(1+A)}\Big]z^{-1}}V_S. \tag{5.2}$$

Both the magnitude and phase errors are suppressed by a factor of $(1 + A)$ at DC. The errors return to the level of the conventional integrator at the Nyquist frequency. The swing at the output of the amplifier will depend on the ratio of the level shifting capacitance to the feedback capacitance. The larger the level shifting capacitor, the lesser the swing but the higher the amplifier power consumption. Thus, there is a trade-off between amplifier swing requirement and power consumption when choosing C_{LS}.

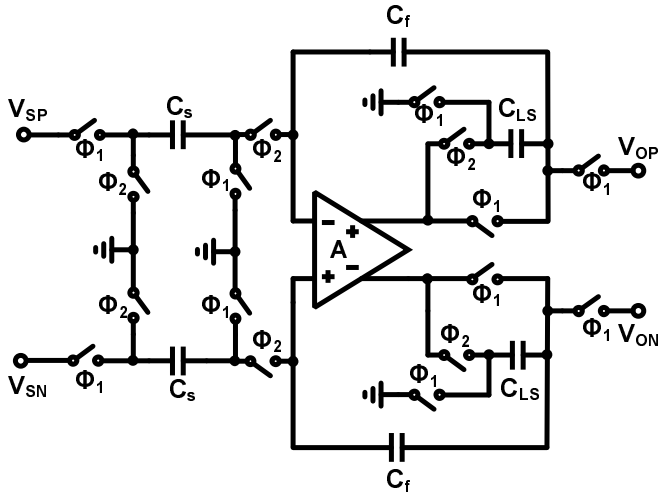

Figure 5.2: CLS Integrator

While the achieved gain enhancement is similar that of the CDS or regular CLS integrators, the proposed CLS integrator has the possibility for better gain if cross-coupling [33] is used to improve the matching between the previous output signal and what gets used for level shifting the amplifier output. If the cross-coupling capacitors are chosen correctly, the phase error of the integrator could be driven to zero. However, this is only a mathematical reality due to the sensitivity of the effective cross-coupling capacitance to the actual amplifier gain.

5.2 Application to $\Delta\Sigma$ Modulators

The proposed CLS integrator is suitable for use in modulator architectures that require very low phase errors. One such architecture is the MASH structure, where accurate loop filters are a necessity. A possible 2-0 MASH modulator where the proposed integrator could be used is shown in Fig. 5.3. The first stage is a 2nd order CIFB structure with a binary quantizer. The second stage is an 8bit flash ADC. The modulator is used to compare the performance of the proposed integrator to the conventional integrator and the CDS integrator of [19].

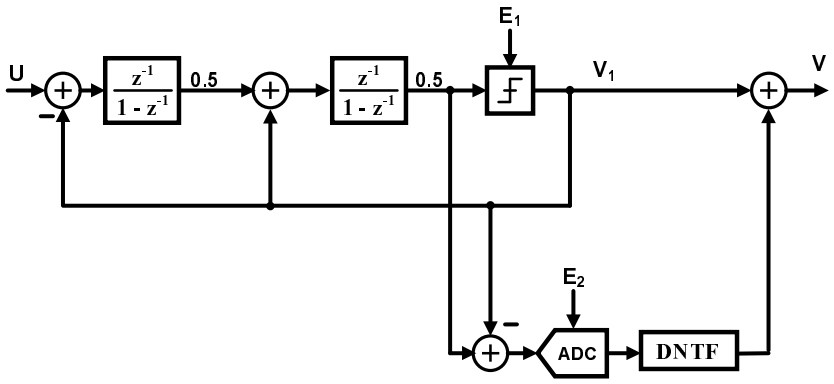

Figure 5.3: 2-0 MASH

5.3 Simulation Results

The transfer functions of the conventional integrator, the CDS integrator of [19] and the proposed CLS integrator of Fig. 5.2 were simulated in Spectre using PAC analysis. The DC gain of the amplifier was chosen to be 26dB and the capacitors were chosen such that $C_s = C_f = C_{LS}$, where C_s is 100fF. As can be seen from Fig. 5.4, the conventional integrator has a low frequency gain of 26dB, while the CDS and CLS integrators obtain a low frequency gain of 52-dB (double that of the conventional). The transfer function of the CLS integrator with cross-coupled gain enhancement capacitor is also shown for completeness, but as discussed earlier, it is sensitive to amplifier gain, making it difficult to achieve very high low frequency gain in practice.

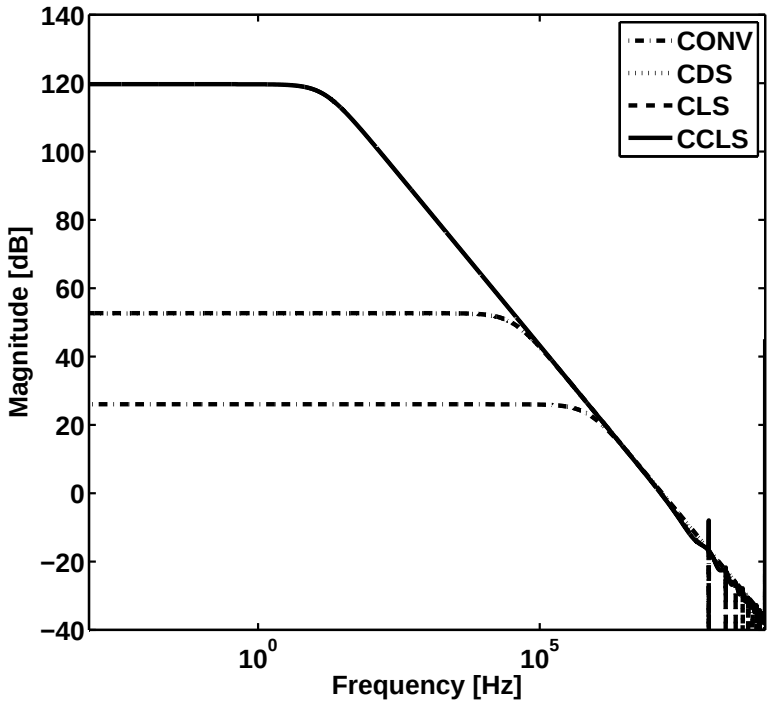

Figure 5.4: Integrator transfer functions

The integrators were also used in the MASH modulator of Fig. 5.3 to compare their respective inband noise suppression. The amplifier DC gain was maintained at 26dB while the two integrators in the loop where designed to have a closed-loop gain of 0.5 each. Simulation results from Spectre shown in Fig. 5.5 show that the modulator with the conventional integrator suffers the worst noise leakage. It achieves an SQNR of 64.0dB at an OSR of 64 while the modulators with the CDS and proposed CLS integrators achieved an SQNR of 80.7dB and 82.0dB respectively. The conventional integrator with an amplifier gain of 120dB (representing ideal) achieves an SQNR of 102.3dB and it is included in Fig. 5.5 as a reference.

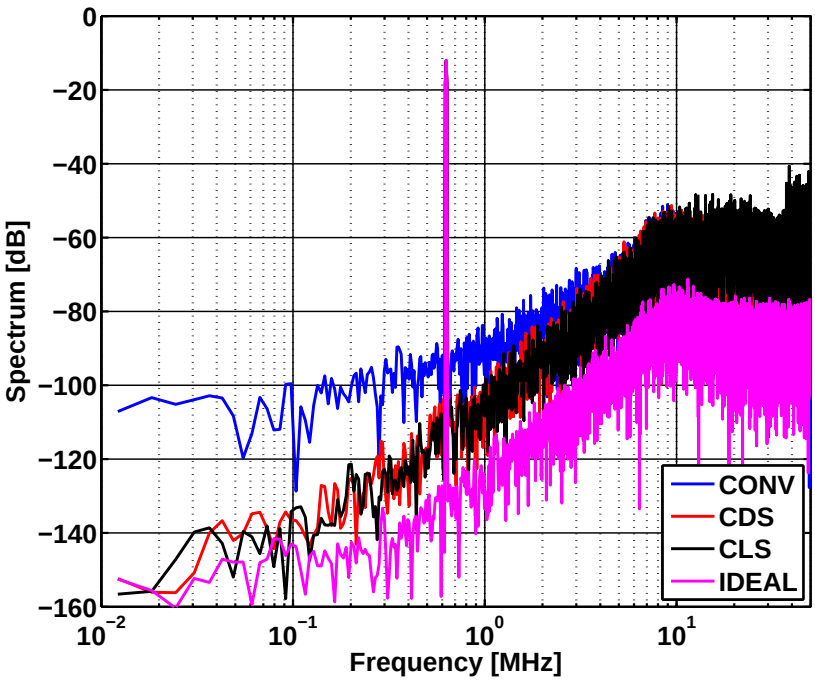

Figure 5.5: Output spectrum of modulator

CHAPTER 6. ALTERNATIVE TO AMPLIFIERS IN SC CIRCUITS

6.1 Introduction

There is a constant research effort devoted to finding alternative ways of implementing active charge transfer in switched-capacitor circuits, since traditional use of amplifiers in closed-loop either limits the frequency of operation or increases power consumption. One approach is to use the amplifier in open loop [34] to realize the 2^N residue amplification. While this approach results in very low power consumption in the open loop amplifier, its nonlinearities remain unabated. A statistical digital background calibration was used to reduce the effect of the nonlinearities on ADC performance.

Another option is to replace the regular amplifiers with inverters in closed-loop operation [35, 36]. The inverter-based SC stages can operate at high speeds due to simple nature of the circuit, but parasitic capacitance and low gain necessitate cascoding to boost the gain and to isolate the parasitic capacitor of the NMOS from the feedback capacitor of the stage. In addition, auto-zeroing is required to reduce the large offset and $\frac{1}{f}$ noise, and to improve the power supply rejection ratio (PSRR).

The capacitive charge-pump based [37] gain stage avoids any active amplification, but still requires a unity-gain buffer (source-follower) to isolate the capacitors in adjacent stages. The amplification was realized by connecting two charged ca-

pacitors in series. Although the effects of parasitic capacitors on the accuracy of the amplification could be improved by careful layout, it is challenging to obtain accurate unity gain from a source-follower. Therefore, digital calibration is used to remove the effects of gain error and ensure good ADC performance.

6.2 Zero-Crossing-Based Circuits

Zero-crossing-based circuits (ZCBCs) have received a lot of attention recently due to their promise to offer a low-power alternative to the traditional amplifier-based switch-capacitor circuits. In ZCBCs, a zero-crossing detector (ZCD) and switched current sources are used to replace the power-hungry amplifier. The technique differs from the amplifier-based approach in that it detects the virtual ground condition, rather than forcing it with active feedback. The technique was presented as comparator-based switched-capacitor (CBSC) circuits in its debut [38]. It was later generalized to ZCBC when [39] was presented.

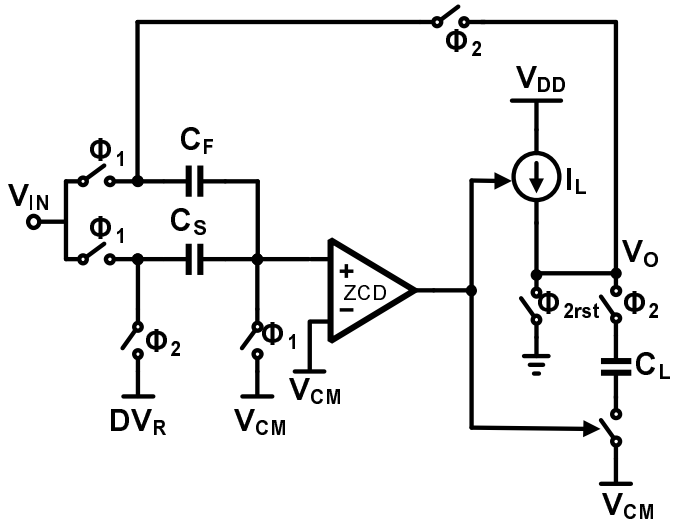

Figure 6.1: Comparator-based MDAC

An MDAC stage employing a conceptual ZCBC is shown in Fig. 6.1. The operation phases of the MDAC is similar to that of its amplifier-based counterpart. The input voltage is sampled on the capacitors, C_S and C_F, at the end of ϕ_1. C_F is flipped over for amplification in ϕ_2. The output is pulled to the lowest potential during ϕ_{2rst} to ensure the input of the ZCD starts below V_{CM}. The output node is charged up after ϕ_{2rst} goes low, charging up the virtual ground in the process. When the positive input of the ZCD crosses V_{CM}, its output flips and turns off the current source. Assuming the current source turns off the very instance the input of the ZCD crosses V_{CM}, the output of the MDAC is ideal, and can be written as

$$V_{Oideal} = \frac{C_S + C_F}{C_F} V_S - \frac{C_s}{C_f} D V_R. \tag{6.1}$$

Due to the delay of the ZCD, the current source does not turn off at the zero-crossing instant, resulting in an overshoot beyond V_{CM} and the ideal output voltage. If the time delay between the zero-crossing instant and the current source turning off is denoted as td, and the equivalent load capacitor as C_{LD}, the overshoot voltage at the ZCD input can be expressed mathematically as

$$V_{OV} = \beta \int_0^{td} \frac{I_L}{C_{LD}} \mathrm{d}t. \tag{6.2}$$

If the current source is ideal (has infinite output impedance), the ZCD delay (td) will be the same for all output voltage levels, reducing Eq. (6.2) to just and offset of magnitude $\beta(I_L td)/C_{LD}$. The offset voltage will be benign in pipelined ADCs as long as it does not saturate the current MDAC. However, for very high speed operation, the value of the current is large and may result in large enough offset to degrade the ADC performance.

6.3 Offset Compensation in ZCBCs

6.3.1 Coarse-fine charging

The overshoot after the zero-crossing could be large in the presence of long ZCD delay or large current. Small charging currents will reduce the offset voltage, but will also reduce the speed of the MDAC. One way to ensure that the offset is low without severely slowing is the charge transfer is to split the charging into two phases, each with its own current source. In the first phase, a large current is used to coarsely sweep for the zero-crossing. This leads to a large overshoot, as expected. In the second phase, a small current is used to finely sweep for the zero-crossing, resulting in a small overshoot voltage. Since the ZCD input starts very close to the threshold in the fine phase, using small charging current does not adversely affect speed.

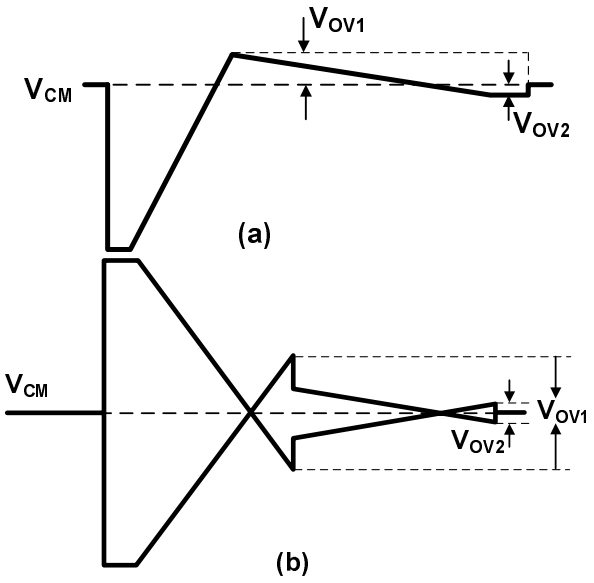

Figure 6.2: Effect of Coarse-fine on overshoot

The waveform of the ZCD input with a coarse-fine charging scheme for a

single-ended and a differential ZCBC is shown in Fig. 6.2. In Fig. 6.2(a), the overshoot at the end of the fine phase can be seen to be much smaller than in the coarse phase. Further offset suppression could achieved if the zero-crossing voltage is raised higher than V_{CM} in the fine phase [38]. However, the amount by which the zero-crossing voltage should be raised is not easily predictable. The removal of a fixed offset by changing the zero-crossing threshold is not possible in a differential ZCBC configuration. In [40], extra overshoot suppression is achieved by using capacitors to inject a corrective charge into the ZCD input at the beginning of the fine phase. The uncertainty in the amount of overshoot that will occur in the fabricated circuit also complicates the choice of the overshoot correction capacitor value, necessitating some sort of trimming or DAC.

6.3.2 Input referred offset compensation

The chopper offset estimation (COE) is a derivative of chopper stabilization developed to estimate the offset of an ADC using ZCBC [41]. Instead of using the estimated offset to cancel the ADC offset in the digital code, the estimated offset is injected back into the MDAC to correct for the ADC offset. The offset addition is done in the ZCD via digitally programmable transistors. This approach is much beneficial than the coarse-fine charging scheme, because the offset is removed from the analog signal. Thus, swing freed up by not processing the offset could be allotted to signal, increasing the SNR.

6.4 Nonlinearities in the Overshoot Error

The current source in Fig. 6.1 will not be ideal in reality. The charging current will have some dependence on the output voltage, no matter how weak. If the current source is assumed to have an output impedance R_L and a quiescent current I_0 , the overshoot voltage from Eq. (6.2) becomes

$$V_{OV} = \frac{\beta}{C_{LD}} \int_0^{td} \frac{V_{DD} - V_O}{R_L} \mathrm{d}t. \tag{6.3}$$

For any practical design, $\tau_L = R_L C_{LD} \gg td$, so Eq. (6.3) becomes

$$V_{OV} = \beta\Big(V_{DD} + R_L I_0 - V_O\Big)\Big(1 - e^{-td/\tau_L}\Big) \approx \beta\Big(V_{DD} + R_L I_0 - V_O\Big)\frac{td}{\tau_L}. \tag{6.4}$$

If the ZCD delay is constant, the overshoot error will have an offset component and a component proportional to the output voltage. The offset component is $\beta\, V_{DD}/\tau_L + \beta(I_0 td)/C_{LD}$, which is slightly more than the ideal situation. The equivalent gain error of the ZCBC MDAC, by inspection of Eq. (6.4), is $\beta\, td/\tau_L$. High current source output impedance increases the output time constant and decreases gain error. Therefore, the coarse-fine charging scheme in [38, 40] also reduces the gain error.

The ZCD delay was assumed to be constant to derive Eq. (6.4). However, the finite output impedance of the current sources varies the zero-crossing slope with the output signal of the integrator. The varying zero-crossing slope modulates the delay of the ZCD causing nonlinearities in the overshoot voltage. The charging of the ZCBC MDAC is unidirectional regardless of the polarity of the output signal, even in the differential realizations, hence both even and odd harmonics of the signal are present in the overshoot voltage.

6.5 Conceptual Zero-Crossing-Based Integrator

A conceptual diagram of the proposed zero-crossing-based integrator (ZCBI) and its timing is shown in Fig. 6.3. During the sampling phase (when ϕ_1 is high), C_S samples the input voltage V_{IN}. C_S is connected to the DAC voltage DV_R during ϕ_2. At the beginning of integration phase, ϕ_2, the output of the Integrator is reset to V_{SS} for a short period when ϕ_{2rst} is high. This causes the voltage V_X to drop below the common-mode voltage. When ϕ_{2rst} is low, the current source charges the V_X up to the common-mode voltage. The ZCD output trips when V_X crosses the common-mode voltage, and thus turns off the current source. At this instance, the output of the integrator is at the desired voltage. The previous charge stored on C_F is shared with C_S and the parasitic capacitance at the ZCD input during the reset phase. However, the shared charge is transferred back to C_F at the end of the charging phase. Thus, to avoid charge leakage, capacitors connected to C_F during the reset phase should not be switched out before the end of the virtual ground detection.

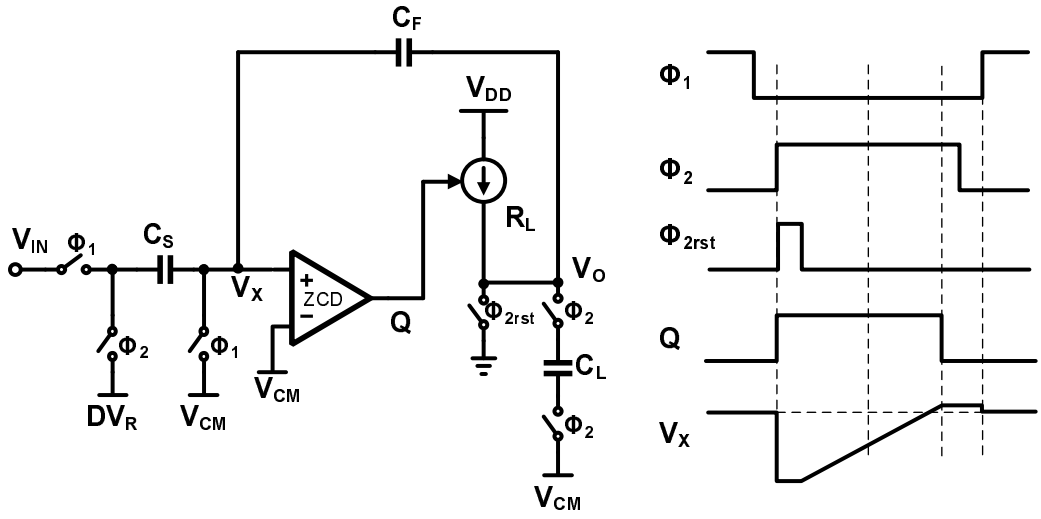

Figure 6.3: Zero-crossing-based Integrator

Due to difficulty in realizing a holding phase to transfer the integrated charge to the next stage's sampling capacitor in the ZCBI, the capacitor is connected during the integration phase (ϕ_2), realizing a half-delay integrator. The transfer function from the input to the output of the integrator, incorporating the effect of finite output impedance, becomes

$$H(z) = \frac{C_S}{C_F}\left[1 - \frac{t_d}{\tau + t_d}\right]\left[\frac{z^{\frac{-1}{2}}}{1 - \alpha z^{-1}}\right] \tag{6.5}$$

$$\alpha = 1 - \frac{(1-\beta)t_d}{\tau + t_d} \tag{6.6}$$

6.6 Multi Rate Charging Scheme

To reduce the errors caused by the overshoot voltage, a large time constant is required at the output of the integrator. However, a large time constant drastically reduces the speed at which the integrator can be operated. To overcome the speed limitation, a multiple rate charging scheme is used. Unlike the coarse-fine charging scheme in [38, 40] where the fine phase charging is in the opposite direction compared to the coarse phase charging, a unidirectional charging scheme is adopted. A high course current is used to ensure fast initial charge transfer. When V_X is a certain voltage below the common-mode voltage, a low fine current is used to make the time constant at the zero-crossing very large. To switch from the coarse to fine charging, an auxiliary ZCD is added with an in-built offset to make it trip before the main ZCD.

This charging scheme could be extended to many sections, where the largest current is used for the input signal farthest from the zero-crossing. The closer the input of the ZCD is to the zero-crossing threshold, the lower the charging current used. For each section added, an extra ZCD is required. However, the extra ZCDs

do not have stringent requirements, making the power penalty for using them low. Fig. 6.4 shows the waveforms at the ZCD input with one, two, three and five charging sections. The more the sections used, the smaller the zero-crossing current, leading to lower overshoot voltage for a given speed of operation. It could be observed from Fig. 6.4 that as the number of sections are increased, the charging approaches that of an amplifier in close loop, without the stability constraints.

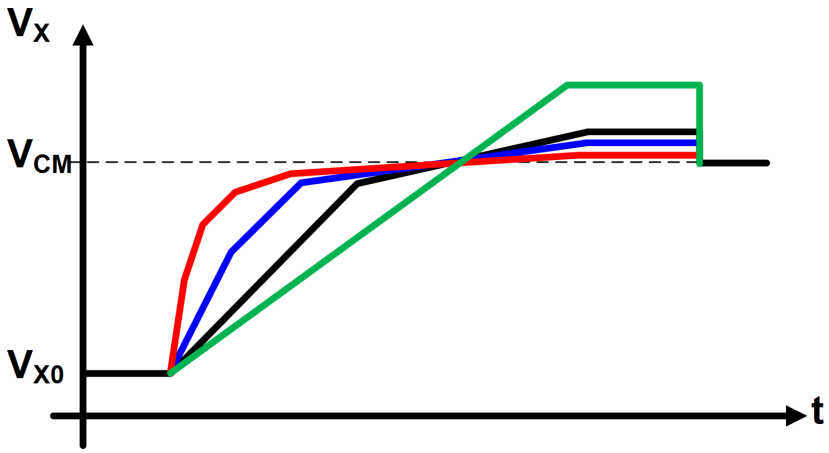

Figure 6.4: Multi-rate charging scheme

Resistors were used instead of transistor current sources to ensure that the output current changes linearly with the output voltage. This might simplify future calibration algorithms to cancel the overshoot voltage. Moreover, the integrator was designed in 45nm CMOS, where the transistor output impedance is so low that replacing the transistor current mirrors with resistors does not result in significant loss in accuracy.

For this design, a two section charging scheme was employed. The circuit realization of the scheme using a resistor current source is shown in Fig. 6.5. Here $R_A \gg R_B$. When the voltage at V_X is below the threshold of the auxiliary ZCD (V_{OC}), both resistor are turned on, causing the output current to be large. When

V_X crosses V_{OC}, R_B is switched off, leaving only R_A to slowly charge the output.

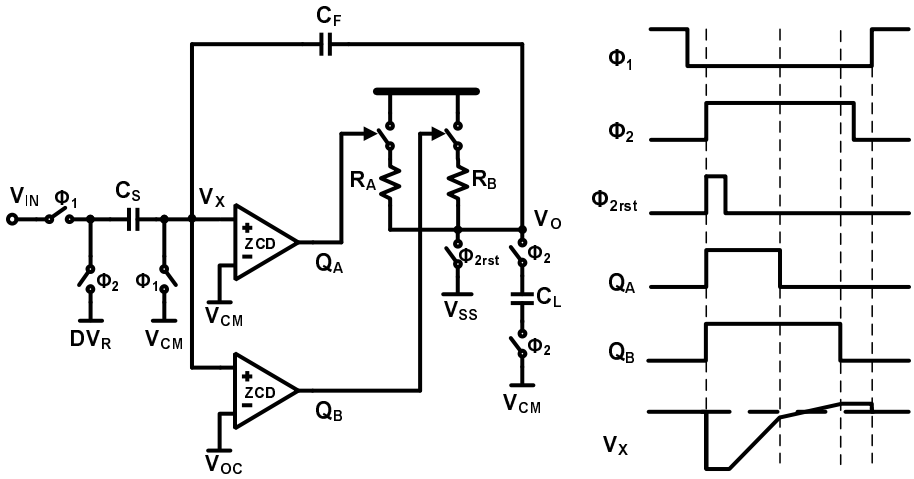

Figure 6.5: Overshoot minimized ZCB integrator

The complete zero-crossing-based integrator, along with its timing, is shown in Fig. 6.6. The same design is used in the main and auxiliary ZCD for simplicity. The auxiliary ZCD has an in-built offset to enable the dual rate charging.

6.7 Modulator Architecture

The ZCBI was used in a $\Delta\Sigma$ modulator shown in Fig. 6.7. The modulator is a second order feedforward topology with a single-bit quantizer. A passive summer is used before the quantizer since the accuracy requirement of the single-bit quantizer is relaxed enough to absorb the attenuation caused by the passive addition. Although the chosen modulator architecture is known for low distortion and low integrator swing, these benefits were forfeited when a binary quantizer was used. The binary quantizer has large quantization error that is strongly correlated to the input signal making the integrator output high and signal-dependent.

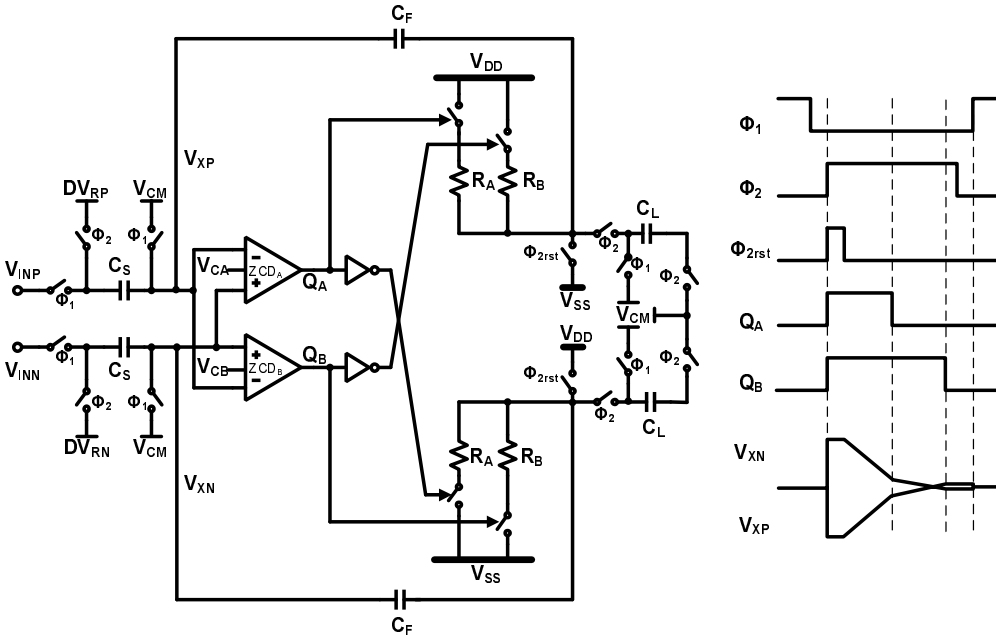

Figure 6.6: Zero-crossing-based integrator

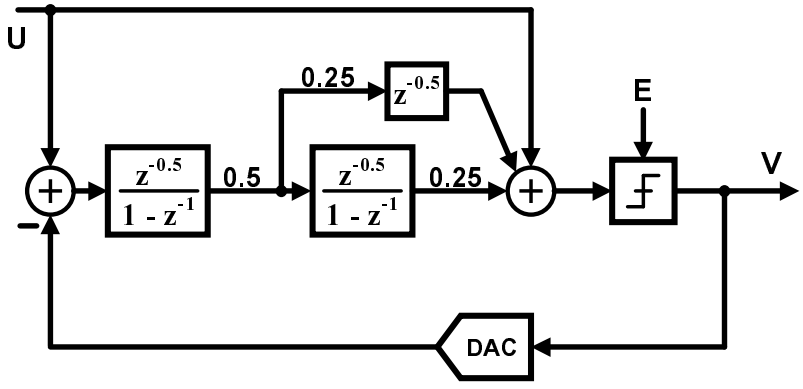

Figure 6.7: 2nd order feedforward $\Delta\Sigma$ modulator

6.8 Circuit Implementation

6.8.1 Switched Resistor Current Sources

Polysilicon resistors were used for the current sources. The unit resistors for R_A and R_B are inter-digitized in layout to improve matching. Since the voltage across the charging and discharging resistors are always the same, their currents match well, making the use of common-mode feedback circuits unnecessary. R_A is chosen to be small to quickly charge (discharge) V_{XP} (V_{XN}) initially, while the larger R_B at the end causes minimal overshoot. Also, the resistance of R_B is chosen to be comparable to the output impedance of a cascode transistor current source in 45nm CMOS to ensure comparable linearity.

6.8.2 Zero-Crossing Detector

The ZCD, shown in Fig. 6.8, is a simplified version of the comparator presented in [42] followed by inverters to give close to digital outputs. Positive feedback is used to enhance the gain of the stage ($(\frac{W}{L})_4 > (\frac{W}{L})_5$). M_3 allows adjusting offset of the ZCD. A ratio of 1 to 4 between M_3 and M_2 was observed in simulation to give the required offset in the auxiliary ZCD. The bias current is switched off when not in use (ϕ_1) to save power. The time allotted to reset at the beginning of ϕ_2 gives the ZCD ample time to fully turn on before a zero-crossing.

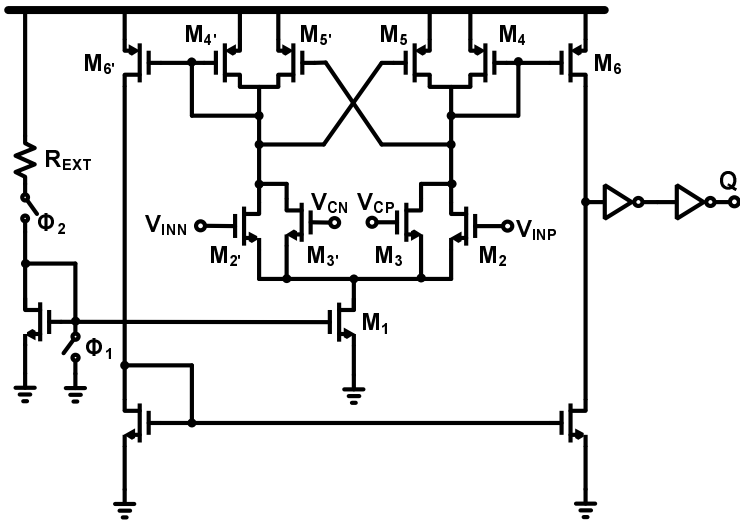

Figure 6.8: Zero-crossing detector

6.8.3 Quantizer

The quantizer is implemented as a cascade of a static preamplifer, a regenerative latch, and digital SR latch, as shown in Fig. 6.9. The first stage of Fig. 6.8 is reused as the preamp, without the offset generating transistors. The preamp buffers the integrator outputs from the latch to reduce kickback.

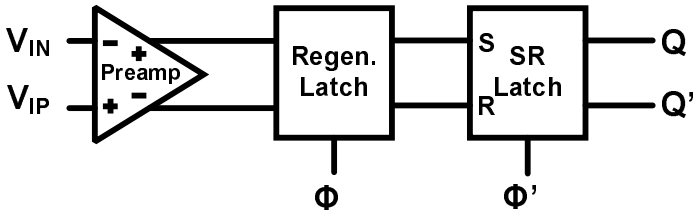

Figure 6.9: Zero-crossing detector circuit

6.8.4 Reset Pulse Generation

The short pulses needed to pull down the output of the integrator at the beginning of the charge transfer phase is generated locally using the rising edge detector shown in Fig. 6.10. The inverter delays were chosen such that the pulse width is wide enough to ensure that the input of the ZCD falls below the zero-crossing threshold.

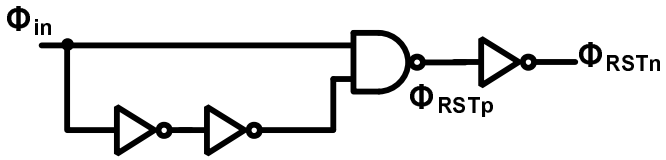

Figure 6.10: Rising-edge detector

6.9 Measurement Results

The ADC was fabricated in a 45nm LP Digital CMOS technology. The measured output spectrum of the modulator at 50MHz, 1.1V supply and 60MHz, 1.2V supply are shown in Fig. 6.11 and Fig. 6.12 respectively. The modulator has a high dc offset due to the overshoot voltage. The measured SNDR versus input signal level characteristic is shown in Fig. 6.13 for the 50 MHz case. The dynamic range is 54.3dB and the peak SNDR is 47.7dB at -3.7dBFs input level. The measured performance summary is presented in Table 6.1. The analog power is 465μW while the digital power is 165μW. The chip micrograph is shown in Fig. 6.14.

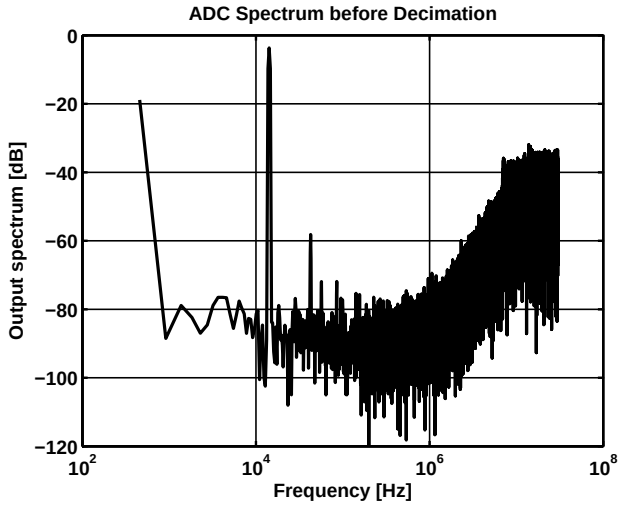

Figure 6.11: Output spectrum of modulator at 1.1V

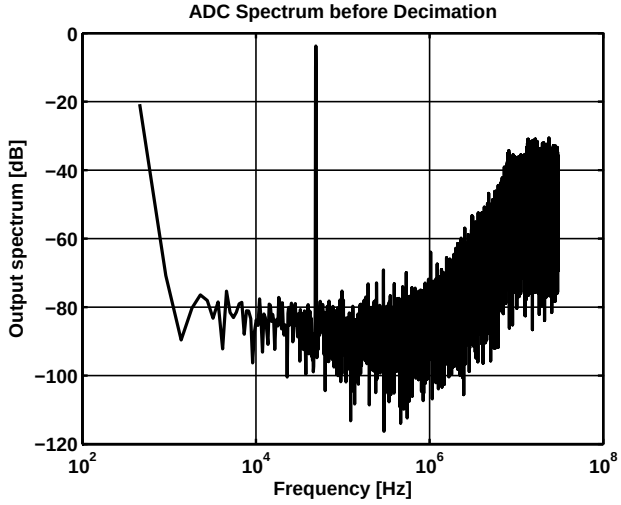

Figure 6.12: Output spectrum of modulator at 1.2V

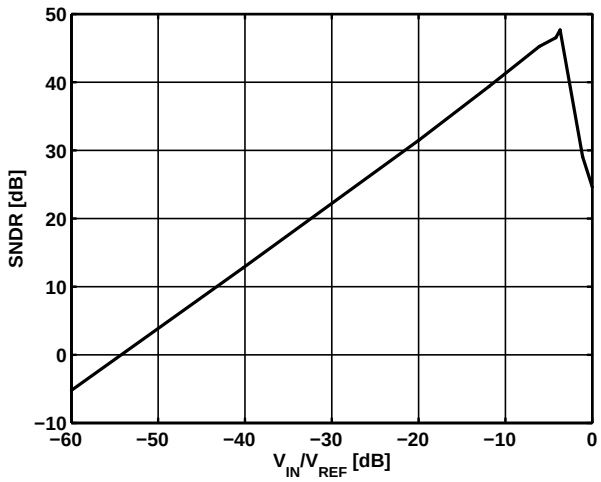

Figure 6.13: SNR vs input level at 1.1V

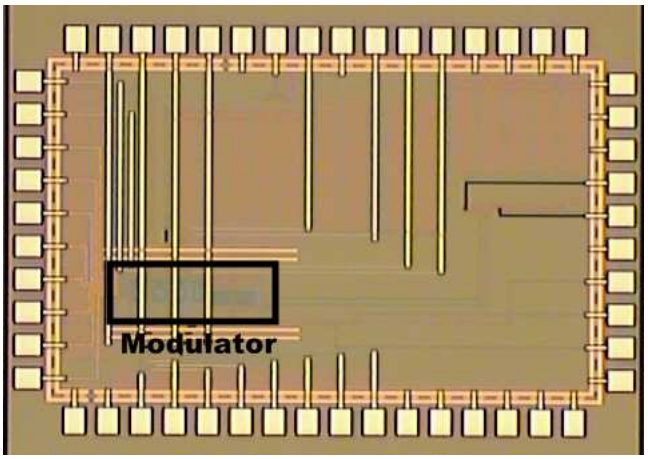

Figure 6.14: Chip micrograph

Table 6.1: Performance summary

Technology	45nm LP Digital CMOS	
Supply voltage	1.2V	**1.1V**
Signal Bandwidth	1MHz	**0.833MHz**
Clock Frequency	60MHz	**50MHz**
Oversampling ratio	30	**30**
Power consumption	1mW	**630μW**
Input range	1.2V$_{PP}$	**1.2V$_{PP}$**
Peak SNR	52.0dB	**52.5dB**
Peak SNDR	47.2dB	**47.7dB**
Dynamic range	53.0dB	**54.3dB**
Active die area	0.0448mm^2(320μm x 140μm)	

CHAPTER 7. CONCLUSION

Several low power design techniques where examined for their ability to realize high performance circuits in deep submicron technologies. New technique that improve on the shortcomings of the examined techniques are proposed. The proposed circuit design approaches involve either using very low gain and low power amplifier to realized high ADC performance or replacing the amplifier with simpler blocks to ensure low power operation. The effectiveness of the proposed techniques was demonstrated in three ADC architectures.

A pipelined ADC that achieves low power operation by using an improved Correlated Level Shifting technique was implemented in 0.18μm CMOS. The improved CLS technique allows the use of very simple op-amp with low gain without the need for calibration, thereby reducing power consumption. Relaxed trade-off between gain and speed in the pipelined stages allows the use of multi-bit per stage configuration. Simulated results show that the pipelined ADC achieves 61dB SNDR, 74dB SFDR at 50MHz while consuming 6mW from 1.2V supply.

An integrator that employs the CLS technique to improve its phase error is proposed. The integrator operation is completed in only two phases due to the leveraging of the integrator memory. Its performance is validated through the design of a 2-0 MASH modulator. Simulation results show similar gain enhancement to CDS, but without the additional thermal noise. The integrator also offers the possibility for further gain improvement.

A zero-crossing-based delta-sigma modulator was presented. The zero-crossing-based integrator uses resistor current sources and a new charging scheme to improve

the accuracy and speed of the integrator. The modulator occupies a very small area during to the minimalist approach adopted in the design. A prototype IC implementation achieved 54.3dB DR, 52.5 SNR, and 47.7dB SNDR while consuming 630μW at 1.1V supply.

CHAPTER 8. APPENDIX

Table 8.1: Gain enhancement in gain stages

Technique	**Effective Gain Error**
POG [9]	$\frac{\Delta}{1+(1+\Delta)A\beta}$
RGB [11]	$\frac{1}{(1+G_{m1}R_o)(1+G_{m2}R_o)}$
RGB [12]	$\frac{1}{(1+A_1G_{m2}R_o\beta)^2}$
CDS [16]	$\frac{1}{1+A\beta_1+A^2\beta_2}$
CDS [17]	$\frac{1}{(1+A\beta)^2}$
CDS [18, 20, 21]	$\frac{1}{(1+A\beta)(1+A\beta_I)}$
CLS [25]	$\frac{1+\lambda}{(1+A\beta)(1+A\beta+\lambda)}$

Table 8.2: Gain enhancement in integrators

Technique	**Magnitude Error**	**Phase Error**
CDS [16]	$\frac{1}{1+A\beta}$	$\frac{1-\beta}{(1+A\beta)(2+A)}$
CDS [17]	$\frac{1}{1+A\beta}$	$\frac{(1-\beta)(1-\beta_2 k)}{(1+A\beta)(1+A\beta_2)}$
CDS [19]	$\frac{1+A(\beta+\beta_1 k)}{(1+A\beta)(1+A\beta_1}$	$\frac{\beta_1(1-\beta)}{(1+A\beta)(1+A\beta_1}$
CLS [32]	$\frac{1+\lambda}{A\beta(1+\lambda+A\beta)}$	$\frac{(1+\lambda)(1-\beta)}{1+\lambda+A\beta(1+\lambda+A\beta)}$
CLS Ch. 5	$\frac{1}{1+A\beta(1+A)}$	$\frac{1-\beta}{1+A\beta(1+A)}$

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