AN ABSTRACT OF THE THESIS OF

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Abstract approved:

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Pavan Hanumolu

This undergraduate thesis provides an overview on analyzing and designing open-loop sample-and-hold (S/H) circuits. It also describes a technique used to verify functions of an S/H circuit known as beat frequency test, as well as an application of S/H circuit, a dual-slope integrating analog-to-digital (A/D) converter. The first section focuses the fundamentals of S/H circuit, its theory of operation and its deviations from the ideal response. Charge injection and bandwidth limitation are the two major problems associated with an open-loop S/H circuit. The next section explains principles behind the beat test, its system setup, and the approach for designing the S/H circuit in a beat frequency test from plotting the major design parameters. A/D converter's fundamentals are introduced, followed by a survey on the system architecture and the analog components inside a dual-slope integrating A/D converter. Computer simulations of the S/H circuits and the measured results from the fabricated monolithic S/H circuits are also presented.

Key Words: MOS sample-and-hold, beat test, dual-slope ADC

Corresponding e-mail address: yangba@onid.orst.edu

A Study of Sample-and-Hold Circuit with Application to Beat Test and Dual-Slope ADC

by

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APPROVED:

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Mentor, representing Electrical Engineering

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Committee Member, representing Electrical Engineering

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Committee Member, representing Electrical Engineering

I understand that my project will become part of the permanent collection of Oregon State University, University Honors College. My signature below authorizes release of my project to any reader upon request.

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Bangda Yang, author

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MOS Sample and Hold Fundamentals

The purpose of the sample-and-hold (S/H) circuit is to capture the input signal and store it for a period of time. The MOS S/H circuits are one of the fundamental building blocks in analog circuit design, and are used in primarily in data conversion systems because most data converters require a stable input for each conversion cycle to take place. This section focuses on the fundamentals of S/H circuit. The author first describes the ideal response of sampling circuits, alone with their limitations and deviations. Then each limitation is explored further with a single NMOS track-and-hold (T/H) circuit as an example. The techniques for reducing noise and distortion in are introduced along the way.

Ideal Sampling Response

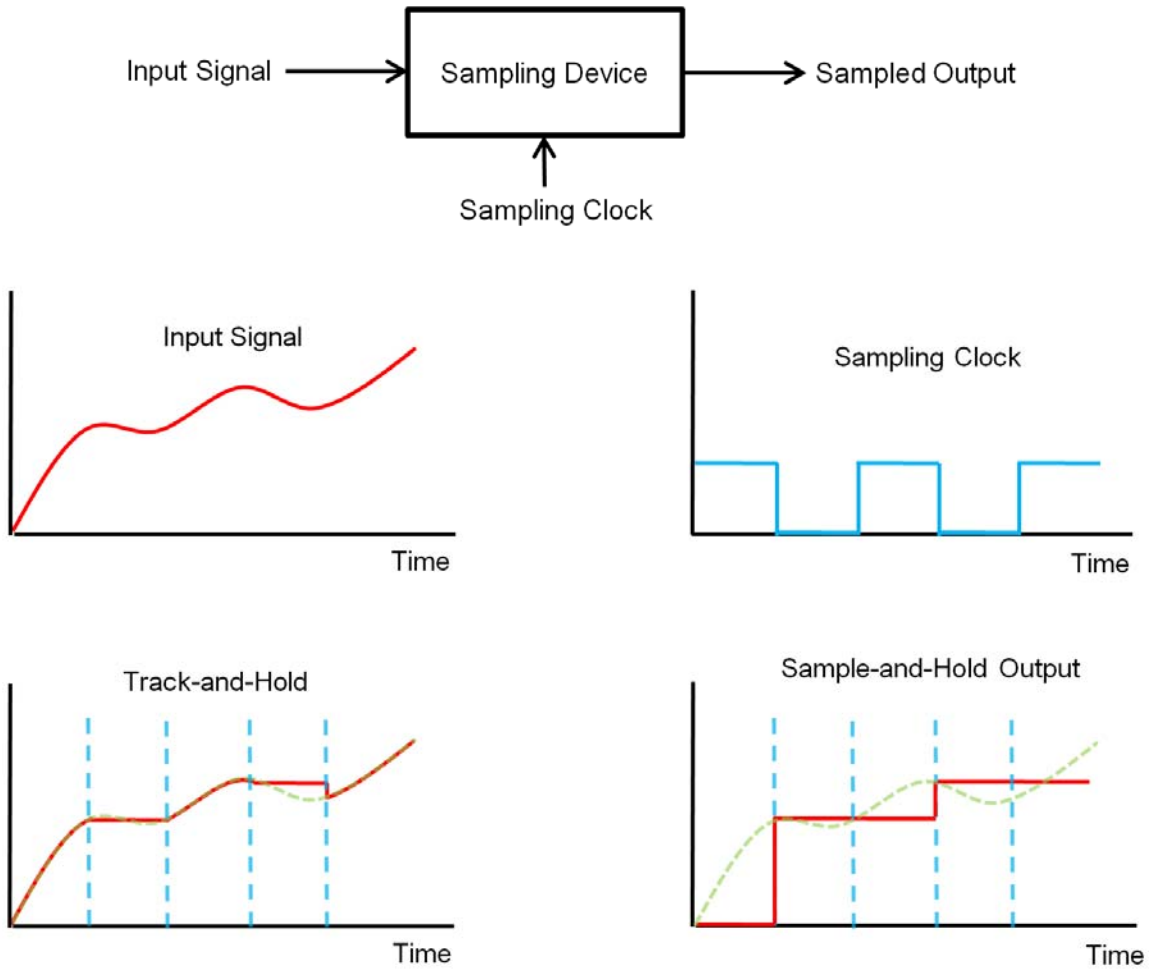

Figure 1: Ideal Sampling Response

The ideal sample-and-hold (S/H) and track-and-hold (T/H) responses are shown in Figure 1. The input signal is captured at fixed intervals and is stored for a fixed amount of time. The only difference is that the output follows input signal during the sampling state for the T/H circuit, while the S/H circuit only shows a "staircase" waveform of the sampled data. The timing for both circuits is controlled by a clock, as shown in Figure 1. For T/H circuits, the rising edges define the tracking instances, and the falling edges define the holding instances. For S/H circuits, only falling edges are required for sampling, and the sampled values are held for one clock cycle.

Deviations from Ideality

A number of limitations and uncertainties force the sampling circuit to deviate from its ideal behavior. These deviations arise from both the intrinsic device noises as well as practical circuit design limitations. The time domain response of a realistic sampling circuit is shown in Figure 2. The major performance limitations of the sampling system include pedestal error**,** bandwidth limitation, acquisition time and aperture delay, and droop rate. A frequency domain response is shown in Figure 3. Ideal sampling would create replicates of the input at each sampling frequency, but the non-idealities introduce noise and distortions that appear as phase noise and white noise in the spectrum.

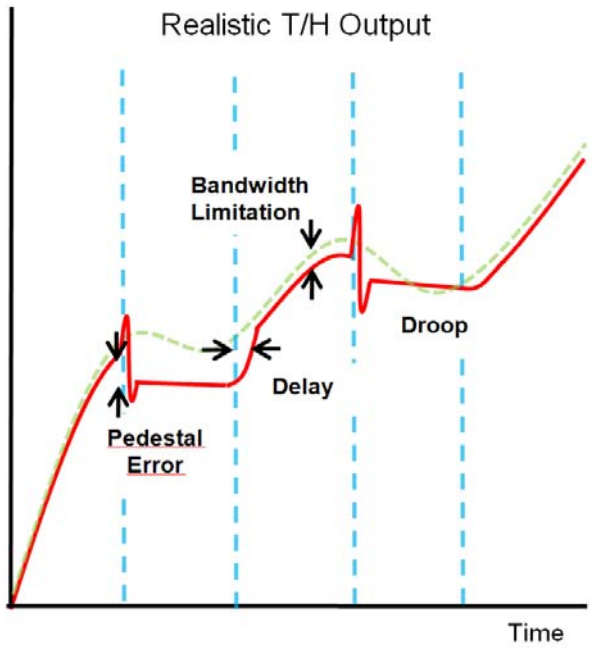

Figure 2: Realistic T/H Output

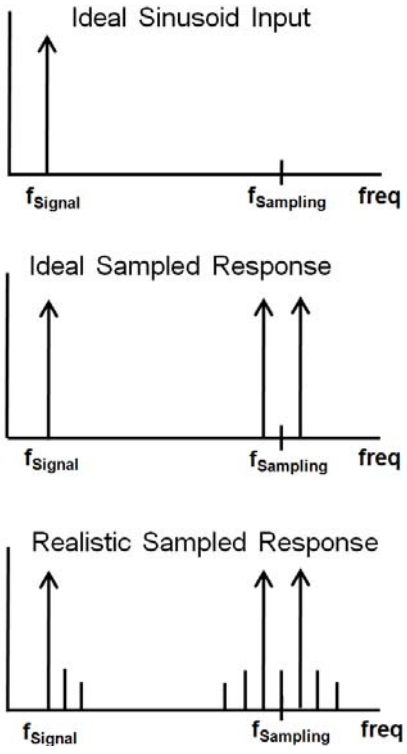

Figure 3: Frequency Domain Perspective

Single MOS Track-and-Hold Circuit

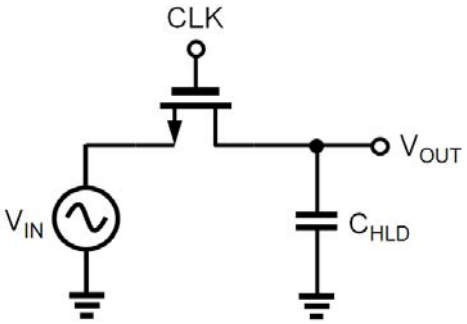

Figure 4: Single NMOS Open Loop T/H

The simplest sampling circuit is shown in Figure 4, which is composed of an n-channel MOSFET and a capacitor. Because the transistor is implemented monolithically, the source and drain are identified only by the potential difference between the two terminals. Therefore, either terminal can be used as input, with the other one being the output. The clock signal is tied to the gate, and a shunt MOS capacitor is connected at the output. Since this circuit will be fabricated in an n-well process, the bulk of the NMOS must be at the lowest potential (not shown).

This T/H circuit accomplishes sampling as follows: when the sample clock at the gate turns HIGH, the MOSFET goes into triode as long as the input is one threshold voltage below the clock. The drain-source connection of the MOSFET ideally becomes a short. Therefore the output simply follows the input. At the same time, the charges at the input flow through the MOSFET's channel onto the hold capacitor. Once the clock turns LOW, the MOSFET goes into cutoff and the drain-source connection ideally becomes an open. The capacitor will hold its value until the arrival of the next clock rising edge. The limitations introduced in the previous section forbid the sampler from this ideal behavior. Using this T/H circuit as an example, the next few sections will discuss each of these limitations in more details.

Pedestal Error

The pedestal error is the offset introduced when the sampler switches from track mode to hold mode. It is the most critical error in for the single NMOS T/H circuit, and is mainly due to MOSFET's charge injection error, capacitor kT/C noise, and the clock aperture jitter. These fluctuations cause the hold value to be different from the input value at hold instant. A great deal of attention had been paid on this subject to force the error to be signal independent [1] [2]. This is because a signal dependent offset introduces nonlinear distortion to the system. The following subsections will further analyze each of these three sources of error. For these simple analyses, the hold capacitor is assumed to be ideal and the leakage current in cutoff and through bulk is assumed to be insignificant.

Charge Injection

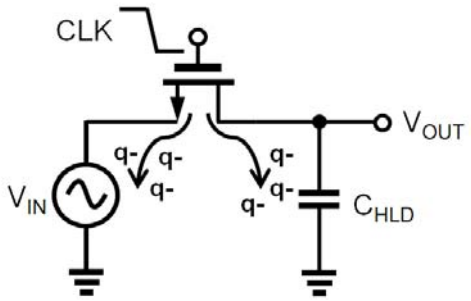

Figure 5: Charge Injection

The charge injection error is a result of the clock's falling edge. The electrical field across the oxide layer between the gate and the substrate disappears, but the charges that are still residing in the inversion channel, and are injected onto the two junctions of the MOSFET, as shown in Figure 5. For the NMOS, the minority carriers are electrons, therefore the output experiences negative glitches every time the clock turns off. The amount of charge injection is a function of the clock fall time, the impedances at the source and the drain, and the transistor size.

For fast falling edge, channel disappears quickly and there is not enough time to the charges at the source and the drain to communicate. Therefore the amount of charge injected onto each terminal approaches one half of the total channel charge independent of the output impedances [3] [4][5]. For slow clock fall time, the charges at source and drain have enough time to communicate, and the charge injected to each node depends on the impedance ratio seeing at the two nodes. According to correspondence [3] [4], the ratio of the charge injected on to the two nodes as a function of clock fall time is governed by the characteristic switching parameter χ:

$$\chi = (V_{HIGH} - V_{TE})\sqrt{\beta / (UC_L)} \tag{1}$$

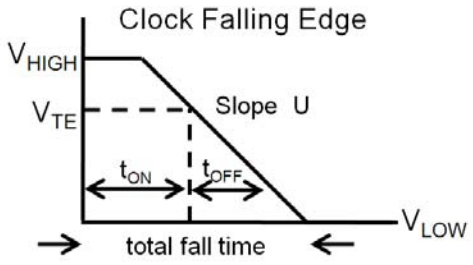

Figure 6: Clock Fall Time Diagram

where beta is given by $\beta = \mu_n C_{ox} W_{eff} / L_{eff}$ and V_{TE} is the effective threshold voltage. The symbol U represents the slope of the fall time as shown in Figure 6. To see how this parameter affects the charge injection, a test circuit shown in Figure 7 is set up for simulation. This setup allows the user to vary the input and output impedances to see their effect on the charge injection.

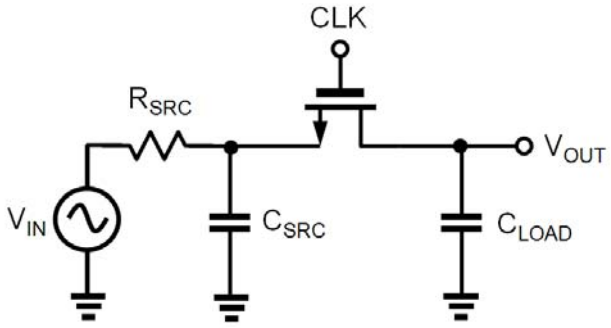

Figure 7: Charge Injection Test Circuit

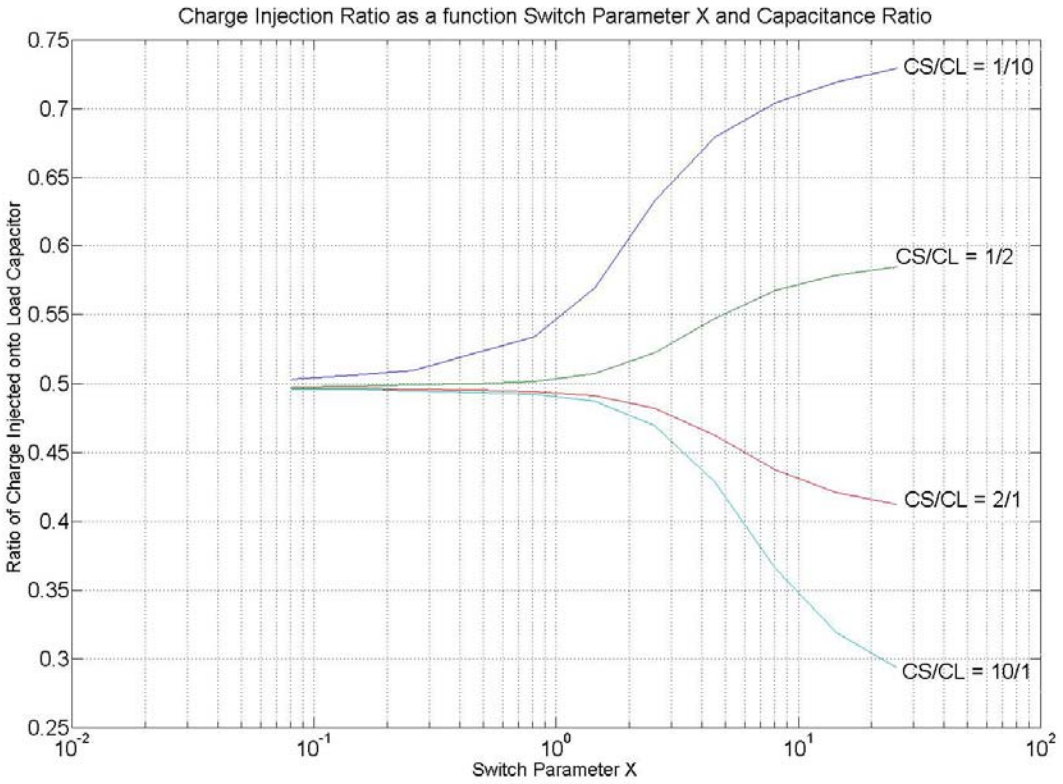

Figure 8: Charge Injection Ratio Plot

Figure 8 shows the charge injection ratio as a function of the switch parameter χ and the capacitance ratio. The simulation shows that for small χ, the amount of charge injected approaches 50% regardless of the capacitance ratio. As for slow cases, the communication between the source and the drain nodes allow the channel to equilibrate and the charges settle according to the capacitance ratio C_L/C_S. The simulation concurs with the device operation of the MOSFET. Base on the results, a few strategies can be deduced to control the amount of charge injected onto the output node. The first way is to reduce the input impedance and choose a large χ. Unfortunately, this setup also cuts down the input bandwidth. The second way is to use a clock with fast switch-off time so that approximately half of the total charge is injected onto both nodes. Then, the injected charge can be partially compensated using a half-sized dummy transistor at the output node [2][5].

There is also an additional charge injected due to the gate overlap capacitance. This phenomenon is known as clock feed-through, and can be approximated as:

$$\Delta V_{clk} \approx -\frac{C_{ox} W L_{ov} (V_{DD} - V_{SS})}{C_{hld}} \quad (2)$$

The clock feed-through depends only on the clock's signal level, and is dominated by charge injection from the inversion channel charges. However, clock feed-through takes over the overall charge injection once the clock falls below V_{TE}, during t_{OFF} phase shown in Figure 6.

To estimate the overall charge injection, equations for both fast and slow are derived from the first-order approximations. For fast case, a small χ is assumed, and 50% of the channel charge is injected onto the output:

$$\Delta V = -\frac{C_{ov}}{C_{hld}}(V_H - V_L) - \frac{1}{2}\frac{Q_{ch}}{C_{hld}} = -V_{in}(1+\varepsilon) + V_{OS} \quad (3)$$

Where $\varepsilon = \frac{1}{2}\frac{WLC_{ox}}{C_{hld}}$ and $V_{OS} = \frac{C_{ov}}{C_{hld}}(V_H - V_L) - \frac{1}{2}\frac{C_{ox}WL}{C_{hld}}(V_H - V_L)$

For slow cases the final expression is same as Equation (3) with $\varepsilon = \frac{C_{ov}}{C_{hld}}$ and

$V_{OS} = (V_{TE} - V_L)\frac{C_{ov}}{C_{hld}}$, assuming the source capacitance is zero. Equation (3) shows that the charge injection is composed of a gain error ε and an offset error V_{OS}. The non-linear V_{TE} also adds to the overall distortion. The systematic offset can be removed in most systems. However, calibration sweep is required to remap the non-linear data points. In addition, because the clock is tied directly to the power and ground rails, care must be taken to make sure that the supply noise is not being couple onto the signal.

Thermal Noise

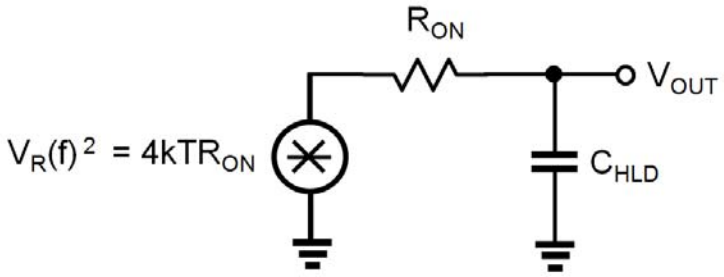

Figure 9: Thermal Noise Simplified Circuit

An ideal capacitor generates no noise since it only stores energy and no thermal energy is dissipated. However, capacitor can integrate noise generated by other source such as a resistor in series, as shown in Figure 9. The sampling MOSFET in triode region is often modeled as a resistor, which constitutes a first-order low pass filter. The noise bandwidth is given as $(\pi/2)\ f_0$ [1], where f_0 is the 3-dB cutoff frequency. The noise at the output is calculated as follows:

$$V_{no(rms)}^2 = V_R^2(f)\left(\frac{\pi}{2}\right) f_0 = (4kTR)\frac{\pi}{2}\left(\frac{1}{2\pi RC}\right) = \frac{kT}{C} \qquad (4)$$

The root-mean-squared (RMS) value of the capacitor noise stored from a resistor is equal to the square root of kT/C, also known as the kT/C noise. One important note is that the RMS value of the noise generated by the sampling circuit is independent of the resistance and the sampling frequency. A small resistance reduces noise spectral density but extends the bandwidth, and vice versa. Therefore the overall voltage noise stays constant. The independence of sampling frequency also allows the user to take large number of samples and average them to reduce the noise signal, a technique known as oversampling [1]. In short, the kT/C noise puts a lower limit on the capacitance for a given bandwidth requirement.

Aperture Jitter

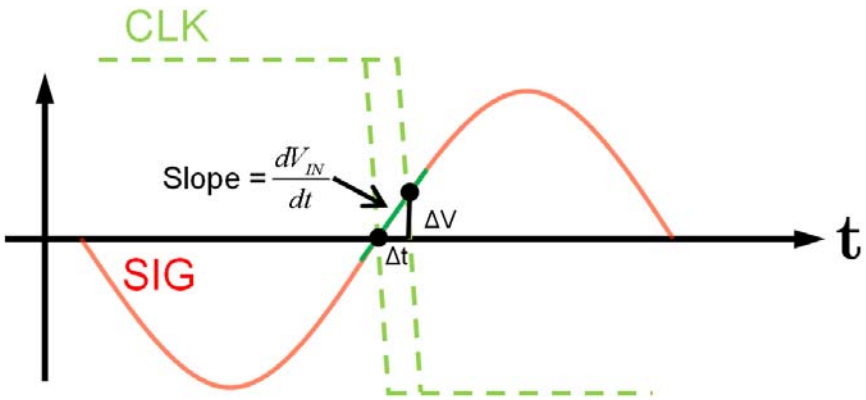

Figure 10: Sampling Sine Wave with Jitter

Aperture jitter, also known as phase noise in frequency, is the deviation of the zero-crossing point of the clock signal. This fluctuation is caused by the fundamental device noises such as thermal and flicker noise, as well as deterministic errors like coupling and interferences. The aperture jitter forces the sampler to capture a value that is different from the value sampled by an ideal clock, as shown in Figure 10. This error voltage is approximately $\Delta V = \frac{dV_{in}}{dt}\Delta t$.

For a sinusoid input $V_{in} = V_{pk}\sin(2\pi f_{in}t)$ with jitter near zero-crossing, the steepest slope that would result a maximum error is $\left.\frac{dV_{in}}{dt}\right|_{t=0} = 2\pi f_{in}$, and the error ratio turns into $\frac{\Delta V}{V_{pk}} = 2\pi f_{in}\Delta t$.

The error voltage is proportional to both the input frequency and the jitter size. Both implications make sense from the diagram. If other pedestal errors are insignificant or eliminated, then aperture jitter directly limits its resolution of a data converter To keep ΔV less than the least significant bit requires:

$$\Delta t < \frac{V_{LSB}}{\pi f_{in} V_{pk}} = \frac{1}{2^N \pi f_{in}} \qquad (5)$$

Bandwidth Limitation

Ideally, the inversion channel of the MOSFET behaves as a short during the ON state and an open during the OFF state. However, the current-voltage characteristic of MOSFET in triode exhibits a linear relationship, known as the on-resistance (R_{ON}) of a MOSFET. Together with the hold capacitance, it can be modeled as a simple lumped RC circuit and forms a first order low pass filter, which directly limits the input bandwidth of the sampling circuit.

When a MOSFET operates in the triode region, its R_{ON} mainly depends on the oxide capacitance, the size and the gate-source potential. By differentiating the first-order approximated current equation of a MOSFET in triode region, one can estimate the value of R_{ON} as:

$$R_{ON} = \frac{1}{\mu_n C_{ox}(W/L)(V_H - V_{in} - V_T)}, \text{ assuming } V_{DS} << V_{GS} \tag{6}$$

So the -3dB bandwidth is given by:

$$f_{-3dB} = \frac{1}{2\pi}\frac{1}{R_{ON}C_{HOLD}} = \frac{1}{2\pi}\frac{\mu_n C_{ox}(W/L)(V_H - V_{in} - V_T)}{C_{HOLD}} \tag{7}$$

According to the Equation (7), a lower R_{ON} can be achieved by increasing W/L ratio or the overdrive voltage. Improvements in technology such as larger oxide capacitance and smaller channel length, as well as lower threshold voltage help increase the bandwidth of the sampler. Unfortunately, the voltage rail is becoming tighter at a rate faster than the benefits, making the overall performance harder and harder to achieve. Increasing width blindly comes with unwanted parasitic such as overlap capacitance and channel charge, which causes more charge injection and clock feed-through error and tend to cancel the positive effect of having a lower R_{ON}. Even though Equation (6) shows the basic relations among the parameters, it is a crude estimation. Simulation of R_{ON} should be plotted for the actual circuit design.

Acquisition and Aperture Delay

Acquisition and aperture delays are the time required for switch to change from sample to hold and vice versa. There will always be some delay after the clock goes HIGH and before the output starts to track the input signal again, and the similar phenomenon occurs when the sampler switches from track to hold mode. These errors are mainly caused by the finite rise and fall time of the clock signal, as well as the finite time MOSFET needed to open its drain-source connection. Since only the hold values are of interest, the acquisition delay would only have a major impact on the output if it is greater than the sampling period. Aperture delay also contributes to the overall jitter error because the MOSFET turns off when the clock signal is one threshold voltage above the input voltage, instead of ideal zero-crossing point.

Droop Rate

Droop rate is the slow drop in the output voltage in the hold mode. In CMOS processes this error can often be ignored since the gate resistance is close to infinite at DC. Usually a buffer stage is also used at the output to reduce the leakage current.

Beat Frequency Test

One method of testing a S/H circuit is to use a method known as beat test. The idea of this test is to apply an input frequency to the sampler, and clock the sampler at a frequency slightly different than the input signal. Then the output is at a frequency that is the difference between the input and the clock, also known as the beat frequency. This beat signal can then be fed into a computer for analysis via a high-speed, high-resolution A/D converter and a microcontroller. This section describes one approach to design an open-loop sampling circuit when it is integrated inside a beat test. First, the sampling theory is introduced, followed by a system level overview of the beat test setup. Then the paper focuses on the design and implementation of the S/H circuit for which the beat test is used.

Equivalent-time Sampling

The technique used for beat frequency test is known as sequential equivalent-time sampling [9]. Suppose the input period is T_{INPUT}, then let the sampling period be: $T_{CLOCK} = T_{INPUT} + \Delta T$; where ΔT is a small fraction of T_{INPUT}. Figure 11 shows a diagram of the sampling process.

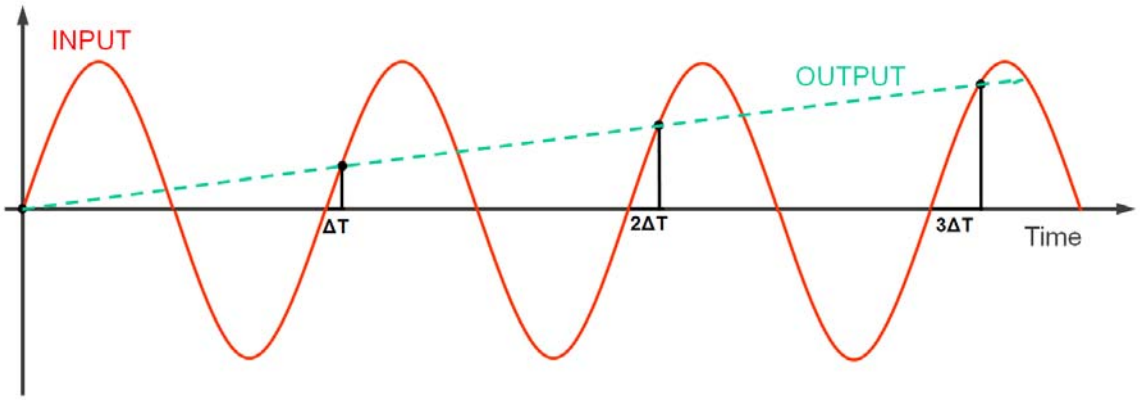

Figure 11: Equivalent Time Sampling

Every time sampling occurs, the sampling instance shifts an additional ΔT away from the beginning of each period of the input waveform. This is equivalent to sampling T_{INPUT} with a period of ΔT. Therefore, $N = T_{INPUT}/\Delta T$ number of samples occur before the output waveform, T_{OUT}, reaches one period. Because each sampling instance takes one clock period T_{CLOCK}, one period of T_{OUT} would take N numbers of T_{CLOCK}. Therefore, the relationship between input and out is:

$$T_{OUT} = N \cdot T_{CLOCK} = \frac{T_{INPUT}}{\Delta T} \cdot T_{CLOCK} = \frac{T_{INPUT} \cdot T_{CLOCK}}{T_{CLOCK} - T_{INPUT}}$$

$$f_{OUT} = \frac{1}{T_{OUT}} = \frac{T_{CLOCK} - T_{INPUT}}{T_{INPUT} \cdot T_{CLOCK}} = f_{INPUT} - f_{CLOCK} \quad (8)$$

Equation (8) confirms that output frequency is the beat between the input and the clock frequency. This technique takes the advantage of the periodic nature of the input waveform, and

does not apply to other types of functions. There are two advantages of using this sampling method. First is that the sampling speed is only required to be the same as the input, instead of the usual Nyquist sampling rate. Secondly, the demodulated output is usually an order of magnitude slower than the input while retaining the overall shape. A slower output experiences less attenuation and distortion when routed on transmission lines.

System Architecture

The system level block diagram for the beat test is shown in Figure 12. The beat frequency from the S/H circuit is feed into an A/D converter that samples the waveform at another frequency. Thus the final waveform shown on the computer also depends on A/D converter's resolution and sampling speed. A D/A converter is also added for calibrating the S/H circuit. The microcontroller serves as the interface between the test system and the computer. It also provides the sampling clocks, calibration select bit, and calibrate sweep for the D/A converter.

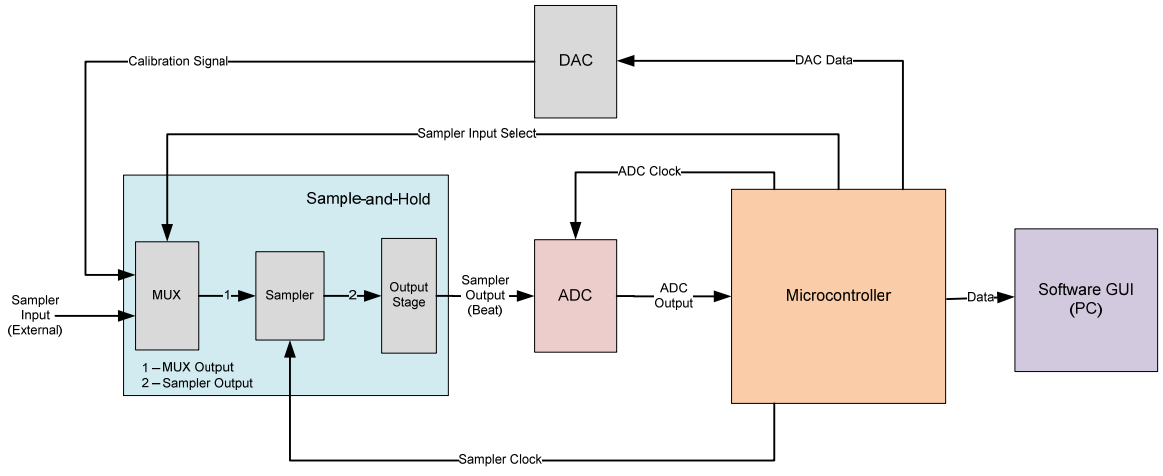

Figure 12: Beat Test System Block Diagram

Sample-and-Hold Circuit Design

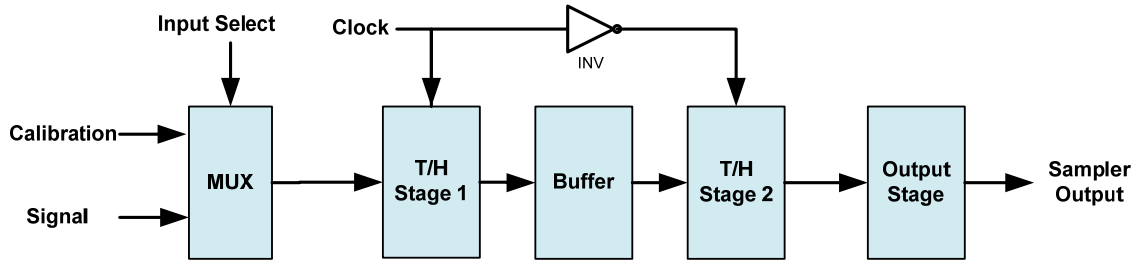

Figure 13: S/H Circuit Block Diagram

Figure 13 shows the block diagram for the S/H circuit. The multiplexer (MUX) is used to switch the input between calibration and input with a control bit. One T/H circuit sustains the sampled value only for half of one clock period. The output of an S/H circuit requires cascading a second stage as shown in Figure 13. The two T/H circuits are set up in master-slave configuration and acts as an analog flip-flop. An identical copy of the T/H circuit is put in place after the MUX for the calibration signal. A source follower buffer is added to prevent the second stage from loading the first one. The output from the second stage T/H is fed through a voltage follower before the signal is loaded onto the A/D converter.

Multiplexer

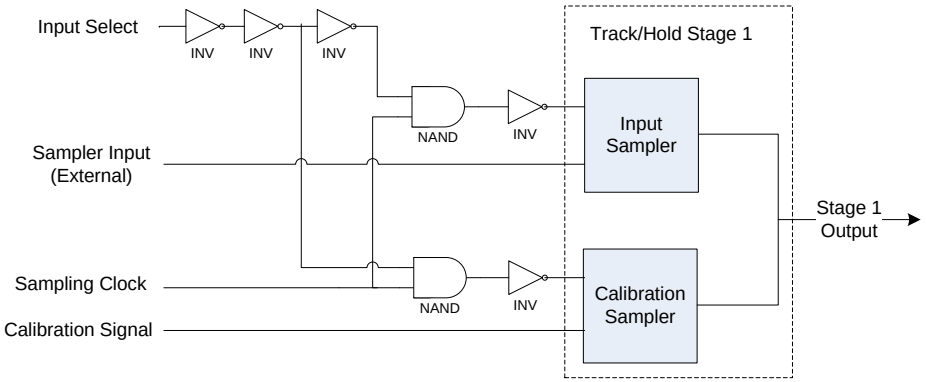

Figure 14: MUX Block Diagram

A multiplexer (MUX) is implemented inside the S/H circuit to provide a choice between the calibration and the input. Figure 15 shows the gate-level diagram of the MUX. It is implemented with standard logic gates, with a total of two NAND gates and five inverters. When the input select bit is HIGH, the sampling clock for the input signal is passed through while the calibration clock is blocked. The opposite occurs when the select bit turns LOW, thus provide the basic switching function. Figure 15 shows the transistor-level schematics for the NAND gate and the inverter implemented in most CMOS technology. The width-to-length (W/L) ratio is commonly adjusted to compensate for the carrier mobility difference between the NMOS and PMOS. The sizes also affect the rise and fall time of the clock, which is critical for charge injection error.

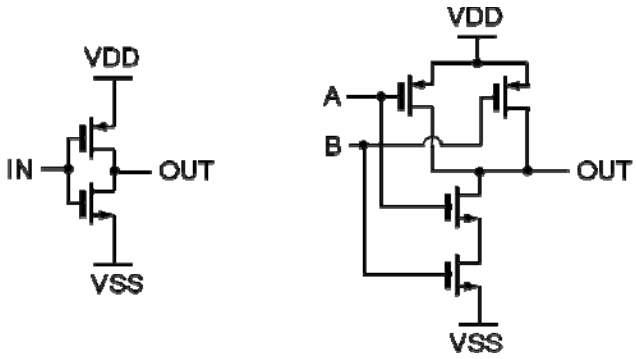

Figure 15: CMOS Implementation of the Inverter and NAND Gate

Track-and-Hold Circuit Design

From the previous discussion on the deviations caused by both the device non-idealities and the practical limitations, several design parameters must be taken into consideration. The pedestal error due to charge injection is the most critical, and the first-order low-pass filter formed by R_{ON} and the hold capacitance directly limits the input bandwidth. Therefore, the goals of designing the S/H circuit are to: 1.) minimizing the effect of charge injection, and 2.) maximize the input bandwidth

Even though understanding how these parameters affect the system are important part of the design process, the actual implementation requires specific requirements before any calculations or simulation can be done. The basic requirements are listed in Figure 16.

Specification	Value
Input Frequency	100MHz
Input Range	3.5V
Pedestal Error	-30dB

Figure 16: T/H Circuit Specifications

The goal is to design an open loop track-and-hold circuit as shown in Figure 4 that meets these specifications. The parameters on hand are the size of the MOSFET in terms of width and length, as well as the hold capacitor size. These three parameters are strong functions of each of the three major specifications. One way is to start with the kT/C noise. Even though it is small compared to the overall pedestal error, it puts a lower limit on the value of the capacitor.

Assuming the input is a sinusoid with peak-to-peak amplitude of 3.5V and centered on 1.75V, a pedestal error expressed in decibels has a equivalent

$$PE(dB) = 20\log\left(\frac{V_{n(rms)}}{V_{pk(rms)}}\right) \Rightarrow V_{n(rms)} = \frac{V_{pk(rms)}}{10^{PE(dB)/20}} \tag{9}$$

Substitute the required pedestal error into Equation (9) translate into of error voltage of 110 mV. With a room temperature of 300K, the minimum hold capacitance for the process is 15fF.

Therefore the worst case kT/C noise of is $V_{n(rms)} = \sqrt{\frac{kT}{C}} = \sqrt{\frac{(1.38\times10^{-23})(300)}{(15\times10^{-15})}} = 0.526mV$. This is much less than the 110mV total allowable pedestal error, and can be ignored in the analysis.

From the minimum capacitance, one way to design the first stage T/H is to estimate the value of the hold capacitor if charge injection was taken into account. Equation (7) can then be used to derive the maximum allowable R_{ON} for the bandwidth of interest. Then from the R_{ON}, the transistor size can be derived using Equation (6). Even though this method is straightforward, the equations assumes a square law relationship between the voltage and current, bypassing higher order effects such as the channel length variations. The equations also require estimated values for μ_n and C_{OX}, which might also be off significantly. The result would most likely be incorrect, and this guess-and-check process would go on indefinitely.

It would be much more feasible to use computer simulation to plot of the basic parameters as a function of the desired variable. To get a better sense of design trade-offs, assume a fast clock with 50% charge distribution, then the product of the approximated charge injection from Equation (3) and the 3-dB bandwidth from Equation (7) shows that:

$$\Delta V \approx \frac{C_{ox}(WL)(V_H - V_{TE})}{2C_{hld}} \qquad \text{and} \qquad \omega_{3-dB} \approx \frac{\mu_n C_{ox}(W/L)(V_H - V_{TE})}{C_{hld}}$$

$$\frac{\omega_{3-dB}}{\Delta V} = \frac{2\mu_n}{L^2} \tag{10}$$

Equation (10) shows a clear trade-off between speed and accuracy. The overall performance is limited by electron mobility and channel length. Using minimum length maximizes both speed and accuracy, and the overall performance scales roughly with the inverse of length squared. The width and the hold capacitance, on the other hand, directly compensate each other. In other words, doubling the width roughly doubles the bandwidth, but it also doubles the charge injection error. Therefore, neither the width nor the hold capacitance seems to affect the overall performance of the sampler. However, as before, the higher order effects have not been taken

into account. Since the exact effects are tedious for hand calculation, plots of channel charge, Q_{CH}, and R_{ON} as a function of width are generated. By multiplying R_{ON} by Q_{CH}:

$$R_{ON} \cdot Q_{CH} = \left(\frac{1}{\omega_{3-dB} C_{hld}} \right) \left(\Delta V \cdot 2C_{hld} \right) = \frac{2\Delta V}{\omega_{3-dB}} \tag{11}$$

The product of R_{ON} and Q_{CH} is defined by the error voltage and the 3-dB bandwidth, which is given by specifications. This is the same expression shown in Equation (10). But instead finding the theoretical maximum performance, $Q_{CH} \cdot R_{ON}$ graph can be used to find the width that is close to meeting the requirements. Figure 17 shows a plot of width vs. $Q_{CH} \cdot R_{ON}$ with minimum length. The width only starts to degrade the overall performance when it is less than 1 μm, and stays fairly independent of the overall performance beyond 3 μm, as expected.

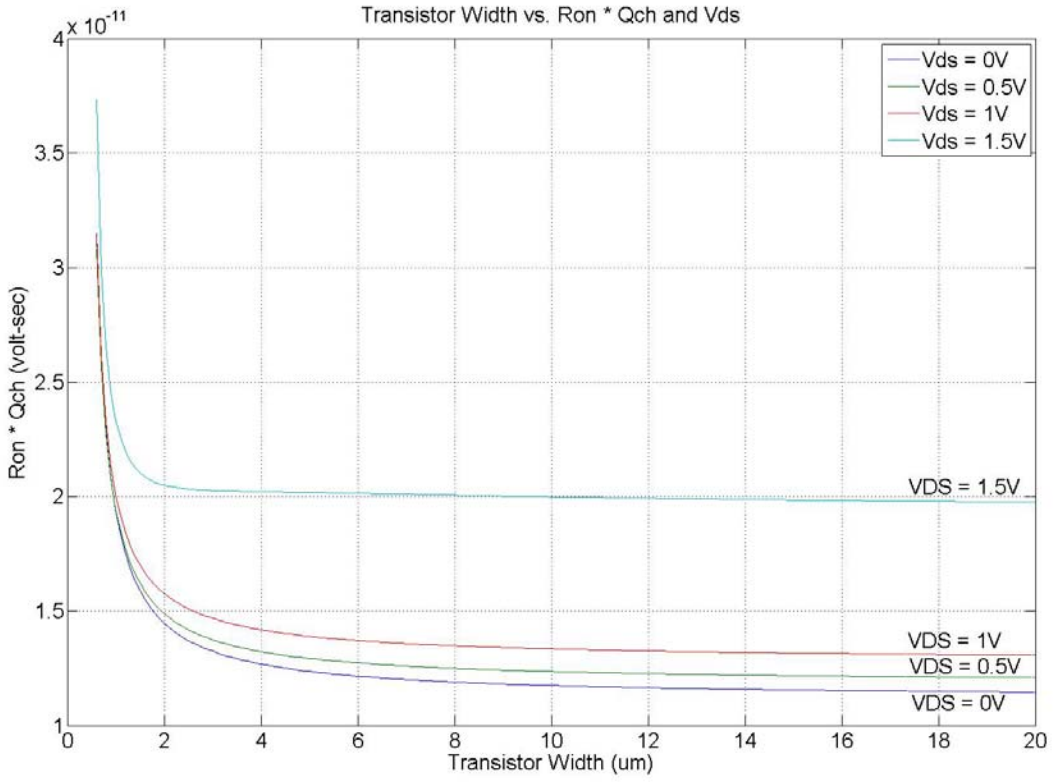

Figure 17: Performance as a Function of Width

The specified input bandwidth is 100 MHz, but a settling time is required to determine the proper cutoff frequency to avoid significant attenuation. A common time constant ratio is seven, or $T_{IN} = 7\tau_{3\text{-dB}}$, which result an error of 0.1% for RC charging functions. Therefore, the required bandwidth for the first stage track-and-hold is:

$$\frac{T_{IN}}{\tau_{3-dB}} = \frac{1}{2 \cdot f_{IN}} \Rightarrow f_{3-dB} = \frac{(T_{IN} / \tau_{3-dB}) f_{in}}{\pi} = \frac{7(100MHz)}{\pi} > 223MHz \qquad (12)$$

A 3-dB bandwidth of 300MHz is chosen is ensure that the dynamic settling error is less than 0.1% for 100 MHz input signal. The bandwidth of the second stage can be much lower because it only sees the sampled value from the first stage, with a beat frequency that is usually an order of magnitude slower than the input.

Dummy Transistor Compensation

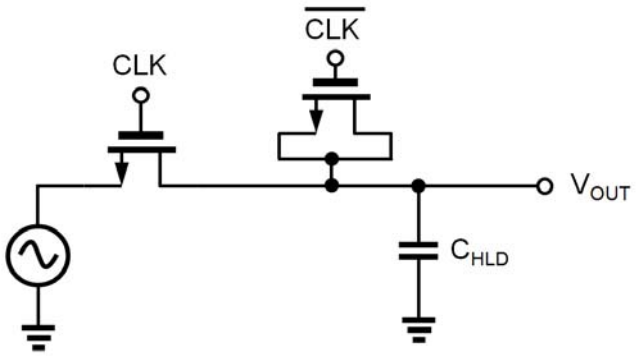

Figure 18: Dummy Transistor Implementation

The amount of charge injected is a strong function of the node impedances, the fall time of the clock and the transistor parameters. As mentioned earlier, one approach to reduce the amount of charge injection is to use a fast clock so that 50% of the channel charge is dumped to both terminals. Then output is attached with a half-sized dummy MOSFET to compensate the injected

charge, as shown in Figure 18. By shorting the drain and the source together, the dummy does not modify the signal when the clock is at steady state. The gate of the dummy is tied to a complementary clock so that when the sampling MOSFET experiences a falling edge, the dummy will experience a rising edge and will partially cancel charges that are injected to the output. Theoretically it would cancel all the injected charge. But this is not possible in practical implementation because the variations in the clock rise and fall times, the large difference in the drain and source impedances as well as the mismatches in transistor sizes.

Buffer Stage

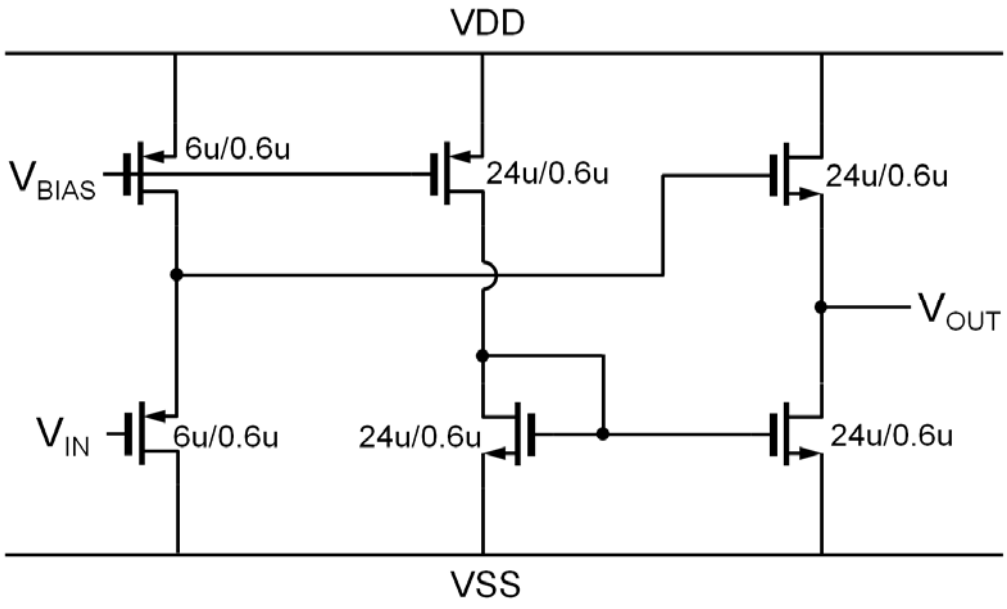

Figure 19: Source Follower Schematic

One problem with two T/H circuits connected directly is the sharing of the charges between the two hold capacitors. Even if clock at the first stage turns ON at the exact time when the second stage turns OFF, there would still be a loading effect on the first stage, and the hold value would

start to droop. This problem reduces the input bandwidth and introduces distortion. A buffer stage is added to isolate the two stages.

The buffer stage shown in Figure 19 uses two sets of NMOS and PMOS configured as source followers. It has a bandwidth off over 300MHz for a 500f load to match the bandwidth of the first T/H stage. The PMOS at the input level shift up by one threshold voltage, and subsequently shifts down by the NMOS. There offset error from the difference in threshold voltages between the NMOS and PMOS can be partially eliminated through calibration.

Output Stage

The output stage consists of a two-stage, single-ended OPAMP with a DC gain of 60dB, a 10MHz unity gain bandwidth, and a phase margin of 70˚ for load capacitance of 25pF. Figure 20 shows the schematic of OPAMP. It is configured in a unity-gain feedback to buffer the output.

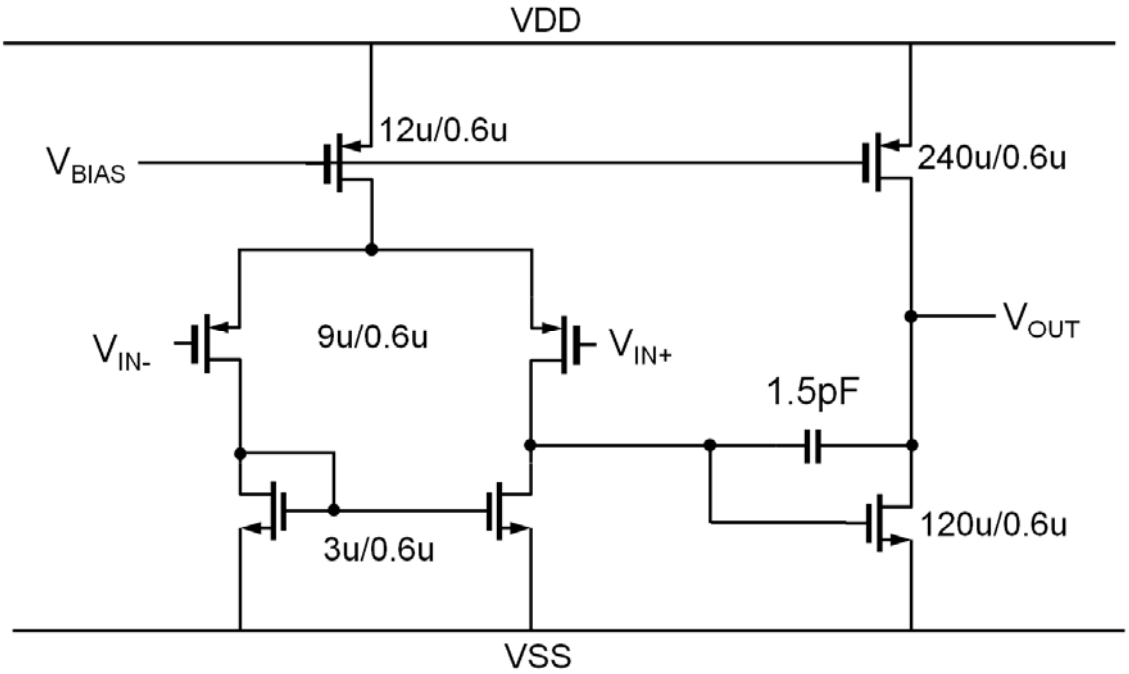

Figure 20: Two-stage OPAMP schematic

The design starts with frequency requirements. Using dominate-pole approximation, the unity gain bandwidth and phase margin determine the trans-conductance, g_m, of the two stages:

First push out the right half-plane zero by setting $\left|\frac{z}{\omega_{UGB}}\right| = \frac{g_{m2}}{g_{m1}} = 40$. Since $\left|\frac{P_2}{\omega_{UGB}}\right| \approx \frac{g_{m2}}{g_{m1}}\frac{C_C}{C_L}$, for a phase margin of 70°, $\left|\frac{P_2}{\omega_{UGB}}\right| \approx \frac{1}{\tan(90^\circ - PM)} = 2.75$ makes $\frac{C_C}{C_L} \approx \frac{1}{15}$. This forces the second pole to be the main contributor of the phase shift around unity gain bandwidth since $\left|\frac{z}{\omega_{UGB}}\right| \gg \left|\frac{P_2}{\omega_{UGB}}\right|$.

The value g_{m2} is then solved with the load capacitance since $P_2 \approx \frac{g_{m2}}{C_L}$. Once g_m's of the two stages are known, a value for the overdrive voltage can be derived from output swing, which is then used to determine the current through both stages. The gain is relatively easy to achieve, therefore minimum lengths are used to boost frequency responses.

The second purpose of the output stage is the filtering of high frequency switching noise beyond 10MHz, because the frequency component beyond the fundamental beat frequency of interest is attenuated by the OPAMP. This simple method of eliminating large switching noises though OPAMP bandwidth is sufficient since the output of the beat test is sampled by another A/D converter and functionality is eventually checked by visual inspection with a computer.

Dual Slope Integrating ADC

One application of S/H circuits is in data converters, which allow modern day electronic systems to interact with the real-world signals. The A/D conversion is done in two steps: the sampling of the input waveform in time from continuous to discrete, and the subsequent quantization of the data from continuous to discrete. The S/H circuit accomplishes the sampling, and the quantization is done in a variety of techniques including successive approximation, interpolating, and flash. A dual-slope integrating A/D converter is used as an example for its relative simple operation and small amount of circuitry required. The design consideration of the sampling circuit is introduced, followed by a description of the working principles behind the dual-slope A/D converter.

Ideal A/D Converter Response

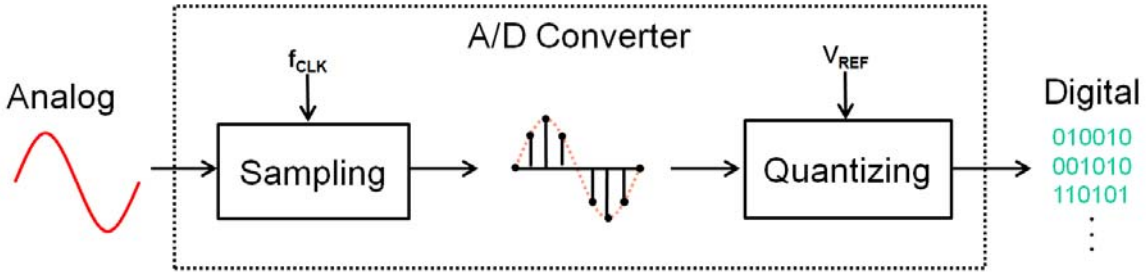

Figure 21: A/D Converter as a block

An analog-to-digital converter takes in a continuous analog value and translates it into a set of discrete levels. Figure 21 shows a black box view of an A/D converter. The input to the system is an analog voltage, and the output is the digital representation of the input V_{IN} as a fraction of the reference voltage, V_{REF}. The ideal response of an ideal 2-bit A/D converter transfer function is plotted in Figure 22. For a 2-bit converter, the output is quantized into $2^N = 4$ digital levels. Since a finite number of levels are used represent an infinite number of input levels, an error known as quantization noise is present even inside an ideal A/D converter. Therefore, the output can be expressed as $B_{OUT} = \frac{V_{IN} + V_E}{V_{REF}}$ where B is the digital output V_E is the error voltage.

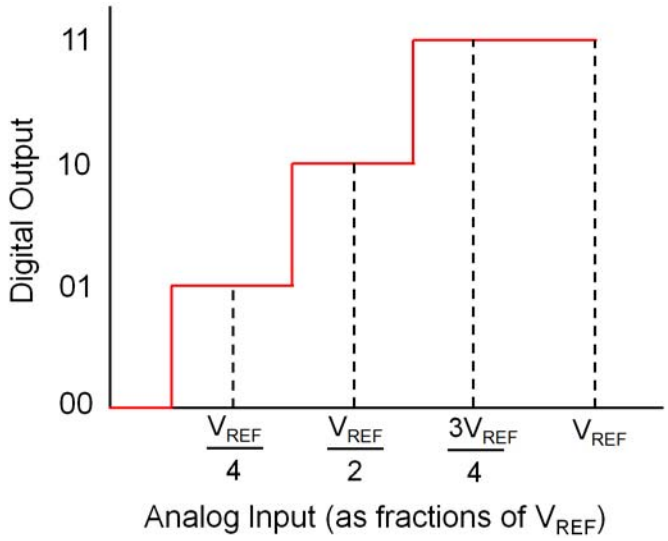

Figure 22: Ideal 2-bit A/D Converter Transfer Function

Quantization noise is usually expressed as the number of least significant bits (LSBs), or $V_{LSB} = \frac{V_{REF}}{2^N}$. Assuming V_{REF} is 4V, and then V_{LSB} equals 1V for the 2-bit converter. Note that Figure 22 shows that input has a ½V_{LSB} (0.5V) offset from the case where each transition occurs at the V_{LSB} (1V). In other words, the output '00' changes to "01" at 0.5V instead of 1V, "01" to "10" at 3/2 V_{LSB} instead of 2 V_{LSB}, and so on. This way the maximum quantization error is bounded by ½V_{LSB} instead of 1V_{LSB}. The down side is that the last transition occurs 3/2 V_{LSB} away from V_{REF}, for which the quantization error exceeds the ½V_{LSB} bound.

Assuming a rapid changing input signal that results a randomly distributed quantization error between -½V_{LSB} and ½V_{LSB}, the output can be modeled as the input plus the quantization noise. Then the RMS value of the quantization noise is given in [1] as:

$$V_{Q(rms)} = \left[\int_{-\infty}^{\infty} x^2 f_e(x) dx \right]^{1/2} = \frac{1}{V_{LSB}} \left[\int_{-\frac{1}{2}V_{LSB}}^{\frac{1}{2}V_{LSB}} x^2 dx \right]^{1/2} = \frac{V_{LSB}}{\sqrt{12}} \qquad (13)$$

Equation (13) shows that quantization error is directly related to V_{LSB}. Since V_{LSB} is related with N and V_{REF}, each additional quantization level reduces quantization noise by 6dB, assuming no other noise is present. Another noise indication is the signal-to-noise ratio (SNR) defined as the ratio of input signal power to output noise power. The SNR for a sinusoid input between 0 and V_{PK} due to quantization noise is:

$$SNR = 10 \log \frac{P_{in(rms)}}{P_{Q(rms)}} = 20 \log \frac{V_{PK} / (2\sqrt{2})}{V_{LSB} / \sqrt{12}} = 6.02N + 1.76dB \qquad (14)$$

Expression (14) shows that sinusoid has 1.76dB more signal power than random signal. This is also the best possible SNR since any reduction in signal amplitude reduces signal power.

A/D Converter Limitations

Similar to charge injection error in S/H circuits, the A/D converter's non-idealities can be expressed as offset error and gain error, as shown in Figure 23. The offset error is defined as the deviation of the first output transition from ½ LSB. Gain error is caused by the deviation of the slopes between the ideal and actual transfer curves when the offset error is reduced to zero. For A/D converters, the gain error is defined by the difference between the transitions to full scale.

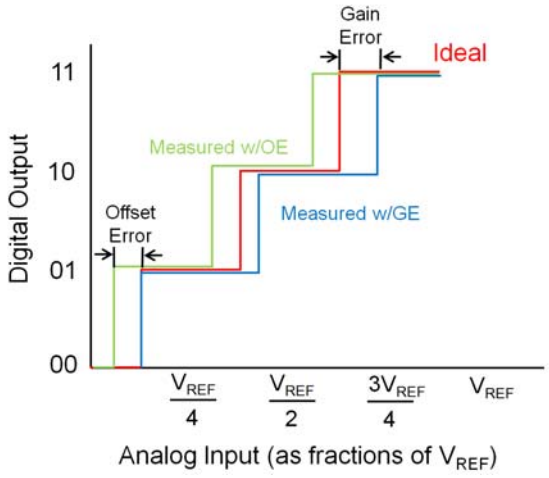

Figure 23: Offset and Gain Error

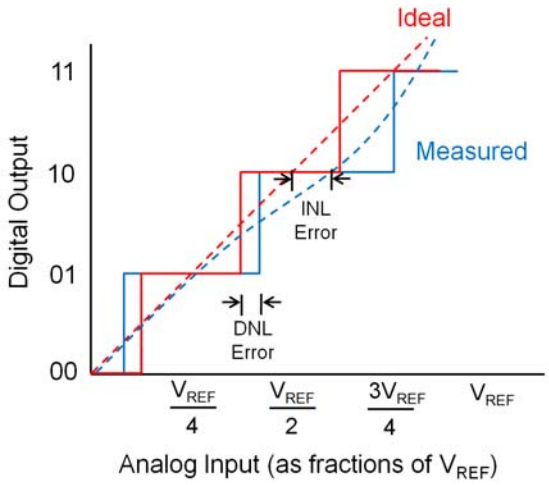

Figure 24: INL and DNL

The accuracy of an A/D converter depends on its offset and gain errors, as well as its linearity. The common measure of linearity include integral nonlinearity (INL), which is the deviation of any code transitions from straight line drawn from zero scale to ½ LSB more than the last transition, and differential nonlinearity (DNL), defined as the difference between the actual transition step size from 1 LSB. Both are illustrated in Figure 24. A DNL of more than 1 LSB has a possibility of missing code, when no value of input will result an output level.

Dual Slope A/D Converter Fundamentals

A dual-slope A/D converter is one type of integrating converters that provide high accuracy and very slow input bandwidth. These data converters have very small offset and gain error, and are highly linear [1]. Another reason for choosing this type of converter as an example application of S/H circuit is the small number of required components and the simple theory of operations. For these reasons, dual slope and other integrating A/D converters are primarily used in measurement instruments such as multi-meters.

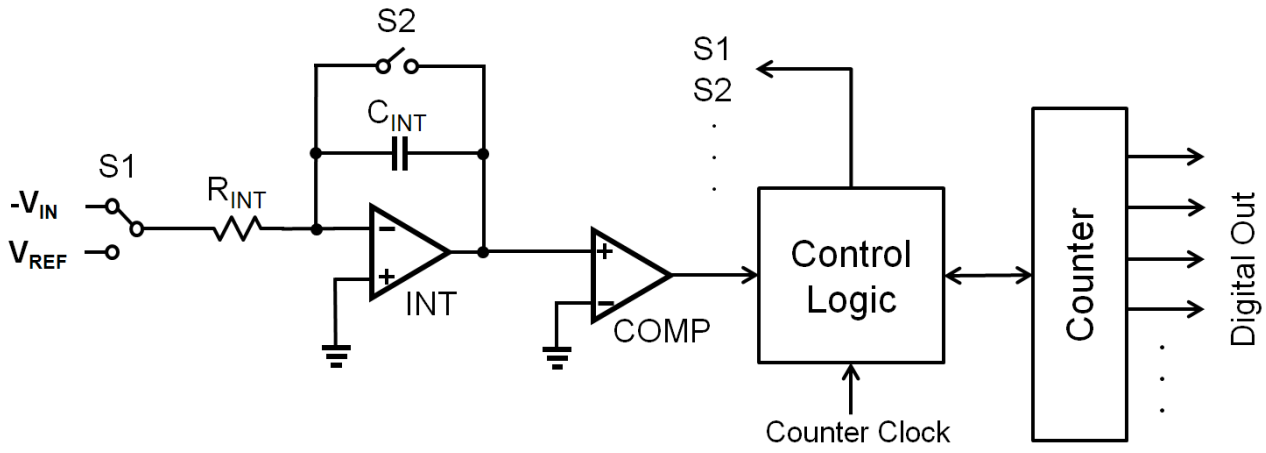

Figure 25: Dual Slope A/D Converter Block Diagram

Figure 25 shows a block diagram of the dual slope A/D converter. The analog side consists of an OPAMP configured as an inverting integrator followed by a comparator. The digital domain contains the control logic for two switches, a clock and a counter, all of which can be provided with a microcontroller. The capacitor and resistor are used to set the time constant for the integrator, and the switches are used for multiplexing the inputs and to discharge the capacitor. The quantization is accomplished in two steps. First switch S_1 shorts $-V_{IN}$ so the output of the integrator, V_X, ramps up for T_1 amount of time. Then S_1 switches to V_{REF} and V_X ramps down with a constant slope until the output reaches the starting point, as shown in Figure 26. The ramp

up time, T_1, is usually set by running a counter for a full scale of 2^N cycles, or $T_1 = 2^N T_{CLK}$.

Assuming a constant input $-V_{IN}$ with an ideal integrator, at the end of the first phase:

$$V_X(T_1) = -\int_0^{T_1} \frac{V_{IN}}{R_{INT}C_{INT}}\,dt = \frac{V_{IN}T_1}{R_{INT}C_{INT}} \tag{15}$$

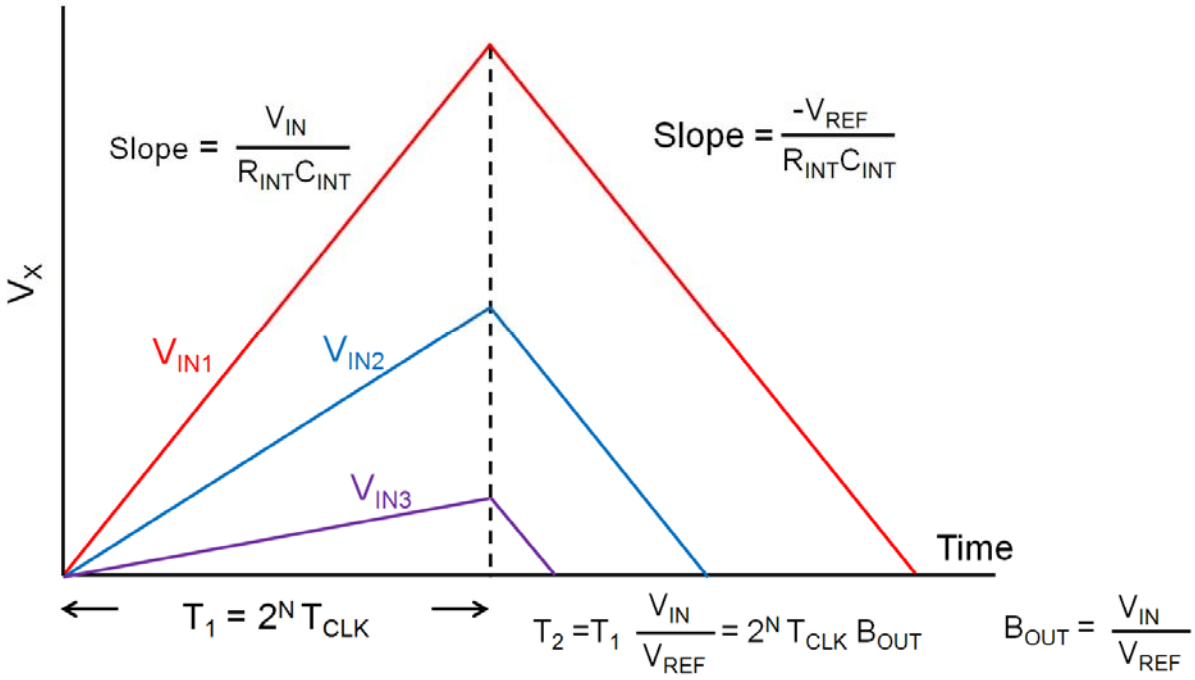

Figure 26: Dual Slope Integration Diagram

During the second phase, the input to the integrator is set to V_{REF}. So V_X ramps down with a constant phase until it reaches the starting point of the first phase, and the comparator triggers.

The length of the downward ramp is T_2, and $V_X(t) = -\int_{T_1}^{t} \frac{V_{REF}}{R_{INT}C_{INT}}\,dt + V_X(T_1)$

When $t = T_1 + T_2$, $V_X = 0$ and: $-\frac{V_{REF}T_2}{R_{INT}C_{INT}} = \frac{V_{IN}T_1}{R_{INT}C_{INT}} \Rightarrow T_2 = T_1\left(\frac{V_{IN}}{V_{REF}}\right)$ (16)

Since $T_2 = 2^N T_{CLK} B_{OUT}$ and $T_1 = 2^N T_{CLK}$, substituting both expressions into Equation (16):

$$B_{OUT} = \frac{V_{IN}}{V_{REF}} \tag{17}$$

B_{OUT} is the normalized binary count of T_{CLK}, and it is independent of the integrating capacitance and resistance. This lessens the drift problem in the single slope A/D converter for which the slope of the ramp starts to misalign with T_{CLK} due to variations in resistance and capacitance. However, proper RC time constant needs to be chosen so that V_X is maximized to increase the signal-to-noise ratio. It is easy to see why input bandwidth is low. For the maximum value of V_{IN}, both T_1 and T_2 run for full scale of 2^N cycles. Therefore, a 10 bit converter clocking at 1MHz, the worst case conversion speed is approximately $\frac{f_{CLK}}{2 \cdot 2^N} = \frac{1MHz}{2048} = 488Hz$.

Another feature of the dual slope A/D converter is the suppression of the harmonics base on the value of T_1. If the first phase last exactly T_1, then multiple harmonics of is theoretically rejected. To see this, assuming a sinusoid input with a noise harmonic at $1/T_1$, the input can be written as $V_{IN} = V_{SIGNAL} + V_{NOISE(1/T_1)}$. The ramp up phase shows that $V_X(T_1) = -\int_0^{T_1} \frac{V_{SIGNAL}}{R_{INT}C_{INT}} dt - \int_0^{T_1} \frac{V_{NOISE(50Hz)}}{R_{INT}C_{INT}} dt$,

where $\int_0^{T_1} \frac{V_{NOISE(50Hz)}}{R_{INT}C_{INT}} dt = \int_0^{T_1} \frac{\sin(2\pi / T_1)}{R_{INT}C_{INT}} dt = \frac{1}{R_{INT}C_{INT}} \left| \cos\left(\frac{2\pi}{T_1} t\right) \right|_0^{T_1} = 0$. The elimination also makes sense from the frequency perspective. The constant ramping up and down corresponds to an impulse response of a square wave. This type of impulse response translates into a sinc function given by $|H(s)| = \left| \frac{\sin(\pi T_1 f)}{\pi T_1 f} \right|$ in the frequency domain that suppresses multiple harmonics of $1/T_1$ as well as a single pole roll-off for all the higher frequencies. In practice the amount of rejection is limited by the performance of the integrator such as its finite gain, slew rate and output swing.

Dual Slope A/D Converter System Design

Designing a dual slope A/D converter at the system level is straightforward. One can start out with the frequency desired to be suppressed by choosing the length of the first phase, T_1. For industrial applications, the line frequency (50Hz/60Hz) is often chosen. This gives a T_1 value of 1/60Hz, or 16.7ms. This also gives a conversion rate of $1 / (2T_1) = 30Hz$. To achieve a 10-bit resolution, the required clock frequency is $f_{CLK} = \frac{1}{T_{CLK}} = \frac{2^N}{T_1} = \frac{2^{10}}{16.7ms} = 61.3kHz$ assuming T_1 runs the full binary scale. If the clock frequency is given beforehand, then integration cycle can be altered to match T_1. But the output B_{OUT} also needs to be adjusted. The value of the RC time constant is calculated base on the desired values for V_X and V_{REF}. For a single supply of 5V, 2.5V can be used as the virtual ground. Assuming the OPAMP operates up to 0.5V from the rails, the input range is between 2.5V and 4.5V. The V_X is set to –2V because the integrator is inverting, meaning a DC input of 4.5V drives the output to ramp from 2.5V to 0.5V. From Equation (15): $\tau = -\frac{T_1 V_{IN(\max)}}{V_{X(\max)}} = -\frac{(16.7ms)(2V)}{-2V} = 16.7ms$. The individual values of R and C are then found base on the load capacity of the integrator. For example, a 10nF capacitor requires a resistance of 1.67MΩ. If the integrator is fabricated monolithically, the passives are usually brought off-chip to conserve die area and allow for easy adjustment, shown in Figure 27.

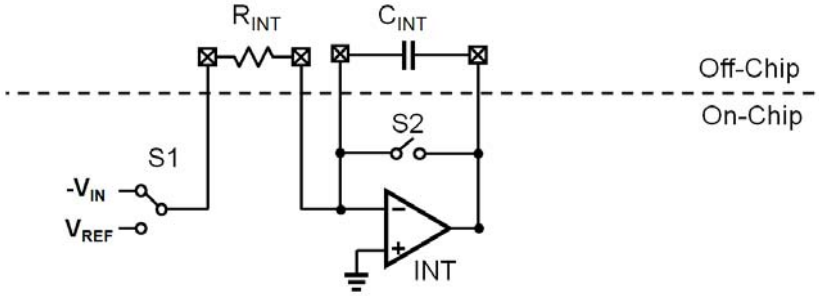

Figure 27: Off-Chip Implementation

Integrator and Comparator

One way to implement the integrator and the comparator is using OPAMPs. Since the input is slow and the resolution is medium, the OPAMP is expected to have high gain, high output swing, and low bandwidth. With a 10-bit resolution and a V_{REF} of 2V, the OPAMP with a minimum gain of 70dB is required to resolve a half LSB of 0.976mV. Figure 28 shows one implementation of an OPAMP. It has a DC gain of at least 80dB from 0.5V to 4.5V. The loop gain of the OPAMP varies during the integration phases, but the worst-case open loop unity gain bandwidth gives a phase margin of 70°. This OPAMP is used for both the integrator and the comparator. Since the comparator is in open loop configuration, no compensation capacitor is required. Omitting the compensation capacitor maximizes the first pole and makes input capacitance of next stage the determining factor for slew rate.

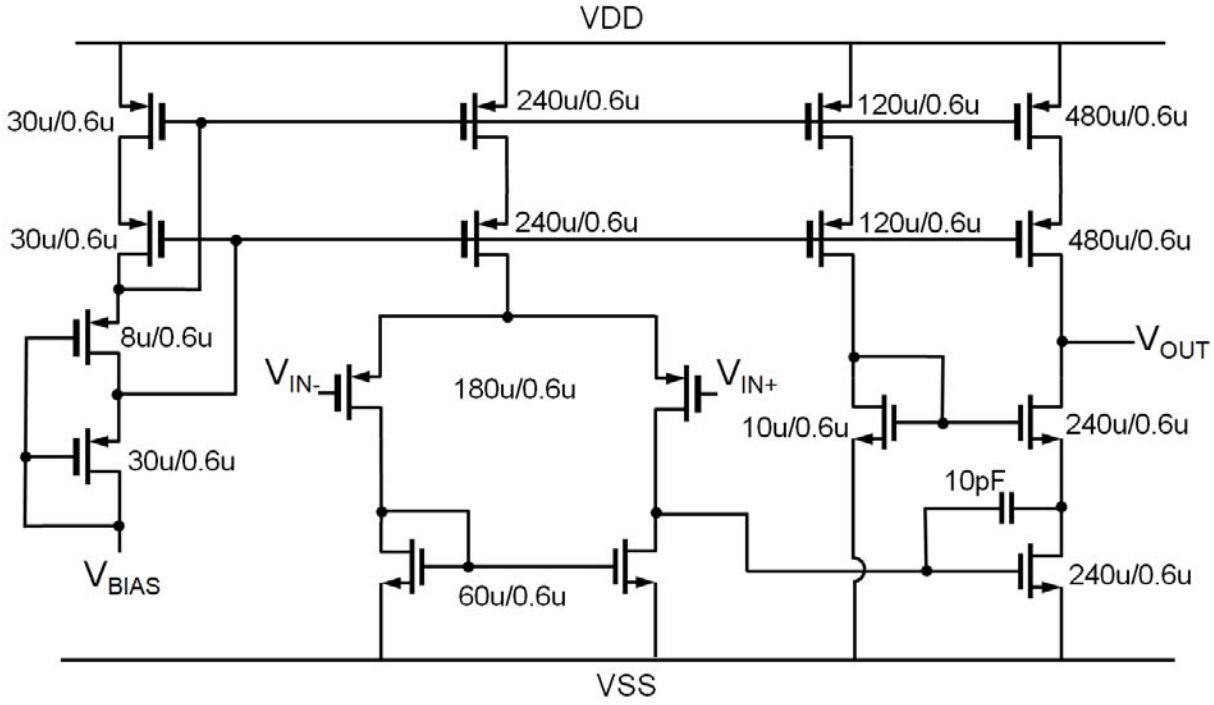

Figure 28: Integrator and Comparator OPAMP

Auto-Zero and Zero Integration Phase

Since the OPAMPs have systematic offset that drifts over time and temperature, the auto-zero phase is used to minimize this effect. The integrator and the comparator are first connected in unity-gain feedback and the offset voltage is stored onto a capacitor, as shown in Figure 29. Then switch S3 opens and S1 closes so that the input is sitting on top the offset voltage. Because the integrating capacitor needs to be discharge to the start point, 2.5V, at the beginning of each cycle, a zero integrator phase is also required. The simplest implementation is to use a MOS switch in parallel with the integrator capacitor. Both the auto-zero phase and the zero integration phase will reduce the overall conversion rate even further.

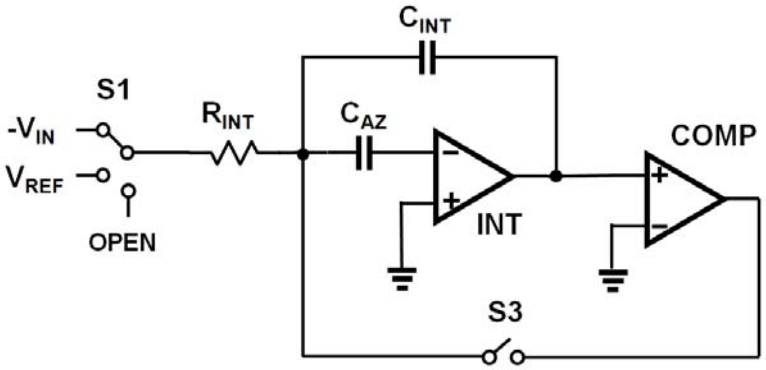

Figure 29: Offset Sampling Circuit

Microcontroller

The microcontroller takes in the reading from the comparator and controls all the switches as well as the counter clock. The microcontroller must procedurally execute the correct operations for all four phases of each conversion cycle. Since the microcontroller is not used to handle conditional events, the algorithm only involves executing the correct the command at the correct phase. Figure 30 shows an example flow chart of the microcontroller algorithm.

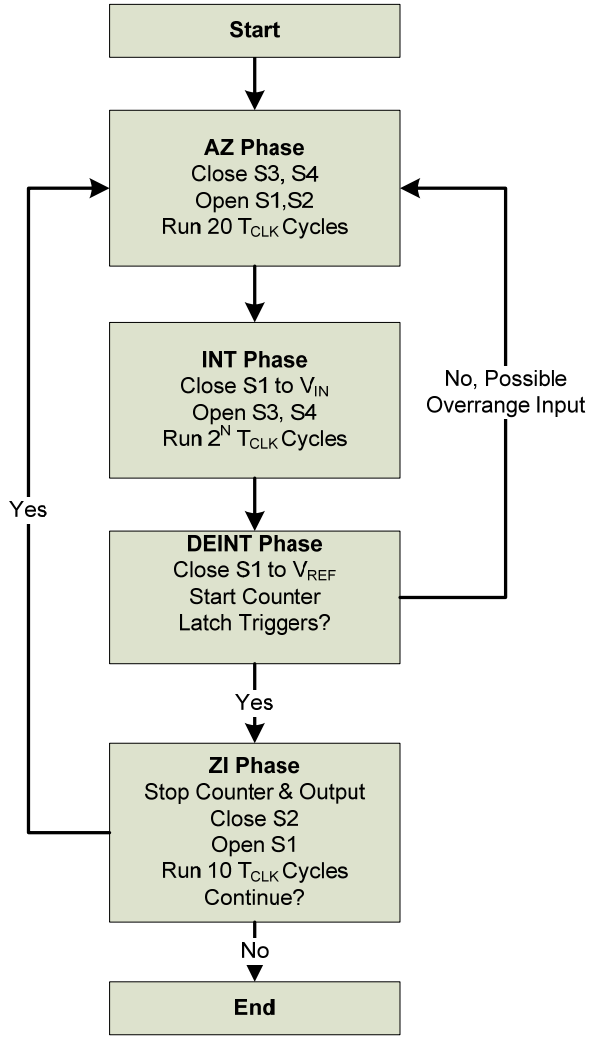

Figure 30: Microcontroller Flow Diagram

Sample-and-hold Circuit Considerations

The sample-and-hold circuit discussed in the last section needs to the modified to fit the requirement of the dual slope A/D converter. Unlike visual inspections from a beat test, the speed requirement is much lower and the error is much tighter. The general strategy is to increase the capacitance size and decrease the MOSFET width. For an 80dB resolution, the

pedestal error must be less than 0.2mV. From Equation (9), the maximum theoretical 3-dB frequency of the single stage sampler is approximately:

$\omega_{3-dB} = \frac{2\mu_n}{L^2}\Delta V = \frac{2(472.09cm^2 \cdot V/s)(0.2mV)}{(0.6\times10^{-4}cm)^2} = 52.45MHz$. With a seven time constant settling time, this translates into a maximum input frequency of $f_{IN} = \frac{\pi f_{3-dB}}{7} = \frac{\pi(52.54MHz)}{7} = 23MHz$.

This value is still an overestimate of the actual input bandwidth since it ignored the errors from clock feedthrough, thermal and flicker noise. Simulations of the sampling circuit with the same technique used in the beat test are required to verify the predictions.

Results and Conclusion

The sampling circuit introduced in the beat frequency test section is fabricated monolithically in AMIS 0.5 micron process, and a prototype test system is built on Printed Circuit Board (PCB). This section shows the HSPICE simulations for each stage of the on-chip sampling circuit, as well as the overall transient response. The measured results from the beat test prototype are also presented in this section. A comparison is drawn and the causes for the difference are discussed, followed by suggestions for future improvement.

Sampling Circuit Simulation Result

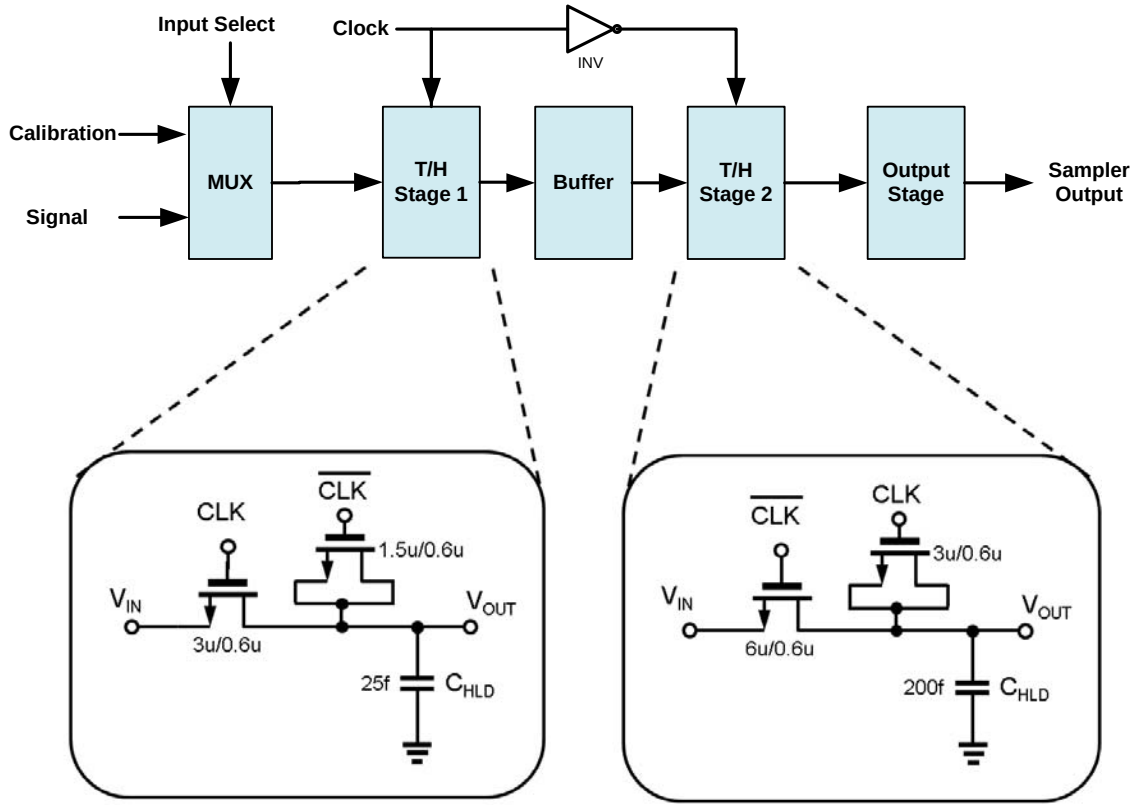

Figure 31: Sampling Circuit Implementation

Figure 31 shows the main sampling circuit discussed in the beat test section consists of two T/H stages, a buffer stage and an output stage. The transistor level schematics for the buffer and the output stage are shown in Figure 19, and Figure 20, respectively. This is the circuit that is fabricated monolithically, and simulations are ran base on the process dependent HSPICE models from AMIS. The transient responses of both T/H stages are first displayed, followed by the AC responses from the buffer and the output stage.

The first simulation is done with the rated 100MHz input sampled at 101MHz. The input is a sinusoid with a peak-to-peak voltage (V_{PP}) of 2V with a 2V DC offset. Figure 32 shows the transient response of a few periods of the input and the output of the first T/H circuit.

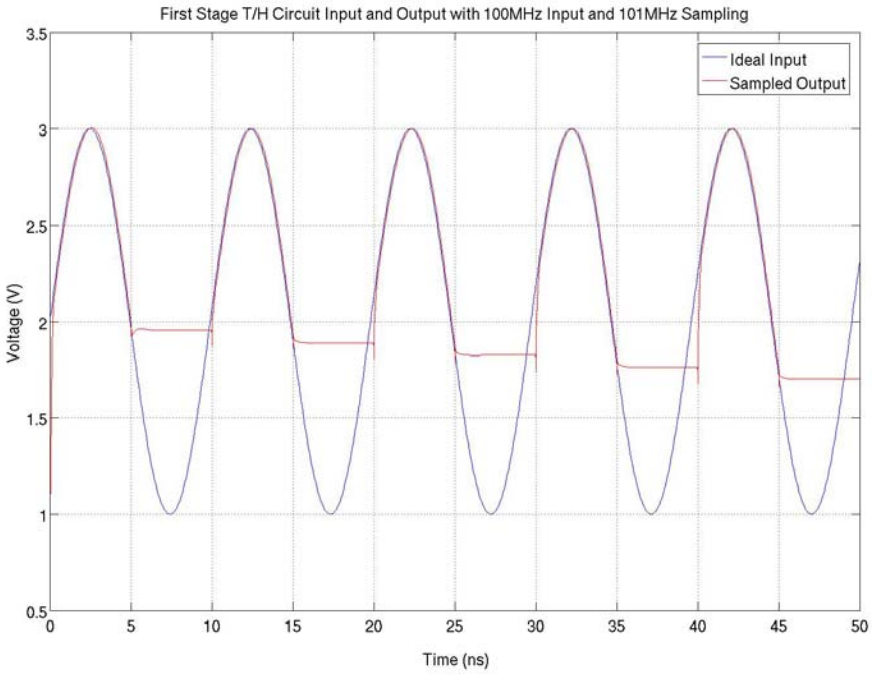

Figure 32: First Stage T/H Transient Response

The distortions discussed in the previous sections are clear evident in this figure. Figure 33 shows the input and the output from the second stage T/H circuit.

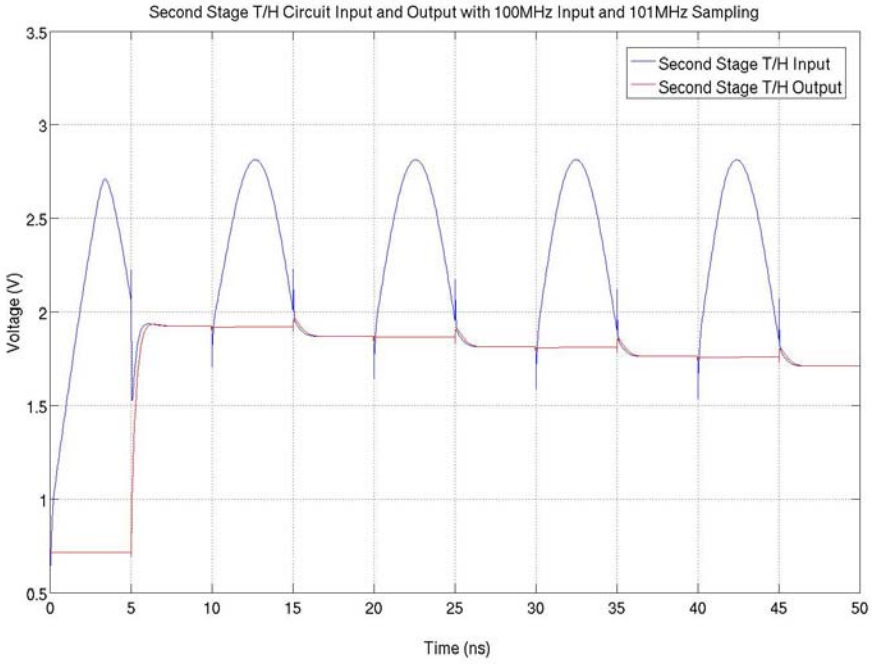

Figure 33: Second Stage T/H Transient Response

As expected, the output of the second stage T/H only shows the "staircase" waveform of the sampled value from the first stage, and sustains the value for one clock period. The amplitude attenuation is due to the bandwidth limitation of the source follower buffer. There is still the apparent negative pedestal error.

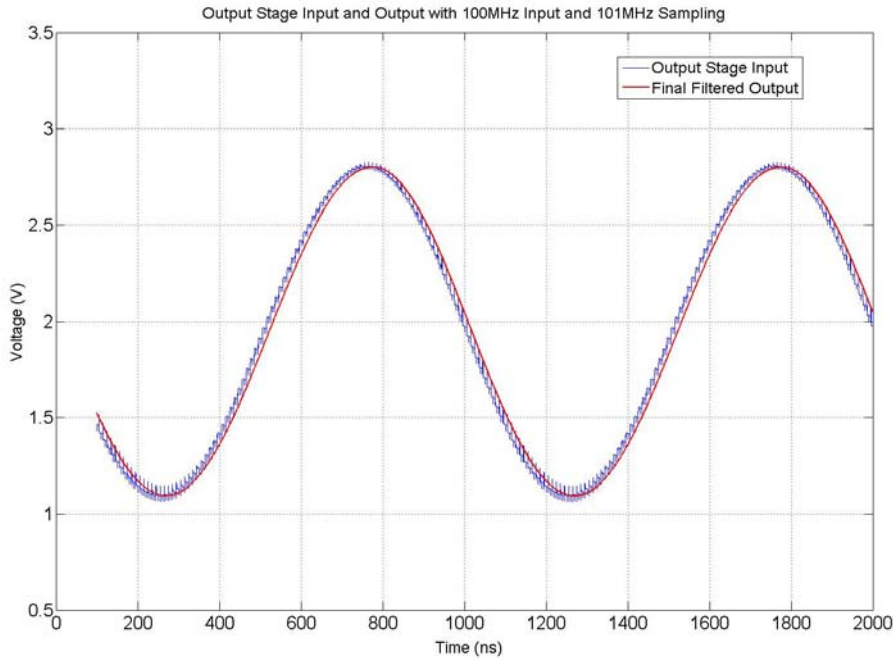

Figure 34: Overall Output Transient Response

The transient simulation for the overall output is shown in Figure 34. The output stage consists of a two-stage OPAMP discussion in the earlier section. With a load capacitance of 25pF, this OPAMP has a unity gain bandwidth of 300MHz, which becomes the 3-dB cutoff bandwidth. The result is that higher harmonics caused by switching noises are filtered out. The filtered output shown in red appears very close to a pure sine wave from naked eye. The next two plots in Figure 35 and Figure 36 show the power spectrum of the waveform before and after going through the output stage.

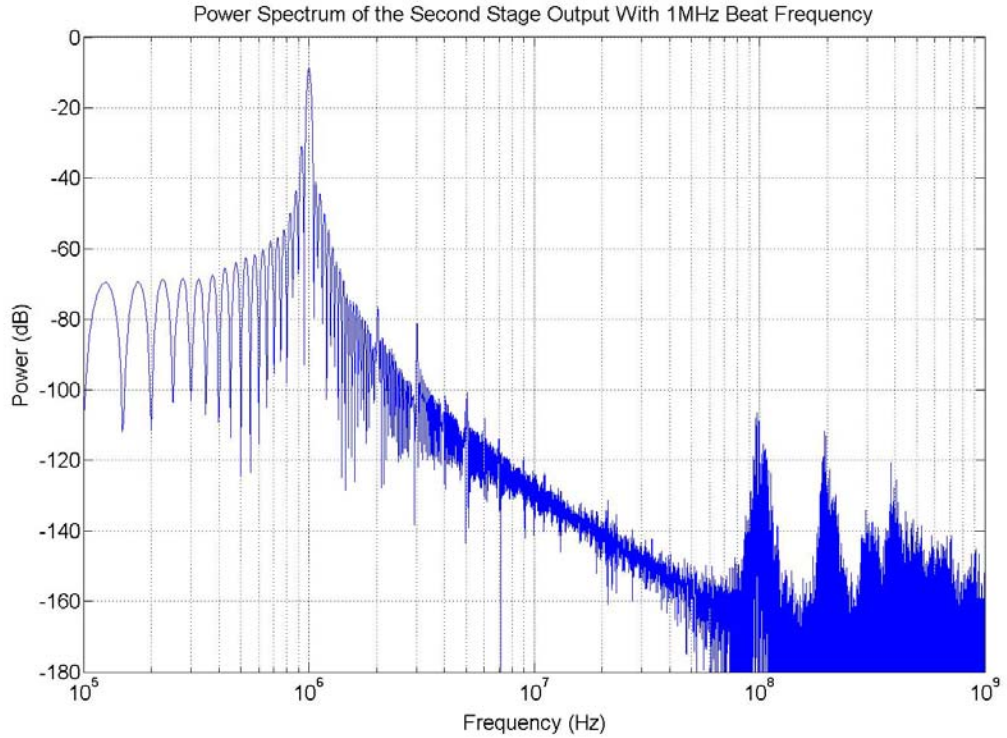

Figure 35: Second Stage Output Power Spectrum

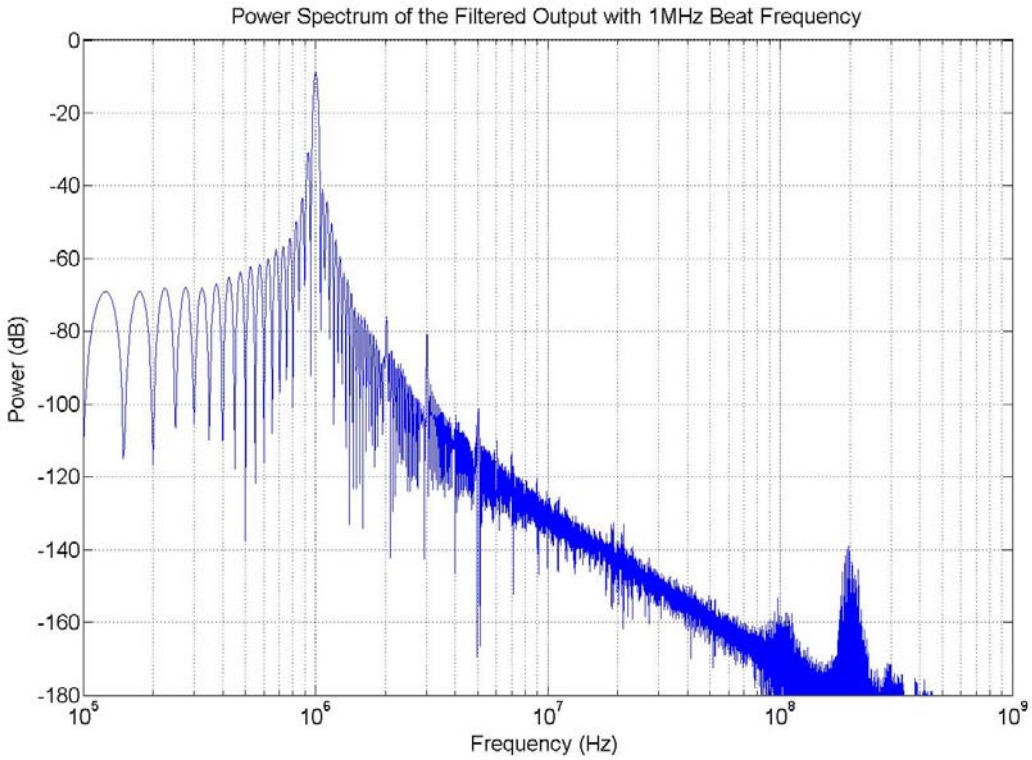

Figure 36: Overall Output Power Spectrum

Measurement Result

The on-chip sampler is fabricated through AMIS 0.5 micron process. Figure 37 shows the overall layout of the sampling circuit. All three metal layers are used and the entire circuit is fit into a 500 micron by 300 micron block.

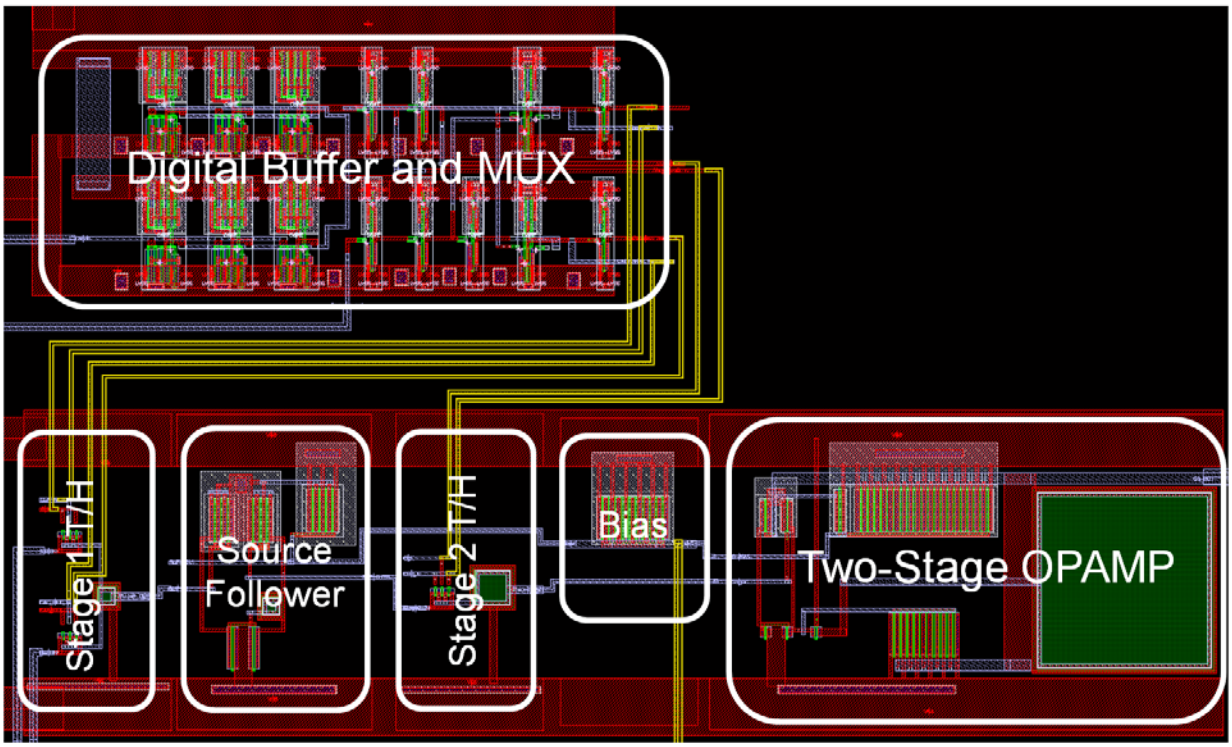

Figure 37: On-chip Sampler General Layout

The beat test system setup is illustrated in Figure 12. The A/D converter processes the output of the on-chip sampler at 150KS/s and sends it to a microcontroller which has 64Kb of memory. The microcontroller then transfers the data to a PC for analysis. The on-chip sampler is calibrated with a D/A converter before the data is written onto an output file. Figure 38 shows the final result obtained by the PC from the on-chip sampler under test, followed by the power spectrum of the data in Figure 39. The sampler is fed with a 1MHz sinusoid input clocked at 1.001MHz with a DC offset of 1.5V.

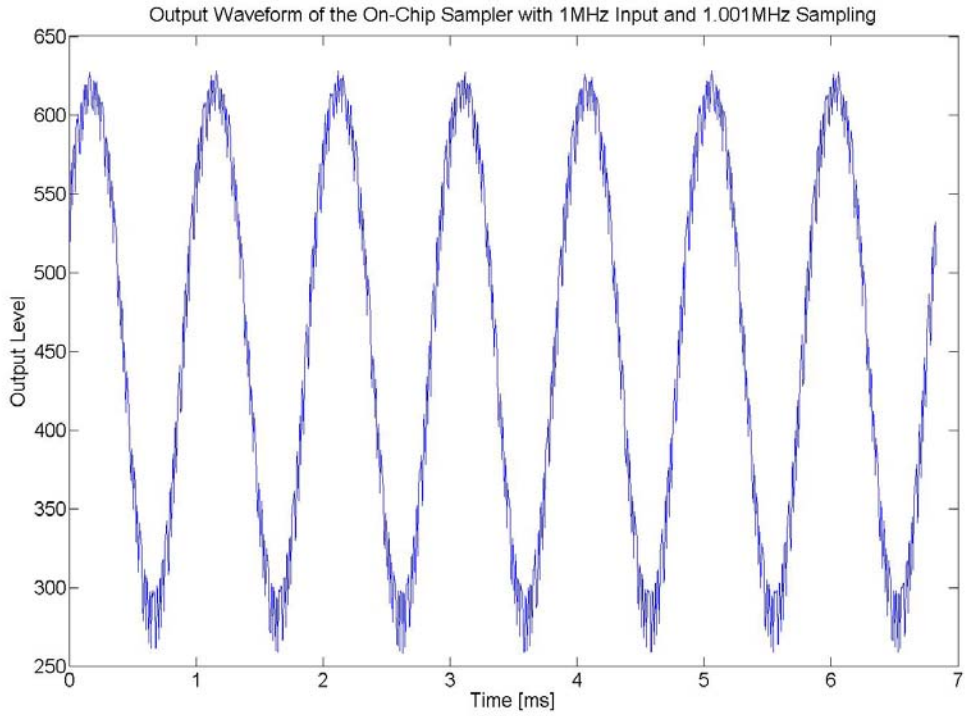

Figure 38: Measured On-Chip Sampler Output

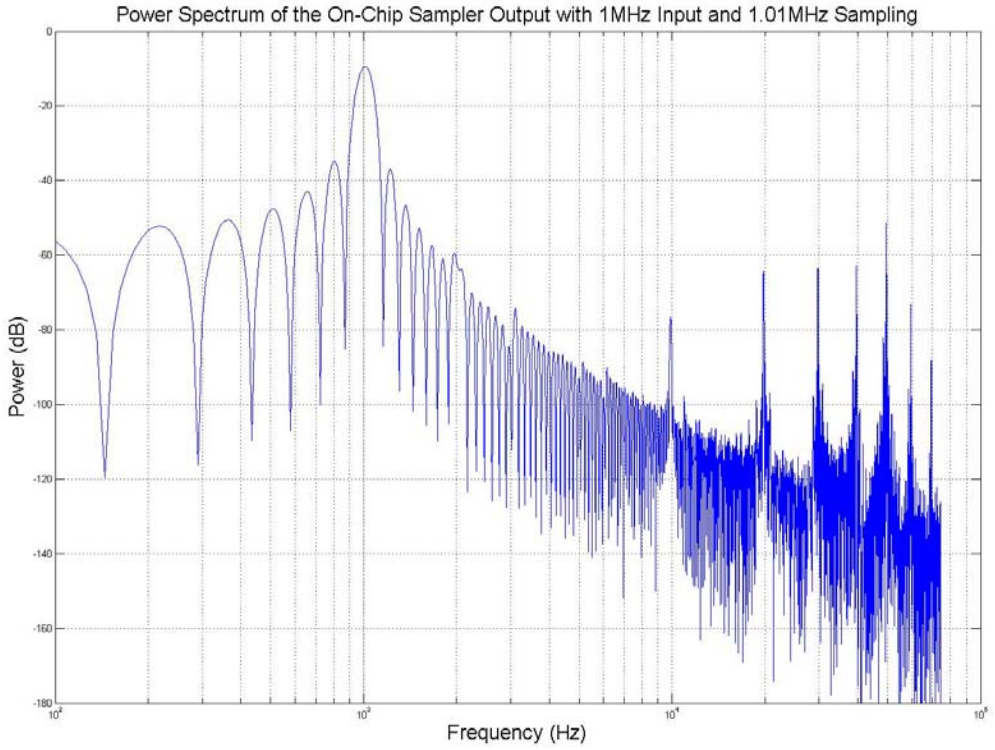

Figure 39: Measured Power Spectrum of the On-Chip Sampler

Conclusion

The sharp spikes on the first stage T/H transient response simulation are most likely due to the slight delay between the sampling MOSFET and the dummy. These high frequency noises are filtered out by the bandwidth of output stage. The more severe errors are the charge injections, appearing as gradual negative slides on every sampling instance. These errors must be taken care of by external calibration. The lower bandwidth of the second stage T/H prevents it from tracking error spikes from the first stage. As a consequence, the transistors are doubled in the width and the capacitance increased by eight times, theoretically cutting the charge injection error by four. The charge injection errors during the sampling instance are indeed smaller, yet the dominating error seems to be the settling time during acquisition. The small downward spikes caused by the dummy at the tracking instance cancel slightly with the upward swing as the T/H tries to track the output from the first stage. The frequency spectrums from simulation clearly show a reduction in the higher frequency beyond 100MHz by the output stage. The density graph shows a -55dB difference in beat harmonic power to the closest major harmonic at 2MHz. No major perturbation around the beat frequency is found.

The measured data from the prototype agrees with the simulated result as far as general functionality. Performance wise, however, the prototype is still below the expect result. The charge injection errors are much worse than it is the simulation base on visual inspection. There are numerous causes for this deviation: the non-ideal input signal and clock rise and fall times, the noise being at a much lower frequency than the bandwidth of the OPAMP, the mismatches between the dummy transistor and the delay in the clocks, and so on. The size of the charge injection varies as the input changes, but averages to be around 3% of V_{PP}. This makes the single NMOS sample unsuitable for any A/D converter requiring more than 5-bits of resolution.

In most cases single MOSFET sampler does not meet the speed-accuracy requirement. The single NMOS open-loop the S/H circuit does not suffice for any A/D converter with more than 5 bits of resolution, and other topologies must be implemented. Another common architecture of S/H circuit is known as bottom plate sampling is often used. This technique involves an additional transistor M2 that turns OFF before the main switch M1, as shown in Figure 40. This way the hold capacitor is left hanging and no charge is injected when M1 turns OFF. There is still charge injection from M2. However, since the source node is always fixed to ground, the charge injection error is the same every time and can be eliminated through a differential signaling or with calibration.

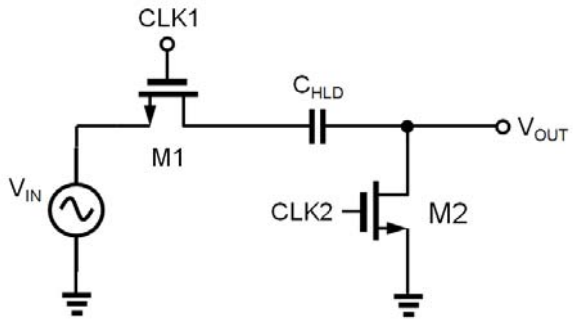

Figure 40: Bottom Plate Sampling

There are also numerous other S/H architectures that have been developed over the years. A switched OPAMP based S/H Circuit is introduced in [7] tried to minimize the effect of charge injection by turning the MOSFET off in saturation instead of triode. Article [8] tries to eliminate distortions by keeping the gate overdrive and threshold constant with bootstrapped technique. These techniques can be simulated and tested for future investigations of S/H circuits.

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