# AN ABSTRACT OF THE THESIS OF

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Title: Opamp Characterization Techniques

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John G. Kenney

Standard methodologies exist for testing and characterizing digital circuits but the same cannot be said of analog circuits. Though much theoretical work has been done to model the linear and nonlinear aspects of analog circuits, a firm practical background for the design of testable analog cells has yet to be set. The industry largely looks for solutions wherein some form of built in self-test (BIST) can be incorporated into the analog circuits to make the testing at the manufacturing level easy and accurate. Since the testers in the industry are generally digital, test circuits that use logic levels at the output to make measurements are attractive.

This thesis examines the design of such test circuits for one specific analog circuit, the opamp. Test circuits to measure the gain, gain-bandwidth product, phase response and the slew rate of the opamp have been designed and experimental results are presented. The main advantages of these tests are that they are simple, fast, accurate and easy to incorporate in an integrated circuit.

Opamp Characterization Techniques

by

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# Table of Contents

# List of Figures

# Opamp Characterization Techniques

## 1. Introduction

This report examines the design and implementation of a testable opamp that can be included in a larger analog system. The underlying philosophy of this work is to design testable cells that are simple to incorporate in VLSI systems, give accurate results and do not change the characteristics of the original system. An additional area of interest was to design test circuits with rectangular waves. Standard digital IC testers currently available in the industry, may be used for making measurements on such test circuits. This approach could prove cost effective, especially in the case of mixed-signal ICs having both digital and analog circuits on the same chip.

### 1.1 Motivation

Digital circuits can be easily characterized and at this point of time test methodologies have been successfully designed and automated. The situation in the field of analog circuits is quite different. Analog testing is by nature exhaustive and time consuming. The reasons for this are numerous. Analog circuits have a number of parameters that vary over their entire frequency and voltage range making parametric testing difficult. In addition, process parameters such as oxide thickness, extent of etching, doping of the various layers etc., may vary across the IC causing local variations in the parametric performance of the analog cell. All these factors make analog testability a challenging and demanding task. Given the complexity of analog testability, it requires a systematic approach to design adequate test circuits to characterize different parts of a large analog system.

The operational amplifier forms an important part of a number of analog and mixed signal systems. The operation and the characteristics of most practical analog circuits like switched capacitor filters, A/D & D/A converters etc., depend heavily on the linear and

non-linear behavior of the opamp. Hence an accurate estimation of these circuit parameters is necessary to evaluate the performance of the entire circuit. The linear parameters of interest are the DC gain, the gain bandwidth product, the first pole of the opamp and its phase margin. The most important non-linear parameter to characterize is the slew rate of an opamp, since it affects the transient response of the opamp to large changes in the input signal. Some amount of prior work has been done in the area of opamp testability[1][2][3] and these are discussed in the next section.

## 1.2 Prior Work

The prior work done on determining opamp parameters has mainly centered around determining its linear parameters. In[1], the authors have proposed to place the opamp in an inverting mode with a unity gain buffer in the feedback loop. The frequency at the input is swept across the entire range and the voltages at the inverting terminal and the output of the opamp are monitored to determine the gain response of the opamp. This work has been used by us as a starting point for developing test strategies for opamps.

In [2], a technique has been proposed to measure the gain bandwidth product and the second pole of an opamp by placing it in an unity gain feedback mode. The opamp was modeled as a two pole system with a very low frequency first pole. In unity gain feedback mode, the phase lag between the input and the output of the opamp can be determined in terms of the gain bandwidth product and the second pole of the opamp. The phase lag is measured at two different frequencies to determine these two unknowns. This measurement requires the use of a network analyzer to make accurate phase measurements. Making such accurate phase measurements at very high frequencies is often difficult due to the fact that getting these signals off chip requires dealing with probe and test jig capacitances.

The technique described in [3] requires characterizing the phase response of an inverting amplifier to compute the gain bandwidth product of an opamp. This method requires determining the ratio between the unity gain frequency and the second pole of the

opamp. As the second pole of this system is far from the dominant pole, the frequency at which the phase shift is +135° is approximated as the location of the second pole. With this information and the ratio between the unity gain frequency and the second pole of the system known, the gain bandwidth product of the opamp is determined. The accuracy of this measurement technique depends not only on the accuracy of the phase measurements but also on the accuracy of the resistors used to form the closed loop system.

All of the above mentioned work has influenced the test designs presented in the report. The test plan proposed in [1] has been implemented on silicon using CMOS technology. The two pole model of the opamp proposed in [2] and [3] has been extensively used in the design of the test circuit for the gain bandwidth product.

## 2. Test Methodologies

This chapter discusses the various test circuits devised to measure the linear and non-linear parameters of an opamp. Two separate methods to measure the gain and phase response of an opamp are presented followed by experiments to measure the gain-bandwidth product and the slew rate. A detailed description of each test circuit along with a discussion about its advantages and potential problems are presented.

### 2.1 Opamp Characterization using Buffers
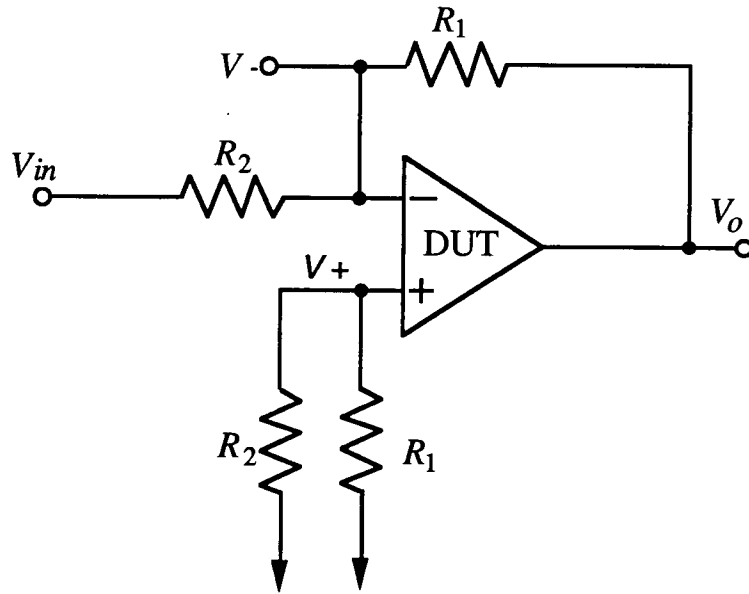


Figure 1. Standard Test Setup for Gain Measurement

A conventional test circuit for opamps [1] is shown in Fig. 1. The opamp is placed in a closed loop and operated as an inverting amplifier so that large inputs can be applied at $V_{in}$ without saturating its output. The open-loop gain of the opamp is given by the ratio of $V_o$ to $V$- where $V$+ is at ground. The resistance at $V$+ is the parallel combination of $R_1$ and $R_2$ so that the input resistance at both $V$+ and $V$- is the same.

The ratio of $V_o$ to $V$-, taking the output impedance into account is

$$\frac{V_o}{V-} = -\frac{A - Z/R_1}{1 + Z/R_1}$$

(1)

This equation shows that the signal produced by the opamp at high frequencies can be much smaller than the feedthrough of the input signal through $R_1$. This is because at very high frequencies the gain of the opamp, being frequency dependent, is quite small so that the output impedance of the opamp becomes a factor(See Fig. 2).



Figure 2. Gain Response of an Opamp



Figure 3. Test Circuit with Unity Gain Buffer

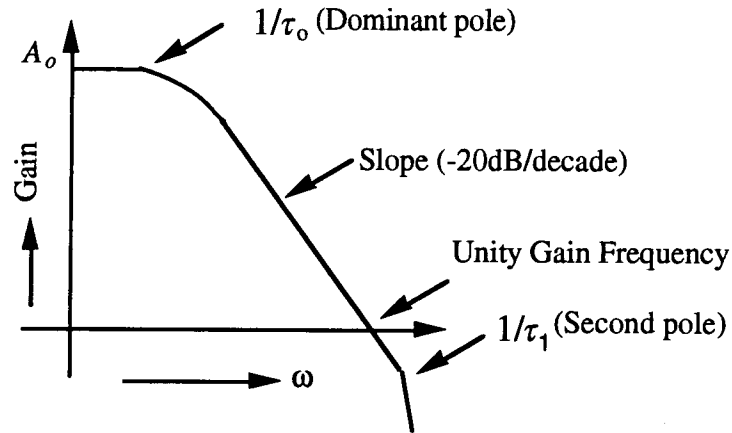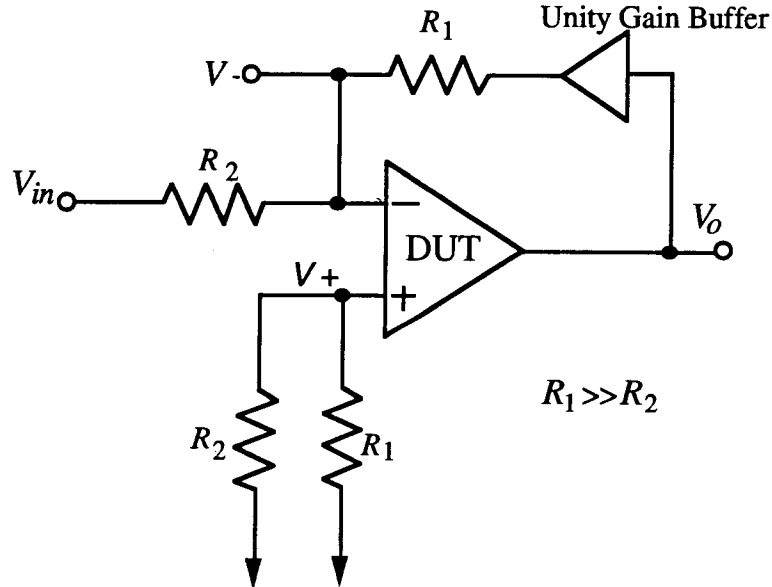A measurement error will occur due to the reduced gain of the opamp at high frequencies and its finite output impedance. The error caused by a finite output impedance can be eliminated by placing a buffer in the feedback path [1](See Fig. 3).

The buffer must have a very high input impedance and a low output impedance. Hence it passes the feedback signal but not the feedforward signal. This eliminates the zero from the transfer function between $V_O$ and $V$ -. The ratio $V_O / V$ - becomes equal to $-A(j\omega)$,i.e., the gain response of the opamp.

Consequently, the ac response of the opamp can be determined by varying the input frequency and determining the ratio $V_O / V$ - at various frequencies. This entire measurement can be automated by using a network analyzer.

A potential problem in this measurement technique arises in the case of opamps with gains of 80 dB or more. At low frequencies the signal at $V$ - will be on the order of microvolts due to the enormous gain of the opamp. Thus the signal at $V$- must be amplified to measure it. This amplification can be achieved by using a single input low gain amplifier with a gain of around 25 dB. It will be necessary to know the gain of this amplifier accurately to determine the gain response of the opamp. For an on-chip amplifier, process variations will affect the amplifier gain and lead to incorrect interpretation of the measurement.

For an on-chip implementation of this circuit, the main component to be designed is the unity gain buffer in the feedback path. This buffer must be fast with good linearity and a gain as close to one as possible. The next section describes the design of one such buffer.

## 2.1.1 Unity Gain Buffer Design

The unity gain buffer must have a 3 dB frequency that is at least one decade higher than the unity gain frequency of the opamp. This is so the buffer will have constant gain

and group delay over the range of frequencies from DC to the unity gain frequency of the opamp.
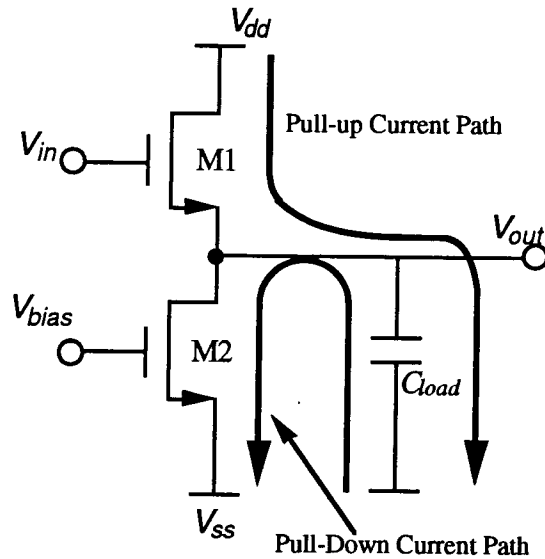


Figure 4. NMOS Source Follower

The regular NMOS source follower topology is shown in figure 4. Transistor M2 forms the current source to bias the source follower and transistor M1 is the input device. For a large signal input, when the input increases, the transistor M1 turns on and the capacitor at the output is charged up by the positive supply. When the signal goes low transistor M1 turns off completely and the capacitor is discharged towards $V_{ss}$ through transistor M2. The regular NMOS source follower has a very high input impedance and a low output impedance. Thus it satisfies the two most important conditions for the buffer in the feedback path. But it suffers from one serious limitation. The downward slew rate is limited by the constant current source formed by M2, meaning slower pull down times and non-linearity in the case of high frequency operations. The output voltage and current for a large signal input are shown in Fig. 5. From this figure, we can see that on the rising edge the current peaks at 1.25mA leading to a pull up time of 16ns. However a very low current of 200μA leads to a much slower pull down time of around 45ns.

To effect an improvement in the downward slewing it is necessary to increase the pull down current. This can be achieved if the size of the transistor M2 is increased greatly or if the bias voltage of M2 is increased. This approach leads to very large transistor sizes, increased power dissipation and a reduction in the linear range of the buffer. An alternative approach is the buffer design shown in figure 6. The speed is improved by turning on a transistor during pull down which provides for more current to discharge the load capacitance $C_{load}$.
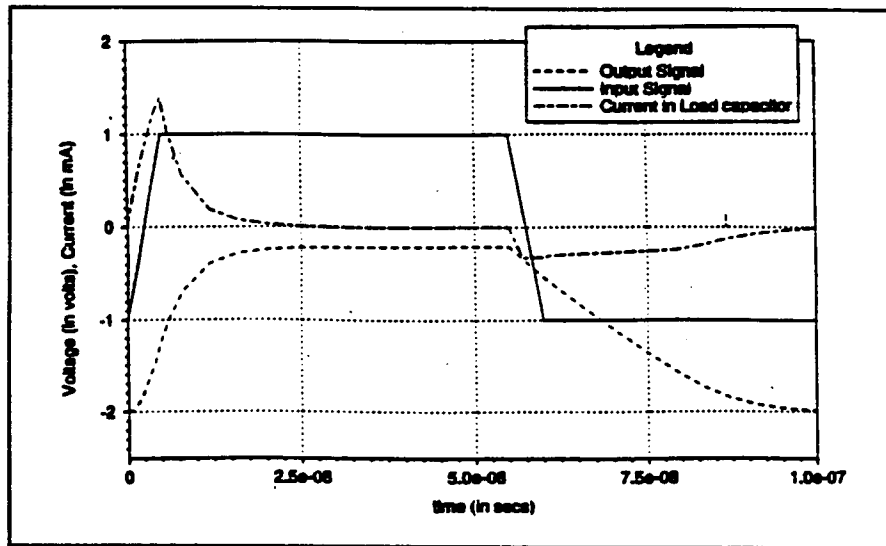


Figure 5. Voltage and Current Signals of a NMOS Source Follower

In the circuit shown in Fig.6, there are two source followers. The one formed by transistors M1 and M2 has a load capacitance at its output and the other formed by transistors M3 and M4 has no load at its output node. The two outputs are fed to the inputs of an amplifier whose output is then fed to the gate of an NMOS transistor (M5).

The operation of this circuit for large signal inputs can be explained as follows. During the falling edge of a large signal input, the source follower with no load on its output will fall faster than the source follower whose output is loaded by a capacitor. This causes a difference between these two signals which is sensed by the slewing detector. Since the negative input to the opamp is lower than the positive input, the opamp output

goes towards the positive rail turning on the pull-down transistor(M5). This provides an additional discharge path to ground which allows the output of the buffer to slew down faster.
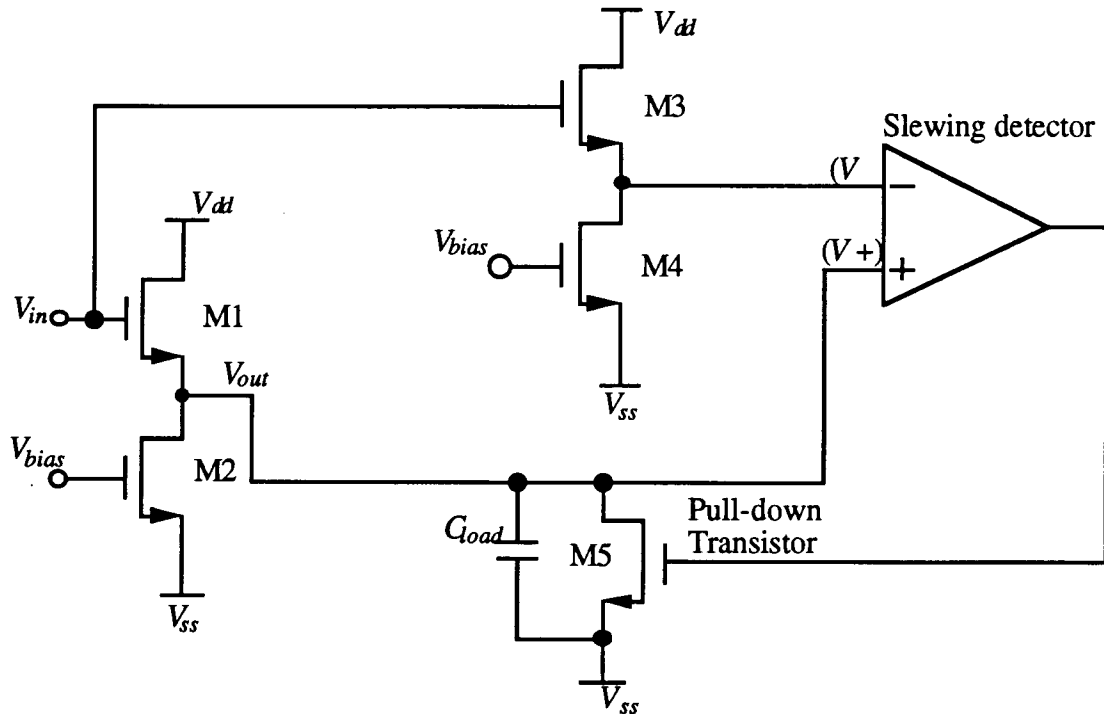
Figure 6. Slew Rate Enhanced NMOS Source Follower
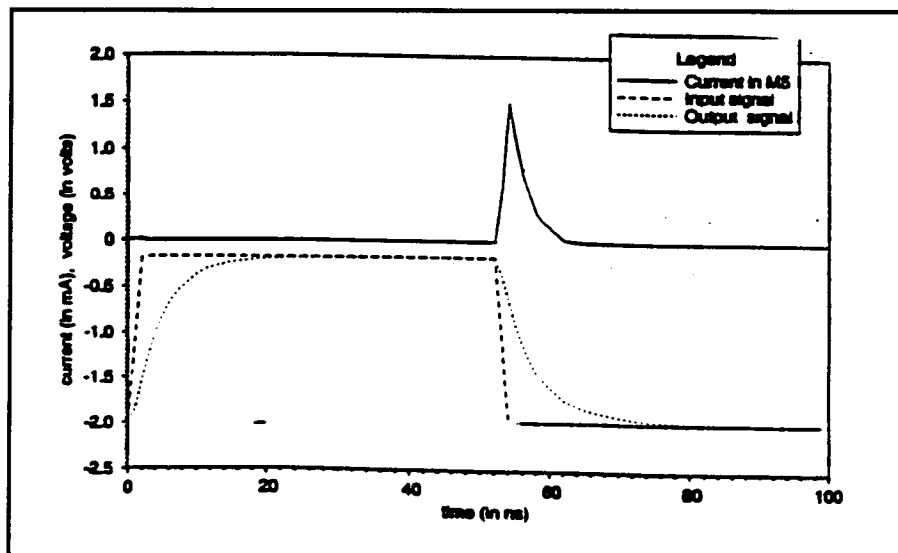
Figure 7. Voltage and Current Signals in the Slew Rate Enhanced Source Follower

On the other hand, during pull up, the voltage at the output of the buffer with a load capacitance goes up slower than the voltage at the output of the unloaded one. This results in the positive input being smaller than the negative input of the opamp causing its output to go to the negative rail. Transistor M5 turns off thereby disabling the auxiliary discharge path to ground. Hence transistor M5 is only turned on when extra current is required during pull-down. This can be clearly seen in figure 7 which shows current flowing through M5 during the time interval from 50ns-70ns, ie., exactly during pull down. This transistor does not play any other role in the operation of the source follower and hence does not affect its gain.



Figure 8. Circuit Schematic of the Slew Rate Enhanced Source Follower

In the improved circuit design, the source followers are regular NMOS structures. The opamp is a single stage with a gain of around 85(See Fig 8). The main reasons for using a single stage are its simplicity and the fact that single stage designs are inherently f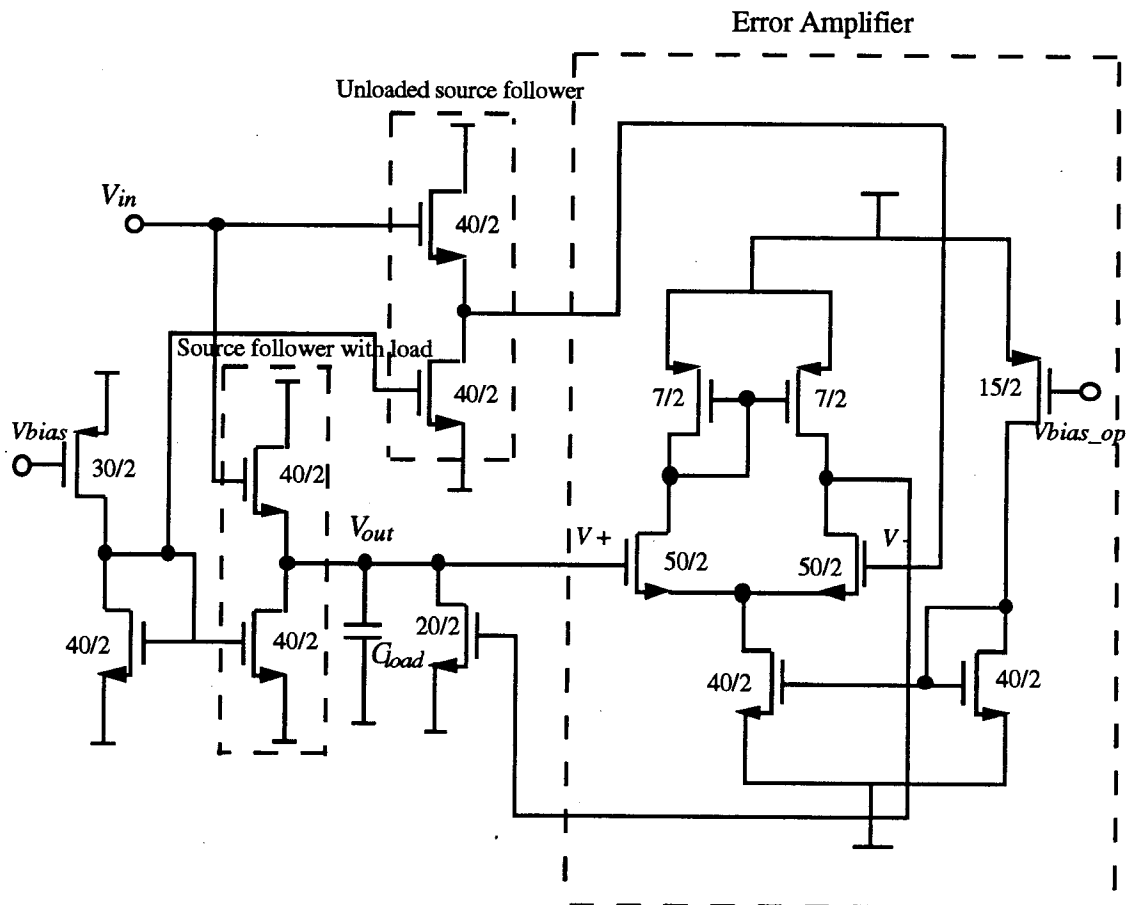aster and require no internal compensation. Since the size occupied by the test circuit is a factor in the design of these circuits, single stage circuits are ideal as they occupy very little area. The gain was determined to be sufficient as the difference between the outputs of the loaded and the unloaded source followers is large enough to cause the output of the opamp to hit the rails. The opamp response is fast and its slewing is not a problem as the output load is only the gate of transistor M5 .

## 2.2 Frequency Response Measurement Technique

The gain response of a stable opamp has a dominant low frequency pole and a second pole above unity gain crossover. Thus the gain drops at the rate of 20 dB/decade after the dominant pole of the opamp until it hits the second pole beyond unity gain (Fig.9).
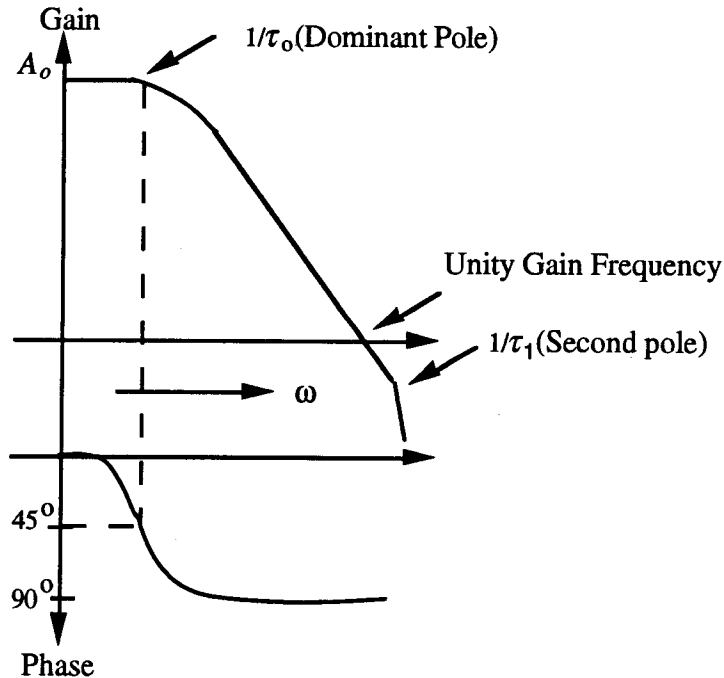


Figure 9. Gain and Phase Response of the Opamp

To reconstruct the gain response of an opamp it is necessary to determine the first pole and the unity gain frequency of the opamp. Once these parameters are determined, a piecewise linear approximation of the opamp's gain response can be constructed.

The dc gain of the opamp is approximated as the gain of the opamp at the first pole. The gain bandwidth product can be determined by the test circuit described in the next section. The first pole of the opamp is at the frequency where the phase difference between the signals at $V$- and $V_{out}$ is -135°. The experiment described in section 2.2.2 determines the frequency at which the first pole is located.

## 2.2.1 Gain Bandwidth Product Measurement

In measuring the GBW of an opamp, its low frequency pole is used to build a sinusoidal oscillator. As mentioned before, in the simplified model of an opamp, there are two poles and a large low frequency gain. The first pole at $1/\tau_0$ is used to force the open-loop gain of the opamp to cross unity before the second pole at $1/\tau_1$ is reached. This allows the opamp to be accurately modeled as a single pole system. For the opamp to oscillate two actions must occur: a known second pole must be added to the system between the dominant pole & the unity gain frequency and the first order term in the closed loop transfer function must be zeroed.

The first objective, namely, adding a second significant pole to the system may be achieved by placing a resistor between the output terminal and the inverting terminal of the opamp. Also a capacitor must be connected between the inverting terminal and a fixed voltage reference such as ground. Although this is a less stable circuit than the unity feedback configuration, positive feedback still needs to be placed around the opamp so that the $s$ term in the closed loop transfer function goes to zero forcing the opamp to oscillate.

The gain of the opamp reduces as the output voltage approaches the supply rails. This amplitude dependent non-linearity in the voltage gain is used to prevent severe

clipping in the output waveform. Assuming that the positive feedback around the opamp is small enough that the circuit does not slew, the output of the opamp gently clips as its amplitude moves into the nonlinear region. Thus sinusoidal oscillations can be sustained. The frequency of oscillation is a function of the gain bandwidth product of the opamp. By measuring the frequency of oscillation, we can compute the gain bandwidth product. The relationship between the gain bandwidth product (GBW) of the opamp and the output frequency of this system is presented below.

In figure 10, the block named DUT (device under test) is our opamp and the second block is the feedback path. The transfer functions of the DUT and the feedback path are
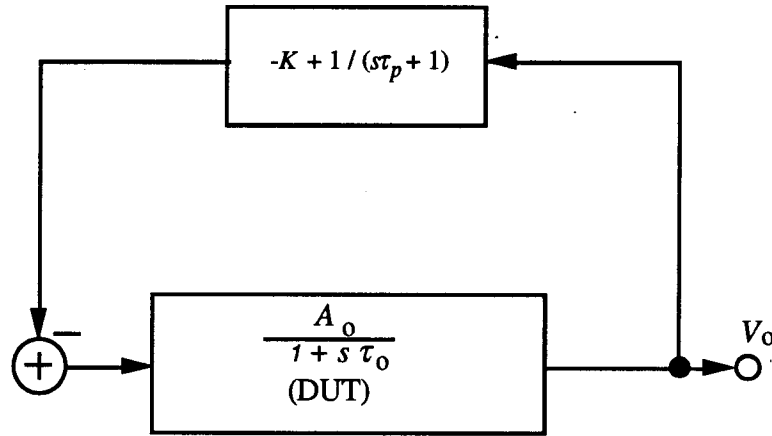


Figure 10. $s$ - Domain Representation of the GBW Test Circuit

indicated inside their respective boxes. The opamp is assumed to be a single pole system with a time constant $\tau_0$. From Fig. 10, the characteristic function $\Delta(s)$ can be derived to be,

$$\Delta(s) = 1 + \beta(s)A(s) \tag{2}$$

where $A(s) = A(s) = A_o/(1 + s\tau_o)$ and $\beta(s) = -K + 1/(1 + s\tau_p)$. Substituting for $A(s)$ and $\beta(s)$ in the above expression for $\Delta(s)$ and putting Eqn.2. to zero, we get :

$$s^2 + s\left(\frac{1}{\tau_o} + \frac{1}{\tau_p} - \frac{A_o K}{\tau_o}\right) + \frac{A_o(1 - K) + 1}{\tau_o \tau_p} = 0 \tag{3}$$

In the above expression, we notice that if the coefficient of the first order term becomes zero, then the poles of the system will become purely imaginary causing the system to oscillate, i.e.,

$$\frac{1}{\tau_o}+\frac{1}{\tau_p}-\frac{A_o K}{\tau_o}=0 \qquad (4)$$

Solving for $K$ gives

$$K=\frac{1}{A_o}+\frac{\tau_o}{A_o\tau_p} \qquad (5)$$

Comparing equation (3) with a general second order system, we get

$$\omega^2=\frac{A_o(1-K)+1}{\tau_o\tau_p} \qquad (6)$$

Since for practical opamps $A_o(1-K)>>1$, the above equation can be rewritten as

$$\omega^2=\frac{A_o(1-K)}{\tau_o\tau_p} \qquad (7)$$

Substituting for $K$ from equation (5) in equation (7), a relationship between the output frequency $\omega$ and the gain bandwidth product (GBW) of the opamp $(A_o/\tau_o)$ is obtained,

$$\omega^2=\frac{A_o}{\tau_o\tau_p}\left(1-\frac{1}{A_o}-\frac{\tau_o}{A_o\tau_p}\right) \qquad (8)$$

Since the DC gain is high for practical opamps, the term $1/A_0$ can be neglected in the above equation and it can be rewritten as,

$$\omega^2=\frac{A_o}{\tau_o\tau_p}-\frac{1}{\tau_p^2} \qquad (9)$$

from which the gain-bandwidth product can be derived to be,

$$GBW = \frac{A_o}{\tau_o} = \omega^2 \tau_p + \frac{1}{\tau_p} \tag{10}$$

By measuring the output frequency and knowing the time constant $\tau_p$, we can find the GBW of the opamp. $\tau_p$ can be realized as a simple RC series network and positive feedback $K$ may be introduced by a voltage divider network as shown in Fig.11. $R_2$ may be varied to provide the proper amount of positive feedback required to make the system
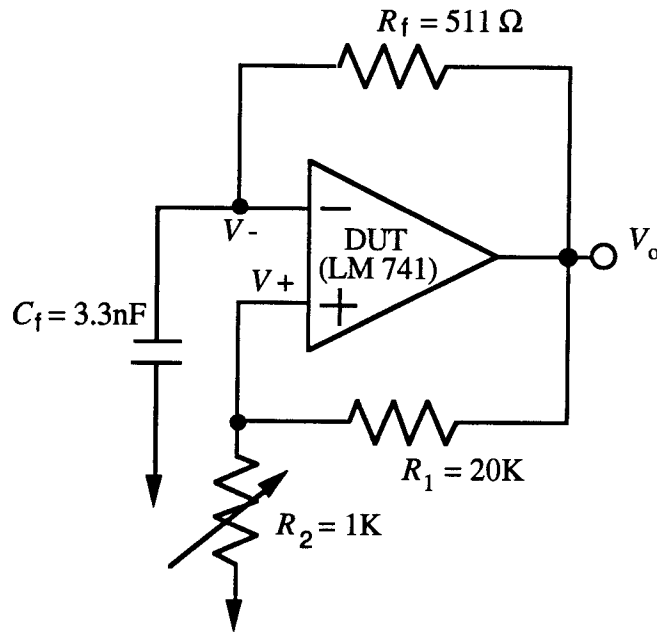


Figure 11. Test Circuit for GBW Measurement

oscillate. The value of $K$ is not important as it does not appear in the final expression. In an IC implementation, the resistors can be laid out using polysilicon. A comparator can be added at the output of the opamp to convert the sinusoid to a rectangular waveform so that the frequency of oscillation can be measured using a digital tester.

The complete analysis of the gain bandwidth circuit has been carried out assuming that the non-dominant pole of the opamp is at a very high frequency and that it has no effect on the overall system. The assumption that the second pole is well beyond the unity gain frequency may not be true in all cases. The non-dominant pole may be quite close to the

unity gain frequency for a number of opamps and a study was done using MATLAB to determine the effect of the relative position of the non-dominant pole on the frequency of oscillation. The opamp was modeled as having a DC gain of 45 dB with its dominant pole at 6.3 kHz. Since the unity gain frequency is at 945 kHz, two different frequencies for the non-dominant pole were used to determine the change in
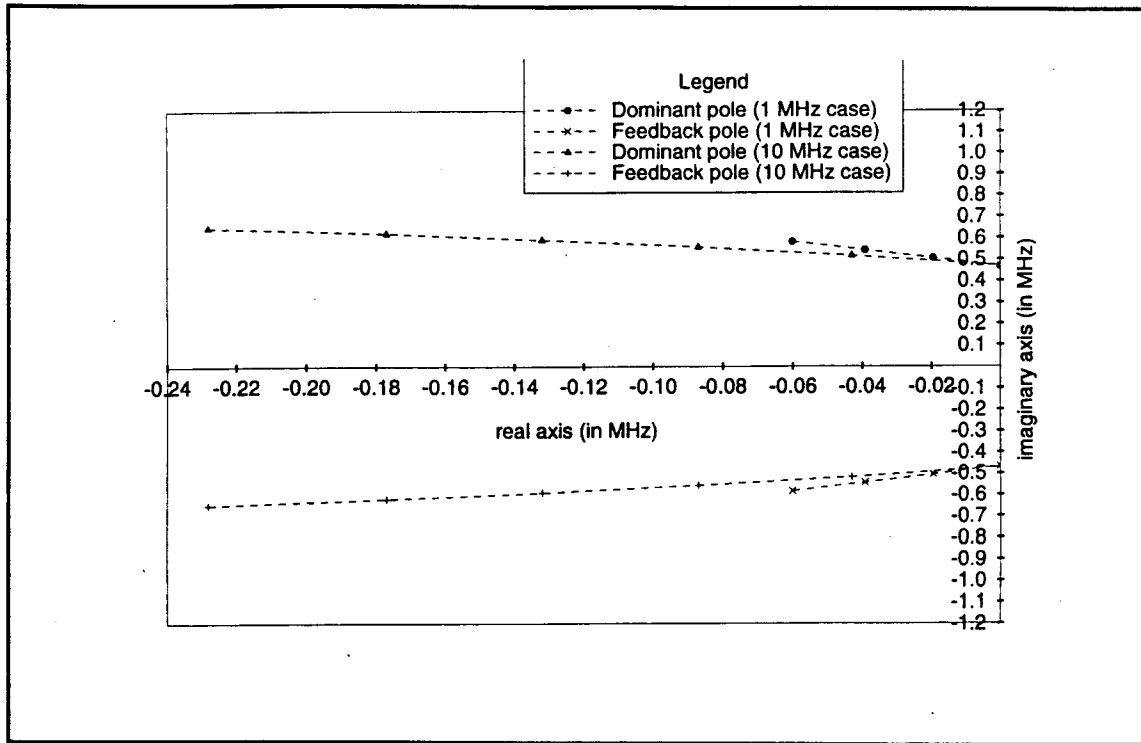


Figure 12. Root Locus Plot for the GBW Circuit

the frequency of oscillation. In the first case, the non-dominant pole is assumed to be at 1MHz and in the second case it is placed a decade higher at 10MHz. The characteristic equation when the non-dominant pole is included is

$$\frac{A_o}{(1+s\tau_o)(1+s\tau_1)}\left[-K+\frac{1}{1+s\tau_p}\right]+1=0$$

(11)

where $\tau_1$ is the non-dominant pole of the opamp.

A root locus of the characteristic equation was performed for $\omega_1$ at both 1MHz and 10MHz to determine the frequency of oscillation after positive feedback had been

applied(See Fig.12). The frequency of oscillation in the first case was found to be 467.8 kHz and in the second case it was 470 kHz leading to a difference of around 0.6 %. Although the amount of positive feedback differed in the two cases, the frequency of oscillation remained relatively unchanged. Hence it can be concluded that the position of the non-dominant pole has a minimal effect on the frequency of oscillation.

## 2.2.2 First Pole Measurement

The first pole of a stable opamp is the frequency at which the phase difference between the signal at $V-$ and the output is $135^{\circ}$. The circuit used to measure the phase margin is an extension to the circuit used to measure the DC gain. The basic idea is to somehow measure the phase difference between the $V-$ and $V_{out}$ without resorting to a network analyzer.

An XOR gate is used as a phase detector. Since the inputs to the XOR gate require binary signals, the voltages at $V-$ and $V_{out}$ have to be converted to a rectangular waveform before being fed to the XOR gate. This can be achieved by using comparators as shown in Fig.13. Since the signals at $V-$ and $V_{out}$ are $180^{\circ}$ out of phase the signal at $V-$ is fed to the negative input of the comparator(C1) and the signal at $V_{out}$ is fed to the positive input of the comparator(C2). The output of the XOR goes high only when one of its inputs is high and the other is low . Thus the output of the XOR gate will be a rectangular wave at the first pole of the opamp with a duty cycle of 0.25. The first pole is at half the frequency of the output of the XOR gate.

The problems that can be encountered are the low value of the signal at $V-$ for opamps with a very large gain($\geq 80$ dB) and the presence of both input offset and output offset voltages. Very large gains will make the signal amplitude at $V-$ so small that it might not be enough to switch the comparator. This is the same problem encountered in the gain

measurement using the unity gain buffer(See section 2.1) and the solution was to amplify
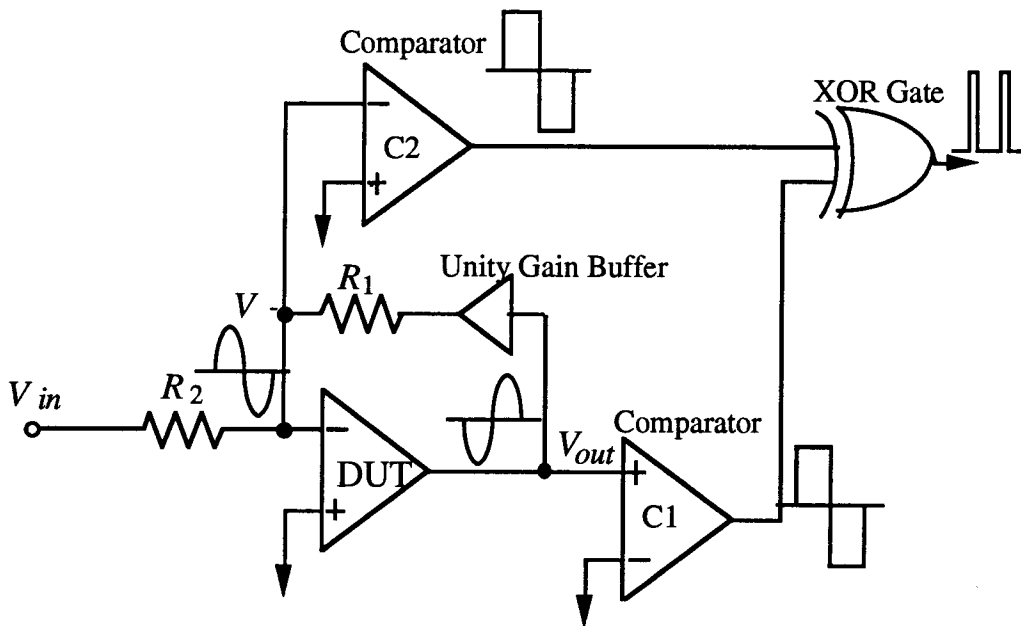
$V$- so that it could switch the comparator.



Figure 13. Test Circuit to Characterize the First Pole and the Phase Margin

The advantage of this method lies in the fact that it is not important to know the exact value of the gain of this amplifier as long it does not add any phase error. This is easily achieved as a relatively low gain amplifier can be built with zero phase at low frequencies. Thus the gain of this amplifier can vary because of process variations but it will not affect the measurement in any fashion. The obvious fact is that phase measurement is insensitive to gain error and hence is better than a direct voltage measurement which is very sensitive to gain error. The other solution to this problem is designing very low offset comparators capable of switching at low input voltages. At low frequencies, the comparator(C2) will not hit the rail as fast as the comaparator(C1) at the output node. This is due to the low signal strength at $V$ - causing the input drive to the comparator C2 to be much lower than the input drive of comparator C1. In figure 14 it is shown that a 0.2$\mu$s lag time occurs between the two output signals for input drives of 10mV and 2V respectively for an LM339.
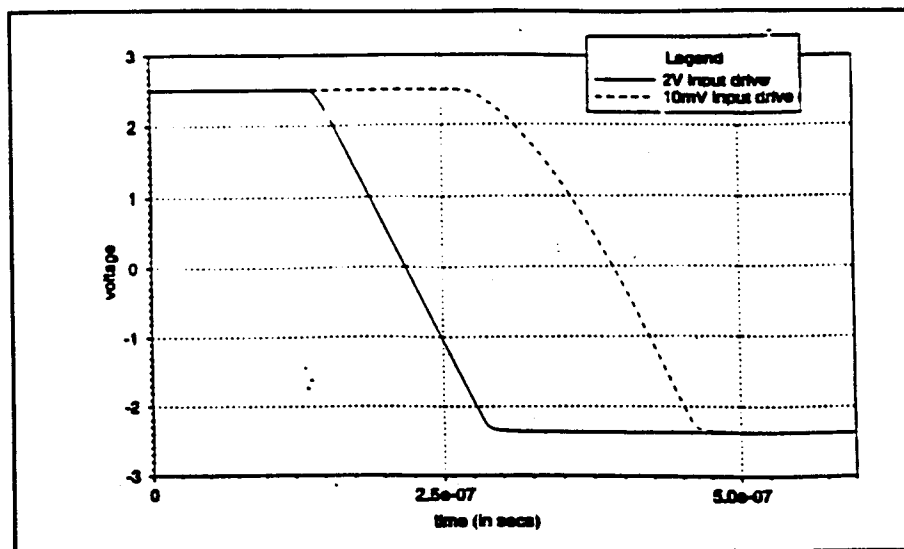
Figure 14. Comparator Response to Different Input Drives

This will cause an error in measurement of the order of around 10%-20 % for opamps having first pole in the megahertz or hundreds of kilohertz range. Thus the signal at $V$- must be sufficiently amplified so that this difference in the switching times are insignificant compared to the frequency of the first pole. Since the first poles of very high gain opamps are at low frequencies(e.g. 1 kHz), this problem can be easily tackled with moderate amplification of the signal at $V$-.

The problem of offset voltages is a serious one as it will generate rectangular pulses and not square pulses as required at the outputs of the comparators. This will lead to erroneous results as the phase difference between the two rectangular waveforms will no longer be equal to 45° at the first pole. Thus an offset cancellation can be performed by applying the requisite amounts of DC voltage with the proper polarity to the positive and negative inputs of comparators C2 and C1 respectively. This will cause the comparator outputs to be square waves. The other alternative is to use the duty cycles of the comparator outputs to come up with the correct position of the first pole. This can be mathematically derived as follows with the help of figure 15.
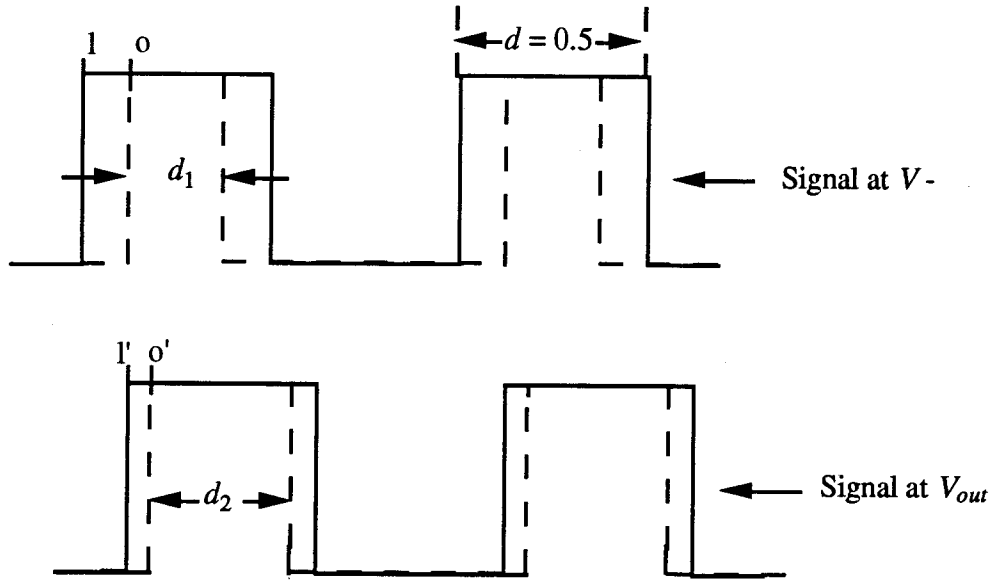
Figure 15. Rectangular Signals at $V$- and $V_{out}$

The solid lines in the figure represent two square waves with a phase difference of 45° between them. The dotted lines represent the same waves but now in a rectangular fashion due to the offset voltages present at $V$- and $V_{out}$. The normalized duty cycles of the two waves now are $d_1$ and $d_2$. Note that the frequency of the waveforms remain the same as before.

The square wave is high for 180° with a duty cycle of 0.5

The rectangular wave($V$-) stays high for $\dfrac{180° d_1}{0.5}$

Therefore, the phase difference between l and o is $0.5\left(180° - \dfrac{180° d_1}{0.5}\right)$

$$= 90°(1 - 2d_1)$$

Similarly for the rectangular wave($V_{out}$) the phase difference between l' and o'is $90°(1 - 2d_2)$

Therefore the phase difference between o and o' is $45° - 90°(1 - 2d_1) + 90°(1 - 2d_2)$

$$= 45° + 180°(d_1 - d_2)$$

New value of Phase difference at the first pole = 45° + 180°($d_1$ - $d_2$)      (12)

This method is useful as long as there is a phase difference to measure between the two waveforms. Hence there exists a limit on the values $d_1$ and $d_2$ beyond which this method may not be useful. This limit is determined to be $(d_2 - d_1) < 0.25$ by making Eqn.12 greater than zero for all $d_1$ and $d_2$, since only in that case would there be phase difference between the two waveforms to measure.

The principal drawback of the above approach is that the offset at $V-$ may be so great that the comparator C1 may not switch at all. In such cases, an offset cancellation circuit using a resistor divider network may have to be built on the IC. The advantage of the above circuit is that the offset cancellation need not be exact. The applied offset voltage can be just enough to cause the comparator to switch and then the above mentioned method may be used to determine the frequency of the first pole.
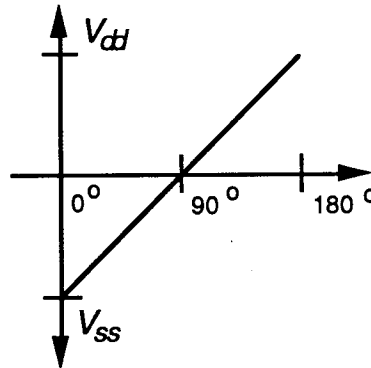


Figure 16. Phase Margin v/s Output DC Level

The phase margin of the opamp can be measured by applying an input signal at a frequency equal to the unity gain frequency of the opamp. For this measurement, it is imperative that the output is a square wave. The phase margin can be determined by the duty cycle of the output of the XOR gate. Alternatively the dc value of the XOR gate output can be determined by low pass filtering it. The phase margin can then be determined by using Fig.16.

This graph assumes that for a phase difference of 0° between two signals, the dc value of the output of the XOR gate will be at $V_{ss}$. Similarly, for a phase difference of 180°, the dc value will be at $V_{dd}$. Since the dc value is a linear function of the phase difference, the two points on the graph can be connected by straight line. The phase difference can thus be measured by noting the y-coordinate of the point on the line whose x-coordinate is the dc value of the XOR gate output.

The amplifier at $V$- can be switched out of the circuit as the signal strength at $V$- will be equal to that of $V_{out}$. At unity gain frequency the proper signal strength required to switch the comparators can be easily applied. Thus any phase error that the amplifier at $V$- might introduce in the phase margin measurement is avoided by removing it completely from the circuit.

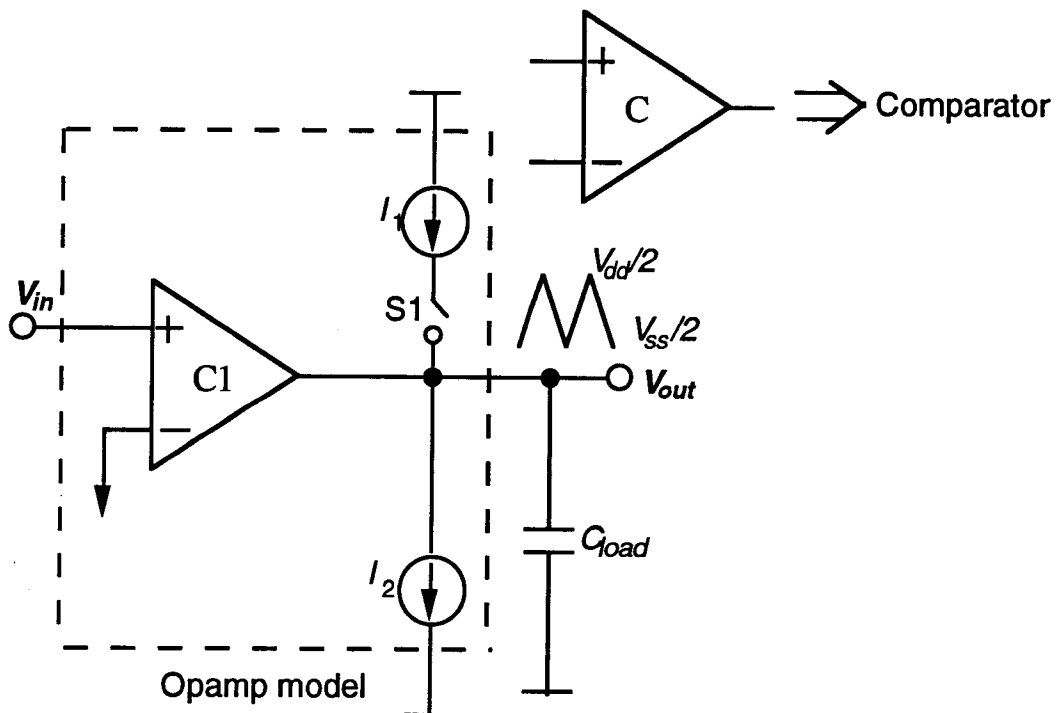

Figure 17. Model of a Slewing Opamp

## 2.3 Slew Rate Measurement

Measuring slew rate, like measuring the gain bandwidth product is done by placing the opamp in a circuit that oscillates. Since slew rate is a nonlinear phenomenon, the circuit needs to be designed so that the opamp behaves in a nonlinear fashion. A simple model of a slewing opamp is shown in figure 17.
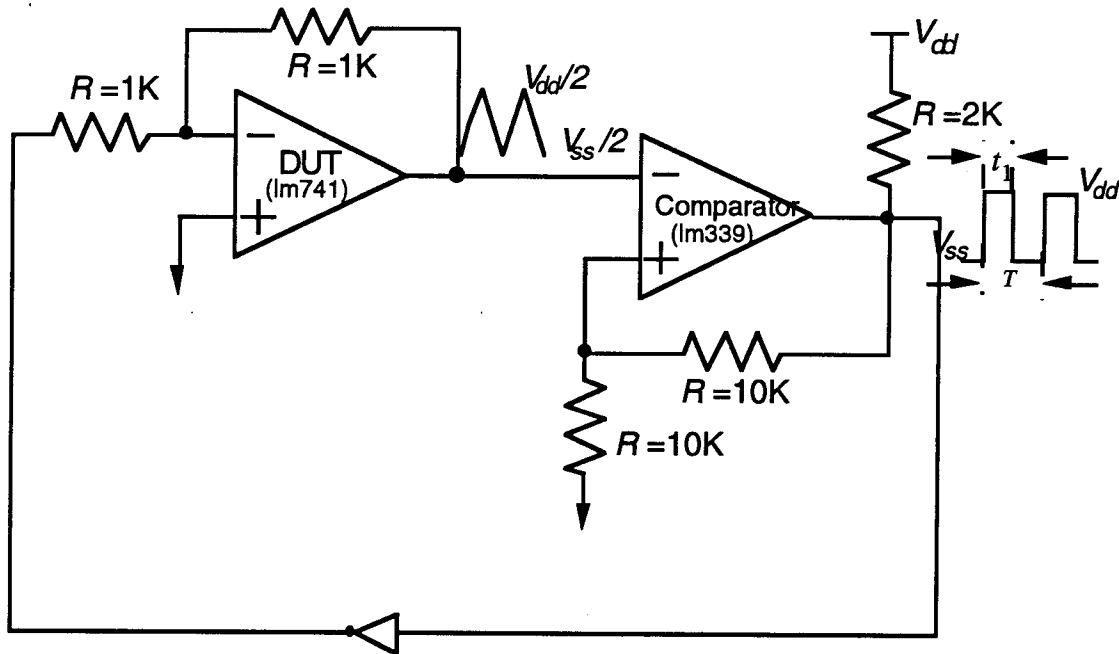


Figure 18. Slew Rate Measurement Setup

The opamp is modeled as a comparator which activates a switch to either charge or discharge the output capacitance. When $V+$ at comparator C1 is higher than $V-$, switch S1 closes causing the opamp output to slew up by charging the output capacitance at the rate of $dV_{out} / dt = (I_1 - I_2) /C$. The other case in which $V+$ is less than $V-$ leads to switch S1 being open causing the output to slew in the negative direction at the rate of $dV_{out}/dt = -I_2/C$. Slewing in the positive and negative directions are not necessarily equal. When the op-amp slews, its output voltage will be in the form of a ramp. If the input $V+$ is set to either of the voltage rails at $V_{dd}$ or $V_{ss}$, the op-amp must slew until the output reaches a voltage rail, or the input at $V+$ changes state. It must be pointed out here that the above

discussion is valid only in the case of a single stage opamp. In the case of a two stage opamp, it is the feedback capacitor that is charged up and down to cause slewing at the opamp output.

Hence in those cases the opamp output need not be loaded for the slewing operation to occur. The entire slew rate measurement circuit can be used without the opamp output having a load capacitance. The circuit proposed in Fig.18 causes the op-amp to slew either in positive or negative direction and prevents the output from reaching the voltage rails. Since it uses an LM741(a two-stage opamp) as the DUT, the opamp output is not loaded. The oscillatory behavior of this circuit can be understood by tracing the signal path of the circuit.

The analysis of the circuit begins by setting the input voltage at the $V-$ node of the opamp at $V_{ss}$ and the output of the comparator at $V_{dd}$. Since $V+$ of the op-amp is greater than $V-$, the output of the opamp begins to slew up. The positive terminal of the comparator sits at $V_{dd}/2$ The opamp output increases until $V_{out} > V_{dd}/2$ at which point the comparator switches state and the input to the op-amp at $V-$ becomes $V_{dd}$. Now the opamp output slews down giving rise to a triangular wave at the opamp output. If the positive going and the negative going slew rates are not equal, the output of the comparator is a rectangular wave. The period of the rectangular wave is used to determine the average slew rate. The duty cycle of the rectangular wave is used to calculate the positive and the negative slew rate of the opamp as will be shown by the equations that follow.

It can be seen that in one full cycle, the opamp output goes from $V_{dd}/2$ to $V_{ss}/2$ and back to $V_{dd}/2$. From this, the average slew rate of the opamp can be computed as :
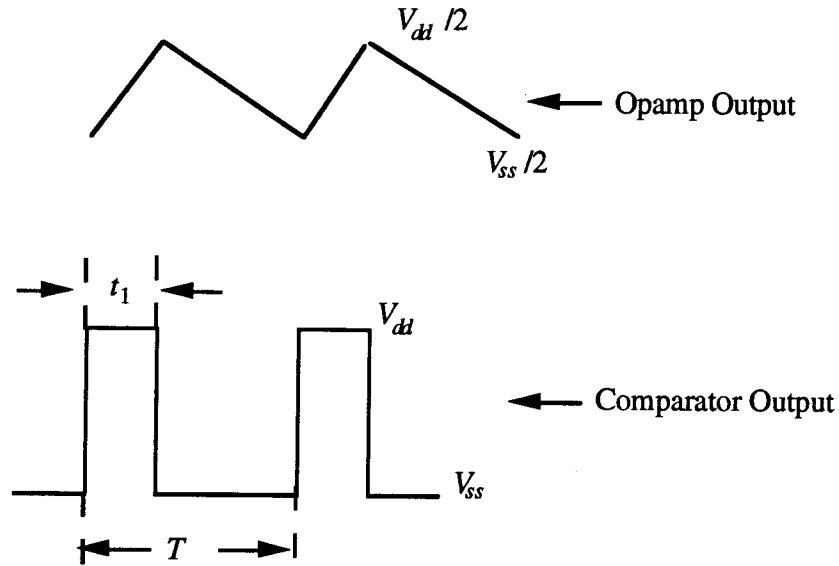
$$SR = \frac{V_{dd}/2 - V_{ss}/2}{T/2} \tag{12}$$

Figure 19. Comparator & Opamp Outputs in the Slew Rate Measuring Circuit

where $T$ = Period of oscillations of the comparator output ($1/f_{osc}$). From the above expression the average slew rate ($SR$) is determined to be,

$$SR = \frac{V_{dd} - V_{ss}}{T} \tag{13}$$

Substituting for $1/\ T = f_{osc}$, $SR$ is

$$SR = \left(V_{dd} - V_{ss}\right) f_{osc} \tag{14}$$

As mentioned previously, the positive and the negative going slew rates can be determined from the duty cycle of the comparator output.

Consider a possible waveform from the comparator shown in figure 19. The positive going slew rate can be expressed in terms of $t_1$, $T$ and $SR$ as

$$SR+ = 2*SR\left(\frac{T - t_1}{T}\right) \tag{15}$$

Likewise, the slew rate in the negative direction is

$$SR- = 2*SR\left(\frac{t_1}{T}\right) \qquad (16)$$

By adding a minimal amount of circuitry namely a comparator and two resistors, the slew rate of the op-amp can be characterized by measuring the duty cycles of a two-level output signal.

# 3. Experimental Results

The different test circuits presented in this report were evaluated to examine the accuracy and the feasibility of using these tests to characterize an opamp. The test setups consisted of an LM741 as the DUT and were implemented on a breadboard to make the measurements. The opamp characterization circuit using high speed buffers was laid out in silicon and submitted for fabrication with an on-chip folded cascode opamp as the DUT. The high speed buffer will be characterized to measure its various dc and ac parameters.

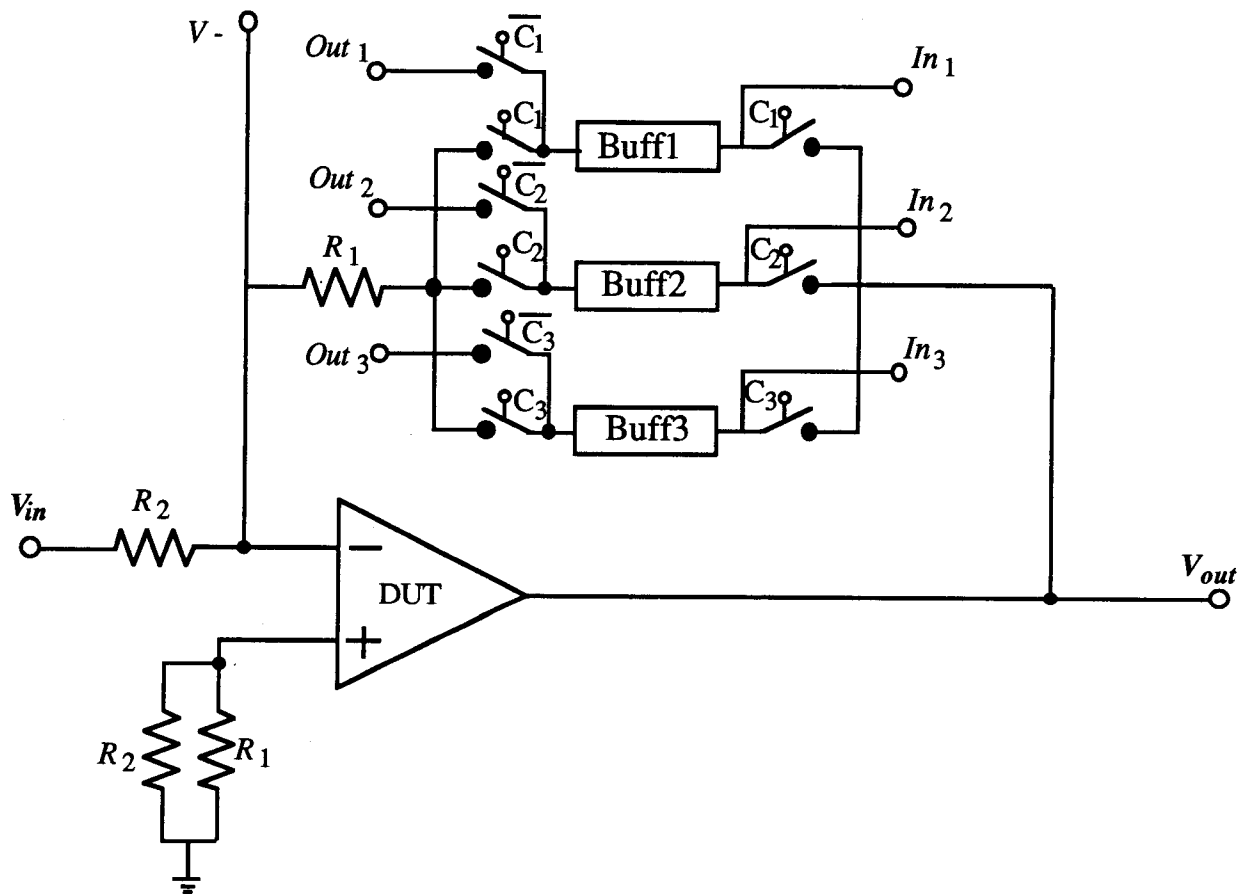## 3.1 Opamp Characterization using Buffers



Figure 20. Block Diagram of the Test Chip

The test circuit used for characterizing an opamp using buffers was laid out in silicon in a $2\mu$ p-well process. The chip had an on-chip folded cascode opamp to be used as

the device under test. The test circuit was laid out so that the opamp could be switched in or out of the test loop and hence could be characterized separately or in conjunction with the testable opamp. The buffer too could be included in the test loop or be characterized separately by means of CMOS switches. The block diagram of the test chip is shown in figure 20. Buff3 represents the buffer described in this report and it is switched into the test loop when C3 is high and is switched out when C3 goes low. The buffer along with the DUT was extracted from the layout and resimulated using HSPICE.



Figure 21. AC Response of the Buffer
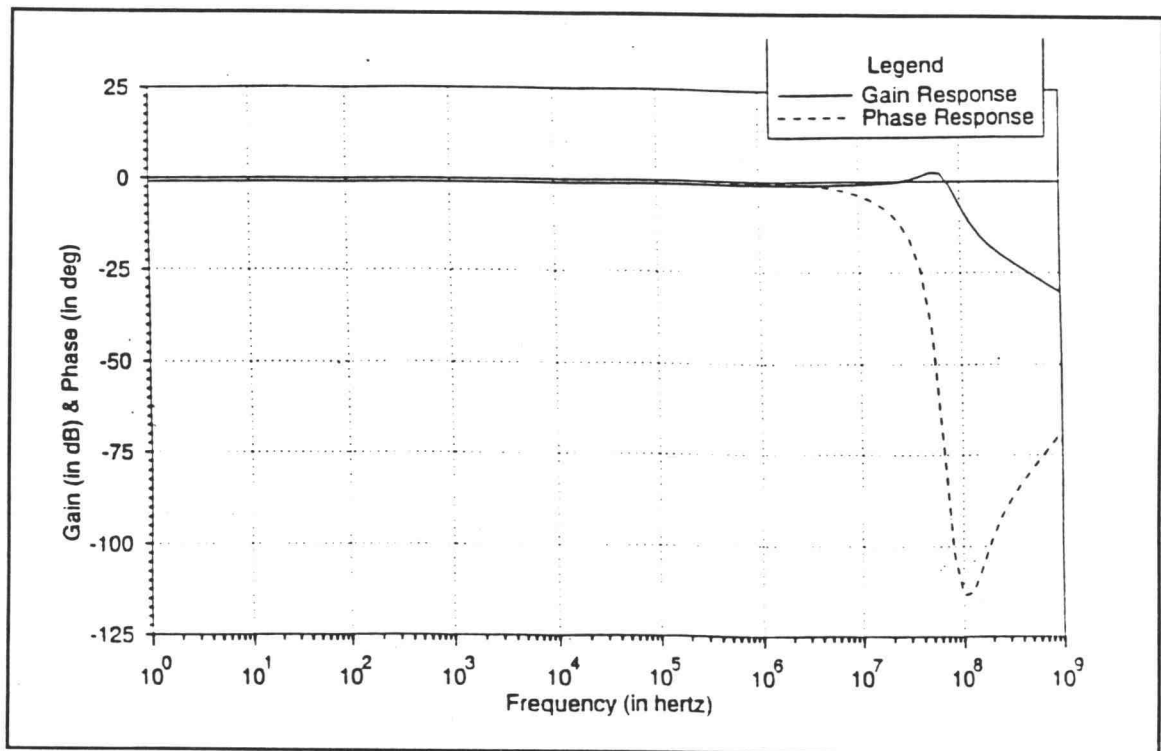
Figure 21 & 22 are the AC transfer curve and the buffer response to a large signal input(2V peak-to-peak square wave input signal). The buffer has a 3 dB frequency of nearly 30 MHz with rise and fall times of 17 ns. The bandwidth of the buffer is sufficient for testing our opamp. The harmonic distortion of the buffer was determined to be 0.2% for a 0.5V p-p sinusoidal input signal.
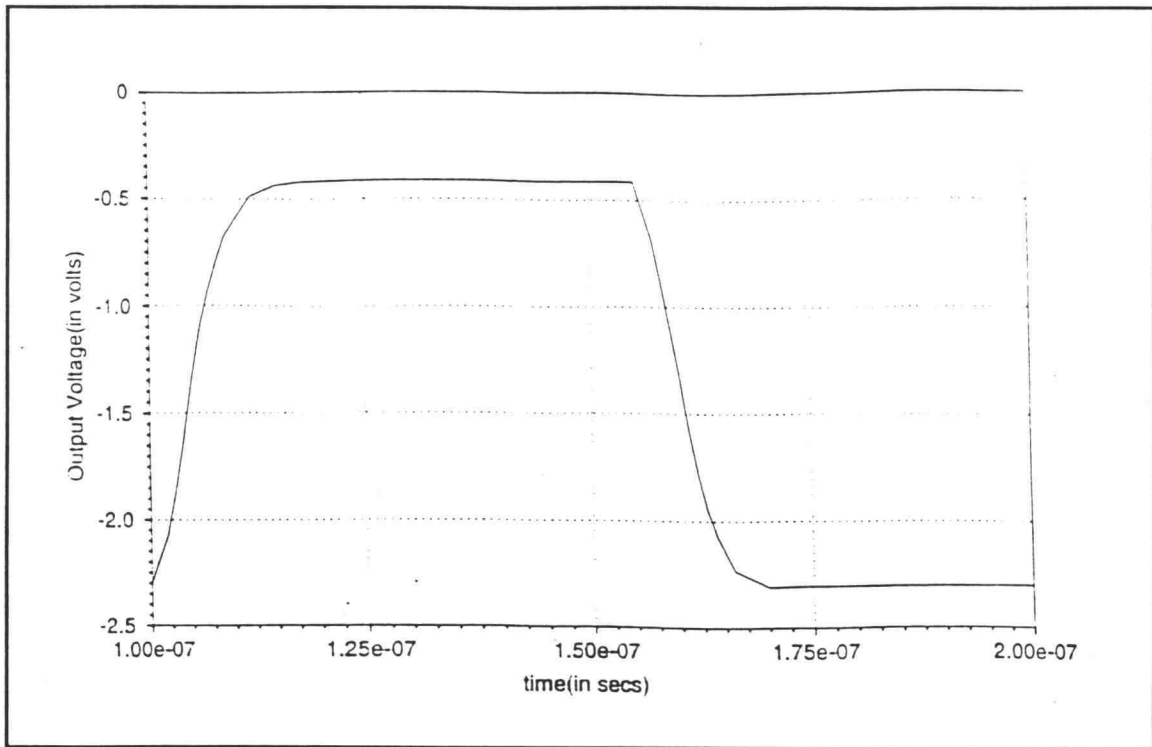
Figure 22. Large Signal Response of the Buffer

The gain response of the DUT with the buffer in the feedback loop was characterized using the extracted SPICE deck. The voltage at $V$ - and $V_{out}$ were monitored to plot the ac response shown in figure 23.

On-chip characterization of the buffer was carried out on the chip received from MOSIS. The gain of the buffer was determined to be 0.85 and its linear range was 1.5 volts. The rise and fall times for a 0.8V step input were 0.5μs and 0.2μs respectively. The reason for these slow responses is that the buffer is loaded with at least 25 pF at its output due to the probe, pad and test bed capacitances(See appendix B for chip measurements).

## 3.2 Gain Bandwidth Measurement

The circuit in figure 11 was implemented on a breadboard using an LM741 as the DUT and discrete resistors and capacitors to provide for the correct positive and the
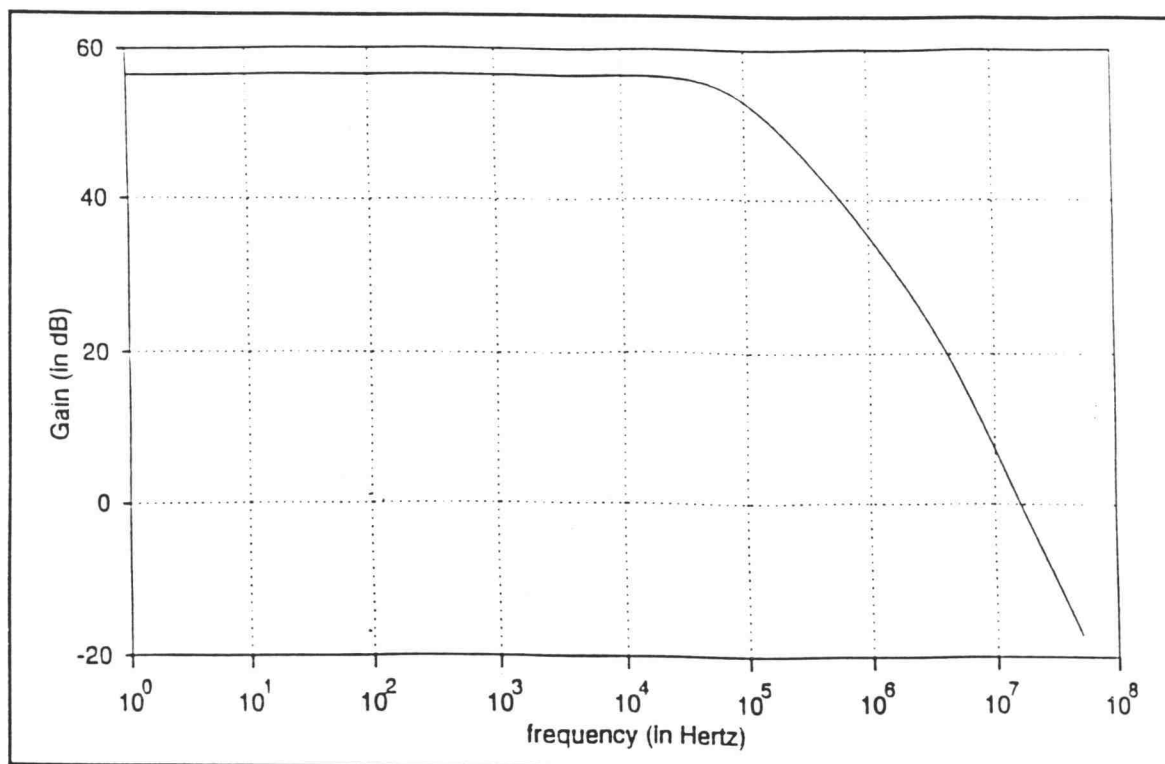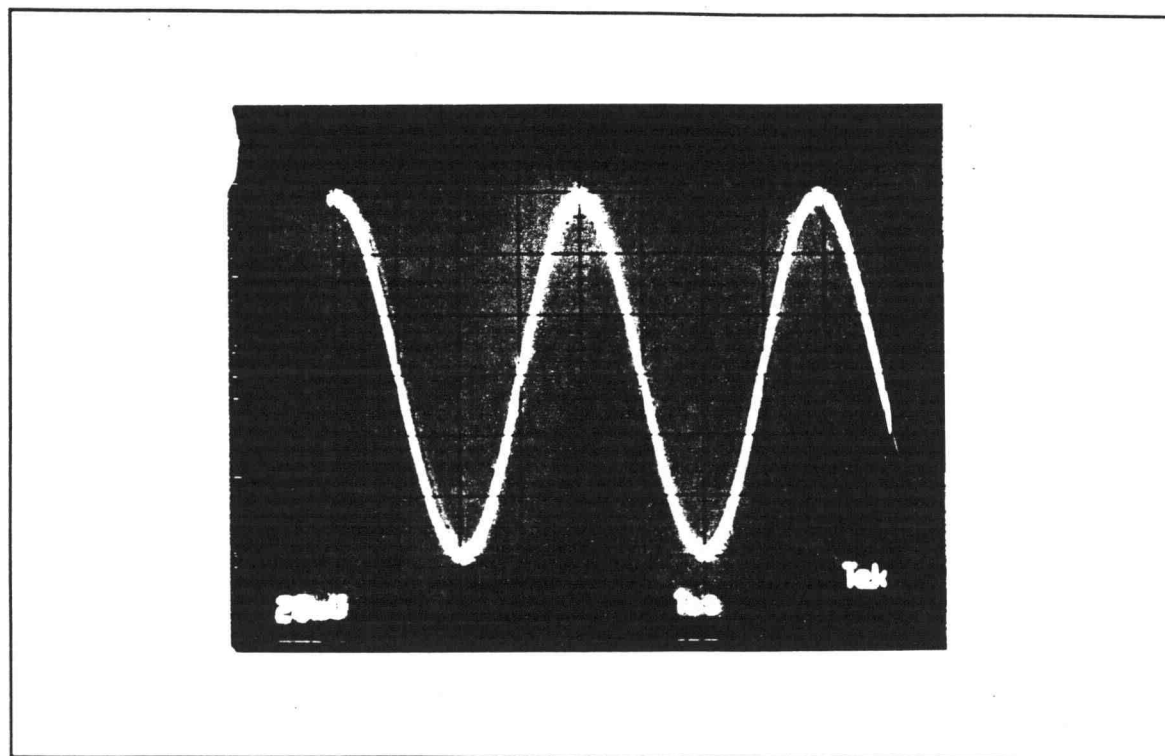
Figure 23. Gain Response of the DUT



Figure 24. GBW Measurement

negative feedback gains. A potentiometer was used in place of $R_2$ to make the positive feedback tunable. The potentiometer is varied so that the opamp output does not slew or clip.

The frequency of the sinewave was measured to be 262 kHz (See Fig. 24), which corresponds to a unity gain frequency of 823 kHz(See Eqn. 10). The unity gain frequency was measured using the test circuit shown in figure 25[4] and was measured at 826 kHz for a 100 mV p-p sinewave input. The two values were found to be in close agreement.



$$f_u = f_{in} V_{out}/V_{in}$$
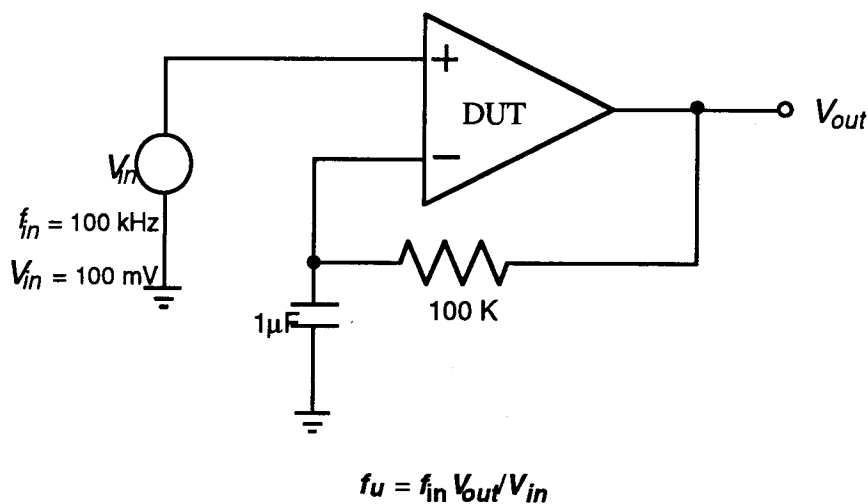
Figure 25. Conventional Test Setup for GBW Measurement

## 3.3 First Pole Measurement

The opamp LM741 has a gain of 110 dB with its first pole at 5Hz. It was not possible to make the measurements at such low frequencies using the available oscilloscope and signal generator. Thus to evaluate the test circuit, the gain of the opamp was reduced to 150 by putting it in the inverting mode as shown in figure 26.

The signals at $V_{in}$ and $V_{out}$ were of sufficient strength so as to switch the two comparators, since the gain of the entire setup was only 150. Some amount of offset cancellation was required for comparator C2 which sits at the output of the opamp to

Figure 26. Experimental Test Setup for First Pole Measurement
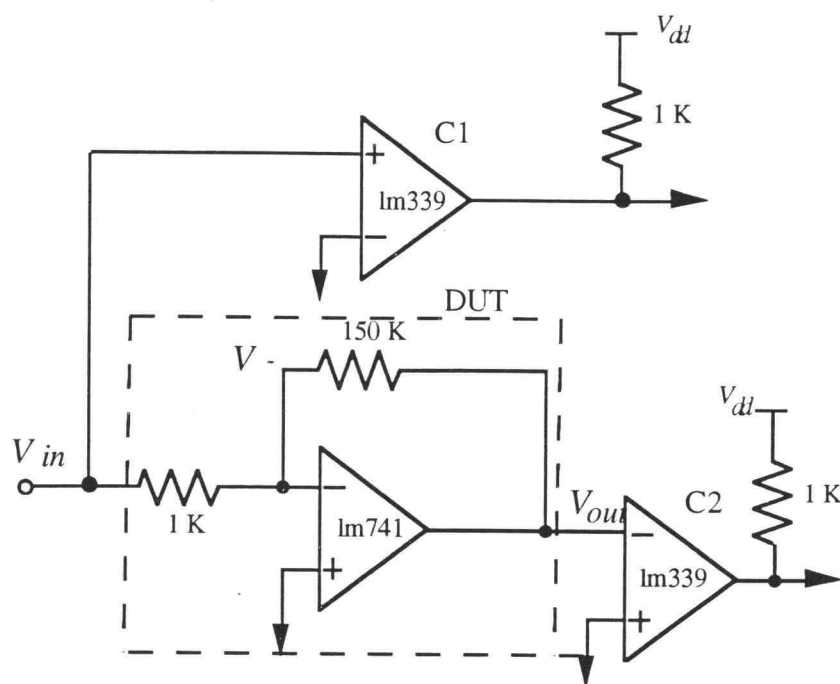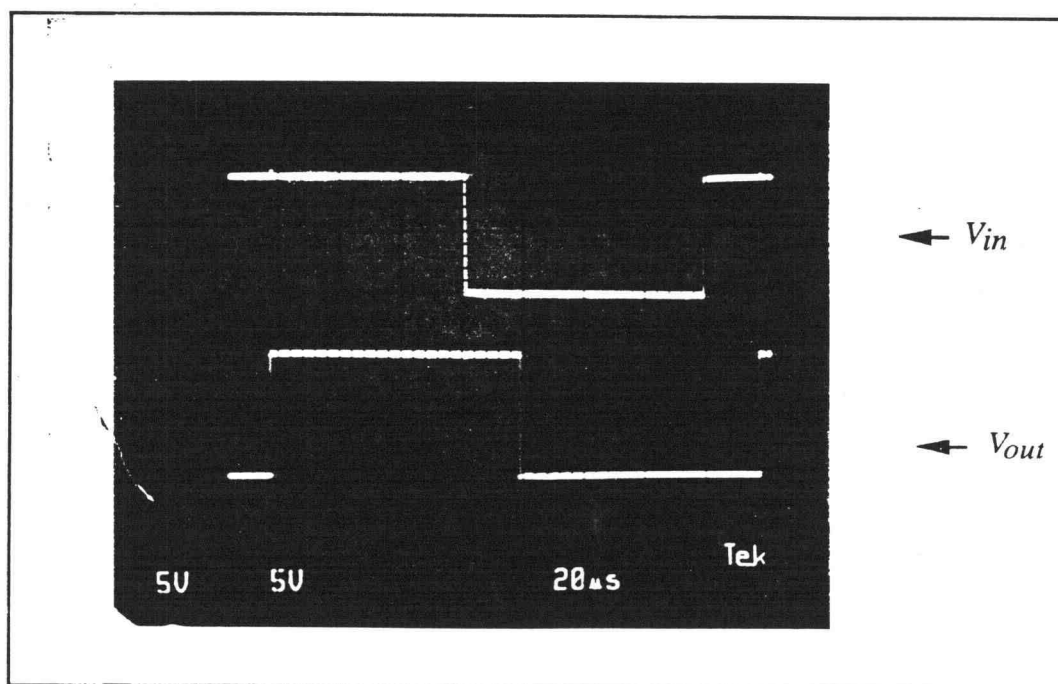


Figure 27. Comparator Outputs in Phase Measurement Circuit with Offset Cancellation

obtain square pulses. The phase difference between the two square pulses was 44.6° at a signal frequency of 6.89 kHz. The outputs of the comparators at the first pole frequency are shown Fig.27.

To test the method proposed in Eqn.12, the offset voltage applied to the positive input of comparator C2 was varied and the phase difference between the leading edge of the two rectangular pulses were measured. The measured values and the calculated values for the phase difference for different values of d1-d2 is shown in figure 28. The measured values and the calculated values are in close agreement as shown by the plot.
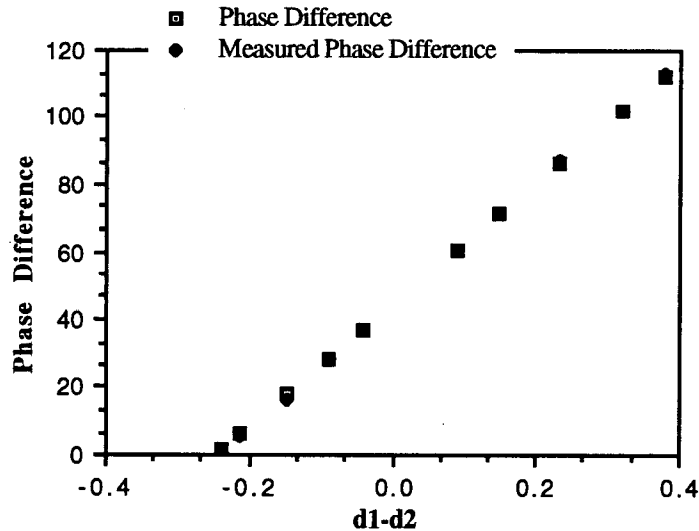


Figure 28. Calculated and Measured Phase Difference v/s (d1-d2)

## 3.4 Slew Rate Measurement

The slew rate measurement circuit was implemented on a breadboard with an LM741 as the DUT. The comparator used in the setup was an LM339. It should be noted that the output of the comparator is an open collector type which must be tied to the positive supply through a resistor. In the setup used for evaluating this circuit, the pull-up resistor had a value of 2K.

The frequency of the square wave at the output of the comparator was determined to be 60 kHz (See Fig.29). Since the output of the comparator in this case is an open collector type, the output does not go all the way to $V_{dd}$ but only to $0.95 V_{dd}$, the formula for average slew rate in Eqn.14 has to be modified to $(0.95 V_{dd} - V_{ss})f_{osc}$. The average slew rate was measured at 0.58 V/μs. The above problem of the comparator output not going all the way to $V_{dd}$ will not occur in the case of comparators that do not have open collector outputs. Consequently Eqn. 11 can be used without modification.
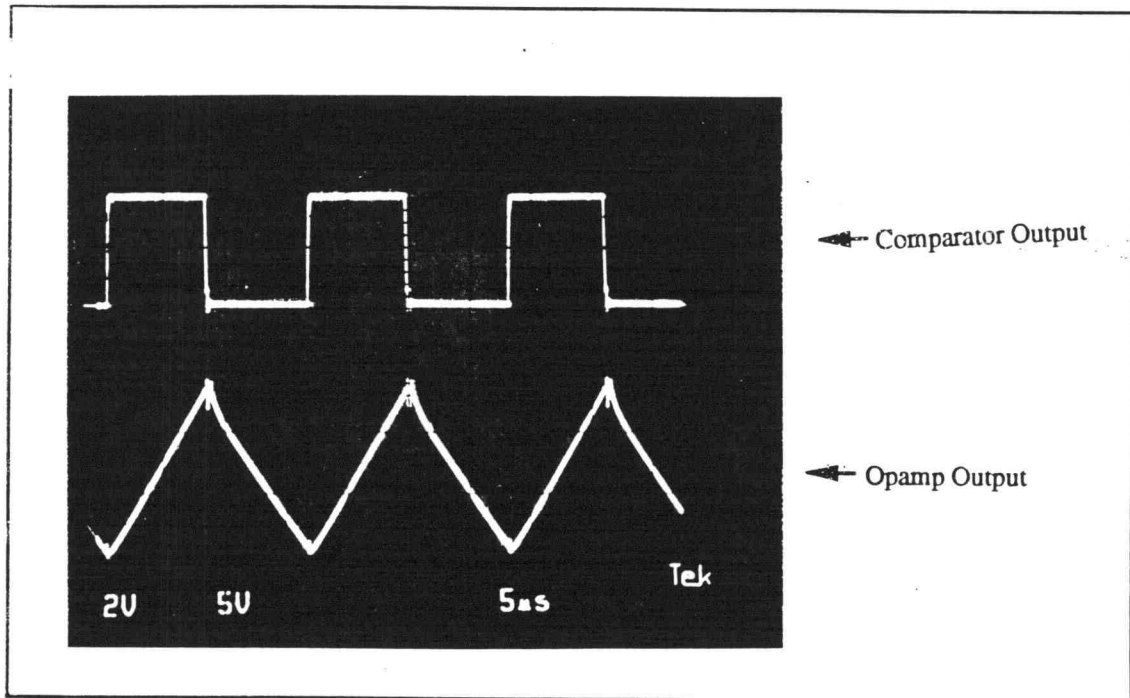


Figure 29. Output Waveforms for Slew Rate Measurement
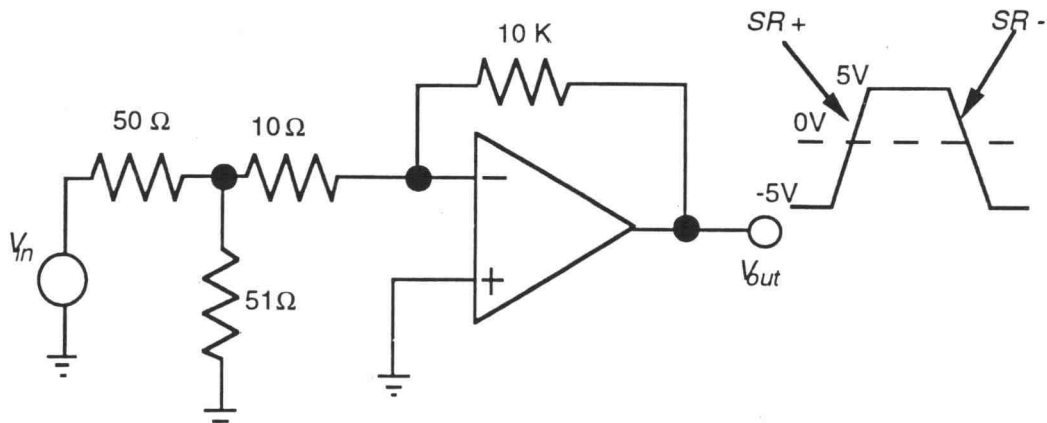


Figure 30. Conventional Test Setup for Slew Rate Measurement

The duty cycle in this case was found to be 0.5 meaning that the positive going and negative going slew rates were each 0.58 V/μs each. The slew rate was determined by using the conventional test setup shown in figure 30. The average slew rate using this method was determined to be 0.61 V/μs. Thus the two values were in close agreement with each other.

# 4. Conclusions

A number of strategies to test an opamp have been proposed and evaluated in this project. The focus of this work was to devise test strategies so that frequency domain parameters could be measured with the help of two level signals. These circuits were implemented on a breadboard where their feasibility was demonstrated.

## 4.1 Conclusions

The test setup used to measure the frequency response of an opamp using buffers was proposed in [1] and it was modified to measure just the gain response of the opamp, since the proposed CMRR measurement was highly dependent on the value of the resistors used. Original work was done in the design of high speed CMOS buffers that were used in the feed-back loop of the test circuitry. This test methodology reflects the philosophy of the frequency domain measurement techniques used to characterize the opamps in the past.

The other method to characterize the gain and phase response of an opamp makes use of an oscillatory circuit and the gain measurement circuit described in[1]. The oscillatory circuit used to measure the gain bandwidth product of an opamp has a sinusoidal output which may be converted into a square wave using a comparator. The principal advantages of this circuit are that it requires very few components, does not require any external input and the gain bandwidth product is a function of the square of the output frequency. Thus the gain-bandwidth measurement is reduced to a simple task of determining the output frequency. The main drawback is that the feedback gain has to be adjusted to a particular value to make sure that the opamp output does not slew which would lead to erroneous measurements.

The test circuit used to measure the first pole of the opamp is a direct offshoot of the opamp characterization technique using buffers. The major difference is that phase measurements are made instead of amplitude measurements making this technique relatively

immune to noise. Also, the characterization of extremely high gain opamps can be done accurately since the first pole is characterized as the point at which the phase difference between the opamp input and output is $45^\circ$ and not by determining the point at which the gain falls by 3dB from its DC value. An additional use of this test is that it can be used to measure the phase margin of the opamp once its unity gain frequency has been determined.

A non-linear parameter of the opamp, i.e., its slew rate, was successfully measured by using the opamp in a Schimitt trigger circuit. This test has the extra overhead of an additional comparator in the circuit . Once again, the output of this test is a two level signal that can be easily measured using a digital tester to determine the frequency of oscillation.

## 4.2 Future Work

The test methods described in this report give a number of techniques to characterize an opamp. Much work needs to be done to incorporate these circuits into VLSI systems. The resistors used in the circuit for measuring gain using the buffers can be replaced with switched capacitor equivalents so that the area occupied in a chip may be reduced.

The gain-bandwidth circuit needs to be made self testing. This can be achieved if the resistor divider network is replaced with a variable attenuation for $R_2$ in figure 11. A variable resistor may be implemented by using a NMOS transistor in the linear region. The gate of this transistor can be controlled by the opamp output to make the circuit self testing. Since the output of the opamp must be small signal the amplitude of the output can be limited by using a peak detector at the opamp output. The output of the peak detector is then fed to loop filter whose output would provide the DC bias required to control the gate of the NMOS transistor.

In the phase measuring circuit, the immediate need is to design high speed comparators. As is the case of the circuit used in opamp characterization the resistors can be replaced with switched capacitor equivalents to save on silicon real estate.

The slew rate circuit again can have its resistors in the circuit replaced with switched capacitor circuits to make it more compact. The design of a good area efficient comparator with a moderate gain would be a big plus in the implementation of this circuit in a VLSI system.

## 4.3 Summary

In summary, this report presents a fresh view at opamp characterization using digital signals. The merits of this method lie in the fact that these measurements are fast, accurate and are relatively immune to noise. One important advantage of using these techniques is that digital testers can be easily configured to make these measurements. In addition the circuits presented require simple analog blocks for implementation in VLSI systems. This work presents a firm theoretical and practical background for incorporating these circuits into VLSI systems. Further work needs to be done in designing test circuits for other analog blocks as comparators, data converters, phase locked loops etc. As a final note it might be useful to start thinking in terms of test methodologies for large analog blocks once test methods for the low level analog cells have been devised.

# Bibliography

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3. K. Martin and A. S. Sedra, "On the stability of the phase-lead integrator," *IEEE Trans. on Circuits and Systems*, vol. CAS-24, pp. 321-324, June 1977.

4. T. M Frederiksen, "Intuitive IC Opamps," *National's Semiconductor Technology Series,* 1984.

5. R. Gregorian and G.C. Temes, *"Analog MOS Integrated Circuits for Signal Processing," John Wiley & Sons,* 1986

6 . J. E Solomon, "The Monolithic Op amp : A Tutorial study," *IEEE Journal of Solid State Circuits,* vol. sc-9, pp.314-332, December 1974.
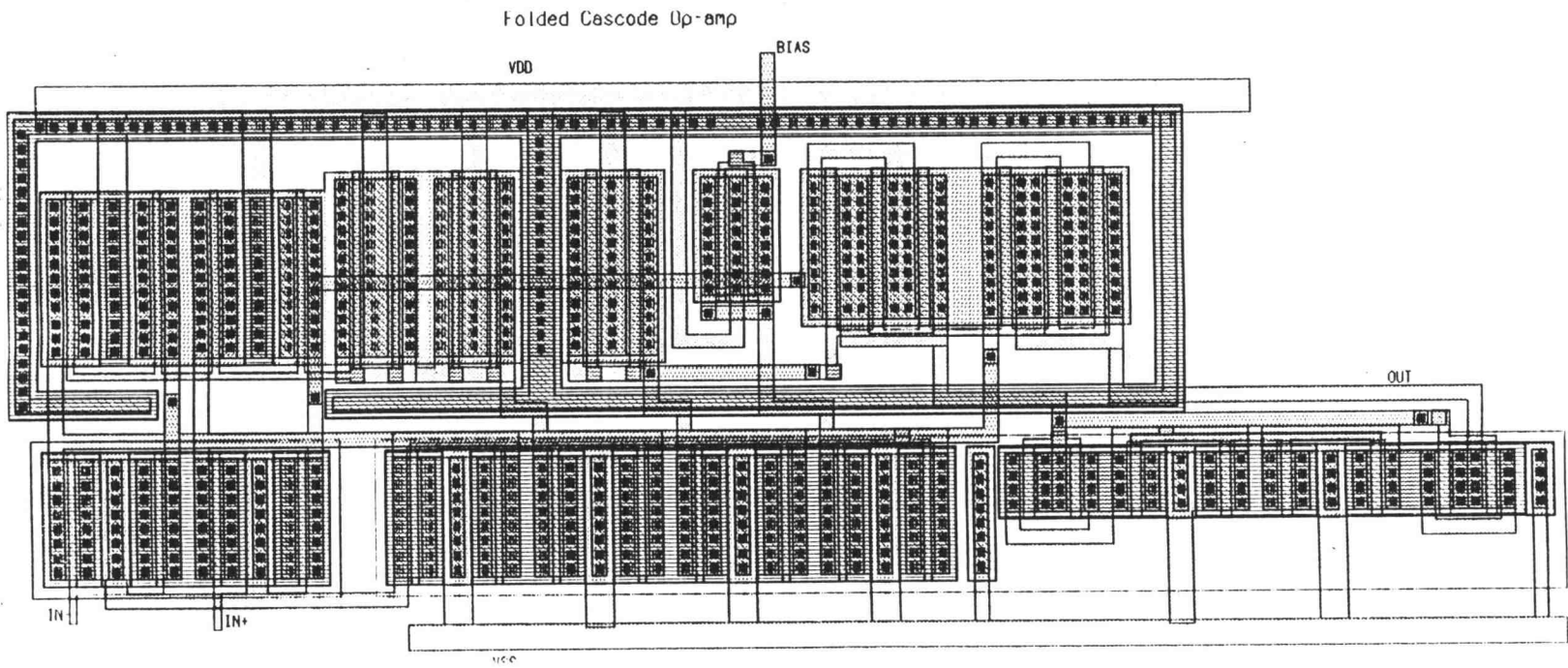
APPENDIX

# Appendix A

This appendix includes the layout of the buffer that was submitted for fabrication on a 2-micron MOSIS p-well process as the first plot. The second plot in this buffer is a plot of the opamp used as the DUT in this test chip.

Slew rate enhanced buffer

VB_OP

VDD

IN

VB_SRC

VSS

OUT

41

Folded Cascode Op-amp
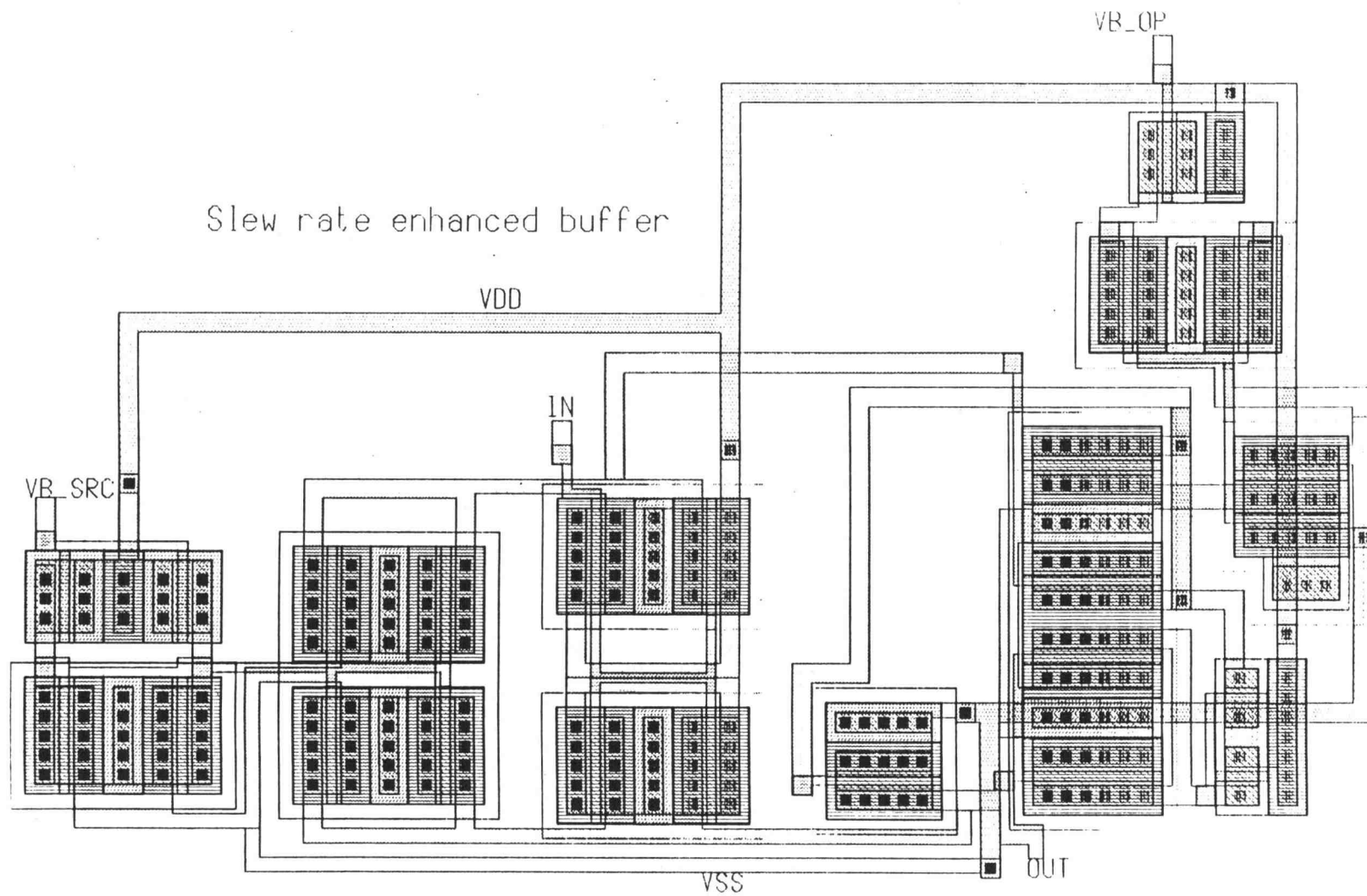
## Appendix  B

The first picture in this appendix is the response of the slew rate enhanced buffer to a 5kHz sinusoidal input. The waveform on the top is the input to the buffer and the waveform below it is the buffer output. The second picture is the buffer response to a 0.8V p-p square wave input signal. The third picture shows the linear range of the buffer.

>1U    1U                    0.1ms         Tek



>0.2V              0.5us         Tek

>0.5V   0.5V   Tek
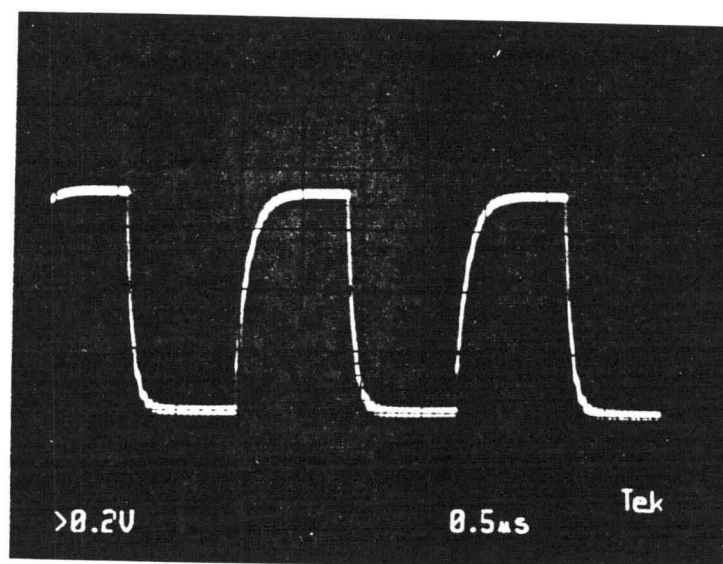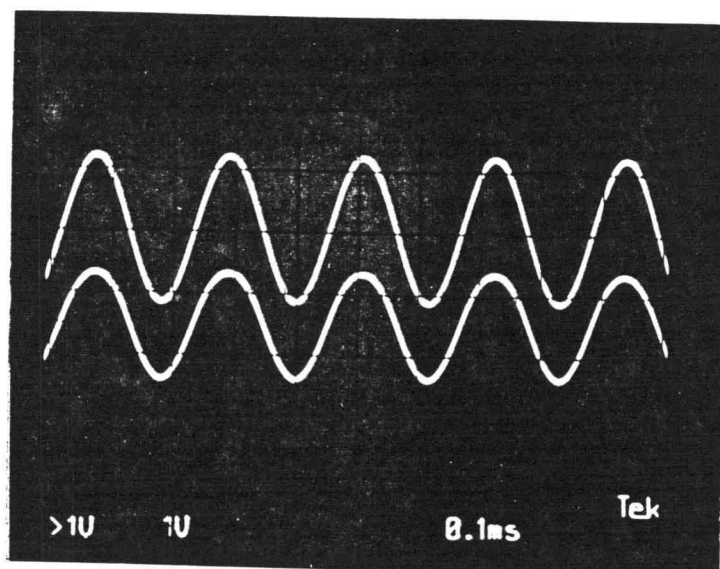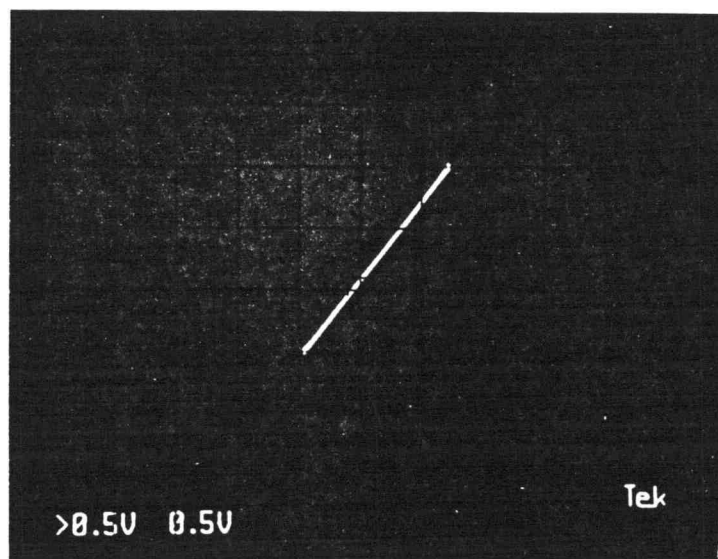
# Appendix C

The first listing in this appendix is the SPICE deck of the buffer that was extracted from the layout using the standard extraction tools provided by MENTOR GRAHPICS.

The second listing is that of the opamp used as the device under test in the test chip.

```
Source follower
.subckt dynBuff VDD VSS IN OUT VB_OP VB_SRC
* devices:
m0 1 VB_SRC VDD VDD Mosis1_P l=2u w=15u ad=75p as=75p pd=40u
ps=40u
m1 1 VB_SRC VDD VDD Mosis1_P l=2u w=15u ad=75p as=75p pd=40u
ps=40u
m2 9 VB_OP VDD VDD Mosis1_P l=2u w=15u ad=75p as=75p pd=40u
ps=40u
m3 6 6 VDD VDD Mosis1_P l=2u w=7u ad=35p as=35p pd=24u ps=24u
m4 8 6 VDD VDD Mosis1_P l=2u w=7u ad=35p as=35p pd=24u ps=24u
m5 1 1 VSS VSS Mosis1_N l=2u w=20u ad=100p as=100p pd=50u ps=50u
m6 1 1 VSS VSS Mosis1_N l=2u w=20u ad=100p as=100p pd=50u ps=50u
m7 OUT 1 VSS VSS Mosis1_N l=2u w=20u ad=100p as=100p pd=50u ps=50u
m9 OUT 1 VSS VSS Mosis1_N l=2u w=20u ad=100p as=100p pd=50u ps=50u
m8 5  1 VSS VSS Mosis1_N l=2u w=20u ad=100p as=100p pd=50u ps=50u
m10 5 1 VSS VSS Mosis1_N l=2u w=20u ad=100p as=100p pd=50u ps=50u
m11 VDD IN OUT OUT Mosis1_N l=2u w=20u ad=100p as=100p pd=50u
ps=50u
m13 VDD IN OUT OUT Mosis1_N l=2u w=20u ad=100p as=100p pd=50u
ps=50u
m12 VDD IN 5 5 Mosis1_N l=2u w=20u ad=100p as=100p pd=50u ps=50u
m14 VDD IN 5 5 Mosis1_N l=2u w=20u ad=100p as=100p pd=50u ps=50u
m15 OUT 8 VSS VSS Mosis1_N l=2u w=20u ad=100p as=100p pd=50u
ps=50u
m16 9 9 VSS VSS Mosis1_N l=2u w=20u ad=100p as=100p pd=50u ps=50u
m21 9 9 VSS VSS Mosis1_N l=2u w=20u ad=100p as=100p pd=50u ps=50u
m17 6 OUT 7 7 Mosis1_N l=2u w=25u ad=125p as=125p pd=60u ps=60u
m18 6 OUT 7 7 Mosis1_N l=2u w=25u ad=125p as=125p pd=60u ps=60u
m19 8 5 7 7 Mosis1_N l=2u w=25u ad=125p as=125p pd=60u ps=60u
m20 8 5 7 7 Mosis1_N l=2u w=25u ad=125p as=125p pd=60u ps=60u
m22 7 9 VSS VSS Mosis1_N l=2u w=20u ad=140p as=100p pd=54u ps=50u
m23 7 9 VSS VSS Mosis1_N l=2u w=20u ad=100p as=140p pd=50u ps=54u


* lumped capacitances:
c1 1 0 45f
c2 VSS 0 210f
c3 VSS 1 2.92f
c4 VDD 0 170f
c5 VDD 1 0.413f
c6 VDD VSS 4.83f
c7 OUT 0 80.3f
c8 OUT VSS 4.06f
c9 OUT VDD 1.02f
c10 5 0 87.3f
c11 5 VSS 0.617f
c12 5 VDD 1.24f
c13 6 0 27.3f
c14 6 VSS 0.68f
c15 6 VDD 0.137f
c16 6 OUT 0.0861f
c17 7 0 70.3f
c18 7 VSS 4.98f
c19 7 VDD 0.68f
c20 7 OUT 0.999f
c21 7 5 0.851f
c22 7 6 0.942f
c23 8 0 63.3f
```

```
c24 8 VSS 0.523f
c25 8 VDD 0.137f
c26 8 OUT 0.01f
c27 8 5 0.896f
c28 8 6 0.413f
c29 8 7 1.37f
c30 9 0 34.4f
c31 9 VSS 2.76f
c32 9 VDD 0.459f
c33 9 7 0.37f
c34 VB_SRC 0 9.57f
c35 VB_SRC 1 0.133f
c36 VB_SRC VDD 0.296f
c37 IN 0 20.6f
c38 IN VDD 2.52f
c39 IN 5 0.511f
c40 VB_OP 0 4.96f
c41 VB_OP VDD 0.136f
.ends dynBuff

X1 1 2 3 4 5 6 dynBuff

vdd 1 0 2.5
vss 2 0 -2.5
vin 3 0 dc -0.8
*vin 3 0 pulse (-1 1 0 5ns 5ns 50ns 100ns)
*vin 3 0 sin(-1 .1 1e7 0 0 0)
*vin 3 0 dc 0 ac=1
vb1 5 0 dc 0.8
vb2 6 0 dc 0.8

cl 4 2  5pF

.op
.tf v(4) vin
*.dc vin -2.5 2.5 0.1
*.plot dc v(4)
*.tran .1ns 200n
*.print tran v(4) v(x1.5) v(x1.8)
*.four 1e7 v(4)
*.plot
*.print  dc v(4) v(3)
*.ac dec 10 1hz 1000MEG
*.plot ac vdb(4)

.include //louie/users/karthik/model/chip/hdr

.end
```

Folded Cascode opamp

```
.subckt foldCasc VDD BIAS OUT IN- IN+ VSS
* devices:
m0 VDD 5 2 VDD mosis1_p l=2u w=45u ad=225p as=225p pd=100u ps=100u
m1 2 5 VDD VDD mosis1_p l=2u w=45u ad=225p as=225p pd=100u ps=100u
m2 VDD 5 4 VDD mosis1_p l=2u w=45u ad=225p as=225p pd=100u ps=100u
m3 4 5 VDD VDD mosis1_p l=2u w=45u ad=225p as=225p pd=100u ps=100u
m4 VDD 5 5 VDD mosis1_p l=2u w=50u ad=450p as=250p pd=118u ps=110u
m5 5 5 VDD VDD mosis1_p l=2u w=50u ad=250p as=450p pd=110u ps=118u
m6 VDD 5 5 VDD mosis1_p l=2u w=50u ad=450p as=250p pd=118u ps=110u
m7 5 5 VDD VDD mosis1_p l=2u w=50u ad=250p as=450p pd=110u ps=118u
m8 VDD 7 7 VDD mosis1_p l=3u w=50u ad=450p as=250p pd=118u ps=110u
m9 7 7 VDD VDD mosis1_p l=3u w=50u ad=250p as=450p pd=110u ps=118u
m10 VDD BIAS 8 VDD mosis1_p l=2u w=33u ad=198p as=165p pd=78u
ps=76u
m11 8 BIAS VDD VDD mosis1_p l=2u w=33u ad=165p as=198p pd=76u
ps=78u
m12 9 7 4 VDD mosis1_p l=3u w=40u ad=400p as=200p pd=100u ps=90u
m13 4 7 9 VDD mosis1_p l=3u w=40u ad=400p as=400p pd=100u ps=100u
m14 9 7 4 VDD mosis1_p l=3u w=40u ad=200p as=400p pd=90u ps=100u
m15 OUT 7 2 VDD mosis1_p l=3u w=40u ad=400p as=200p pd=100u ps=90u
m16 2 7 OUT VDD mosis1_p l=3u w=40u ad=400p as=400p pd=100u
ps=100u
m17 OUT 7 2 VDD mosis1_p l=3u w=40u ad=200p as=400p pd=90u ps=100u
m18 3 IN- 2 3 mosis1_n l=2u w=33u ad=165p as=165p pd=76u ps=76u
m19 2 IN- 3 3 mosis1_n l=2u w=33u ad=165p as=165p pd=76u ps=76u
m20 3 IN+ 4 3 mosis1_n l=2u w=33u ad=165p as=165p pd=76u ps=76u
m21 4 IN+ 3 3 mosis1_n l=2u w=33u ad=165p as=165p pd=76u ps=76u
m22 VSS 8 3 VSS mosis1_n l=2u w=33u ad=165p as=165p pd=76u ps=76u
m23 3 8 VSS VSS mosis1_n l=2u w=33u ad=165p as=165p pd=76u ps=76u
m24 VSS 8 5 VSS mosis1_n l=2u w=33u ad=165p as=165p pd=76u ps=76u
m25 5 8 VSS VSS mosis1_n l=2u w=33u ad=165p as=165p pd=76u ps=76u
m26 VSS 8 7 VSS mosis1_n l=2u w=33u ad=165p as=165p pd=76u ps=76u
m27 7 8 VSS VSS mosis1_n l=2u w=33u ad=165p as=165p pd=76u ps=76u
m28 VSS 8 8 VSS mosis1_n l=2u w=33u ad=165p as=165p pd=76u ps=76u
m29 8 8 VSS VSS mosis1_n l=2u w=33u ad=165p as=165p pd=76u ps=76u
m30 9 9 10 VSS mosis1_n l=3u w=16u ad=160p as=80p pd=52u ps=42u
m31 10 9 9 VSS mosis1_n l=3u w=16u ad=80p as=160p pd=42u ps=52u
m32 VSS 10 10 VSS mosis1_n l=3u w=16u ad=80p as=80p pd=42u ps=42u
m33 10 10 VSS VSS mosis1_n l=3u w=16u ad=80p as=80p pd=42u ps=42u
m34 VSS 10 12 VSS mosis1_n l=3u w=16u ad=80p as=80p pd=42u ps=42u
m35 12 10 VSS VSS mosis1_n l=3u w=16u ad=80p as=80p pd=42u ps=42u
m36 OUT 9 12 VSS mosis1_n l=3u w=16u ad=160p as=80p pd=52u ps=42u
m37 12 9 OUT VSS mosis1_n l=3u w=16u ad=80p as=160p pd=42u ps=52u
* lumped capacitances:
c1 VDD 0 460f
c2 2 0 100f
c3 2 VDD 2.1f
c4 3 0 107f
c5 3 2 6.1f
c6 4 0 94.9f
c7 4 VDD 6.4f
c8 4 2 6.22f
c9 4 3 1.26f
c10 5 0 136f
c11 5 VDD 3.36f
c12 5 2 5.19f
```

```
c13 5 3 0.563f
c14 5 4 3.96f
c15 VSS 0 347f
c16 VSS 3 1.16f
c17 VSS 5 1.16f
c18 7 0 133f
c19 7 VDD 2.34f
c20 7 2 5.19f
c21 7 4 1.5f
c22 7 5 0.563f
c23 7 VSS 1.16f
c24 8 0 98.1f
c25 8 VDD 2.19f
c26 8 2 5.1f
c27 8 3 1.3f
c28 8 4 1.33f
c29 8 5 1.63f
c30 8 VSS 1.16f
c31 8 7 2.83f
c32 9 0 89.9f
c33 9 2 0.544f
c34 9 4 1.38f
c35 9 7 1.55f
c36 10 0 52.8f
c37 10 VSS 0.903f
c38 10 9 0.4f
c39 OUT 0 66.6f
c40 OUT 2 1.45f
c41 OUT 7 0.592f
c42 OUT 9 0.446f
c43 12 0 30.8f
c44 12 VSS 0.883f
c45 12 10 2.73f
c46 12 OUT 0.453f
c47 BIAS 0 14.7f
c48 BIAS VDD 1.83f
c49 BIAS 4 0.272f
c50 BIAS 8 0.0667f
c92 IN- 0 11.9f
c93 IN- 3 0.444f
c94 IN+ 0 12.1f
c95 IN+ 3 0.74f
.ends foldCasc

x1 vd vb vo 0 vip vs foldCasc

cload vo vs 5p

vbias vb 0 dc 1.0
vdd vd 0 2.5
vss vs 0 -2.5

vin vip 0 dc 0 ac =1

.ac dec 10 1 50MEG
.print vdb(vo)
.include //louie/users/karthik/model/chip/hdr
.end
```