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Title: An Ultra Low Power Frequency Reference For Timekeeping Applications

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An ultra low power crystal oscillator that provides a frequency reference for battery powered timekeeping applications is presented. An amplitude control circuit is employed to ensure that minimum current is consumed. A subthreshold voltage regulator provides a supply voltage for the oscillator with minimum current consumption. The oscillator and regulator are designed in a standard $0.18\mu m$ CMOS process. Measured results show the regulator works for battery voltages that range from 1.4 - 4.5V. The crystal oscillator consumes a current of 17.6nA at a minimum supply voltage of 0.8V, making it the lowest power crystal oscillator demonstrated to date. The complete system (oscillator and regulator) consumes a current of 30.6nA when a supply voltage of 3.3V is used.

An Ultra Low Power Frequency Reference For Timekeeping Applications

by

Hector Ivan Oporta

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Dean of the Graduate School

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Hector Ivan Oporta, Author

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Academic

I would like to begin by thanking all of the graduate students in KEC3040 for creating a comfortable and enjoyable work environment. I want to express my appreciation to James Ayers, Thomas Brown, and Napong Panitantum for all of their useful input during the course of this work. Their knowledge in analog circuit design and in using Cadence was a huge asset to have in the lab. I would like to thank all three of them for the helpful conversations we had and for the technical feedback they were able to provide during my time at Oregon State University. I would also like to show great appreciation to both of my major professors Terri Fiez and Kartikeya Mayaram for giving me the opportunity to do this work and for their help along the way. This work was supported by the National Science Foundation (NSF) whose funding made all of this possible.

Personal

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AN ULTRA LOW POWER FREQUENCY REFERENCE FOR TIMEKEEPING APPLICATIONS

1 INTRODUCTION

This paper presents an ultra low power time reference to address the need for timekeeping in small battery operated systems. The reference has applications in a new area of research related to tracking migratory animals [1]. Many birds, for example, leave their north temperate breeding range as winter approaches and travel to temperate habitats in the southern hemisphere as spring arrives there. The current inability to track individual birds throughout their annual cycle leads to a complete lack of knowledge regarding where specific individuals breed and winter. Small migratory animals can be tracked by using a miniature micropower cell phone. One important requirement is the size of the unit, it needs to be small enough for attachment to migratory birds (2 grams or less, the weight of a penny) captured in their tropical wintering grounds. This weight restriction requires that a tiny battery be used to power the system, such as a small coin cell lithium battery. After the bird migrates from the tropics to its breeding grounds in North America, the cell phone will activate and make contact with a local tower to initiate the registration process. To conserve power, a timer in the unit will keep it dormant until a preprogrammed date arrives. This timer must consume minimal current so that the battery is not depleted during the months that no transmission is required.

All timekeeping integrated circuits consist of an oscillator and a frequency divider. The oscillator is the time base for the system and high stability is required so that good accuracy and precision are achieved in the timekeeping device. A quartz crystal is usually used. This is a piezoelectric material that begins to vibrate when an electric potential is applied to it and is widely used in oscillators to generate a precision frequency reference for a variety of integrated circuits. Precision has to do with frequency stability of the time device independent of environmental conditions, such as temperature. Accuracy has to do with having the frequency set to the proper value. In a quartz crystal, precision is intrinsic to the technology of the tuning fork crystal [7], and accuracy is set by the oscillator circuit. The quality factor, Q, of commercially available crystals range from several thousand to several hundred thousand. Given the high Q and the fact that the frequency dependence with respect to time and temperature is very stable makes the quartz crystal the solution of choice for timekeeping applications.

The application considered in this paper requires keeping time with an unusually low current consumption. When timekeeping is needed with such demanding power constraints, a great deal of effort is needed to improve the oscillator block, since it accounts for the largest part of the timers current consumption. Prior work in crystal oscillators has operated with tens of nanoamps, in applications where current consumption is of prime interest [4]. Crystal oscillators optimized for both minimum current and voltage have also been considered, to minimize power [5]. Presented in this paper is an ultra low power crystal oscillator which constitutes the time base of a timekeeping system. New circuit techniques are implemented so that minimum power consumption is achieved.

The oscillator cannot rely on the battery as its supply, since small coin cell lithium batteries are manufactured to provide high voltages of 3V or above. A low power DC-DC converter is designed to take the battery as its input and provide the oscillator with a low supply voltage. The benefit of this is lower current consumption for a wider range of battery voltages (the range is 1.4V to 4.5V for this system). The oscillator supply is typically shared with the frequency divider that follows it. This allows a high battery voltage to be used with this system, while still maintaining a low supply voltage for the digital circuitry. As a result, power is saved, since current consumption increases significantly with supply voltage in the frequency divider.

The paper is organized as follows. Section 2 shows a detailed analysis and design of the low power crystal oscillator while Section 3 describes the design of the DC-DC converter. In Section 4 experimental results are presented and compared with previous publications on low power crystal oscillators. Section 5 provides a summary of the key

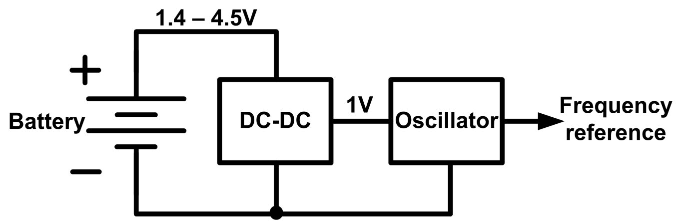

FIGURE 1.1: Block diagram for ultra low power time base.

points and concludes the paper.

2 LOW POWER CRYSTAL OSCILLATOR

The oscillator must generate a logic signal that can be used as a frequency reference for timekeeping. In a timekeeping system, a counter counts the pulses of the logic signal generated by the oscillator. For this application, the timekeeping device is expected to run on a small battery for a long period of time (a few months or more) with very little current consumption. Therefore, three conditions need to met. First, ultra low power consumption in the oscillator is critical. Second, a stable frequency with respect to time and temperature is required in order to keep accurate time. Finally, a low frequency is necessary in order to limit the power needed for the frequency division that precedes the counter.

The proposed system is shown in Fig. 1.1. It is comprised of a DC-DC converter and an oscillator. The oscillator uses a crystal and provides the time base necessary for timekeeping. The DC-DC converter can take any battery in the range of 1.4 - 4.5V as an input, and provides 1V to the oscillator. All circuits have been designed and optimized for the lowest possible current consumption due to the rigorous power requirements imposed by the application.

An effective method used in this design for conserving power, is the inclusion of a buffer in the amplitude control loop. This isolates the oscillator core from the rest of the circuit and minimizes current consumption. Also, a new configuration is used in the current mirror of the loop, that allows the oscillator to operate at a lower supply voltage. The prototype shows the lowest power consumption of any crystal oscillator to date.

Using a crystal resonator allows very good frequency stability at low frequencies. The lower the frequency the better, but, lower frequency crystals are rather large and cannot be used in portable applications. The balance of low frequency and small size has made the 32.768kHz quartz resonator a standard in portable timekeeping applications.

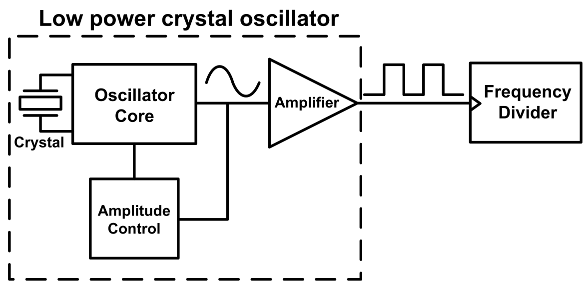

FIGURE 2.1: Low power crystal oscillator.

Low power consumption will dictate the choice of the oscillator topology that will be used. The circuit will operate with a standard 32.768kHz crystal. Figure 2.1 shows the block diagram for the ultra low power crystal oscillator. It consists of the oscillator core, an amplitude control block and an amplifier. The logic signal used as the frequency reference is shown in the figure as the input to the frequency divider. The amplitude control is the most important block for achieving a low current consumption. The amplitude control circuit will reduce the supply current when an acceptable amplitude is reached in the oscillator core. The amplitude of oscillation is minimized so that minimum power is consumed. As this amplitude is always much smaller than the supply voltage, an amplifier is necessary to interface to the frequency divider. This amplifier must also be designed for the lowest possible power consumption.

Next, a brief summary of crystal oscillator design and analysis is presented. This is followed by the detailed design procedure of the low power oscillator in Fig. 2.1.

2.1 Crystal resonator

Fig. 2.2 shows the electrical equivalent circuit of a crystal resonator at a given frequency. The oscillations are characterized by the crystal's mechanical resonant frequency given by:

$$\omega_m = \frac{1}{\sqrt{LC}} \tag{2.1}$$

and its quality factor:

$$Q = \frac{1}{\omega_m CR} \tag{2.2}$$

where L, C and R are the inductor, resistor and capacitor that make up the series branch in the equivalent circuit of the crystal resonator, Fig. 2.2. The crystal impedance with loading taken into account is given in [2] and is expressed as:

$$Z_m = R + \frac{j}{\omega_m C}(\frac{\omega}{\omega_m} - \frac{\omega_m}{\omega}) \tag{2.3}$$

where ω_m is the mechanical resonant frequency of the crystal resonator and is defined by Eq. (2.1). When the crystal resonator is loaded with a circuit to form an oscillator, the oscillation frequency ω will differ slightly from the mechanical resonant frequency. The real part of Z_m, R, represents the loss in the circuit that needs to be negated for oscillations to occur. The imaginary part of Z_m is affected by the loading, which pulls the frequency away from ω_m. The relative amount of frequency pulling p above the mechanical resonant frequency ω_m of the resonator is defined as:

$$p = \frac{\omega - \omega_m}{\omega_m} \tag{2.4}$$

Since $p \ll 1$, the impedance Z_m can be expressed as:

$$Z_m = R + j\frac{2p}{\omega C} \tag{2.5}$$

This gives a general expression for the impedance of a loaded crystal resonator. In an oscillator, p is a function of the capacitor values in the circuit (Section 2.2), which set the imaginary part of Z_m. To build oscillations, the circuit will need to provide a negative resistance that exceeds R in Eq. (2.5).

2.2 Three-point oscillator

A configuration that is commonly used for crystal resonators is the three-point oscillator shown in Fig. 2.3 [2]. This configuration, along with the crystal, consists of two capacitors and a MOS or bipolar device that provides a transconductance g_m. The negative resistance that is provided by this circuit (which is necessary for oscillation) depends on g_m.

The analysis begins by splitting the oscillator into two parts, as shown in the small-signal equivalent circuit of Fig. 2.4. The circuit is split into the impedance Z_m and the remaining circuit, which includes the shunt capacitance of the resonator, C_0.

For a small oscillation amplitude, we can approximate the circuit to be linear. The small-signal impedance Z_c as shown in Fig. 2.4 is found to be:

$$Z_c = \frac{Z_1 Z_0 + Z_2 Z_0 + g_m Z_1 Z_2 Z_0}{Z_1 + Z_2 + Z_0 + g_m Z_1 Z_2} \tag{2.6}$$

The critical condition for oscillation is given by:

$$Z_c + Z_m = 0 \tag{2.7}$$

where Z_m is given in Eq. (2.5). There is a MOS device transconductance value that satisfies the condition of Eq. (2.7). This is called the critical transconductance or g_{mcrit} and is obtained from:

$$-Re(Z_c) = R \tag{2.8}$$

where $Re(Z_c)$ is the real part of impedance Z_c. From Eq. (2.8):

$$g_{mcrit} = \frac{\omega}{QC} \cdot \frac{(C_1 C_2 + C_2 C_0 + C_0 C_1)^2}{C_1 C_2} \tag{2.9}$$

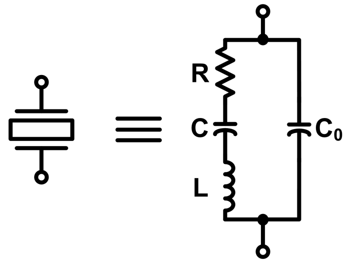

FIGURE 2.2: Equivalent circuit of a crystal resonator.

where C is the capacitance associated with the resonator and C_1, C_2 and C_0 make up the impedances shown in Fig. 2.4. When the critical transconductance is exceeded by applying a dc bias current to the active device above a critical value I_{crit}, oscillations build up. The amplitude of steady-state oscillation is determined by the large-signal transconductance G_m [3]. For the crystal oscillator, G_m is equal to g_{mcrit} [2, 3]. This means that reducing the critical transconductance reduces the minimum current necessary to both build up and sustain oscillations. The frequency pulling, p, is found from:

$$-Im(Z_c) = \frac{2p}{\omega C} \tag{2.10}$$

with $Im(Z_c)$ being the imaginary part of impedance Z_c. Solving for p from Eq. (2.10) gives:

$$p = \frac{C}{2(C_0 + \frac{C_1 C_2}{C_1 + C_2})} \tag{2.11}$$

Eq. (2.9) shows that g_{mcrit} can be reduced by reducing C_1, C_2 and C_0, but the trade-off is an increase in frequency pulling p. Ideally, both g_{mcrit} and p should be small for low power consumption and reduced frequency pulling.

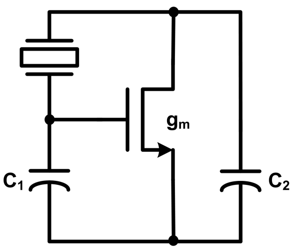

FIGURE 2.3: Three-point oscillator.

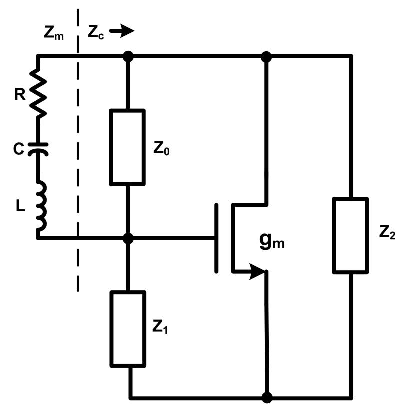

FIGURE 2.4: AC schematic of the three-point oscillator.

2.3 Circuit design

2.31 Oscillator core

The oscillator core, shown in Fig. 2.5, is implemented using both an NMOS and PMOS transistor as an inverter [2]. The analysis for this circuit is the same as the one presented for the three-point oscillator in Section 2.2. The advantage of this configuration is that from an ac perspective the two transistors are in parallel and their transconductances add. Capacitor C_3 is large enough (much larger than C_1 and C_2) so that the source of M2 is an ac ground. Since both transistors are biased with the same current, half the current is needed for the same transconductance when using only one active device. M1 and M2 are sized so that they operate in weak inversion. This region of operation provides the maximum value of transconductance for a given bias current [6]. In weak inversion g_m is given by:

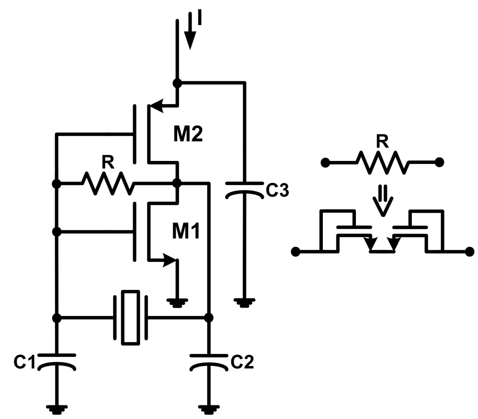

FIGURE 2.5: Oscillator core.

$$g_m = \frac{I_D}{nV_T} \tag{2.12}$$

where I_D is the transistor bias current, $V_T = \frac{kT}{q}$, and n is the slope factor.

The feedback resistor R is used for biasing and forces the gates and drains of M1 and M2 to have the same dc value. This resistance must be very high so it does not load the resonant circuit. Resistor R was implemented using two MOS transistors as shown in Fig. 2.5.

2.32 Amplitude control

Fig. 2.6 shows the schematic of the oscillator and the amplitude control loop that controls the current in the oscillator core. The loop is formed by transistors M1, M3, M6 and M7 operating in the weak inversion region. The loop gain is set to a value greater than one. As a result, the currents in both branches increase and are limited by the amount of current M3 and M7 are able to provide. The current in the oscillator core is high and, therefore, oscillations build up. The lowpass filter, labeled LPF in Fig. 2.6, filters out the ac component of the voltage at the gates of M1 and M2, V_G. The average of this voltage appears at the gate of M3. As the amplitude of V_G increases, its average value must decrease so that the average drain current of M1 and M2 remains constant. The drop in dc voltage at the gate of M3 reduces the current in the oscillator core to a value just necessary to sustain this amplitude of oscillation.

The current consumption that this oscillator is designed for is extremely low, therefore, a new structure is used for implementing the current mirror in the amplitude control loop. M6 and M7 make up a weak inversion current mirror that is self cascoded. The cascode devices, M5 and M8, are there so that M6 and M7 can operate in subthreshold with matched V_{DS} voltages for good current mirroring. These devices need to be large enough to ensure that the drain currents of M6 and M7 are saturated. There are two main reasons why a weak inversion current mirror is a better choice than operating these devices in strong inversion. First, the length of M6 and M7 can be made smaller at really low currents, and second, a lower minimum V_{dd} is achieved when they operate in subthreshold. This can be shown if M5 and M8 are ignored for the moment were it can be seen that the lowest value of V_{dd} that can be used safely is limited by the V_{DSAT} of transistor M7. In weak inversion if $V_{DS} > 3V_T$ ($\approx 78mV$ at room temperature) then I_D saturates, in strong inversion V_{DSAT} would be larger for this current mirror, which makes weak inversion the better alternative if a lower supply voltage is desired. The drain voltage of transistor M8 can reach a value very close to its source voltage (a few millivolts) without significantly affecting the matching of the current mirror. Simulation shows that V_{dd} can be as little as 80mV above V_{S2}, in Fig. 2.6, without any current mismatch between M6 and M7. V_{S2} is set by the sizes of the M1/M2 devices and the biasing current.

Transistor M4 is another addition not seen in other designs [4, 6], but is critical for the correct operation of this amplitude control loop. This device needs to be included if M6 is in weak inversion. M4 controls the drain voltage of M3, otherwise the drain of M3 would be pulled up close to the supply (by the gate voltage of M6) and the loop would not work. M4 needs to be sized large enough to ensure that the drain current of M3 is saturated.

The low-pass filter can be implemented in various ways. The new approach taken in this design is targeted at minimizing current consumption. Making sure the filter does

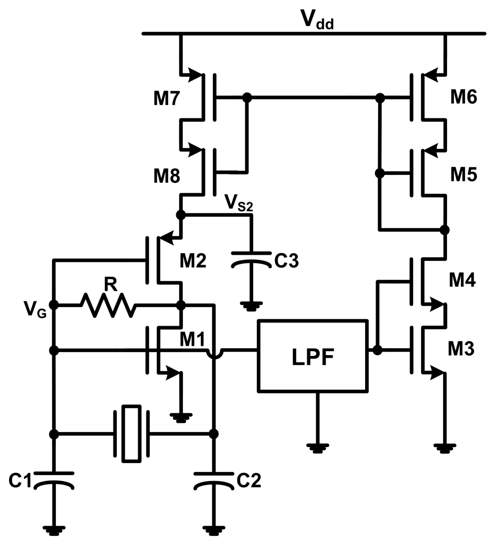

FIGURE 2.6: Oscillator with amplitude control.

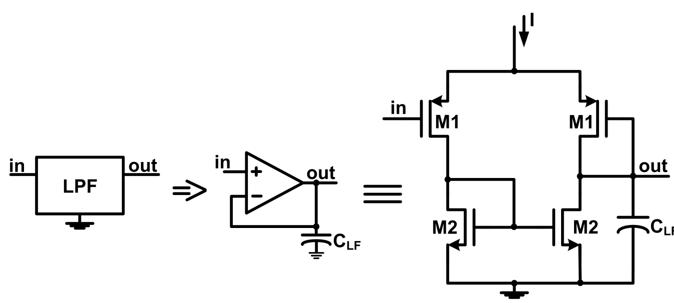

FIGURE 2.7: Low-pass filter for the amplitude control loop.

not load the oscillator is very important. If a simple R-C filter is used, the resistor must be very large to provide as much decoupling as possible from the oscillator. If loading occurs, more current is required for oscillation since more g_m is needed to compensate for the loading effect (see Appendix A for more details).

Figure 2.7 shows the circuit schematic of the low-pass filter. This is a simple differential amplifier with a current mirror load and its output is connected to the negative input thus achieving unity gain. The benefit of this approach is that the amplitude control loop and the oscillator are completely decoupled and no loading occurs. The input capacitance of the buffer is negligible since it is small compared to C_1 at the gate of M1. Since the dc component of V_G at the gate of M3 is needed, significant attenuation must occur at the oscillation frequency of 32.768kHz. Therefore, the amplifier bandwidth must be as low as possible whereby a very small current can be used to bias the buffer. A bias current value of 1 to 2nA is sufficient. In addition to using a very low current, the M1 pair in Fig. 2.7 can be sized to operate as close to strong inversion as possible, thus reducing the g_m of these devices even further. Finally, a large capacitor, C_{LF}, is placed at the output of the buffer to reduce the bandwidth to the desired value.

The oscillator is part of a larger system in which a low power on-chip current reference will have to be generated to bias the DC-DC converter. Therefore, the current needed to bias the amplifier will be available.

2.33 Amplifier stage

Since the amplitude of the oscillator is much smaller than the supply voltage, an amplifier stage is necessary to produce a logic signal. This stage should draw a minimal amount of current. In the steady state oscillating condition the drain currents in M1 and M2 in the oscillator core are strongly modulated and shifted by half a period (Fig. 2.8). The shape of the current waveforms shown in Fig. 2.8 are ideal for charging and discharging a capacitive circuit node. It has the best possible efficiency since there are never two transistors conducting at the same time. These currents can be useful in designing an amplifier stage optimized for low power consumption [5]. The currents are replicated with matched devices (M3 and M4) as shown in Fig. 2.9.

Currents I_1 and I_2 in Fig. 2.9 are set by the amplitude control loop. Current I_2 can be set to a fraction of I_1 because the current required in this stage is only the amount necessary to charge and discharge the small capacitance at the output node labeled V_D.

The logic signal V_D is limited by the dc voltage at the source of M3, which is held constant by capacitor C_4 (V_{S3} in Fig. 2.9). Since signal V_D is close to V_{dd} but is not quite rail to rail, a second stage is required to interface to the logic. This second and final stage is a simple inverter. Thick gate-oxide devices are used in this inverter to minimize power

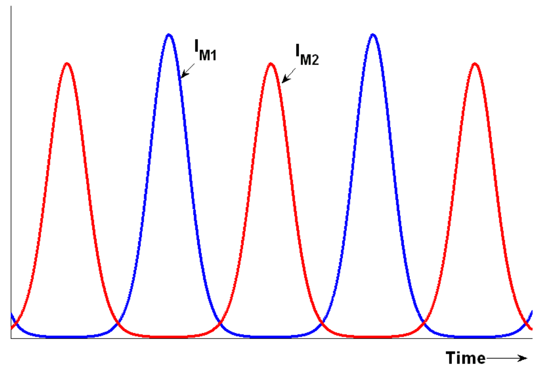

FIGURE 2.8: Currents vs. time for the two transistors in the oscillator core.

consumption due to the higher threshold voltages.

The complete oscillator with amplitude control is shown in Fig. 2.10. Table 2.1 shows a summary of the simulated currents for the complete circuit in steady state oscillation. The oscillator consumes a total current of 14nA. The amplitude control keeps the peak-to-peak voltage in the oscillator core (node V_G in Fig. 2.10) at a low value of 168mV, and the current consumption in the oscillator core is only 7nA. The simulated result for V_G is shown in Fig. 2.11. Also plotted in this figure is the output node of the buffer, V_{GDC}. It can be seen that the ac component of V_G has been filtered and the buffer outputs the average value of the signal. A current of 2nA is used in the buffer.

The 168mV peak-to-peak voltage at node V_G shown in Fig. 2.11 is amplified to a logic signal at the output of the oscillator. This is done by the amplifier stage in the oscillator with a total current consumption of 2nA. The simulation is shown in Fig. 2.12.

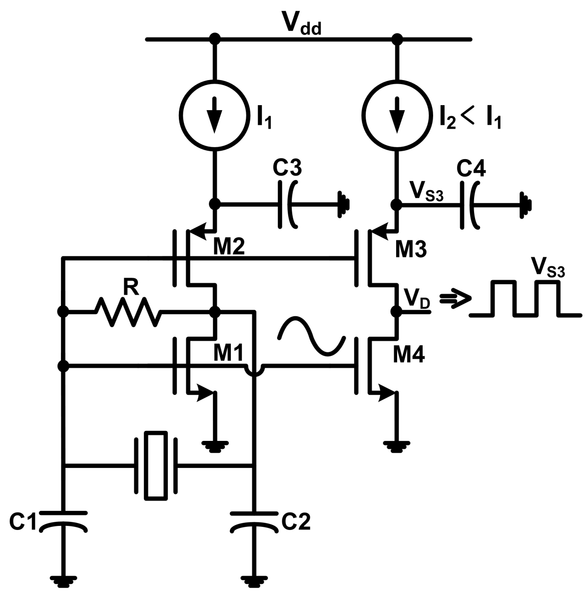

FIGURE 2.9: High efficiency voltage amplification.

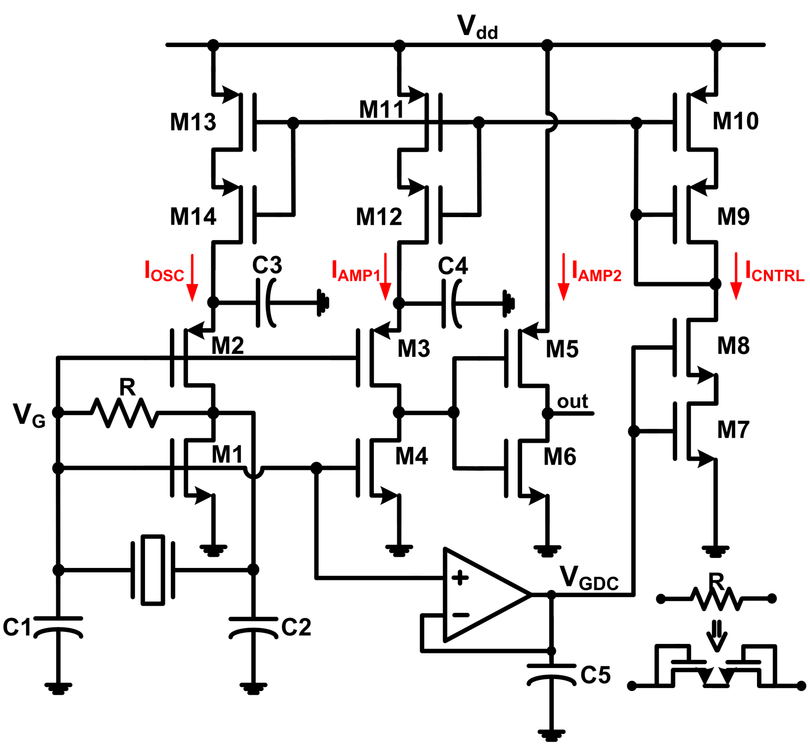

FIGURE 2.10: Complete schematic of oscillator including amplitude control and output amplifier.

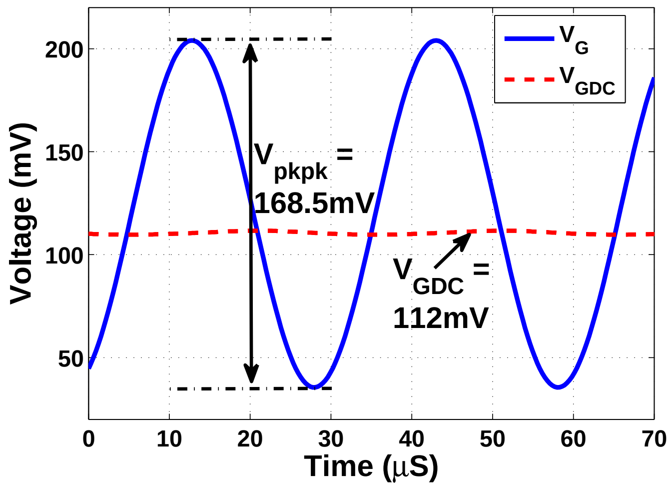

FIGURE 2.11: Simulated V_G and V_{GDC} for the low power oscillator (see Fig. 2.10 for notation).

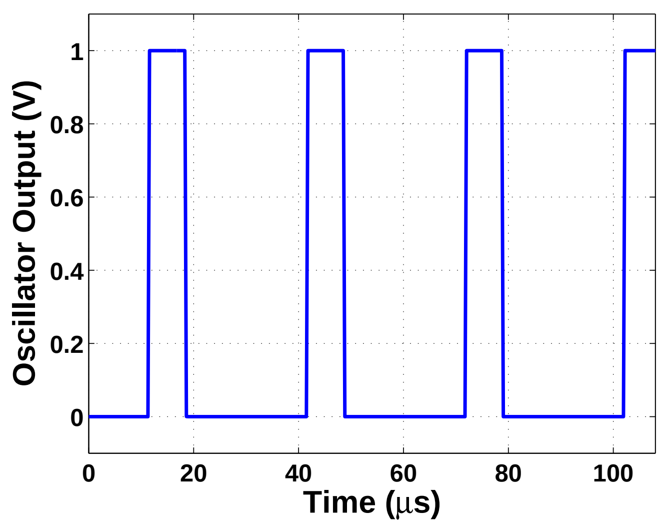

FIGURE 2.12: Simulated output of the low power oscillator (node 'out' in Fig. 2.10).

TABLE 2.1: Simulation results for the low power oscillator, $V_{dd} = 1$V. Currents are shown in Fig. 2.10.

I_{OSC}	7 nA
I_{AMP1}	1.7 nA
I_{AMP2}	300 pA
I_{CNTRL}	3 nA
$Buffer$	2 nA
I_{TOTAL}	14 nA

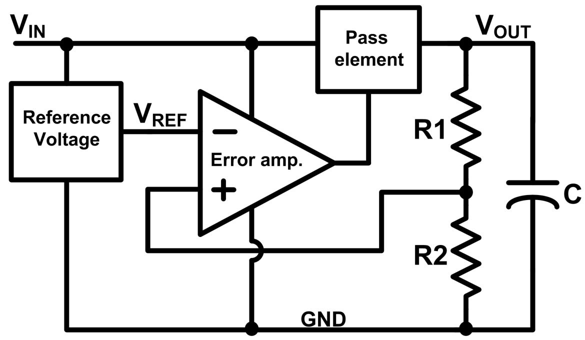

FIGURE 3.1: Linear voltage regulator.

3 SUBTHRESHOLD LINEAR REGULATOR

A linear voltage regulator down converts the battery voltage to a value of 1V. The output of this regulator is the supply voltage for the oscillator circuitry. Due to the stringent power requirements of the system, the current consumption of the regulator must be extremely low and it must be designed to operate in the subthreshold region.

Figure 3.1 shows the block diagram of a linear voltage regulator [8]. The basic blocks in any linear regulator are a reference voltage, an error amplifier, a pass element, resistor divider $R1$ and $R2$, and output capacitor C. The output voltage is given by:

$$V_{OUT} = V_{REF}\left(1 + \frac{R1}{R2}\right) \tag{3.1}$$

The error amplifier compares the sampled output voltage from the resistive divider with the reference voltage to control the current through the pass element. The current in the pass element is either increased or decreased depending on whether V_{OUT} is low or high.

The output capacitor C is a critical component and is needed to stabilize the regulator. Since the error amplifier is designed to operate in subthreshold and at a low current, the output voltage V_{OUT} must change slow enough for the amplifier output to respond. For this, the capacitor C must be sized accordingly.

3.1 Reference voltage

A proportional-to-absolute temperature (PTAT) current is needed to design the reference voltage for the regulator as well as bias the amplifier. Shown in Fig. 3.2 is the schematic of the PTAT current reference. Thick gate-oxide devices are used and cascoded so that no device exceeds the oxide break down voltage of 3.3V for the given process. Cascoding allows a battery voltage of up to 4.5V to be used.

When the devices are operated in weak inversion a small PTAT voltage develops at the source of transistor M2. This voltage is expressed as:

$$V_R = V_T ln(\frac{N2}{N1}) \tag{3.2}$$

where $V_T = \frac{kT}{q}$ and $\frac{N2}{N1}$ is the $\frac{W}{L}$ ratio of transistors M2 and M1. This voltage generates a PTAT current through resistor R, which is extracted by a current mirror as shown in Fig. 3.2 and used to bias the regulator. The value of this reference current is given by:

$$I_{PTAT} = \frac{V_T}{R} ln(\frac{N2}{N1}) \tag{3.3}$$

At $27°C$ an I_{PTAT} of approximately 5nA is generated by using $R = 1.87M\Omega$. Figure 3.3 is a simulation that shows the linearity of the reference current with temperature.

The threshold voltage of a PMOS transistor is complimentary to absolute temperature (CTAT). Consequently a PMOS device can be sized so that the temperature coefficient of the PTAT current and CTAT threshold cancel out [9]. This will give a constant reference voltage versus temperature. A schematic of this reference voltage, V_{REF}, is shown in Fig. 3.4. In addition to using long devices, multiple transistors are stacked on top of each other so that 0.5V can be generated with only 1nA of current.

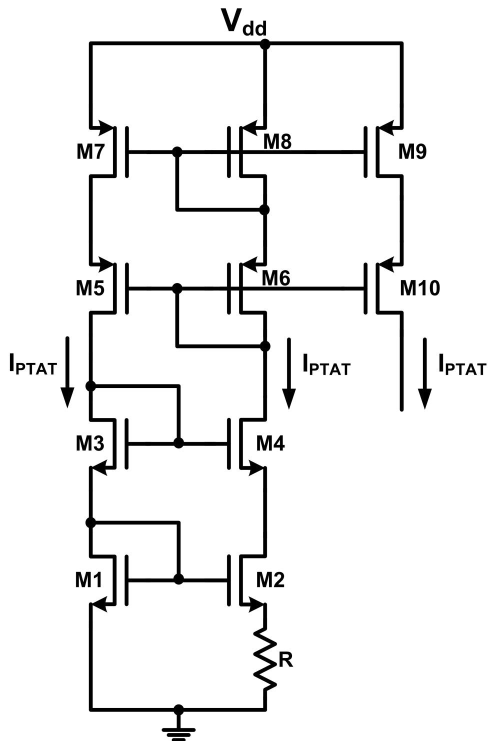

FIGURE 3.2: PTAT current reference where V_{dd} is the battery voltage.

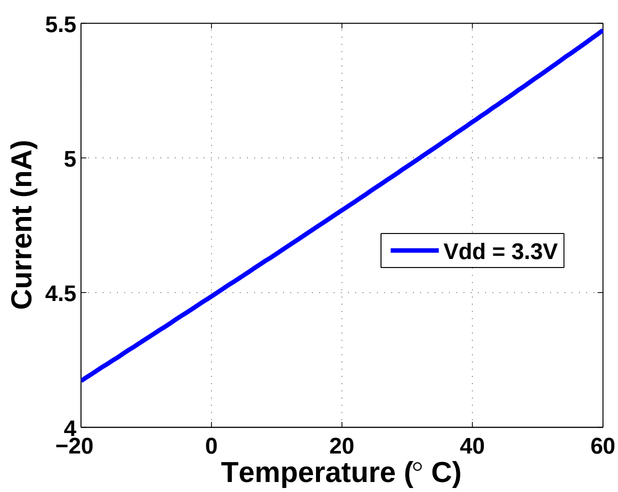

FIGURE 3.3: Simulated PTAT current vs temperature.

3.2 Subthreshold amplifier and voltage divider

The amplifier used in the regulator is a two-stage opamp with a cascoded output stage, shown in Fig. 3.5. The opamp is designed to operate in subthreshold, the currents

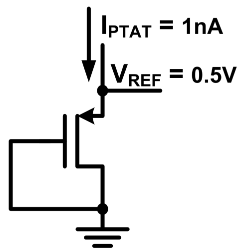

FIGURE 3.4: Temperature compensated reference voltage.

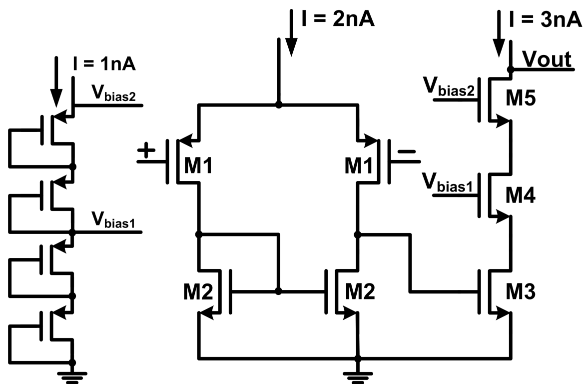

FIGURE 3.5: Schematic of two-stage opamp used in the regulator.

labeled in the figure are mirrored from the PTAT current reference described in Section 3.1.

From Eq. (3.1), if a regulator output voltage of 1V is desired then R1 = R2. This means that each resistor would have 0.5V across it. This voltage division is done by replicating the reference voltage shown in Fig. 3.4 at the output of the regulator. If two of these devices are placed in series, and each device generates a V_{REF} voltage, then the desired 1V will be provided at the output [9]. Fig. 3.6 shows how the output voltage is divided down using MOS devices. The output of this voltage divider connects to the input of the opamp, Fig. 3.1. The opamp compares this voltage to the reference voltage $V_{REF} = 0.5V$. Since the device used for V_{REF} and the device used for the voltage divider are matched (same W and L) the current consumption of this branch is 1nA when $V_{OUT} = 1V$, as shown in Fig. 3.6.

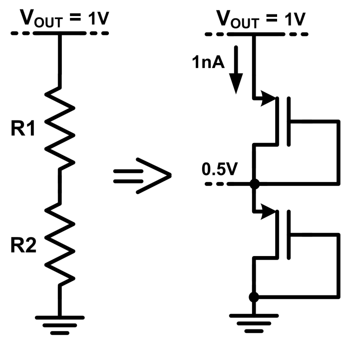

FIGURE 3.6: R1 and R2 implemented with MOS devices.

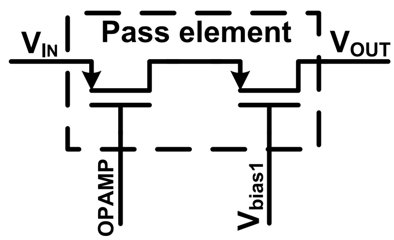

FIGURE 3.7: Pass element shown in Fig. 3.1 implemented with two PMOS devices.

3.3 Pass element

The pass element shown in Fig. 3.1 is implemented with two PMOS transistors connected in series, Fig. 3.7. This reduces the voltage drop across each transistor so that breakdown does not occur. The gate of the first transistor is connected to the amplifier output. The first device controls the current delivered to the output capacitor and the load. The second transistor in the series connection has its gate biased at a dc voltage that is generated using the PTAT current. This is the same voltage used for biasing the opamp (V_{bias1} in Fig. 3.5).

Simulations show that the opamp, reference voltage, and voltage divider in the regulator consume a current of 8nA. The current consumption for the PTAT circuit shown in Fig. 3.2 is 10nA, 5nA for the left and right branches, respectively.

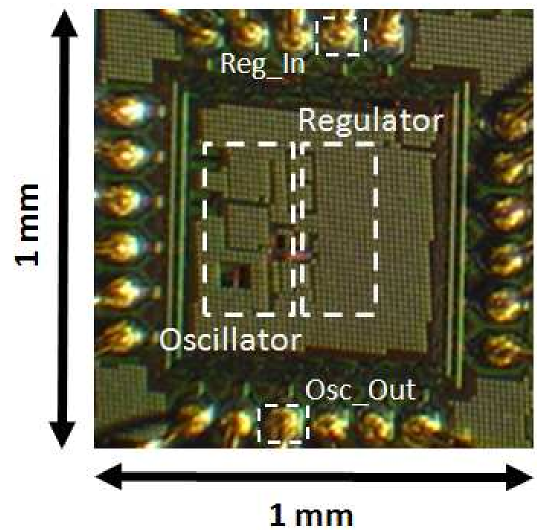

FIGURE 4.1: Chip microphotograph.

4 EXPERIMENTAL RESULTS

The proposed ultra low power time base has been fabricated in a standard $0.18\mu m$ CMOS process. Figure 4.1 shows the microphotograph of the fabricated circuit. All external pins are fully ESD protected. The chip was bonded in a MLF48 package, a standard leadless QFP type package. A standard FR4 circuit board was used for lab testing.

4.1 Low power oscillator

Table 4.1 provides a summary of the measured results for the complete low power oscillator of Fig. 2.10, with $C_1 = C_2 = 6pF$. Fig. 4.2 shows the measured output of the oscillator with $V_{dd} = 1V$. The current consumption of the complete oscillator (including the buffer), I_{SUPPLY}, in Table 4.1 was measured at V_{dd} of 1V and 0.8V, respectively. The oscillator has the lowest measured current and power consumption of any crystal

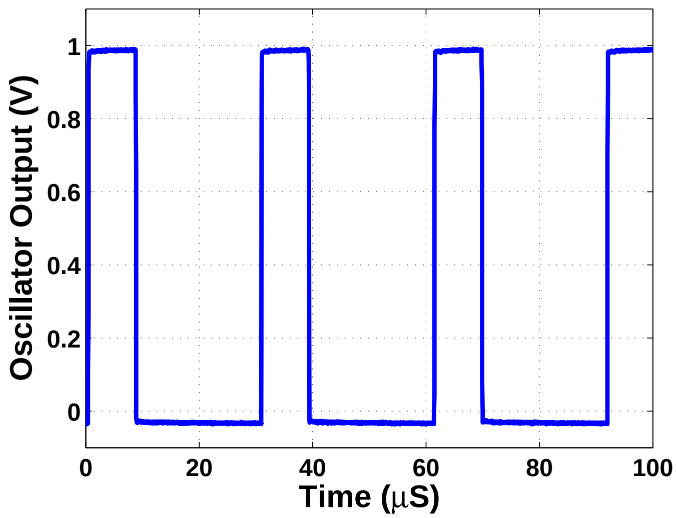

FIGURE 4.2: Measured output of the low power oscillator (node 'out' in Fig. 2.10).

TABLE 4.1: Measured results for low power oscillator.

Parameter	**Measured Value**
$Frequency$	32.7694 kHz
$I_{SUPPLY}(V_{dd} = 1V)$	19.35 nA
$I_{SUPPLY}(V_{dd} = 0.8V)$	17.6 nA
$Min.\ V_{dd}$	0.8 V

oscillator reported to date. Table 4.2 shows the prototype oscillator compared to the best performing crystal oscillators.

The frequency stability of the oscillator is set by the tuning fork crystal. This was calculated by measuring the rms jitter of the oscillator. The measured rms jitter is 630 ps which translates to approximately 20ppm. This is in agreement with the frequency stability specified in the datasheet of the tuning fork crystal.

TABLE 4.2: Performance comparison of the lowest power crystal oscillators to date.

	This Work	[5]	[4]
Technology	0.18μm CMOS	2μm CMOS	0.8μm CMOS
I_{SUPPLY} (nA)	17.6	39	30
$Min.\ V_{dd}$ (V)	0.8	0.67	1.5
Power Consumption (nW)	14.08	26.13	45

4.2 Regulator and PTAT current reference

The PTAT current reference at room temperature generates 2.8nA at $V_{dd} = 3.3V$. Fig. 4.3 shows the measured PTAT current versus V_{dd}. The design works for a supply voltage as low as 1.4V, below which the current begins to decay rapidly. The current reference will work up to a supply of 4.5V without any device exceeding the oxide breakdown voltage of 3.3V for the given process.

The regulator provides a regulated voltage of 0.9V. The measured output voltage versus input voltage for the regulator is shown in Fig. 4.4. The linear regulator will begin to regulate at an input voltage of 1.4V. For this input voltage the output is approximately 0.9V.

The input voltage of the regulator is the V_{dd} for the PTAT current reference. This circuit provides the biasing for the regulator. The minimum input voltage for the regulator is limited by the minimum V_{dd} required by the PTAT current circuit. Once the PTAT current begins to work at a V_{dd} of 1.4V, so does the regulator. This makes the system function for battery voltages that range from 1.4V to 4.5V.

When unloaded the regulator output is 0.9V. Fig. 4.5 shows the output voltage of the regulator versus load current. It can be seen from the graph that the output voltage

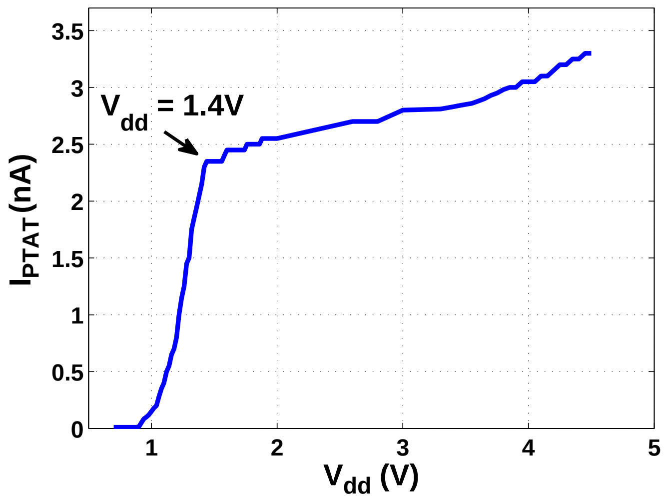

FIGURE 4.3: Measured PTAT current vs. supply voltage.

stays constant up to a load current as high as 80 μA. When the output current is increased to 415 μA the output voltage drops to approximately 0.83V. This regulator was designed for a very light current load (the oscillator only consumes 17.6nA). Therefore, for low power applications such as this one, there will be no variation in the regulator output voltage.

The current consumption of the complete system (this includes all circuits: PTAT current reference, regulator and oscillator) was measured with input voltages of 1.4V, 3.3V and 4.5V. The measured results are shown in Table 4.3. A small variation in the current consumption is seen when the input voltage is varied from its minimum to its maximum value, 1.4V to 4.5V respectively. The system generates a 0-0.9V clock signal at a frequency of 32.7694 kHz.

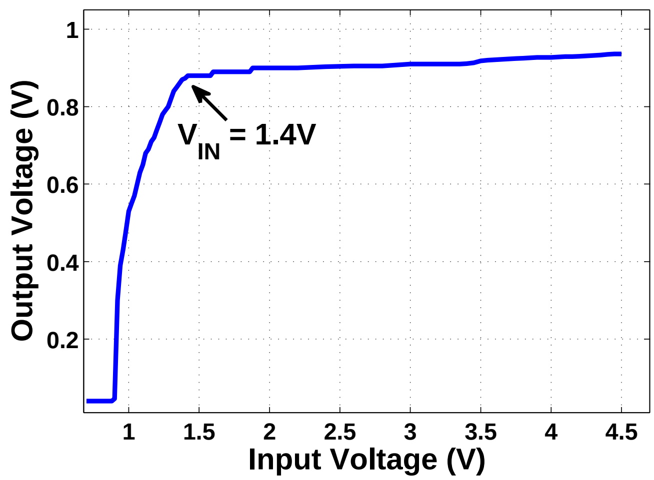

FIGURE 4.4: Measurement results for regulator output voltage vs. input voltage.

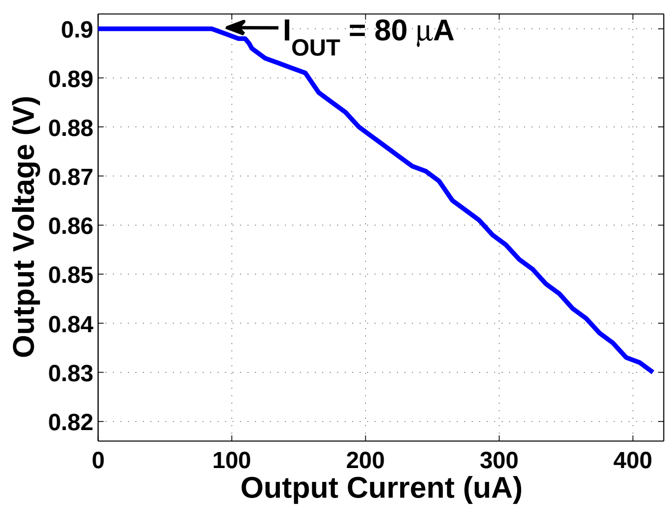

FIGURE 4.5: Measurement results for regulator output voltage vs. output current.

TABLE 4.3: Current consumption of the complete system.

Input Voltage	**Measured Current (nA)**
$1.4V$	28.25
$3.3V$	30.6
$4.5V$	31.85

5 CONCLUSION

A low power time base has been implemented to meet the requirements of a portable timekeeping device that operates from a small battery. The crystal oscillator utilizes circuit techniques for ultra low current consumption. The DC-DC converter is implemented by a subthreshold linear regulator that operates at extremely low power levels. The system has been implemented in a standard $0.18\mu m$ CMOS process. Measured results show that the system consumes a current of only 30.6nA when a supply voltage of 3.3V is used.

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APPENDIX

A LPF loading on oscillator core

The following shows the effect of loading on a crystal oscillator core. If an R-C filter is used as shown in Fig. A.1 it loads the oscillator and a larger g_m is required to compensate for this. For a simplified analysis, the shunt capacitance of the resonator, C_0, is neglected. This capacitance can be considered as an additional load. Neglecting C_0 implies that Z_0 in Fig. 2.4 is infinite. The real part of impedance Z_c then becomes:

$$Re(Z_c) = \frac{-g_m}{\omega^2 C_1 C_2} \tag{A.1}$$

To sustain oscillations $-Re(Z_c)$ must be equal to resistance R shown in Eq. (2.5). With an R-C filter the three-point oscillator schematic can be redrawn as shown in Fig. A.2. This is a modified version of the schematic shown in Fig. 2.3, the impedance of the R-C filter formed by R_x and C_x will be in parallel with capacitor C_1 of the oscillator. The real part of Z_c in Eq. (A.1) is modified and is now given by:

$$Re(Z_c) = \frac{-g_m\left(\frac{1}{\omega^2 C_1 C_2} + \frac{(R_x C_x)^2}{C_2(C_1+C_x)}\right)}{\frac{C_1+C_x}{C_1} + \frac{\omega^2 C_1 (R_x C_x)^2}{C_1+C_x}} \tag{A.2}$$

As $R_x \rightarrow \infty$ and/or $C_x \rightarrow 0$, $Re(Z_c)$ in Eq. (A.2) approaches the value in Eq. (A.1). Any smaller value of R_x or larger value of C_x decreases $Re(Z_c)$. As a result, more g_m is necessary to satisfy the condition for oscillation given by Eq. (2.7).

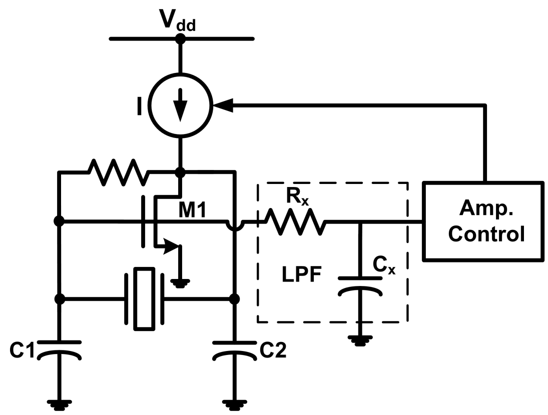

FIGURE A.1: Oscillator with an R-C low-pass filter.

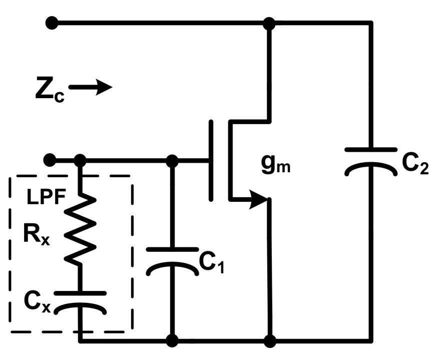

FIGURE A.2: Loading effect of R-C filter on oscillator.