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Patrick Yin Chiang Arun S. Natarajan

The release of the IEEE802.15.6 standard has led to increased interest in low-power technologies for wireless body-area-networks (WBANs). The power dissipation, supply voltage, and die area are some of the most important criteria for successful WBAN implementations. Digital-intensive RX architectures can potentially result in sub-1V operation with significant reductions in power consumption and area, but require system and circuit-level innovations to achieve desired sensitivity and linearity. A PSK receiver (RX) is proposed that employs a digital-intensive architecture based on sub-sampling, Q-enhancement, and digital IF to enable low-power (1.3mW) and low-voltage (0.6V) operation. Implemented in 65nm CMOS, this work is compatible with the IEEE 802.15.6 narrowband physical layer specification and achieves -91dBm and -96dBm sensitivity at 10^{-3} BER for π/4-DQPSK and π/2-DBPSK modulation, respectively. The proposed highly-digital

architecture and supply voltage scaling lead to a 3x improvement in RX energy efficiency and minimize silicon area consumption (~0.35mm^2 in 65nm CMOS) while achieving state-of-the-art sensitivity. While this implementation focuses on IEEE 802.15.6 narrowband demodulation, the proposed architecture and circuit techniques are generally applicable to RX targeting ultra-low power consumption for sensor networks.

Analysis and Design on Low-Power Short-Range Radios for Wireless Body Area Networks

by

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I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

Jiao Cheng, Author

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TABLE OF CONTENTS

Page

Chapter 1. Introduction 1

1.1 Trends in Medical and Healthcare Applications 1
1.2 Features of Wireless Body Area Networks 4
1.3 Motivation...7
1.4 Dissertation Organization 9

Chapter 2. Background...11

2.1 Overview of Short Range Wireless Standards 11
2.2 State-of-the-Art Low Power Receivers 15
2.2.1 Super-Regenerative Receivers...15
2.2.2 Current-Reuse Receivers 18
2.2.3 Zero-IF Receivers...19
2.2.4 Sliding-IF Receivers...21
2.2.5 Transformer-Coupled Low-Voltage Receivers 22
2.3 Performance Summary and Comparison 24

Chapter 3. A 2.4GHz Low-Power Low-Voltage Sub-Sampling Receiver 26

3.1 Introduction...26
3.2 System Level Analysis...27
3.2.1 Low Noise Figure Operation in Sub-Sampling 28
3.2.2 Front-End Frequency Tunability 33
3.2.3 Frequency Plan 35
3.2.4 Oversampling A-to-D Conversion 37
3.3 Circuit Implementation 39
3.3.1 Receiver Topology 39
3.3.2 Q-Enhancement LNA..40
3.3.3 Sample-and-Hold Stage...48
3.3.4 1-bit Quantizer...50
3.3.5 Local Oscillation 52
3.3.6 Clock Generation...53

TABLE OF CONTENTS (Continued)

Page

3.3.7 Digital Intermediate Frequency (IF) Stage 54
3.3.8 Digital Baseband 55
3.4 Experimental Results 60
3.4.1 Q-Enhancement LNA 61
3.4.2 1-bit Quantizer 63
3.4.3 Sub-Harmonically Injection-Locked Ring Oscillator 65
3.4.4 Sensitivity 66
3.4.5 Linearity 68
3.4.6 Power Breakdown and Comparison 70
3.4.7 2.7GHz Operation 71
3.5 Summary and Comparison 72

Chapter 4. Conclusion 75

Bibliography 77

LIST OF FIGURES

Figure Page

Figure 1.1: Biomedical and healthcare applications around human body 2

Figure 2.1: (a) SRR system block diagram (b) SRO principle 16

Figure 2.2: Schematic of LNA, mixer and VCO (LMV) stacking front-end...........19

Figure 2.3: System block diagram of the zero-IF (direct-conversion) receiver.......20

Figure 2.4: System block diagram of the sliding-IF receiver 22

Figure 2.5: Schematic of transformer-coupled low-voltage LNA 23

Figure 3.1: Noise folding in sub-sampling (a) without and (b) with preceding high-Q filtering...29

Figure 3.2: Block diagram of the cascaded filtering and sub-sampling stages........30

Figure 3.3: Cascaded noise figure vs. sub-sampling frequency for different filter Q 32

Figure 3.4: Gain reduction and fluctuation in high-Q RF front-end........................33

Figure 3.5: (a) Gain reduction and (b) gain variation versus Q for different frequency tuning LSB 34

Figure 3.6: Frequency plan of the proposed sub-sampling receiver........................35

Figure 3.7: Relative signal and noise power level when measuring ACR...............37

Figure 3.8: System block diagram of the proposed sub-sampling receiver.............39

Figure 3.9: Schematic of the Q-enhancement LNA..41

Figure 3.10: Schematic of the coarse tuning capacitor bank 42

Figure 3.11: LNA output resonance and equivalent Q calibration steps 43

LIST OF FIGURES (Continued)

Figure Page

Figure 3.12: (a) small signal circuit of the single-end positive feedback loop; differential impedance of the positive feedback loop in (b) series and (c) parallel .45

Figure 3.13: Small-signal circuit of the input matching network and transistor......47

Figure 3.14: Schematic of the 1-bit A-to-D converter 50

Figure 3.15: Monte Carlo simulation of the quantizer input DC offset 51

Figure 3.16: Schematic of the ring oscillator. 53

Figure 3.17: Schematic and timing diagram of the clock generation circuit 54

Figure 3.18: Block diagram of the modified CIC filter 55

Figure 3.19: Block diagram of the linear-phase-response FIR 56

Figure 3.20: Frequency response of the 33rd-order FIR filter 57

Figure 3.21: π/4-DQPSK constellation 58

Figure 3.22: Block diagram of the symbol timing recovery circuit.........................59

Figure 3.23: Die photo 60

Figure 3.24: Measurement of LNA output resonance tuning with (a) coarse code and (b) find code 61

Figure 3.25: Comparison between measurement and calculation of enhanced Q and LNA bias current...62

Figure 3.26: Measurement of LNA input matching..63

Figure 3.27: 1-bit quantizer measurement setup with (a) external voltage sources and (b) internal control words..64

Figure 3.28: Measured quantizer output accumalative Gaussian distribution curve versus (a) external input and (b) internal control word...65

LIST OF FIGURES (Continued)

Figure Page

Figure 3.29: Phase noise of the ring oscillator (a) without and (b) with injection locking..........65

Figure 3.30: Spectrum of the injection-locked ring oscillator 66

Figure 3.31: BER measurement set up..........67

Figure 3.32: Measuremnt of sensitivity versus enhanced Q in LNA..........67

Figure 3.33: Measurement of compression point versus enhanced Q in LNA..........68

Figure 3.34: ACR measurement set up 69

Figure 3.35: Measurement of ACR for (a) π/4-DQPSK and (b) π/2-DBPSK 69

Figure 3.36: Power breakdown and comparison with prior art..........70

Figure 3.37: 2.7GHz operation performance summary 71

Figure 3.38: FOM comparison with prior arts 74

LIST OF TABLES

Table Page

Table 1.1: Data Rates of Ordinary Biomedical Applications 5

Table 1.2: The Average Path Loss (dB) Around Human Body at 2.36GHz..............6

Table 2.1: Physical Layer Specification Comparison in Typical Mode 13

Table 2.2: Performance Summary and Comparison of Prior Low-Power Receivers 24

Table 3.1: Numeric Example of the Equivalent Q vs. Bias Current........................47

Table 3.2: Coefficients in the 33rd-order FIR Filter...57

Table 3.3: Performance Summary and Comparison with Prior Arts 73

Analysis and Design on Low-Power Short-Range Radios for Wireless Body Area Networks

Chapter 1. Introduction

1.1 Trends in Medical and Healthcare Applications

The annual healthcare expenditure in U.S. has increased from $3 trillion in 2012 to $3.65 trillion in 2013 [1], and is expected to maintain an average growth rate of 6% in the projected cost trend for 10 years [2], within which the annual total healthcare expenditure is projected to reach almost 20% of the Gross Domestic Product (GDP) [3]. In the mean time, the average life expectancy was reported as 71.0 years worldwide and 79.8 years in U.S. in the year of 2013 [4]. According to the U.S. Bureau of the Census, the population of elderly people over age 65 has increased from 35 million in 2001 to 45 million in 2013 and is expected to reach 65 million in 2025, which is almost doubled in 25 years [5]. Statistics listed above strongly suggest the needs of more convenient and more affordable biomedical and healthcare solutions with more advanced features.

The evolution of semiconductor technologies benefits higher level integration and miniaturization of biomedical sensors and actuators, resulting in ubiquitous, low-power and low-cost applications in biomedical and healthcare systems, such as

EXG, activity tracker, hearing aids and endoscopy shown in Figure 1.1. These wearable and implantable devices are keys to facilitate satisfying the increasing demanding for medical and healthcare services with acceptable cost and powerful functionalities, and they normally do not impact the level of comfort very much as the mobility of the subject is not limited.

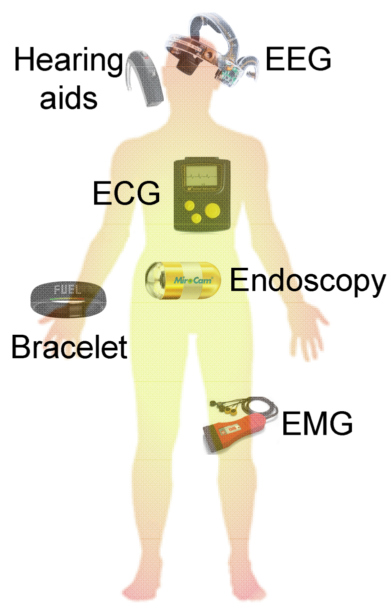


Figure 1.1: Biomedical and healthcare applications around human body

However, traditional portable solutions without wireless data links still prevent themselves from wider acceptance, especially when real-time monitoring and high-data-volume recording are required. For example, the classic ambulatory electrocardiography (ECG) device, Holter monitors, can only collect data when they are engaged. For further processing and analysis, the data have to be downloaded offline [3], which makes such devices inconvenient for long-term uninterrupted monitoring. Moreover, online data streaming with wired connections is not a practical option either because it ultimately limits the patient’s activity and level of comfort. Another example to reinforce this argument is the traditional fiber-optic gastroscope which requires a cable to be inserted through the subject’s throat and all the way to the stomach, causing a lot of pain and discomfort [6].

Thus, reliable wireless data links with sufficient communication bandwidth have to be introduced to provide connections between wearable and implantable devices and personal equipments which have faster processors and larger storage, such as smart phones and tablet computers, therefore enable real-time bio-signal monitoring and analysis without significantly increasing the power and cost budget on the wearable and implantable devices end. Through the internet connection provided by the personal mobile platform, even more powerful computing engines (e.g., cloud) can be involved to perform more comprehensive pattern analysis on collected bio-data, facilitating prevention and early detection of disease.

1.2 Features of Wireless Body Area Networks

Since the optimal place to monitor a variety of vital signs, inject drugs and therapeutic signals can be different and all over the human body (Figure 1.1), a wireless network should be introduced to provide convenient communication links between sensors, actuators and processing elements at different locations on and/or around the human body. Such a network is so-called Wireless Body Area Network (WBAN).

Based on the characteristics of wearable and implantable biomedical and healthcare applications, the physical implementation of WBANs should feature two major specifications. First, the data link bandwidth (i.e., the information rate) should be sufficient. For example, typical electrocardiography (ECG) usually requires 8-to-11bit resolution for the analog-to-digital conversion (ADC) with the sampling frequency ranging from 64Hz to 1kHz or so [7]-[9], yielding an equivalent maximum data rate of 11kbps. On the other hand, with similar requirements of ADC resolutions, typical electroencephalography (EEG) features higher sampling rate since it measures the voltage fluctuations resulting from ionic current flows within the neurons of the brain, which usually have much higher signal bandwidth than that of the heart. With 10-to-11bit ADC and 4-to-32kHz sampling rate [10]-[12], EEG generally reaches a maximum data rate around 350kbps. Moreover, wireless endoscopy is also a major medical application which requires high data rate to ensure the image quality for pathological diagnosis. The state-of-the-art image compression algorithm introduces a compression ratio from 1.96bits/pixel to 3.75bits/pixel for different image qualities [13]. With a typical resolution of 256×256 pixels and a frame rate of 4fps, the final data rate requirement ranges from 500kbps to 980kbps. In addition, hearing aid and audio services generally require data rates of 200kbps and 1Mbps, respectively [14][15]. The data rate requirement discussed above is summarized in Table 1.1.

Table 1.1: Data Rates of Ordinary Biomedical Applications

Applications	Data Rate (kbps)
ECG	0.5 - 11
EEG	40 - 350
Endoscopy	500 - 980
Hearing aid	200
Audio	1000

In general, WBAN implementations are supposed to target an effective data rate around 1Mbps to cover most of the medical and healthcare applications.

Second, the link budget of WBANs should also be maintained high enough to accommodate the non-line-of-sight (NLOS) nature of the network. The large variation of the measured path-loss exponents from below three [16] to above six [17] shows that the distance-based path-loss model ignoring transceiver placement and movement, which is widely used in line-of-sight (LOS) communications, is not appropriate for the body area networks. Instead, scenario-specific measurements of the path loss should be considered as the practical criterion for link budget estimation.

Table 1.2: The Average Path Loss (dB) Around Human Body at 2.36GHz

Action	Receiver at Right Hip; Transmitter at:					Receiver at Chest; Transmitter at:		
	Chest	Right Wrist	Left Wrist	Right Ankle	Left Ankle	Back	Right Wrist	Right Ankle
Standing	65.3	44.5	74.7	60.9	70.7	73.0	70.5	66.3
Walking	59.1	47.3	59.8	53.9	58.5	72.0	64.9	62.4
Running	55.9	36.3	52.5	55.0	59.0	71.7	57.4	63.3

Table 1.2 lists the 2.36GHz narrow band average path loss with the transceiver pair placed at different locations on the human body and three typical human actions [18]. As can be seen in Table 1.2, due to the absorption and reflection of the human tissue, the average path loss of shorter distance (from back to chest when

one is standing, 73dB) can actually be larger than that of longer distance (from right ankle to chest when one is standing, 66.3dB). Even for the same location of the transceiver pair, the average path loss is varying when the human action changes and the variation can be more than 20dB (from left wrist to right hip). In a word, the wireless link budget in WBAN is supposed to accommodate the actual NLOS path loss based on different application scenario, but not simply set by the short communication distance of the network.

1.3 Motivation

With the accomplishing of the technical specification discussed in the previous section to satisfy fundamental requirements of biomedical and healthcare services, the practical implementation of WBANs should further be evaluated in the following aspects.

(1) Power and peak current consumption: Wearable and implantable devices in biomedical applications are expected to be powered by button batteries for the sake of convenience. To avoid frequent replacement of batteries for a large amount of sensor nodes, the power consumption of the wireless transceivers should be minimized. Besides, the peak current consumption of the radio is sometimes specifically evaluated due to the finite power handling capacity of the button battery. For example, when a CR2032 button battery is discharged with continuous

current of 3mA, the total capacity it can deliver before its output voltage drops too low is only about 50% of that when the continuous discharging current is 500uA [19]. Thus, minimizing the peak current consumption of the radio is also very important to improve the battery's life time, especially when the application is real-time monitoring with the radio always on, such as wireless endoscopy.

(2) Supply voltage: Despite the low power consumption potential due to low supply voltage operation, the CMOS technology scaling trend is pushing the supply voltage lower and lower. According to International Technology Roadmap for Semiconductors (ITRS) 2013 Overall Roadmap Technology Characteristics (ORTC) Table, the supply voltage even for high voltage transistor will be only 0.8V in 2017. Therefore innovative circuit topology suitable for low supply voltage should be developed in order to leverage the advanced CMOS technology. Moreover, energy harvesting techniques have recently been incorporated into the biomedical sensor system to further improve the user experience by eliminating battery replacement [20]-[22]. Given that ordinary energy harvesting sources (e.g., thermal, solar, electrical) output relatively low voltages ranging from 30mV to 1V, the supply voltage of the sensor system should be brought down accordingly to increase the conversion efficiency of the power management circuits.

(3) Cost: For high volume applications such as WBANs, the cost of a single transceiver in the network is supposed to be kept low to enable disposal/ubiquitous sensor deployment. When talked in integrated circuit design, this means that the

implementation should avoid any expensive manufacture process and target as small active area as possible.

A number of implementations of WBANs with impressive performance have been published recently. However, at least one of the three key features discussed above is still open for optimization in each prior art (Details of the prior arts overview and comparison will be expanded in Chapter II). Therefore, this dissertation is going to explore the trade-offs among the stringent design specifications of high performance applications in WBAN and propose an innovative wireless receiver architecture satisfying all three key features without sacrificing major performance.

1.4 Dissertation Organization

Chapter 2 starts with an overview and comparison of the existing short range wireless standards, followed by an overview of the prior techniques utilized in low-power high-performance wireless receiver design. Then the summary and comparison of the prior arts are drawn.

Chapter 3 first introduces the background and the key challenges in low-power wireless receiver design, then elaborates the system-level considerations for successfully utilizing the digital-intensive architecture. Next, the design of circuit building blocks is described in detail. After that, experimental results are shown to validate the proposed architecture and techniques. The performance summary of this work and comparison with prior arts are made at last.

Chapter 4 concludes this dissertation by summarizing the analysis and selection of the wireless standard and the receiver architecture, circuit design techniques, and the contribution of this dissertation.

Chapter 2. Background

2.1 Overview of Short Range Wireless Standards

When communication distance and bandwidth are considered particularly for body area network applications, most popular wireless standards include Bluetooth Low Energy (BLE), IEEE 802.15.4 (WPAN) and IEEE 802.15.6. Although the last standard is also known as Wireless Body Area Network (WBAN), it will be always referred as IEEE 802.15.6 to avoid confusion with the actual WBAN (which indicates the network instead of the standard) in this dissertation. Among all the frequency bands that the standards specify, the 2.4GHz band is selected here to perform the comparison for two main reasons: 1) this is a common frequency band that every standard listed above specifies; 2) the form factor of the final implementation in 2.4GHz will be relatively small if half-wave antennas have to be utilized to maintain high radiation efficiency.

BLE was originally introduced by Nokia in 2006 under the name Wibree, and then absorbed into the main Bluetooth standard in 2010 [23]. It aims at low-power short-range applications in healthcare, fitness, security and home entertainment. Different from the classic Bluetooth protocol (i.e., Bluetooth Basic Rate), BLE operates in connectionless mode, which significantly decreases the on-time of the radio, thus features considerably lower average power consumption without decreasing the communication rage. Frequency hopping is utilized in BLE to handle the co-existence of different radios in 2.4GHz band.

IEEE 802.15.4 (WPAN) focuses on low-cost, low-speed communication between nearby devices with little to no underlying infrastructure [24]. The standard only defines fundamental lower network layers including media access control protocol and physical layer, upon which other higher level standards (e.g., ZigBee, WirelessHART, etc.) further develop the upper layers which are not defined in WPAN to specify the entire protocol for different applications. Other than BLE, WPAN performs Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA) or ALOHA protocol to deal with the in-band interference from other devices occupying same frequency band.

IEEE 802.15.6 is an international standard for short-range wireless communication in close proximity to, or inside, a human body [25]. It combines the requirements of reliability, quality of service (QoS), low power and data rate for medical and relevant application environments. IEEE 802.15.6 also performs CSMA/CA or ALOHA protocol for collision avoidance. Among the three physical layers defined in this standard, this dissertation mainly focuses on the narrowband (NB) specification.

Table 2.1 compares the primary physical layer specifications in typical operation mode among the three standards.

Table 2.1: Physical Layer Specification Comparison in Typical Mode

Specifications	Bluetooth LE	IEEE 802.15.4	IEEE 802.15.6
Modulation	GFSK	O-QPSK	π/4-DQPSK
Raw peak bit rate	1 Mbps	250 kbps	1.2 Mbps
Channel spacing	2 MHz	5 MHz	1 MHz
TX minimum output power	-20 dBm	-3 dBm	-10 dBm
Adjacent channel power ratio	<0 dB	-20 dB	-26 dB
RX maximum sensitivity	-70 dBm	-85 dBm	-83 dBm
Adjacent channel rejection	-15 dB	0 dB	9 dB

Although BLE specifies a raw peak bit rate of 1Mbps, it is intended to provide much lower power consumption by heavily duty-cycling the device. Thus BLE devices usually achieve an actual throughput of around 0.27Mbps, and are applied for state-report operations. WPAN specifies an even lower raw peak bit rate of 250kbps, preventing itself from applications requiring relatively high data rate. On the contrary, IEEE 802.15.6 specifies 1.2Mbps raw peak bit rate and achieves a reasonably good information rate of 971kbps for a typical transmission packet including the preamble, header and BCH coding. When data streaming with relatively high bandwidth is required such as in wireless endoscopy and audio, IEEE 802.15.6 should be the first choice.

Besides, when a BLE transceiver transmits minimum power of -20dBm, and achieves -70dBm sensitivity (i.e., worst case), it can only handle 50dB path loss, which is not sufficient for the body area network applications based on the discussion in Chapter 1. WPAN accommodates 82dB path loss when the transceiver operates in worst case, but the minimum output power for TX is relatively high. When compared to IEEE 802.15.6, the transmitter implemented in WPAN has to deliver 7dB higher (which is 5 times) output power, resulting in an asymmetric wireless link very likely. In general, the link budget defined in IEEE 802.15.6 is more appropriate for body area network applications than the other two.

Moreover, IEEE 802.15.6 specifies the smallest channel spacing (1MHz) out of the three standards, which allows more channels with fixed communication bandwidth. This feature can be critical for body area network applications when a large number of sensor nodes are expected, since the allowed bandwidth at 2.4GHz is very limited.

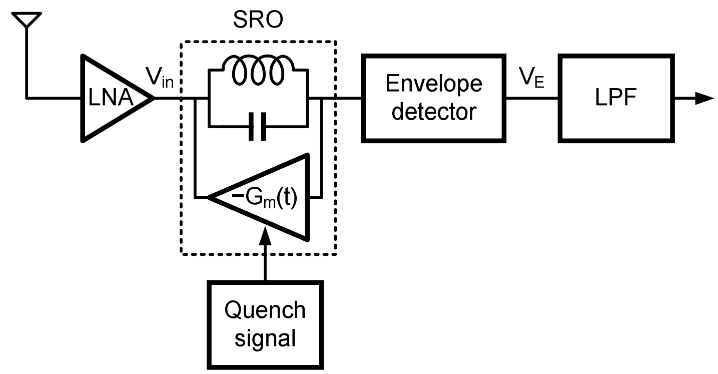
Last but not least, in addition to the classical ISM band of 2.4G to 2.5GHz, IEEE 802.15.6 also releases a frequency band of 2.36GHz to 2.4GHz for narrowband physical layer. The latter one is a much quieter band with only a few primary users (Aeronautical mobile telemetry and radio astronomy) and not specified in either BLE or WPAN. Thus, IEEE 802.15.6 provides higher reliability than the other two standards.

Therefore, IEEE 802.15.6 will be principally referred when examples of transceiver specifications are needed in this dissertation. Nonetheless, the proposed architecture and techniques are applicable to many other low power wireless standards as well.

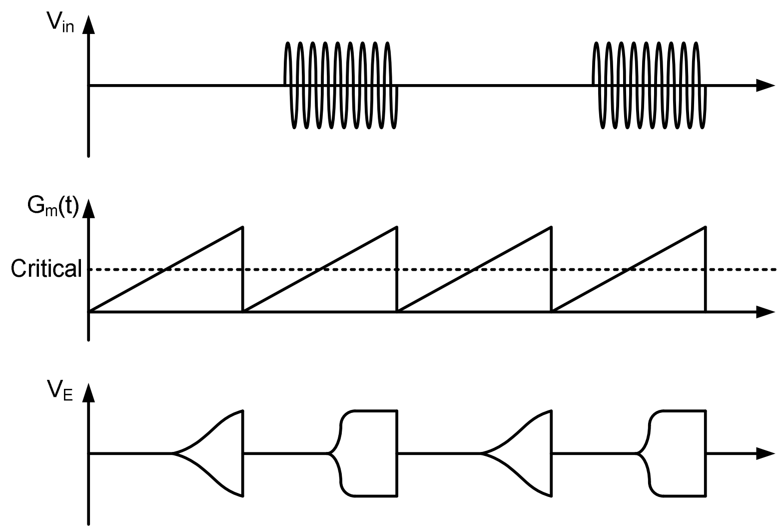
2.2 State-of-the-Art Low Power Receivers

2.2.1 Super-Regenerative Receivers

Super-regenerative receivers (SRRs) are well suited to low-power, short-range wireless communications due to their exceptional low hardware complexity. Based on the principle introduced by Armstrong in 1922 [26], a number of implementations have been published with significant reductions in power consumption [27]-[30]. Figure 2.1 (a) shows the typical SRR system block diagram, including the LNA, the super-regenerative oscillator (SRO), the envelope detector and the low pass filter. With the elimination of high frequency mixing and multi-bit analog-to-digital conversion (ADC), and the duty-cycled operation of the SRO, the overall power consumption is decreased. Sometimes the LNA is also removed to further reduce the power dissipation.



(a)



(b)

Figure 2.1: (a) SRR system block diagram (b) SRO principle

Positive feedback in the SRO can be tuned by a periodic quench signal, usually with the form of saw tooth or sine wave, to drive the SRO from quenching into oscillation repeatedly. General solutions for the SRO output waveform with arbitrary quench signal can be found in [31]. For the specific case of saw tooth quench signal, the time-domain response of the SRR is shown in Figure 2.1 (b). The critical G_m is defined as the value when the positive feedback exactly cancels the intrinsic loss of the selective network (usually an LC tank) in the circuit. In other words, when $G_m(t)$ is larger than $G_{m,critical}$, then SRO starts oscillating. Since the oscillation builds up from the original amplitude proportional to the input signal [29], the settling of the oscillation with the existence of RF signal is faster than that with the noise floor only. Therefore the envelope of the SRO output can be sampled to demodulate OOK modulated signal.

This kind of selectivity does not only happen to the amplitude, but also to the frequency of the input signal. As demonstrated in [30], if the SRO has a free running frequency of f_0, and there are two input RF signals with carrier frequency of f_1 and f_2 satisfying $|f_1 - f_0| < |f_2 - f_0|$, the SRO settling with signal f_1 will be faster than that with signal f_2. Then the same methodology used in OOK demodulation can be applied to demodulate FSK signals.

However, the frequency selectivity of the SRO is not very practical for FSK modulation with small frequency shift. The settling time difference for two carriers with 1MHz space is actually much smaller than 1ns even with a tank quality factor of 1000 [30], while BLE specifies a maximum frequency deviation of only 275kHz for the GFSK modulation. This poor selectivity also impairs the adjacent channel rejection (ACR) of SRRs when the channel spacing is narrow. Besides, since the envelop of the SRO output does not preserve any phase information of the RF signal, SRRs are never used in wireless communications which employ phase modulation, such as phase-shift-keying (PSK) and Quadrature Amplitude Modulation (QAM).

2.2.2 Current-Reuse Receivers

By stacking different functional blocks (usually analog cells) on top of each other to reuse the bias current as shown in Figure 2.2, an RF front-end can have less number of biasing branches while maintaining similar functionality and performance. This current-reuse technique is very popular when the supply voltage is relatively high and the headroom for the analog building block is sufficient [32]-[37], and generally saves more than 50% power consumption when compared to the traditional non-stacking receiver topology [35].

The drawback of this technique is also prominent. Although several prior arts try very hard to not only stacking the blocks but also share as many devices as possible to reduce the required headroom [35], [36], supply voltages applied are still above 1.2V for all the implementations. As the CMOS technology scaling down keeps going, supply voltage in this range will no longer be applicable in the future. The relatively high supply voltage also introduces extra power management circuits if one wants separate lower supply for the digital blocks to further save power consumption in the system-on-chip (SoC) design.

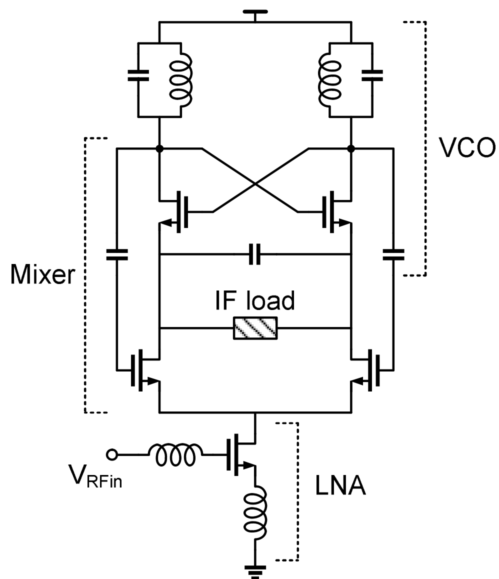


Figure 2.2: Schematic of LNA, mixer and VCO (LMV) stacking front-end

2.2.3 Zero-IF Receivers

A zero-IF receiver, also known as direct-conversion or homodyne receiver, down-converts the RF signal to direct current (DC), with a local oscillation (LO) frequency which is equal or very close to that of the RF carrier, for the following demodulation in the baseband [38]-[43]. Figure 2.3 shows the typical system block diagram of such a receiver. Unlike the standard super-heterodyne receiver, the amplification and the A-to-D conversion after the first mixing in zero-IF receiver are done at an extremely low frequency, so the corresponding power consumption is lower. Besides, image interference is no longer a problem in zero-IF receivers since in-phase and quadrature (I/Q) mixing is applied and/or the image is now the signal itself.

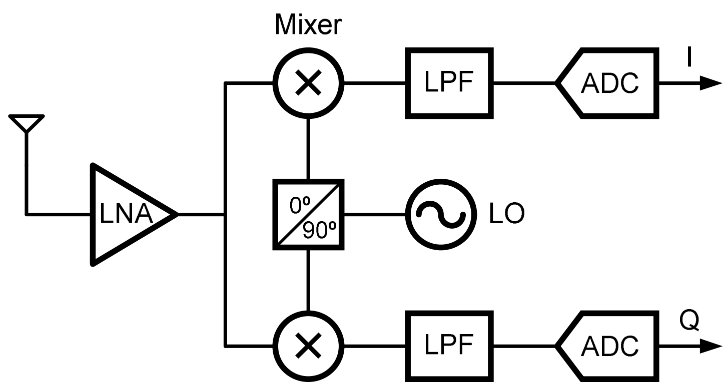


Figure 2.3: System block diagram of the zero-IF (direct-conversion) receiver

However, the I/Q oscillation generation at high frequency is still power consuming. For example, [40] employs a two-stage buffer to introduce 90 degree phase shift in I and Q paths, while the buffer consumes even more power than the frequency synthesis. A quadrature voltage controlled oscillator (QVCO) is utilized in [42] to directly generate I/Q waveform for the mixer, but the QVCO contains two LC oscillation paths which draw twice the current. Another method implemented in [43] is dividing a higher oscillation frequency by 2 to perform the I/Q splitting. Anyhow, increasing the oscillation frequency to twice the carrier frequency still increases power consumption by a large amount.

2.2.4 Sliding-IF Receivers

In order to mitigate the I/Q oscillation generation stress in zero-IF receiver design, an alternative sliding-IF architecture is introduced [44]-[48]. As shown in Figure 2.4, instead of directly down converted to DC from the carrier frequency, the RF signal is first mixed with a lower frequency LO and translated to IF to perform the I/Q mixing, which avoids complicated I/Q oscillation generation in high frequency. An LO frequency of integer times IF is usually chosen to further simplify the I/Q splitting.

Sliding-IF receivers usually achieve lower power consumption than zero-IF receivers, but there is still a trade-off in the frequency plan which sets the lower boundary of the power consumption. For example, when a high LO frequency plan 16/17 (i.e., $f_{LO} = f_{RF} \times 16/17$) is chosen to achieve low IF for low power I/Q mixing, it is difficult to bring down the power consumption of LO generation [45],

[46]. On the contrary, when a low LO frequency plan 2/3 is performed, the I/Q mixing at IF will increase significantly and consume as much power as the LO [44]. As a result, the power consumption reduction introduced by the sliding-IF architecture is quite moderate.

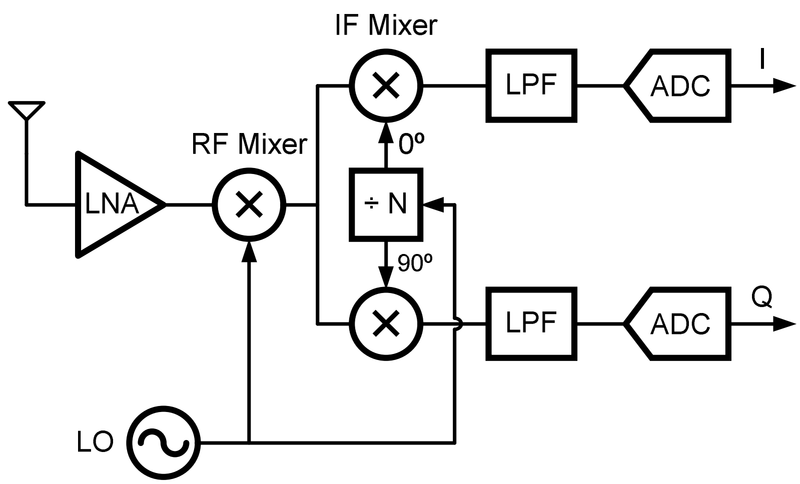


Figure 2.4: System block diagram of the sliding-IF receiver

2.2.5 Transformer-Coupled Low-Voltage Receivers

Transformer-coupled low-voltage design goes to an opposite direction to the current-reuse technique, by pushing the supply voltage to an extremely low level.

As long as the bias current can be maintained the same, the power consumption of the analog circuits can be reduced linearly.

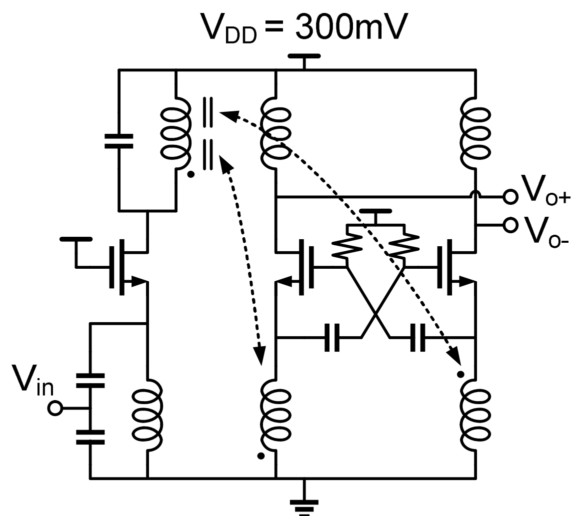


Figure 2.5: Schematic of transformer-coupled low-voltage LNA

Figure 2.5 shows the schematic of the transformer-coupled low-voltage LNA proposed in [49], [50] as an example. In this circuit, the signal at the drain of the input transistor is fed to the cascode transistors through the magnetic coupling of the transformer, therefore no extra DC voltage drop is required. In the mean time, the transformer also performs single-to-differential conversion, which enables the g_m-boosting topology for the cascode transistors.

Despite the power dissipation reduction reported in [49], [50], this architecture still has two major disadvantages: a) transformers generally take a large die area, resulting in increased manufacture cost; b) since this architecture is still analog-intensive, the peak current is not scaled with the supply voltage and remains as high as 5mA or so.

2.3 Performance Summary and Comparison

Table 2.2: Performance Summary and Comparison of Prior Low-Power Receivers

Receiver topology	Power consumption	Supply	Area	Modulation
Super-regenerative	Low	Moderate	Small	OOK/BFSK
Current-reuse	Moderate	High	Moderate	All
Zero-IF	High	Moderate	Moderate	All
Sliding-IF	Moderate	Moderate	Moderate	All
Transformer-coupled	Low	Low	Large	All

Table 2.2 summarizes the key performance of the prior low-power receiver architectures discussed in this chapter. As we can see, there is no existing receiver

topology that simultaneously achieves low power consumption, low supply voltage and small die area, which are some of the most important criteria for successful WBAN implementations (super-regenerative receivers do not support DPSK demodulation). Therefore, innovations in receiver architectures are desired in order to break the trade-offs in existing low-power receiver topologies.

Chapter 3. A 2.4GHz Low-Power Low-Voltage Sub-Sampling Receiver

3.1 Introduction

The IEEE 802.15.6 standard focuses on low power, short range wireless links for biomedical applications [25]. Notably, this standard aims to achieve reliable wireless data links around and/or inside a human body to enable a variety of healthcare services. The targeted application space implies that most WBAN radios will be battery-powered and long operating lifetime requirements motivate minimization of radio power consumption. Furthermore, button cell lithium batteries rated at 3.0 Volts typically have low peak current delivery capacity (e.g., 20mA for CR2032). This makes it desirable to reduce peak RX power consumption, thereby increasing the peak current and power budget for other system components such as bio-sensors and potentially enabling increased local processing for system-on-chip (SoC) solutions. In addition to the peak and average power consumption, the active die area of the implementation must also be minimized to enable low-cost ICs for disposal/ubiquitous WBAN sensor deployment.

As discussed in Chapter 2, the existing low power receiver architectures are still open for optimization in at least one of the three key features of successful WBAN implementations. Therefore in this dissertation, we propose a WBAN-compatible digital-intensive receiver architecture that leverages sub-sampling, Q-enhancement and digital IF to simultaneously achieve low power, low voltage, low peak current, and small active die area [51]. System design considerations for the proposed sub-sampling architecture are introduced in Section 3.2. The receiver topology and the detailed circuit design of key building blocks are discussed Section 3.3. Measurement results of the sub-sampling receiver prototype are shown in Section 3.4, validating the proposed architecture. Finally, performance summary and comparison with prior-arts are drawn in Section 3.5.

3.2 System Level Analysis

RF and analog architecture and circuit techniques can substantially reduce RX power consumption. However such techniques are limited by the power consumption of the LO-generation circuits and the analog IF. For example, in [47], a sliding-IF RX topology and a push-pull RF mixer lead to state-of-the-art ~3.8mW power consumption. Notably, the circuits related to frequency translation, including LO generation and high frequency mixing, consume over 50% of the total power budget. Furthermore, the analog IF stage also consumes a significant share (~25%) of the total power. Achieving further reductions in power consumption for sub-1mW RX operation requires a holistic approach that includes architectures and circuits to minimize analog and high-frequency building blocks. In this work, we investigate sub-sampling in the RF frontend to reduce power in the frequency translation circuits, and focus on a digital IF scheme that takes advantage of advanced CMOS nodes and uses standard digital place-and-route synthesis methodology to replace analog IF signal processing.

3.2.1 Low Noise Figure Operation in Sub-Sampling

As shown in Figure 3.1 (a), when a signal is sampled at the frequency f_S, the spectrum around harmonics of f_S or Nf_S , where N is an integer, is translated to DC, along with the desired signal. As long as f_S is larger than twice the sampled signal bandwidth f_{SB}, aliasing can be avoided. For narrow band receivers, the signal bandwidth f_{SB} is much smaller than the carrier frequency f_{RF} ($f_{SB} \ll f_{RF}$) and hence f_S satisfying non-overlapping criterion ($f_S > 2f_{SB}$) can be much lower than f_{RF}. However, selecting $f_S \ll f_{RF}$ leads to frequency translation from the noise bands at image frequency (f_{IMi}, $i = 1,2,3,...$) with respect to each harmonic of f_S. This well-known noise folding phenomena in sub-sampling can seriously degrade the overall noise figure [52]. For this reason, sub-sampling is seldom employed at RF to perform frequency translation in prior arts [37], [53], [54], which only gain moderate improvement on power consumption.

This degradation due to noise folding can be reduced by placing a highly selective filter at RF that reduces the noise from other harmonics of f_S, as shown in Figure 3.1 (b).

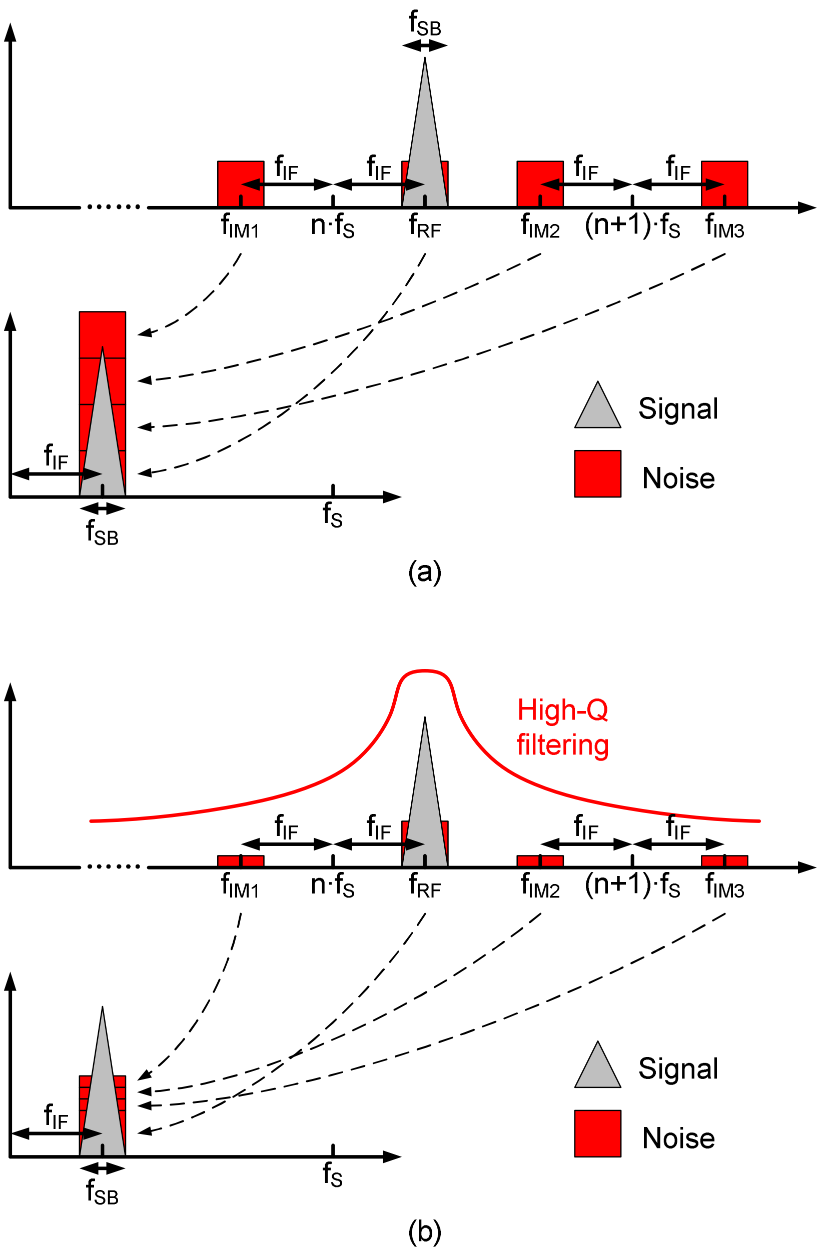


Figure 3.1: Noise folding in sub-sampling (a) without and (b) with preceding high-Q filtering

The system NF can be calculated for combinations of RF filter bandwidths, Q, and sub-sampling frequency f_S as shown in Figure 3.2.

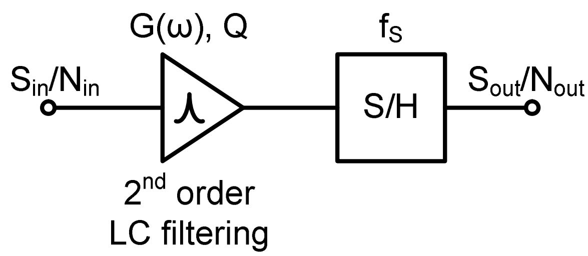


Figure 3.2: Block diagram of the cascaded filtering and sub-sampling stages

Assuming that the gain stage $G(\omega)$ preceding the sample and hold introduces 2nd order filtering with a quality factor Q, the noise factor of the cascaded system can be calculated as

$$F_{cascaded} = \frac{S_{in}/N_{in}}{S_{out}/N_{out}}$$

$$= \frac{1}{G(\omega_0)} \cdot \frac{N_{in} \sum_{k=0}^{\infty} G\left(\omega_0 \pm k \cdot \frac{f_S}{2}\right) + \frac{N_{G(\omega_0)}}{G(\omega_0)} \sum_{k=0}^{\infty} G\left(\omega_0 \pm k \cdot \frac{f_S}{2}\right)}{N_{in}}$$

$$= \frac{N_{in} G(\omega_0) + N_{G(\omega_0)}}{N_{in} G(\omega_0)} \cdot \sum_{k=0}^{\infty} \frac{G\left(\omega_0 \pm k \cdot \frac{f_S}{2}\right)}{G(\omega_0)}$$

$$= F_{G(\omega_0)} \sum_{k=0}^{\infty} \frac{G\left(\omega_0 \pm k \cdot \frac{f_S}{2}\right)}{G(\omega_0)} \tag{3.1}$$

where $N_{G(\omega_0)}$ denotes the noise spectrum density contributed by $G(\omega)$ at frequency ω_0, and $F_{G(\omega_0)}$ denotes the noise factor of $G(\omega)$ at frequency ω_0. The expression for noise factor in (3.1) assumes a) the spectrum of input noise and the spectrum of the noise contributed by the gain stage before filtering are flat across the frequency of interest; b) the gain of the sample and hold stage is 0dB; and c) that the IF equals $f_S/4$ (discussed further in Section 3.2.2). As we can see in (3.1), the noise factor of the cascaded system consists of the sum of the scaled noise factor of $G(\omega)$ at ω_0, where the scaling factor is the normalized gain at all image frequencies. The relationship among NF, f_S and Q, based on (3.1) is shown graphically in Figure 3.3.

This figure indicates that low NF operation at 2.4GHz RF can be achieved using sub-sampling receivers for sampling frequency f_S higher than 150MHz if filter Q is larger than 100. While such high-Q filters can be achieved using external or co-integrated components such as BAW or FBAR resonators [53], [55], this work focuses on fully-integrated RX in a commercial CMOS technology with no external high-Q filters. Since the Q of on-chip RF inductors in CMOS technologies is < 20 even with thick metal layers in the backend, active Q-enhancement in the LNA is utilized in this work to achieve the desired narrowband filtering at RF.

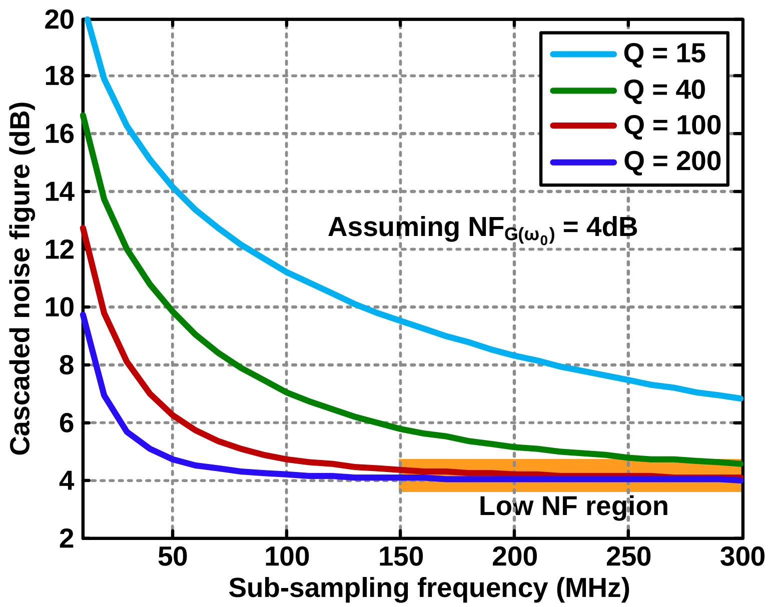


Figure 3.3: Cascaded noise figure vs. sub-sampling frequency for different filter Q

Q-enhancement technique intrinsically degrades the front-end linearity, therefore limiting the RX large signal performance. However, for typical short-range low-power communication, the transmitter (TX) output power is relatively low (< 0dBm) and therefore adjacent channel interferers can be tolerated while achieving targeted BER with linearity degradation caused by Q-enhancement. For example, the WBAN standard specifies an adjacent channel power of 9dB with received signal amplitude 3dB higher than reference sensitivity and as shown in Section 3.4.5, the proposed RX achieves targeted 10^{-3} BER for such adjacent channel power.

3.2.2 Front-End Frequency Tunability

The Q-enhanced RF front-end should have sufficient frequency tunability to closely align the center frequency with the RF signal carrier, to avoid reduction and variation in gain. As shown in Figure 3.4, if the least significant bit (LSB) of RF front-end frequency tuning is f_L, the signal carrier frequency f_C will be $f_L/2$ off with respect to the front-end center frequency f_O in the worst case.

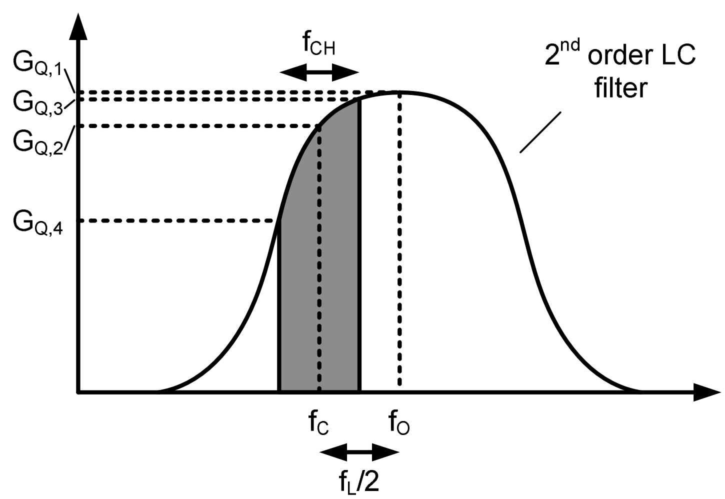


Figure 3.4: Gain reduction and fluctuation in high-Q RF front-end

The gain reduction due to an offset between RF carrier and center frequency can be calculated as

$$\Delta G_Q = G_{Q,1} - G_{Q,2} = G_Q(f_O) - G_Q\left(f_O - \frac{f_L}{2}\right) \tag{3.2}$$

where

$$G_Q(f) = \frac{1}{\sqrt{Q^2\left(\frac{f}{f_O} - \frac{f_O}{f}\right)^2 + 1}}$$

denotes the normalized gain profile of the 2nd-order LC filter. The gain variation across the channel bandwidth can also be calculated as

$$\Delta G_{CH} = G_{Q,3} - G_{Q,4} = G_Q\left(f_O - \frac{f_L}{2} + \frac{f_{CH}}{2}\right) - G_Q\left(f_O - \frac{f_L}{2} - \frac{f_{CH}}{2}\right) \quad (3.3)$$

where f_{CH} is the channel bandwidth. Figure 3.5 (a) and (b) graphically represent (3.2) and (3.3), respectively, demonstrating that 1MHz resolution in frequency tuning is sufficient to ensure less than 0.5dB reduction and variation in gain for filter Q in the range of 50 to 400 that are of interest in this work.

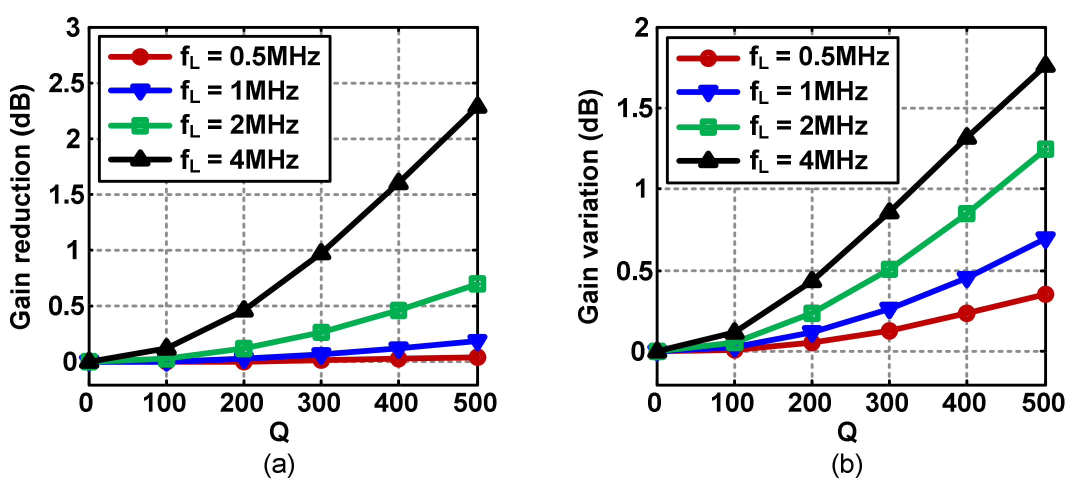


Figure 3.5: (a) Gain reduction and (b) gain variation versus Q for different frequency tuning LSB

3.2.3 Frequency Plan

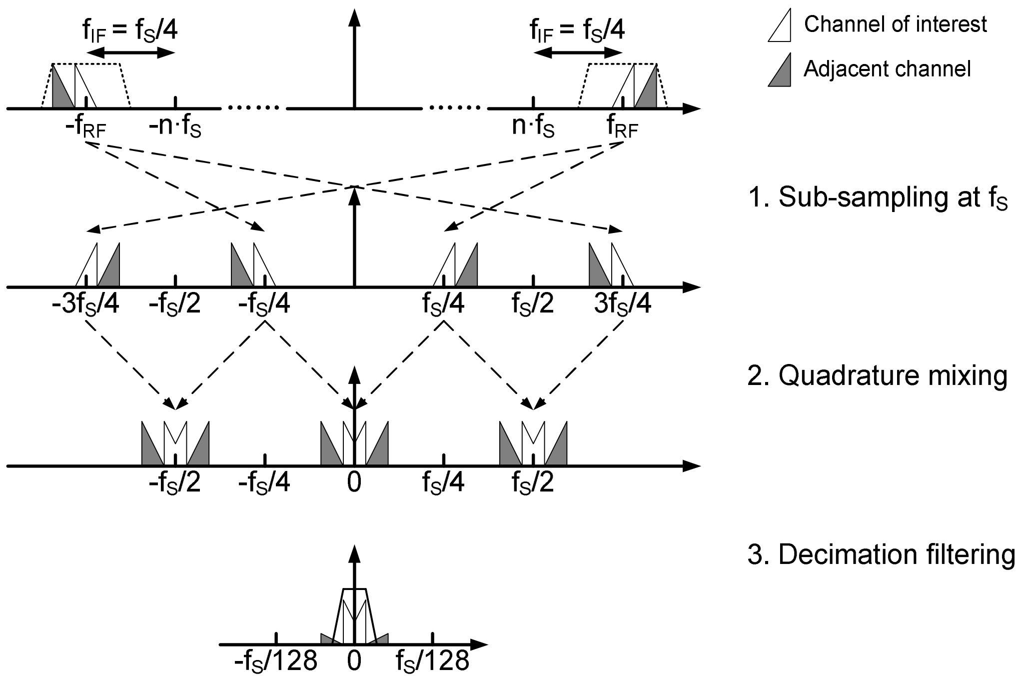


Figure 3.6: Frequency plan of the proposed sub-sampling receiver

Figure 3.6 shows the frequency plan of the proposed sub-sampling receiver. The received signal is filtered and amplified at RF by the high-Q front-end, and then translated to IF by the sub-sampling mixer. Subsequent quadrature down-conversion is achieved in the digital domain. Selecting an IF frequency that is $f_S/4$, where f_S is the sampling frequency, results in a sampled quadrature wave at IF where

$$\cos 2\pi f_{IF} \cdot \frac{N}{f_S} = \cos 2\pi \frac{f_S}{4} \cdot \frac{N}{f_S}$$

$$= \cos \frac{\pi}{2} \cdot N = \{1,0,-1,0,\ldots\}, \qquad N = \{0,1,2,3,\ldots\}$$

$$\sin 2\pi f_{IF} \cdot \frac{N}{f_S} = \sin 2\pi \frac{f_S}{4} \cdot \frac{N}{f_S}$$

$$= \sin \frac{\pi}{2} \cdot \mathrm{N} = \{0,1,0,-1,\ldots\}, \qquad \mathrm{N} = \{0,1,2,3,\ldots\} \tag{3.4}$$

According to (3.4), the digital quadrature mixing operation at IF assigns odd (even) quantized samples to I (Q) channel. While this mixing scheme implies an equivalent sampling scheme of $f_S/2$, it facilitates the design of the interface between the high-Q LNA and the sample and hold circuit (discussed in detail in Section 3.3.1). Decimation filtering of the digital quadrature mixer output attenuates the adjacent channel interference. The effective sampling rate of the decimation filter output is 4.92MHz, oversampling the baseband signal by a factor of 8, facilitating baseband signal processing.

3.2.4 Oversampling A-to-D Conversion

The WBAN standard requires 9dB ACR for π/4-DQPSK modulation (channel spacing 1MHz) [25]. Figure 3.7 shows the relative signal and noise power level for ACR measurements according to the WBAN standard. In Figure 3.7, P_S denotes signal power, P_A denotes adjacent channel power, P_Q denotes the quantization noise level of the ADC, P_N denotes the noise contributed by the input source and the whole receiver chain except for the ADC quantization noise and P_T is the overall noise floor (sum of P_Q and P_N). SNR_{DEM} is the SNR required by the baseband demodulator to achieve 10^{-3} bit error rate (BER). $SQNR_{ADC}$ is the signal to quantization noise ratio of the ADC.

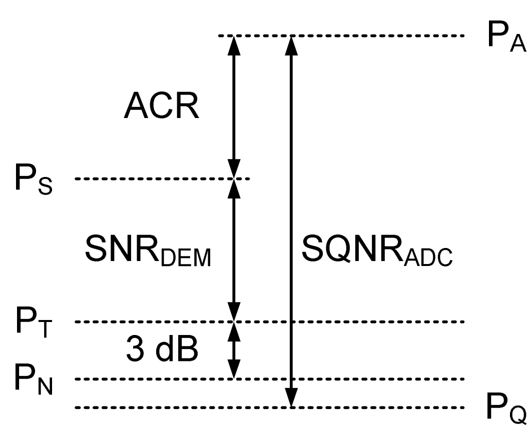


Figure 3.7: Relative signal and noise power level when measuring ACR

The WBAN standard specifies P_S to be 3dB higher than the sensitivity when ACR is measured. Therefore, at 10^{-3} BER for this signal power, overall noise floor P_T is 3dB higher than P_N. This implies $P_Q = P_N$, and hence

$$SQNR_{ADC} = ACR + SNR_{DEM} + 3 \tag{3.5}$$

System simulations were performed to evaluate SNR_{DEM}, resulting in ~17dB target, implying that $SQNR_{ADC} = 29$dB. Therefore, 4.5-bit ADC resolution is targeted for this implementation.

Early digitization in the RX chain reduces the analog components and leverages the standard digital synthesis and place-and-route methodology, resulting in lower power consumption, smaller die area and fewer design iterations, but requires sophisticated design to avoid extra power penalty due to the increased sampling frequency. In this work, the quantizer can be conveniently inserted after the S/H stage to leverage the 150MHz sampling frequency required for low NF operation. Since the S/H oversamples the baseband signal by a factor of 128, an over-sampled, low-resolution ADC scheme is adopted since only 1-bit quantization is necessary at 150MHz to achieve 4.5-bit equivalent ADC resolution, resulting in negligible power overhead and simplified ADC design.

3.3 Circuit Implementation

3.3.1 Receiver Topology

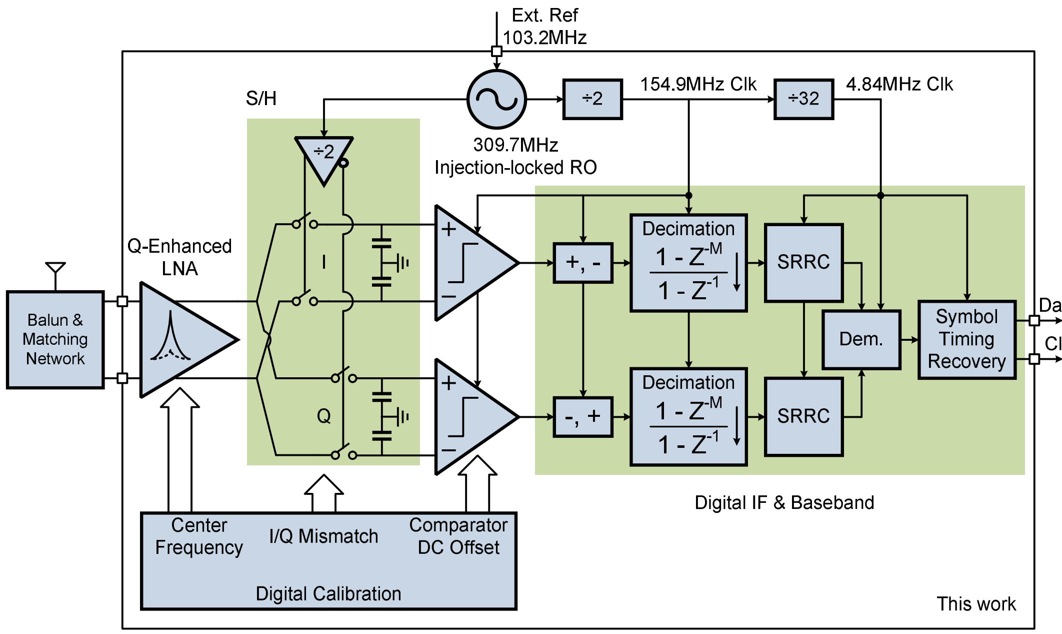


Figure 3.8: System block diagram of the proposed sub-sampling receiver

The architecture of the proposed receiver is depicted in Figure 3.8. The receiver RF signal is first amplified and filtered by the Q-enhancement LNA, then sampled by the sample and hold stage. The sampled signal is provided to a dynamic comparator that performs 1-bit A-to-D conversion. The quantized signal is then fed into the digital IF and baseband circuit for further processing. The local oscillation frequency is chosen to be 309.7 MHz satisfying the noise folding suppression described in Figure 3.3 and (3.1). It must be noted that the sampling rate ensures that the baseband is oversampled by a factor of 128. The only purely analog component in the receiver chain in Figure 3.8 is the Q-enhancement LNA, while the remaining circuits operate dynamically and do not consume static power. Furthermore, the digital-intensive architecture allows the whole IF and baseband to be implemented using standard digital synthesis and place-and-route methodology, simplifying design and layout. As described in Section 3.2.3, the choice of $f_{IF} = f_S/4$, simplifies the IF digital mixing with alternate samples. Therefore, two identical samplers are implemented at the output of the LNA and turned on alternatively which separates I and Q samples. An important benefit of this approach is that it ensures that the Q-enhancement LNA always see a constant load impedance, which is important to keep the resonance frequency of a high-Q tank constant.

3.3.2 Q-Enhancement LNA

The LNA employs differential inductively-degenerated common source architecture as shown in Figure 3.9. Capacitors C_1 through C_4 are added to form a positive feedback with the cascaded transistors M_3 and M_4, resulting in a negative resistance appearing in parallel with the tank, which cancels part of the intrinsic tank resistance and enhances effective tank Q. As mentioned in Section 3.2.2, high-Q operation must be accompanied by fine frequency resolution to ensure that all channels can be received. In this work, coarse tuning is achieved using 128-bit thermometer coded capacitor bank ensuring monotonicity and linearity. 3-bit binary coded thermometer bank provides fine frequency control.

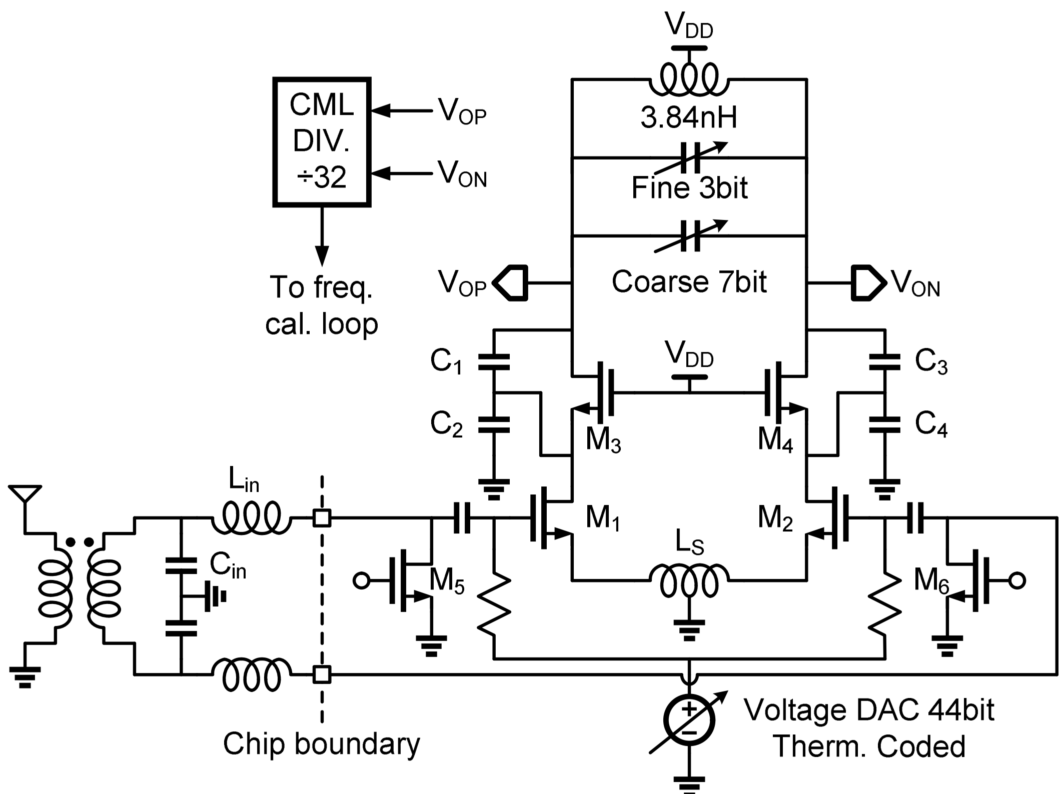


Figure 3.9: Schematic of the Q-enhancement LNA

A voltage DAC with 44-bit thermometer tuning code controls the bias current of the Q-enhancement LNA, enabling a current tuning range from 0.66mA to 3mA with a worst-case tuning step of 90uA to achieve Q as high as 400 (discussed further in following paragraphs). Capacitors C_{in}, inductors L_{in} in matching network and the single-to-differential balun are implemented off-die.

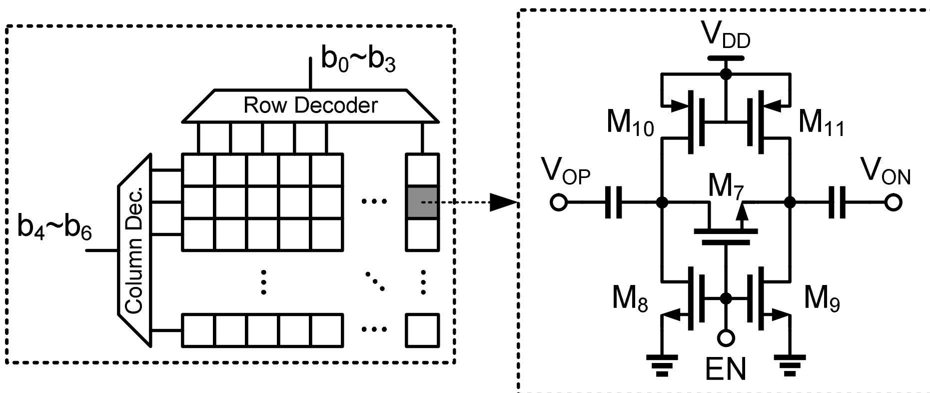


Figure 3.10: Schematic of the coarse tuning capacitor bank

The circuit of a single unit switch capacitor in the coarse tuning bank is shown in Figure 3.10. When a larger capacitance is needed, EN is set to logic high and the drain/source of M_7 is pulled down to ground by NMOS M_8 and M_9, resulting in minimum turn-on resistance for M_7. On the other hand, when a smaller capacitance is needed, EN is set to logic low and the drain/source of M_7 is pulled up to V_{DD} by

PMOS M_{10} and M_{11}, resulting in maximum turn-off resistance for M_7. The widths of M_{10} and M_{11} are made 6 times of that of M_8 and M_9 to make sure pulling up happens when M_8 and M_9 are turned-off.

Variations across process, voltage and temperature (PVT) impact the resonance frequency and the equivalent Q of the LNA output tank. Therefore a frequency and Q-enhancement calibration scheme (shown in Figure 3.11) is necessary for practical operation to facilitate high-Q operation.

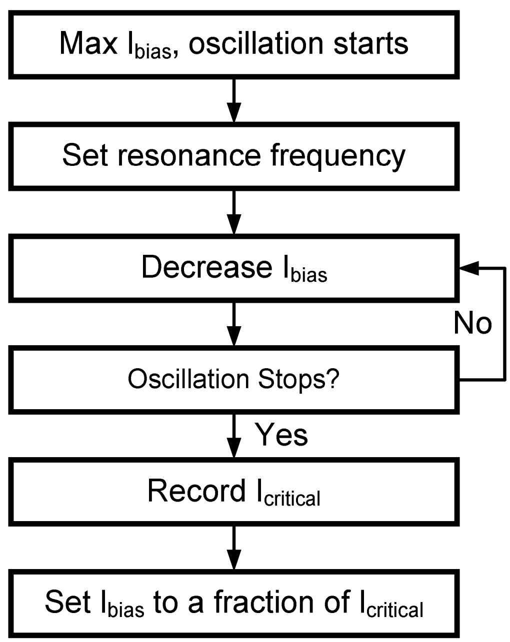


Figure 3.11: LNA output resonance and equivalent Q calibration steps

In this calibration scheme, transistors M_5 and M_6 are turned on initially to short the LNA input and shield interference from external signals during calibration. Following this, the LNA bias current is set to its maximum value, increasing positive feedback leading to oscillation. The oscillation frequency is sensed by comparing it to the reference frequency using frequency dividers and counters, and the resonant tank is tuned to the targeted center frequency by adjusting the coarse and fine tuning code of the capacitor banks. After center-frequency calibration is complete, the bias current is decreased until the amplifier stops oscillating, which is also detected using the counter. This is the so-called critical current for an oscillator. Finally, the operating bias current is set as a fraction of the critical current according to (3.9).

Based on the small signal model of the positive feedback loop consisting of M_3, C_1 and C_2 shown in Figure 3.12 (a), the impedance looking into the drain of M_3 can be derived as

$$Z_d = R_s + \frac{1}{j\omega C_s} = -\frac{g_{m3}}{\omega^2 C_1 C_2} + \frac{1}{j\omega (C_1 \parallel C_2)}$$

therefore the differential impedance looking into V_{OP} and V_{ON} shown in Figure 3.12 (b) is

$$Z_{d,diff} = R_{s,diff} + \frac{1}{j\omega C_{s,diff}} = 2R_s + \frac{2}{j\omega C_s}$$

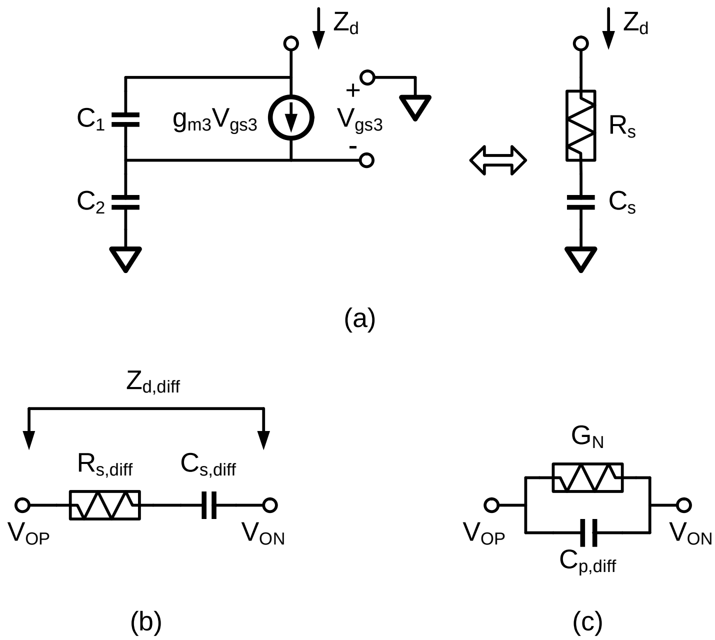


Figure 3.12: (a) small signal circuit of the single-end positive feedback loop; differential impedance of the positive feedback loop in (b) series and (c) parallel

After the series-to-parallel conversion, the negative admittance shown in Figure 3.12 (c) offered by the Q-enhancement circuit is obtained as

$$G_N = -\frac{g_{m3}C_1C_2}{2(C_1+C_2)^2} = -k\sqrt{I_{bias}}\,, \qquad k = \frac{C_1C_2}{2(C_1+C_2)^2}\cdot\sqrt{2\mu C_{ox}\left(\frac{W}{L}\right)_3} \tag{3.6}$$

When the bias current reaches the critical current value, the tank's intrinsic loss G_T should equal the absolute value of the negative admittance in (3.6) as

$$G_T = \frac{1}{Q_T \omega L} = k\sqrt{I_{critical}} \tag{3.7}$$

where Q_T indicates the intrinsic quality factor of the tank. Thus, with the bias current set to be a fraction of the critical current as $I_{bias} = mI_{critical}$, the equivalent Q of the LNA output tank can be derived as

$$Q_{eq} = \frac{1}{(G_T + G_N)\omega L} = \frac{1}{\omega L} \cdot \frac{1}{k\sqrt{I_{critical}} - k\sqrt{mI_{critical}}} = \frac{Q_T}{1 - \sqrt{m}} \tag{3.8}$$

(3.8) can be rearranged as

$$m = \frac{I_{bias}}{I_{critical}} = \left(1 - \frac{Q_T}{Q_{eq}}\right)^2 \tag{3.9}$$

A numeric example of the equivalent Q versus corresponding bias current is shown in Table 3.1 based on (3.9). For a simulated Q_T of 15, a bias current which is 93% of the critical current yields an equivalent Q of 420. The worst-case bias current tuning step of 90uA mentioned in this part earlier is only 4% of simulated critical current, ensuring that Q of 420 can be achieved by appropriate I_{bias} setting.

Table 3.1: Numeric Example of the Equivalent Q vs. Bias Current

I_{bias}/I_{crit}	Q_{eq}
75%	112
80%	142
85%	192
90%	292
93%	421
Simulated Q_T = 15	

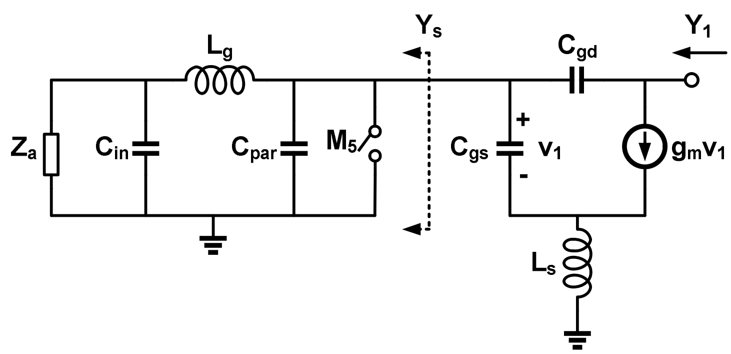


Figure 3.13: Small-signal circuit of the input matching network and transistor

The difference in LNA output resonance frequency with switch M_5 off and on must be considered to ensure calibration with M_5 on is valid during actual operation with M_5 off. The admittance looking into the drain of M_1 can be derived using the small-signal circuit shown in Figure 3.13 (C_{par} denotes the lumped parasitic capacitance due to M$_5$ and the pad) as

$$Y_1 = sC_{gd}\left(1 + \frac{g_m}{s^2 g_m L_s C_{gd} + s\left(g_m L_s Y_s + C_{gs}\right) + Y_s}\right) \tag{3.10}$$

where Y_s is the admittance looking to the left side of M$_5$ (assuming $\omega^2 L_s C_{gd} \ll 1$, $\omega^2 L_s C_{gs} \ll 1$, and ignoring the channel-length modulation and body effect). When switch M$_5$ on and off, we have

$$Y_{s,off} = \frac{1 + sC_{in}Z_a}{s^2 L_g C_{in} Z_a + sL_g + Z_a} + sC_{par}, \qquad Y_{s,on} = \infty \tag{3.11}$$

Thus, the difference in Y_1 with switch M$_5$ on and off is

$$\Delta Y_1 = sC_{gd} \cdot k_n, \quad k_n = \frac{g_m}{s^2 g_m L_s C_{gd} + s\left(g_m L_s Y_{s,off} + C_{gs}\right) + Y_{s,off}} \tag{3.12}$$

Since the magnitude of the k_n is smaller than 5 for typical g_m, L_s, C_{gd}, C_{gs} and $Y_{s,off}$, and C_{gd} is much smaller than C_2 in Figure 3.9, the LNA output resonance frequency variation due to the change of Y_1 can be ignored, ensuring that accurate calibration can be performed with M$_5$ on.

3.3.3 Sample-and-Hold Stage

The holding capacitor at the sample-and-hold stage should be large enough to suppress the kT/C noise for low NF, but small enough to accommodate resonance tuning capacitor banks and positive feedback capacitors that are a significant fraction of the total capacitance at the LNA output. For 290K room temperature, 1MHz system bandwidth, 40dB voltage gain and 4dB NF of LNA, 0dB gain of the sample and hold stage, the amplitude of the noise contributed by the input source and the LNA can be estimated as

$$N_{in,LNA} = -174dBm + 10\log 10^6\, dB + 40dB + 4dB = -70dBm = (100\mu V)^2$$

The kT/C noise contribution from the sample-and-hold switch is

$$N_{kT/C} = \frac{kT}{C_{hold}} \times 2 \times \frac{1}{128}$$

where the factor 2 indicates that there are two differential holding capacitors and the factor 1/128 is due to the filtering of the following digital IF and baseband. Thus, 60fF holding capacitor yields

$$N_{kT/C} = 0.1N_{in,LNA}$$

indicating that the contribution of kT/C noise is negligible.

3.3.4 1-bit Quantizer

The architecture achieves early low-resolution quantization using a dynamic comparator that performs 1-bit quantization shown in Figure 3.14. Since the comparator inputs are driven by the preceding holding capacitors, a two-stage architecture is implemented to isolate the holding capacitors and the regenerative Armstrong latch.

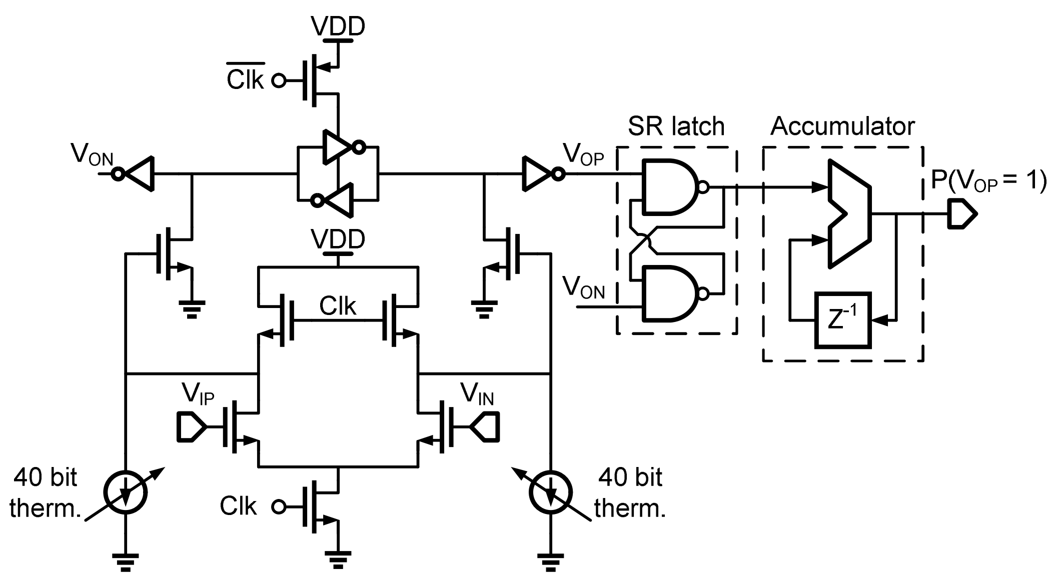


Figure 3.14: Schematic of the 1-bit A-to-D converter

As the signal is at IF ($f_{RF} - Nf_S$ = 77.4MHz) when it is quantized, comparator DC offset does not impair signal spectrum after I/Q mixing and low pass filtering in digital domain as long as the offset does not saturate the comparator. However, the offset must be reduced to ensure that RX can detect the targeted -90dBm signal at RX input. Given the LNA gain of ~40dB, the -90dBm signal at RF input implies ~1mV signal amplitude at comparator input. In this work, comparator DC offset calibration is implemented with the tunable current sources on both sides of the comparator input. By adjusting the current drawing from the drain of the input transistors, the DC offset of the comparator due to the mismatch of the transistor's size/threshold and parasitic variations can be cancelled. The calibration achieves 1 mV LSB, which yields a 0.5mV worst-case DC offset residue.

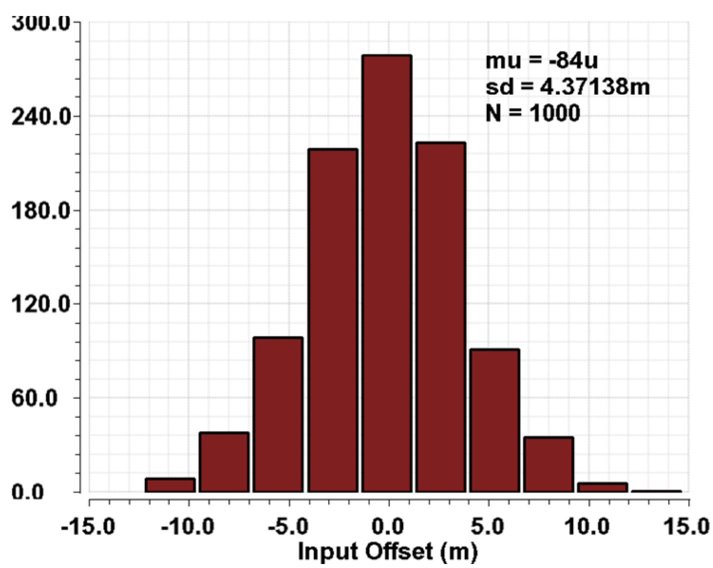


Figure 3.15: Monte Carlo simulation of the quantizer input DC offset

Figure 3.15 shows the 1000-run Monte Carlo simulation of the quantizer input DC offset, with a standard deviation of 4.4mV. Therefore a 40-bit thermometer coded current DAC is implemented to cover up to 9-σ of the DC offset variation. With the comparator inputs connected to fixed DC voltage, the following 16-bit accumulator adds up the comparator output through 2^{16} comparisons to calculate the probability of ‘1’s. Since the input-referred noise voltage amplitude of the comparator satisfies Gaussian distribution for a large number of samples, this probability will reflect the equivalent differential input voltage (i.e., the sum of the input voltage and the input-referred DC offset), and therefore quantify the DC offset residue.

3.3.5 Local Oscillation

Ring oscillators are superior to LC oscillators with respect to die area and power consumption when the oscillation frequency is relatively low. In this dissertation, a 4-stage, cross-coupled, current starved differential ring oscillator is implemented to provide 100MHz-to-360MHz local oscillation, as shown in Figure 3.16. All delay cells in the oscillator share one top and one tail current source, which can be programmed by the 4-bit current DAC to control the free running frequency.

Injection locking is achieved by the NMOS transistor M_1 syncing the transition of the delay cell with the reference frequency when its gate voltage is high. To make use of the 3rd sub-harmonic injection locking with the off-die reference of 103.2MHz, a pulse generator is inserted to prevent the injection signal from quenching the ring oscillator.

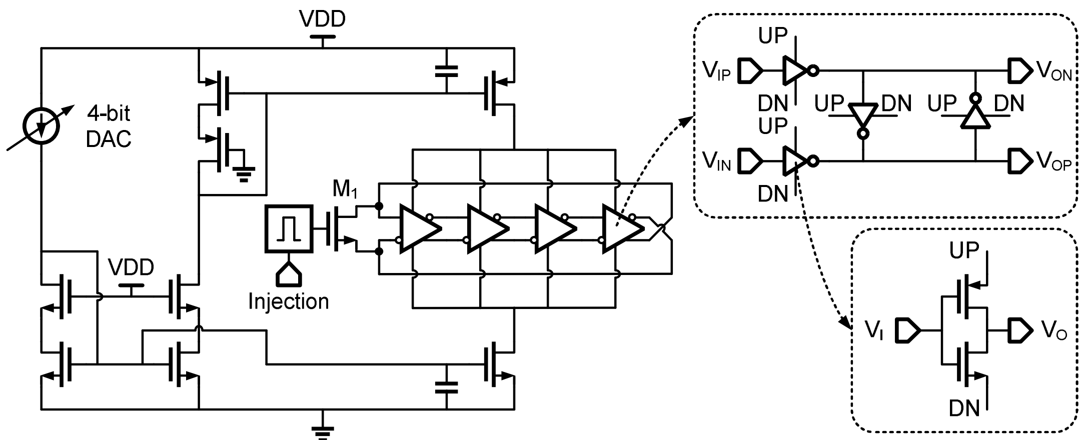


Figure 3.16: Schematic of the ring oscillator.

3.3.6 Clock Generation

Unlike traditional I/Q receivers that have 90° phase shift in I/Q oscillations, I/Q separation in this sub-sampling receiver is performed by two clocks with 180° phase difference, generated by a cross-coupled divider, as shown in Figure 3.17. SHI and SHQ denote the sampling clock for I channel and Q channel S/H stage, respectively. Phase asymmetry between I/Q sampling clock is trimmed through the tunable delay line inserted in each clock path. QI and QQ denote the clock driving the 1-bit quantizers in I channel and Q channel, respectively. The quantizers are fully reset in the sample phase of the corresponding samplers, minimizing the parasitic capacitance contributed to LNA output.

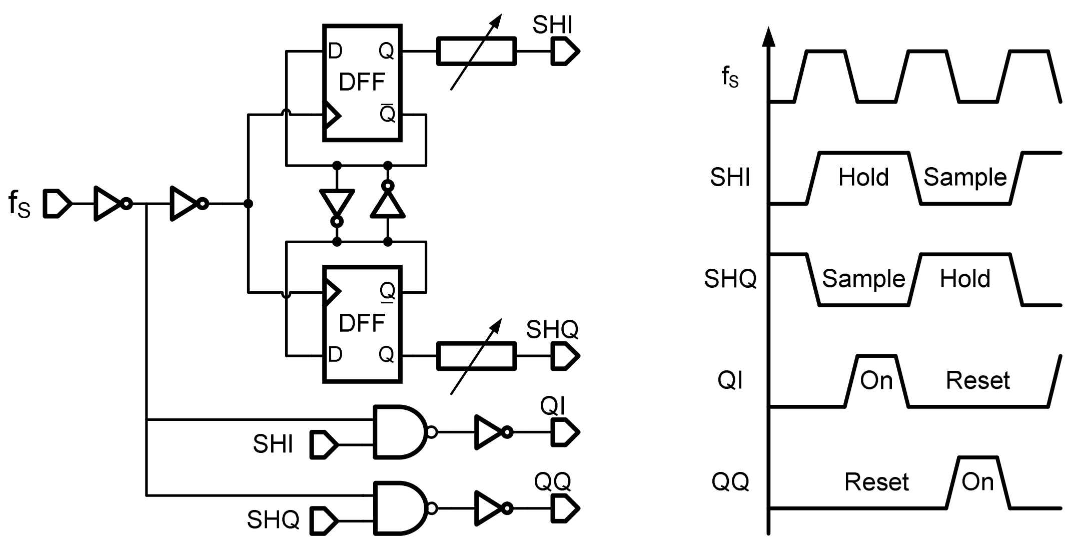


Figure 3.17: Schematic and timing diagram of the clock generation circuit

3.3.7 Digital Intermediate Frequency (IF) Stage

Figure 3.18 shows the block diagram of the modified cascaded integrator-comb (CIC) filter which performs decimation filtering. The sampling frequency of the quantized samples, 154.9MHz, leads to a decimation rate of 128 for 500 kHz signal bandwidth in baseband. However, the down-sampling rate in the decimation filter is set to 32 in order to ensure adequate data-transition timing resolution for the symbol timing recovery circuit. This results in a baseband clock frequency of 4.84MHz, which is 8-times oversampling for 600kHz symbol rate. The delay in the differentiator is changed to 4 clock cycles in order to keep the decimation rate constant at 128.

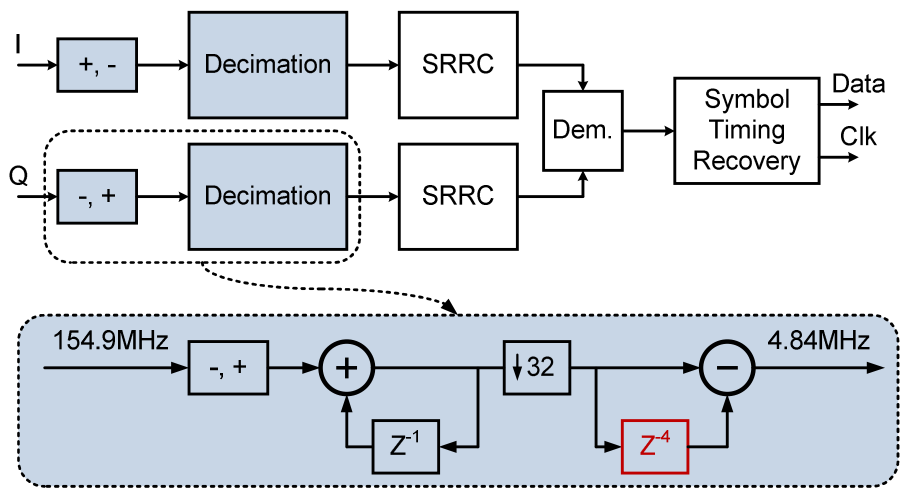


Figure 3.18: Block diagram of the modified CIC filter

3.3.8 Digital Baseband

IEEE 802.15.6 NB specifies Raised-cosine filter response to result in zero inter-symbol interference (ISI) and splits the task equally to TX and RX. Therefore at the

RX side, a square-root-raised-cosine (SRRC) filter is required to perform the matched filtering to the TX filter. It is also the channel selecting filter which removes the adjacent channel interference. In this work, the SRRC filter is implemented with the finite impulse response (FIR) filter architecture because it is inherently stable, offers linear phase response, and is much easier to design than the infinite impulse response (IIR) filter. As the SRRC filter features symmetric time domain response, only 17 multiplying needs to be performed in the 33rd-order FIR filter, as shown in Figure 3.19.

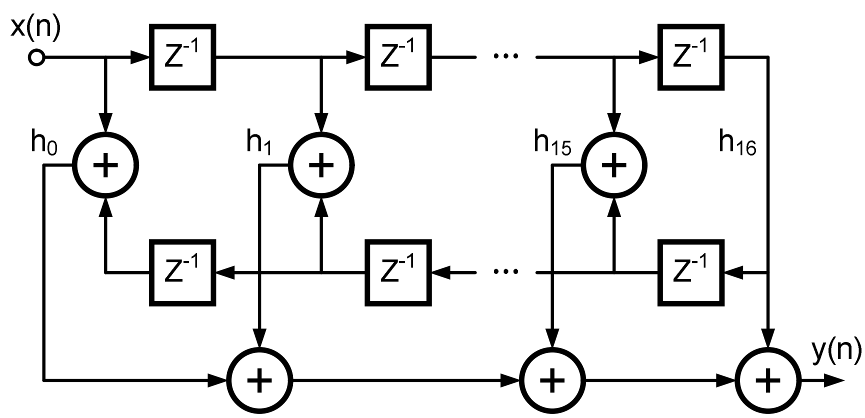


Figure 3.19: Block diagram of the linear-phase-response FIR

Since there is no feedback in the FIR filter, the rounding errors due to finite digital bits in coefficients will not be accumulated through summed iterations. Thus, the coefficients are rounded up to 4-bit signed numbers (shown in Table 3.2) to reduce the hardware complexity and decrease power consumption. Figure 3.20 shows the frequency response of the FIR filter, with 450kHz system bandwidth.

Table 3.2: Coefficients in the 33rd-order FIR Filter

h_0	h_1	h_2	h_3	h_4	h_5	h_6	h_7	h_8
0	0	0	0	0	-1	-1	-1	-1
h_9	h_{10}	h_{11}	h_{12}	h_{13}	h_{14}	h_{15}	h_{16}	
0	1	2	4	5	6	7	7	

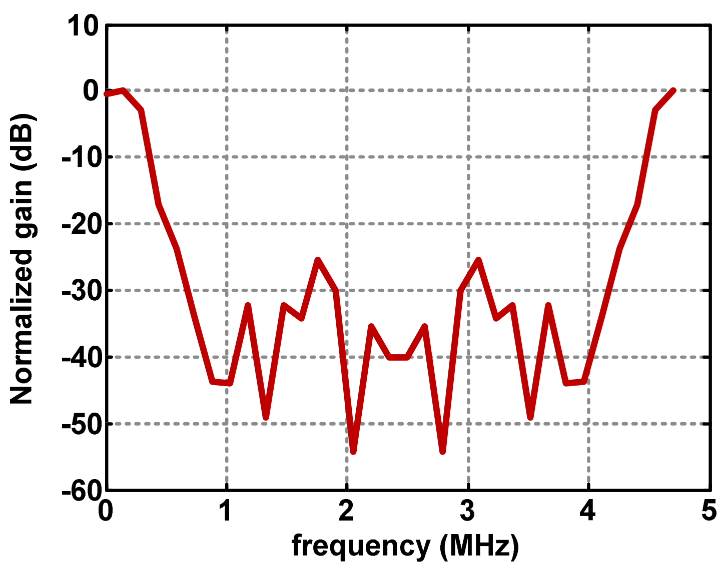
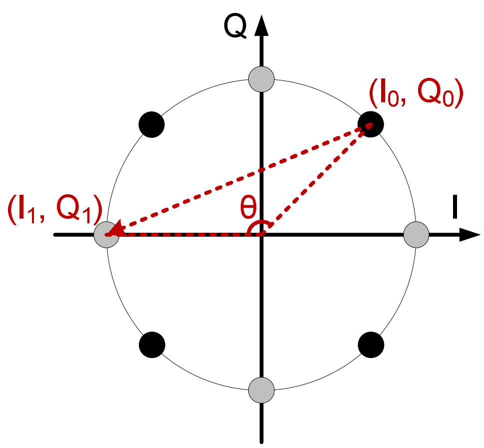


Figure 3.20: Frequency response of the 33rd-order FIR filter

In differential phase shift keying, the information is carried by the phase shifting, θ, of two consecutive symbols, as shown in Figure 3.21. π/4-DQPSK is nicely coded so that the information bits can be demodulated from only the signs of $\cos\theta$ and $\sin\theta$.



θ	cosθ	b_{2n}	sinθ	b_{2n+1}
π/4	>0	0	>0	0
3π/4	<0	1	>0	0
-3π/4	<0	1	<0	1
-π/4	>0	0	<0	1

Figure 3.21: π/4-DQPSK constellation

According to trigonometric formula, $\cos\theta$ and $\sin\theta$ can be calculated as

$$\cos\theta = \frac{I_1 I_0 + Q_1 Q_0}{\sqrt{(I_0^2 + Q_0^2)(I_1^2 + Q_1^2)}}$$

and

$$\sin\theta = \frac{Q_1 I_0 - I_1 Q_0}{\sqrt{(I_0^2 + Q_0^2)(I_1^2 + Q_1^2)}}$$

respectively. Since the denominators in both expressions are always larger than zero, only the signs of the numerators need to be calculated, featuring low hardware complexity and power consumption.

The 600 kHz symbol clock is generated from the 4.84MHz baseband clock to avoid an extra frequency reference. A fractional-N divider is utilized in the symbol timing recovery circuit, as shown in Figure 3.22, since the baseband clock is not integer times of the symbol clock. The programmable fractional divider also ensures constant baseband clock for different RF channel frequencies.

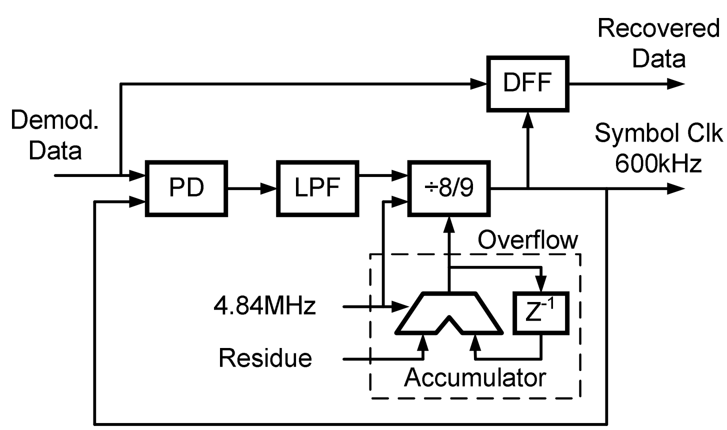


Figure 3.22: Block diagram of the symbol timing recovery circuit

3.4 Experimental Results

The proposed WBAN-compatible sub-sampling receiver is implemented in 65nm CMOS technology with a 3.4um thick metal layer for inductors. The digital-intensive architecture results in elimination of most analog circuits following the LNA. Therefore, the receiver occupies only 0.35mm^2 active area (0.3mm^2 in the LNA) as shown in the die photograph in Figure 3.23.

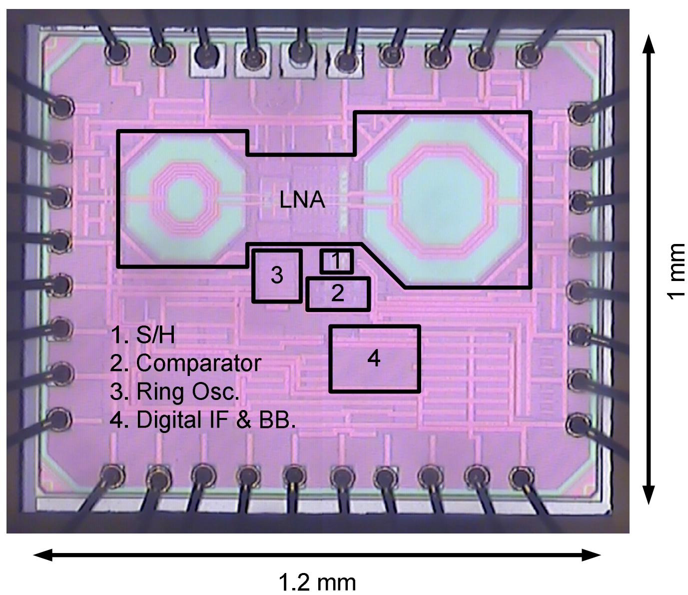


Figure 3.23: Die photo

3.4.1 Q-Enhancement LNA

With the hybrid coarse/fine tuning strategy, the LSB of the LNA output resonance frequency tuning at 2.4GHz is measured to be smaller than 0.9MHz, yielding a worst case center frequency offset of 0.45MHz, as shown in Figure 3.24. The small size in relation to the carrier frequency of 2.4GHz means that this high-Q front-end can be operated with effective Q enhanced up to 400 with only 0.1dB gain reduction and 0.5dB gain fluctuation for 1MHz channels at 2.4GHz.

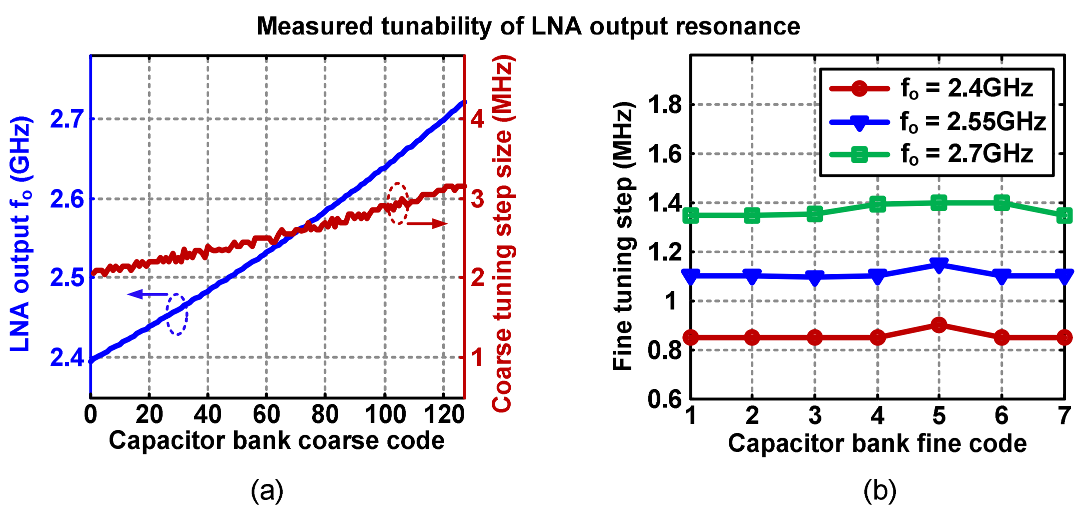


Figure 3.24: Measurement of LNA output resonance tuning with (a) coarse code and (b) find code

Figure 3.25 validates the relationship between LNA bias current and effective tank Q as described in equation (3.9). The highest measured filter Q is close to 400 and the 44-bit digital bias current tuning translates to a Q step size of about 70 in Q-enhancement operation.

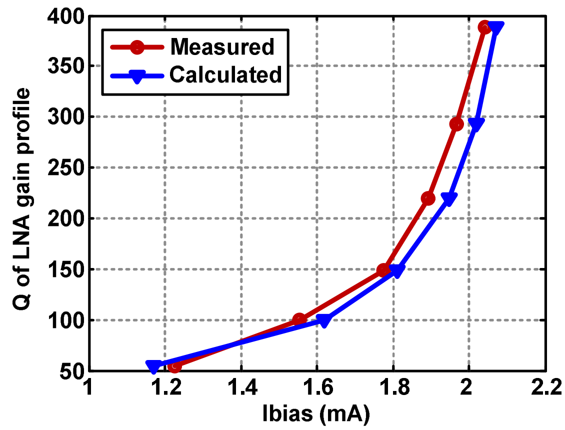


Figure 3.25: Comparison between measurement and calculation of enhanced Q and LNA bias current

In WBAN application, antenna impedance can vary due to surrounding objects, resulting in a variation in source impedance for the LNA. To examine the impact of such changes, the input S11 is measured when the LNA is tuned to different center frequencies. As shown in Figure 3.26, the input matching does not change when the resonance frequency is tuned across the entire tuning range (validating the approximation in (3.12)), allowing input matching and LNA resonance calibration to be performed independently.

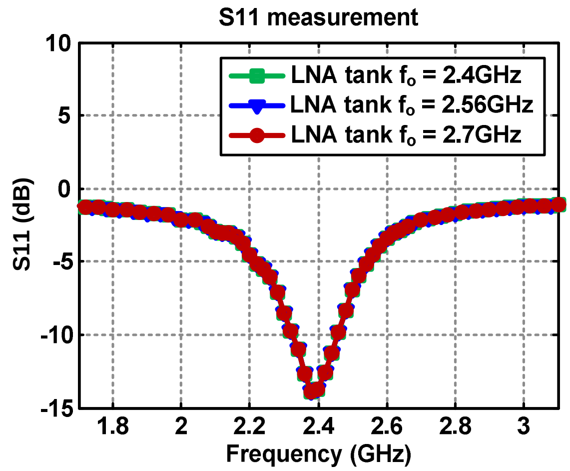


Figure 3.26: Measurement of LNA input matching

3.4.2 1-bit Quantizer

External DC voltage sources are involved in measuring the performance and on-chip calibration accuracy for the 1-bit quantizer, as shown in Figure 3.27 (a). By sweeping the differential DC input voltage of the 1-bit quantizer, a cumulative probability distribution curve is drawn based on the output of the accumulator. Figure 3.28 (a) shows an example of such measurement, in which the quantizer DC offset is calculated to be 8.9mV and the input referred noise sigma is 0.88mV.

The actual on-die offset calibration does not involve those external DC voltage source. Only the internal digital control word of the current DAC shown in Figure 3.27 (b) needs to be set to bring the possibility of ‘1’s close to 0.5. A similar cumulative curve can also be measured by sweeping the internal control word. The measurement example in Figure 3.28 (b) shows a calibration step size of 1.02mV, yielding a worst case offset residue of 0.51mV.

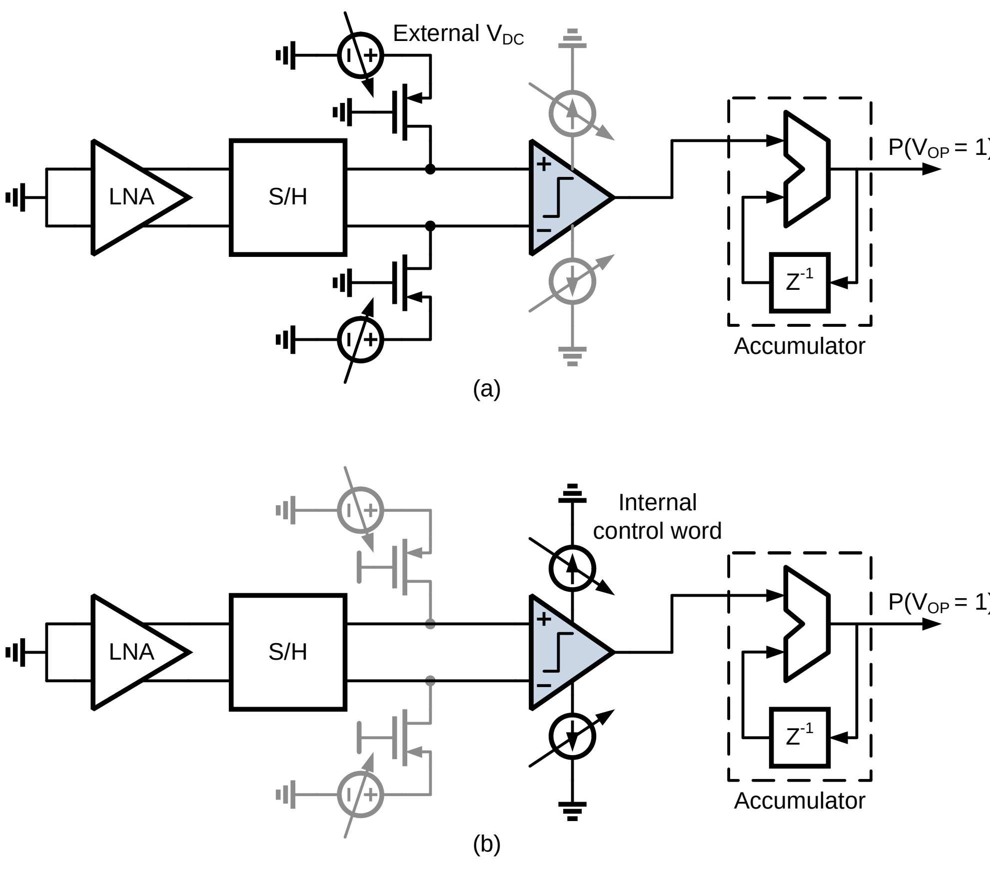


Figure 3.27: 1-bit quantizer measurement setup with (a) external voltage sources and (b) internal control words

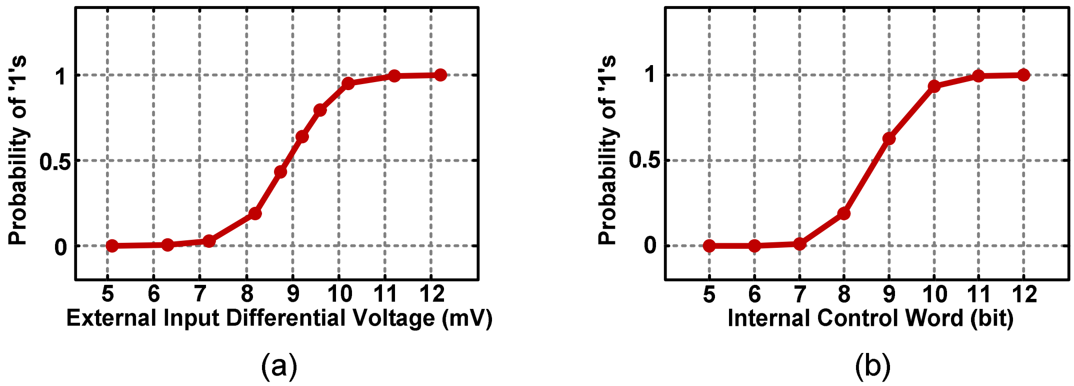


Figure 3.28: Measured quantizer output accumalative Gaussian distribution curve versus (a) external input and (b) internal control word

3.4.3 Sub-Harmonically Injection-Locked Ring Oscillator

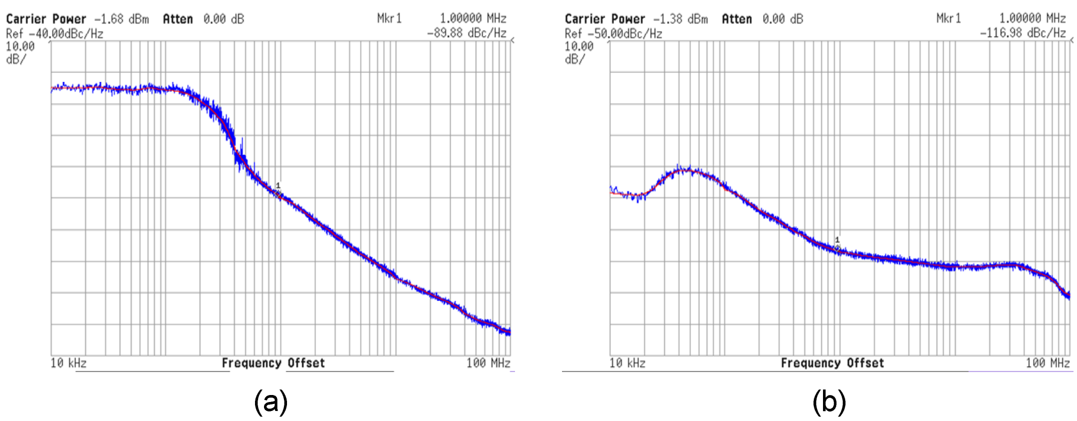


Figure 3.29: Phase noise of the ring oscillator (a) without and (b) with injection locking

As shown in Figure 3.29, when injection locked to the external frequency reference, the phase noise of the ring oscillator is improved from -90dBc/Hz at

1MHz offset to -117dBc/Hz at the same frequency offset, resulting in less than 1ps rms jitter. In the mean time, the carrier to spur ratio is measured to be 48dB as shown in Figure 3.30, which means the deterministic jitter is also ignorable.

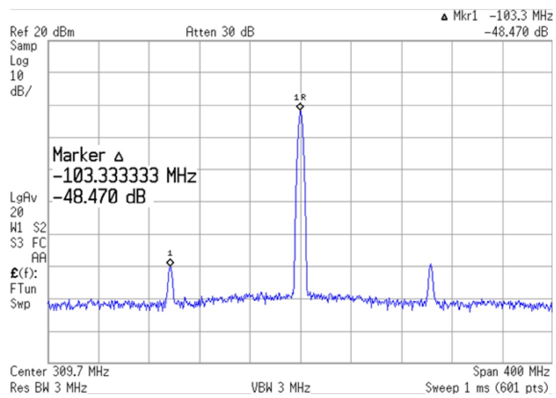


Figure 3.30: Spectrum of the injection-locked ring oscillator

3.4.4 Sensitivity

Figure 3.31 shows the set up for bit error rate (BER) measurement. An I/Q baseband waveform based on a 32767-bit PRBS is generated using MATLAB and a Tektronix 7062B arbitrary waveform generator (AWG). The AWG provides the baseband I/Q signal to an Agilent 8267D signal source that generates the I/Q modulated RF input signal for the device under test. An Agilent 16801A logic analyzer samples the demodulated data at the output and calculates BER.

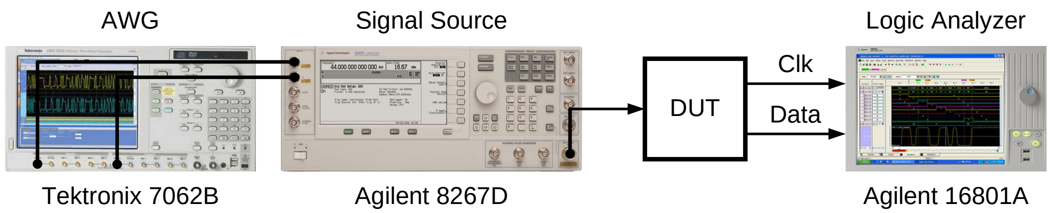


Figure 3.31: BER measurement set up

The receiver sensitivity is measured based on 10^{-3} BER for different enhanced-Q values in the LNA. As shown in Figure 3.32, sensitivities of both π/4-DQPSK and π/2-DBPSK are finally converged to -92dBm and -97dBm, respectively, as predicted in Section 3.2.1.

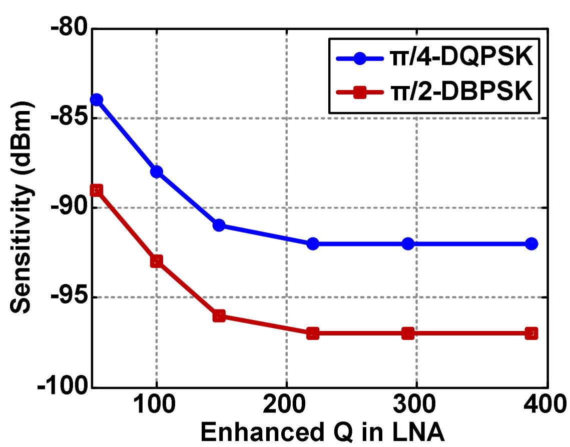


Figure 3.32: Measuremnt of sensitivity versus enhanced Q in LNA

3.4.5 Linearity

The large signal performance of the proposed sub-sampling receiver is measured by increasing the input signal amplitude to find the point where the BER drops back to 10^{-3}, which is named as "compression point" in Figure 3.33. While the enhanced Q in LNA increases from 54 to 388, the compression point decreases from -26dBm to -43dBm due to the voltage gain variation of the LNA. This feature can be used to accommodate the potential variation of the received signal dynamic range.

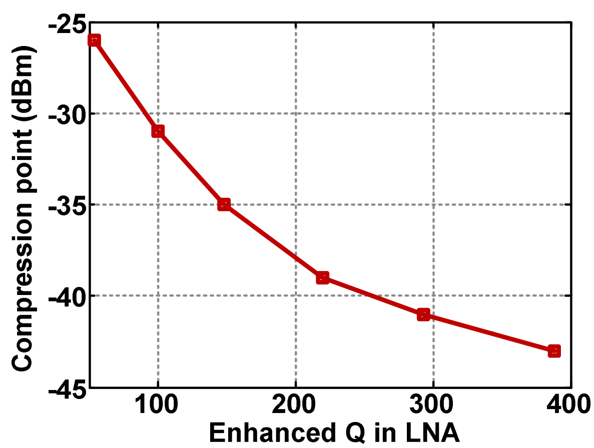


Figure 3.33: Measurement of compression point versus enhanced Q in LNA

Another Agilent 8267D signal source is added to emulate the adjacent channel signal in ACR measurement, as shown in Figure 3.34.

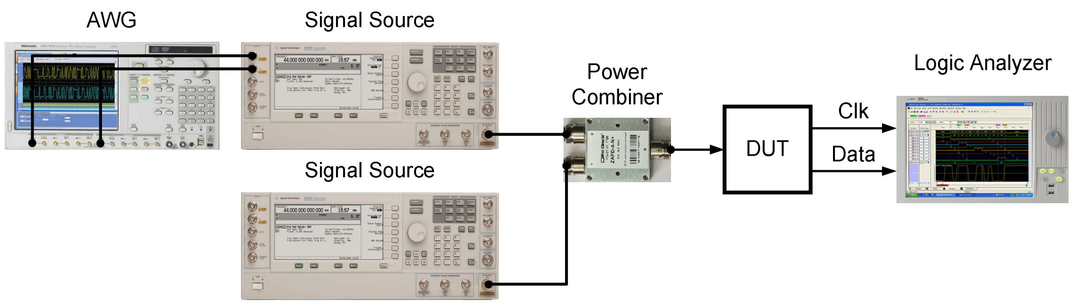


Figure 3.34: ACR measurement set up

With the sampling frequency of 309.7MHz, the ACR of DQPSK and DBPSK are measured to be 10dB and 14dB, respectively. When the sampling frequency is decreased to 157.4MHz, an expected 3dB degradation in ACR is observed, as shown in Figure 3.35, since the 2 times lower oversampling rate leads to 3dB lower linearity in oversampled A-D conversion.

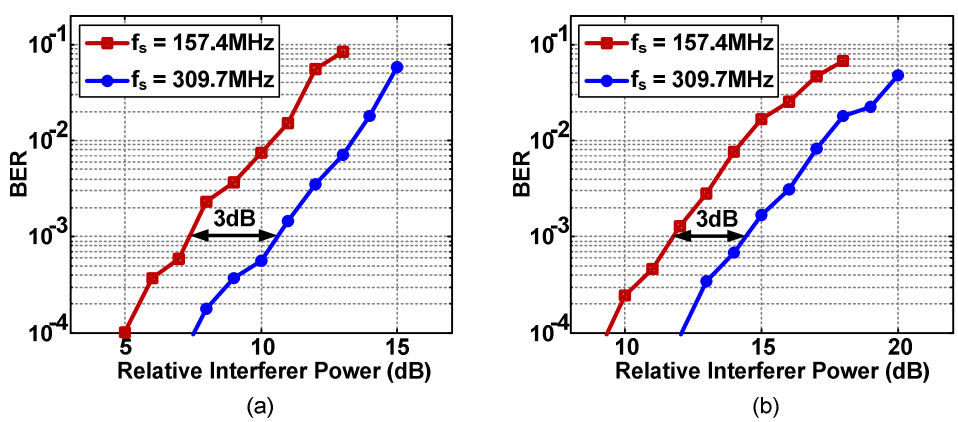


Figure 3.35: Measurement of ACR for (a) π/4-DQPSK and (b) π/2-DBPSK

3.4.6 Power Breakdown and Comparison

Figure 3.36 shows the power breakdown of this work. When compared with the prior IEEE 802.15.6 NB compatible implementation [47], this work significantly brings down the power consumption of the frequency translation and the IF stage, since sub-sampling technique and digital-intensive architecture are utilized. The overall receiver power consumption is improved 3 times.

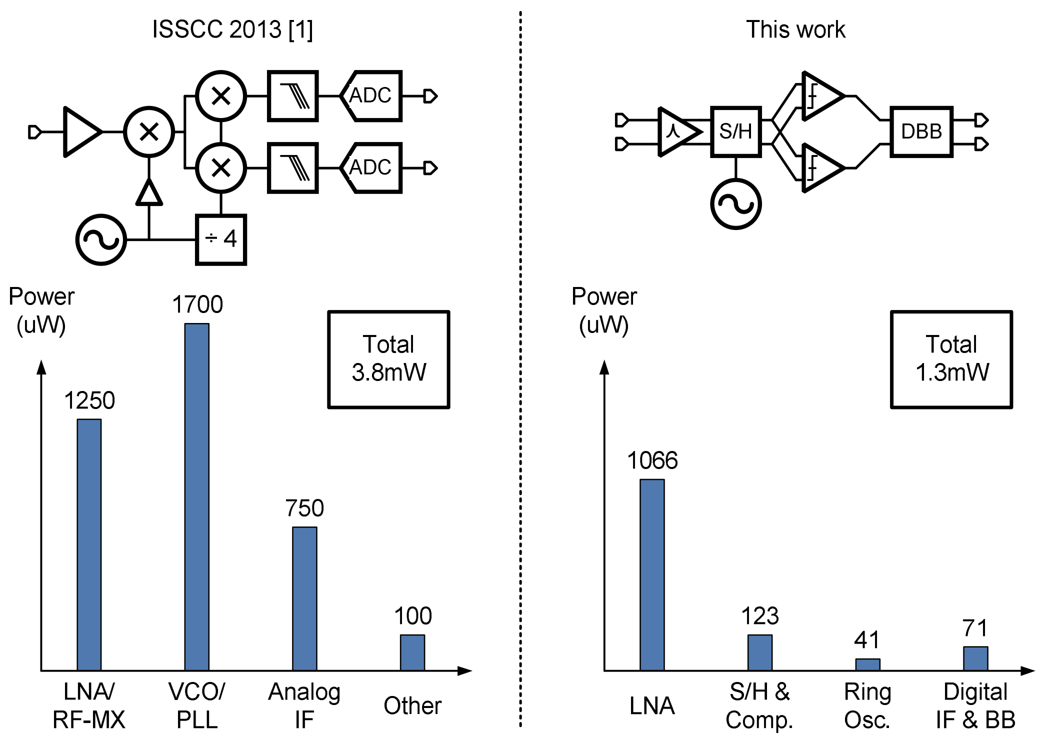


Figure 3.36: Power breakdown and comparison with prior art

3.4.7 2.7GHz Operation

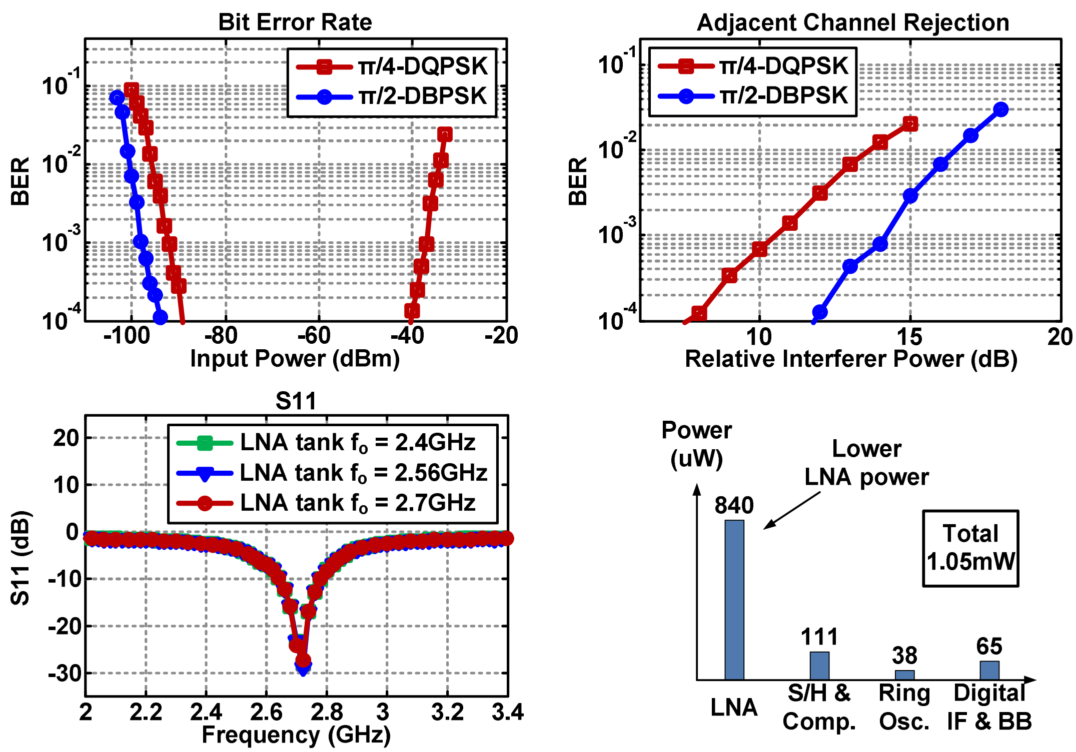


Figure 3.37: 2.7GHz operation performance summary

In measurement, the highest intrinsic Q of the passive inductor and switched capacitors was found to be at 2.7GHz. Because the bank capacitors are all switched off and the intrinsic loss is smaller, lower LNA bias current at 2.7GHz is needed as compared to 2.4GHz to obtain the same Q. We characterized the performance of the receiver with a carrier frequency of 2.7GHz as well and as can be seen the 2.7GHz operation achieves similar performance as 2.4GHz with even lower power consumption of 1.05mW, as shown in Figure 3.37. Therefore, we estimate that increasing the inductor size to increase intrinsic Q at 2.4GHz will lead to sub-mW RX power consumption.

3.5 Summary and Comparison

Table 3.3 compares the sub-sampling receiver prototype with other recently published low power 2.4GHz receivers. With noise figure and sensitivity comparable to the state of art, this work achieves 3 times lower power consumption [45]-[47] and 3 times lower energy per bit than the receiver with lower spectrum efficiency modulation (BFSK) [49], [50], [57]. Figure 3.38 shows the RX figure of merit (FOM) (defined in Table 3.3) of the proposed sub-sampling receiver and prior 2.4GHz low power receivers, demonstrating that the proposed architecture and implementation advances state-of-the-art in low-power wireless radios. Note that input referred noise $kTBF$ (k as the Boltzmann Constant, T as the Kelvin temperature, B as the system bandwidth, F as the receiver noise factor) is used here to present the noise performance of the receivers because a) some reference do not report sensitivity performance due to the lack of digital baseband and b) sensitivities are measured based on different types of error rates.

Table 3.3: Performance Summary and Comparison with Prior Arts

	JSSC 13 [45] [46]	ISSCC 13 [47]	JSSC 13 [57]	JSSC 13 [49] [50]	This work [1]	
RX architecture	Sliding IF	Sliding IF	Low IF	Low IF	Sub-sampling	
Modulation	π/2-DBPSK / π/4-DQPSK	π/4-DQPSK	BFSK	BFSK	π/2-DBPSK / π/4-DQPSK	
Data rate	121 kbps / 971 kbps	971 kbps	1 Mbps	200 kbps	486 kbps / 971 kbps	
Frequency band	2.4 GHz	2.4 GHz	2.4 GHz	2.46 GHz	2.4 GHz	2.7 GHz
Noise figure	6 dB	6 dB	6 dB	6.1 dB	6 dB	5 dB
Sensitivity	-104 dBm / -96.5 dBm (10% PER)	-96 dBm (10% PER)	-84 dBm (0.1% BER)	-91.5 dBm (0.1% BER)	-96 / -91 dBm (0.1% BER)	-97 / -92 dBm (0.1% BER)
Compr. (10^{-3} BER)	-	-	-	-	>10 / -35 dBm	>10 / -38 dBm
ACR	-	-	40 dB	-	14 / 10 dB	14 / 10 dB
Image rejection	-	35 dB	-	-	33 dB	33 dB
Active / die area	**- / 5.9 mm^2 (130nm)**	**2 / 3.7 mm^2 (90nm)**	**- / 6.25 mm^2 (130nm)**	**- / 2.5 mm^2 (65nm)**	**0.35 / 1.2 mm^2 (65nm)**	
Supply	**1 V**	**1.2 V**	**1 V**	**0.3 V**	**0.6 V**	
Power dissipation	**4.8 mW** [3]	**3.8 mW** [2]	**3.45 mW**	**1.6 mW** [2,3]	**1301 uW**	**1054 uW**
RX energy effi.	**4.9 nJ/b**	**3.9 nJ/b**	**3.45 nJ/b**	**8 nJ/b**	**1.34 nJ/b**	**1.09 nJ/b**
RX FOM [4]	**221 dB**	**222 dB**	**217 dB**	**216 dB**	**227 dB**	**228 dB**

1. Measured with a typical Q of 148
2. Power dissipation excluding digital baseband
3. Power dissipation excluding ADC / off chip drivers
4. RX FOM = - 10*log(kTBF) - 10*log(P_{DC}/Data rate), based on [1]

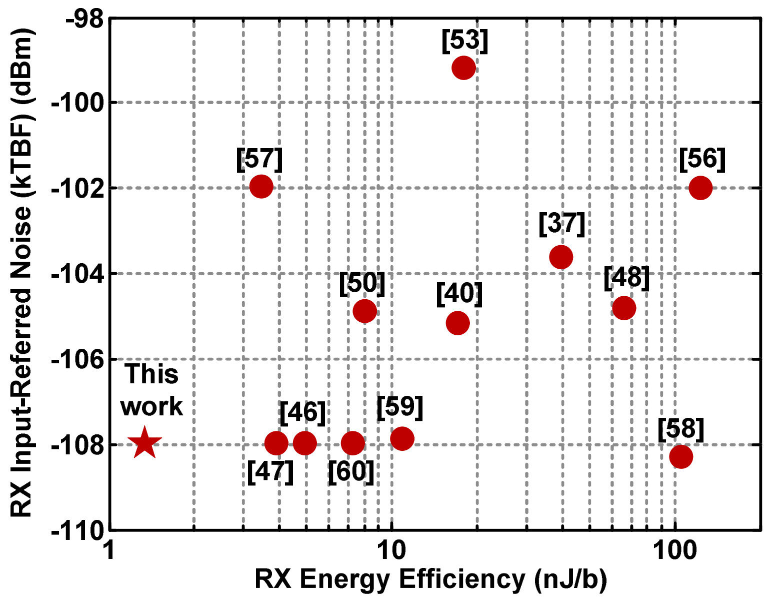


Figure 3.38: FOM comparison with prior arts

Chapter 4. Conclusion

The rapid growth of healthcare expenditure and elderly population has introduced the large demanding of ubiquitous, low-power, lower-cost biomedical sensor and actuator solutions, within which the wireless body area network plays a vital role as it provides highly reliable and convenient communication links among wearable/implantable devices and the controllers. The release of the IEEE 802.15.6 standard further normalizes the design and implementation in wireless body area network, promoting the development of related research and industry.

The power dissipation, supply voltage and the IC area are some of the most important criteria for successful WBAN implementations. The existing low power wireless receiver architectures with analog-intensive topology have demonstrated several enhancements in one or two aspects mentioned above, but none of them achieve improvements in all three features simultaneously. Digital-intensive RX architectures can potentially in sub-1V operation with significant reductions in power consumption and die area, but require system and circuit-level innovations to achieve desired sensitivity and linearity.

A PSK receiver is proposed that employs a digital-intensive architecture based on sub-sampling, Q-enhancement, early digitization and digital IF to enable low-power (1.3mW) and low-voltage (0.6V) operation. System and circuit analysis are elaborated in detail, along with simulation results. Experimental results obtained from the prototype chips are also presented to validate the proposed techniques and architectures.

Implemented in 65nm CMOS, this work fully meets IEEE 802.15.6 narrowband physical layer specification and achieves -91dBm and -96dBm for π/4-DQPSK and π/2-DBPSK modulation, respectively, for 10^{-3} BER. With comparable noise performance to the state of art, this work improves the receiver energy efficiency by at least 3 times and occupies only $0.35mm^2$ active area. The proposed techniques demonstrate the feasibility of sub-mW 2.4GHz WBAN RX in advanced CMOS technologies. These techniques are applicable to other low-power wireless standards and the digital-intensive techniques can be further extended to achieve lower power, smaller area and improved sensitivity with scaling to more advanced CMOS technologies.

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