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The problem of synchronization arises in the interaction among digital systems not sharing a common clock reference. The reliability of synchronizers is related to metastable operation of bistable elements. Because of its subtle nature, the phenomenon until recently was not widely researched. However, the literature now contains a sound theoretical basis concerning the nature of metastability and its relationship to synchronization failure. Methods exist for construction of circuits with high synchronization reliability.

This paper describes the performance of synchronizers constructed in an integrated CMOS technology. A discussion of the characteristics of CMOS circuits in metastable operation is given, with attention to various device capacitances. The effect of transient channel charging current is included. A high-performance CMOS realization is described and experimental measurements of the synchronization reliability are compared with predicted performance curves. A comparison to NMOS circuits is given.

# SYNCHRONIZATION IN A CMOS TECHNOLOGY

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Stephen T. Flannagan

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# SYNCHRONIZATION IN A CMOS TECHNOLOGY

## I. Introduction

### A. History of the Problem

Given two or more mutually asynchronous digital systems (i.e. not sharing a common clock reference) interactions among them can result in signals of non-defined logic levels. The sampling of an input while it is in the transition region can result in anomalous events in the circuit.

Sequential logic machines require that asynchronous inputs (those which may change at any time with respect to the machine clock) be processed by an input synchronizer. Otherwise, such an input may change while the machine is in transition from one state to another, in which case some machine registers may respond to the new value of the input, while others may respond to the previous value, thus resulting in a nonvalid state for the machine. Synchronizers are needed on interrupts and other similar inputs to computers, and in interlocks to mediate conflicting requests on common resources, in which an arbiter configuration is used.

Synchronization and arbitration failure relate to the event in which an undefined input causes a bistable decision element to enter a metastable state for some period of time. If such a state is not resolved before the information is required, a failure can result.

The use of bistables in synchronizers and the problem of metastable behavior resulting from asynchronous inputs was discussed in

an early paper by Catt [1]. However, until the early 1970's the problem of metastable action was not widely recognized due to its subtle nature and low probability of occurrence. In 1972 Chaney et. al. [2,3] awakened new interest in the problem and suggested that it might be responsible for a number of previously unexplained computer "crashes". The problem has been the subject of some papers [4-15] and the theory is well established. Design principles exist for construction of systems with known reliability. The probability of failure can be reduced to negligibly small values, at the cost of introducing delay elements which provide time for metastable states to resolve.

The question as to whether or not it is possible to develop a bistable completely free of metastable operation has been a subject of controversy. Some have assumed that certain circuits, such as a schmitt trigger, could "regularize" transitional levels, thereby avoiding metastable action. However Chaney [16] provided experimental evidence that this assumption is not true, and that a metastable region does exist for the circuit in question. In fact, there is considerable theoretical evidence that any device having two stable states must necessarily have a region of metastable behavior. Hurtado and Elliot [7] give an abstract proof of the inevitability of metastable operation for any bistable device. The theory is further generalized and extended by Marino [15] to include any digital system exhibiting sequential behavior.

The possibility of processing asynchronous input changes with an Asynchronous Sequential Network (ASN) combined with a device known as an inertial delay was discussed in [10] and it was con-

cluded therein that none of the types examined were free of anomalous behavior. Strom [11] has proven that reliable inertial delays and time-bounded arbiters are equally realizable. Consequently, all theoretical limitations which apply to one will also apply to the other.

In summary, there is very compelling evidence that in a synchronizer or arbiter, a region of metastable behavior must necessarily exist, notwithstanding the presence of any other special circuits interconnected with the decision elements. Therefore, the correct design strategy is not to attempt to avoid metastable action, but rather to provide means with a high probability of resolution of such states. The relationship of this probability to synchronizer reliability is reviewed in section I-D.

Equally important is the strategy whereby synchronizers are placed in systems. The nature of the signal interactions determines the locations in which synchronizers are needed, and how they are to be interfaced with the elements which they support.

## B. Noise Independence

The probability of escape from the metastable region, and hence the synchronization reliability, is not dependent on the level of noise in the circuit. A proof of noise independence is given by Couranz and Wann [6] using a Fourier Transform method. In another treatment, Kinnament and Woods [9] show that a noise signal is equally likely to move a bistable element into the metastable region as to move it away from that region, thus demonstrating noise independence of the error rate.

## C. Review of Theory and Equations Governing Metastable Action

A bistable can be applied as the decision element of either an arbiter or synchronizer. Figure 1 shows a flip-flop with two controlling inputs. (For discussion, only the flip-flop is shown. It is not intended to represent a complete synchronizer circuit.) The inputs "A" and "B" may change at any time with respect to each other, as shown in figure 2. In an arbiter, "A" and "B" originate from two asynchronous and conflicting commands entering a system, and in the case of nearly simultaneous requests the problem is to determine which of the signals occurred first. In a synchronizer, "B" is considered to be a machine clock which marks the validity of the asynchronous input "A", and the problem is to determine whether "A" is high or low. Thus, the proximity of the two signals can be regarded in terms of their time separation $\delta$ or in terms of the differential voltage $\Delta V$, both of which may be arbitrarily small or negative (figure 2). In this context, the problems of synchronization and of arbitration are equivalent. A component which contains an input synchronizer is referred to as "asynchronous" because it is capable of dealing with asynchronous inputs.

The event of interest is the transition of both inputs within some very small interval, such that the flip-flop will enter a metastable condition. Such a state will resolve within a finite time $\tau$ as shown in figure 3. Smaller values of $\delta$ will result in

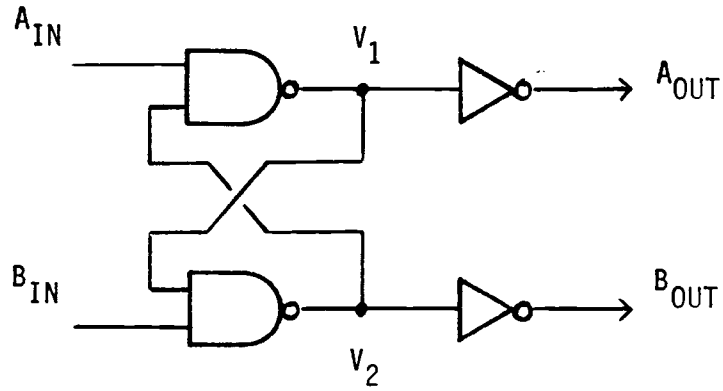


Figure 1 Flip-flop with asynchronous inputs

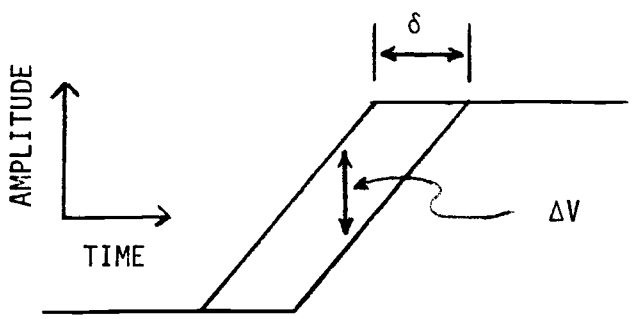


Figure 2 Proximity of inputs "A" and "B" can be defined in terms of time separation or voltage difference, both of which may be arbitrarily small.

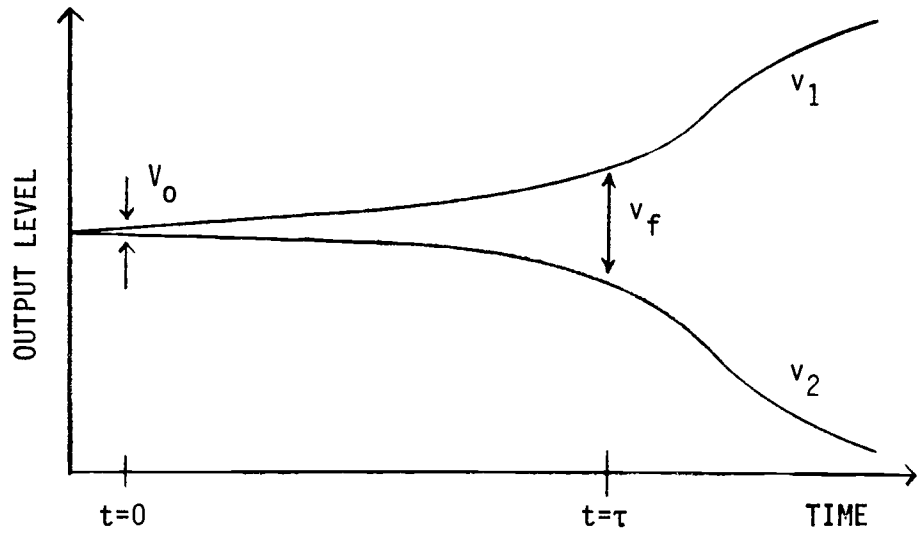


Figure 3 Metastable decay

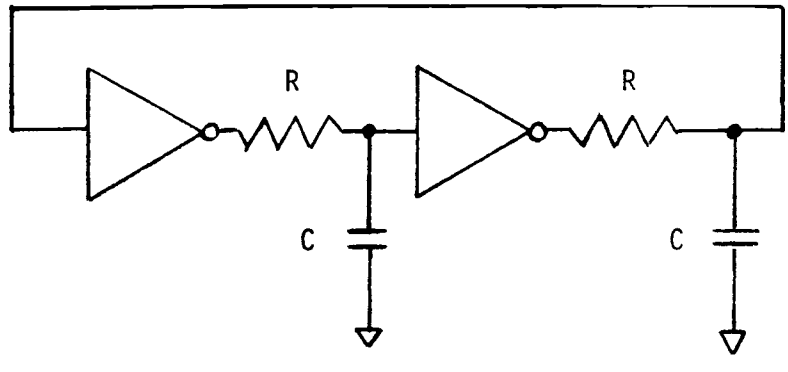


Figure 4 Simple flip-flop model

smaller initial offset $V_o$ and hence longer resolution time. A typical circuit model for a flip-flop is shown in figure 4.

In the following discussion, the variables $x_1$ and $x_2$ represent the voltage displacements from the metastable level $V_{MS}$, so that $v_1$ and $v_2$ represent the actual voltages at the nodes.

A generalized nonlinear gain can be given as

$$(1) \qquad V_{out} = A_1 V_{in} + A_2 V_{in}^2 + A_3 V_{in}^3$$

Methods of dealing with nonlinear systems are discussed, for example, in reference [17]. Figure 5 shows a phase plane trajectory for one of the flip-flop outputs x. This trajectory reflects the fact that the rate-of-change of the output increases with the output level, until the flip-flop approaches one of its stable states, when the rate of change returns to zero. (Actually the stable state is never reached but is approached asymptotically.)

The region we are interested in is the portion of the trajectory near the origin in figure 5. For circuits in which a linear approximation is valid, in the metastable region, the following equations can be written:

$$(2) \qquad \dot{x}_1 = \frac{1}{RC} (-Ax_2 - x_1)$$

$$(3) \qquad \dot{x}_2 = \frac{1}{RC} (-Ax_1 - x_2)$$

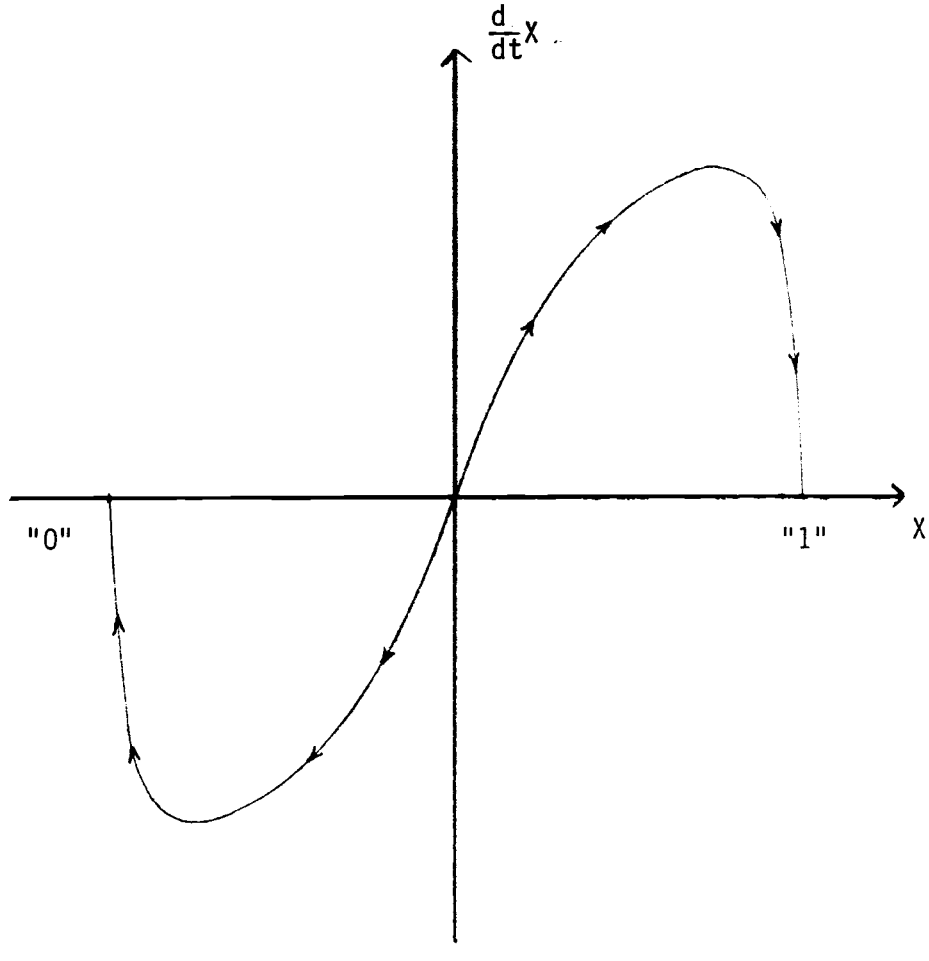


Figure 5

Typical phase trajectory for one of the outputs of a flip-flop. The variable $x$ represents the displacement of the voltage from the metastable level, so that $x(t) = v(t)-v_{ms}$. Thus, metastable operation is associated with the origin. The applicability of the linear model depends upon the approximation of the phase trajectory as a straight line near the origin.

the full solution is given by

$$x_1 = K_1 e^{\frac{1}{RC}(A-1)t} + K_2 e^{\frac{-1}{RC}(A+1)t} \quad (4)$$

$$x_2 = -K_1 e^{\frac{1}{RC}(A-1)t} + K_2 e^{\frac{-1}{RC}(A+1)t} \quad (5)$$

the variable of interest is the differential offset $v$ given by:

$$v = v_1 - v_2 = x_1 - x_2 \quad (6)$$

so that the equation for $v(t)$ can be determined as

$$v(t) = 2K_1 e^{\frac{1}{RC}(A-1)t} \quad (7)$$

Clearly, the initial offset is $V_o = 2 K_1$ . Since $A >> 1$ we approximate $A-1$ simply as $A$. The factor $A/RC$ is interpreted as the closed-loop gain-bandwidth product for the circuit, and may be written as $A\omega$ . Therefore we have

$$v(t) = v_o e^{A\omega t} \quad (8)$$

Justification of the linear model for the circuits to be discussed in this paper will be given in section II-B.

A metastable state can be induced by full-level transitions occurring nearly at the same time, or by a single input with insufficient level or duration. These two possibilities are shown in figure 6. The state variables are the flip-flop outputs $v_1$ and $v_2$ . Metastable operation is associated with a trajectory located within some small vicinity of the 45-degree line. The resolution time increases as the distance from this line to the locus of operation decreases. Figure 6-a represents the system response to

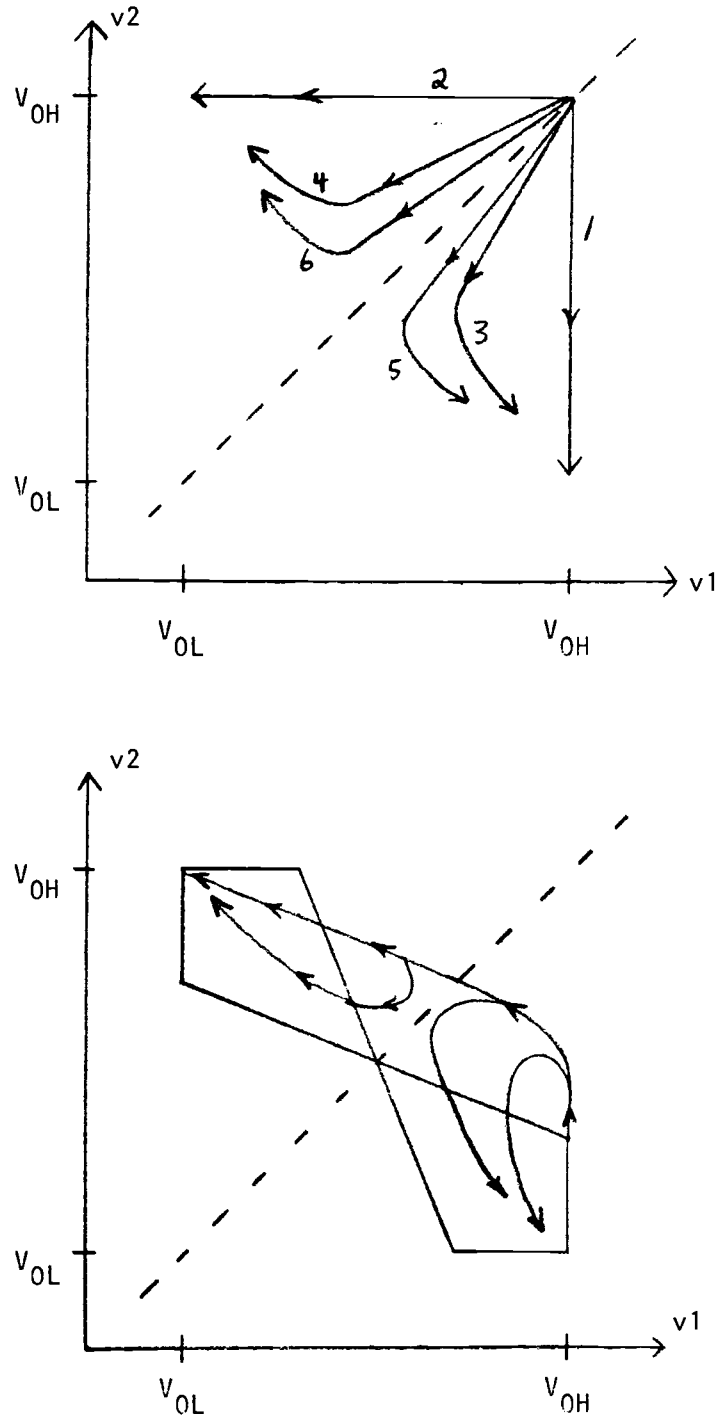


Figure 6 Flip-flop response to (a) nearly simultaneous transitions on both inputs, and (b) a pulse on one input, with insufficient duration.

nearly simultaneous transitions on inputs "A" and "B" in which neither signal returns to its original state before the response of the flip-flop has settled. Paths #1 and #2 represent the response to a transition on a single input. Paths #3 - #6 show the response to inputs on both "A" and "B" when their time separation is less than the response time of the circuit. In such an event, metastable operation near the midline is possible. Figure 6-b shows the system response to a pulse on one input whose duration is shorter than the flip-flop transition time. This type of a non-standard input can generate a metastable state even if only one input is active.

### D. Probability of Synchronization Failure

By definition, successful arbitration or synchronization consists in the choice of exactly one of two conflicting possibilities within some specified time requirement. A failure then would result in the selection of both actions, or neither action within the required time interval. Neither choice by itself can be classified as the "right" or "wrong" action in terms of the state of any other part of the system nor its inputs.

The recognized method for ensuring acceptable synchronization reliability is to provide a very high-gain flip-flop and to isolate the element during some fixed time delay. Approaches using variable delays have been described [8,12]. One technique for providing such a variable delay is the use of a flip-flop combined with level detectors, [2,9] called an indicating flip-flop in [9]. The variable delay method, however, is subject to the same basic

constraint, i.e., that the resolution time of a flip-flop is nonzero and is unbounded. This paper will deal only with the fixed-delay approach.

Figure 7 shows a typical logic configuration for a time-bounded synchronizer. $\phi_1$ is a system clock which determines the validity of the input "A". A necessary condition is that the asynchronous inputs be isolated from the flip-flop at the beginning of the interval. This requirement is important because behavior of the flip-flop must be independent of input changes subsequent to the transition of $\phi_1$.

Transitions on "A" may occur at any time with respect to $\phi_1$. Thus, the probability distribution of $\delta$ is uniform in the region of interest, so that arbitrarily small values of flip-flop offset may occur. A failure is defined as a trajectory persisting in the metastable region for a time longer than the interval $\Delta T$, so that the probability of failure in any one event is:

$$P_f = P(\tau > \Delta t) \tag{9}$$

From equation 8 the time required for resolution $\tau$ is:

$$\tau = (\ln \frac{v_f}{v_o})(\frac{1}{A\omega}) \tag{10}$$

where $v_f$ is the minimum signal required for a meaningful output. The probability of failure is then

$$P_f = P(V_o < v_f e^{-A\omega\Delta t}) \tag{11}$$

so that a minimum required input signal can be calculated as:

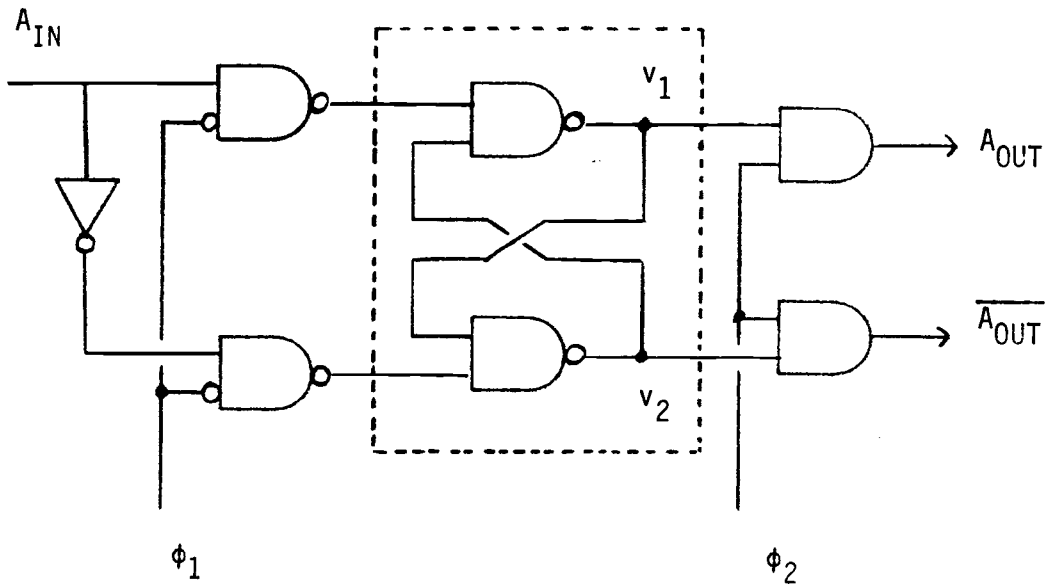


Figure 7 Conceptual logic configuration for synchronizer. Delay from clock $\phi_1$ to $\phi_2$ is fixed. Input $A_{IN}$ is asynchronous. The elements enclosed by dotted line form a flip-flop which may enter a metastable (balanced) condition at the time of phase 1. Synchronization failure can occur if this condition is not resolved at the time of the transition on phase 2.

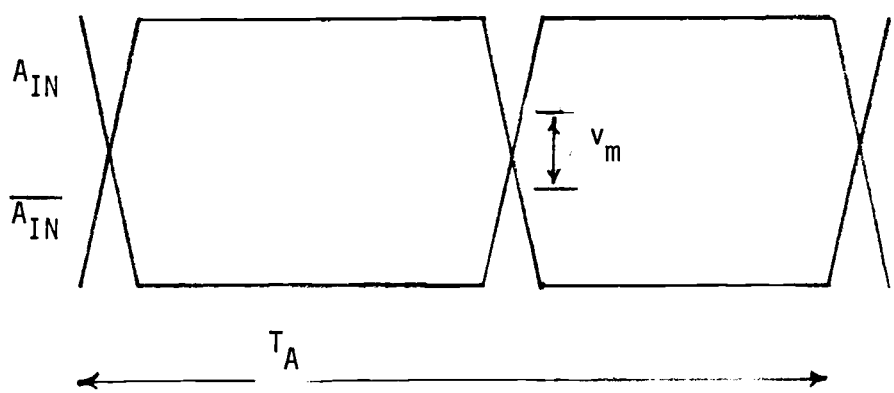


Figure 8 Characteristics of input. $T_A$ may vary from one cycle to another. $v_m$ is shown exaggerated for clarity.

(12) $$v_m = v_f \, e^{-A\omega\Delta t}$$

Values of $V_o$ greater than $v_m$ are then required for successful resolution. In these equations it is clear that the probability of failure must necessarily be nonzero. There are several treatments of this probability, for example [4,6,9,14]. Following the analysis of [9], the probability of failure is

(13) $$P_f = \frac{2}{T_A A\omega} e^{-A\omega\Delta t}$$

the error rate per unit time is

(14) $$R_E = P_f \, f_B$$

thus the error rate can be expressed as

(15) $$R_E = \frac{2 f_A f_B}{A\omega} e^{-A\omega\Delta t}$$

Where $T_A$ is the average period of the asynchronous input, $f_B$ is the system sampling frequency, and $f_A$ is defined as $1/T_A$ .

In equation 15, the factor $(2f_A f_B) / (A\omega)$ gives a measure of the probability of a metastable state being generated. The exponent relates to the probability that a metastable state will not be successfully resolved. The error rate is the product of these two factors.

This equation shows that the critical factor governing the reliability is $A\omega\Delta T$ . Figure 9 shows the theoretical error rate vs $\Delta T$ for a given value of $A\omega$ . This curve indicates that an increase in the gain-bandwidth product will allow a proportionate

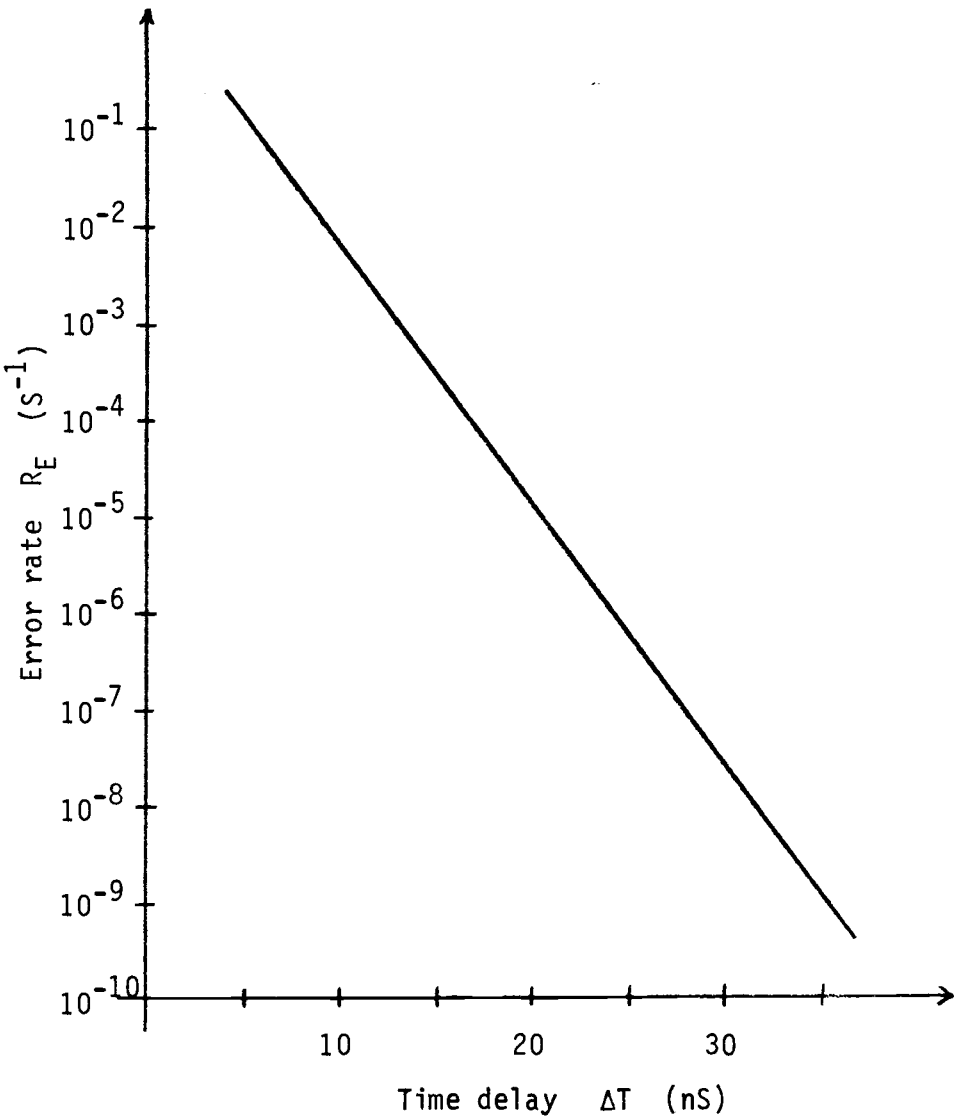


Figure 9

Example of synchronization error rate vs time delay

decrease in the delay required, thus increasing the overall system speed without altering the reliability.

An offset or inherent asymmetry in the flip-flop will not remove the possibility of metastable states. Such an imbalance would shift the relative positions of inputs "A" and "B" required to produce a metastable condition. The validity of this fact is a special case of the previously cited evidence that all bistable devices must necessarily have a region of metastability.

As an example of synchronization reliability, we consider a 1.0 MHz system clock in which an asynchronous input occurs once per second. Suppose the value of $A\omega$ is $5 \times 10^8\ S^{-1}$ and an interval of 20 nS is available before a decision must be made. Then from equation 15, $R_E = 1.82 \times 10^{-7}$ corresponding to approximately one error every 64 days. However, if the average frequency of inputs were increased to $10^6$ per second, $R_E$ would become $1.82 \times 10^{-1}$ which would probably be unacceptable. If the factor $A\omega$ cannot be further increased, it would be necessary to increase $\Delta T$ in order to restore the original intended level of reliability.

Synchronization has also been treated in terms of the energy input to the device [5]. Mead and Conway [13] give an interesting analysis of the switching energy and also suggest an ultimate limit based on the probability that a flip-flop changes state due to random thermal motion of electrons.

# II. Design Considerations for CMOS Flip-Flops used as Synchronizers

An analysis of NMOS flip-flops used as synchronizers was given by Veendrick [14]. This section will examine CMOS flip-flop behavior and determine their performance in synchronizers. The design constraints for the CMOS technology will be determined, with attention to the effects of intrinsic and extrinsic capacitance. A detailed expression for capacitance will be used, and the effect of transient channel-charging current will be included. Comparisons to NMOS and passive load circuits will be made.

## A. Capacitance

The parameter $A\omega$ is proportionate to the conductance of the active elements in the circuit and is inversely related to the total effective capacitance associated with the nodes of the flip-flop. Methods of determining MOSFET capacitances are well established [18-24]. In general, treatment of the capacitances is separated into extrinsic capacitance (that associated with junctions, etc.) and intrinsic capacitance (associated with the intrinsic device, which excludes source and drain junctions.) Capacitances such as $C_{gd}$ and $C_{gb}$, because of their dependence on the operating state of the device, can be determined in the context of a model incorporating "partitioning" as in references [21,22].

Figure 10 shows a CMOS flip-flop and capacitances. The gate length (L) is assumed to be the same for all devices. The width (W) may be chosen differently for p-type and n-type devices. In the metastable region, all four devices are in saturation. Since an

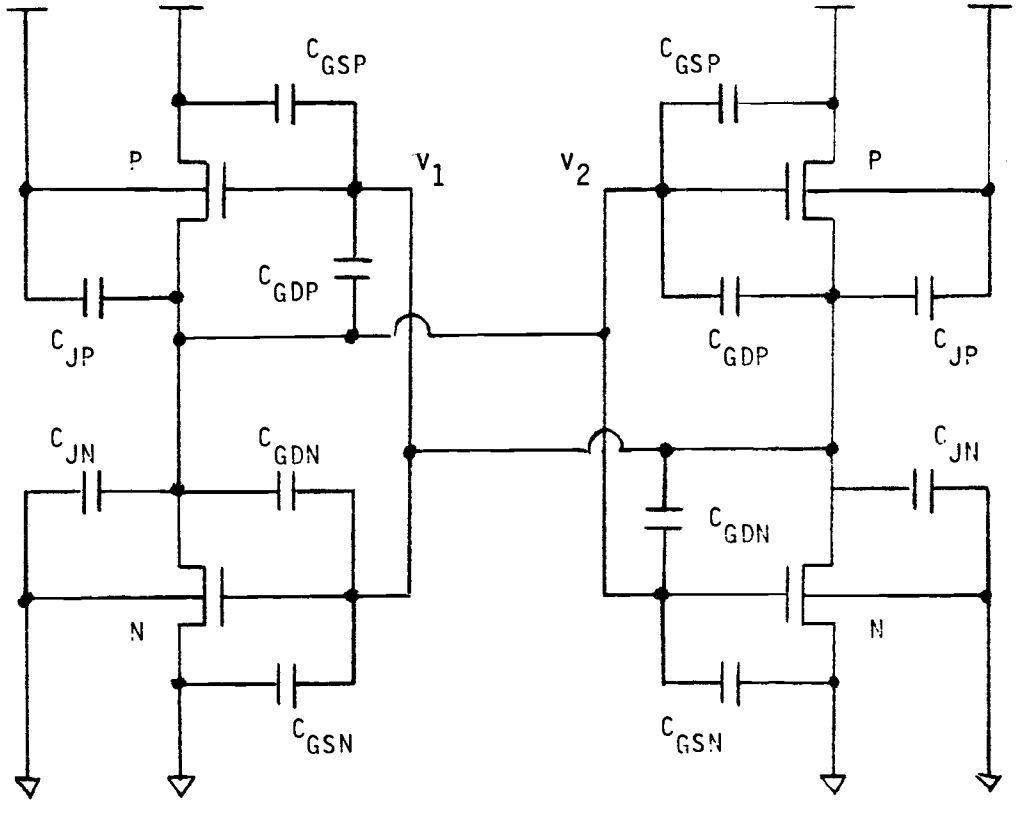


Figure 10

Capacitances associated with CMOS flip-flop. In the metastable region, all transistors are in saturation. $C_{GD}$ is negligible in both p-type and n-type transistors due to pinch-off. However, in the charging-current model a non-zero capacitance $C_{DG}$ is introduced into the circuit model in order to account for transient currents associated with variation of the channel charge.

exit from that region requires only a small change in voltages $v_1$ and $v_2$, the devices will be in saturation during the entire period of interest. In this analysis, voltage dependent parameters which do not change appreciably in this region will be treated as constant. Further, the values of channel length, mobility, and threshold used in these equations shall be those applicable in the metastable region. Because of pinch-off, $C_{gd}$ is zero in the gate-capacitance model. However, when channel charging is considered, a capacitance $C_{dg}$ can be introduced.

The gate capacitance approach to device analysis does not accurately reflect source, drain or substrate currents under transient conditions in which the channel charge is changing. Methods for analyzing MOS transient drain and source currents are discussed by Oh, Ward, and Dutton [23,24]. The total drain and source currents are expressed as a superposition of two components, a transport current and a charging current. The effects of channel-charging current are discussed in terms of non-reciprocal capacitances in reference [23]. In saturation, the drain voltage is separated from the channel by pinch-off, so that a change in $V_d$ does not affect $Q_G$, and therefore the capacitance

$$C_{gd} = \frac{\partial Q_G}{\partial V_D}$$

is zero in saturation. However, a change in gate voltage causes a change in channel charge, some of which is associated with drain current. This capacitance is given by

$$C_{dg} = \frac{\partial Q_D}{\partial V_G}$$

and can be treated as non-zero in order to account for the fact that some of the drain current is associated with the change in channel charge.

Figure 11 shows a model for the flip-flop using the simple MOS formula for saturation current. The effective nodal capacitance applicable to this model is given as:

$$C_T = C_{GSN} + C_{GSP} + C_{MIL} + C_{jN} + C_{jP} + C_{MIL2} + C_{LOAD} \quad (16)$$

where:

$C_T$ = Total effective nodal capacitance

$C_{GSN}$ = N-device gate-to-source

$C_{GSP}$ = P-device gate-to-sourve

$C_{jN}$ = Junction at drain of n-device

$C_{jP}$ = Junction at drain of p-device

$C_{MIL}$ = Miller capacitor equivalent of $C_{dg}$

$C_{MIL2}$ = Miller equivalent of overlap capacitance

$C_{LOAD}$ = Capacitance of subsequent circuit stage, interconnect parasitic and other capacitances

The following definitions of terms will be used (CMOS equations):

$$C_o = C_{ox}(L)(W_N + W_P)$$

$$a_0 = (C_{GSN} + C_{GSP}) / C_o$$

$$a_1 = C_{MIL} / C_o$$

$$a_2 = (C_{jn} + C_{jp}) / C_o$$

$$a_3 = (C_{LOAD}) / C_o$$

$$a_4 = C_{MIL2} / C_o$$

$$a = a_0+a_1+a_2+a_3+a_4$$

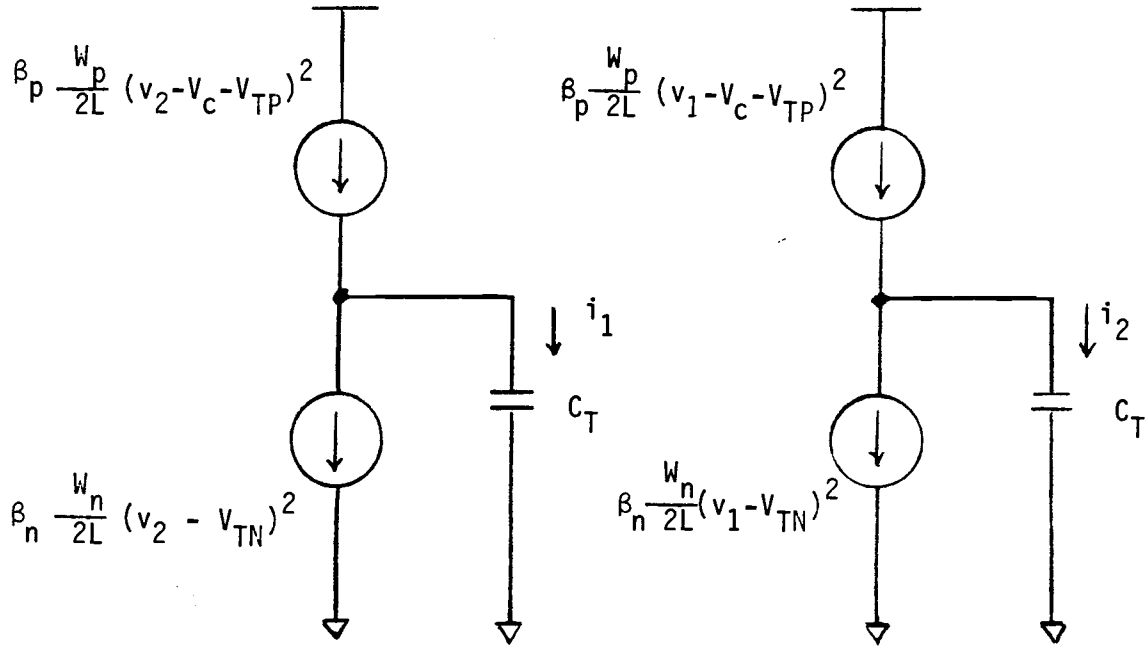


Figure 11

Circuit model for CMOS flip-flop in the metastable region of operation

so that $a_2$ and $a_3$ give a measure of the efficiency of the circuit. We then have:

$$C_T = C_0(a_0+a_1+a_2+a_3+a_4)$$

$a_2$ is relatively constant for a given technology because junction capacitance will increase roughly proportionate to device widths. $a_3$ however can be minimized by making the active devices of the flip-flop large with respect to the load elements in the subsequent circuit stages and with respect to interconnect capacitance.

In saturation, $C_{gs}/C_{ox}$ is 2/3, therefore $a_0 = 0.67$ . The analysis in [23] shows that partitioning of the channel charge in saturation is 3/8 to the drain and 5/8 to the source. Therefore,

$$C_{dg} = (3/8)(2/3)C_o.$$

Because this capacitor couples v1 and v2, it translates into the model of figure 11 as a Miller capacitor. The Miller factor is given as (1-K) where K is the ratio of the small-signal components of $v_1$ and $v_2$. For this factor we use the approximation K = -1 resulting in:

$$C_{MIL} = (1-K)(C_{dg})$$

$$C_{MIL} = (2)(3/8)(2/3)(C_o) = (0.50)(C_o)$$

Therefore, $a_1 = 0.50$ for CMOS.

The term $a_4$ accounts for the Miller capacitance associated with overlap, and is estimated at $a_4 = 0.3$ . Summarizing the above:

$$C_T = (a)C_o$$

$$a_{CMOS} = (0.67 + 0.5 + 0.3 + a_2 + a_3)$$

These parameters will be used in the calculations in sections II-D and III-B.

## B. CMOS Circuit Behavior in the Metastable Region

Referring to the simple model in figure 11 and treating the total capacitance as $C_T$ we write the equations describing $v_1$ and $v_2$ as

$$\dot{v}_1 = \frac{1}{2C_T}\left[\beta_p\frac{W_p}{L}(v_2-V_c-V_{TP})^2 - \beta_n\frac{W_n}{L}(v_2-V_{TN})^2\right] \tag{17}$$

$$\dot{v}_2 = \frac{1}{2C_T}\left[\beta_p\frac{W_p}{L}(v_1-V_c-V_{TP})^2 - \beta_n\frac{W_n}{L}(v_1-V_{TN})^2\right] \tag{18}$$

These equations can be written in the form:

$$\dot{v}_1 = -A_1 v_2^2 - A_2 v_2 - A_3 \tag{19}$$

$$\dot{v}_2 = -A_1 v_1^2 - A_2 v_1 - A_3 \tag{20}$$

where the constants are:

$$A_1 = \frac{(\mu_n W_n - \mu_p W_p)}{2L^2(W_p+W_n)(a)}$$

$$A_2 = \frac{-(\mu_n W_n 2V_{TN} - \mu_p W_p 2(V_c+V_{TP}))}{2L^2(W_p+W_n)(a)}$$

$$A_3 = \frac{(\mu_n W_n V_{TN}^2) - \mu_p W_p (V_c+V_{TP})^2}{2L^2(W_p+W_n)(a)}$$

The metastable voltage is given by

$$V_{MS} = \frac{V_c + V_{TP} + V_{TN}\sqrt{RQ}}{1 + \sqrt{RQ}} \tag{21}$$

where $R = W_N / W_P$ and $Q = \frac{\mu_N}{\mu_P}$

equations 19 and 20 are combined and written in terms of the differential offset $v = v_1 - v_2$

$$\dot{v} = \left[A_1(v_1+v_2) + A_2\right] v \tag{22}$$

The linear model can be justified if the phase trajectory is approximately linear in the region of interest. The time-variations of $v_1$ and $v_2$ are opposite in sign, and the coefficient in equation 22 will not vary substantially with time. We make the approximation

$$v_1 + v_2 \doteq 2V_{MS} \tag{23}$$

so that the linear approximation for equation 22 is then

$$\dot{v} = \left[2A_1V_{MS} + A_2\right] v \tag{24}$$

combining equations 8 and 24, the gain-bandwidth product is:

$$A\omega = 2A_1V_{MS} + A_2 \tag{25}$$

substituting the parameters previously defined, we get

$$A\omega = \frac{\mu_n W_n(V_{MS}-V_{TN}) + \mu_p W_p(V_c+V_{TP}-V_{MS})}{L^2(W_p+W_n)(a)} \tag{26}$$

The fact that the coefficients associated with each device width are positive reflects the fact that both P and N type devices contribute to gain in the circuit. In NMOS and passive-load circuits only the pull-down device coefficient would be positive.

The conditions for maximizing $A\omega$ in terms of $W_N$ and $W_P$ can be obtained by substitution of equation 21 into equation 26. After some algebra the parameters $W_N$ and $W_P$ are arranged so as to appear only in terms of the ratio R. The result is

$$A\omega = \frac{(V_c+V_{TP}-V_{TN})\sqrt{\mu_n\mu_p}}{L^2(a)} \left[\frac{\sqrt{R}}{1+R}\right] \tag{27}$$

In this first-order analysis, then, $A\omega$ will be maximized when $R = 1$. The value of $A\omega$ scales with the inverse-square of channel length. Oxide thickness does not appear in the equation, but would have an indirect effect, for example, due to its influence on threshold, unless the threshold is intentionally compensated so as not to change as the technology is scaled. Other second order effects are channel length variation, and mobility reduction associated with high vertical and lateral fields. When this effect becomes more severe, it is then necessary to use the lower value of mobility appropriate to the metastable region of operation.

The parameter $a_3$ requires that device widths in the flip-flop be sufficiently large so that $C_{LOAD}$ will be small compared with $C_O$. Beyond this point, $A\omega$ does not change substantially with device width.

A simple computer program was used to determine the variation of gain-bandwidth product with respect to device ratio and to loading. The results for the ideal case (with no load) is shown in figure 12, which gives lines of constant $A\omega$. Because of the process dependence, the graphs have been normalized. Figures 13-15 show the effects of non-zero load capacitance. The graphs give lines of constant $A\omega$, normalized globally over these graphs. $C_{LOAD}$ is given as a percentage of $C_O$ at the midpoint of each graph. These results indicate that even for small values of $C_{LOAD}$ the ratio optimization criterion breaks down. Therefore, the flip-flops must have low external capacitive loading and be well buffered if maximum performance is to be achieved. Further, a precise selection of

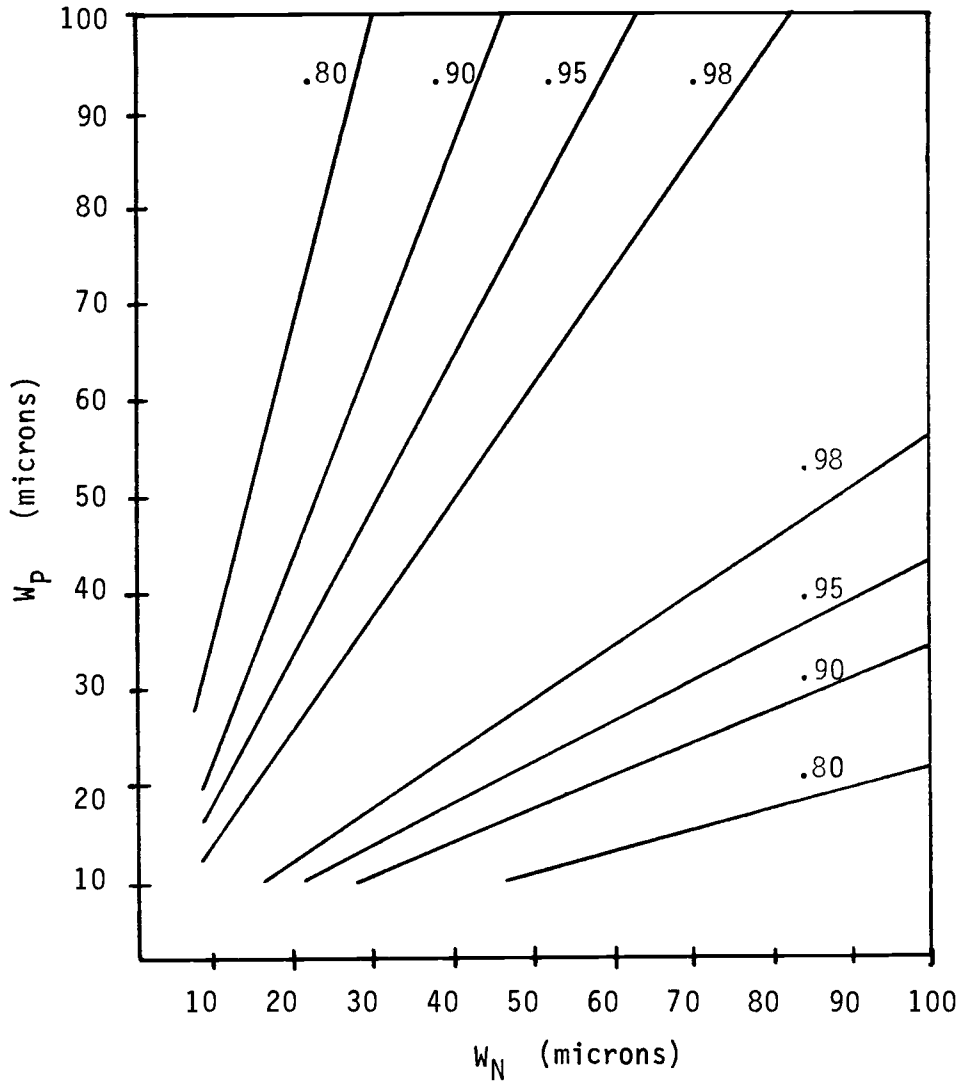


Figure 12

Loci of constant normalized $A\omega$ for the ideal case of zero external capacitance

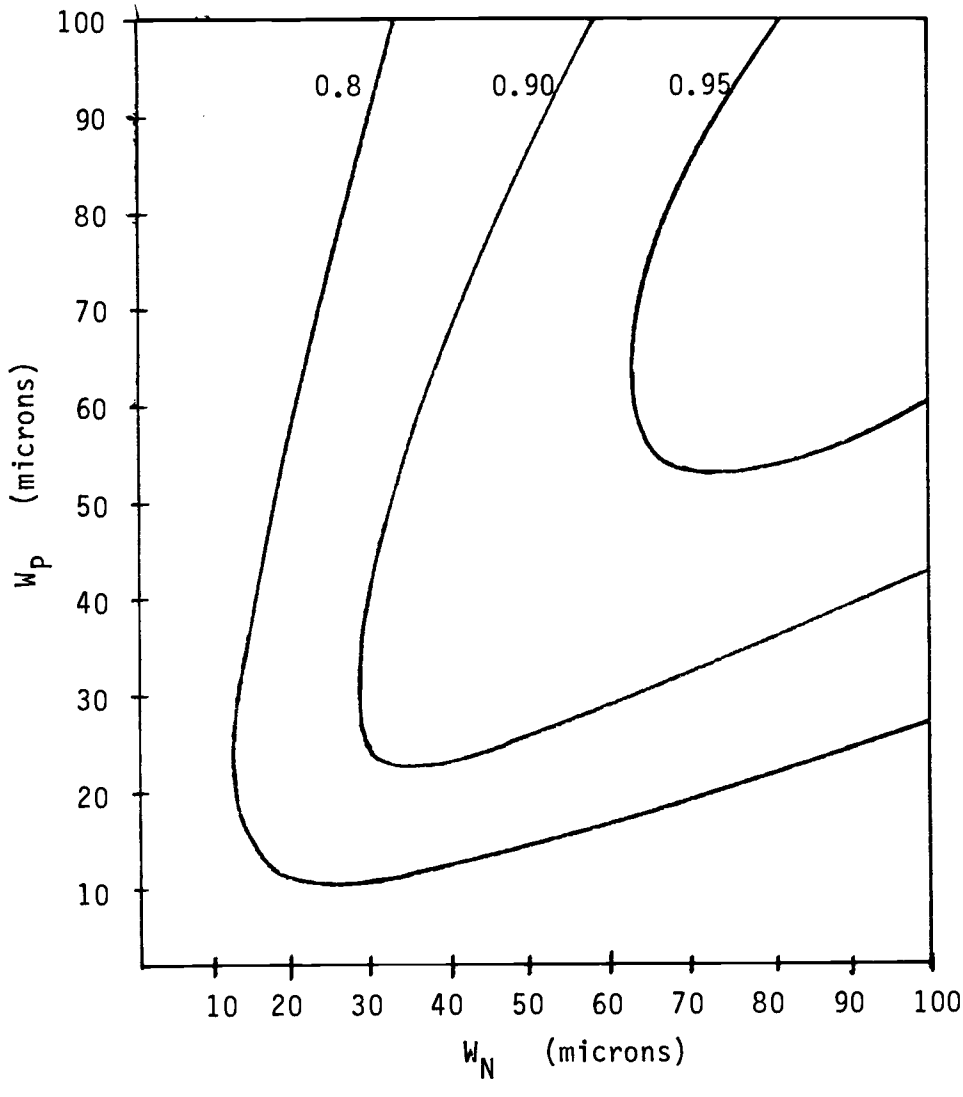


Figure 13

Lines of constant Aω for $C_{LOAD}$ of 3.0 % of the internal capacitance at midpoint of the graph.

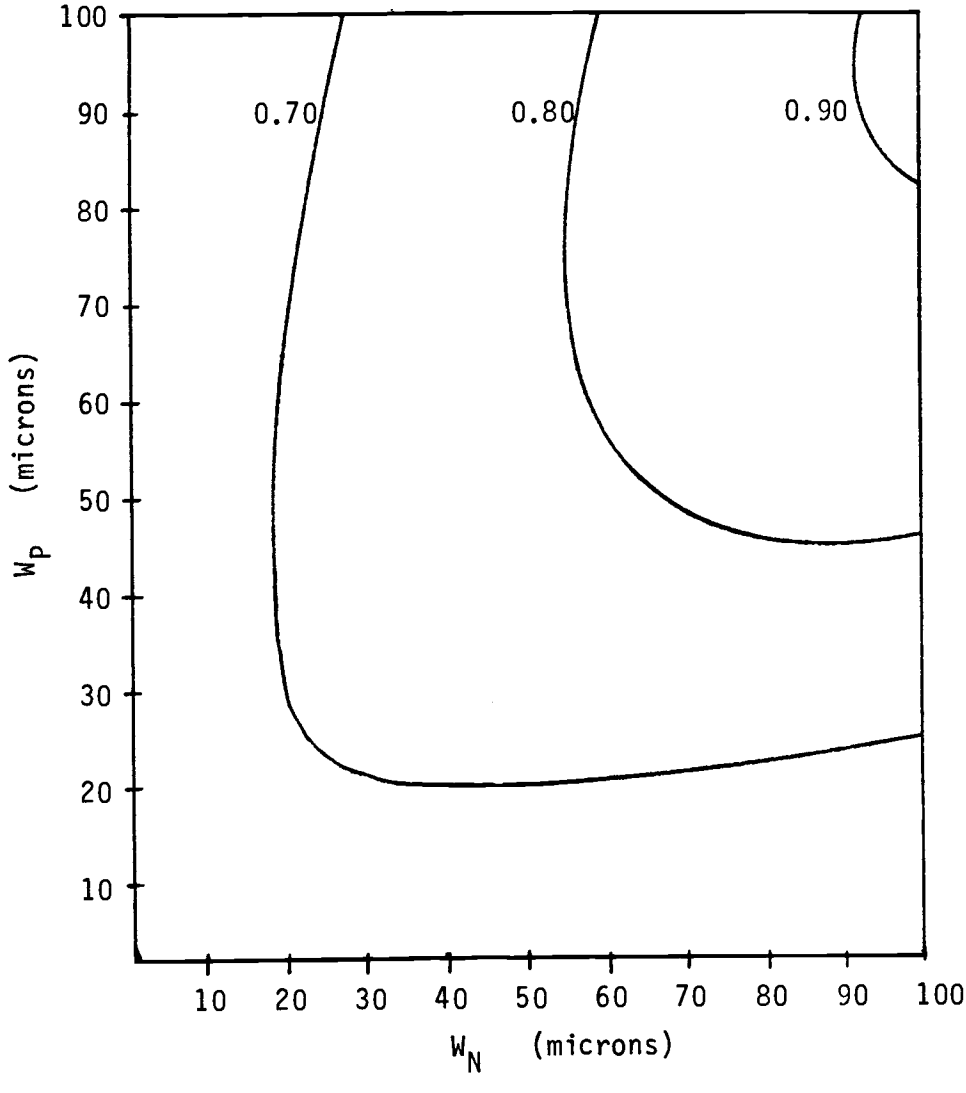


Figure 14

Lines of constant Aω for $C_{LOAD}$ of 10.0 %

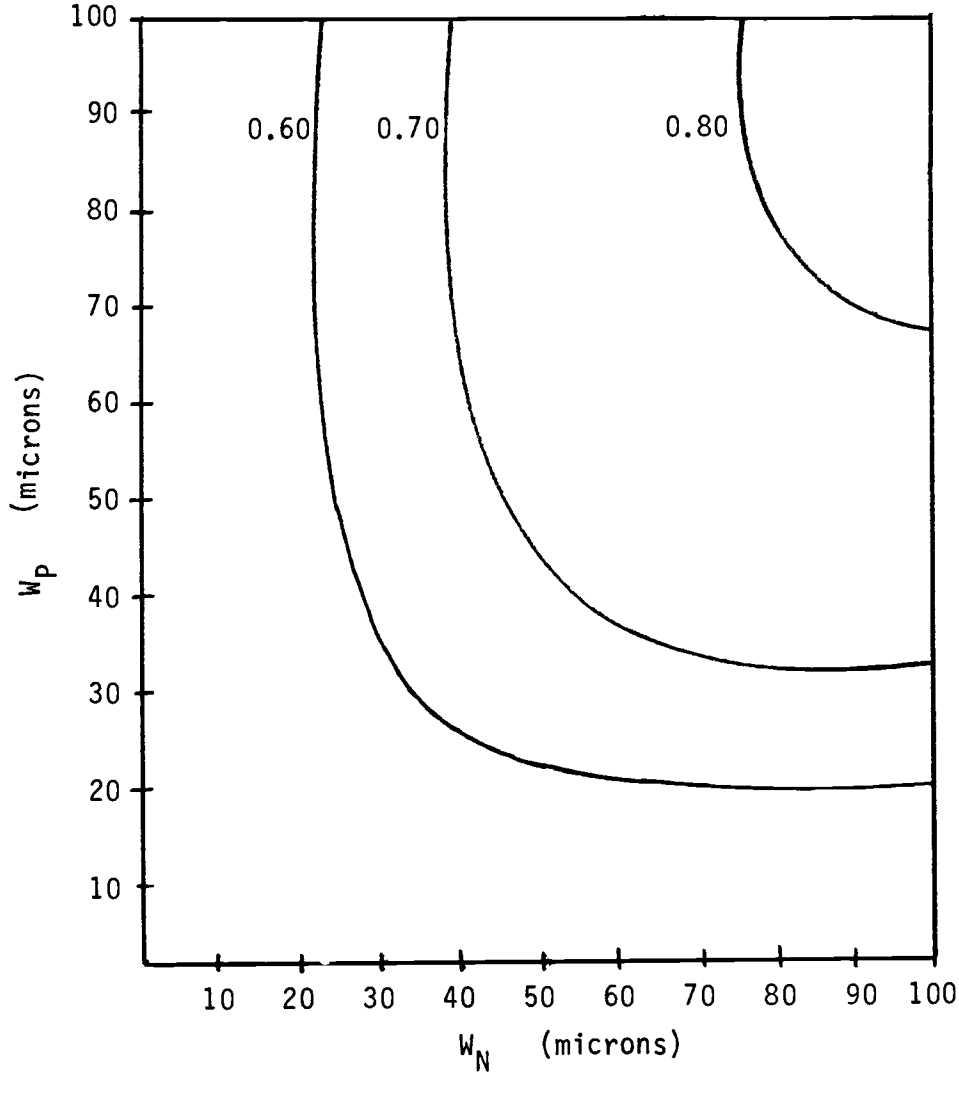


Figure 15

Lines of constant Aω for $C_{LOAD}$ of 20.0 %

device ratio R is not critical, as the regions of 90 percent efficiency are wide.

## C. NMOS Circuit Behavior in the Metastable Region

The nature of NMOS flip-flops is such that their load devices do not provide gain, but they do add nodal capacitance which tends to reduce $A\omega$ . Figure 16 shows a depletion-load flip-flop, and figure 17 shows the corresponding enhancement-load circuit. Depletion loads of course are superior because they provide a full supply-voltage level without capacitive boosting techniques, in circuits where full-level transitions are important. In the metastable region they are preferred because of gain. Enhancement loads cause a reduction in gain because of the negative feedback which they introduce into the closed-loop gain for the circuit.

Referring to figure 18 and applying the same assumptions as before, the NMOS equations are:

$$\dot{v}_2 = \frac{\beta}{2C_T}\left[\frac{W_2}{L}(V_c - v_2 - V_{TN})^2 - \frac{W_1}{L}(v_1 - V_{TN})^2\right] \tag{28}$$

$$\dot{v}_1 = \frac{\beta}{2C_T}\left[\frac{W_2}{L}(V_c - v_1 - V_{TN})^2 - \frac{W_1}{L}(v_2 - V_{TN})^2\right] \tag{29}$$

$$V_{MS(NMOS)} = \frac{V_c + V_{TN}(\sqrt{B}-1)}{\sqrt{B}+1} \tag{30}$$

$$A\omega_{(NMOS)} = \frac{\mu_n W_2(V_{MS(NMOS)} + V_{TN} - V_c) + \mu_n W_1(V_{MS(NMOS)} - V_{TN})}{L^2(W_2+W_1)(a)} \tag{31}$$

where for NMOS circuits the parameters are defined as:

$$C_T = C_{GS1} + C_{GS2} + C_j + C_{MIL} + C_{MIL2} + C_{LOAD}$$

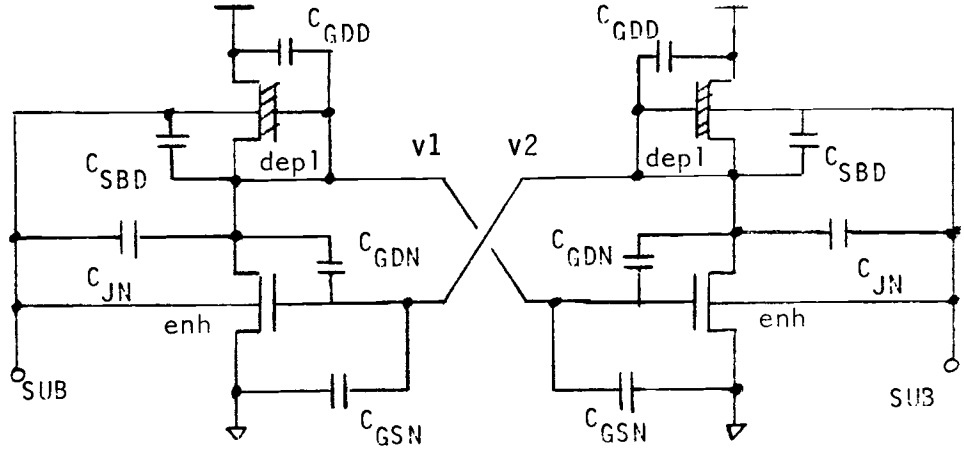


Figure 16

Depletion load flip-flop

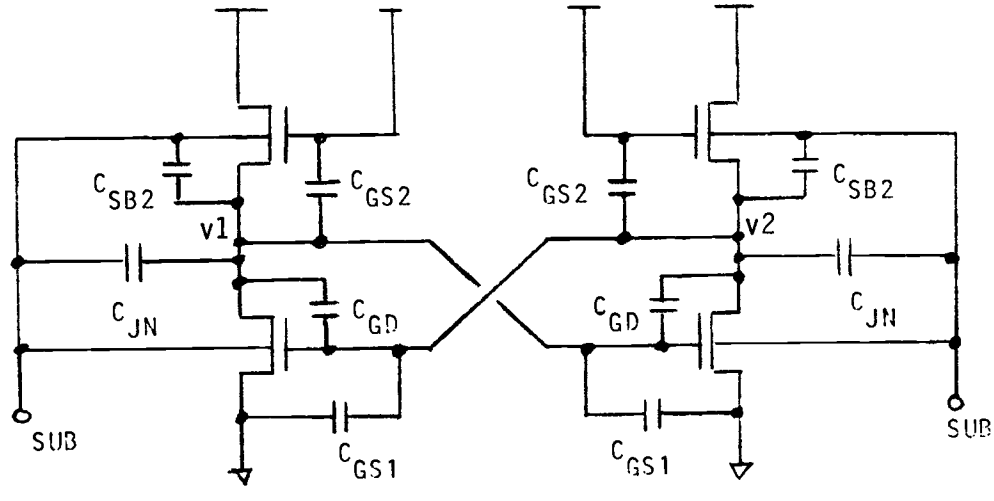


Figure 17

Enhancement load flip-flop.

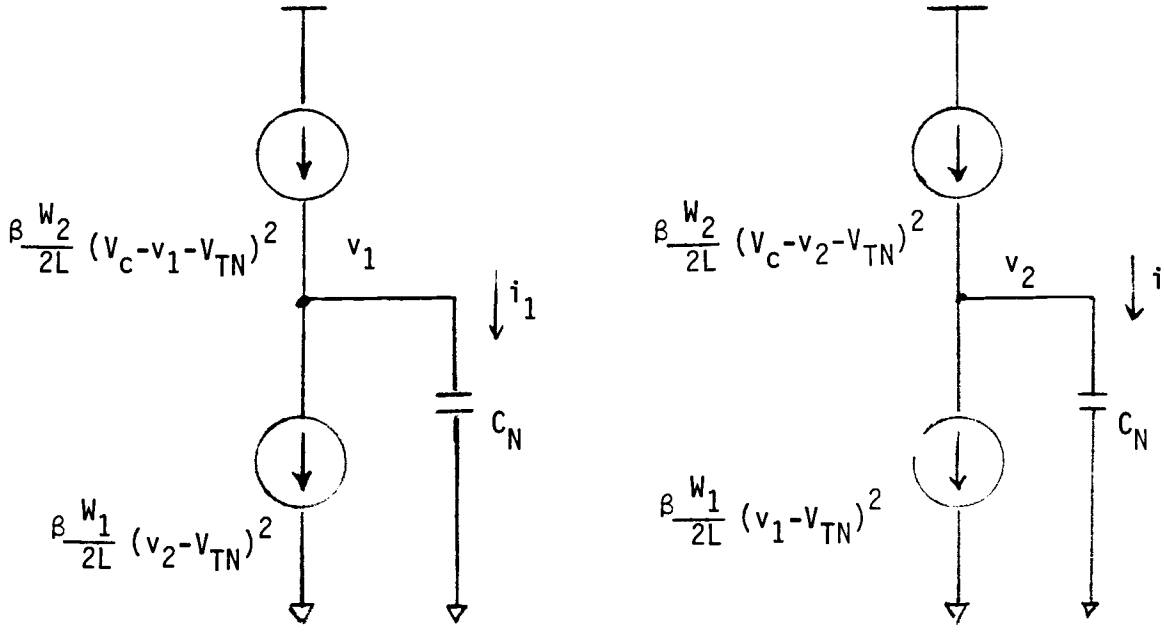


Figure 18

Circuit model for NMOS flip-flop in the metastable region. Enhancement loads are indicated here. The model for a depletion load flip-flop would substitute constant-current sources for the pull-up devices.

$C_T = C_o(a_0+a_1+a_2+a_3+a_4)$

$W_2$ = width of pull-up device

$W_1$ = width of pull-down device

$C_o = C_{ox}(W_1+W_2)(L)$

$C_{MIL}$ = Miller equivalent of $C_{dg}$

$C_{MIL2}$ = Miller equivalent of overlap

$a_0 = (C_{GS1} + C_{GS2})/C_o$

$a_1 = C_{MIL} / C_o$

$a_2 = C_j / C_o$

$a_3 = C_{LOAD} / C_o$

$a_4 = C_{MIL2} / C_o$

$B = W_1 / W_2$

The value of $a_1$ for the NMOS circuit depends on $C_{dg}$ for the pull-down device and can be approximated as a constant at the optimum value of B, later shown to be B=8. Thus, $a_1$ for NMOS is (2)(3/8)(2/3)(8/(1+8)) or 0.45 . Therefore we have, for NMOS,

$$C_T = (a)C_o$$

$$a_{NMOS} = (0.67 + 0.45 + 0.3 + a_2 + a_3)$$

Proceeding as before, the optimization equation is obtained:

$$(32) \qquad A\omega_{(NMOS)} = \frac{\mu_n(V_c-2V_{TN})}{L^2(a)} \left[ \frac{\sqrt{B}}{B+1} \cdot \frac{\sqrt{B}-1}{\sqrt{B}+1} \right]$$

Equation 32 differs from the result reported in reference [14]. The magnitude includes a more complete expression for capacitance. The maximizing factor (in square brackets) differs due to the inclusion of the capacitance $C_{GS2}$ from figure 17. We expect that the maximum of $A\omega$ and the minimum metastable state duration should both occur at the same value of B. The analysis given in [14] noted some

disagreement between these two extremes. Figure 19 shows that when equation 32 is applied, a better agreement between these two extremes is obtained.

## D. CMOS and NMOS Circuit Performance

A comparison can be made between equations 27 and 32 which give $A\omega$ for CMOS and NMOS circuits, respectively. The NMOS equation contains $\mu_n$ where the CMOS equation has $\sqrt{\mu_n \mu_p}$ . The mobility ratio $\mu_p / \mu_n$ is typically less than 0.3, but as electron mobility decreases, the ratio increases. Further, as channel length L is decreased the ratio also increases, as described by K. Yu. et. al. [25]. The transistors are operating in the saturation region.

Circuit simulations were performed to determine the variation of $A\omega$ with device ratio for CMOS and NMOS circuits. The simulator used is a highly complex model which incorporates various higher-order effects such as those affecting channel length, mobility reduction, channel charge, etc. The device size ratio B was varied with different values of $W_1$ and $W_2$ while maintaining a constant total $(W_1 + W_2) = 100$. A 20 percent capacitive load was used ($a_2+a_3 = 0.2$). Substrate bias was zero. The circuit parameters were:

$V_C = 5$ v $\qquad V_{TD} = -2.5$ v
$V_{TN} = 0.8$ v $\qquad L = 2.5$ μm
$V_{TP} = -0.8$ v $\qquad a_2+a_3 = 0.2$

Simulated curves of $A\omega$ were determined by applying equation 8 to the simulated decay of a metastable state. The results are plotted in figure 20, for CMOS, NMOS enhancement-load, and NMOS depletion-

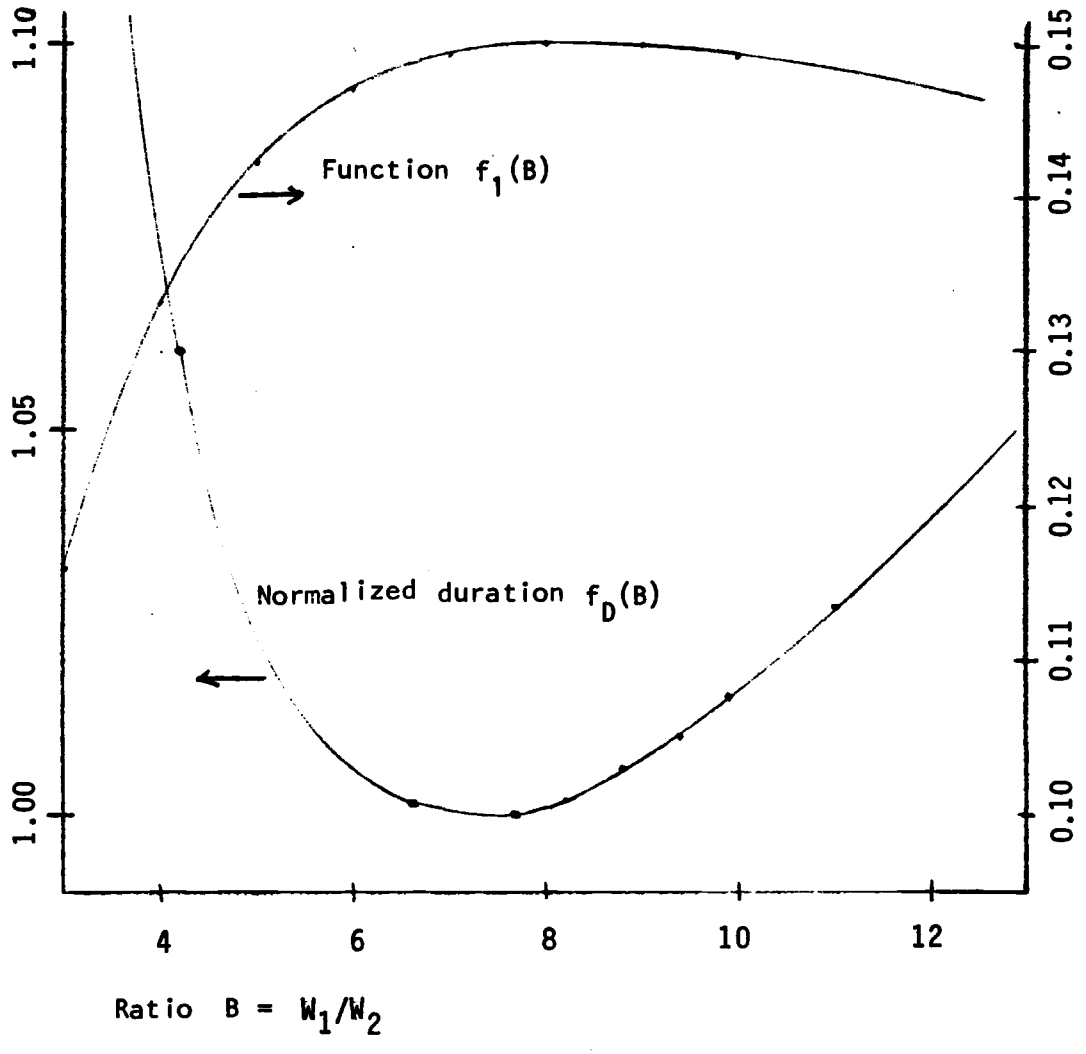


Figure 19

Curve of normalized duration $f_D(B)$ and function $f_1(B)$ showing coincidence of extremes when load capacitance $C_{GS2}$ is taken into account.

load circuits. The CMOS characteristic is wider, indicating that the optimization of device-size ratio is less critical. As predicted by equation 27, the maximum occurs at R=1. The depletion-load characteristic reaches a high maximum value, but falls very quickly as the width of the load device increases.

The values of mobility applicable in this region are significantly lower than the low-field values. For the calculations, we substitute the values obtained by applying the simple MOS formula to the current at $V_{ds} = V_{gs} = 2.5$, resulting in 543 $cm^2/V\text{-}S$ for electrons (in both CMOS and NMOS) and 176 $cm^2/V\text{-}S$ for holes. (In the actual circuit, these will not be constant but will have some dependence on device-size ratio.) Determination of effective channel length is given in the Appendix.

Curves based on equations 27 and 32 (shown in dashed lines in figure 20) are calculated using the effective values of mobility and channel length in the region of operation. (An analytical curve is not shown for the depletion load case, because equation 27 is not applicable to that circuit.)

Simulations were performed to determine the supply power versus $A\omega$ for various flip-flop circuits (figure 21). A clocking frequency of 1.0 MHz was used. The graph shows a lower power requirement for CMOS for a given value of $A\omega$. The slopes of the curves are technology specific, and have units of energy.

NMOS synchronization circuits in integrated form have been given in references [14] and [26]. Figure 22 shows an NMOS synchronizer circuit with a provision for input isolation, as described in reference [26].

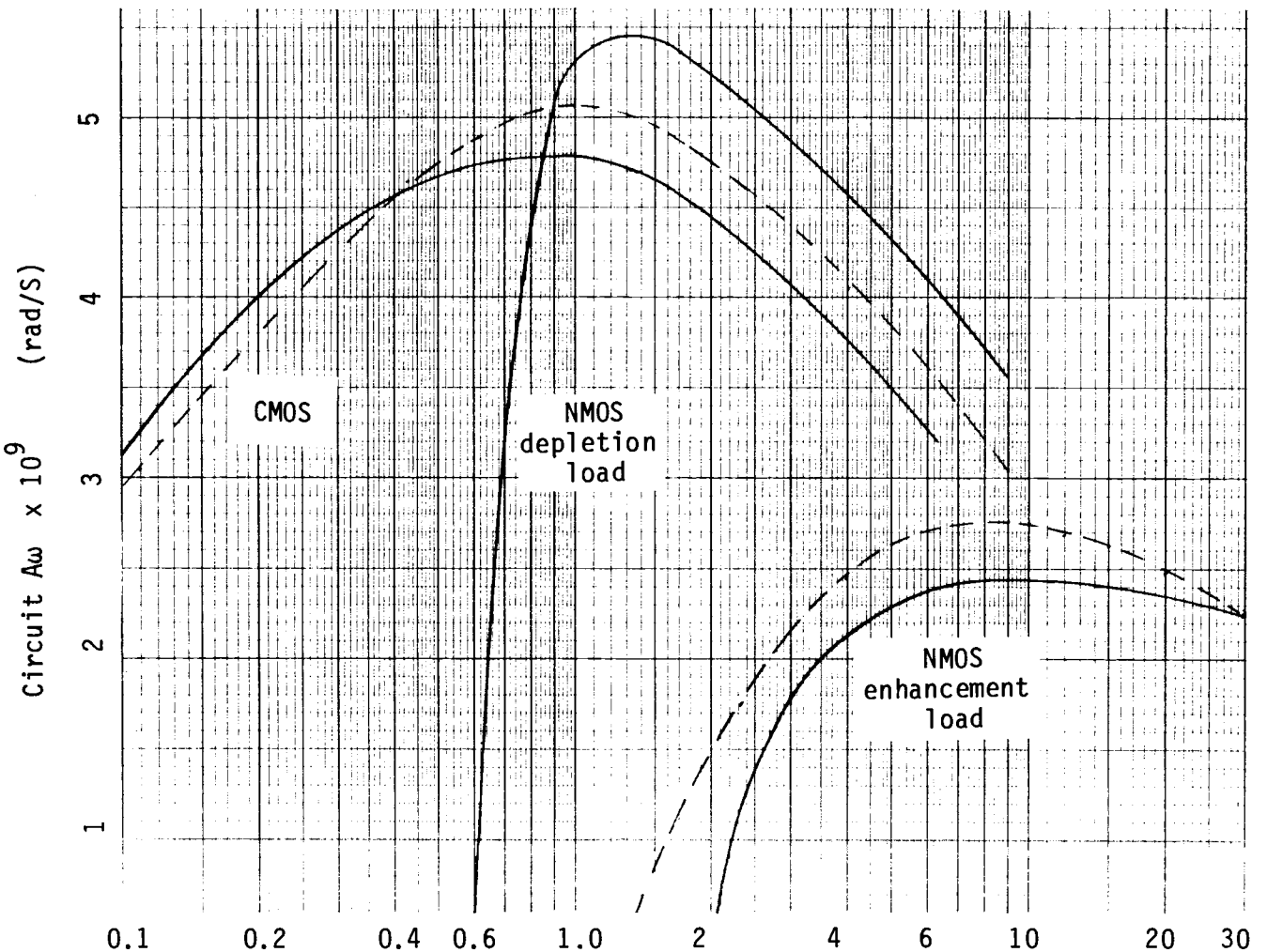


Figure 20 Circuit gain-bandwidth product variation with device size ratio in NMOS and CMOS. Simulation result is in solid line. Dashed line is result of calculation using equations 27 and 32, with known effective channel lengths and mobility as parameters.

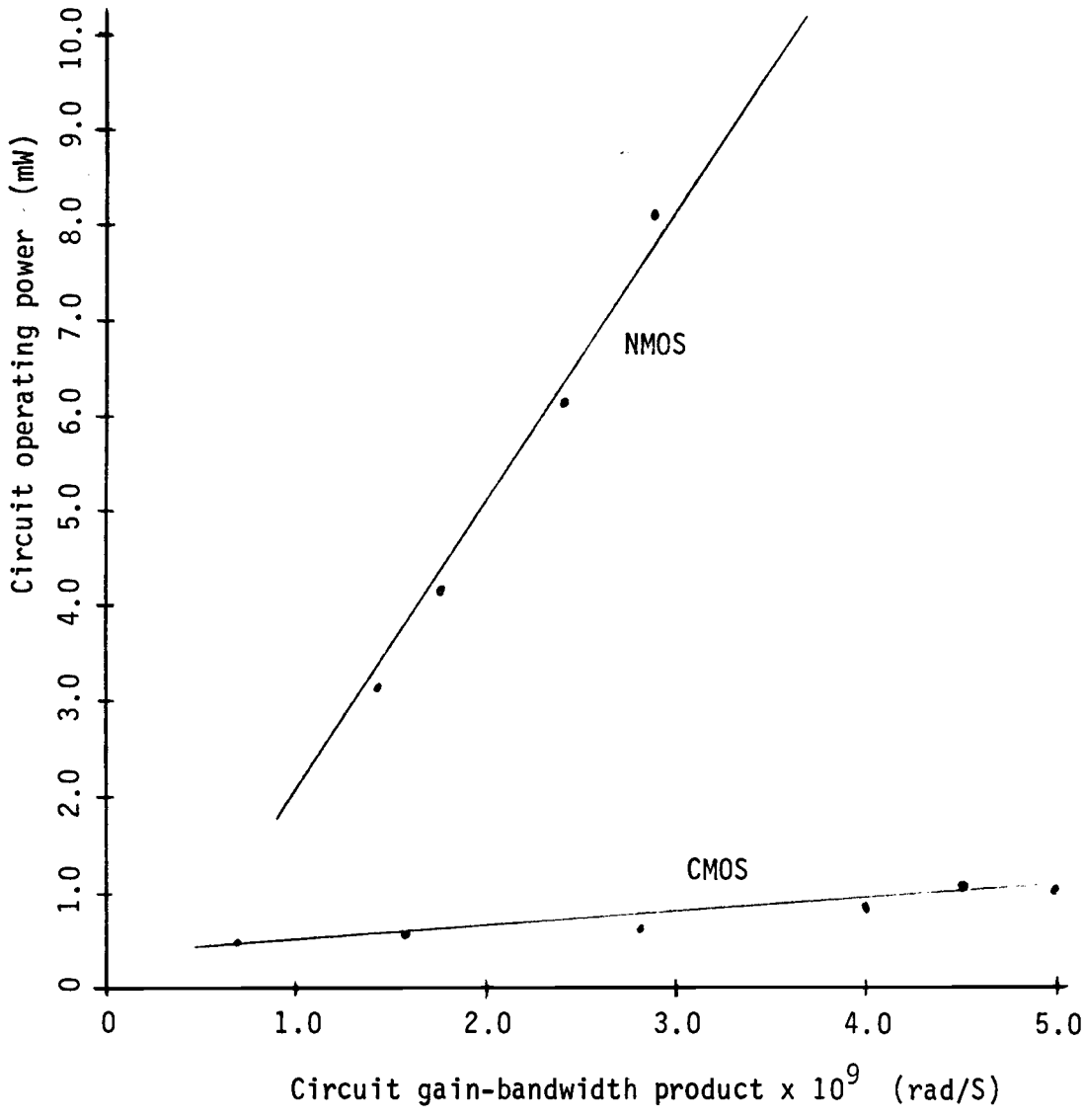


Figure 21

Aω vs operating power at 1.0 MHz for CMOS and NMOS. The slope of each curve has units of energy.

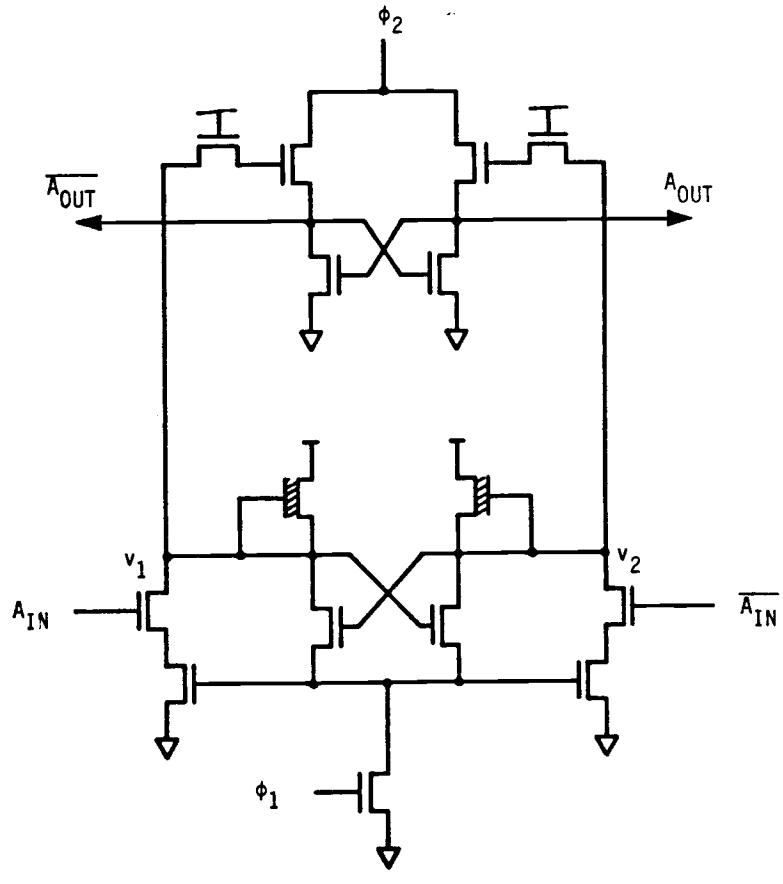


Figure 22

NMOS Synchronization Circuit
given in reference [26].

# III. CMOS Synchronizer Design

## A. Essential Requirements

The recognized requirements for ensuring compliance with established design principles are summarized as:

1. High gain-bandwidth product. A High-gain bistable element is provided, with synchronous (i.e. system) clocks to gate the asynchronous inputs into the bistable, and to gate the result out of the bistable. The bistable is isolated during the interval between the system clock transitions.

2. Input isolation. The first system clock isolates the inputs from the bistable so that input changes cannot influence the bistable after the beginning of the interval.

3. Output isolation. Data from the bistable is gated to the next circuit stage of the machine by the occurrence of the second system clock, at the end of the time interval (a constant in time-bounded designs.)

When used as an arbiter to mediate conflicting requests in a system, there may be another circuit to fulfill some queuing requirement for the rejected request. Each asynchronous input should be processed by an input synchronizer before it is allowed to influence the machine's control signals.

## B. Integrated CMOS Synchronization Test Circuit

Figure 23 shows the integrated configuration used to test synchronization in a CMOS process. This circuit was constructed in a high-performance CMOS process similar to that described by K. Yu et. al. [25] Except that channel length was 2 microns in [25] and 2.5 microns in the circuit of figure 23. A photomicrograph of

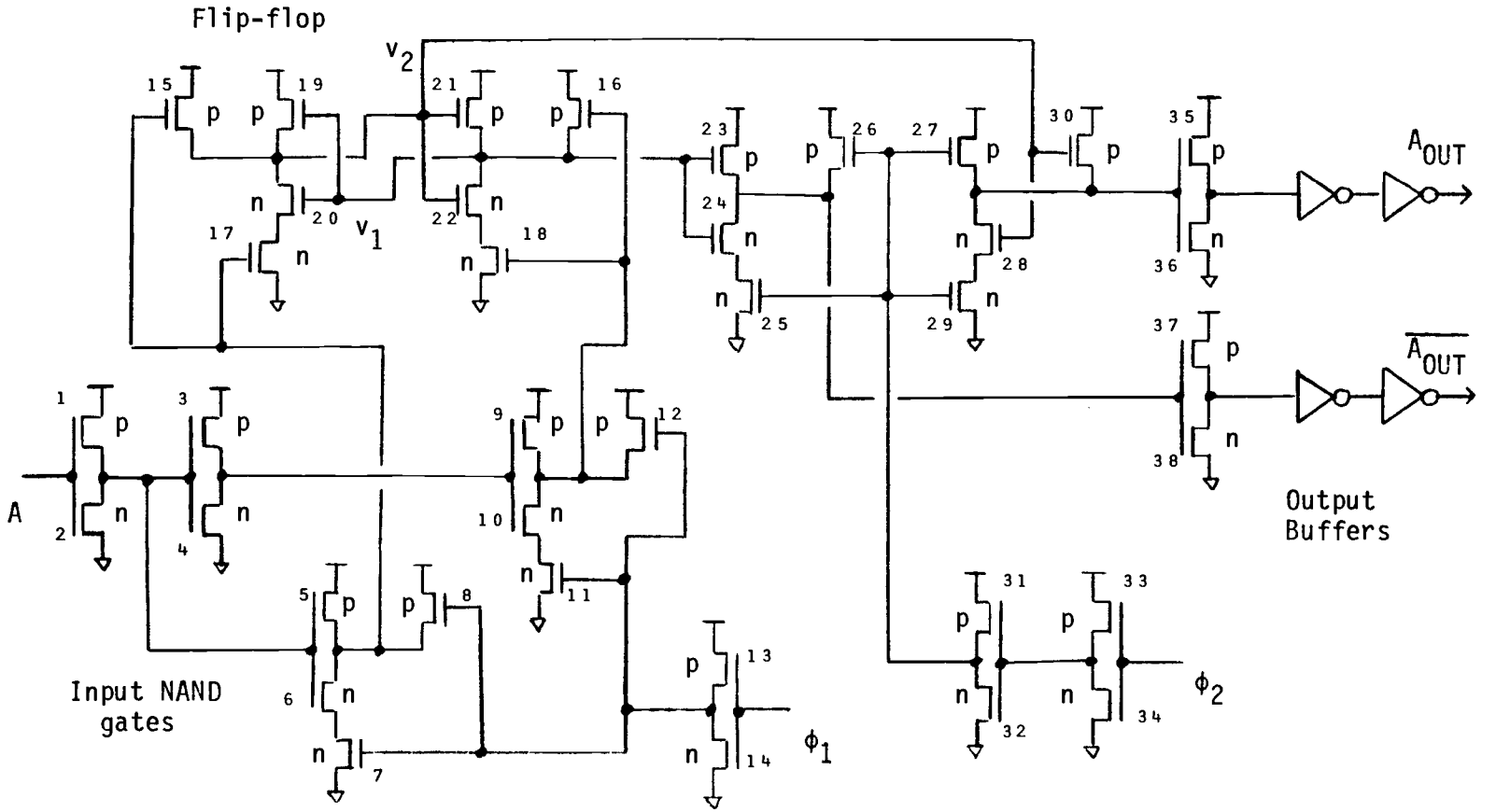


Figure 23 Integrated CMOS Synchronization Test Circuit

the integrated realization is shown in figure 24.

NAND gates formed by M1-M14 isolate the asynchronous input "A". $\phi_1$ and $\phi_2$ are system clocks which control the delay interval. After the sampling event, M15-M16 are "off" and M17-M18 are "on" so that the flip-flop M19-M22 will be free of external influence during the interval. The transition of $\phi_2$ controls special output buffers which have been added to drive external measuring equipment. In an actual system these buffers would not be necessary, and the clock $\phi_2$ could be used to control series transfer devices, as shown in figure 25. The use of these circuits would further reduce the nodal capacitance, and thus increase overall performance. The addition of another cross-coupled circuit at the output could be added if needed to drive some following circuit load, but such an addition would be effective only after completion of the arbitration event, and hence would not increase the arbitration speed.

A calculation can be made for the gain-bandwidth product of the flip-flop of figure 23, by using equation 27 and the effective parameters applicable in the metastable region of operation as described in section II-D. The values of R, $a_2$ and $a_3$ are obtained from the mask design geometries. The values used for this circuit were:

$V_{TN}$ = 0.71 v
$V_{TP}$ = -0.71 v
L = 2.45 μm
$\mu_n$ = 524 $cm^2$/V-S
$\mu_p$ = 226 $cm^2$/V-S
$V_c$ = 5.0 v
R = 0.66
$a_2$ = 0.72
$a_3$ = 0.97

resulting in a calculated value of $A\omega$ :

$$A\omega \text{ (cal)} = 3.2 \times 10^9 \text{ rad/S}$$

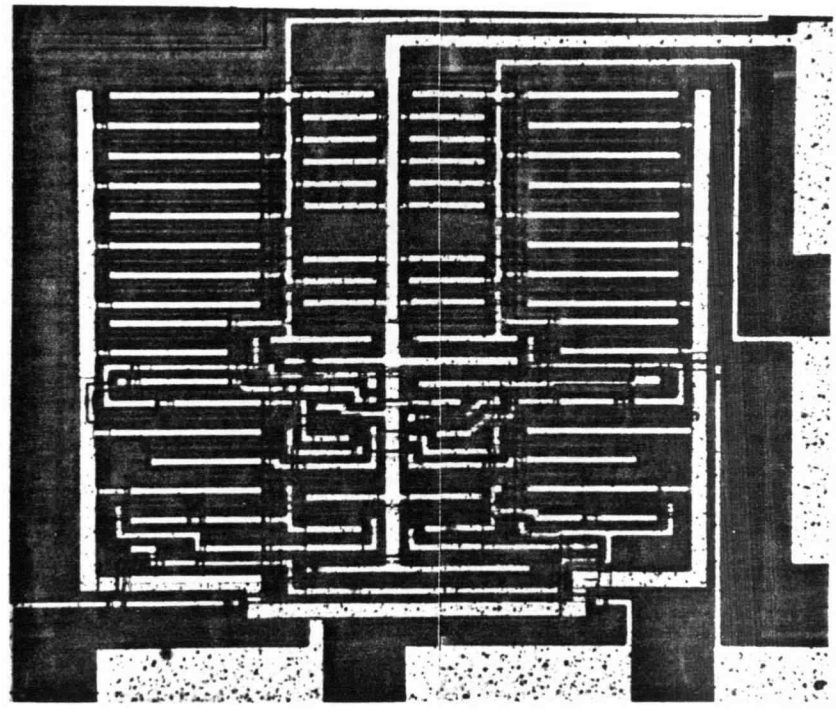

Figure 24 Photomicrograph of the circuit of figure 23. Synchronizing flip-flop is in the center. Large devices at the top are the output buffers. Logic NAND gates for inputs are at the lower left and right. Power supply interconnect is provided at center and at sides.

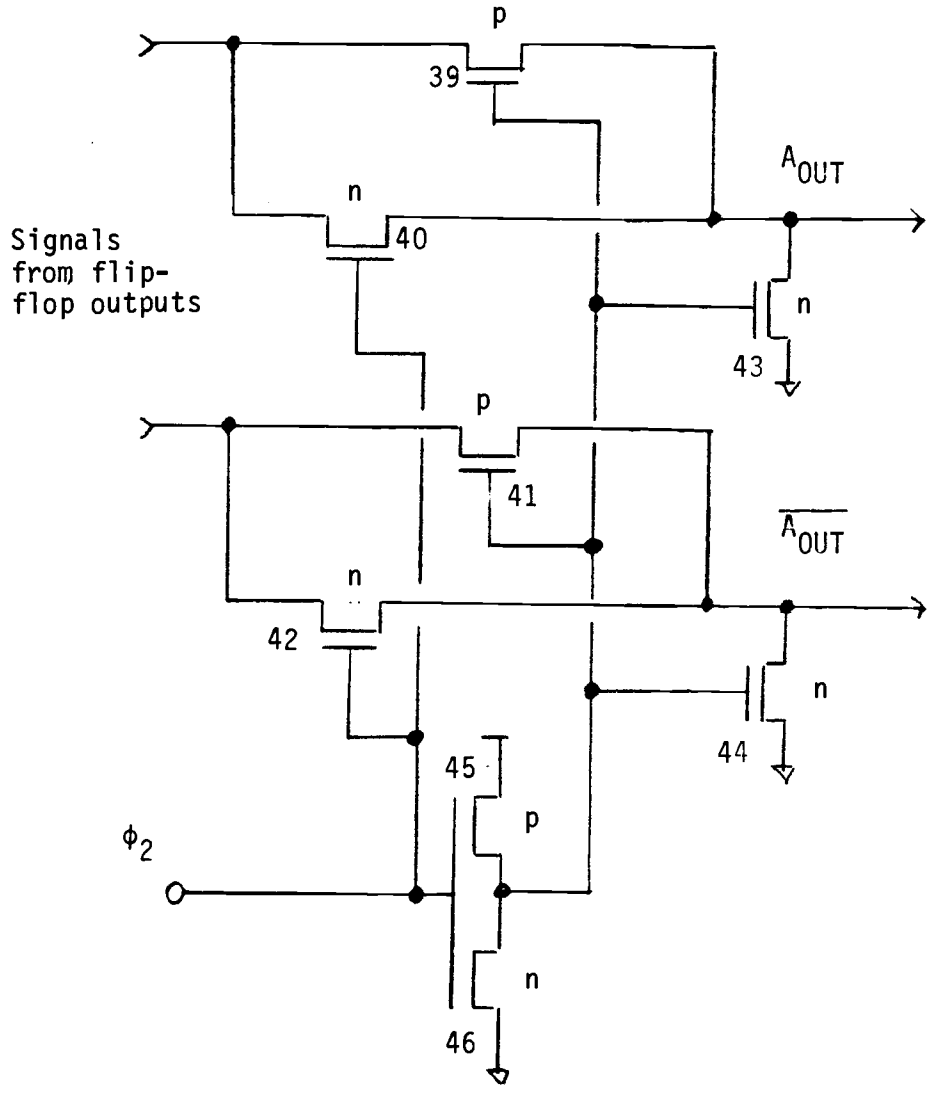


Figure 25

Alternate sampling circuit can be used in integrated synchronizers not requiring output amplifiers as the test circuit does. M39-M42 are "off" during the critical resolution period, so that flip-flop nodes have a lower load capacitance. The outputs then are used to drive other on-chip circuitry and do not need high-current capability. M43 and M44 are provided for noise clamping so that the outputs will not be "floating" (i.e. high impedance) during resolution time.

Simulations were performed to predict the settling characteristics of the flip-flop in this circuit. The network model included junction, interconnect and fringing capacitances. The network simulation input is given in appendix A. The simulation output in tabular form is given in table 1. The graphic simulation output is shown in figure 26. Equation 8 is applied to this data, resulting in a value of:

$$A\omega\,(\text{simulation}) = 2.91 \times 10^{9}\ \text{rad/S}$$

Equation 15 is then applied to determine the predicted error rate for the synchronizer. The simulated and calculated error rates are plotted and compared with experimental data in section IV.

| TIME | V * 1.0D+00 8 7 | V * 1.0D+00 7 0 | V * 1.0D+00 8 0 |
|---|---|---|---|
| 0.0 | 0.00040 | 2.00000 | 2.00040 |
| 1.0000D-10 | 0.00054 | 2.12663 | 2.12717 |
| 2.0000D-10 | 0.00071 | 2.23687 | 2.23759 |
| 3.0000D-10 | 0.00095 | 2.31288 | 2.31383 |
| 4.0000D-10 | 0.00128 | 2.36520 | 2.36648 |
| 5.0000D-10 | 0.00171 | 2.40098 | 2.40269 |
| 6.0000D-10 | 0.00229 | 2.42517 | 2.42745 |
| 7.0000D-10 | 0.00306 | 2.44151 | 2.44457 |
| 8.0000D-10 | 0.00410 | 2.45249 | 2.45659 |
| 9.0000D-10 | 0.00549 | 2.45975 | 2.46524 |
| 1.0000D-09 | 0.00734 | 2.46435 | 2.47169 |
| 1.1000D-09 | 0.00982 | 2.46698 | 2.47680 |
| 1.2000D-09 | 0.01314 | 2.46806 | 2.48120 |
| 1.3000D-09 | 0.01757 | 2.46780 | 2.48538 |
| 1.4000D-09 | 0.02351 | 2.46626 | 2.48976 |
| 1.5000D-09 | 0.03144 | 2.46334 | 2.49478 |
| 1.6000D-09 | 0.04205 | 2.45882 | 2.50087 |
| 1.7000D-09 | 0.05624 | 2.45233 | 2.50857 |
| 1.8000D-09 | 0.07522 | 2.44332 | 2.51853 |
| 1.9000D-09 | 0.10059 | 2.43101 | 2.53161 |
| 2.0000D-09 | 0.13453 | 2.41436 | 2.54889 |
| 2.1000D-09 | 0.17959 | 2.39210 | 2.57169 |
| 2.2000D-09 | 0.23909 | 2.36258 | 2.60167 |
| 2.3000D-09 | 0.31721 | 2.32371 | 2.64091 |
| 2.4000D-09 | 0.41907 | 2.27290 | 2.69197 |
| 2.5000D-09 | 0.55078 | 2.20706 | 2.75784 |
| 2.6000D-09 | 0.71942 | 2.12259 | 2.84201 |
| 2.7000D-09 | 0.93286 | 2.01543 | 2.94829 |
| 2.8000D-09 | 1.19880 | 1.88125 | 3.08005 |
| 2.9000D-09 | 1.51514 | 1.71912 | 3.23426 |
| 3.0000D-09 | 1.86838 | 1.53693 | 3.40530 |
| 3.1000D-09 | 2.23966 | 1.34632 | 3.58597 |
| 3.2000D-09 | 2.60968 | 1.15830 | 3.76797 |
| 3.3000D-09 | 2.96340 | 0.98020 | 3.94360 |
| 3.4000D-09 | 3.28926 | 0.81774 | 4.10700 |
| 3.5000D-09 | 3.57969 | 0.67451 | 4.25420 |
| 3.6000D-09 | 3.83061 | 0.55146 | 4.38207 |
| 3.7000D-09 | 4.04397 | 0.44707 | 4.49104 |
| 3.8000D-09 | 4.22405 | 0.35982 | 4.58387 |
| 3.9000D-09 | 4.37429 | 0.28785 | 4.66214 |
| 4.0000D-09 | 4.49811 | 0.22918 | 4.72730 |
| 4.1000D-09 | 4.59902 | 0.18183 | 4.78085 |
| 4.2000D-09 | 4.68047 | 0.14390 | 4.82437 |
| 4.3000D-09 | 4.74567 | 0.11371 | 4.85938 |
| 4.4000D-09 | 4.79752 | 0.08978 | 4.88730 |
| 4.5000D-09 | 4.83848 | 0.07086 | 4.90934 |
| 5.0000D-09 | 4.94498 | 0.02122 | 4.96619 |

Table 1

Tabular results of computer simulation of metastable decay for circuit of figure 23.

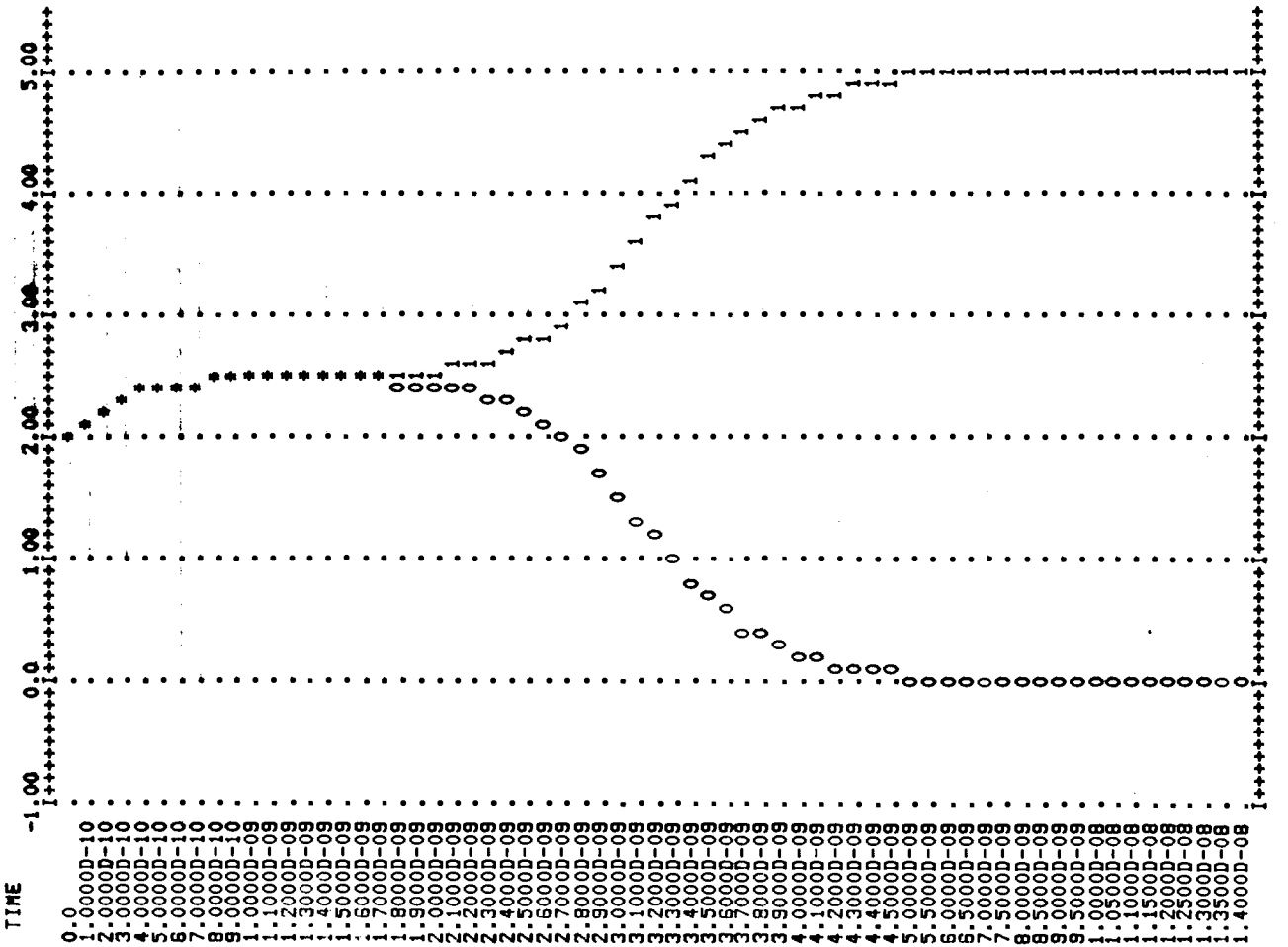


Figure 26 Graphic output of simulation showing metastable decay for circuit of figure 23.

# IV. Experimental Measurement of Synchronization Reliability

## A. Test Set-up and Measurement Technique

To evaluate the performance of the synchronizer, a technique similar to that reported in reference [26] was used. Errors are defined as the persistence of a metastable state beyond the provided delay period. Figure 27 shows the testing scheme. Figure 28 shows a photograph of the test set-up. Figure 29 shows oscilloscope traces for the case in which no conflict occurs. A uniform distribution of input offset values is provided by a very slow sawtooth at input "A" and sampling at a very high frequency at $\phi_1$. The on-chip output buffers are designed with input switching levels such that neither of the outputs will be high until the internal nodes of the flip-flop are well resolved. This allows the use of a logic gate externally, instead of off-chip comparators as were used in the experiments described in [26]. A counter is used to record the number of times that a fully resolved level is not obtained at the outputs at the time of $\phi_3$. The counter is strobed by the signal CNT. Testing is done at an accelerated rate by the use of a delay interval much shorter than would actually be used in a real system. This method provides an accelerated error rate sufficiently high to be measured with a reasonable experiment. Error rates are recorded for various values of delay $T_{EXT}$, measured from $\phi_1$ to $\phi_3$.

The external delay $T_{EXT}$ differs from the internal delay $\Delta T$ due to various combined propagation delays. The approximate values

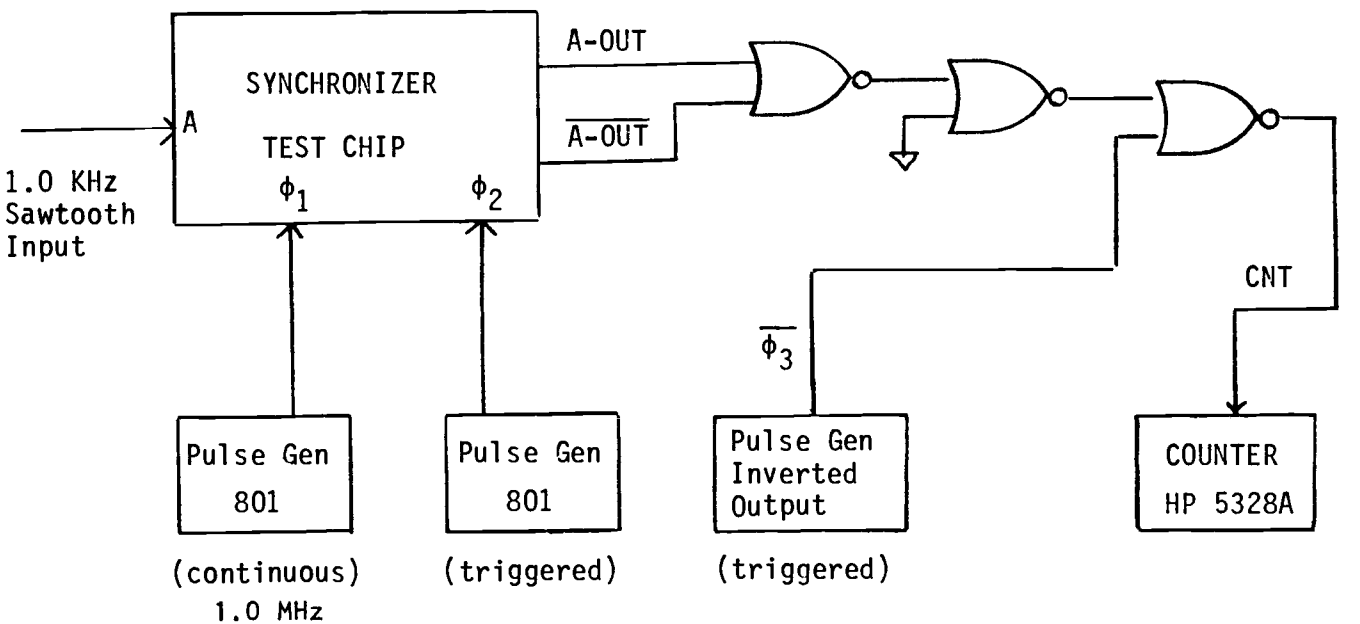


Figure 27 Experimental test set-up

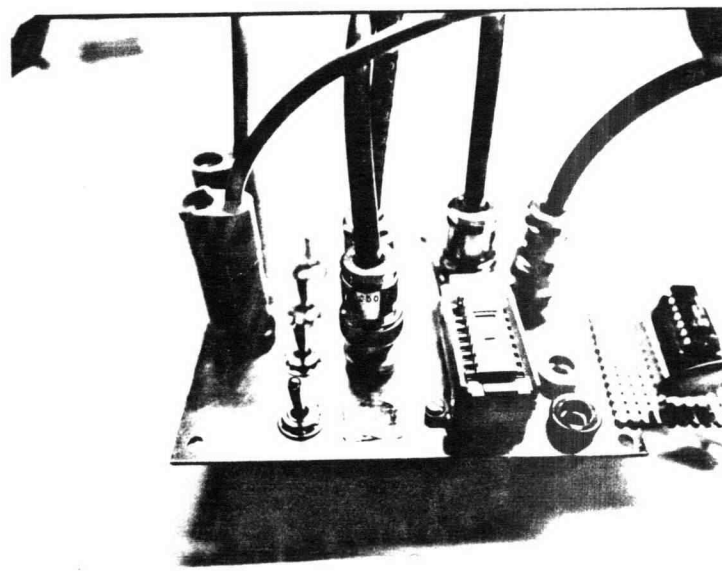

Figure 28 Photograph of test circuit board

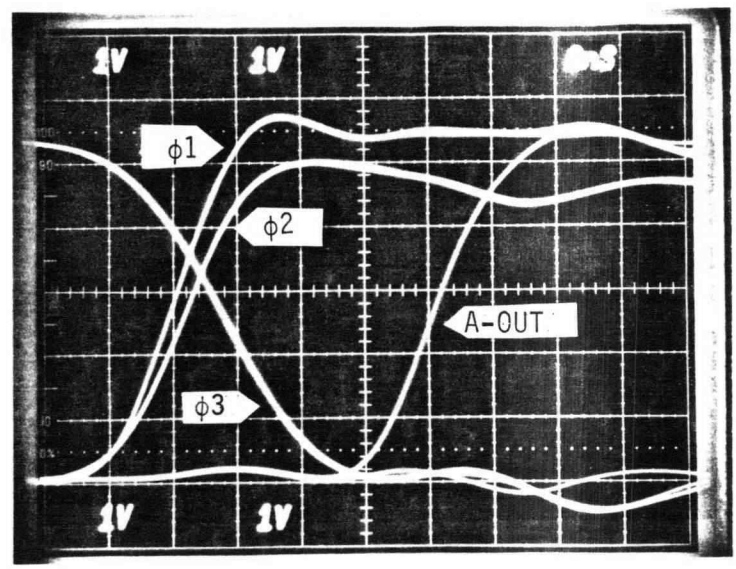


Figure 29

Oscilloscope traces for case in which no arbitration conflict occurs. Only propagation delay is shown. Signal $\phi 3$ is used in the counter clocking circuit.

of these delays were determined by oscilloscope as:

| | | |
|---|---|---|
| t1 = | AOUT(rise) to CNT(fall) | 14 nS |
| t2 = | $\phi_3$(fall) to CNT(rise) | 5 nS |
| t3 = | $\phi_2$(rise) to AOUT(rise) | 7 nS |

The net propagation offset determines the effective internal delay as:

$$T = T_{EXT} - T(prop) \tag{33}$$

The values of t1, t2, t3 above result in a net T(prop) of about 2 nanoseconds. It is clear that this propagation difference is on the same order of magnitude as the value of $\Delta T$ we are using in the accelerated experiment. Hence, for maximum accuracy, the value of $A\omega$ should be determined from the slope of the measured error-rate curve by application of equation 15 at two locations:

$$A\omega = \frac{\ln\left(\frac{R_{E1}}{R_{E2}}\right)}{\Delta T_2 - \Delta T_1} = \frac{\ln\left(\frac{R_{E1}}{R_{E2}}\right)}{T_{EXT,2} - T_{EXT,1}} \tag{34}$$

This result is then independent of T(prop), which then is related to the axis intercept so that:

$$T(prop) = T_{EXT} + \frac{1}{A\omega} \ln\left(\frac{E_R A\omega}{2 f_A f_B}\right) \tag{35}$$

and the error rate can be plotted against $\Delta T$.

## B. Experimental Results

Oscilloscope loading was present at all times during the experiment. The horizontal time-base provided a resolution in which the smallest division represents 0.4 nS. The range over which

meaningful measurements could be made proved to be quite narrow, about 2 nanoseconds. Error counts were recorded at various values of $T_{EXT}$. The results are given in table 2. Determining $A\omega$ from the slope (averaged), the values for the curve are:

$A\omega$ (measurement) = $3.06 \times 10^9$ rad/S

T(prop) = 3.2 nS

Figure 30 gives the error rate vs $\Delta T$ for the simplified model, simulation, and experimental results.

The predicted error rates for larger values of delay $\Delta T$ are shown in figure 31, as calculated from equation 15. From the curve it is clear that even for moderate values of $\Delta T$ the mean time between failure can be made so extremely large that the question of synchronization failure ceases to be a consideration.

It is noted that selection of a guardband for a design should be with regard to $\Delta T$ rather than to MTBF, because a very large guardband in error rate translates into a very small guardband in delay interval. The delay will vary over processing and operating conditions, hence the guardband is designed to accomodate worst-case variation in $\Delta T$.

| $T_{EXT}$ (nS) | $R_E$ ($S^{-1}$) |
|---|---|
| 3.4 | 0.3500 |
| 3.8 | 0.0733 |
| 4.2 | 0.0304 |
| 4.4 | 0.0167 |
| 4.8 | 0.0048 |

Table 2 Experimental measurements of $R_E$

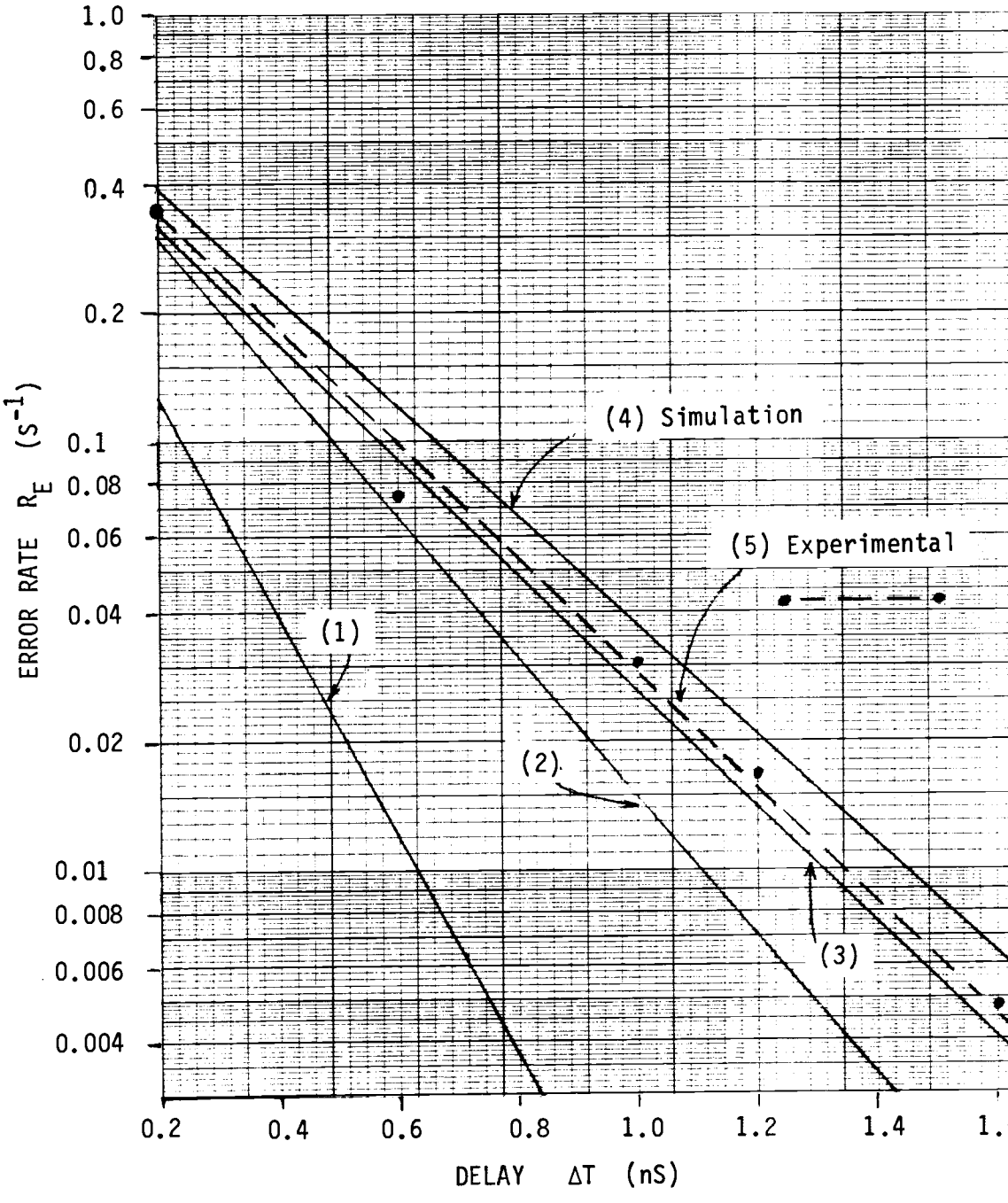


Figure 30

Comparison of error-rate curves versus delay, as determined by:

1) The simple linear equation with low-field mobility
2) Result using effective mobility to reflect velocity saturation
3) Result using parameters for reduced mobility, effective channel length, and capacitance for transient channel-charging (section III-B)
4) Simulation result (section III-B)
5) Experimental data points (section IV-B)

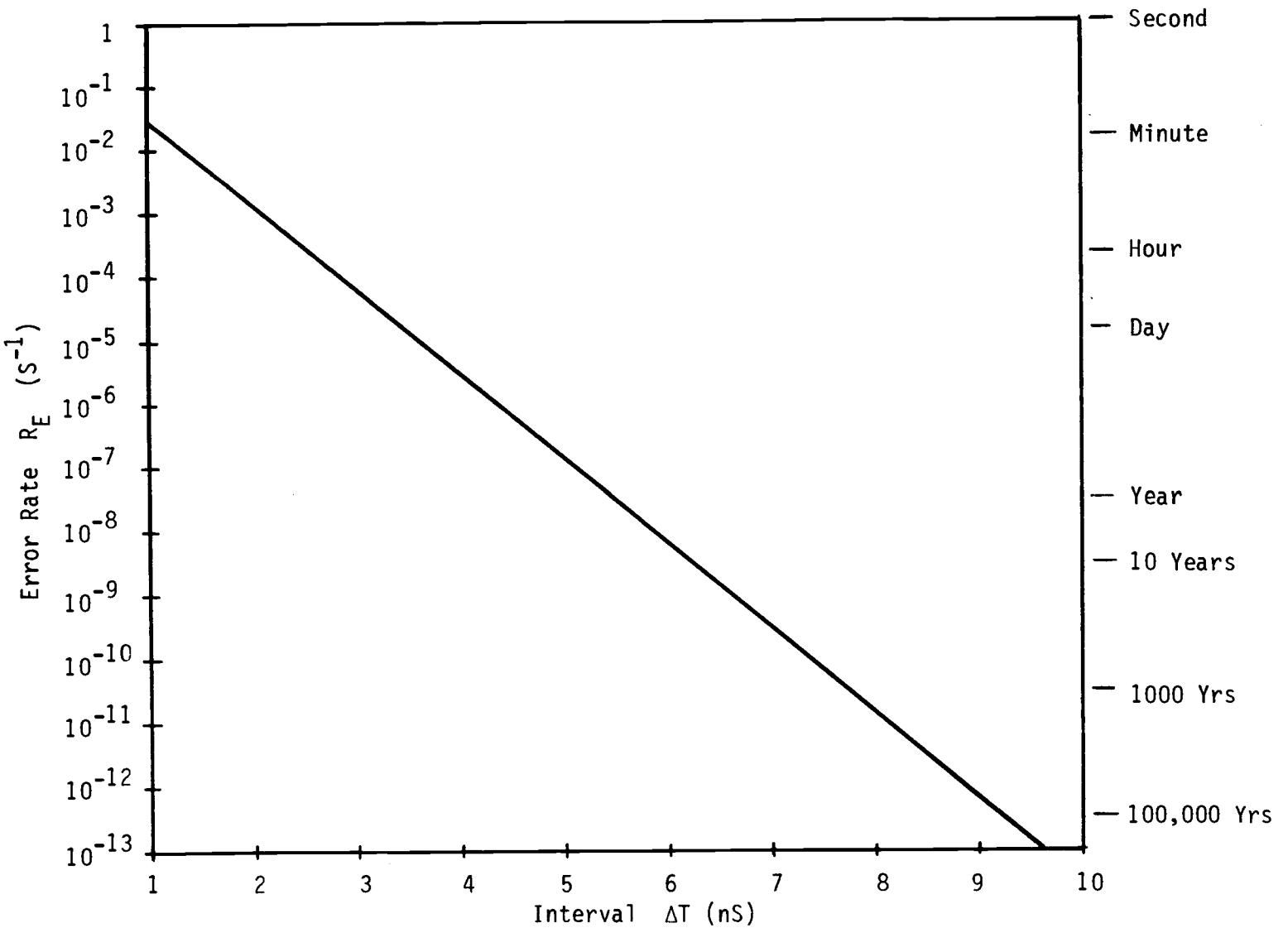


Figure 31 Predicted error rates at $A\omega = 3.06 \times 10^9$, $f_A$ = 1 KHz, $f_B$ = 1 MHz

# V. Summary

In integrated applications using high-frequency asynchronous inputs the required delay is determined from the exponential characteristic of equations 8 and 15 as applied to the parameters of the circuit and of the technology in which it is constructed. The predicted error rate increases linearly with the frequency of the system and of its inputs, but decreases exponentially with the delay interval $\Delta T$, so that in a circuit with high gain-bandwidth product, a very high synchronization reliability can be obtained with very moderate values of $\Delta T$.

High performance synchronization has been demonstrated in an advanced CMOS process technology. Accelerated experimental measurements of circuit reliability were compared with theoretical performance. Design optimization factors have been examined, with attention to various device capacitances and to the effect of channel charging current. It has been shown that while the nodes of a decision flip-flop should be well buffered, an exact selection of device ratio is non-critical. A comparison between CMOS and NMOS circuits has been made. The effect of technology scaling on synchronization performance was reviewed. Attention was called to the importance of recognizing the inevitability of metastable action, and to the importance of flip-flop isolation during metastable decay.

Because of the high-speed characteristics of the integrated realization, high reliability synchronization can be obtained with moderate values of circuit delay, on the same order as that allocated for various sequential operations in a digital system.

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# APPENDIX

# APPENDIX

The simulation network file is given in this appendix. The devices specified are MOSFETs (M) and diodes (D). Sizes are given in microns. The simulator automatically adjusts L for lateral effects, combined with optical mask sizing, etc. Actual channel length being computed internally by the program can be obtained by first performing a simple test-case with two transistors (network file and output below). At very low $V_{ds}$ the effective length is computed from the slopes of the current curves as $V_{gs}$ is slowly varied starting at zero. The two devices are specified at $L_1 = L_{MIN}$ and $L_2 = 100$, so that a determination of $L_{MIN}$ is actually $L_{EFF}$.

(A-1) $$I_D = \mu C_{ox} \frac{W}{L} \left((V_{gs}-V_T)V_{ds} - \frac{V_{ds}^2}{2}\right)$$

(A-2) $$I_D \doteq \mu C_{ox} \frac{W}{L} (V_{gs}-V_T)V_{ds} \qquad \text{(valid at low } V_{ds}\text{)}$$

(A-3) $$\text{slope} = \frac{\Delta I_D}{\Delta V_{gs}}$$

(A-4) $$L_{EFF} = L_1 = L_2 \frac{(\text{slope1})}{(\text{slope2})}$$

$$= 100 \frac{(.02551-.01326)}{(1.2006-.70127)} = 2.453 \text{ microns}$$

```
$ L-EFFECTIVE EXPERIMENT.   FILE NAME = LEFF EXPER
.LIB TTC
.TEMP 25
.PARAM L=4
$  VBB 1 0 DC 0
VDS 2 0 DC 0.3
VGS 3 0 DC 0 PL 0 1000NS 2.5 26000NS
.TRAN 1000NS 26000NS
.PRINT VGS 3 0 I M1 I M2
M1 2 3 0 0 N 100 100
M2 2 3 0 0 N 100 L
.END
```

| TIME | VGS * 1.0D+00 3 0 | I * 1.0D+03 M1 | I * 1.0D-03 M2 |
|---|---|---|---|
| 0.0 | 0.0 | 0.0 | 0.0 |
| 1.0000D-06 | 0.0 | 0.00000 | 0.00000 |
| 2.0000D-06 | 0.10000 | -0.00000 | -0.00000 |
| 3.0000D-06 | 0.20000 | -0.00000 | -0.00000 |
| 4.0000D-06 | 0.30000 | -0.00000 | -0.00000 |
| 5.0000D-06 | 0.40000 | -0.00000 | -0.00000 |
| 6.0000D-06 | 0.50000 | -0.00002 | -0.00000 |
| 7.0000D-06 | 0.60000 | -0.00012 | 0.00001 |
| 8.0000D-06 | 0.70000 | -0.00022 | 0.00017 |
| 9.0000D-06 | 0.80000 | -0.00029 | 0.00218 |
| 1.0000D-05 | 0.90000 | -0.00013 | 0.02893 |
| 1.1000D-05 | 1.00000 | 0.00078 | 0.08781 |
| 1.2000D-05 | 1.10000 | 0.00237 | 0.17787 |
| 1.3000D-05 | 1.20000 | 0.00465 | 0.29838 |
| 1.4000D-05 | 1.30000 | 0.00748 | 0.43299 |
| 1.5000D-05 | 1.40000 | 0.01037 | 0.56897 |
| 1.6000D-05 | 1.50000 | 0.01326 | 0.70127 |
| 1.7000D-05 | 1.60000 | 0.01588 | 0.81261 |
| 1.8000D-05 | 1.70000 | 0.01838 | 0.91805 |
| 1.9000D-05 | 1.80000 | 0.02082 | 1.01484 |
| 2.0000D-05 | 1.90000 | 0.02319 | 1.10854 |
| 2.1000D-05 | 2.00000 | 0.02551 | 1.20054 |
| 2.2000D-05 | 2.10000 | 0.02778 | 1.29851 |
| 2.3000D-05 | 2.20000 | 0.03000 | 1.37348 |
| 2.4000D-05 | 2.30000 | 0.03218 | 1.45581 |
| 2.5000D-05 | 2.40000 | 0.03433 | 1.53579 |
| 2.6000D-05 | 2.50000 | 0.03643 | 1.61352 |

- END OF RUN -

Test simulation for effective channel length

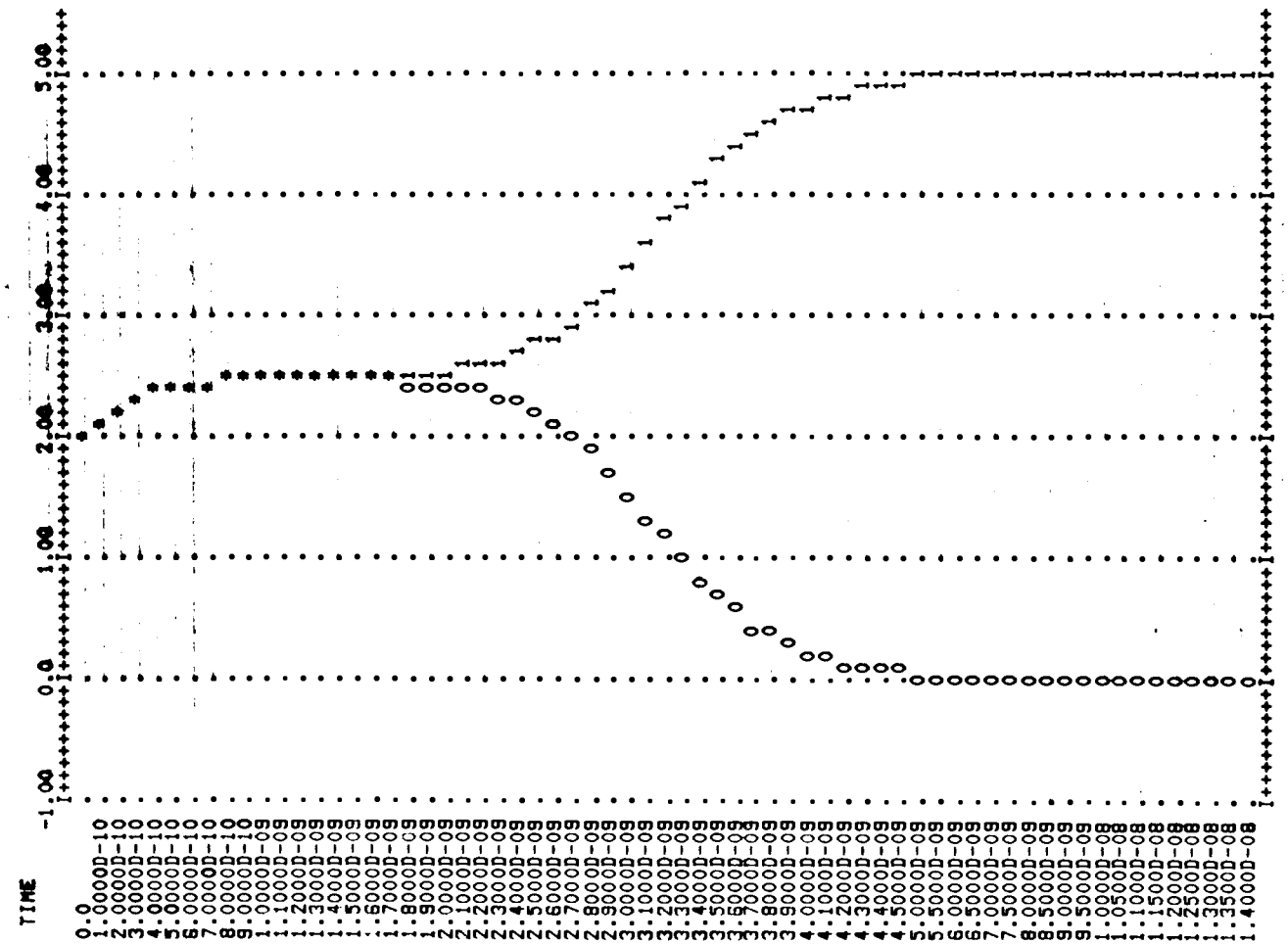
## Simulation of Metastable Decay

Simulation of the metastable decay is accomplished by simulating the entire circuit with some small initial offset, here $V_o$ = 0.00040 volts. $A\omega$ is then computed using two data points and applying equation 8. It is also necessary to ensure a completely balanced and symmetrical bistable in the network file being simulated. Flip-flop imbalance has no statistical effect on synchronizers over a sample of many events, as discussed in section I-D. However, the simulation of a metastable decay represents only one event and hence the result would be significantly affected by an inherent imbalance. Voltage sources at nodes 6 and 15 are added to isolate the asymmetry coupled to the flip-flop by the input stages. These two nodes are normally at a constant high voltage after the occurence of the first stobe, during which time the metastable decay takes place.

In order to verify that the input network file circuit is truly balanced, a test case is performed in which $V_o$ = 0.00000 volts and this balanced condition is observed to persist indefinitely to the limits of numerical accuracy. This test was performed and the persistence observed. The test circuit input file follows. Simulation output was given in section III-B of this paper.

```
$    CMOS SYNCHRONIZER #3   OUTPUTS SIZED FOR TEST CHIP.
$                          DATE 12/03/81   21:57:34
.LIB TTC
 .TEMP 25
 .PARAM VC=5.0
 VCC 2 0 DC VC
 VSUB 1 0 DC 0
 VNWELL 3 0 DC VC
 $
 $    FOR FUNCTIONAL TEST
 $
 $    VSYN1 4 0 DC 0 PL 0 4.5NS 5 9.5NS
 $    VSYN2 25 0 DC 0 PL 0 5NS 5 10NS
 $    VASYN 13 0 DC 0
 $    .TRAN 0.5NS 20NS
 $    .DCVOLT 5=5 6=0 7=VC 8=0 9=0 10=0 11=0 12=5 14=0 15=VC 16=0 17=0
 $    .DCVOLT 18=0 19=VC 20=4 21=5 22=0 23=0 30=5 32=0 33=0 31=5 24=5
 $    .PLOT -1 9 V 4 0 V 25 0 V 32 0
 $    .PLOT -1 9 V 14 0 V 15 0 V 8 0 V 7 0 V 21 0 V 19 0
 $    + V 22 0 V 23 0 V 30 0 V 31 0 V 32 0 V 33 0 V 25 0 V 6 0 V 17 0
 $
 $    FOR RESOLUTION TEST
      V6 6 0 DC 5.0
      V15 15 0 DC 5.0
      .DCVOLT 7=2 8=2.0004  9=0 10=0 5=0 4=5 13=0 12=5 14=0 16=0
      .DCVOLT 24=0 17=5 18=2 20=2 19=5 21=5 22=0 23=0 30=5 31=5 32=0 33=0
      VCIN 25 0 DC 5
      .PRINT V 8 7 V 7 0 V 8 0
       .TRAN 0.1NS 4.5NS  0.5NS 14NS
      .PLOT -1 9 V 7 0 V 8 0 V 23 0 V 32 0
 $
 $
 $.PRINT V 7 8 V 7 0 V 8 0 V 17 0 V 21 0 V 5 0 V 6 0 V 4 0 V 24 0
      .PLOT -1 9 V 7 0 V 8 0
 $.PRINT V 9 0 V 10 0 V 11 0 V 12 0 V 13 0 V 14 0 V 15 0 V 16 0 V 18 0
 $.PRINT V 19 0 V 20 0 V 22 0 V 23 0 V 25 0
 M1 2 8 7 3 P 75 4
 M2 2 7 8 3 P 75 4
 M3 2 6 7 3 P 40 4
 M4 2 15 8 3 P 40 4
 M5 7 8 9 1 N 50 4
 M6 8 7 10 1 N 50 4
 M7 9 6 0 1 N 50 4
 M8 10 15 0 1 N 50 4
 M9 2 5 6 3 P 40 4
 M10 2 12 6 3 P 40 4
 M11 6 12 11 1 N 40 4
 M12 11 5 0 1 N 40 4
 M13 2 4 5 3 P 20 4
 M14 5 4 0 1 N 100 4
 M15 2 13 12 3 P 20 4
 M16 12 13 0 1 N 100 4
 M17 2 12 14 3 P 40 4
 M18 14 12 0 1 N 40 4
 M19 2 14 15 3 P 40 4
 M20 2 5 15 3 P 40 4
 M21 15 14 16 1 N 40 4
 M22 16 5 0 1 N 40 4
 M23 2 7 21 3 P 50 4
 M24 21 7 20 1 N 25 4
 M25 20 17 0 1 N 25 4
 M26 2 17 21 3 P 50 4
 M27 2 8 19 3 P 50 4
 M28 19 8 18 1 N 25 4
 M29 18 17 0 1 N 25 4
 M30 2 17 19 3 P 50 4
```

```
M31 2 21 22 3 P 400 4
M32 22 21 0 1 N 400 4
M33 2 19 23 3 P 400 4
M34 23 19 0 1 N 400 4
M35 2 24 17 3 P 60 4
M36 17 24 0 1 N 20 4
M37 24 25 0 1 N 100 4
M38 2 25 24 3 P 20 4
$
$ OUTPUT STAGE
$
M39 2 22 30 3 P 200 4
M40 30 22 0 1 N 100 4
M41 2 30 32 3 P 500 4
M42 32 30 0 1 N 250 4
M43 2 31 33 3 P 500 4
M44 33 31 0 1 N 250 4
M45 31 23 0 1 N 100 4
M46 2 23 31 3 P 200 4
D3 1 3 DJN 10000 1000
D5N 1 5 DJN 1000 120 200 1260
D5P 5 3 DJP 200 50
D6N 1 6 DJN   0   0 800 500
D6P 6 3 DJP 920 180
D7N 1 7 DJN 405 68 1132 567
D7P 7 3 DJP 1020 65
D8N 1 8 DJN 405 68 1132 567
D8P 8 3 DJP 1020 65
D9N 1 9 DJN 150 4
D10N 1 10 DJN 150 4
D11N 1 11 DJN 150 4
D12N 1 12 DJN 700 120 400 200
D12P 12 3 DJP 200 50
D14N 1 14 DJN 700 120 300 150
D14P 14 3 DJP 200 50
D15N 1 15 DJN 0   0  800 500
D15P 15 3 DJP 200 50
D16N 1 16 DJN 150 4
D17N 1 17 DJN 700 120 800 500
D17P 17 3 DJP 200 50
D18N 1 18 DJN 150 4
D19N 1 19 DJN 300 50 236 900
D19P 19 3 DJP 1200 148
D20N 1 20 DJN 150 4
D21N 1 21 DJN 300 50 236 900
D21P 21 3 DJP 1200 148
D22N 1 22 DJN 700 90 300 400
D22P 22 3 DJP 800 100
D23N 1 23 DJN 700 90 300 400
D23P 23 3 DJP 800 100
D24N 1 24 DJN 700 110 400 200
D24P 24 3 DJP 200 50
D30N 1 30 DJN 500 20 200 300
D30P 30 3 DJP 1500 20
D31N 1 31 DJN 500 20 200 300
D31P 31 3 DJP 1500 20
D32N 1 32 DJN 1500 110 0 19320
D32P 32 3 DJP 4500 190
D33N 1 33 DJN 1500 110 0 19320
D33P 33 3 DJP 4500 190
COUT32 32 0 25PF
COUT33 33 0 25PF
.END
```




Graphic output of simulation showing metastable decay for circuit of figure 23.

| TIME | V * 1.0D+00 8 7 | V * 1.0D+00 7 0 | V * 1.0D+00 8 0 |
|---|---|---|---|
| 0.0 | 0.00040 | 2.00000 | 2.00040 |
| 1.0000D-10 | 0.00054 | 2.12663 | 2.12717 |
| 2.0000D-10 | 0.00071 | 2.23687 | 2.23759 |
| 3.0000D-10 | 0.00095 | 2.31288 | 2.31383 |
| 4.0000D-10 | 0.00128 | 2.36520 | 2.36648 |
| 5.0000D-10 | 0.00171 | 2.40098 | 2.40269 |
| 6.0000D-10 | 0.00229 | 2.42517 | 2.42745 |
| 7.0000D-10 | 0.00306 | 2.44151 | 2.44457 |
| 8.0000D-10 | 0.00410 | 2.45249 | 2.45659 |
| 9.0000D-10 | 0.00549 | 2.45975 | 2.46524 |
| 1.0000D-09 | 0.00734 | 2.46435 | 2.47169 |
| 1.1000D-09 | 0.00982 | 2.46698 | 2.47680 |
| 1.2000D-09 | 0.01314 | 2.46806 | 2.48120 |
| 1.3000D-09 | 0.01757 | 2.46780 | 2.48538 |
| 1.4000D-09 | 0.02351 | 2.46626 | 2.48976 |
| 1.5000D-09 | 0.03144 | 2.46334 | 2.49478 |
| 1.6000D-09 | 0.04205 | 2.45882 | 2.50087 |
| 1.7000D-09 | 0.05624 | 2.45233 | 2.50857 |
| 1.8000D-09 | 0.07522 | 2.44332 | 2.51853 |
| 1.9000D-09 | 0.10059 | 2.43101 | 2.53161 |
| 2.0000D-09 | 0.13453 | 2.41436 | 2.54889 |
| 2.1000D-09 | 0.17959 | 2.39210 | 2.57169 |
| 2.2000D-09 | 0.23909 | 2.36258 | 2.60167 |
| 2.3000D-09 | 0.31721 | 2.32371 | 2.64091 |
| 2.4000D-09 | 0.41907 | 2.27290 | 2.69197 |
| 2.5000D-09 | 0.55078 | 2.20706 | 2.75784 |
| 2.6000D-09 | 0.71942 | 2.12259 | 2.84201 |
| 2.7000D-09 | 0.93286 | 2.01543 | 2.94829 |
| 2.8000D-09 | 1.19880 | 1.88125 | 3.08005 |
| 2.9000D-09 | 1.51514 | 1.71912 | 3.23426 |
| 3.0000D-09 | 1.86838 | 1.53693 | 3.40530 |
| 3.1000D-09 | 2.23966 | 1.34632 | 3.58597 |
| 3.2000D-09 | 2.60968 | 1.15830 | 3.76797 |
| 3.3000D-09 | 2.96340 | 0.98020 | 3.94360 |
| 3.4000D-09 | 3.28926 | 0.81774 | 4.10700 |
| 3.5000D-09 | 3.57969 | 0.67451 | 4.25420 |
| 3.6000D-09 | 3.83061 | 0.55146 | 4.38207 |
| 3.7000D-09 | 4.04397 | 0.44707 | 4.49104 |
| 3.8000D-09 | 4.22405 | 0.35982 | 4.58387 |
| 3.9000D-09 | 4.37429 | 0.28785 | 4.66214 |
| 4.0000D-09 | 4.49811 | 0.22918 | 4.72730 |
| 4.1000D-09 | 4.59902 | 0.18183 | 4.78085 |
| 4.2000D-09 | 4.68047 | 0.14390 | 4.82437 |
| 4.3000D-09 | 4.74567 | 0.11371 | 4.85938 |
| 4.4000D-09 | 4.79752 | 0.08978 | 4.88730 |
| 4.5000D-09 | 4.83848 | 0.07086 | 4.90934 |
| 5.0000D-09 | 4.94498 | 0.02122 | 4.96619 |

Tabular results of computer simulation of metastable decay for circuit of figure 23.