

AN ABSTRACT OF THE THESIS OF

Xiaofeng Xu for the degree of Master of Science in Electrical and Computer Engineering presented on March 12, 1992.

Title: Analysis and Design of Oversampled Digital-to-Analog Converters

Abstract
approved:

Redacted for Privacy

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Oversampled data converters are becoming increasingly popular for high-precision data conversion. There have been many publications on oversampled analog-to-digital (A/D) converters but relatively few on oversampled digital-to-analog (D/A) converters. In this thesis, issues concerning the analysis and design of the oversampled D/A converters are addressed. Simulation tools and analytical methods are discussed. A novel dual-quantization technique for achieving high-precision D/A conversion is proposed. A design example is presented to demonstrate that in many aspects the proposed technique is superior to existing techniques.

The thesis is divided into four chapters. Chapter 1 is an introduction to the general concepts of Nyquist-rate and oversampled data converters. Chapter 2 describes some building blocks to be used in oversampled D/A converters and gives both theoretical and simulation methods for analyzing them. Chapter 3 describes the proposed dual-quantization D/A converters, including the structure, the associated design issues and an example to verify the validity of this technique. Finally, Chapter 4 summarizes the properties of the simulated system and proposes some future research work.

Analysis and Design of Oversampled Digital-to-Analog Converters

by

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A THESIS

Submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Completed March 12, 1992

Commencement June 1992

APPROVED:

Redacted for Privacy

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This thesis is formatted by Xiaofeng Xu.

Date thesis is presented March 12, 1992.

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Analysis and Design of Oversampled Digital-to-Analog Converters

CHAPTER 1 INTRODUCTION

An analog-to-digital (A/D) data converter is a signal conversion system that takes an analog signal (a physical quantity) as its input and produces a digital signal (a mathematical quantity) as its output. A digital-to-analog (D/A) data converter is a signal conversion system that converts signals in a direction opposite to that of an A/D converter.

A digital signal is represented by a discrete-time, discrete-magnitude data sequence. An analog signal may be either continuous time, continuous magnitude or discrete time, continuous magnitude. The continuous magnitude of an analog signal is measured by a physical quantity such as electrical voltage, current, etc.

If we evaluate a D/A converter by its input versus output relationship, then an ideal D/A converter has all its output points on the line $y=Gx$, where G is the gain of the converter and its unit is the same as the output physical quantity y , while x is the input digital signal and y is the output analog signal. For a nonideal D/A converter, some of the output points may lie off the line $y=Gx$. The corresponding errors are classified as offset error, gain error, differential and integral nonlinearities [1]. Among these errors, the

most harmful ones are the nonlinearity errors since they cause harmonic distortion to the signal.

If an analog signal has a limited bandwidth and its highest signal frequency is f_h , its Nyquist rate is defined as $2f_h$. To avoid signal aliasing, the digital signal originally converted from the analog signal usually has a clock frequency slightly above the Nyquist rate of the corresponding analog signal. If a digital signal is to be converted into its analog form, it is usually converted directly without changing the clock rate of the digital signal. These conventional converters are called *Nyquist-rate D/A converters*.

If a digital signal is converted to the corresponding analog signal by first increasing the digital signal clock rate to a rate much higher than its corresponding Nyquist rate, then converted into the analog form, the method is called the oversampling method and the converters are called *oversampled D/A converters*.

The main advantage of Nyquist-rate data converters is that these converters can operate at a relatively low clock frequency for a given sample conversion rate (samples/second). However, the conversion accuracy of these Nyquist-rate data converters depends on the use of high precision analog components. This requirement is contrary to the development of the integrated circuit processing technology, which is going along a direction that can provides higher and higher operational speed but lower and lower component accuracy as a result of a consistent reduction in device dimensions and on-chip supply voltage [2].

The oversampling conversion method offers a good alternative for high-precision data conversion. It takes full advantage of the high operating speed offered by modern IC technology by trading speed for high conversion accuracy. In addition, the harmful nonlinearity errors associated with conventional data converters are eliminated when a single-bit internal D/A converter is used in oversampled data converters [3].

The research efforts in the field of oversampling data conversion technology have mainly been focused on oversampled A/D converters. The main argument for this is that once the structure of an oversampled A/D converter is well defined, it can be easily transformed into an oversampled D/A converter. This argument is valid for the overall structure of the two types of oversampled data converters [4]. However, there are some fundamental differences between A/D and D/A data conversion in oversampled data converters. First, in oversampled A/D converters, the noise-shaping task is done mainly in the analog domain and also partly in the digital domain. In oversampled D/A converters, the noise-shaping task is done in the digital domain only. This difference has many consequences in the design process. Second, in oversampled A/D converters, both internal A/D and D/A converters are required while in oversampled D/A converters, only internal D/A converters are needed. Third, and perhaps most important, the removal of the out-of-band noise is done differently. In an oversampled A/D converter, the out-of-band noise is filtered digitally but in an oversampled D/A converter, it is

filtered in analog domain. This difference makes the design of oversampled D/A converters in many aspects more difficult than the design of oversampled A/D converters, which is the opposite for Nyquist-rate data converters.

In this thesis, to simplify the discussion, all analog systems discussed are assumed to be discrete-time systems. Specifically, the analog functions are assumed to be implemented in switched-capacitor circuits.

CHAPTER 2 ANALYSIS OF OVERSAMPLED D/A CONVERTERS

2.1 Basic Structures

A basic structure of oversampled D/A converters is shown in Figure 2.1 [4], where IF is a digital interpolation filter; NL is a digital noise-shaping loop; DAC is a D/A converter and LPF is an analog lowpass (smoothing) filter. The input signal x is a digital signal represented by a sequence of N_1 -bit digital number at a sampling frequency (clock rate) of f_s . This frequency can be assumed to be the Nyquist frequency of the corresponding analog signal. The interpolation filter increases the sampling frequency to $f_s * R$, which is much higher than f_s (R is the oversampling ratio, $R \gg 1$), and may reduce the number of bits used to represent the signal from N_1 to N_2 . The IF also removes all replicas of the signal in the frequency domain except those centered around the integer multiples of $f_s * R$. It is preferable that the interpolation filter removes the replicas as completely as possible, since this eases the design of the following analog lowpass filter. Since the interpolation filter is followed by a noise-shaping loop NL, which

introduces significant out-of-band noise, the IF only needs to attenuate the replicas to the point where they are lower than the out-of-band noise introduced by the NL.

The NL is used to change the signal from N_2 bits to one bit while maintaining the information in the signal band. The single-bit D/A converter following the noise-shaping loop converts the one-bit digital signal into its analog form. The advantage of using a single-bit D/A converter is that a single-bit D/A converter is inherently linear. If the internal D/A converter is multibit, any nonlinearity in the D/A converter will cause harmonic distortion in the signal band in the final output of the converter [5]. However, using a signal-bit internal D/A converter also has some major disadvantages which will be discussed in the following sections. The focus of this research is to combine the advantages of using a single-bit and a multibit internal D/A converter for an oversampled D/A converter.

Figure 2.2 shows two commonly used noise-shaping architectures (the NL block shown in Figure 2.1) for shaping the digital quantization error $e(n)$. As the figure indicates, all signals are digital. This makes the design of such a loop very flexible and the circuit implementation easy. In addition, the operation of digitally implemented circuit is perfectly accurate if there is no overflow or truncation occurring in the loop.

In general, to achieve the same degree of noise shaping, the error feedback scheme shown in Figure 2.2(b) usually leads to a

simpler circuit implementation than the delta-sigma scheme shown in Figure 2.2(a).

The relationship between the input and the output of the above systems can be generally written as

$$Y = H_S X + H_N E \quad (2.1)$$

where X and Y are the z -transforms of the input signal $x(n)$ and the output signal $y(n)$ respectively; E is the z -transform of the error $e(n)$ due to the digital quantization; H_S is the signal transfer function and H_N is the noise transfer function of the loop. The design of the noise-shaping loop should be such that the signal transfer function H_S does not affect the signal in the signal band and the noise transfer function H_N suppresses the quantization error in the signal band as much as possible.

The single-bit D/A converter following the noise-shaping loop shown in Figure 2.1 converts the single-bit digital data stream into the corresponding analog form in a linear manner. The converted analog output signal from the 1-bit D/A converter contains the same power spectrum as the digital input signal in the signal band. However, it also includes the large quantization noise power which was introduced and highpass shaped by the noise-shaping loop. This out-of-band noise power is then removed by the following analog lowpass filter. The final output analog signal should have the same frequency domain characteristics as the input digital signal in the frequency range $0 \sim f_s/2$.

Because a frequency domain characteristic corresponds to a unique time-domain signal, the output analog signal in the time-domain also closely resembles the input digital signal, assuming that the D/A conversion system does not distort the signal phase.

2.2 Theoretical Analysis

Since the internal digital quantizer in a noise shaping loop is a nonlinear element, an oversampled D/A converter is a nonlinear dynamic system and it is difficult to theoretically analyze such a system without some simplifying assumptions [6][7]. The essential assumption here is that the digital quantization error is an additive white noise, uncorrelated with the other signals. Even though this assumption is not true, it helps us to obtain the initial design parameters. Based on this assumption, linear models can be obtained for oversampled D/A converters. The analysis of the oversampled D/A converters in this section is based on these linearized models.

2.2.1 Digital quantizer and its quantization error

A digital quantizer (sometimes called digital truncator) is a digital system which takes a digital signal as its input, and outputs a digital signal with shorter wordlength than the input signal according to a given algorithm.

The error introduced by a digital quantizer is defined as the difference between the output and the input signals. The characteristics of this error are somewhat similar to those of the quantization error in a conventional A/D converter especially if the wordlength of the input signal to the digital quantizer is much longer than that of its output.

Figures 2.3 and 2.4 shows schematically the outputs of 3-level and M -bit (2^M -level) digital quantizers, and their quantization errors as functions of the input signal. The two curves are shown here as continuous lines, but in fact consist of discrete points. If we assume that the input digital wordlength is much longer than the output signal wordlength, the continuous curves shown represent a good approximation.

The error can be expressed as

$$e(n) = y(n) - x_1(n) \quad (2.2)$$

It is bounded by $(-\Delta/2, \Delta/2)$ when the quantizer is not saturated, where Δ is the level spacing between the output levels. For an M -bit digital quantizer with maximum output levels of $\pm 2^N$

$$\Delta = (2^{N+1}) / (2^M - 1) \quad (2.3)$$

If the error is uniformly distributed in $(-\Delta/2, \Delta/2)$, then the mean-square value of the quantization error $e(n)$ is

$$e_{rms}^2 = \Delta^2 / 12 \quad (2.4)$$

The 3-level digital quantizer is an important element in oversampled D/A converters. Corresponding to a 3-level digital quantizer, the output digital signal of the noise-shaping loop will have 3 levels as well. Thus, a 3-level D/A converter is needed following the noise shaping loop. Such a 3-level D/A converter can be easily implemented with high linearity in a switched-capacitor circuit [8]. To use a digital quantizer with more than 3 output levels is not practical since it is very difficult to implement a D/A converter with more than 3 output levels with high linearity.

The operation of the 3-level digital quantizer is quite different from the commonly used single-bit (2-output-level) digital quantizer. A single-bit digital quantizer is simply a digital truncator which takes the most significant bit of its input as its output and the quantization error (truncation error) is the negative of the remaining bits of the input signal. For a 3-level digital quantizer, its output needs to be determined by the two most significant bits of its input and the error is no longer simply a truncation error but needs to be determined by a subtractor or some simple logic circuit.

As an example, consider the input-output relationship of a 3-level quantizer shown in Figure 2.3(a). Suppose the three levels of the output signal $y(n)$ are chosen to be $\pm 2^{18}$ and 0 ($N=18$ in Figure 2.3.) Then, the range of the input digital signal to the quantizer $x_1(n)$ should be $-3 \cdot 2^{18} < x_1(n) < 3 \cdot 2^{18}$, which corresponds to the unsaturated mode operation of the quantizer. The signal $x_1(n)$ can be represented by a 20-bit interger number.

The quantizer can be implemented with a combinational digital logic circuit. Assume that d_0 is the most significant bit and d_{19} is the least significant bit of the signal $x_1(n)$ and that $x_1(n)$ is expressed in two's-complement notation. The 3-level digital output signal $y(n)$ can be expressed by the following two-bit code

D_0	D_1	Quantizer output
0	1	$+2^{18}$
0	0	0
1	0	-2^{18}

The logic equations for the output $y(n)$ can be obtained from the input-output relationship shown in Figure 2.3(a). They are

$$D_0 = d_0 (\bar{d}_1 + \bar{d}_2) \quad (2.5)$$

$$D_1 = \bar{d}_0 (d_1 + d_2) \quad (2.6)$$

A digital circuit implementation of this logic is shown in Figure 2.5. Since the circuit is very simple, the digital quantizer can be considered to be delay-free.

2.2.2 First-order noise shaping

In equation (2.1), if the noise transfer function $H_N(z)$ is $(1 - z^{-1})$, the noise is first-order high-pass shaped.

As we have discussed in the previous sections, in order to implement the internal D/A converter following the noise-shaping loop with a high linearity, the number of the output levels of the digital quantizer in a noise-shaping loop is limited to 2 or 3 levels. A 2-level digital quantizer is just a digital truncator, which does

not require any digital logic for its output nor for the error. The corresponding 2-level D/A converter is also very simple, and can be easily implemented by using some switches and a reference voltage. A 3-level digital quantizer requires some digital logic for its output and a relatively short wordlength subtractor for the error. The 3-level D/A converter needed is somewhat more complex than the 2-level one. It requires some switches and capacitors and an opamp [8]. The tradeoff between using a 2-level or a 3-level internal D/A converter will be further discussed in the next section

For first-order noise shaping, a 2-level digital quantizer (a single-bit truncator) is a good choice since the system is then very simple and has adequate stability [9]. A stability problem in a digital feedback loop will cause signal overflow or signal amplitude clipping in the loop, and will consequently introduce significant noise power into the signal band [10]. In a practical circuit where the wordlength of the registers in the loop is given, solving the stability problem corresponds to preventing the overflow or amplitude clipping from happening.

Figure 2.6(a) shows a noise-shaping loop, which is the first-order realization of the system shown in Figure 2.2(b). The difference equations for the loop can be written as

$$e(n) = y(n) - x_1(n) \quad (2.7)$$

$$x_1(n) = x(n) - e(n-1) \quad (2.8)$$

$$y(n) = x(n) + e(n) - e(n-1) \quad (2.9)$$

If the digital quantizer has only 2 output levels $y(n)=\pm q$, the error $e(n)$ will be $|e(n)| \leq q$ if and only if $|x_1(n)| \leq 2q$, which is the condition for the quantizer to be operated in an unsaturated mode. From equation (2.8), we can see that the single-bit digital truncator will not be saturated as long as the input signal amplitude is less than the maximum output value of the quantizer q . Thus, no amplitude clipping occurs in such a loop when the wordlength of the registers in the loop is greater than $\log_2(2q)+1$.

Next, we discuss the oversampling ratio needed for a given system resolution in the first-order noise-shaping case.

Suppose that the input digital signal $x(n)$, which is to be converted into the corresponding analog signal, has a k bit wordlength. This signal can be represented by an integer number such that $-2^{k-1} < x(n) \leq 2^{k-1}$. Since the upsampling operation ideally does not affect the signals in the baseband, the inband quantization noise power associated with the input signal $x(n)$, which is the signal after the upsampling operation, is the same as the quantization noise power before upsampling. Assume that the quantization noise associated with the digital signal before upsampling is a white noise and is evenly distributed in the range of $[-1,1]$. Then, the noise power inherently associated with the signal $x(n)$, when measured by its mean-square value, is

$$n_k^2 = e_{k\text{rms}}^2 = 1/12 \quad (2.10)$$

On the other hand, the truncation error introduced in the noise-shaping loop is bounded by $-2^{k-1} < x(n) \leq 2^{k-1}$, when a 2-level digital quantizer is employed. The mean-square value of the error $e(n)$ is

$$e_{rms}^2 = (2^{k-1})^2 / 12 \quad (2.11)$$

Since the error $e(n)$ is high-pass shaped by $(1-z^{-1})$, the spectral density of the shaped error $e(n)$ is

$$N(f) = e_{rms} \left| 1 - e^{j2\pi f / 2Rf_0} \right| = 4 \frac{1}{\sqrt{Rf_0}} e_{rms} \left| \sin(\pi f / 2Rf_0) \right| \quad (2.12)$$

where R is the oversampling ratio and f_0 is the passband frequency. Thus, the noise power in the signal band contributed by the error $e(n)$ is

$$n^2 = \int_0^{f_0} |N(f)|^2 df = \pi^2 e_{rms}^2 / 3R^3 \quad (2.13)$$

To ensure that the truncation noise power introduced in the noise shaping loop is less than the input digital signal quantization noise power in the signal band, we obtain

$$n^2 < 1/12$$

This requires that the oversampling ratio R needs to satisfy

$$R^3 > 12\pi^2 e_{rms}^2 / 3 \quad (2.14)$$

Then, from equation (2.11), we obtain

$$R^3 > \pi^2 (2^{k-1})^2 / 3 \quad (2.15)$$

For a 16-bit resolution D/A converter ($k=16$), the above equation requires that the oversampling ratio should be at least 2418 so that the noise power introduced in the noise-shaping loop is about the same as that inherently associated with the input signal. Usually, n^2 should be much smaller than n_k^2 . If the converter is to have an N -bit conversion resolution, we may require that k should be at least equal to $N+1$ in equation (2.15). This simply means that the theoretically calculated noise power contributed by error $e(n)$ in the signal band will be 6 dB less than the quantization noise power of the input digital signal, without taking the nonlinear effects and the nonidealities of the analog circuit realizing the smoothing filter into account.

As we have shown above, oversampled data converters using first-order noise-shaping loops require a large oversampling ratio in order to achieve a 16-bit resolution. This is a major drawback of first-order noise-shaping data converters. Another important drawback of these data converters is that they often need a dithering signal to reduce the nonlinear limit-cycle effect [11]. This may significantly reduce the input signal's dynamic range, and thus reduce the overall system dynamic range and resolution. To overcome these difficulties, higher-order noise-shaping loops are often used.

2.2.3 Second-order noise shaping

If the noise transfer function $H_N(z)$ in equation (2.1) is $(1 - z^{-1})^2$, the digital quantization noise is second-order highpass shaped.

The operation of second-order noise shaping loops is somewhat more complex than that of first-order ones since there is a possibility of amplitude clipping in second-order noise shaping loops unless the digital quantizer in the loop has more than 4 output levels [4]. The internal operation of a second-order noise-shaping loop will be examined in the following.

Suppose that the second-order noise shaping is accomplished in a single-loop and single-bit noise-shaping loop as shown in Figure 2.6(b) with $M=2$. The difference equations are

$$e(n) = y(n) - x_1(n) \quad (2.16)$$

$$x_1(n) = x(n) - 2e(n-1) + e(n-2) \quad (2.17)$$

$$y(n) = x(n) + e(n) - 2e(n-1) + e(n-2) \quad (2.18)$$

Since the quantizer again has 2 output levels $y(n)=\pm q$, $x_1(n)$ must be bounded by $\pm 2q$ in order for the quantizer to not be saturated, i.e., $e(n)$ being bounded by $\pm q$. From equation (2.17), it is clear that $x_1(n)$ will not be bounded by $\pm 2q$ even when the input $x(n)=0$. So, the clipping of the signal amplitude or data overflow in the loop is inevitable in a single-loop, single-bit second-order digital noise-shaping loop.

To avoid such clipping, the truncator needs to have at least 4 output levels $y(n)=\pm q/3, \pm q$. In this case, the condition for the digital quantizer to be operated in the unsaturated mode is that $x_1(n)$ be bounded by $\pm 4q/3$, which results in the error $e(n)$ being bounded by $\pm q/3$. A sufficient condition from equation (2.17) is

that $|x(n)| \leq q/3$. Then, no overflow or amplitude clipping will occur in the loop.

The operation of the digital truncator with 4 output levels is essentially the same as the one with 2 output levels except that the quantizer output is now the most significant two bits of its input signal.

However, as we have discussed in section 2.2.1, a noise-shaping loop using a digital quantizer with 4 output levels requires a 4-level D/A converter following the noise-shaping loop to convert the signal into the analog form. Since it is difficult to make a 4-level D/A converter with high linearity, the nonlinearity error of the 4-level D/A converter will become a dominant noise source in the final output.

A good compromise between using a 2-level and a 4-level digital quantizer in a second-order noise-shaping loop is to use a 3-level digital quantizer. A 3-level digital quantizer in the noise-shaping loop requires the use of a 3-level D/A converter to convert the signal into the analog form. This is practically feasible because a 3-level D/A converter can be easily implemented in a switched-capacitor circuit with high linearity [8]. The input-output relationship and the implementation of the 3-level digital quantizer were discussed in section 2.2.1.

The possibility of amplitude clipping is still present in a second-order noise-shaping loop utilizing a 3-level digital quantizer. To prevent the clipping, computer simulations are needed to find the

maximum node values for all possible overflow nodes in the loop in order to determine the number of bits required in the internal registers.

As we have discussed in the previous section, the oversampling ratio needed for oversampled D/A converters with first-order noise-shaping characteristics is quite large. In the following, the oversampling ratio needed for the oversampled D/A converters with second-order noise shaping characteristics will be discussed.

Suppose a second-order noise-shaping loop has m output levels, equivalent to $M = \log_2(m)$ bits (Figure 2.6b). The wordlength of the input digital signal to the loop $x(n)$ is k bits, which can be represented by integer numbers $-2^{k-1} < x(n) \leq 2^{k-1}$. The maximum output value of the quantizer q is set to be equivalent to 2^{k-1} . If we assume that the digital quantizer is operated in the unsaturated mode, the mean-square value of the quantization error $e(n)$ introduced in the noise-shaping loop is

$$e_{rms}^2 = \frac{[(2^{k-1})/(m-1)]^2}{12} \quad (2.19)$$

Since the error $e(n)$ is second-order highpass shaped by $(1-z^{-1})^2$, its spectral density is

$$N(f) = e_{rms}^2 \left| 1 - e^{j(2\pi f/2Rf_0)} \right|^2 = \frac{16}{Rf_0} * e_{rms}^2 \sin^2\left(\frac{\pi f}{2Rf_0}\right) \quad (2.20)$$

The mean-square value of the noise in the signal band is

$$n^2 = \int_0^f |N(f)|^2 df = \frac{\pi^4 e_{rms}^2}{5R^5} \quad (2.21)$$

In order for the noise power n^2 to be less than the inherent quantization noise power of the input digital signal $x(n)$, from equations (2.10) and (2.21), the oversampling ratio must satisfy

$$R^5 > \frac{12\pi^4 e_{rms}^2}{5} \quad (2.22)$$

From equation (2.19), we obtain

$$R^5 > \frac{\pi^4 [(2^k - 1)/(m - 1)]^2}{5} \quad (2.23)$$

Thus, for a 16-bit resolution oversampled D/A converter with a 3-level digital quantizer used in the noise shaping loop, R only needs to be larger than 116 from the above equation. This is a considerably smaller value than the ratio of 2418 required in the first-order case.

2.3 Computer Simulations

2.3.1 Introduction

Characterization of conventional (Nyquist-rate) data converters can be done by comparing the input samples to the corresponding output samples. This is appropriate since there exists a one-to-one correspondence between the input data samples and the output data samples in Nyquist-rate data converters. Their performance is usually measured by the peak error, and/or the differential and the integral nonlinearities [1].

The evaluation of oversampled data converters cannot be done by using this conventional method because there is no one-to-one correspondence between the input data samples and the output data samples, or to say it more accurately, the sample-to-sample error after digital decimation (or analog smoothing) is not just a function of the characteristics of the data converter but also a function of the input signal. The use of digital decimation filters in oversampled A/D converters and digital interpolation filters in oversampled D/A converters means that each input sample contributes to a certain number or all of the output samples depending on whether the filters are FIR or IIR. The objective in this conversion is not to accurately convert samples one-to-one from one signal form to the other, but rather to convert the signals in such a way that the information in the signal band is accurately preserved. Consequently, it is more appropriate to measure the modulator performance in the frequency domain by measures such as signal-to-noise ratio and dynamic range.

The dynamic range, peak signal-to-noise ratio and the signal-to-noise ratio as a function of the input signal amplitude are the most commonly used specifications for oversampled data converters [12]. The input signal used to verify the above specifications is usually a sinusoidal signal. When the performance of oversampled data converters is to be compared with conventional Nyquist-rate data converters, these specifications can be converted into an equivalent number of bits. If the above specifications are expressed in logarithmic scale (in dB), the formula for converting these

specifications into the equivalent number of bits B in the case of sinusoidal input signal can be approximately written as $B \approx (\text{SNR in dB})/6$.

For a given oversampled data conversion system, our goal in doing computer simulations for the system is to determine its performance and to help us understand these nonlinear systems. Due to the difficulties in obtaining analytical expressions for such nonlinear systems, most of the analytical results are based on the linearized models which assume that the quantization or truncation errors can be represented by white noise. The analytical results are important in getting the initial design parameters, but are inadequate for determining the SNR accurately and for determining the bounds on signals in the time domain. As a result, the design of oversampled data converters is heavily dependent on computer simulations. Developing tools to enhance the simulations is an important part of the research.

Since different methods and different programs used to do the simulations can give slightly different results, it is necessary to specify the methods used in order to correctly interpret the results of these simulations. The programs used in this research are all written in the FORTRAN programming language.

2.3.2 System simulation

In oversampled D/A converters, the noise-shaping loop is a digital system as discussed in section 2.1. In order to include the

finite wordlength operation of a digital circuit in a computer simulation, integer arithmetic is used in the simulations.

An important error source associated with digital circuits is data overflow (amplitude clipping).

In digital circuits, overflow error will occur only if the internal registers are not long enough. Neither overflow nor amplitude clipping permissible in a noise-shaping loop since either effect will cause a significant noise power increase in the signal band. To prevent any overflow in the noise-shaping loop, the maximum value of all internal signals in the loop should be found as a function of the input signal amplitude. This determines the minimum wordlength needed for each internal register and shows when the digital quantizer will be overloaded. Figure 2.7 shows such a plot for the signal $x_1(n)$ of the system shown in Figure 2.6(b). After obtaining these plots, each internal register wordlength can be chosen such that no overflow or amplitude clipping will happen.

By using dynamic system simulation methods [13], the time domain data of the system's response to the input signal can be obtained.

2.3.3 Frequency response

The time-domain response of an oversampled D/A converter to a input sine signal, which can be obtained from the system simulation discussed above, can be used to calculate the spectrum

by means of FFT algorithms. The data is first multiplied by a properly chosen window, and then we use FFT algorithms to estimate the power spectrum of the signal.

Windowing plays an important role in power spectrum estimation [14]. Simulation results indicate that the Hanning window is a good compromise between computational complexity and accuracy for our purpose and it was used throughout this research to ensure the consistency in comparison of different modulator structures.

A typical output spectrum for an oversampled D/A converter with sine wave input is shown in Figure 3.5.

2.3.4 Signal-to-noise ratio

As we have discussed in section 2.3.1, the signal-to-noise ratio as a function of the input signal amplitude is one of the most important characterizations of oversampled data converters. From this calculation, we can determine the dynamic range and the resolution of the system under investigation. In addition, since nonlinear effects are functions of the input signal amplitude, many nonlinear effects which are hard to analyze in the linearized model can be detected from this calculation.

There are several methods for calculating the signal-to-noise ratio [15] [16]. The most commonly used one is to use the periodogram to estimate the spectral density and then calculate

the signal power and the noise power from the calculated spectral density.

If we assume that the modulator output signal $y(n)$ is a stationary signal and is ergodic, to estimate its power, it can be first multiplied by a window $w(n)$, which gives

$$y_w(n) = y(n)w(n) \quad (2.24)$$

where $w(n)$ is a real sequence with finite length $N+1$. The Fourier transform of the resulting sequence $y_w(n)$ is

$$Y_w(e^{j\omega}) = \sum_{n=-\infty}^{\infty} y_w(n)e^{-j\omega n} = \sum_{n=0}^N y_w(n)e^{-j\omega n} \quad (2.25)$$

Then, the total power in the signal frequency band $[0, f_0]$ is [14]

$$P_y = \frac{1}{2\pi} \sum_{k=0}^{(N+1)f_0} |Y_w(k)|^2 \quad (2.27)$$

where

$$Y_w(k) = Y_w(e^{j\omega}) \big|_{\omega=2\pi k/(N+1)}$$

which can be calculated by $(N+1)$ point FFT algorithm, and $f_0 = \frac{\omega_0}{2\pi}$ is the passband frequency normalized to f_s , the sampling frequency.

To remove the bias introduced by the window in this estimation, proper scaling is needed. Since our purpose is to

obtain the ratio of the signal power and the noise power, the bias in estimating the noise power and the signal power will be cancelled. Thus, the bias of the estimation method is not of concern. But the consistency of the estimation method needs to be taken into account in some cases. To improve the consistency of the estimation, the average of the periodogram can be used instead of the periodogram [14]. Then the power is estimated by

$$\Pi_v = \frac{1}{L} \sum_{r=0}^{L-1} P_y(r) \quad (2.28)$$

where L is the number of the periodograms used to do the averaging.

The above method gives a general procedure for estimating the power and the power density of a given data sequence. For an oversampled data converter, the output signal sequence $y(n)$ contains both the input signal $x(n)$ and the quantization noise $e(n)$. If we choose the input signal frequency to be $\omega_t = (2\pi)n_t/(N+1)$, where n_t is an integer number, then the signal power can be estimated by

$$P_S = \frac{1}{2\pi} |Y_w(n_t)|^2 \quad (2.29)$$

To reduce the window effects in estimating the noise power, the two adjacent power density points to the input signal frequency need to be deleted in the calculation of the noise power. To have sufficient estimation accuracy, N needs to be sufficiently

large so that the deletion will not affect the estimation of the noise power. The noise power is estimated by

$$P_N = \frac{1}{2\pi} \sum_{k=0}^{n_t-2} |Y_w(k)|^2 + \frac{1}{2\pi} \sum_{k=n_t+2}^{(N+1)f_0} |Y_w(k)|^2 \quad (2.30)$$

The signal-to-noise ratio (SNR) in dB is then estimated from

$$\text{SNR} = 10 \log_{10}(P_S/P_N) \quad (2.31)$$

Some typical plots of the signal-to-noise ratio as a function of the input signal amplitude are shown in Figure 3.4.

CHAPTER 3 DUAL-QUANTIZATION OVERSAMPLED D/A CONVERTERS

3.1 Introduction

An oversampled D/A converter using a single-bit D/A converter can achieve high linearity because a single-bit D/A converter is inherently linear. However, the output signal waveform from a single-bit D/A converter is a square wave with a large amplitude as well as steep slopes, and hence contains considerable noise power outside the signal band. This power has to be removed by the following analog smoothing filter. Since any analog circuit has some nonlinearities and the effects of the nonlinearities are dependent on the signal fed into the filter, the fast-slewing large input signal from the single-bit D/A converter to the smoothing filter makes the design of the smoothing filter with the required linearity very difficult. The overall performance of oversampled D/A converters is usually limited by the harmonic distortion caused by nonlinear effects in the analog circuitry [17]. In addition,

the noise power outside the signal band which needs to be removed by the smoothing filter is large. This makes the smoothing filter more complex and thus more likely to possess nonlinear effects.

To ease the design of the analog filter and to increase the resolution without increasing the oversampling ratio, a multibit internal D/A converter can be used in an oversampled D/A converter instead of a single-bit one. The added bits not only add to the resolution and the dynamic range of the final system, but also greatly reduce the out-of-band quantization noise and the harmful limit-cycle effect [18]. The output signal waveform from a multibit D/A converter is a signal with small increments from sample to sample [19].

The above discussion assumed that the internal multibit D/A converter is ideal. If the internal D/A converter is not an ideal one and it is directly placed in the signal path, the nonlinearity error of the multibit D/A converter will appear in the system output directly without any shaping. This will introduce harmonic distortion and extra noise into the signal band which greatly degrade the system performance [19].

Several techniques have been developed to overcome this difficulty. One technique is to implement the internal multibit D/A converter by converting the digital number into a width-modulated pulse train [17]. This technique requires a very fast clock signal and associated fast circuitry, with a clock frequency $2^M Rfs$, where

M is the bit resolution of the internal multibit D/A converter and R is the oversampling ratio. While this method can achieve high linearity, the output of the internal D/A converter is still a fast slewing pulse train. Another technique is to store the actual nonideal output values of the multibit D/A converter in a RAM and use these data to correct the nonlinearities of the multibit D/A converter digitally in the noise-shaping loop [20][21]. This process eases the design problems of the analog filter but it requires an extra calibration time period in the noise-shaping loop as well as added hardware for the necessary calibration process.

In this research, another technique is proposed to achieve multibit internal D/A conversion without placing the multibit D/A converter in the signal path. The system uses a 3-level and a multibit (m -level) internal D/A converter. The 3-level D/A converter is used in a path called the *signal path* and the multibit D/A converter is used in a path called the *correction path*. This technique overcomes some of the major disadvantages of the techniques for achieving multibit internal D/A conversion described above.

3.2 Dual-Quantization Oversampled D/A Converters

To help explain the basic ideas behind the proposed technique, a general structure of the dual-quantization oversampled D/A converter is shown in Figure 3.1.

In this figure, the basic noise-shaping loop and the correction path noise-shaping loop can be any structure with first, second or higher-order noise-shaping characteristics.

The L -bit digital quantizer is usually a 2-level (single-bit) or 3-level one. It requires a 2-level or 3-level D/A converter following the noise-shaping loop, which can be easily implemented with high linearity.

The path developing signal y_1 is the *signal path*. It contains the L -bit D/A converter and is used to convert the input digital signal in a linear manner to its analog form. The path developing signal y_2 is the *correction path*. It contains the M -bit D/A converter and is used to cancel the quantization error of the L -bit quantizer e_L so that only the much smaller highpass-filtered M -bit quantization error e_M and the high-pass filtered M -bit D/A converter nonlinearity error d_M are present in the output y along with the input signal x .

In the linearized model, the basic noise-shaping loop can be characterized by the z -transforms of its two outputs, u and v . Let the z -transforms of the signals be denoted by the capital letters, we obtain

$$U = H_S X + H_N E_L \quad (3.1)$$

$$V = H_X X + H_{EL} E_L \quad (3.2)$$

The correction path can be characterized by

$$\begin{aligned}
W &= H_V V + H_{EM} E_M \\
&= H_V H_X X + H_V H_{EL} E_L + H_{EM} E_M
\end{aligned} \tag{3.3}$$

The final output is

$$\begin{aligned}
Y &= H_1 U + D_L + H_2 H_3 W + H_3 D_M \\
&= (H_1 H_S + H_2 H_3 H_V H_X) X + (H_1 H_N + H_2 H_3 H_V H_{EL}) E_L \\
&\quad + H_2 H_3 H_{EM} E_M + H_3 D_M + D_L
\end{aligned} \tag{3.4}$$

The L -bit D/A converter in the signal path must be implemented with high linearity such that comparing with the other terms in the right hand side of the equation (3.4), D_L is negligible. Thus

$$D_L \approx 0 \tag{3.5}$$

Any arithmetic operation in H_1 will increase the wordlength of the digital signal, which will increase the number of bits needed for the following L -bit D/A converter and thus makes the high linearity requirement on this D/A converter difficult to fulfill. Hence, H_1 is chosen to be $H_1 = z^{-k}$, where k delays balance the delays in the correction path.

If the error e_L is to be completely cancelled in the final output y , then we have

$$H_1 H_N + H_2 H_3 H_V H_{EL} = 0 \tag{3.6}$$

The final output is

$$Y=(H_1 H_S+H_2 H_3 H_V H_X)X+H_2 H_3 H_{EM} E_M +H_3 D_M \quad (3.7)$$

The above equations are the two basic design equations for the dual-quantization oversampled D/A converter.

The choice of the two noise-shaping loops, the functional blocks H_2 and H_3 , and of the number of bits in the D/A converters is dependent on the applications as well as the available technology. Nevertheless, some basic design principles can be stated.

1) The two noise-shaping loops, and H_1 and H_2 are digital circuits. They are flexible and their complexity is not a major concern.

2) The M -bit D/A converter can be implemented in a pipelined structure since the D/A converter is not in any feedback loop. Its latency can be balanced in the signal path by the delays in block H_1 .

3) The structure of H_2 should be simple since any arithmetic operation in H_2 may increase the wordlength and introduce truncation errors.

4) H_3 should be as simple as possible because it is implemented by an analog circuit.

5) H_3 should be able to attenuate the error d_M such that the in-band noise power contributed by this error is equal to or less than that contributed by the error e_M , which is attenuated by $H_2 H_3 H_{EM}$. Otherwise, increasing the number of bits in the correction path

will only reduce the out-of-band noise and the in-band noise will be dominated by the error d_M .

There are some other design considerations which will be discussed further in the following design example.

3.3 A Design Example

In this section, a design example is presented to verify the validity of the proposed technique and to illustrate some design issues for dual-quantization oversampled D/A converters.

The basic objective in this example is to design a dual-quantization oversampled D/A converter with a second-order, 5-bit internal D/A conversion noise shaping characteristics. The oversampling ratio is chosen to be 128. The resulting system will be compared with the standard second-order oversampled D/A converter with a single-bit as well as with an ideal 5-bit D/A converter.

3.3.1 Signal path

From equation (3.7), to obtain a second-order noise shaping of the error e_L , the following equation must hold

$$H_2 H_3 H_{EM} = (1 - z^{-1})^2 \quad (3.8)$$

If we chose the input to the correction path to be just the negative of the quantization error e_L , i.e., $V = -E_L$, then

$$H_X = 0, \quad H_{EL} = -1 \quad (3.9)$$

Since $H_1(z) = z^{-k}$, where the value of k depends on the delay in the M -bit D/A converter, we can let $k=0$ as an initial design parameter, then

$$H_1 = 1 \quad (3.10)$$

Thus, from equations (3.6), (3.8), (3.9) and (3.10), we obtain

$$H_N H_{EM} = (1 - z^{-1})^2 H_V \quad (3.11)$$

If we chose $H_V = 1$, which means that the correction path noise-shaping loop will not affect the signal fed into it, we can see from equation (3.11) that the noise-shaping task can be shared by the basic noise-shaping loop and the correction path noise-shaping loop. Because the cancellation of the L -bit quantization error relies on the accuracy of the correction path which contains analog circuitry, the error will not be completely cancelled due to the analog circuit nonidealities. So, it is advantageous to have a second-order noise shaping in the basic noise-shaping loop so that the uncanceled L -bit quantization error e_L in the final output y will not become a dominant noise source.

Based on the above discussion, a second-order error feedback noise-shaping loop shown in Figure 2.6(b) was chosen as the basic noise-shaping loop. The z -transforms of its two outputs u and v (as indicated in Figure 3.1) are as follows

$$U = X + (1 - z^{-1})^2 E_L \quad (3.12)$$

$$V=-E_L \quad (3.13)$$

Other structures that have second-order noise-shaping characteristics may also be used.

3.3.2 Error correction path

The choice of the basic noise-shaping loop predetermined that the correction path noise-shaping loop should have the transfer functions

$$H_V=1, \quad H_{EM}=1 \quad (3.14)$$

To ease the design of the analog block H_3 , we chose $H_3=(1-z^{-1})$. This block can be easily implemented in a switched-capacitor circuit and it will suppress the nonlinearity error of the M -bit D/A converter. The circuit implementation and the limitations of this choice will be discussed in the next section.

With the above choices for H_{EM} and H_3 , H_2 can be obtained from equation (3.8)

$$H_2=(1-z^{-1}) \quad (3.15)$$

This digital operation following the M -bit digital quantizer will theoretically increase the wordlength from M bits to $M+1$ bits, which increases the number of bits needed in the following multibit D/A converter from M to $M+1$. This is equivalent to a loss of 6 dB in the signal-to-noise ratio (and the dynamic range). However, since the function $H_2=(1-z^{-1})$ does not in practice

increase the wordlength by one bit and the maximum value of the error e_L does not reach the full scale of the M -bit digital quantizer (these values can be found from the simulations), a scaling by a constant $k < 1$ can be used to optimize the amplitude of the signal feeding the M -bit digital quantizer so that the maximum output value from the output of the block $H_2 = (1 - z^{-1})$ is always in the range of M bits. Another scalar $1/k$ is used following the M -bit DAC to make the gain of the correction path the same as that of the signal path.

The complete system is shown in Figure 3.2. The z -transform of the analog output signal y is

$$Y = X + \frac{1}{k} (1 - z^{-1})^2 E_M + \frac{1}{k} (1 - z^{-1}) D_M \quad (3.16)$$

3.3.3. Analog differentiator

The successful design of the analog differentiator H_3 shown in Figure 3.1 is the key to the proposed dual-quantization D/A converter. In the previous section we discussed the design of this block, and chose $H_3 = (1 - z^{-1})$. In a real circuit implementation, the analog circuit nonidealities will result in both gain and phase errors in H_3 [22], which gives a nonideal transfer function of H_3

$$H_3 = (1 + \delta) [1 - (1 + \alpha) z^{-1}] = (1 + \delta) (1 - z^{-1}) + \alpha (1 + \delta) z^{-1} \quad (3.17)$$

where δ corresponds to a gain error and α corresponds to a phase error.

We can see from equation (3.17) that the phase error α will introduce first-order-shaped errors E_L , E_M and unshaped error D_M directly into the system output. Thus, this error has to be very small in order to keep it from becoming the dominant error source in the system. This requirement is fulfilled by using a single capacitor to implement H_3 . In such an implementation, the needed zero at $z=1$ is perfectly realized, thus $\alpha \approx 0$. One such circuit is shown in Figure 3.3. In the figure, the capacitor C_1 is the capacitor used to implement the differentiator $H_3=(1-z^{-1})$. The signals shown correspond to the signals shown in Figure 3.2.

The main nonideality effects of this circuit affecting the cancellation of e_L is the capacitor mismatch between the capacitor C_1 and the capacitors implementing the 3-level D/A converter.

The uncanceled terms in the output y which result from the gain error is

$$\delta (1 - z^{-1}) [D_M + (1 - z^{-1})(-E_L + E_M)]$$

Assume first that the errors contributed by d_M and e_M are negligible compared to that contributed by e_L . Then, the uncanceled error term contributed by e_L is the second-order highpass filtered noise, which can be expressed as

$$\delta (1 - z^{-1})^2 E_L$$

Using the same method as we used in section 2.3.3 for calculating the in-band signal-to-noise ratio, we can obtain the in-band noise power corresponding to the above error term

$$\delta^2 \pi^4 e_{Lrms}^2 / 5R^5$$

where R is the oversampling ratio. On the other hand, from equations (2.3) and (2.4), the in-band noise power contributed by e_M is

$$\pi^4 e_{Mrms}^2 / 5R^5$$

Thus, as long as

$$|\delta| < \frac{e_{Mrms}}{e_{Lrms}} \quad (3.18)$$

the error contribution due to capacitor mismatch will not be a dominant noise source.

Since the two D/A converters must have the same gain in order to cancel the error e_L in the output y , the maximum input digital numbers to the two D/A converters must correspond to the same maximum output value of the two D/A converters, which is V_{ref} . Thus, the two digital quantizers must have the same maximum output values. For a 33-level and a 3-level digital quantizer, the above requirement gives that $|\delta| < 1/16$ from equation (3.18). This corresponds to an approximately 6% allowable capacitor mismatch (see Figure 3.7), which poses no practical problem.

Simulation results also confirmed that a 1% capacitor mismatch has very little effect on the output SNR value. Finite opamp dc gain A is even less of a problem since it does not affect the error

cancellation but merely introduces a common gain error for both paths.

A second important design parameter is the linearity requirement of the M -bit D/A converter. Optimum design requires that the noise power in the signal band contributed by d_M , the M -bit DAC nonlinearity, be equal to or less than that contributed by e_M . Since d_M is first-order noise-shaped, its power in the signal band is

$$\pi^2 d_{Mrms}^2 / 3R^3$$

In order for the D/A converter nonlinearity not to be a dominant noise source, we must have

$$\pi^4 e_{Mrms}^2 / 5R^5 > \pi^2 d_{Mrms}^2 / 3R^3$$

and hence

$$\frac{d_{Mrms}}{e_{Mrms}} < \frac{\sqrt{0.6\pi}}{R} \quad (3.19)$$

Since the two D/A converters must have the same maximum output values for a fixed reference voltage as we discussed above, we obtain

$$\frac{d_{Mrms}}{e_{Mrms}} \leq \frac{2^{M-1}}{2^{N-1}} \quad (3.20)$$

where N is the M -bit D/A converter linearity expressed in bits. Hence, equation (3.20) leads to the condition

$$N > \log_2 \left[\frac{R}{\sqrt{0.6\pi}} (2^{M-1} + 1) \right] \quad (3.21)$$

For an oversampling ratio of 128, the linearity of the M -bit D/A converter needs to be higher than $M+6$ bits. When $M=5$, a D/A converter with 11-bit linearity is needed. This is not easy to achieve for a parallel D/A converter. However, since the M -bit DAC can be implemented with a pipelined architecture, and such a circuit can have high linearity (over 12 bit linearity was reported in [23]), this implementation is feasible.

This design becomes more attractive in high speed applications where the oversampling ratio is low. For example, when $R=32$, a 5-bit D/A converter with 9-bit linearity is adequate for a 14-bit overall resolution.

3.3.4 Simulation Results

The performance of the system shown in Figure 3.2 was simulated extensively under the following conditions:

1) The output levels of the 3-level digital quantizer in the basic noise-shaping loop were represented by integer numbers $\pm 2^{19}$ and 0. The characteristics of the 3-level digital quantizer are shown in Figure 2.3, where now $N=19$. The subsequent D/A converter had also three output levels: $\pm V_{ref}$ and 0 volts.

2) The M -bit digital quantizer used in the correction path had 33 output levels. They were represented by integer numbers: 0, $\pm 1 \cdot 2^{15}$, $\pm 2 \cdot 2^{15}$, $\pm 3 \cdot 2^{15}$, ..., $\pm 16 \cdot 2^{15}$. The characteristics of the 33-

level quantizer are shown in Figure 2.4 with $N=19$. The M -bit D/A converter following the block $H_2=(1-z^{-1})$ also had 33 output levels: $0, \pm 1 \cdot 2^{-4}V_{ref}, \pm 2 \cdot 2^{-4}V_{ref}, \dots, \pm 16 \cdot 2^{-4}V_{ref}$,

3) The sampling frequency was assumed to be $f_s=16,384$ Hz. The sine signal discussed in section 2.4.2 was used as the input signal. Its frequency was $f_t=13$ Hz and its amplitude was $A_m=2^{18}$, which when referred to the maximum quantizer 2^{19} , it was $20\log_{10}(2^{-19}A_m)$ (dB)=-6 dB.

4) The nonlinearity of the 33-level D/A converter was included by generating random errors in the M -bit D/A converter output levels. The RMS value of the errors was 1.5% of the level spacing, corresponding to about 11-bit linearity;

5) The inaccuracies of the analog function $H_3=(1-z^{-1})$ was also considered by using an inaccurate function $H_3=(1+\delta)(1-z^{-1})$, with $\delta=\pm 0.01$, corresponding to 1% capacitor mismatch.

The results of the simulations are given in Figures 3.4~3.6. Figure 3.4 shows the output signal-to-noise ratio as a function of the input sine-wave amplitude for the uncorrected system where the M -bit correction path is eliminated, as well as for the corrected system with ideal and nonideal M -bit D/A converters. This figure shows the correction path adds about 20 dB to the SNR and this improvement is tolerant of DAC nonlinearity. A peak SNR of 115 dB (about 19 bits) is achieved with a 5-bit DAC possessing 11-bit linearity. Figure 3.5 shows the system output spectra for both the corrected and uncorrected systems. These figures again

show the 20 dB noise reduction which results from using the correction scheme. The reduced out-of-band noise is an especially important feature, as it lowers the attenuation requirements on the analog filter. Figure 3.6 shows the output signal waveforms of the system before and after correction. The sample-to-sample slew rate is greatly reduced as a result of employing the correction scheme (it is about 8 times smaller than that of the uncorrected one.) This feature also makes the design of the analog filter with a high linearity more feasible.

CHAPTER 4 CONCLUSIONS AND FUTURE RESEARCH

Oversampled data converters take full advantage of the high operating speed offered by modern integrated circuit technology while being insensitive to component mismatching. The practical importance of the oversampled data converter has been demonstrated in many implementations.

In the development of these data converters, both simulation tools and modulator structures play important roles. In this research, some fundamental simulation and analytical methods have been studied and used in developing novel oversampled D/A converters.

A dual-quantization method was proposed for implementing oversampled D/A converters with high linearity and high resolution. It is an alternative (and in many cases preferable technique) to existing oversampled D/A conversion techniques.

The dual-quantization D/A converter may be applied with various choices of noise-shaping functions, bit resolution of the internal D/A converters and oversampling ratio. The best choices are determined by the context of the application. For the purpose of illustration, a second-order oversampled D/A converter employing 3 and 33-level quantizers was examined with the oversampling ratio set to 128. The simulated performance of this converter achieved a peak SNR of 115 dB with 1% capacitor mismatch and an 11-bit DAC linearity.

The requirement on the M -bit DAC linearity is rather strict when the transfer function of the analog differentiator is $H_3=(1-z^{-1})$. The DAC linearity requirement can be reduced to near its bit resolution if the transfer function of the analog differentiator is $H_3=(1-z^{-1})^2$. Then, both M -bit digital quantization error e_M and the DAC nonlinearity error d_M are second-order highpass shaped. Unfortunately, this calls for more complex analog circuitry realizing H_3 . Investigation into implementation of the analog second-order differentiator $H_3=(1-z^{-1})^2$ will be left for future research work.

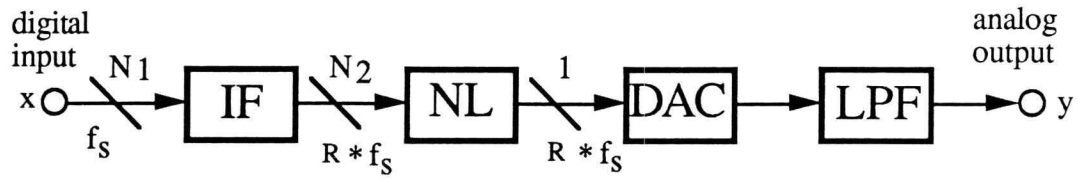


Figure 2.1 Oversampled D/A converter system

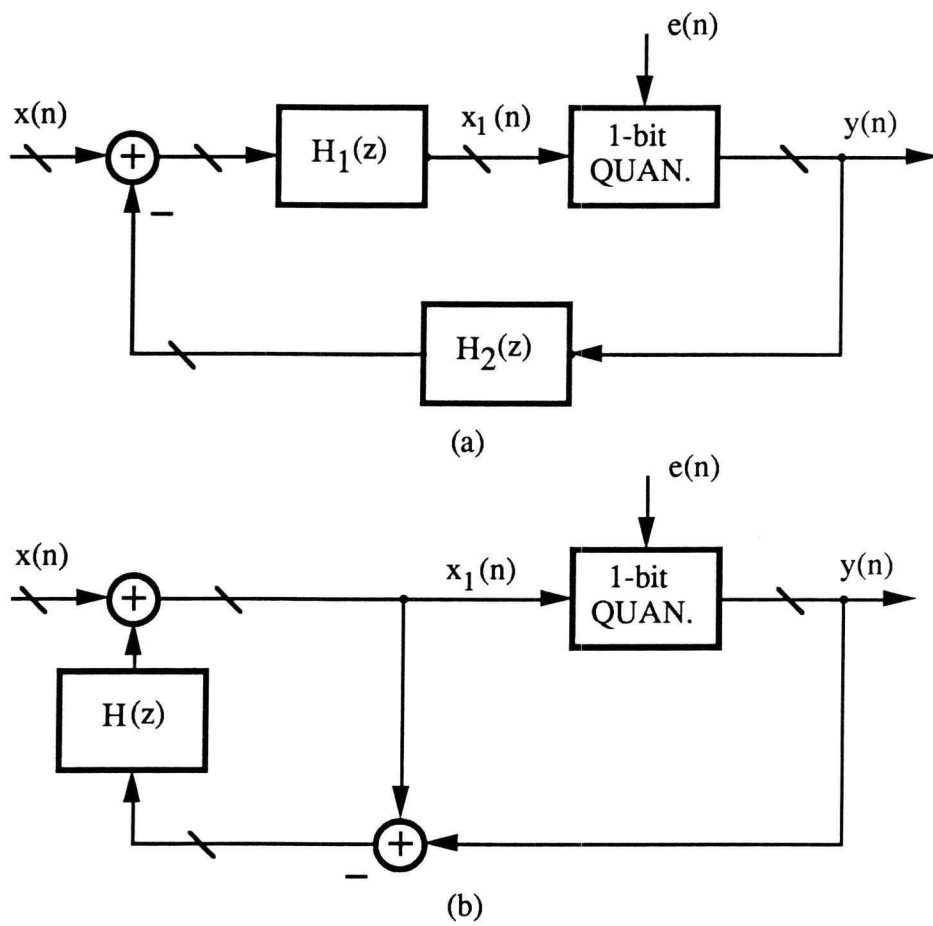


Figure 2.2 Digital noise-shaping loops
 (a) Delta-Sigma scheme
 (b) Error feedback scheme

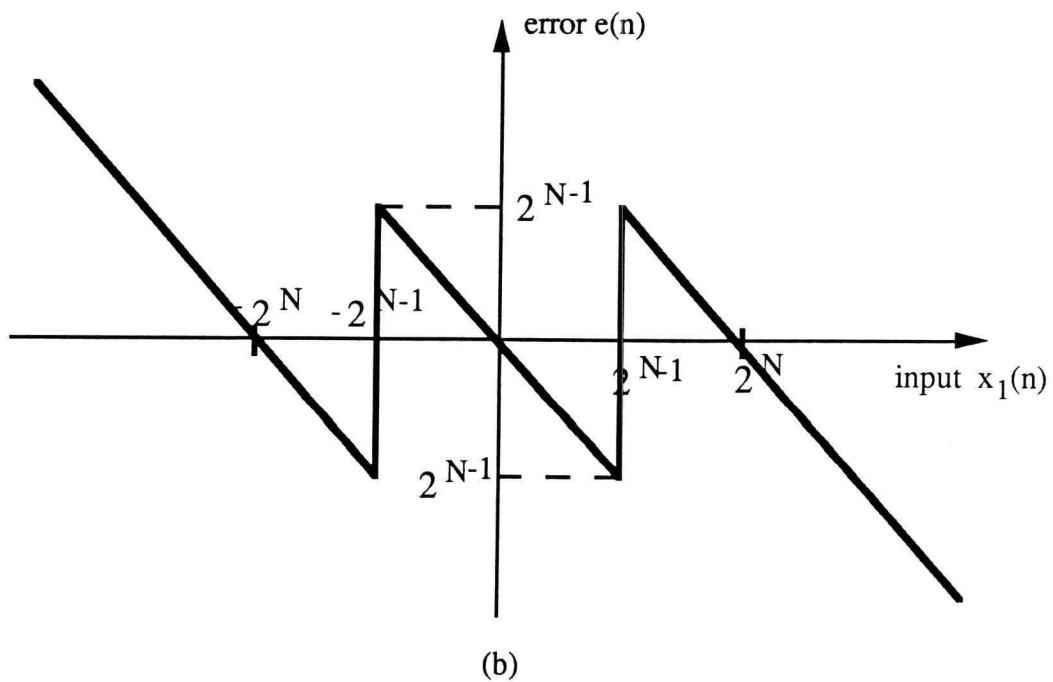
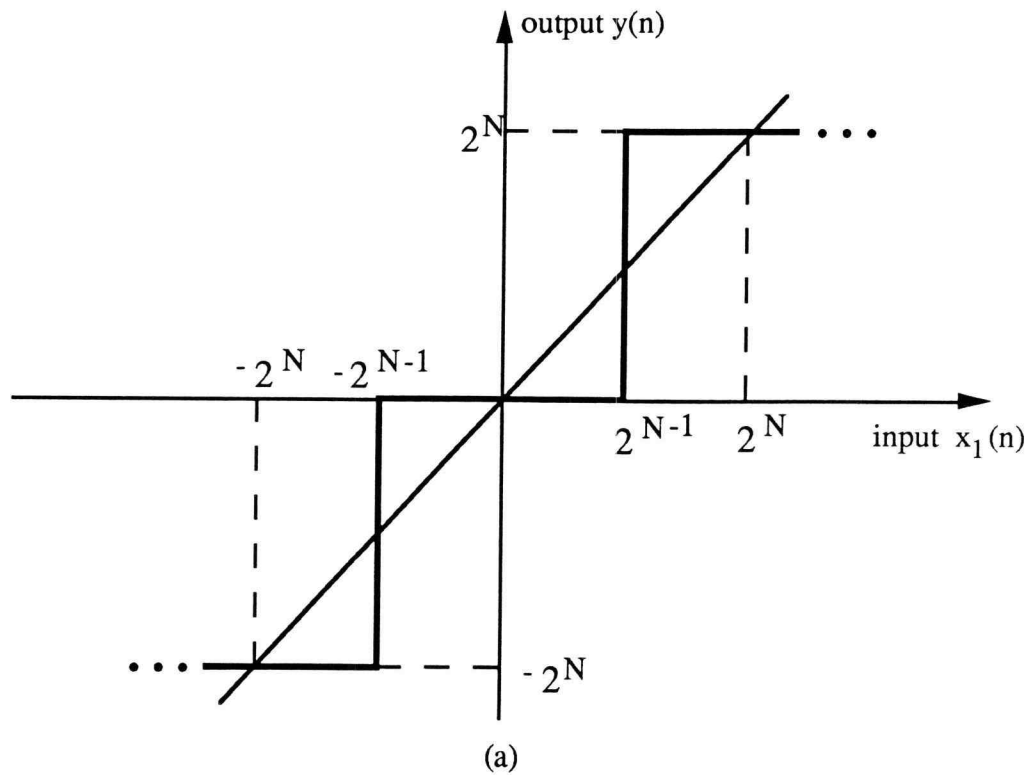


Figure 2.3 The characteristics of a 3-level digital quantizer (a) the input-output relationship (b) the error

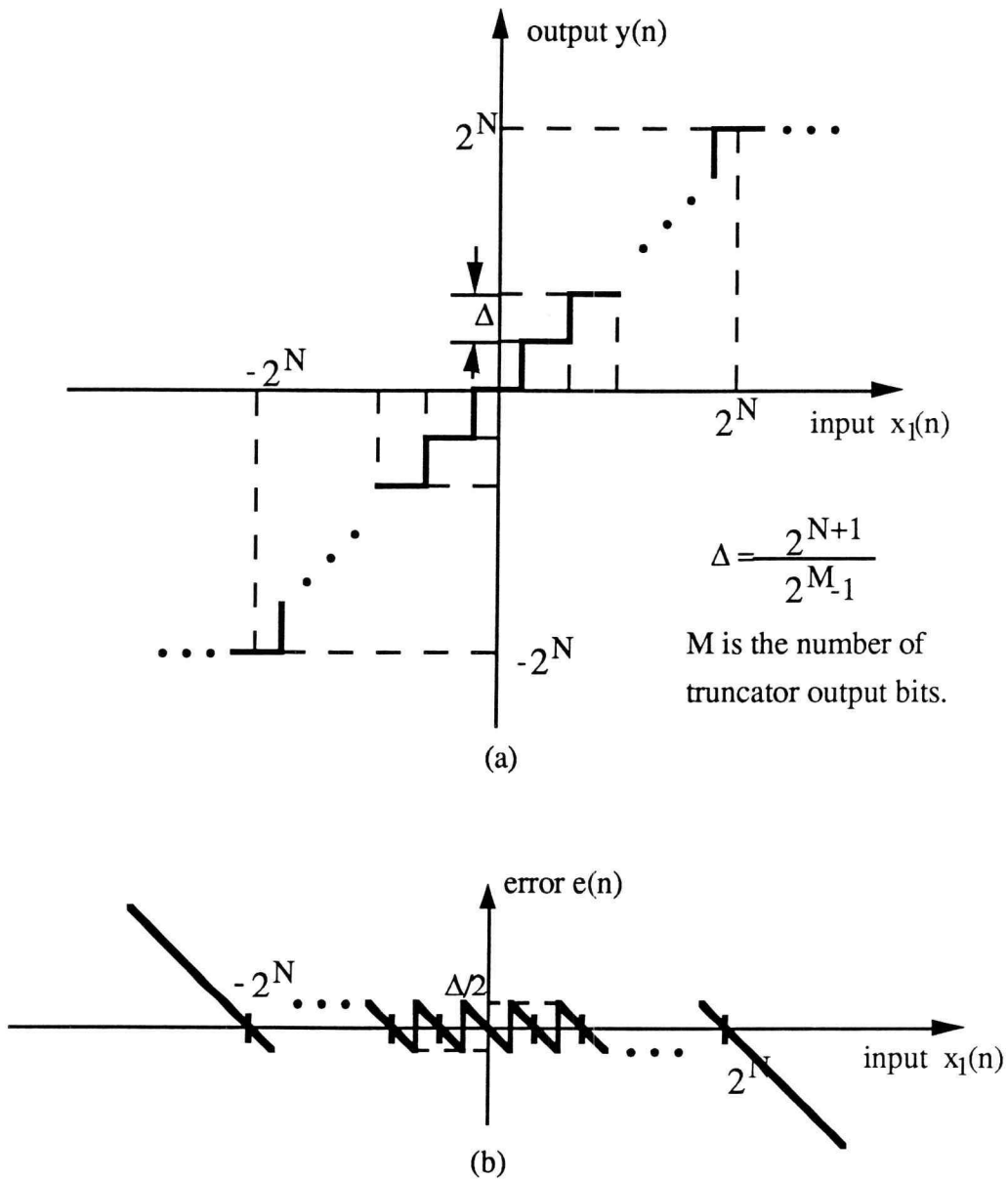


Figure 2.4 The characteristics of the M-bit digital quantizer; (a) the input-output relationship (b) the error

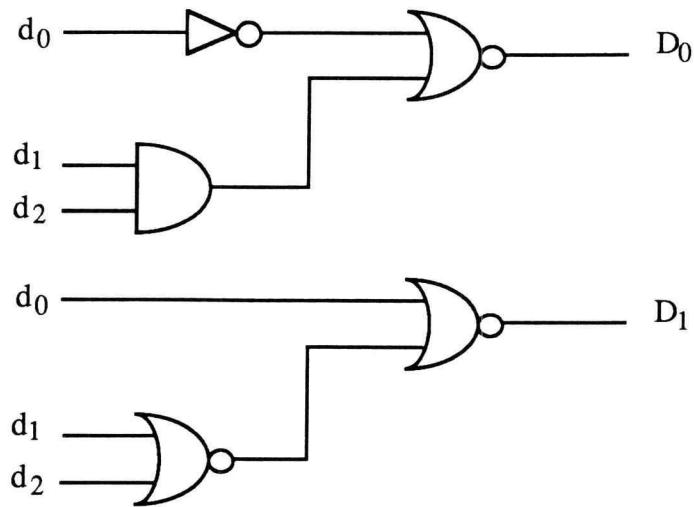


Figure 2.5 An implementation of the 3-level digital quantizer

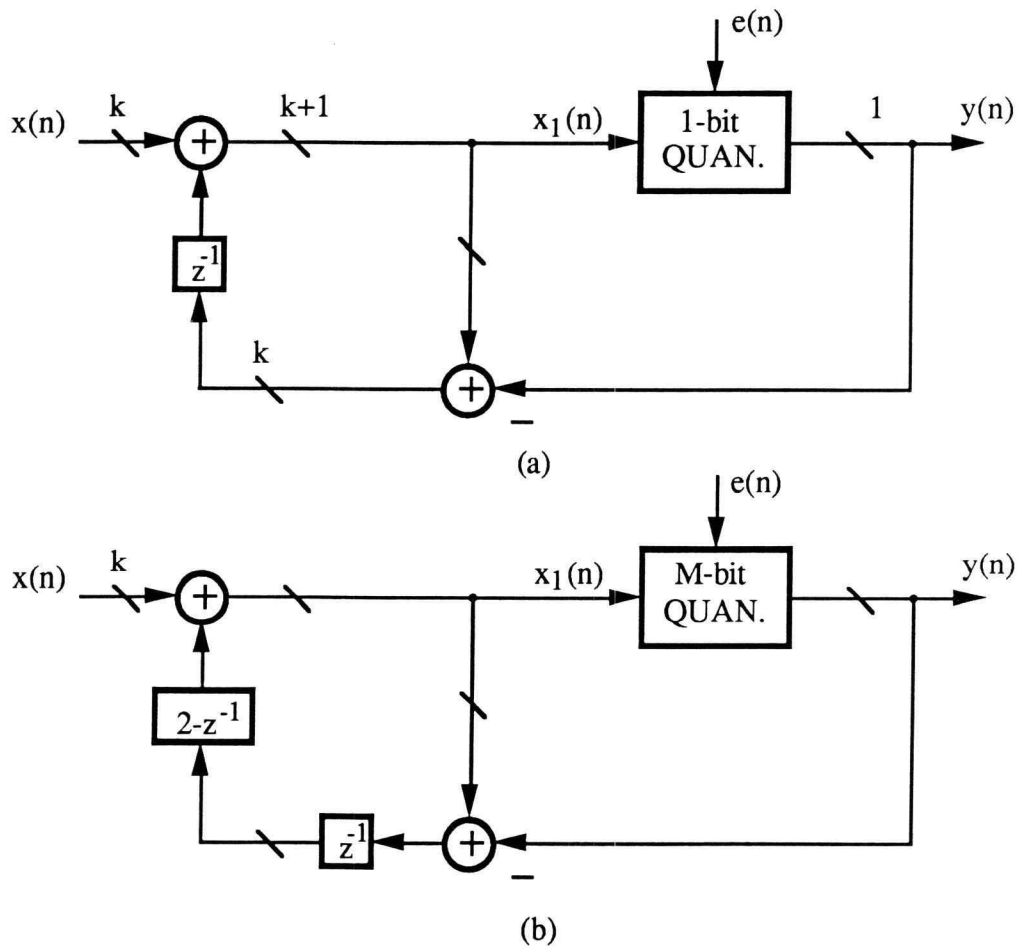


Figure 2.6 Error feedback digital noise shaping loops; (a) first-order (b) second-order

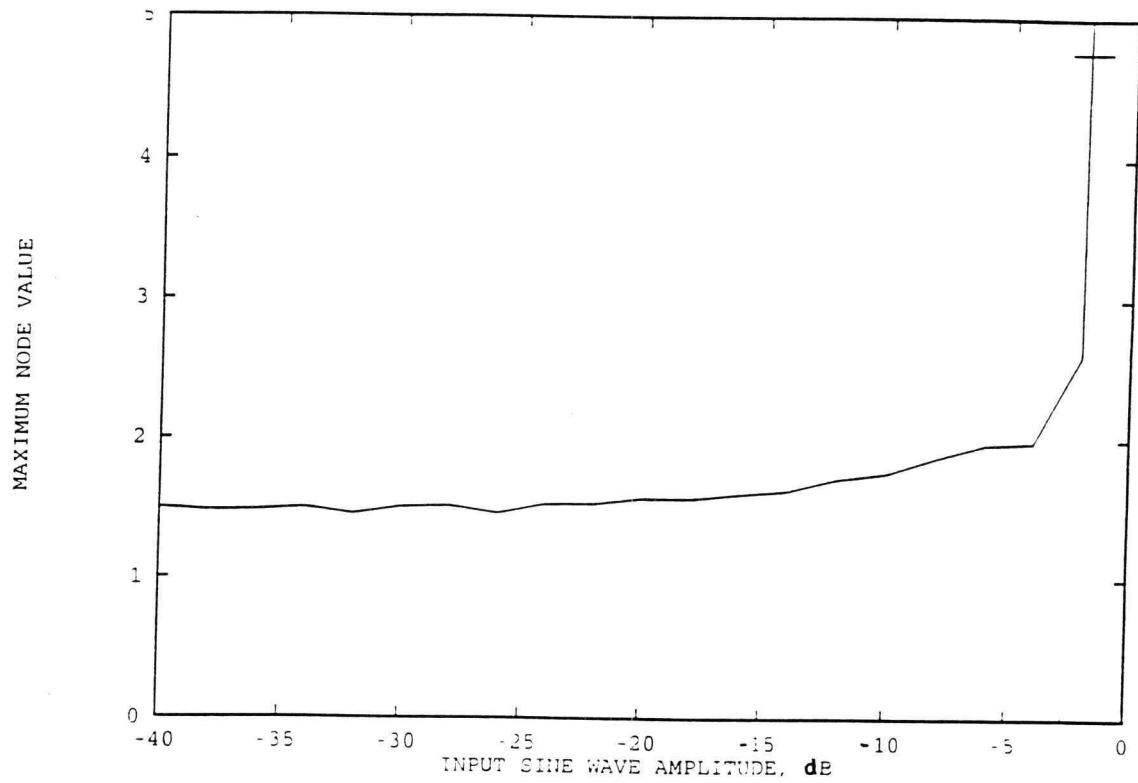


Figure 2.7 The maximum input value of to the 3-level digital quantizer of the system shown in Figure 2.6(b)

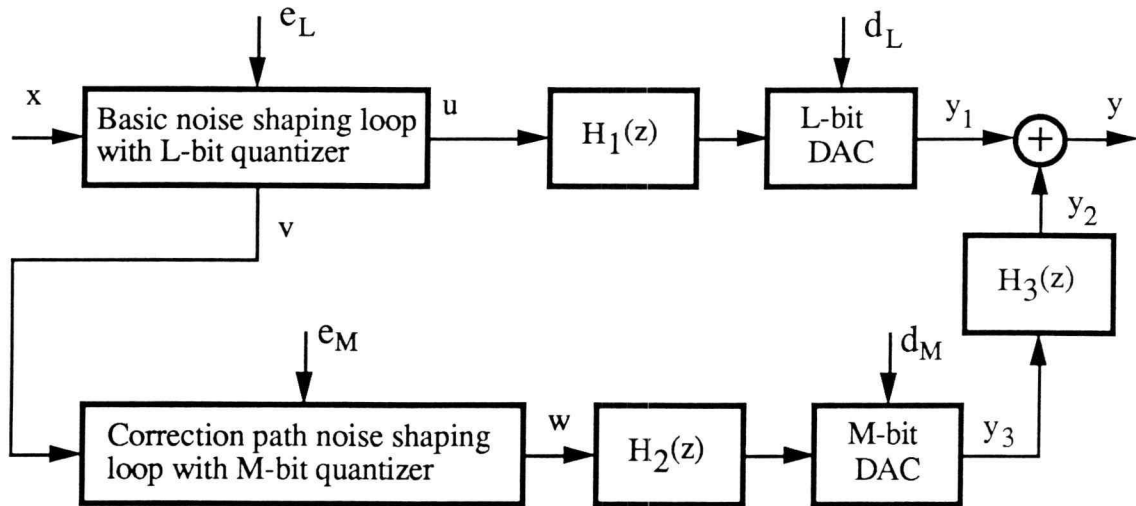


Figure 3.1 A general structure of the dual-quantization oversampled D/A converter

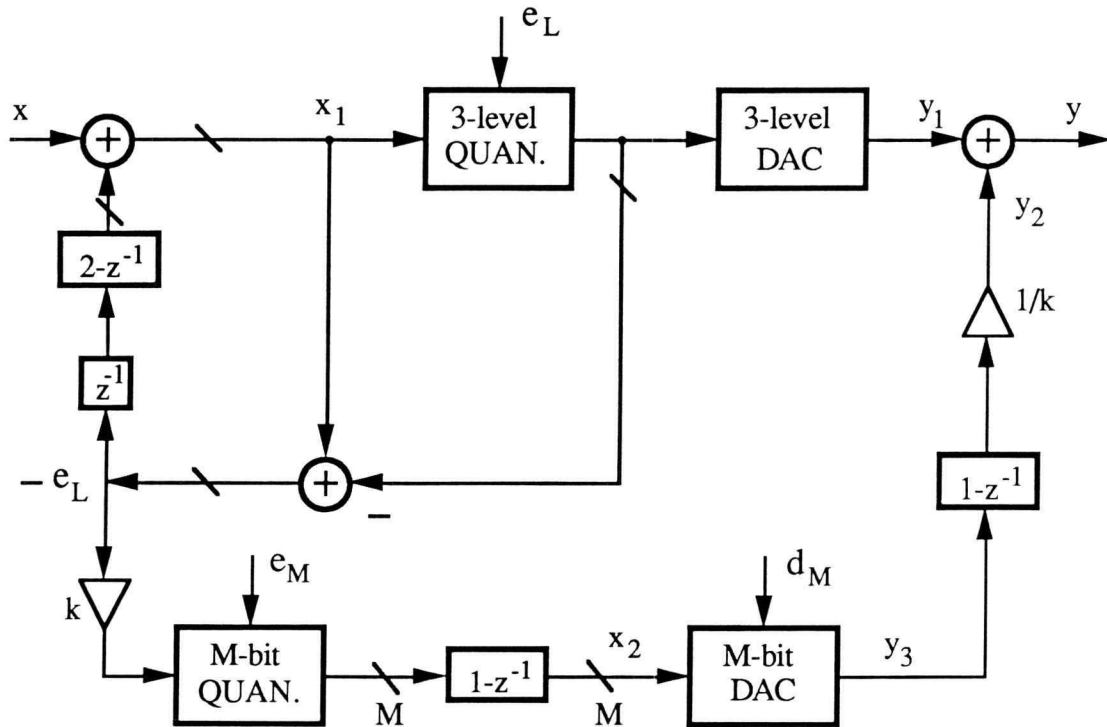


Figure 3.2 A practical implementation of the general structure shown in Figure 3.1

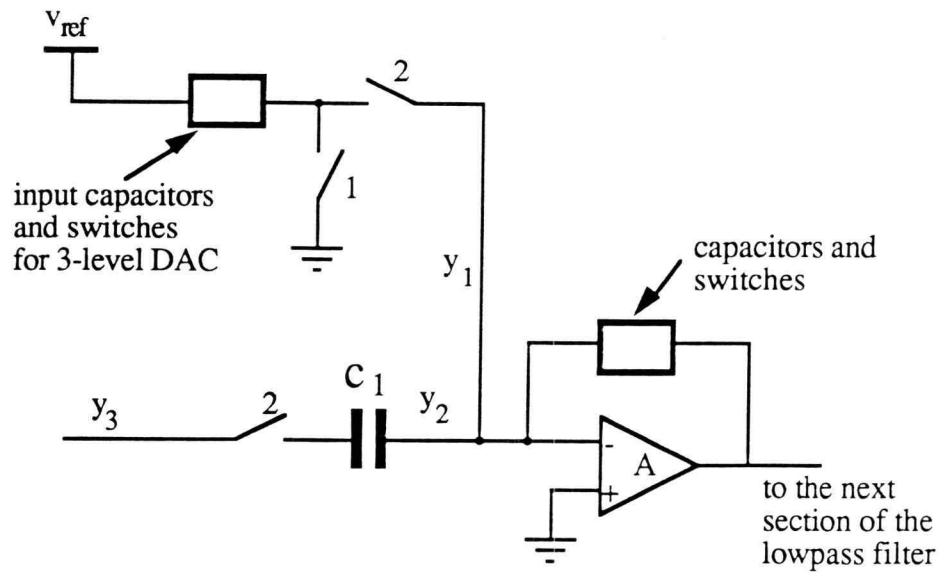


Figure 3.3 An SC circuit illustrating the realization of the first-order differentiator

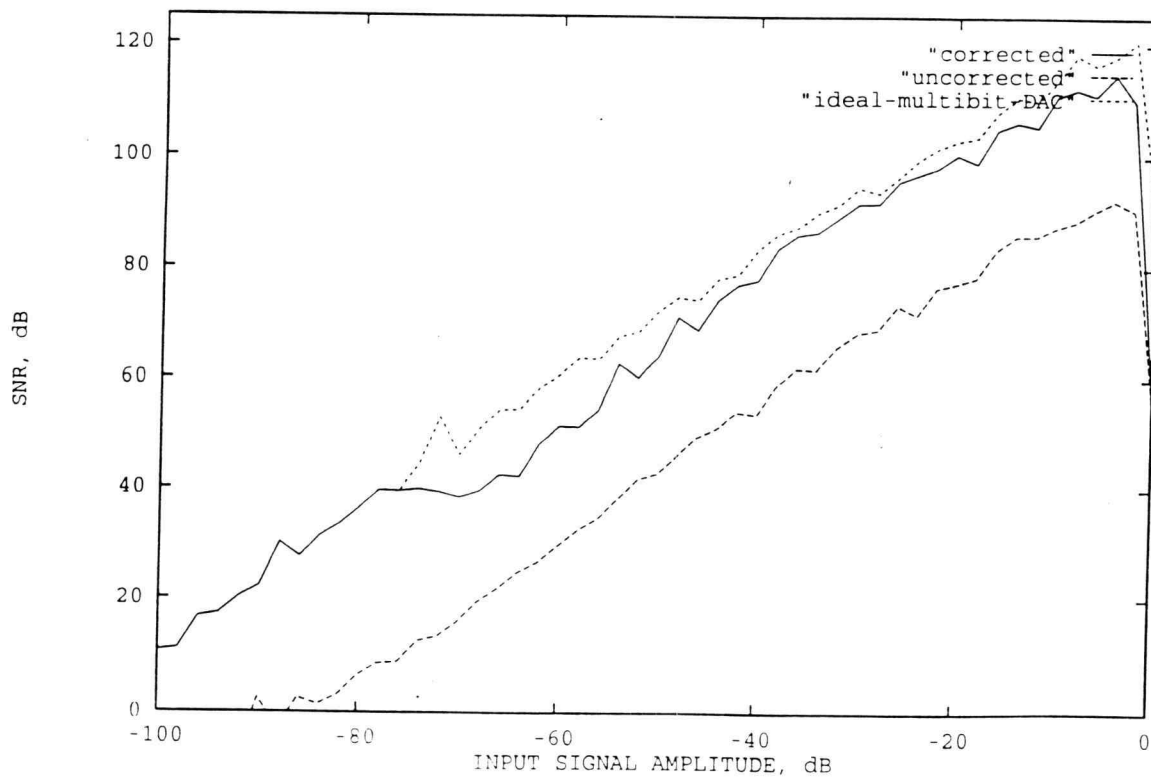
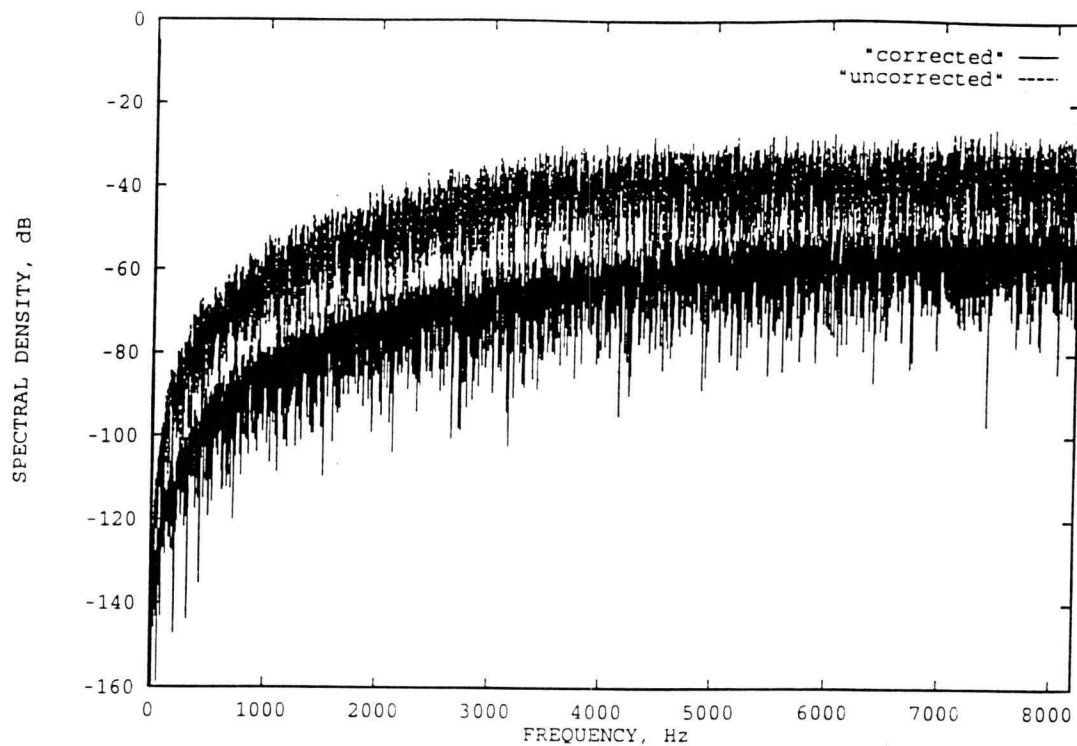
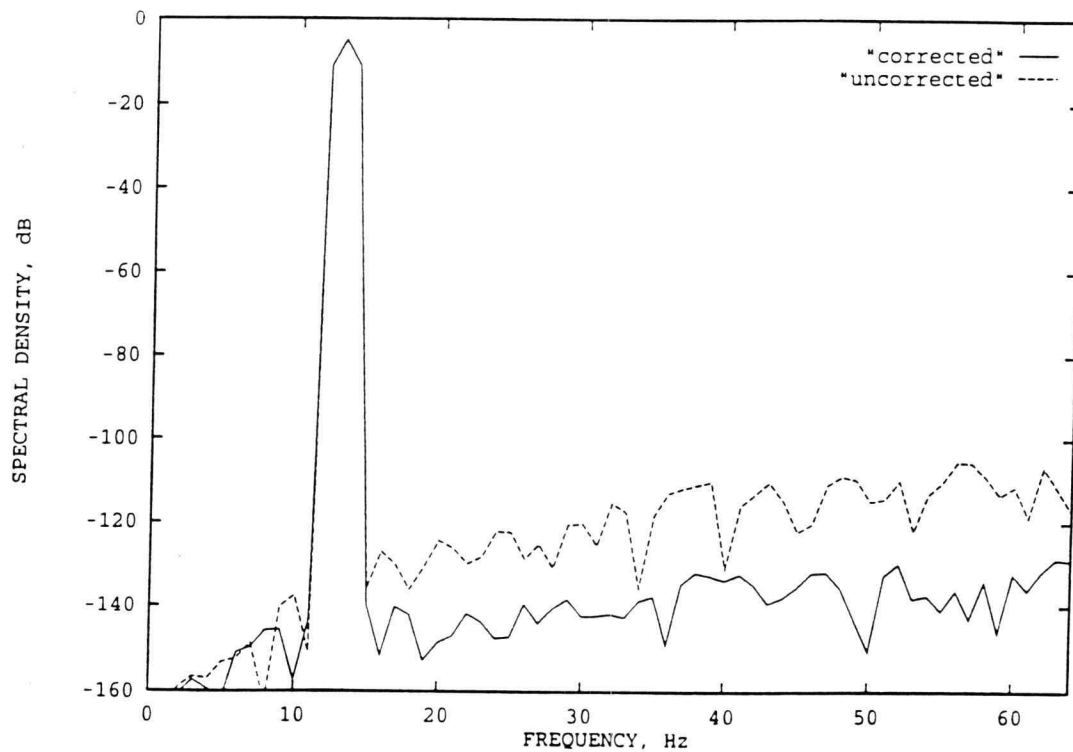


Figure 3.4 Simulation results: signal-to-noise ratio as a function of the input signal amplitude



(a)



(b)

Figure 3.5 Simulation results: output signal spectra: (a) the spectra inside the $f_s/2$ (b) the spectra in the passband for a oversampling ratio of 128

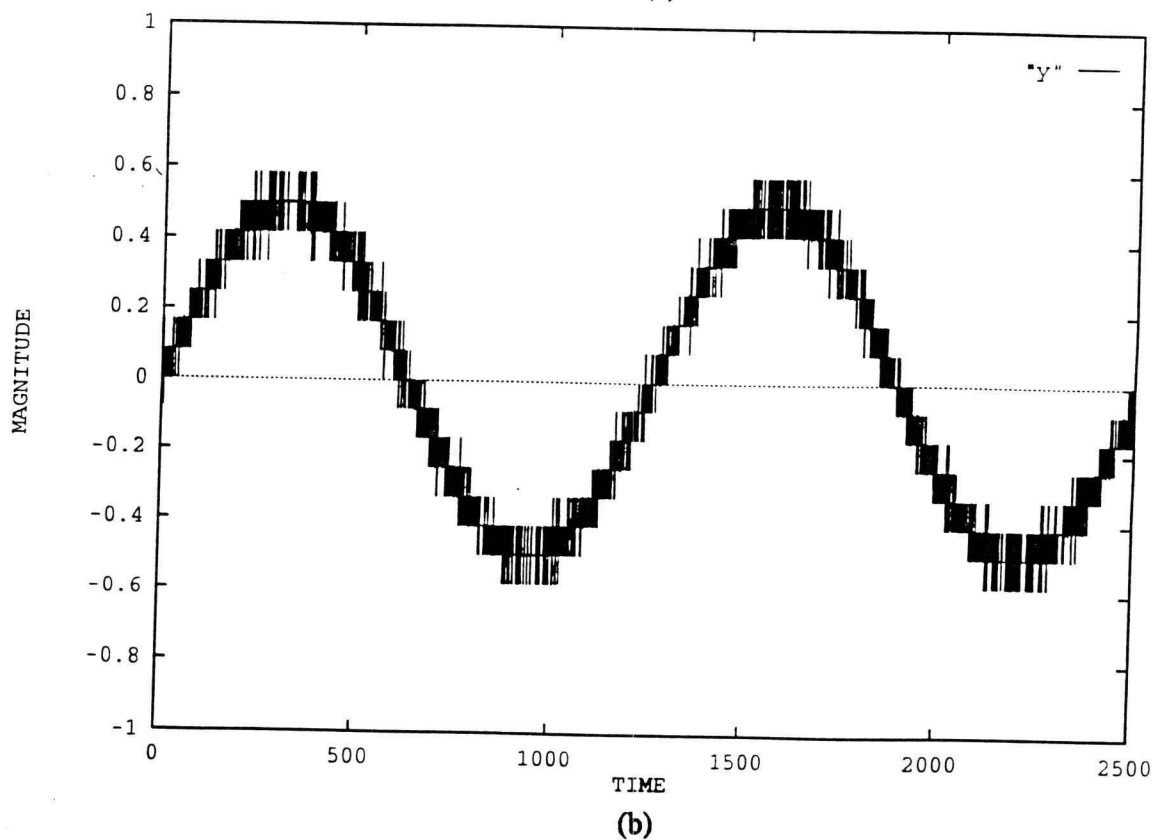
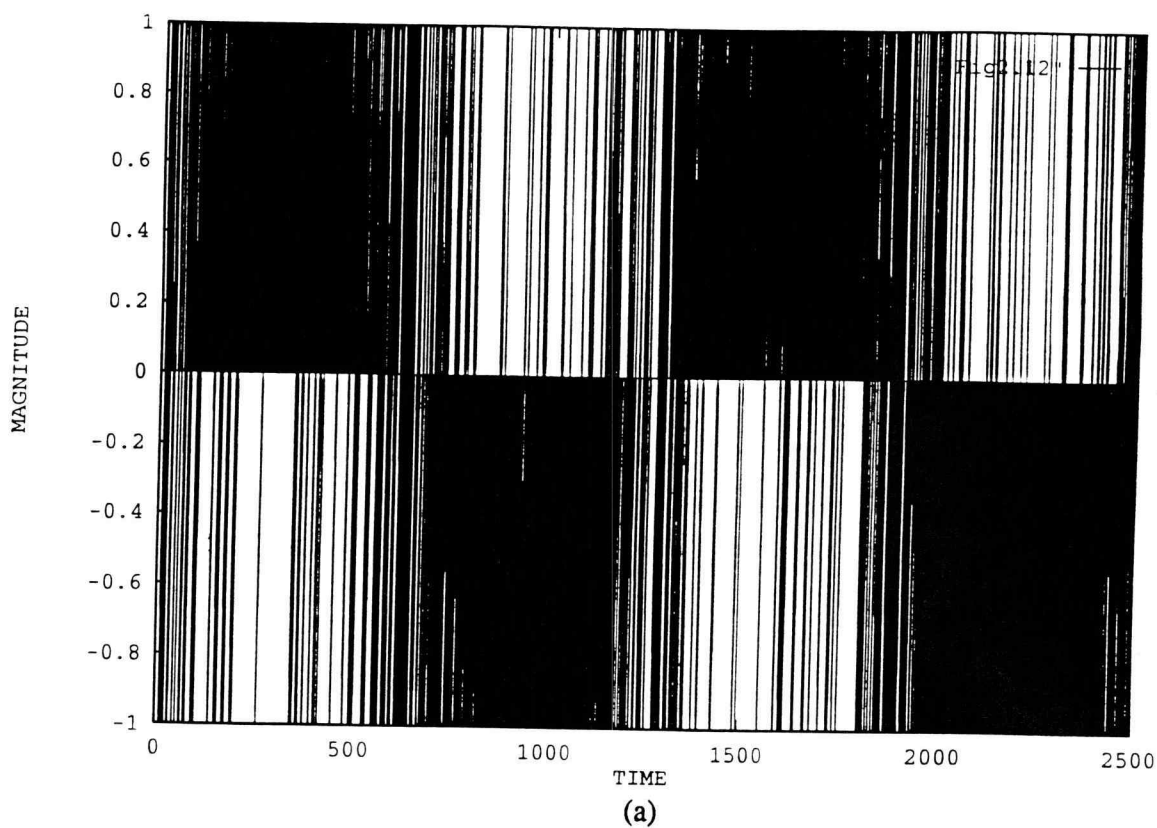


Figure 3.6 Simulation results: output signal waveforms: (a) from uncorrected system (b) from corrected system

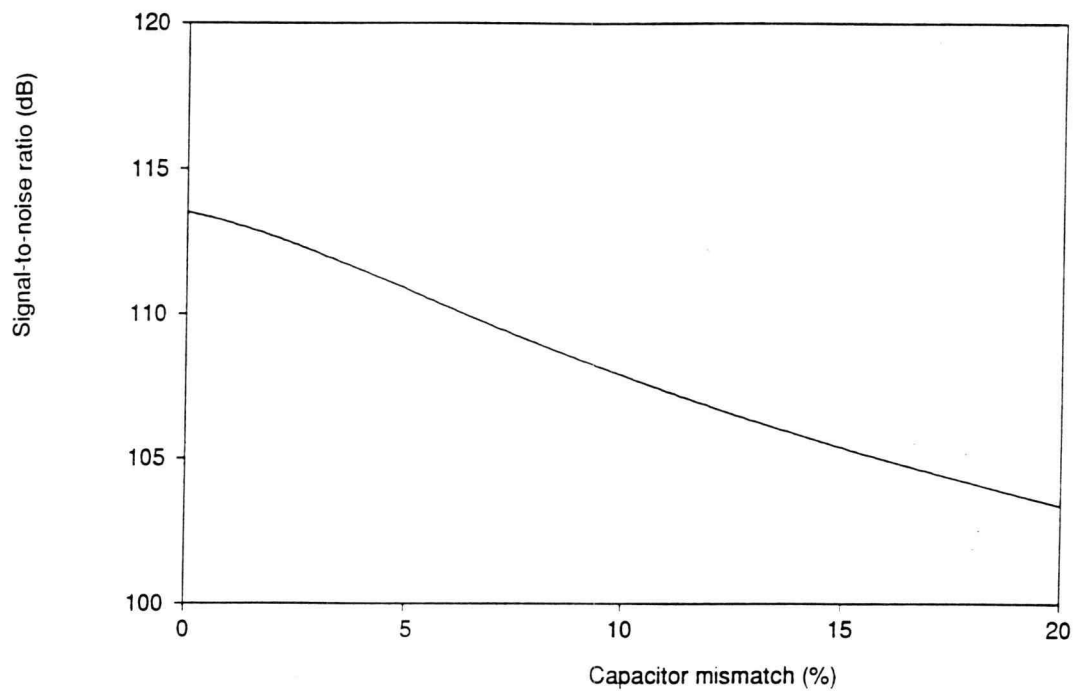


Figure 3.7 Effects of capacitor mismatch on signal-to-noise ratio

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