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Abstract approved: Redacted for Privacy

David J. Allstot

It has become customary in electrical engineering to think of signal processing in terms of voltage variables to the exclusion of current variables. This tendency has resulted in voltage signal processing circuits such as voltage-controlled voltage sources (VCVS) and voltage-mode operational amplifiers. However, the VCVS operational amplifier has several limitations which prevent high performance operation. One of these limitations is that the product of the closed loop -3dB bandwidth and the closed loop voltage gain is approximately a constant. Thus, for a typical internally compensated operational amplifier the closed loop -3dB bandwidth decreases as the closed loop voltage gain increases. By taking advantage of a current-controlled current source (CCCS) to form a current-mode operational amplifier, this limitation can be overcome.

A Universal CMOS Current-Mode Operational Amplifier

by

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Student

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Special thanks are due to Scott Williams for his constant encouragement, advice, and assistance throughout the last two years of my studies.

"The Wind Beneath My Wings" by Larry Henley and Jeff Silbar

It must have been cold there in my shadow,
to never have sunlight on your face.
You were content to let me shine, that's your way,
you always walked a step behind.

So, I was the one with all the glory,
while you were the one with all the strength.

It might have appeared to go unnoticed,
but I've got it all here in my heart.
I want you to know I know the truth, of course I know it,
I would be nothing without you.

Did you ever know that you're my hero,
and everything I would like to be?
I can fly higher than an eagle,
'cause you are the wind beneath my wings.

Thank you, thank you, thank God for you,
the wind beneath my wings.

For Mom and Debbie, who have always believed in me just a little bit more than I ever believed in myself.

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A UNIVERSAL CMOS CURRENT-MODE OPERATIONAL AMPLIFIER

Chapter 1. INTRODUCTION

Over the years, many amplifier designs have been manufactured that produce a controlled voltage output from a voltage input. A basic building block of these networks has been the voltage-mode operational amplifier, or voltage-controlled voltage source (VCVS). Thus, it has become customary for electrical engineers to think of analog signal processing solely in terms of voltage variables. This is unfortunate because there is often a demand in analog signal processing for circuits of well-defined current signal processing properties, for example, current-controlled current sources (CCCS), and current-mode operational amplifiers (op amps). In fact, current-based amplifier circuits can offer certain high-performance advantages, such as speed, bandwidth, and accuracy which make them preferable to voltage amplifier designs. This potential has been recognized by many circuit designers, as evidenced by the amount of research into the design and application of current-mode techniques over the last two decades. [1]

Most of the recently published current-mode circuit research utilizes the Gilbert translinear principle, [2] exploiting the linear relationship between transconductance and collector current in bipolar devices. It holds over many orders of magnitude and is in widespread use in a variety of analog

circuits such as multipliers, dividers, squarers, higher-power-function generators, geometry-correction systems for cathode ray tube displays, etc. The main distinguishing feature of a translinear circuit is that it uses an even number of forward biased p-n junctions arranged in one or more loops, with each loop having the same number of junctions connected in one polarity as the other. The translinear principle can be modified to analyze CMOS circuits, as will be discussed in chapter 2.

Currently, a great deal of research is being done on the application of current-mode techniques in operational amplifiers, filters, current conveyors, transconductance amplifiers, transresistance amplifiers, current followers, precision rectifiers, and peak detectors. However, in almost every application, a voltage-mode operational amplifier (VOA) is utilized with additional circuitry designed to sense the current the VOA draws from its supply rails to obtain a "current-mode" topology. Toumazou and Lidgey [1] summarize the use of this topology as follows:

> "Though it is somewhat ironic, we also show circuits which use VOAs to achieve current-mode performance can often, in turn, deliver an improved performance when configured as voltage amplifier circuits.
>
> Whilst the extended VOA approach to current-mode performance does work well, it is inherently limited by the voltage processing architecture."

Allen and Terry [3] were apparently the first researchers

to realize that a CCCS amplifier could be used to achieve a voltage amplifier having a -3dB frequency independent of the closed-loop voltage gain and an increased slew rate. Their original designs were implemented in bipolar technology. Thus, the move towards a true current-mode op amp is not only more direct and logical, it offers improved performance.

This thesis explores an entirely new design for a CMOS current-mode amplifier and analyzes in detail its potential in the areas of accuracy, gain, and bandwidth. The CMOS circuit, derived by modifying the Gilbert BJT translinear principle, is an appropriate building block in many of the circuits currently using the VOA supply-sensing technique. It offers the potential for increased accuracy, slew-rate, gain and bandwidth characteristics.

Chapter 2 examines the advantages and disadvantages of some past designs, explains the Gilbert translinear principle, and illustrates some of its applications.

In Chapter 3, the basic CCCS amplifier is constructed, and the experimental environment described. Then, both theoretical and experimental characteristics of the CCCS amplifier are presented.

Chapters 4 considers the accuracy, gain and bandwidth of the CCCS amplifier.

Chapter 5 discusses applications of the CCCS amplifier as an op amp and as a current conveyor and shows simulation results. Past designs are examined and compared to the new

design.

Finally, Chapter 6 presents a summary of conclusions.

Chapter 2. LITERATURE SEARCH

2.1 Background

In 1968, Smith and Sedra introduced the concept of the current conveyor [4] which is essentially a voltage/current-mode hybrid circuit. The versatility and high performance of the current conveyor make it a powerful building block, as confirmed by the wealth of literature inspired by it, including this work. Smith and Sedra developed the current conveyor using a two-port approach, Fig. 1. When input terminal y is connected to potential V, an equal voltage appears at x. In a dual manner, when a current I is forced into input x, an equal current flows through y, and is conveyed to z which is a high-impedance current source port. Moreover, the potential of input x, fixed by that of y, become independent of the current I forced into x. Likewise, the current I through input y, fixed by that through x, becomes independent of the voltage V applied to y. Described in terms of a hybrid, H, two-port notation, the relationship between terminals x and y with z grounded is

$$\begin{vmatrix} vx \\ iy \end{vmatrix} = \begin{vmatrix} 0 & 1 \\ 1 & 0 \end{vmatrix} \begin{vmatrix} ix \\ vy \end{vmatrix} \qquad (2.1)$$

$$H_{xy} = \begin{vmatrix} 0 & 1 \\ 1 & 0 \end{vmatrix}. \qquad (2.2)$$

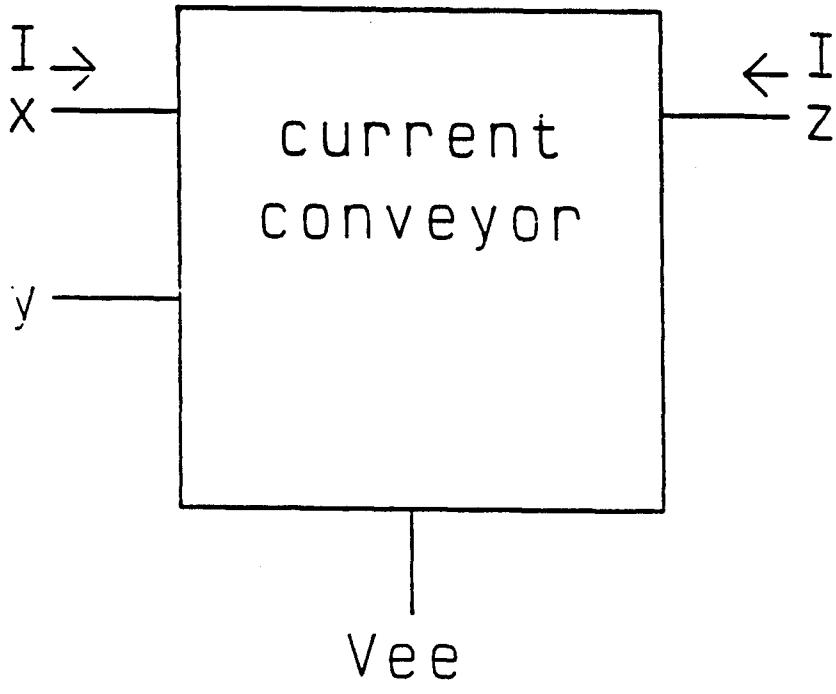

Figure 1. Two port representation of Smith and Sedra's current-conveyor.

and the relationship between terminals x and z with y grounded is

$$\begin{vmatrix} v_x \\ i_y \end{vmatrix} = \begin{vmatrix} 0 & 0 \\ 1 & 0 \end{vmatrix} \begin{vmatrix} i_x \\ v_z \end{vmatrix} \tag{2.3}$$

$$H_{xz} = \begin{vmatrix} 0 & 0 \\ 1 & 0 \end{vmatrix}. \tag{2.4}$$

The transfer characteristic of matrix H_{xz} (in 2.4) is clearly that of a CCCS.

Figure 2 shows Smith and Sedra's suggested first-order implementation of the current conveyor principle, which provides moderate accuracy and high speed.

The next step was to configure a VOA as a current conveyor to exploit its high performance properties. Figure 3 shows a traditional VOA current conveyor scheme. Although the voltage gain varies with rload, the current in the feedback path remains fixed assuming fixed vin and rref. The input impedance is low (rref) and nearly all the input current is drawn through the load by the negative feedback action. The input current differs from the load current only by the small amount flowing into the VOA. Even this small error is eliminated by using MOSFET inputs. One limitation to this approach is that the current driven load is not ground referenced, which would be desirable to assure a well-defined and easily accessible current flowing through the resistor.

The circuit of Fig. 4 developed by Howland [1] solves the

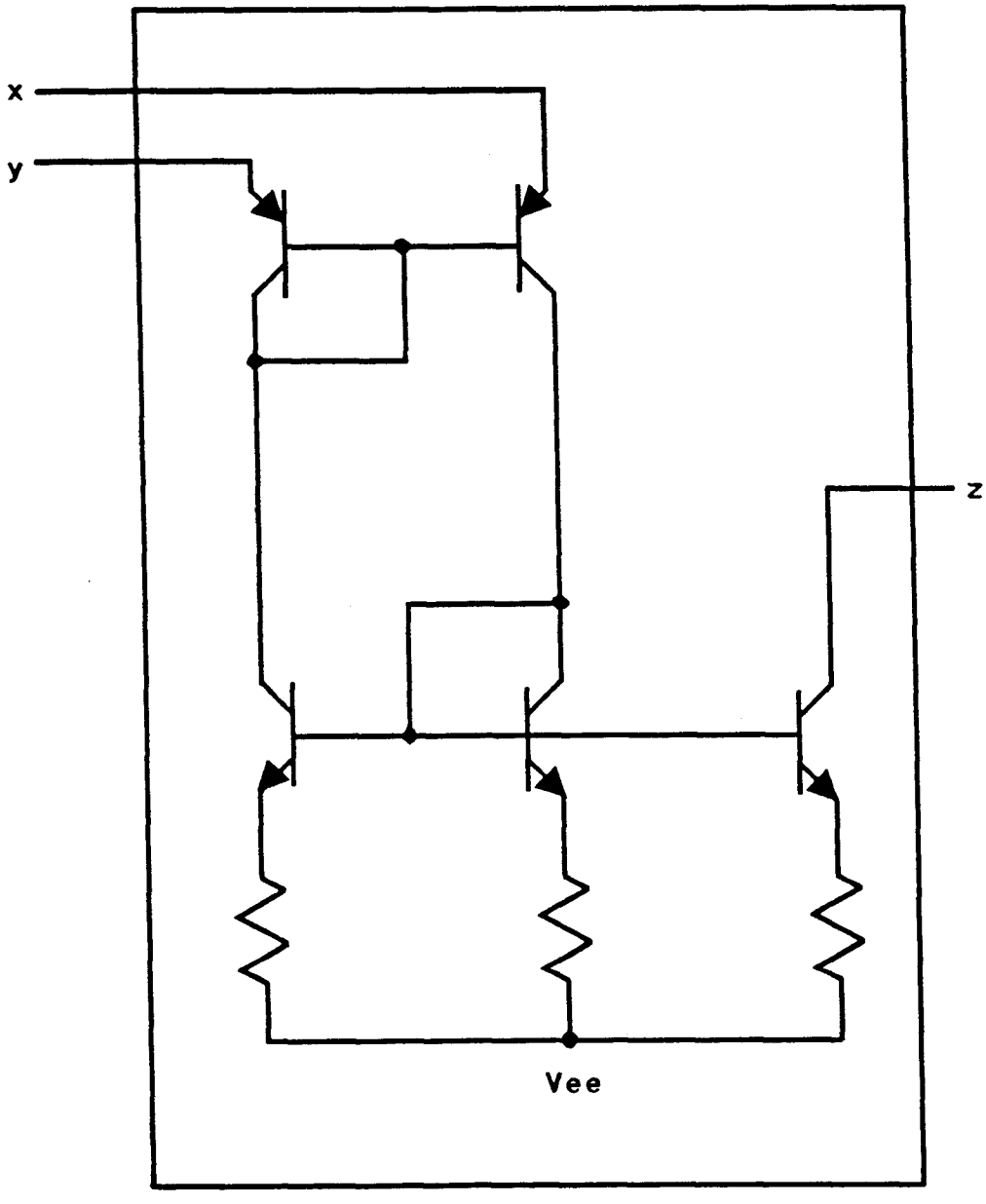

Figure 2. First order implementation of Smith and Sedra's current-conveyor.

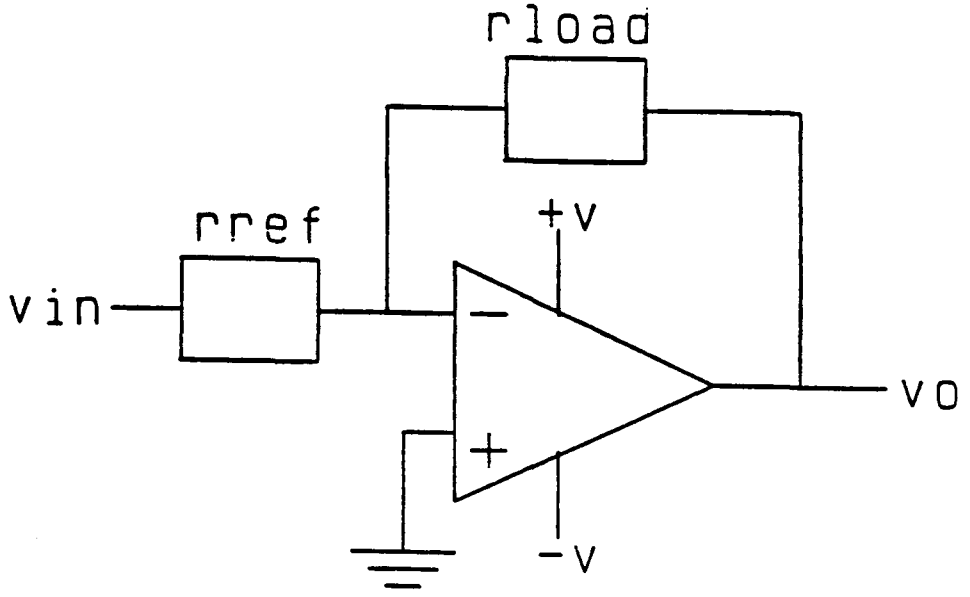

Figure 3. Traditional VOA current-conveyor.

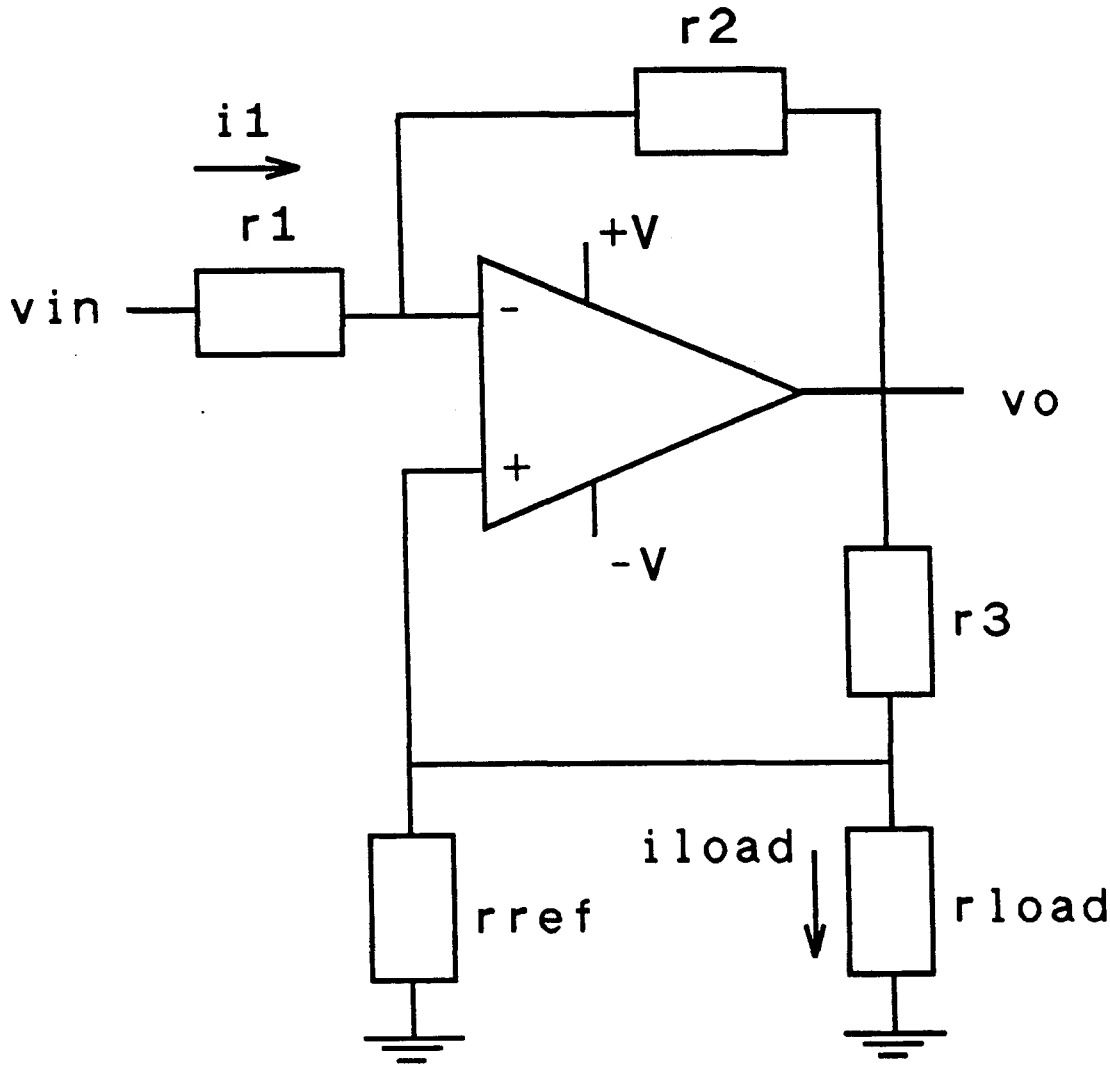

Figure 4. Howland's current source.

ground referenced problem. The circuit acts as a current source of il = -vin/rref for the condition that r3/rref = r2/r1. Unfortunately, relying on the combined positive and negative feedback in this way means that small departures from ideal balance conditions cause instability. A great deal of effort was put into modifying the Howland design employing several op amps, but the original problems were never adequately overcome.

The next step toward a true current-mode topology was to make use of the fact that the sum of the currents in the supply leads to the VOA is equal to the output current, provided that no other connections exist with ground that carry substantial current. This concept has been the hallmark of two decades of current-mode research. Current mirrors are used to sense the current to each supply rail and to recombine them at a single high impedance output node. This technique was reported by Graeme [1] in 1973, as shown in Fig. 5. The JFET current sources q1 and q2 are controlled by the high-gain feedback around the VOA. The n in the nR is just a multiplying factor. The difference in the two currents is the output current. Output current is controlled by vin which is compared to the feedback voltage provided by the current sensing resistors, rs. In general, the circuit shows high-precision and wide bandwidth but is again sensitive to mismatch due to the two feedback connections.

Hart and Barker [1] made the next step in 1975. They suggested the class-B voltage to current-conveyor of Fig. 6. This circuit similarly employed the VOA as its main gain block with a

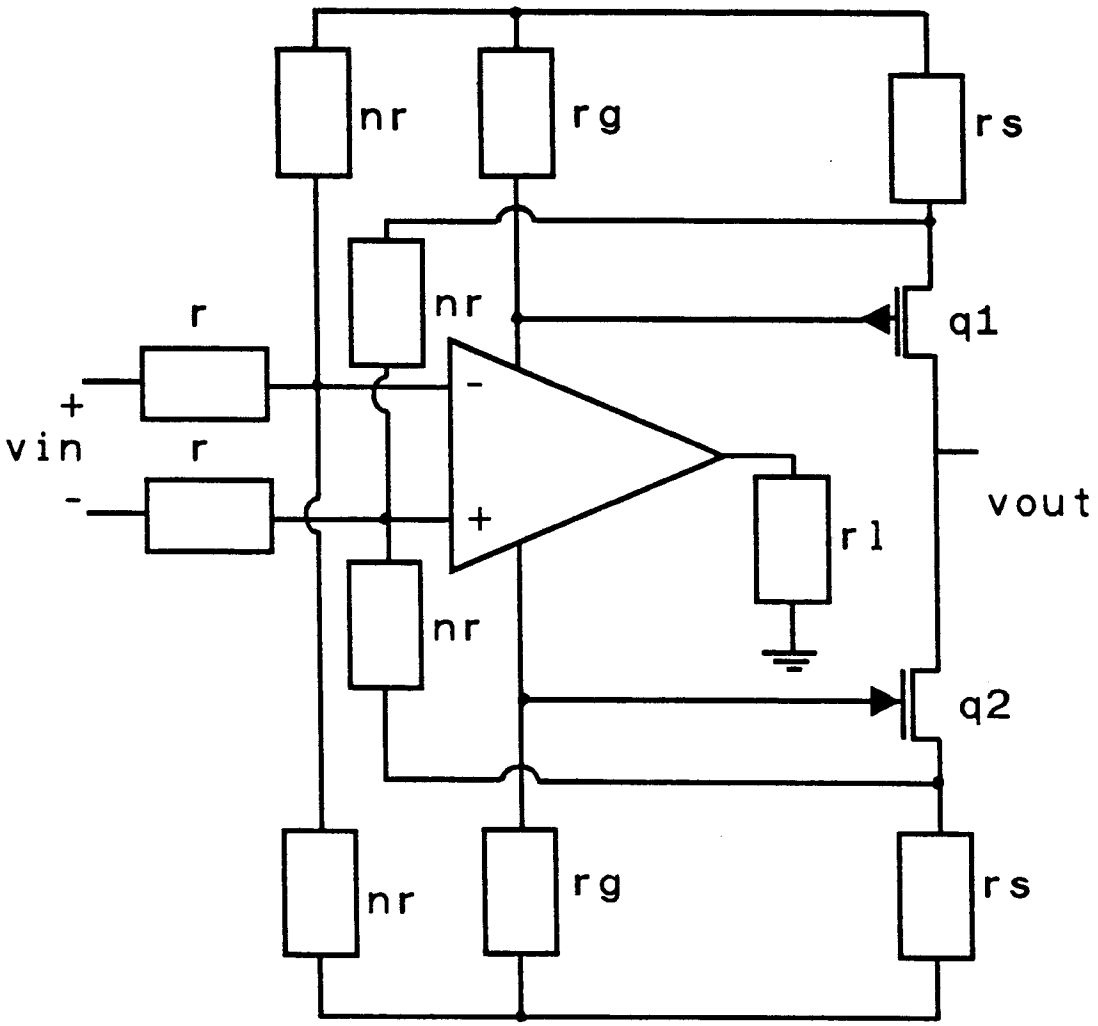

Figure 5. Supply current sensing controlled current source.

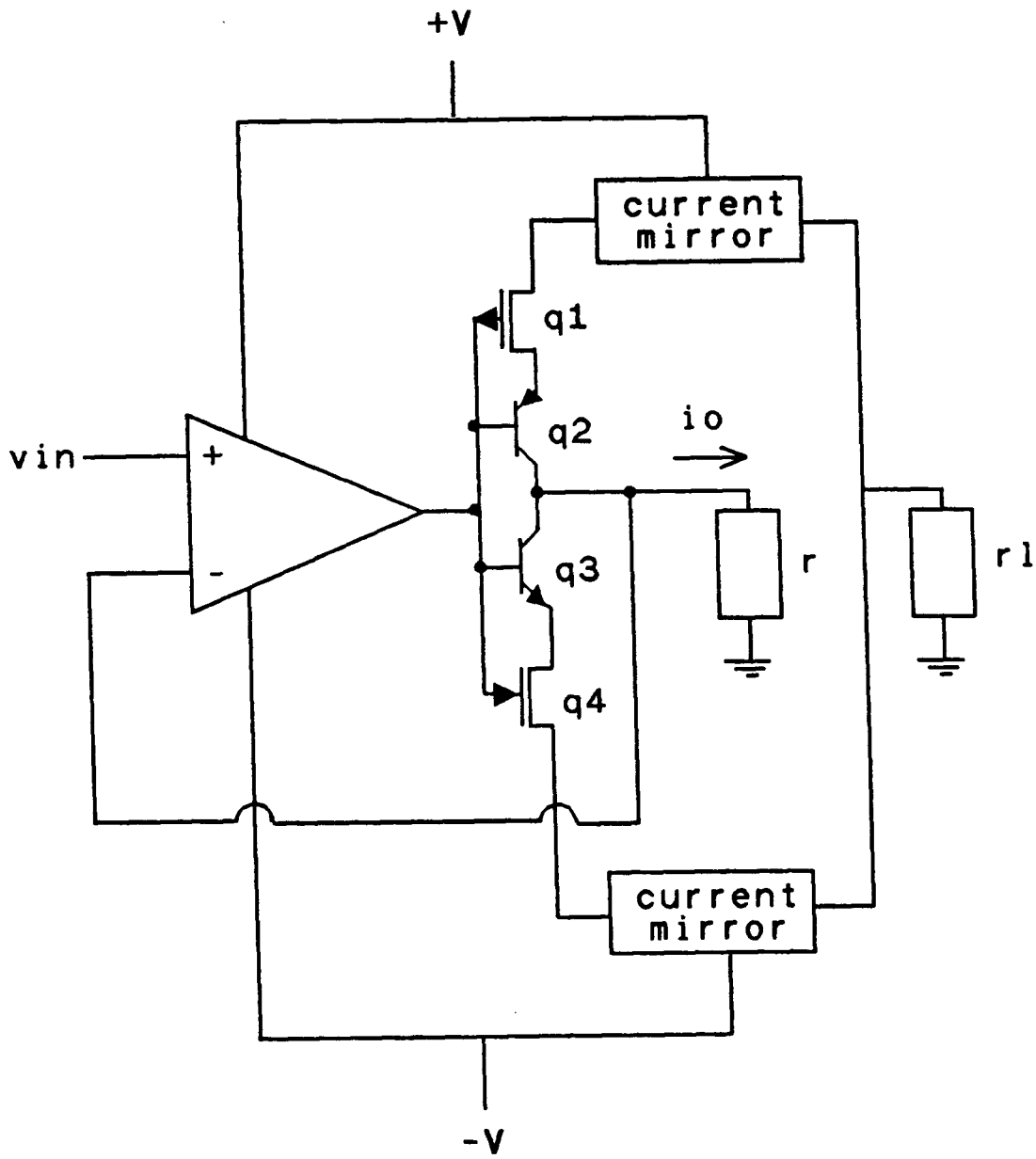

Figure 6. Hart and Barker's current-conveyor.

set of complimentary current mirrors used to sense the output current. Transistors q1 through q4 give the circuit high current gain and high output resistance. Positive and negative current mirrors (e.g., a four transistor Wilson current mirror) and JFETs in the output branch improve the overall output impedance and output voltage swing. This scheme avoids the resistor matching problem, but the class-B mode of operation resulted in considerable cross-over distortion in mid-range where all devices turn off.

This problem was identified and solved by Rao and Haslett [5] in 1978. Their circuit, Fig. 7, is operated in class-AB mode to eliminate cross-over distortion, and exhibits greater frequency performance together with improved output current drive. This scheme combines the ideas of using complimentary current mirrors and sensing the VOA supply current.

A similar VOA structure had been proposed by Hart and Barker [6] as a universal operational amplifier converter, Fig. 8. In this design, an arrangement of four resistors within the VOA circuit was employed to configure the network into any of the four main amplifier topologies, i.e., voltage-to-voltage, current-to-current, transconductance, and transresistance.

The trend of using current mirrors to sense the VOA's supply current and provide a well-defined output current proved far superior to traditional feedback techniques, and by the early 1980s had been well documented.

As previously stated, Allen and Terry [7] appear to have been the first to realize the potential of using a current sensing of a

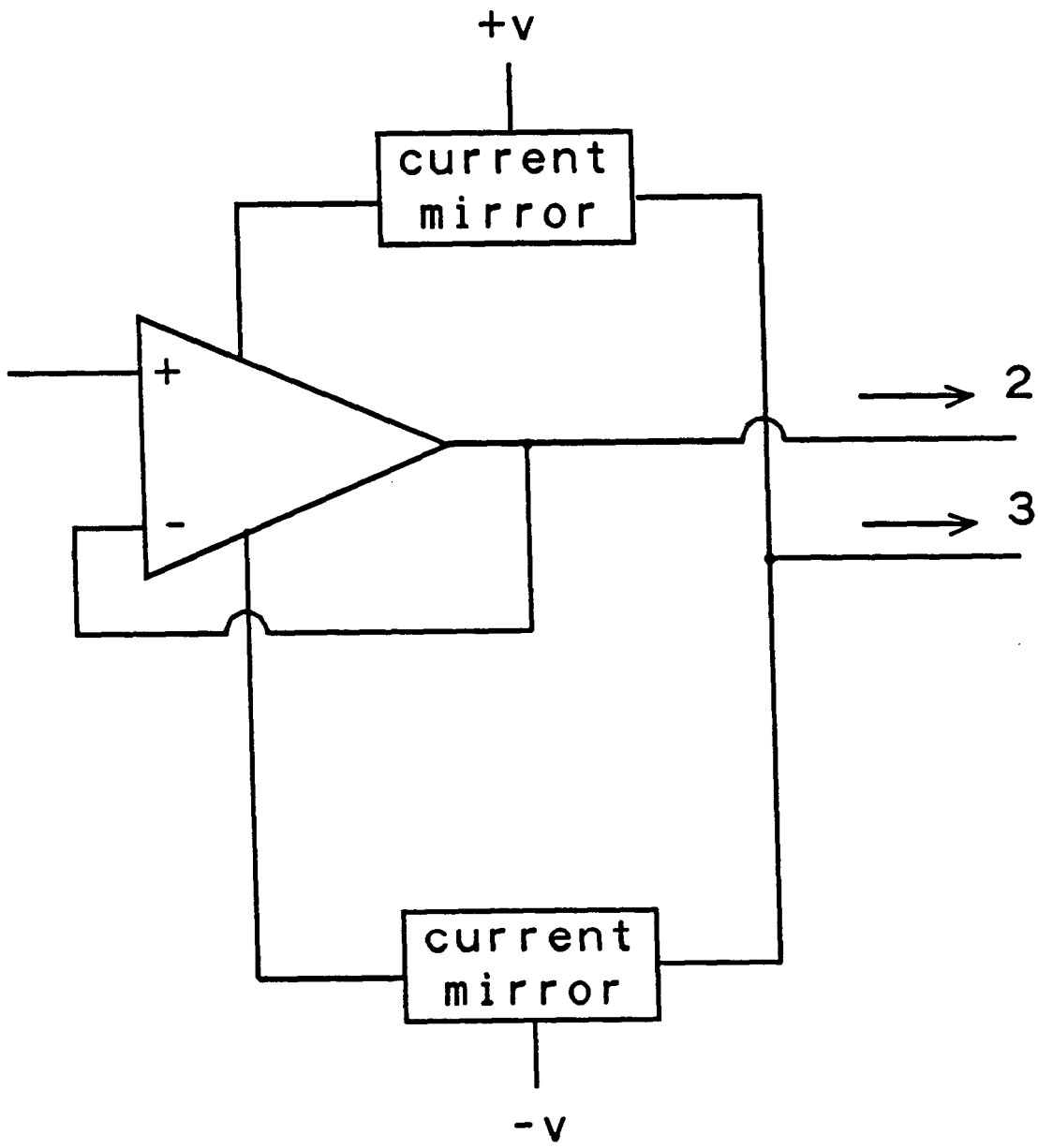

Figure 7. Class-AB current-convertor.

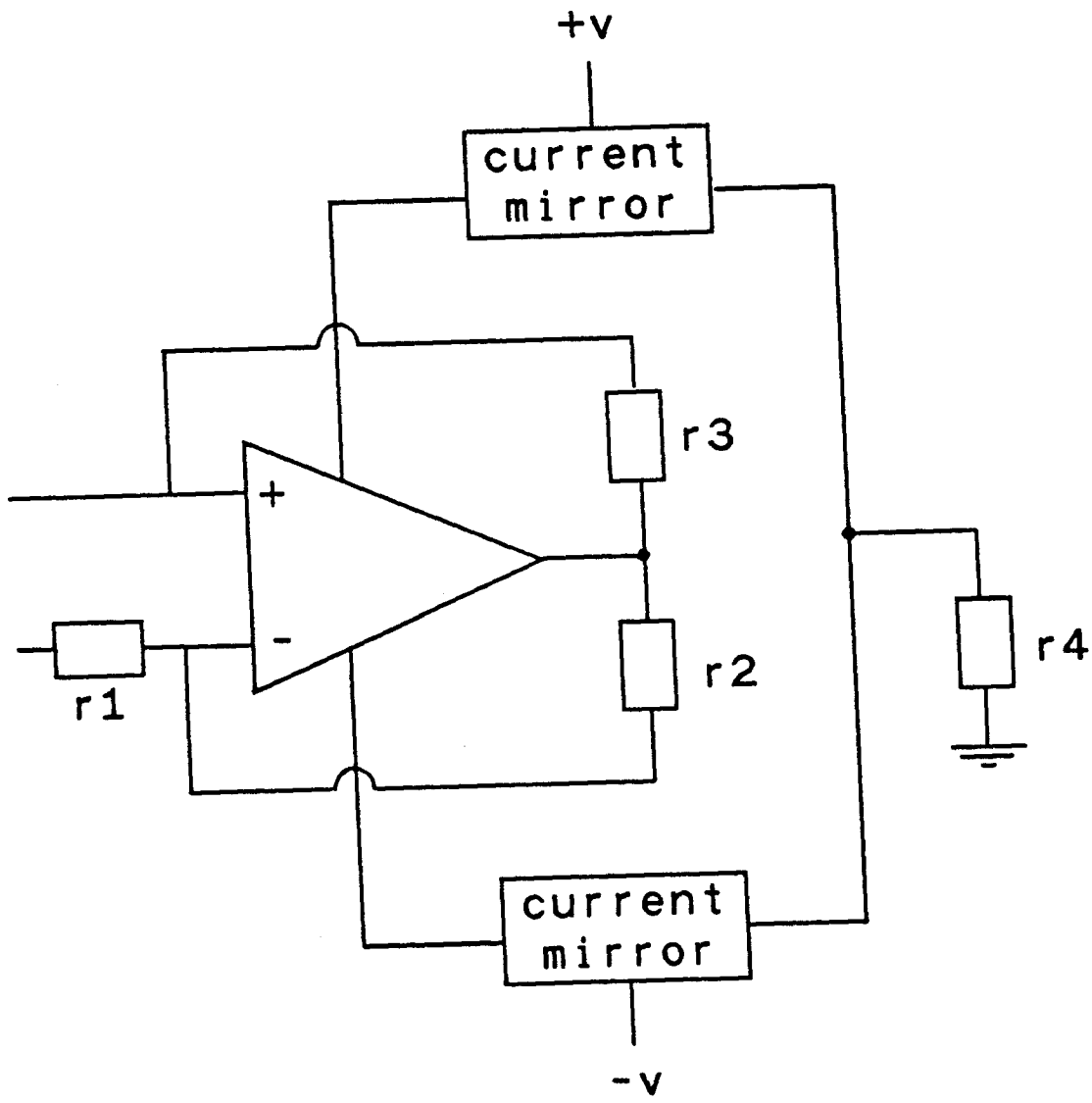

Figure 8. A universal convertor network.

VOA. Their circuit is shown in Fig. 9. When applied as an operational amplifier, it is not limited by constant gain bandwidth product, unlike the VOA based circuits, which is one of the main themes incorporated in this thesis.

2.2 The Gilbert Translinear Principle

The main distinguishing feature of a translinear circuit [2] is that it uses an even number of forward biased p-n junctions arranged in one or more loops, with the same number of one polarity as the other. This concept is equally applicable to MOSFET devices arranged with an even number of Vgs voltages forming one or more loops. The translinear input cell of a current-mode op amp proposed by Toumazou and Lidgey [1] is shown in Fig. 10. Starting at node 1, we move through the base/emitter junctions of T1, T3, T4, and T2 to meet the specifications of a translinear loop. Applying Kirchoff's voltage law and the equation for the voltage across a base/emitter junction to the loop, we obtain

$$0 = Vbe2 - Vbe4 + Vbe3 - Vbe1 \tag{2.5}$$

$$Vbe2 - Vbe1 = Vbe4 - Vbe3 \tag{2.6}$$

$$Vt[\ln(I2/Is2) - \ln(I1/Is1)] = Vt[\ln(I4/Is4) - \ln(I3/Is3)]. \tag{2.7}$$

Where $Vt = kT/q$, Ii is the collector current of transistor Ti, and Isi is the E-B saturation current of Ti. Assuming matched pairs of

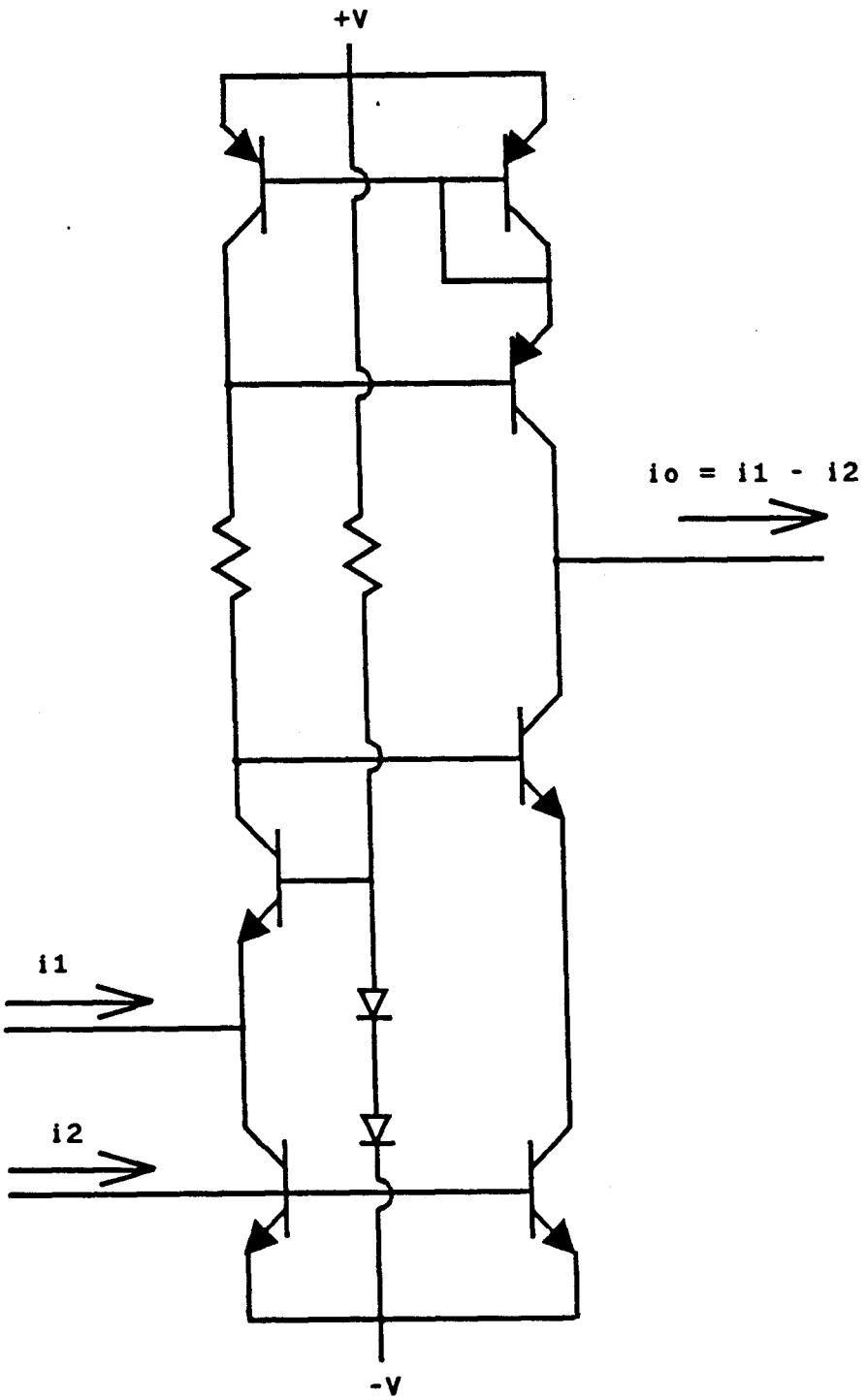

Figure 9. Allen and Terry's current controlled current source.

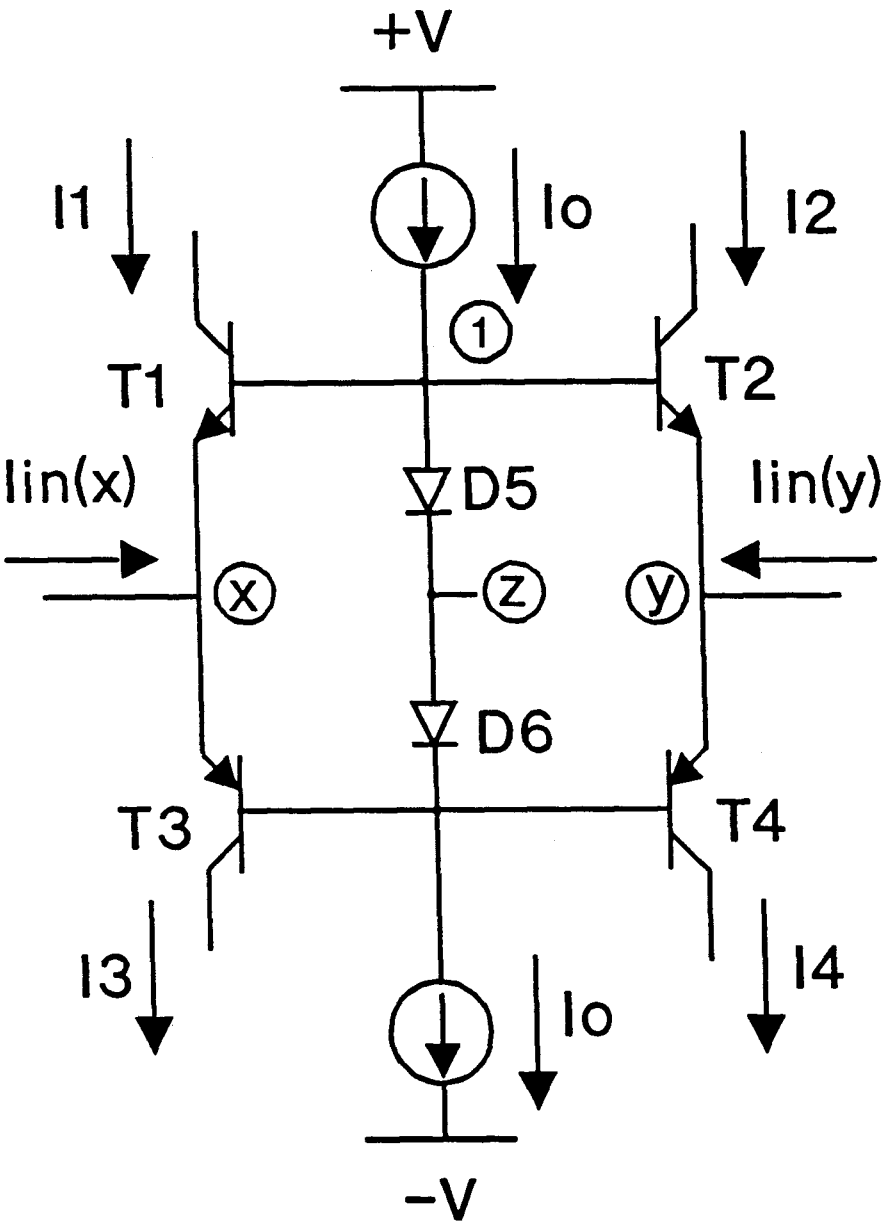

Figure 10. Translinear input cell of a BJT current-mode op amp.

transistors at the same temperature so that Vt is the same for both pairs, and with Is1 = Is2 = Is5, and Is3 = Is4 = Is6, we obtain

$$I2/I1 = I3/I4, \tag{2.8}$$

or equivalently,

$$I2*I4 = I1*I3. \tag{2.9}$$

From a similar derivation including the two biasing diodes D5 and D6 in a loop with either T1T3 or T2T4, we get

$$I1*I3 = I4*I2 = Io^2. \tag{2.10}$$

Also, applying Kirchoff's current law at nodes x and y, we see that

$$I1 = I3 - Iin(x), \tag{2.11}$$

$$I2 = I4 - Iin(y). \tag{2.12}$$

For zero input current, i.e. Iin(x) = Iin(y) = 0, I1 = I3 and I2 = I4; therefore, dc bias conditions are established by the translinear loops so that

$$I1 = I3 = I2 = I4 = Io. \tag{2.13}$$

Note that the bias currents in T1-T4 can be scaled relative to Io by

scaling Is1-Is4 relative to Is5-Is6. As we apply a common-mode input current Iin, i.e. Iin(x) = Iin (y) = Iin, with a peak value < Io (so that cutoff never occurs),we substitute (2.11) and (2.12) into (2.10) and solve the resulting quadratic equation to find

$$I1 = I2 = Io - Iin \tag{2.14}$$

$$I3 = I4 = Io + Iin. \tag{2.15}$$

If we apply the input current differentially with current Iin going into x and out of y, then using the same methods applied to (2.14) and (2.15), we obtain

$$I2 = I3 = Io + Iin \tag{2.16}$$

$$I1 = I4 = Io - Iin. \tag{2.17}$$

A further feature of this translinear cell is that with Iin(x) = Iin(y) = 0, the potential at z is reflected at x and y via emitter follower action. The result is a flexible current mirror/current differencer.

Chapter 3. PROPOSED CCCS CIRCUIT

3.1 Introduction

This quad BJT cell can be readily transformed into a similar and simpler MOSFET circuit (Fig.11). If the bias current is applied directly to one branch, and the input current is applied at the same node as in Fig. 11, the voltages between nodes x and z will adjust to whatever level is necessary to support the forced current, I1 = I2 = Ibias - Iin. the peak value of Iin need only be less than Ibias so that the transistors are always conducting and in the saturation region. We can analyze Fig. 11 as a MOS equivalent of a BJT translinear loop with q1-q4 operating in the square-law saturation region. The notation SQRT{} shall be used to indicate a square root function, k'n = un*Cox and k'p = up*Cox, where un and up are electron and hole mobilities respectively, and Vtn and Vtp are threshold voltages for n and p type devices respectively.

For n type MOSFETs q1 and q3:

$$I = (k'n/2)(W/L)(Vgs - Vtn)^2 \quad (3.1)$$

$$Vgs = SQRT\{I*2*L/(k'n*W)\} + Vtn. \quad (3.2)$$

For p type MOSFETs q2 and q4:

$$I = (k'p/2)(W/L)(Vsg - |Vtp|)^2 \quad (3.3)$$

$$Vsg = SQRT\{I*2*L/(k'p*W)\} + |Vtp|. \quad (3.4)$$

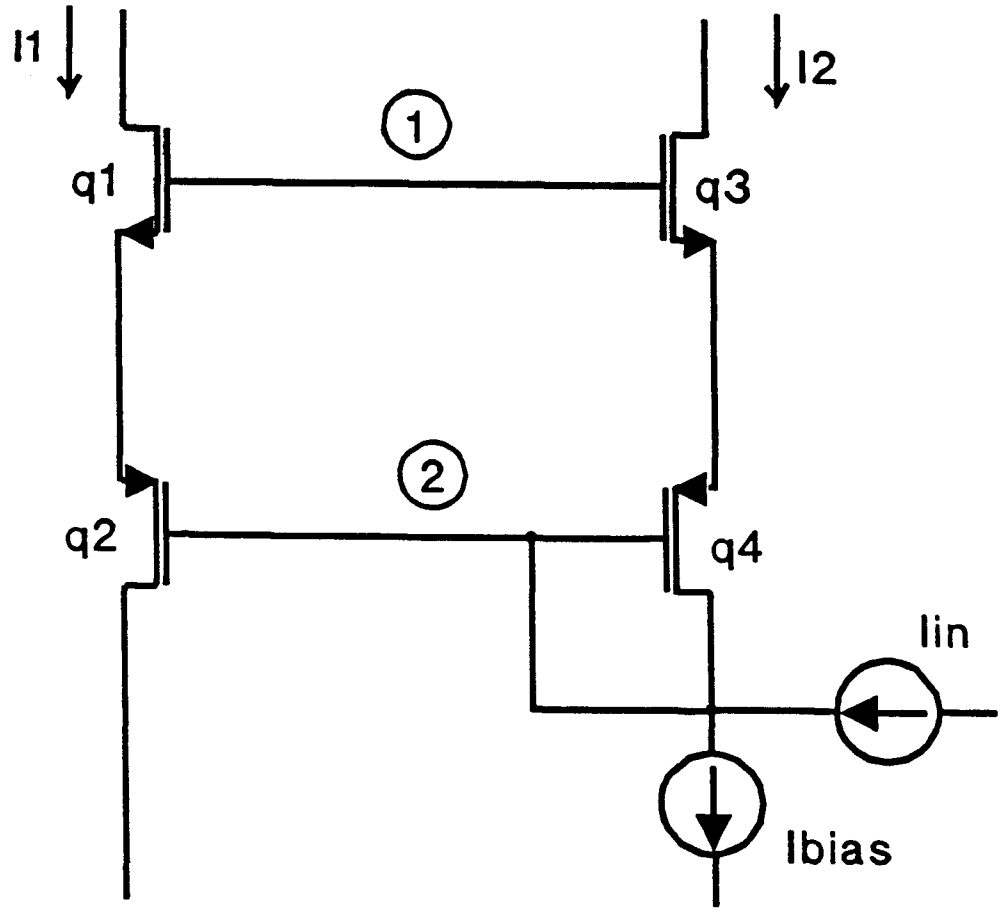

Figure 11. MOSFET version of input cell.

Assuming a p-well process, the n-type transistors will have their backgates connected to their sources, and therefore will not suffer a backgate effect on Vtn. The p-type transistors will suffer some backgate effect, but due to the current-mirroring action, the voltage at each of the sources must be the same, so that

$$Vt2 = Vt4 = Vtp. \tag{3.5}$$

Summing voltages around the translinear loop,

$$Vgs1 + Vsg2 = Vgs3 + Vsg4. \tag{3.6}$$

Assuming matched transistors

$$[SQRT\{I1*2*L/(k'n*W)\} + Vtn] + [SQRT\{I1*2*L/(k'p*W)\} + Vtp] = [SQRT\{I2*2*L/(k'n*W)\} + Vtn] + [SQRT\{I2*2*L/(k'p*W)\} + Vtp]. \tag{3.7}$$

After rearranging and simplifying,

$$SQRT\{1/k'n\}*SQRT\{I1*2*L/W\} + SQRT\{1/k'p\}*SQRT\{I1*2*L/W\} = SQRT\{1/k'n\}*SQRT\{I2*2*L/W\} + SQRT\{1/k'p\}*SQRT\{I2*2*L/W\} \tag{3.8}$$

and assuming all widths and lengths are equal,

SQRT{I1*2*L/W}*[SQRT{1/k'n} +
SQRT{1/k'p}] =
SQRT{I2*2*L/W}*[SQRT{1/k'n} +
SQRT{1/k'p}]. (3.9)

Finally

I1 = I2 (3.10)

and

I2 = Ibias - Iin. (3.11)

A current-controlled current source (CCCS) should operate as

Iout = k*Iin. (3.12)

where k is a linear scaling factor. We can alter the circuit of Fig. 11 into a circuit that is governed by this equation by adding branches that will precisely replicate the bias current, and by noting that scaling is easily accomplished by ratioing the widths of the transistors in each branch while keeping the lengths of like transistors the same, i.e. Ln need not equal Lp

(see 3.9).

In order to extract the bias current, we need a precise mirroring of one branch that carries just the bias current, and the other branch that carries the bias current minus the input current. This is accomplished as shown in Fig. 12 using a class-AB topology. Again, we are making use of the translinear principle. One loop runs through q7, q8, q6, and q3; and the other through q1, q2, q4, and q5. Scaling can be accomplished here by manipulating shape factors. If the notation of I36 is used to mean the current through transistors q3 and q6, then

$$I36 = I78\{ [(W/L)36] / [(W/L)78] \}. \qquad (3.13)$$

Of course the ratio of the shape factors of q1 and q2 : q4 and q5 should be the same as the ratio of the shape factors of q7 and q8 : q3 and q6, so that we mirror an identically scaled ibias.

Next we need to extract the bias current. This can be done by mirroring (Fig. 13). High swing cascode current mirrors (e.g. q23, q24, q27, q28, and q13, q14, q17, q18) can be used so that only 2 Vdsat voltage drop per mirror is lost from the full voltage range. Dummy loads (e.g. q19, q20, q21, q22, q9, q10, q11, q12) are placed on non-critical ends of branches to replicate loading effects so that currents are not inaccurately mirrored due to channel length modulation and Vds differences.

3.2 Experiment Description

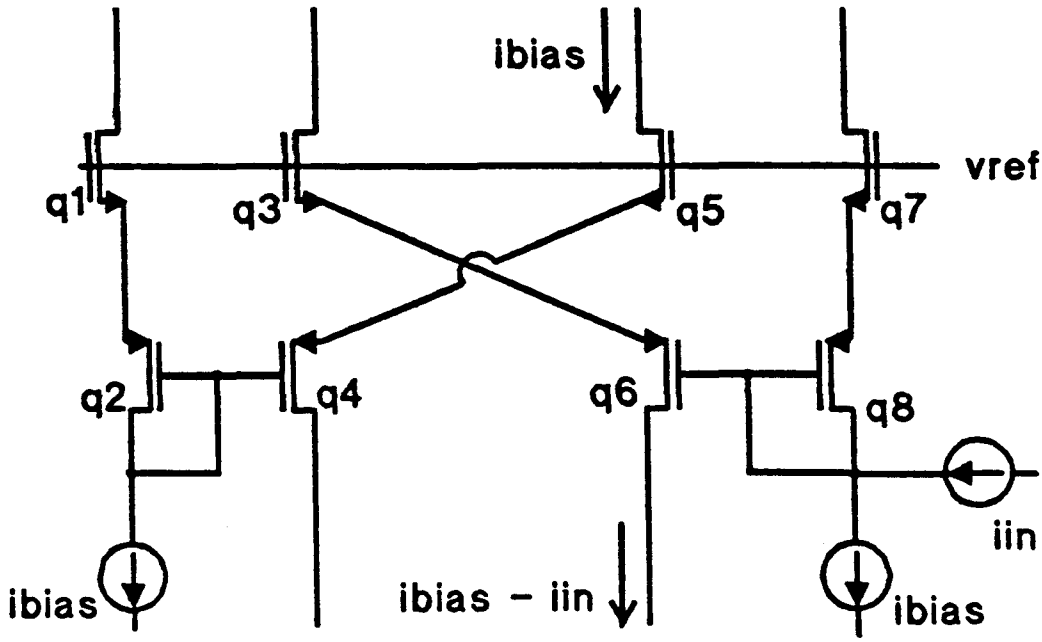

Figure 12. MOSFET input cell with current mirrors.

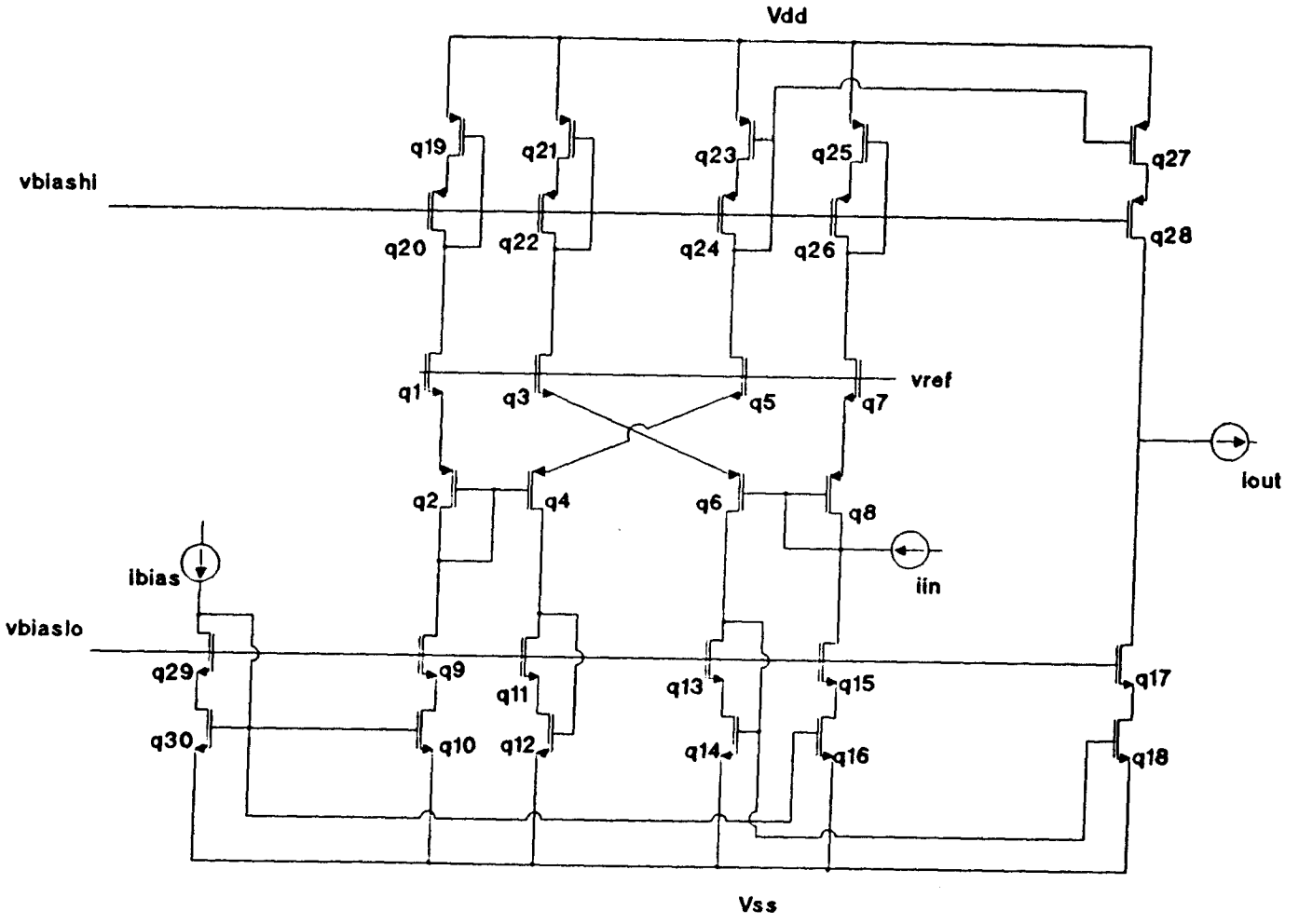

Figure 13. Proposed CCCS.

Experiments were conducted assuming a 2um p-well CMOS process, and as such all n-channel devices are designed to have their sources connected to their backgates and all p-channel devices have their sources connected to the most positive voltage, Vdd. The circuit is driven with +5v and -5v power supplies and the transistor model parameters shown in Fig. 14 as supplied by the MOSIS fabrication service for gate lengths of 2um are used in the simulation. A reference bias current of 75uA was chosen simply because it is within the range of common current levels in modern CMOS integrated circuits.

3.3 Bias Condition Tradeoffs

Optimum transistor widths and lengths for a bias current of 75uA are found as follows. In saturation, and neglecting channel-length modulation effects,

$$Id=(k'/2)(W/L)(Vgs - Vt)^2. \tag{3.14}$$

The voltage from gate to source can be thought of as the voltage required to invert a channel, Vt, plus enough additional voltage to assure that the device is in strong inversion, Vgs = Vt + Vdsat. Substituting into (3.14), we obtain

$$Id = (k'/2)(W/L)(Vt + Vdsat - Vt)^2. \tag{3.15}$$

```
MODEL NTRAN MFET2: LEVEL=1 POL=NMOS LD=0.458388U
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KP=4.464000E-05 GAMMA=0.8759  PHI=0.6 UO=362.246
UEXP=9.499054E-02 UCRIT=130365  DELTA=1.000000E-06
VMAX=100000 XJ=0.250000U LAMBDA=1.446553E-02
NFS=1.245818E+12 NEFF=1 NSS=1.000000E+12 TPG=1.000000
RSH=20.580001 CGDO=5.652906E-10 CGSO=5.652906E-10
CGBO=4.291585E-10  CJ=4.015000E-04 MJ=0.446500
CJSW=5.023000E-10 MJSW=0.270500 PB=0.750000
;Weff = Wdrawn - Delta_W
;The suggested Delta_W is 0.35 um


MODEL PTRAN MFET2: POL=PMOS LEVEL=1 LD=0.355084U
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;Weff = Wdrawn - Delta_W
;The suggested Delta_W is 0.38 um
;OPTIONS LIMPTS=500 LVLTIM=4 TRTOL=10 GMIN=1E-10 RELTOL=0.5
```

Figure 14. Model parameters used in simulations.

Vdsat can be chosen so that the required Vgs for saturation is known. A Vdsat of 350mV is small enough so that significant range is not lost, but large enough to ensure square law operation of these devices. Therefore

$$W/L = [(Id*2)/k'n](1/Vdsat)^2$$
$$= 27.43. \qquad (3.16)$$

for the n-type devices. Rounding to 30 and choosing lengths of 10um for good analog operation (no short channel effects), the device size is 300/10. The p-type devices are chosen to be this size as well, in the interest of symmetry of layout.

A high quality CCCS will have low input impedance and high output impedance. Input and output impedances of the circuit in Fig. 13 are calculated using small-signal models as follows where gm is transconductance:

$$Ids = (k'/2)(W/L)(Vgs - Vt)^2$$

$$gm = dId/dVgs = k'(W/L)(Vgs - Vt)$$
$$Vgs - Vt = SQRT\{(Id*2*L)/(k'*W)\}$$
$$gm = k'(W/L)SQRT\{(Id*2*L)/(k'*W)\}$$
$$= SQRT\{2*k'*W*Id/L\}$$

and output resistance

ro = Va/Id

where Va is the early voltage.

For an n-type device biased with a drain current of 75uA
gm = 450uA/V; ro = 921kohm

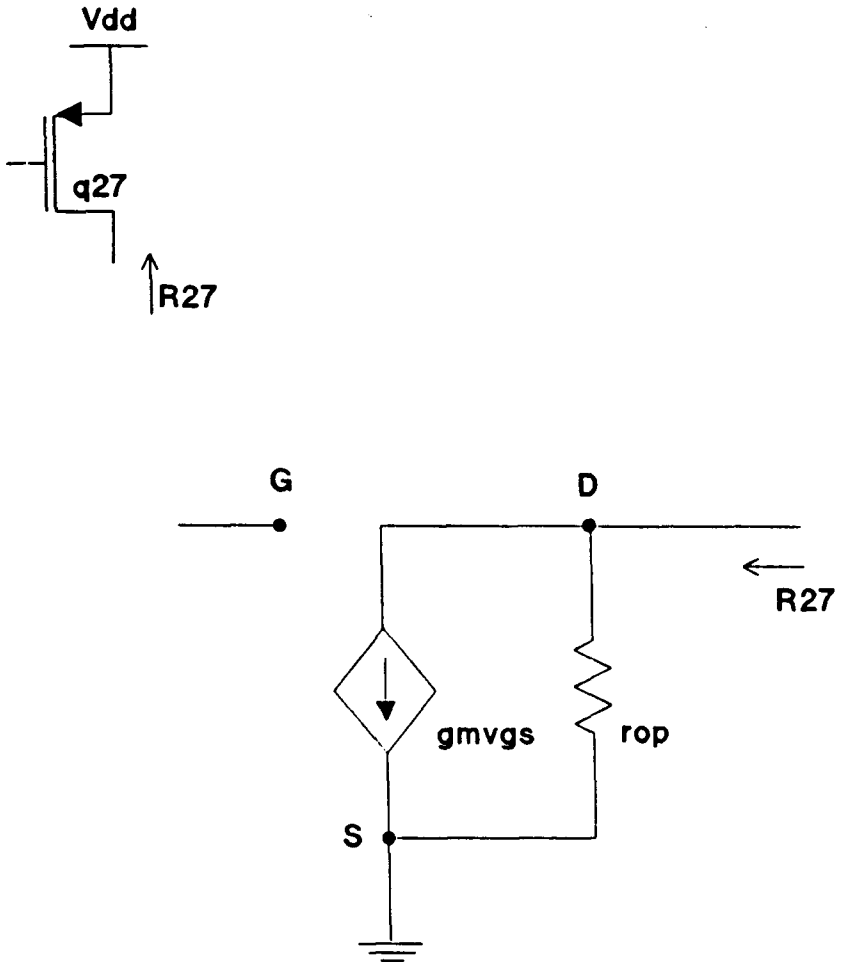
and for p-type device biased at 75uA
gm = 337uA/V and ro = 203kohm.

Both resistances can be found by small-signal analysis. Figure 15 shows the calculation of the resistance looking into the drain of q27 (see Fig. 13 for complete circuit). Figure 16 then uses that resistance to find the resistance looking into the drain of q28. Figure 17 shows the calculation of resistance looking into the drain of q18. Then Fig. 18 in turn shows the use of R18 to find the resistance looking into the drain of q17. The total output resistance is then

Rout = R17//R28 = 14meg//383megohm
= 13.5megaohm. (3.17)

The simulated output impedance is shown in Fig. 19. The -3dB bandwidth is measured to be 18.5kHz. Using the equation

$f_{-3dB} = (1/2*pi)*(1/Rout*Cout)$



R27 = rop = 203k ohm

Figure 15. Small signal analysis of R27.

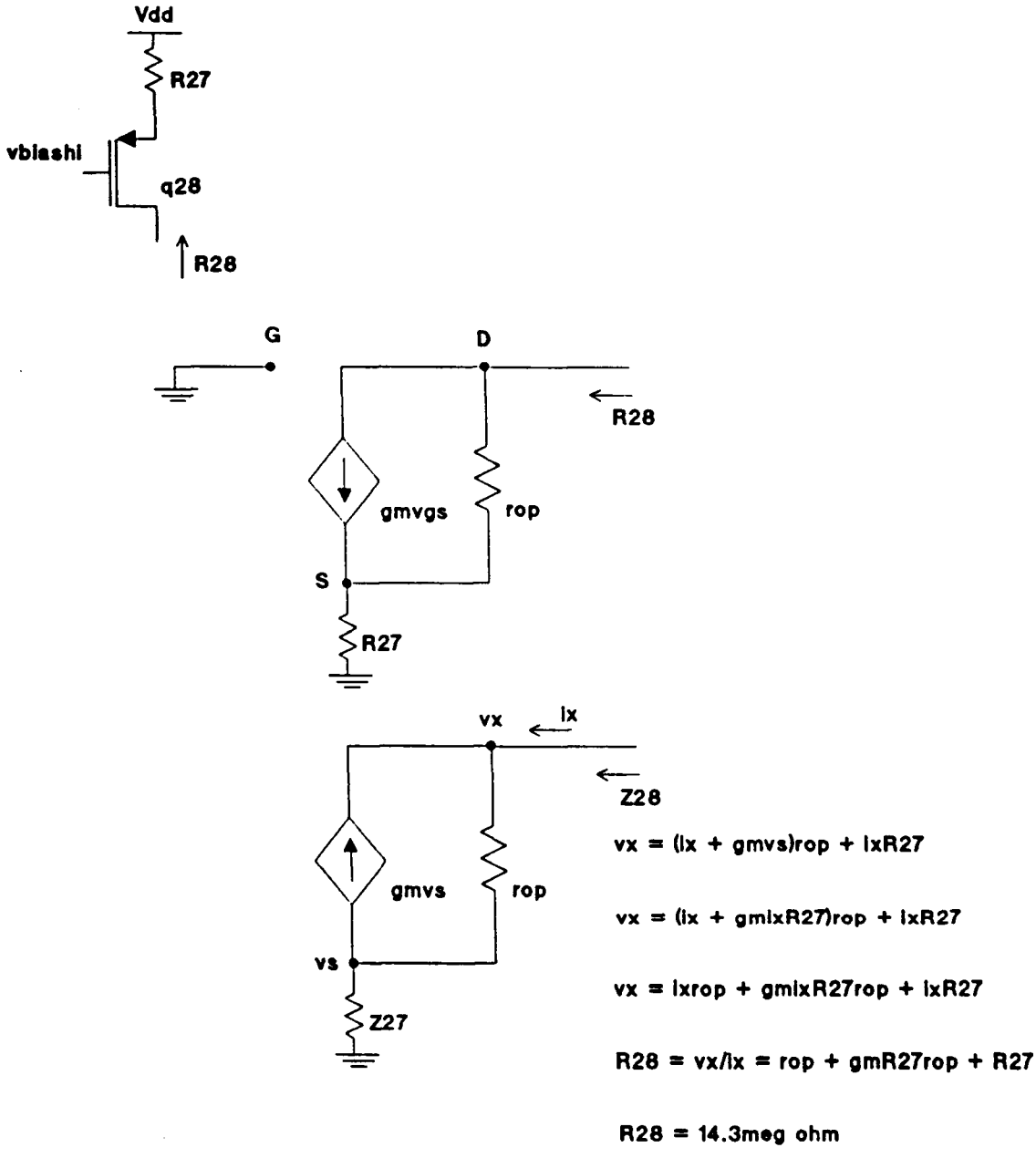
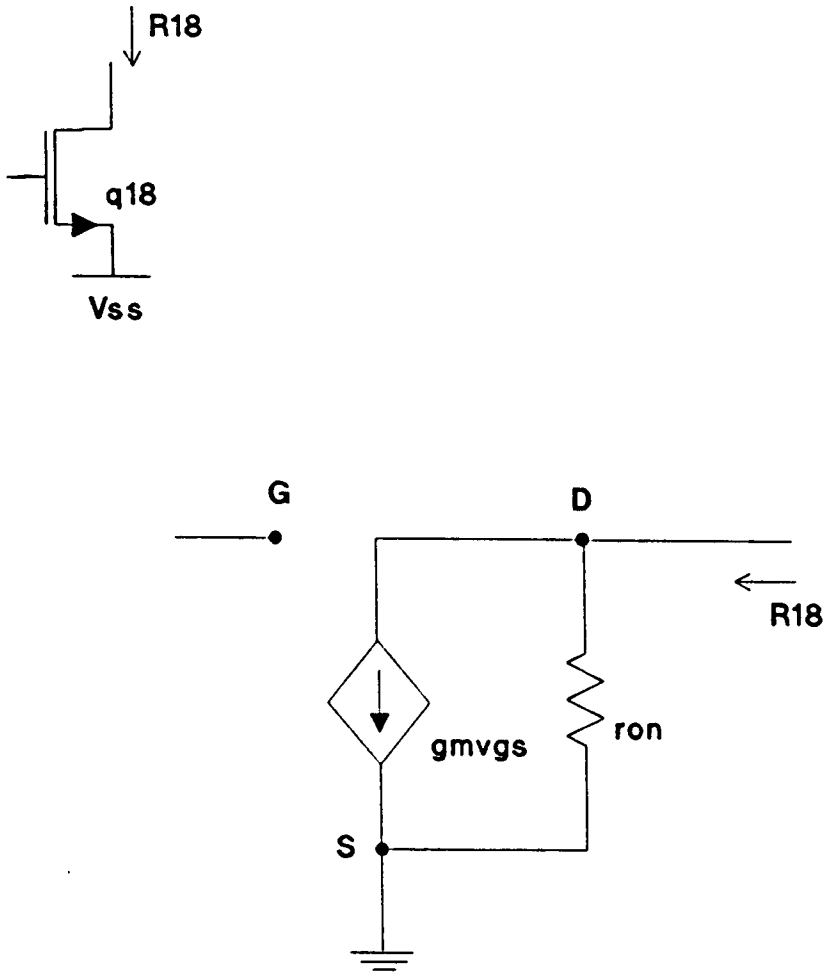


Figure 16. Small signal analysis of R28.



R18 = ron = 921k ohm

Figure 17. Small signal analysis of R18.

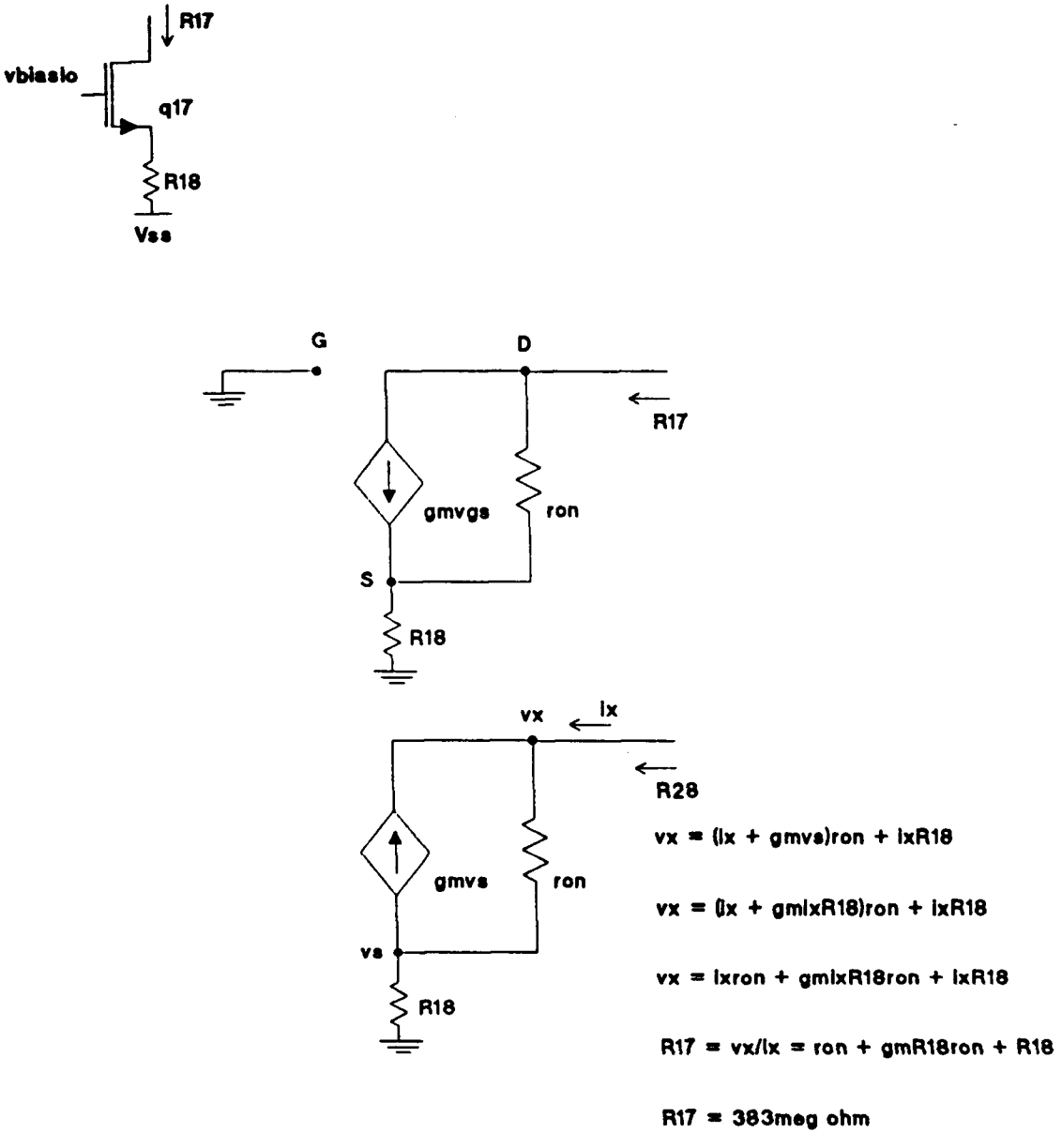


Figure 18. Small signal analysis of R17.

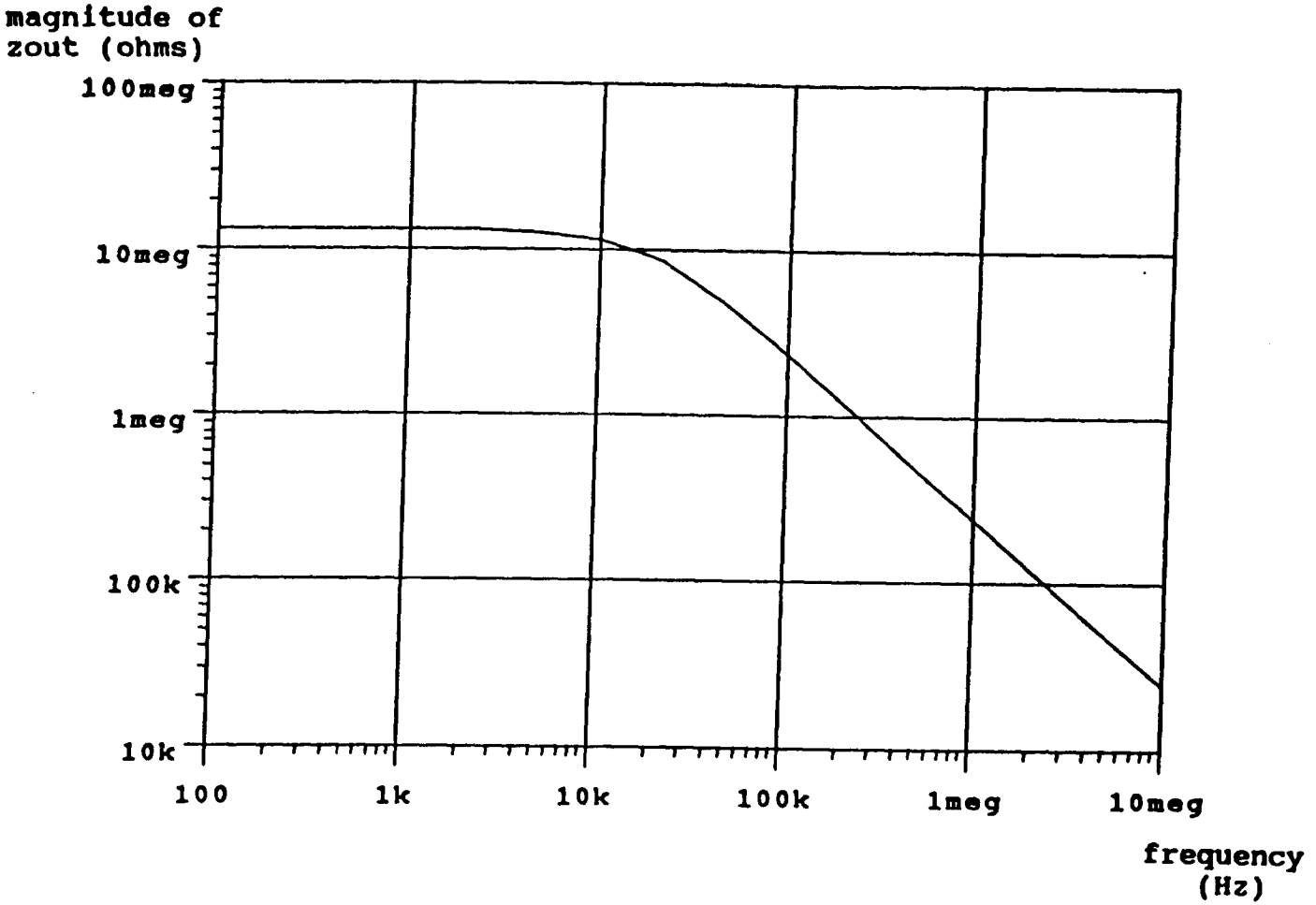


Figure 19. Simulation of Zout.

to calculate output capacitance, Cout = 860pF.

The same approach can be used to calculate Rin. R15 is equal to R17 by an identical calculation. The resistance looking into the drain of q26 and gate of q25, called Rmir, is calculated in Fig. 20. This then, is used to find R7, looking into the source of q7 as in Fig. 21. R7 is used to find R8, the resistance looking into the gate and drain of q8 in Fig. 22. Finally, Rin is found by

Rin = R8//R15 = 5.12k//14 megaohm
= 5.12kohm. (3.18)

Similar calculations for Cin yield Cin = 31pF. Simulation results for Rin are shown in Fig. 23.

This value of input resistance is fairly high. It can be decreased by the use of an amplifier stage as shown in Fig. 24. In this way, Rin is reduced by

Rin (closed loop) = Rin (open loop)/(1 + loop gain). (3.19)

For an active-load amplifier with 75 uA bias current, and devices of 300/10um, the

loop gain = gm*Rl
= gmn*(rop//ron)
= 317uA/V * (1.84 megaohm//406kohm)

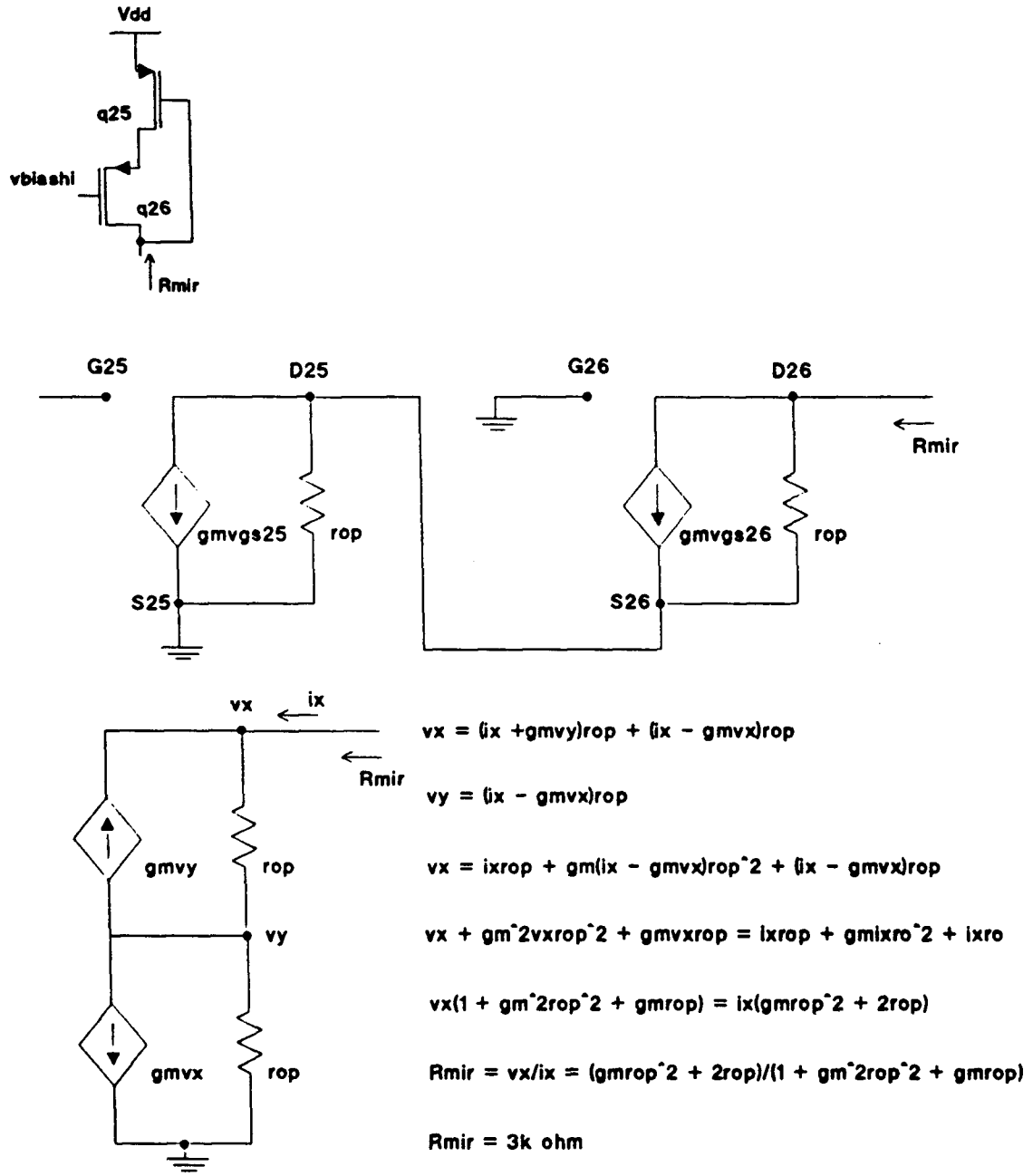
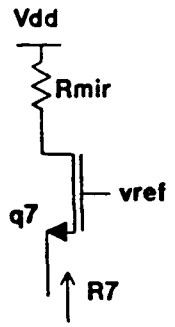
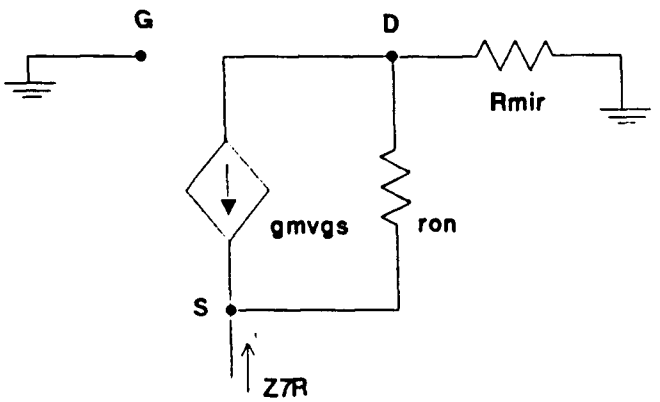
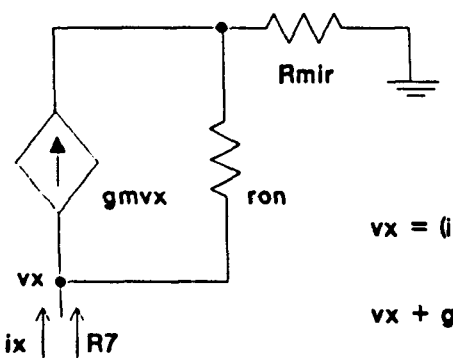


Figure 20. Small signal analysis of Rmir.







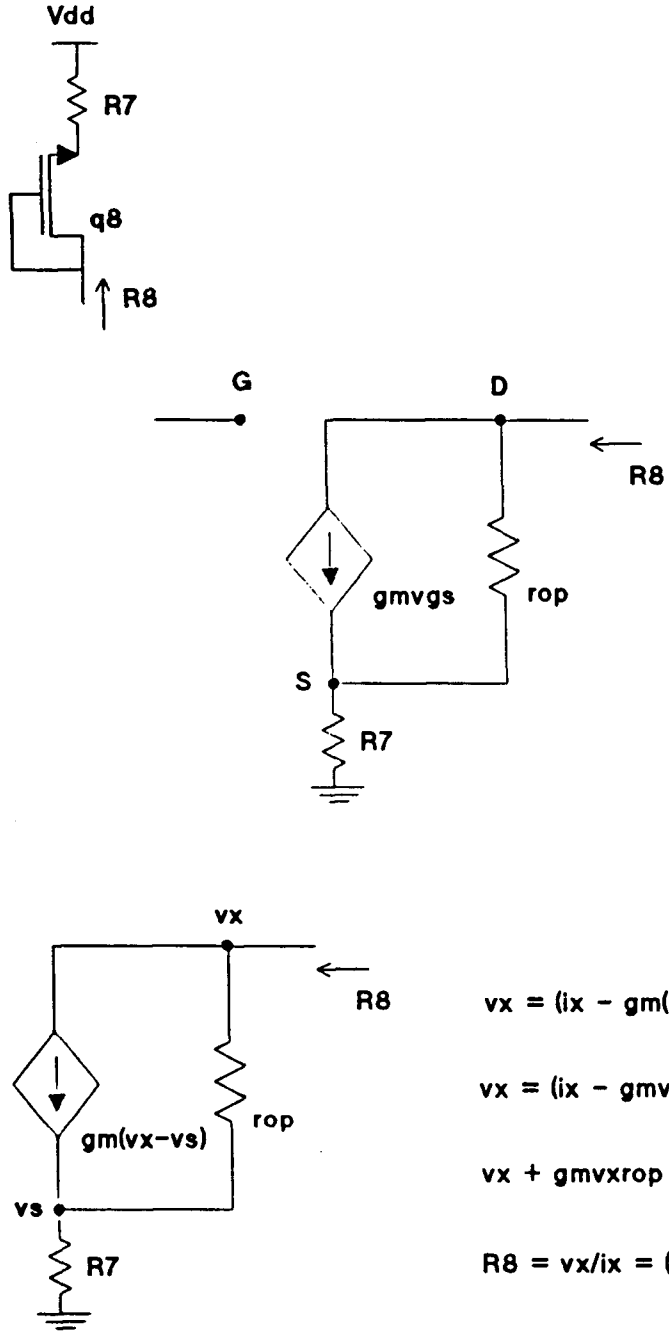
$vx = (ix - gmvx)ron + ixRmir$

$vx + gmvxron = ixron + ixRmir$

$r7 = vx/ix = (ron + Rmir)/(1 + gmron)$

$R7 = 2.2k\ ohm$

Figure 21. Small signal analysis of R7.



$$vx = (ix - gm(vx - vs))rop + ixR7$$

$$vx = (ix - gmvx + gmixR7)rop + ixR7$$

$$vx + gmvxrop = ixrop + gmixR7rop + ixR7$$

$$R8 = vx/ix = (rop + gmR7rop + R7)/(1 + gmrop)$$

$$R8 = 5.12k \text{ ohm}$$

Figure 22. Small signal analysis of R8.

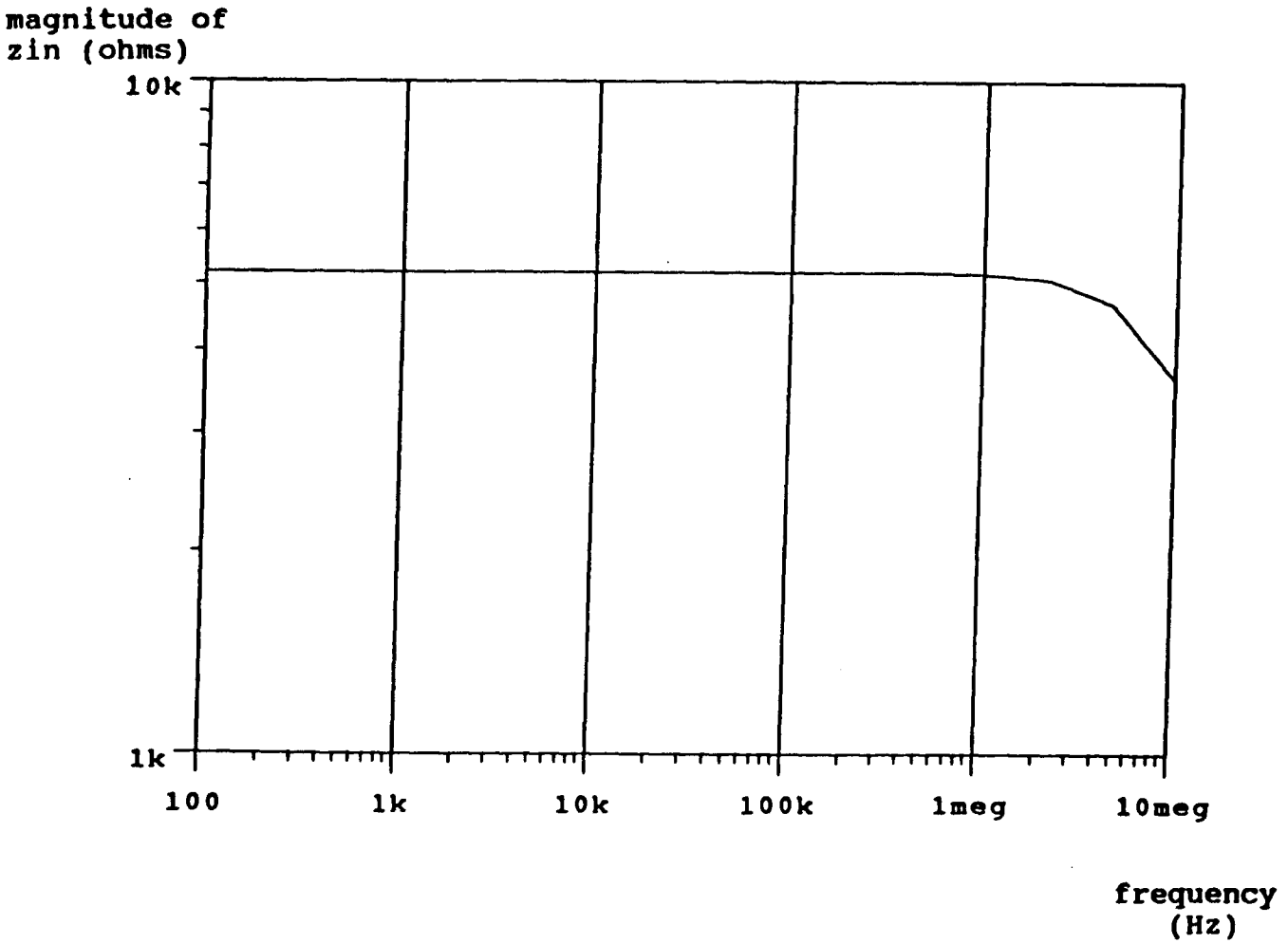


Figure 23. Simulation of Zin.

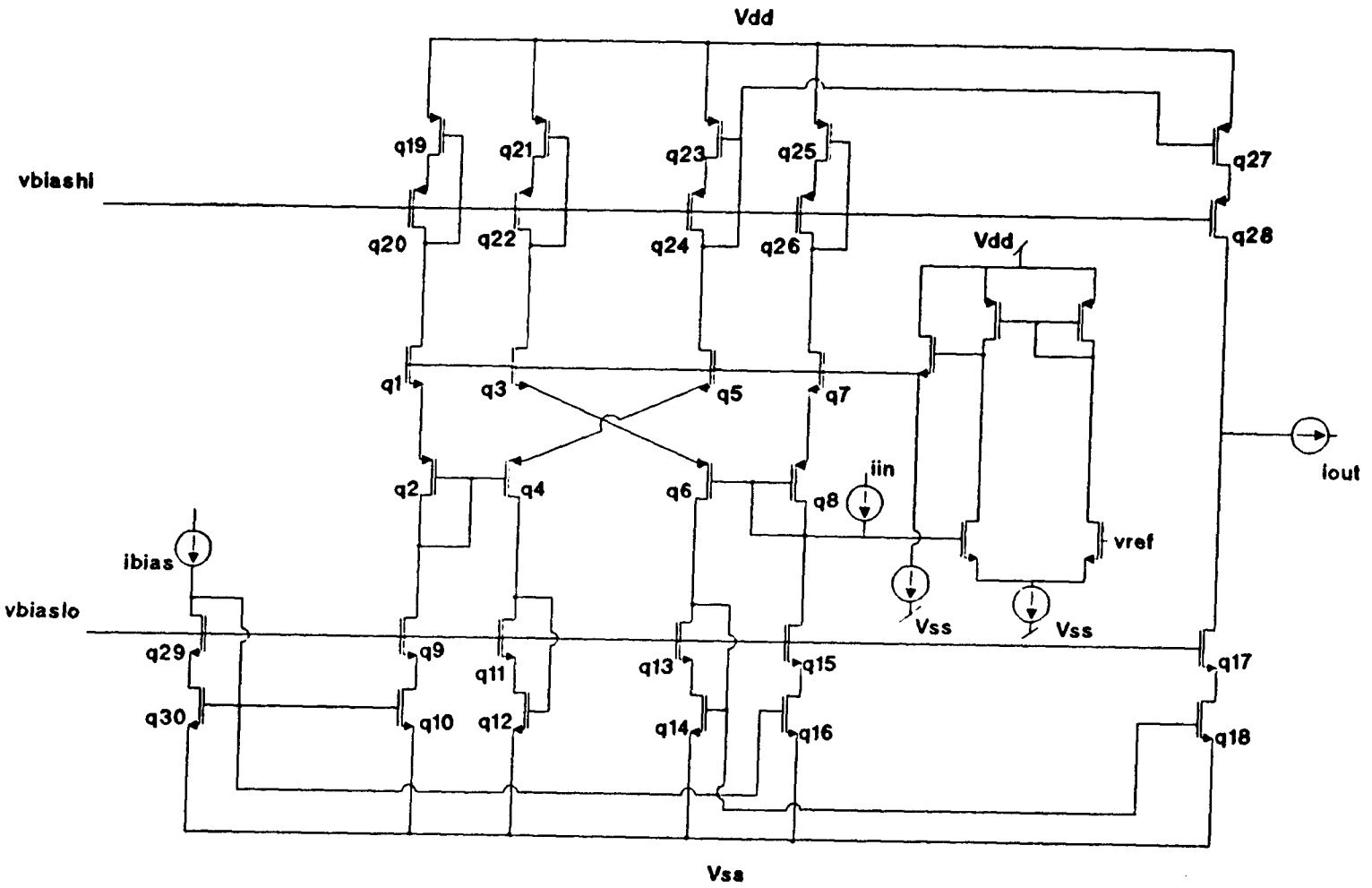


Figure 24. Final circuit design.

~ 105. (3.20)

Rin (closed loop) = 5.12kohm/106

~ 48ohm. (3.21)

Using the equation

f-3dB = (1/2*pi)*(Lin/Rin)

the input inductance is found to be Lin = 30megH. The simulation results are shown in Fig. 25.

Also, the bandwidth of Zout can be improved by reducing the width, and therefore capacitance, of devices q28 and q17. The accuracy of the CCCS is not affected by using a width of 150um and length of 10um. Recalculating for this size device at 75uA

For n-type devices,
gm=317uA/V
ro=921kohm
and for p-type devices,
gm=239uA/V
ro=203kohm.

which predicts Zout = 9.9megaohm. Figure 26 shows the simulation of Zout with the smaller device sizes. Thus a

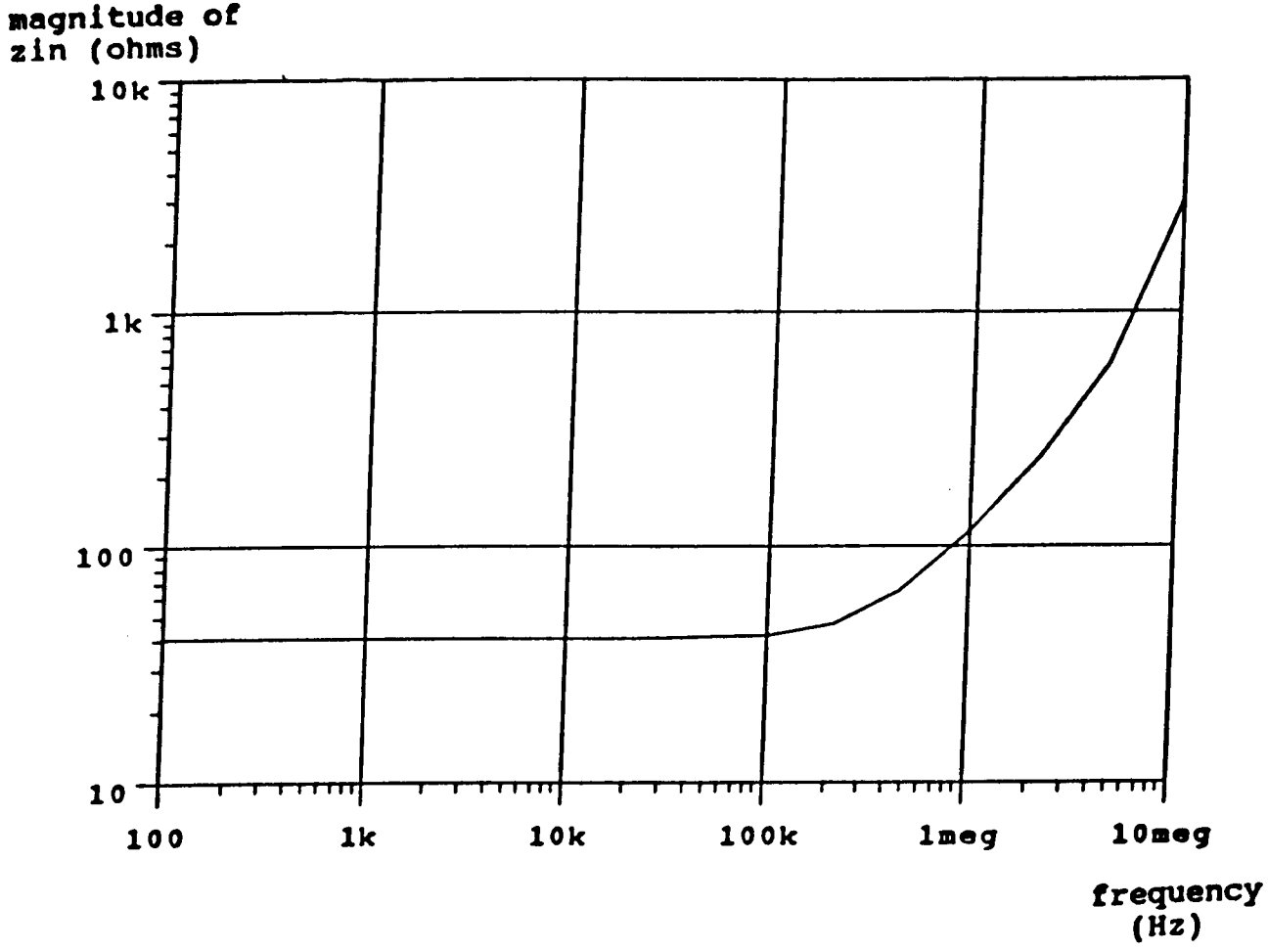


Figure 25. Zin with amplifier.

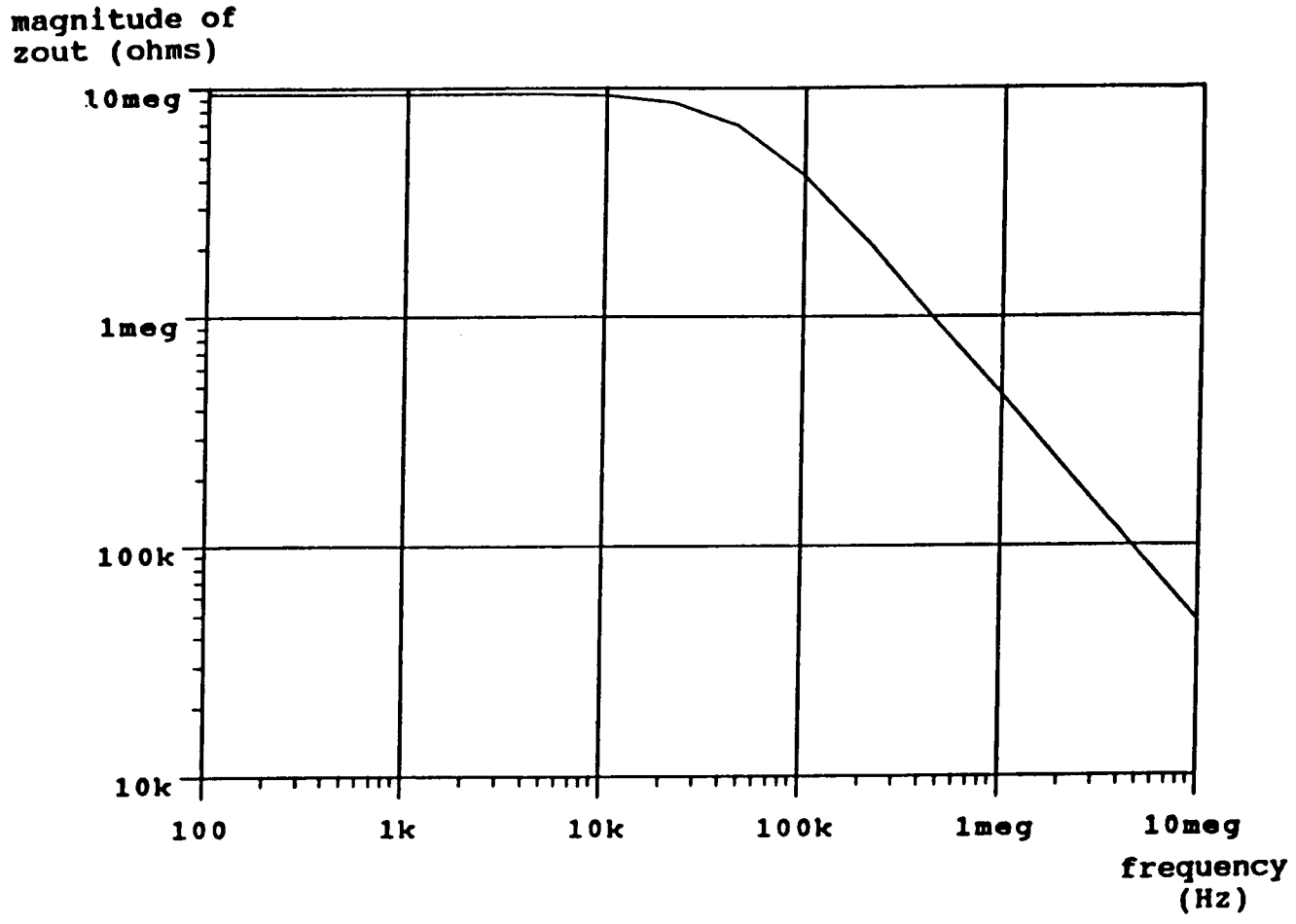


Figure 26. Zout with smaller output devices.

small penalty in the magnitude of Zout gives an improvement in bandwidth from 18.5kHz to 48.8kHz. Bandwidth of output impedance is not important, but it determines the bandwidth of current gain, which is.

Chapter 4. ACCURACY, GAIN, AND BANDWIDTH

Accuracy is one of the single most important attributes of a current controlled current source. The proposed circuit of Fig. 24 exhibits excellent accuracy over an input current range of -25 uA to +25 uA with a bias current of 75 uA. Figure 27 shows the dc transfer curve for the unity gain configuration. A simulation set-up as in Fig. 28 reveals the error current shown in Fig. 29. The maximum error occuring at -25 uA input is an error of .34 uA or .68% as seen from Fig. 29. Figure 30 shows the slope of the transfer curve, ideally equal to +1 for this configuration.

Figure 31 presents a study of the effects of temperature on the accuracy of the circuit. From a range of -50 to +150 degrees Celsius there is virtually no change in output current. This is due to the fact that the output versus the input is dependent only on current mirroring, and therefore device ratioing, which is entirely independent of temperature.

Figures 32 and 33 show the magnitude and phase responses respectively for the small signal current gain. The bandwidth of the circuit is simulated to be 12.86 megahertz.

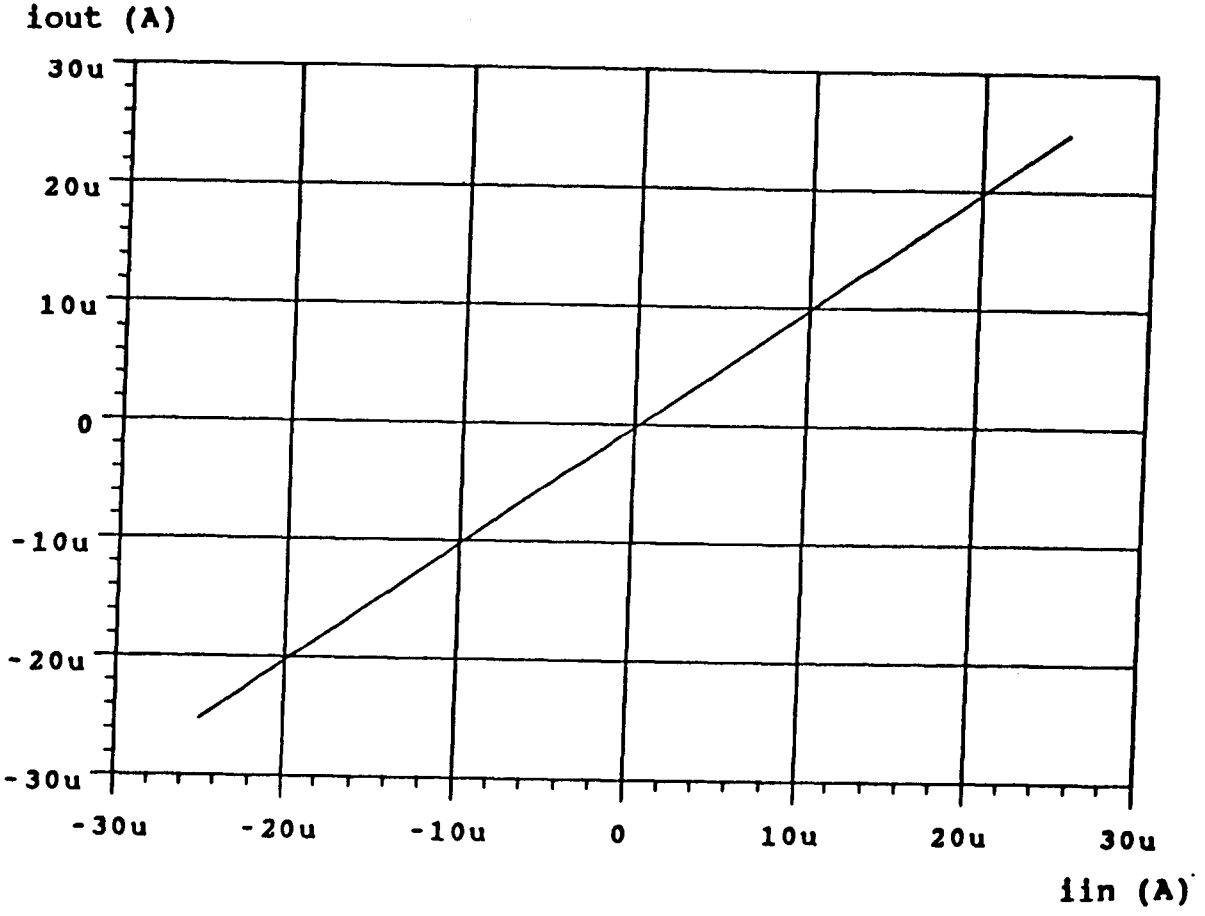


Figure 27. DC transfer curve of CCCS.

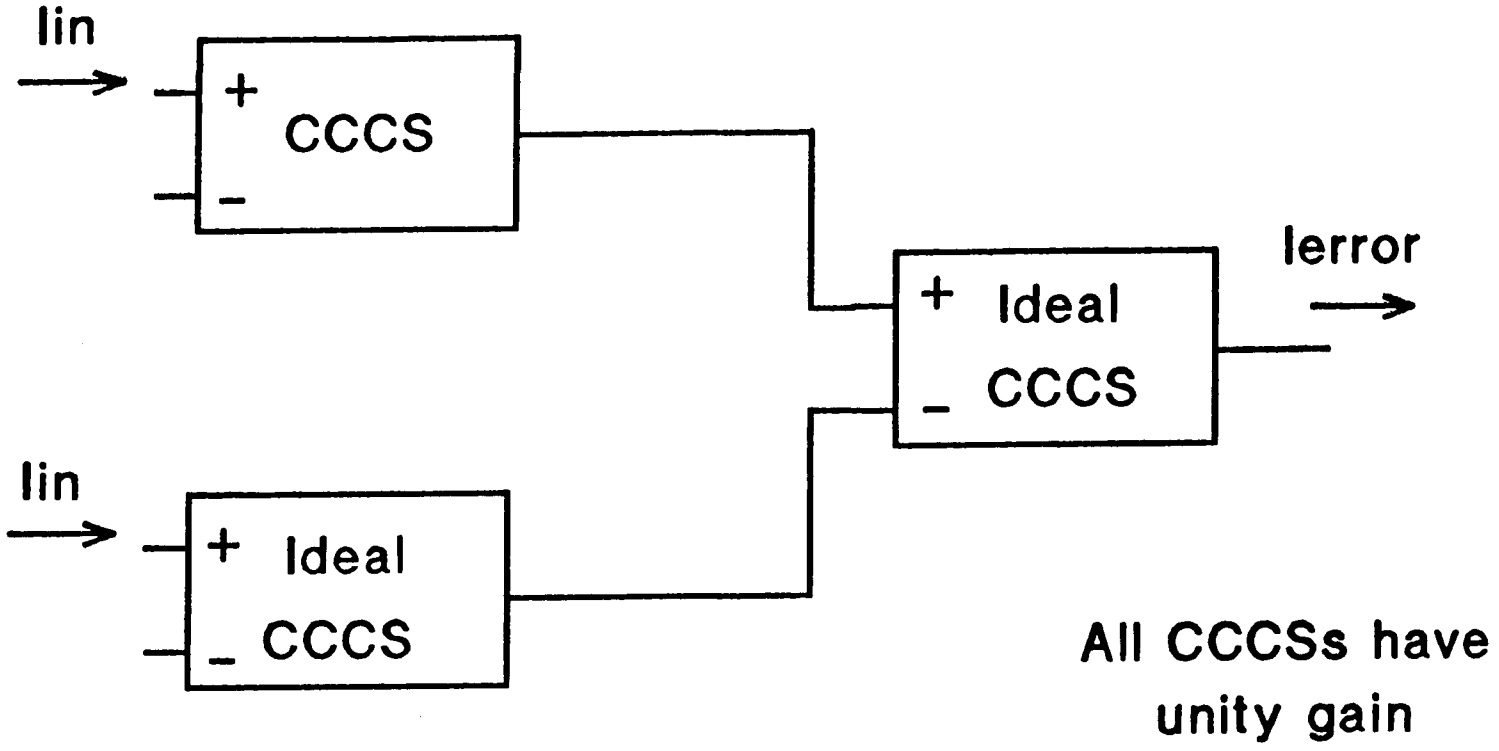


Figure 28. Simulation to find Ierror.

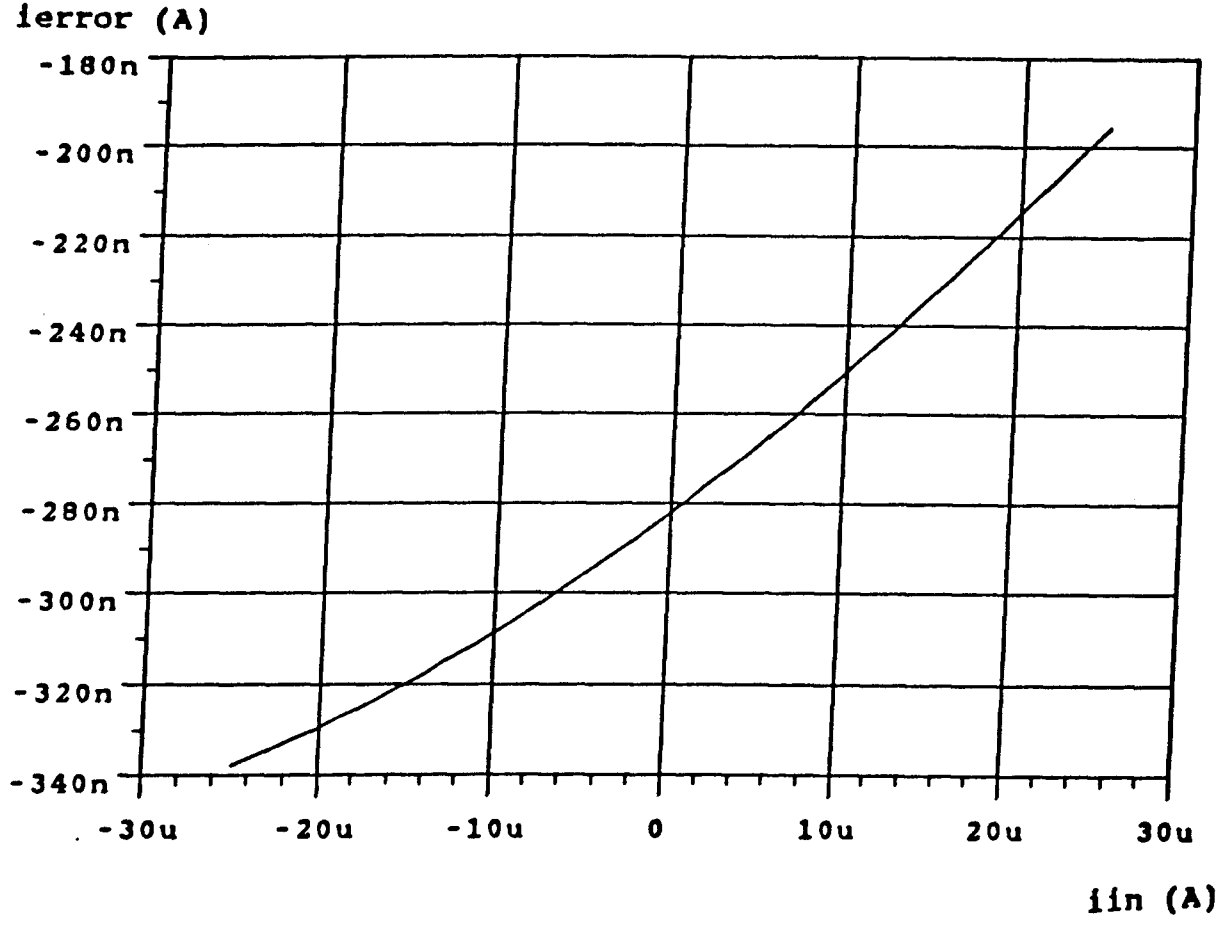


Figure 29. Error current.

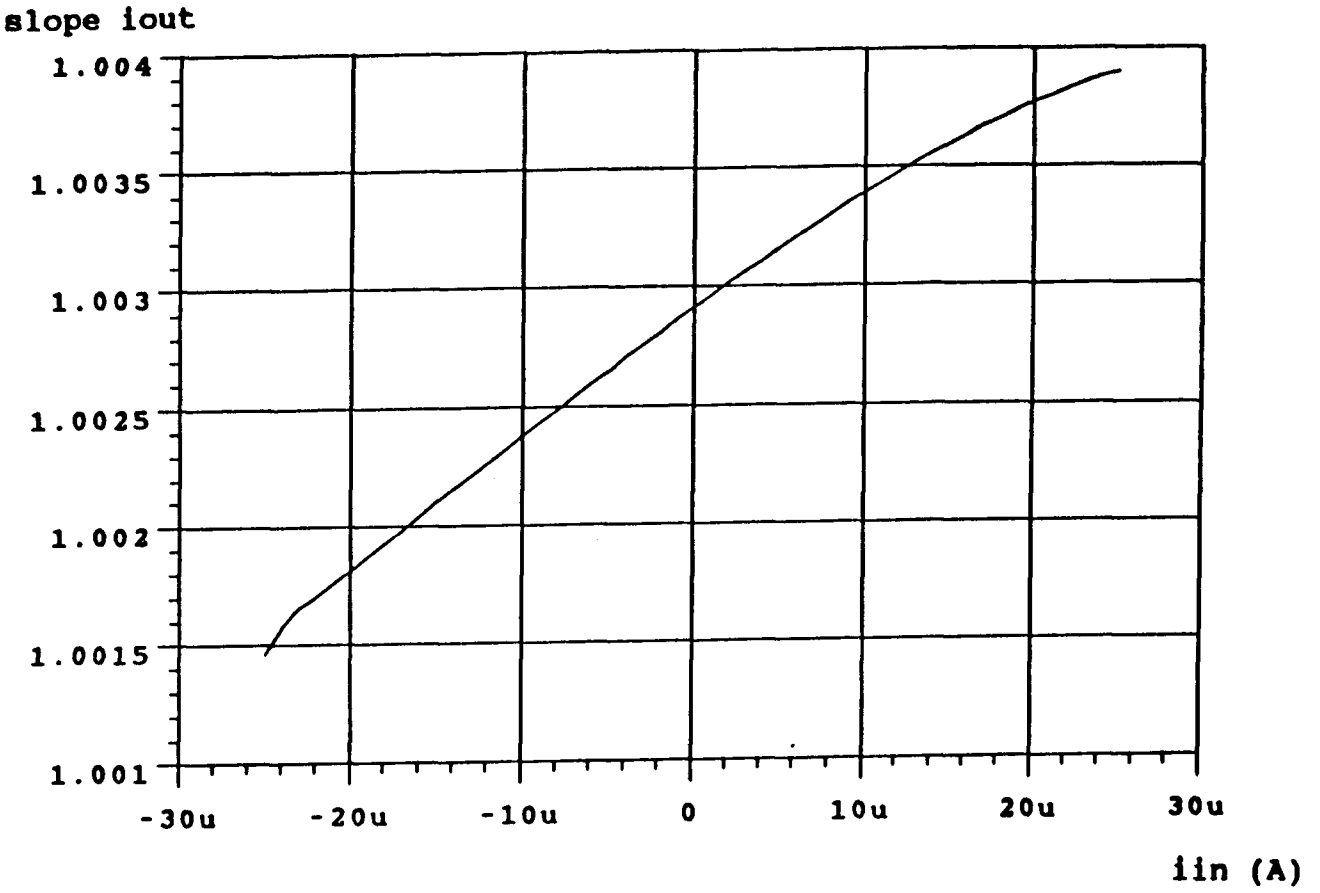


Figure 30. Slope of transfer curve.

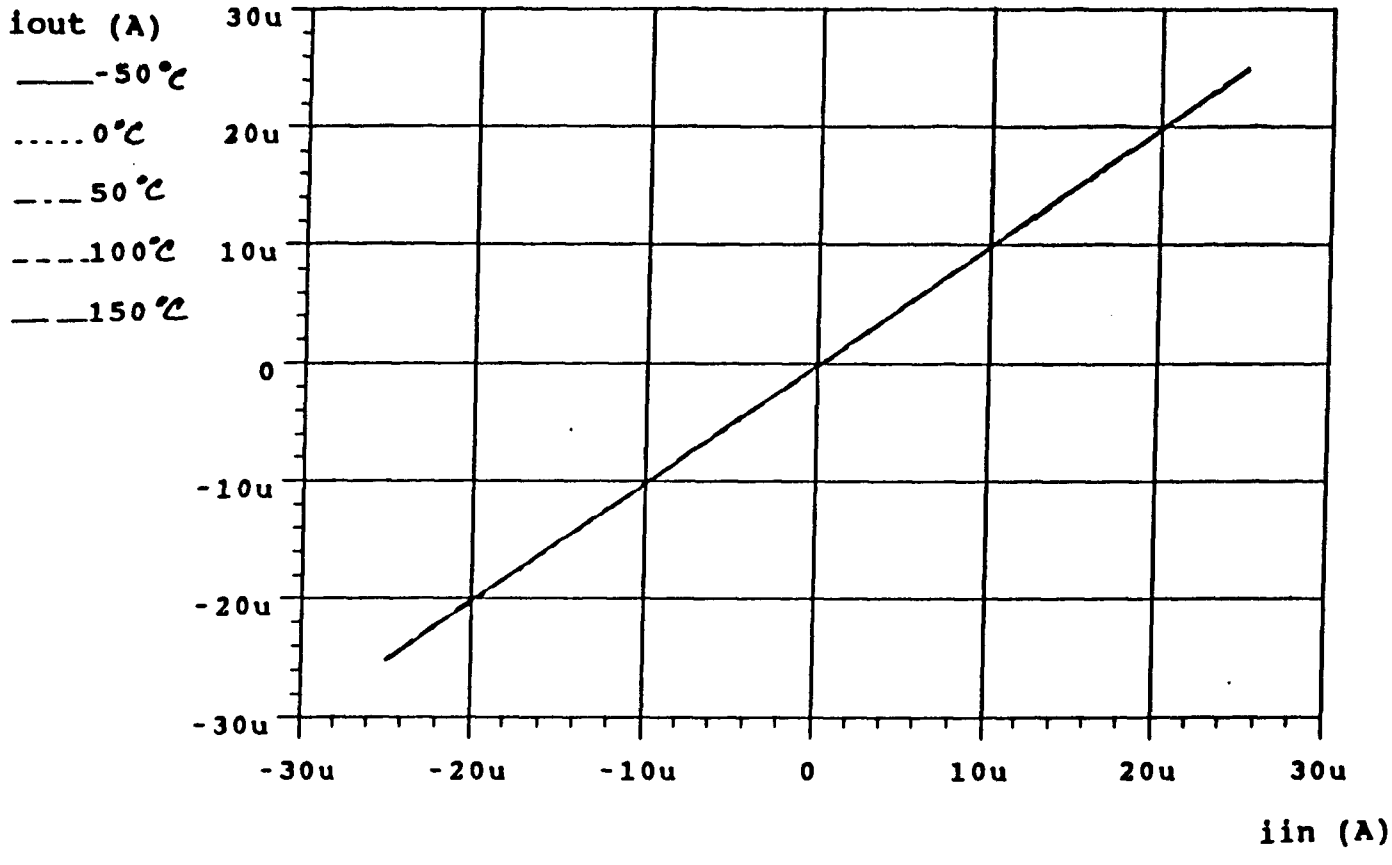


Figure 31. Transfer curve over -50 to +150 degrees C.

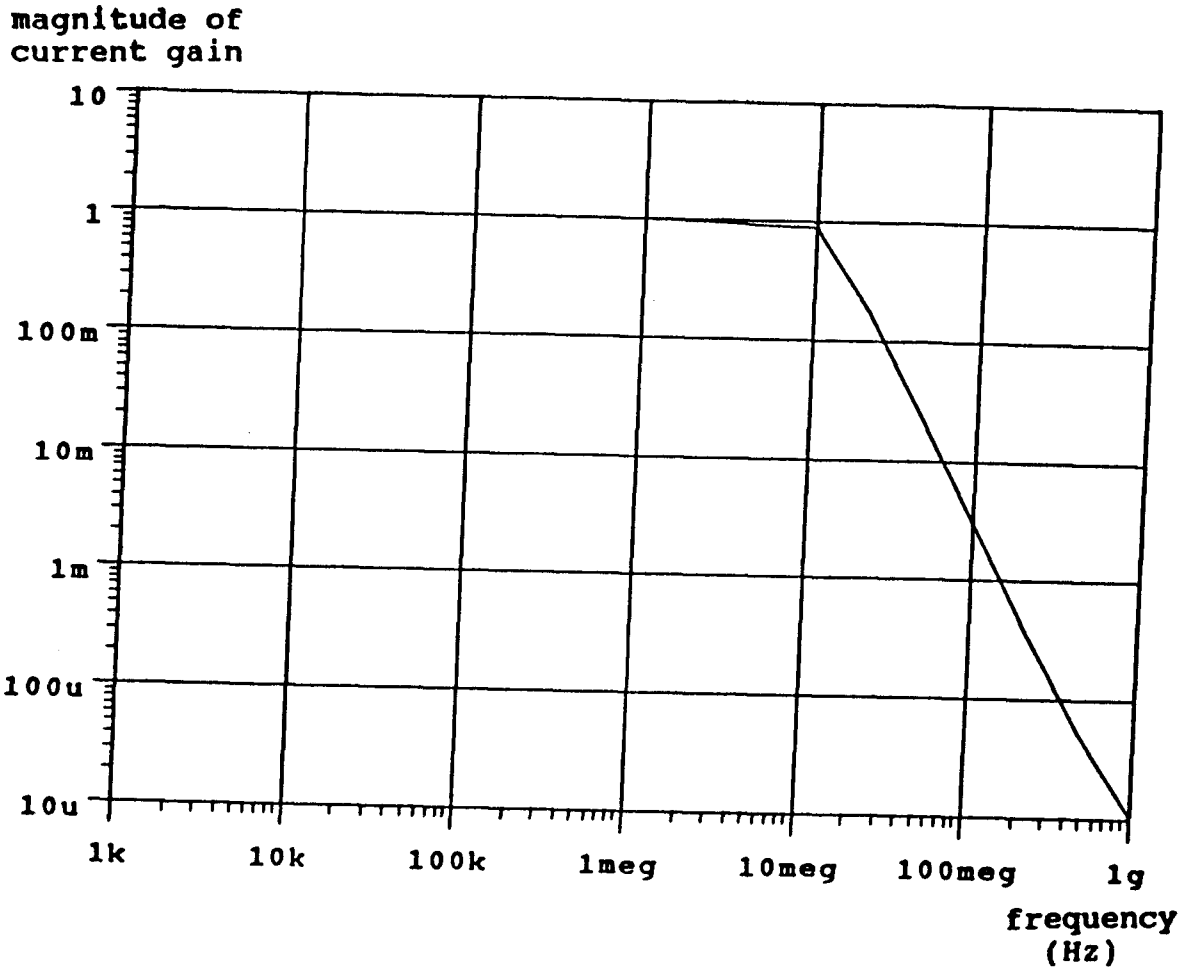


Figure 32. Magnitude response of CCCS.

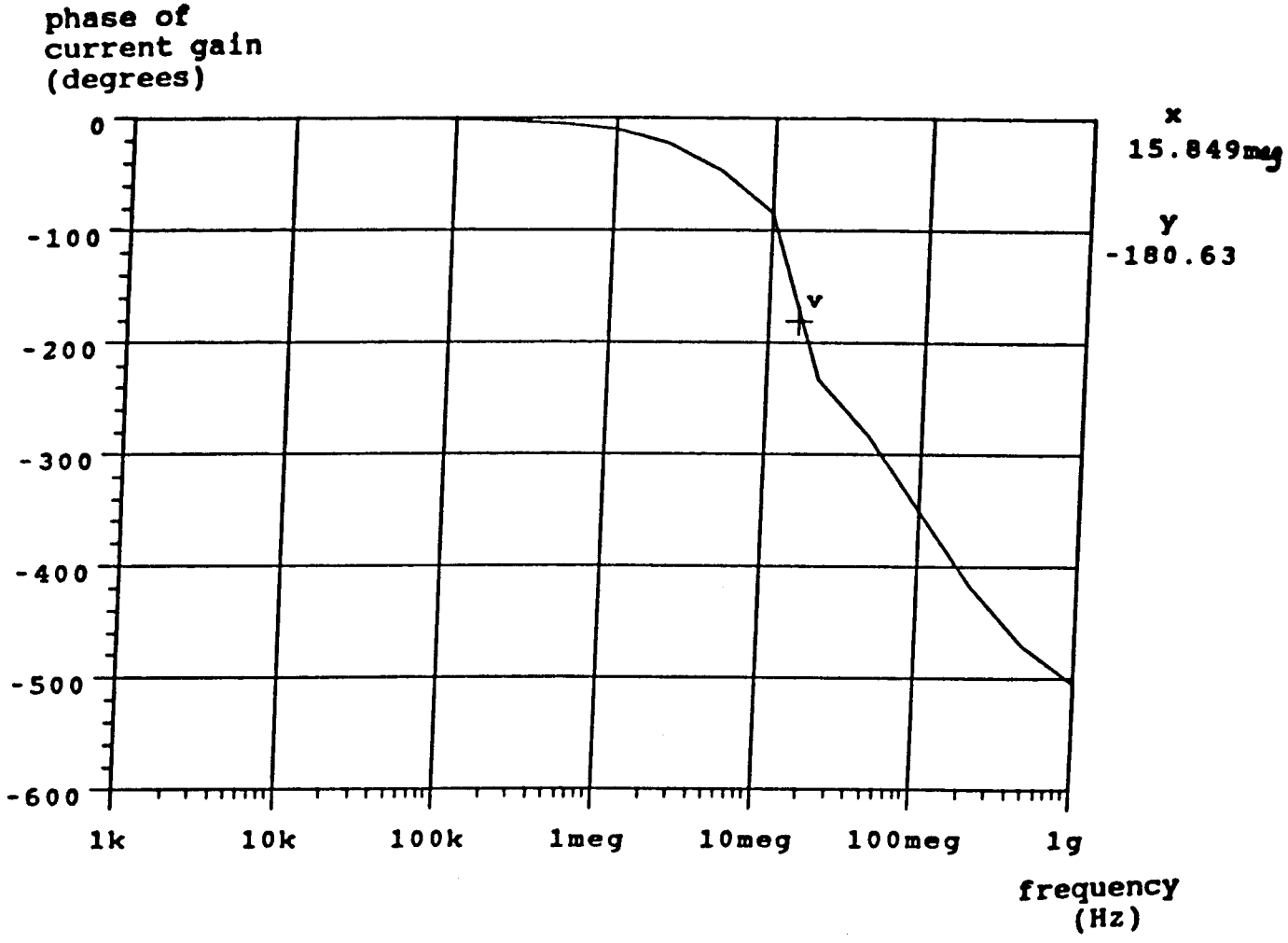


Figure 33. Phase response of CCCS.

Chapter 5. APPLICATION OF THE CCCS IN AN OPERATIONAL AMPLIFIER

The improved performance of the CCCS can be utilized in an operational amplifier. In order to be compatible with voltage signal processing circuits, it is desirable to keep the closed-loop input and output variables of an analog signal processing circuit as voltage variables. With this design however, it is not necessary to use high gain voltage amplifiers in the feedback configuration to achieve this end. As discussed in much recent literature, non-voltage-mode operational amplifiers have often been used to first realize VCVS type amplifiers, which are then used with feedback to design voltage operational amplifiers. The desire to treat the CCCS as a voltage amplifier in this way nullifies the original advantages. It will be shown that by using the CCCS directly, a VCVS operational amplifier can be formed which has a fairly constant -3dB bandwidth, independent of gain. That is, this design is not bound by the constant gain-bandwidth product rule which applies to voltage amplifiers.

Figure 34 shows a block diagram of the current-mode operational amplifier. The CCCS amplifier is described by the relationship

$$I_{out} = A_i(I_1 - I_2) \qquad (5.1)$$

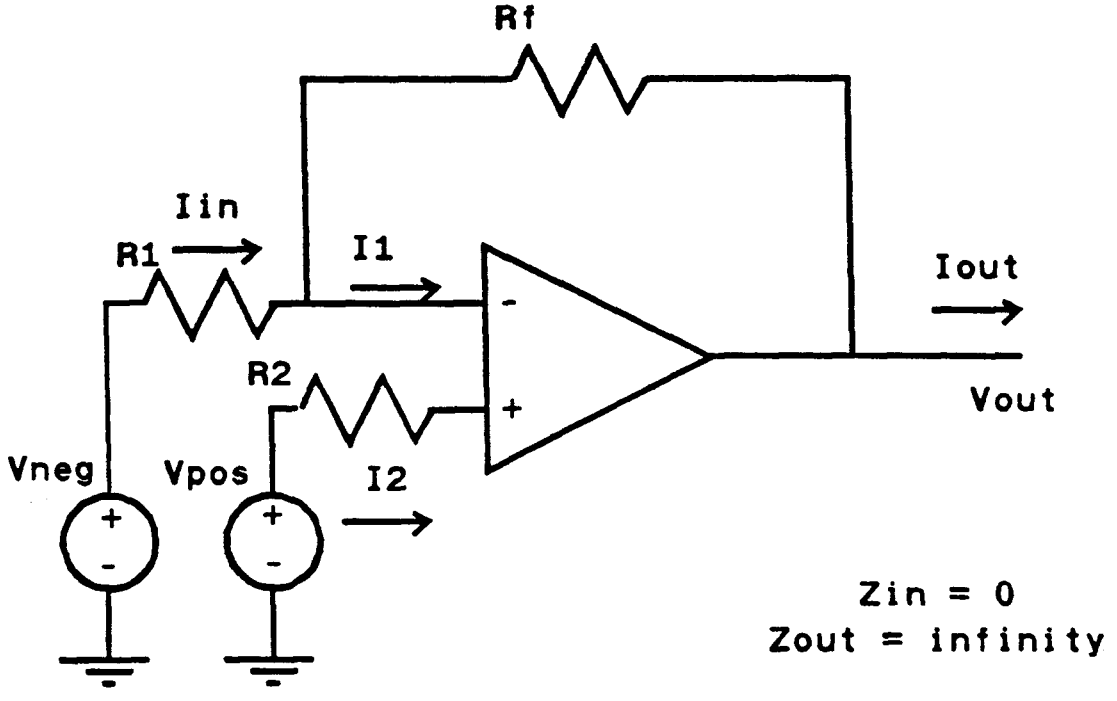


Figure 34. Block diagram of an ideal current-mode op amp.

where Ai is the current gain of the CCCS. Assuming that the input impedance approaches zero and the output impedance approaches infinity, the operational amplifier in Fig. 34 is described by

$$I2 = Vpos/R2 \tag{5.2}$$

and

$$I1 = -Iout + Iin$$
$$= (Vout/Rf) + (Vneg/R1). \tag{5.3}$$

Substituting (5.2) and (5.3) into (5.1)

$$\{Vout/Rf + Vneg/R1 - Vpos/R2\}Ai = -Vout/Rf$$

Rearranging, we obtain

$$Vout/Rf(Ai + 1) = Ai(Vpos/R2 - Vneg/R2)$$

and finally

$$Vout = [Ai/(Ai+1)]*\{Vpos(Rf/R2) - Vneg(Rf/R1)\}. \tag{5.4}$$

At this point it becomes clear why it was important to reduce Rin and increase Rout. By doing so, it can be assumed that all

current goes into the input node, and none goes into the output node, and therefore these equations hold true.

The closed-loop gains are -Rf/R1 and Rf/R2 for Vneg and Vpos respectively. Note that Ai is the only frequency dependent variable, and therefore the sole determinant of the -3dB bandwidth. This observation was first made by Parrish [16]. Recall that a voltage-mode operational amplifier has an open loop feedback of Av*B where B is related to closed loop gain, which gives rise to the gain/bandwidth dependence. Note from equation (5.4) that as Ai approaches infinity, Vout approaches

$$Vpos(Rf/R2) - Vneg(Rf/R1), \tag{5.5}$$

and as Ai approaches unity, Vout approaches

$$1/2*\{Vpos(Rf/R2) - Vneg(Rf/R1)\}.$$

Ai in the CCCS is controlled with device ratioing in the current mirrors, and it is not reasonable to attempt to have gain of much more than about 10, and a slight price is paid in bandwidth. Figure 35 is a simulation of the op amp operated with a compromise of Ai=4, providing a little greater gain for a small price in the original bandwidth of the CCCS, which was around 12.8 megahertz. Over this range of gain, bandwidth is between 1 to 2 megahertz. Note, however, that for the different levels of gain bandwidth varies little.

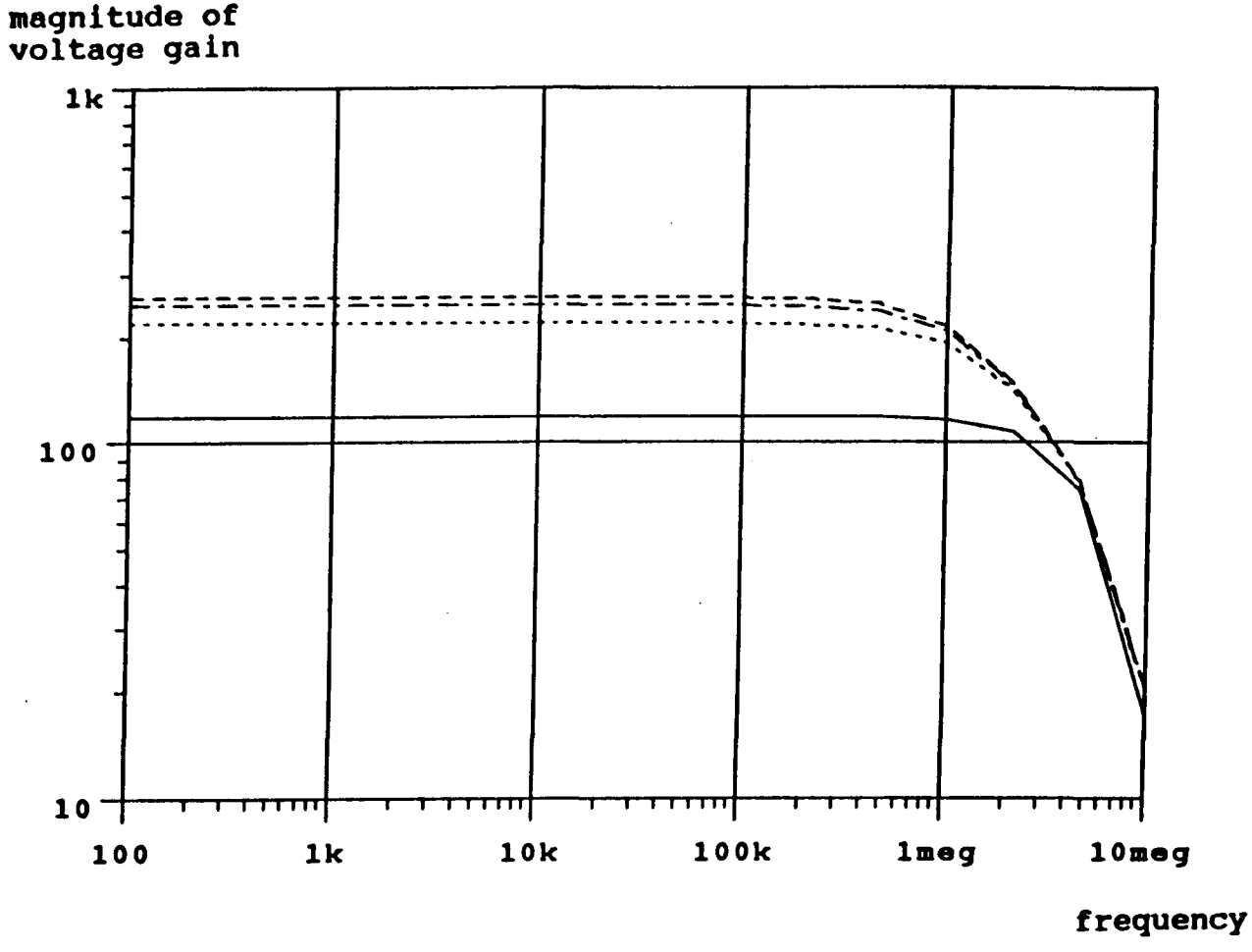


Figure 35. Simulation results for current-mode op amp.

Chapter 6. CONCLUSIONS

In conclusion, this research shows that current-conveyor theory and the Gilbert translinear principle can be applied to form a basic CCCS. By honing the Rin low, the Rout high and the current-gain bandwidth large, this basic CCCS can be used as a building block for an operational amplifier. The current-mode topology allows freedom from the constant gain-bandwidth product rule which governs voltage-mode topology op amps.

This unique aspect is useful in a variety of analog applications where it is desirable to be able to control gain independently from bandwidth, i.e. multipliers, dividers, squarers, higher-power-function generators, and geometry-correction systems.

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