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Title: Low Power Receivers for Wireless Sensor Networks

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Wireless sensor networks are becoming important in several monitoring and sensing
applications. Ultra low power consumption in the sensor nodes is important for extend-
ing the battery life of the nodes. In this dissertation, two low power BFSK receiver
architectures are proposed and verified with prototype implementations in silicion.

A 2.4 GHz 1 Mb/s polyphase filter (PPF) BFSK receiver demonstrates ± 180 ppm
frequency offset tolerance (FOT) and 40 dB adjacent channel rejection (ACR) at a mod-
ulation index (MI) of 2, with a power consumption of 1.9 mW. High FOT at low MI
is achieved by a frequency-to-energy conversion architecture using PPFs without any
frequency correction. The proposed hybrid topology of the PPF provides an improved
ACR at reduced power.

To further improve the energy efficiency, a low energy 900 MHz mixer-less BFSK
receiver is designed. High gain frequency-to-amplitude conversion and better sensitivity
is achieved by a linear amplifier with Q-enhanced LC tank, eliminating the need for

local oscillators and mixers. With a power consumption of 500 μW, the receiver achieves sensitivities of -90 dBm and -76 dBm for data rates of 0.5 Mb/s and 6 Mb/s, respectively. The energy efficiency is 80 pJ/b when operating at 6 Mb/s.

Low Power Receivers for Wireless Sensor Networks

by

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I understand that my dissertation will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my dissertation to any reader upon request.

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Ronghua Ni, Author

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Chapter 1: Introduction

1.1 Overview of Wireless Sensor Networks

After their first introduction in the early 2000s [1], wireless sensor networks (WSNs) have been used widely to monitor environmental parameters and transmit them wirelessly to a base station. The automatic data collection and communication through WSNs are time efficient and accurate. A typical WSN, as shown in Fig. 1.1, consists of multiple sensor nodes and a central hub. The sensor nodes are deployed in an ad-hoc fashion. The desired data is monitored by each sensor node, and then communicated
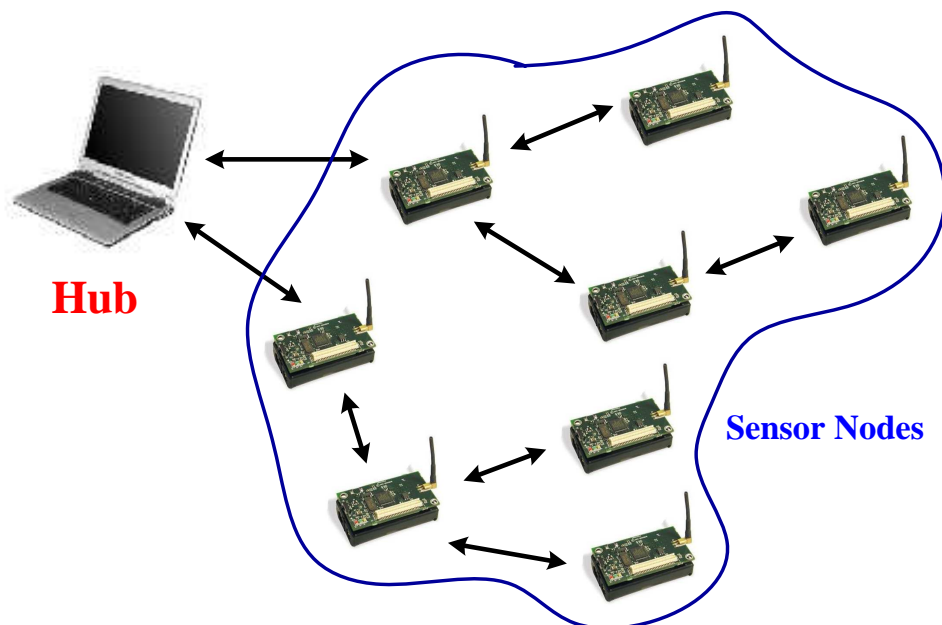
Figure 1.1: A typical wireless sensor network.

between itself and the surrounding nodes or the hub. The central hub collects the data for evaluation. The optimal communication path from the sensor nodes to the hub is either preprogrammed into the sensor nodes or dictated by the hub. While the hub is assumed to have an unlimited source of power, the sensor nodes are mostly operated on a small-size battery or energy harvester. Therefore, low power operation of the sensor nodes is of critical importance to extend the battery life of the WSNs or for reliable operation with energy harvesters.

1.1.1 Applications of WSNs

An important application of WSNs is building and home automation [2]. Environmental parameters that can be monitored include temperature, humidity, brightness, smoke, and carbon-dioxide. Unlike previous solutions that communicate using wires, wireless sensor nodes can be deployed everywhere within the building. These sensor nodes monitor the environment and are controlled by a central hub resulting in building automation.

Another application domain is industrial automation [3]. Installed in a manufacturing line, sensor nodes detect and report malfunctioning of machines. They also play an important role in inventory control during supply chain management. Furthermore, easy reconfiguration of sensor nodes dramatically reduces the installation cost and increases the flexibility for different industrial applications.

Wireless sensor nodes are also found commonly in traffic control systems [4]. Sensor nodes are deployed to detect the traffic flow, whereby traffic lights can be controlled in a dynamic and adaptive way. Live information about traffic congestion can be pro-

vided along with traffic routing advice. Multimedia sensor nodes can be used to monitor the speed of vehicles and detect traffic violations for traffic enforcement. Furthermore, smart parking system using WSNs allows monitoring available parking spaces and provide drivers with automated parking advice.

Medical monitoring is another domain that WSNs find wide applications [5]. Sensor nodes are attached to the body of a patient to track vital signs such as body temperature, heart/respiration rate, electrocardiogram, and fetus movement. With wireless connectivity, patients can move comfortably.

WSNs are also receiving increased attention in military applications, including battle field surveillance, battle damage assessment, enemy tracking, and nuclear or chemical attack detection.

1.1.2   Features and Requirements of WSNs

All WSNs, regardless of the application, share some common features and requirements as described below.

- Low cost:
  Since a network consists of a large number of sensor nodes, reducing the cost of each node is an important consideration. This limits the choice of the material and components, and increases the design challenges.

- Low power:
  As most of the sensor nodes are powered by small batteries or energy harvesters,

the power consumption should be minimized to prolong the lifetime of the network.

- Short range:

  The radio specification of WSNs are regulated by Federal Communications Commission (FCC) [6]. In the United States, the radio communication of WSNs is confined within ISM bands, with a maximum transmitted power of 1 W. On the receiver side, the sensitivity is generally not better than -90 dBm for the trade for low power consumption. These limit the maximum node distance for reliable communication. As a result, most of the WSNs operate within a distance ranging from 5 meters to 15 meters.

- Good interferer tolerance:

  The unlicensed ISM bands, where the WSNs operate, are crowded with multiple radio standards as shown in Fig. 1.2. Consequently, the sensor nodes must operate with the presence of interferers that may be strong enough to block the desired signal. In some applications, such as medical monitoring and military surveillance where communication reliability is important, retransmission is required and the total power consumption can be potentially high. In addition, the latency introduced by multiple transmissions is intolerable in some emergency applications such as fire detection. Therefore, good interferer tolerance is required in the sensor receivers.

Cordless Phone
DSSS / FHSS

Zigbee
DSSS

Cordless Phone
DSSS / FHSS

Bluetooth
FHSS

WirelessUSB
DSSS

802.11b
DSSS

Zigbee
DSSS

2MHz   1.2MHz

10MHz   15MHz   1MHz   22MHz   3MHz

902 ~ 928MHz

2.4 ~ 2.4835 GHz

Cordless Phone
DSSS / FHSS

802.11a
OFDM

UWB, DS-UWB, OFDM

22MHz

5.725 ~ 5.85 GHz
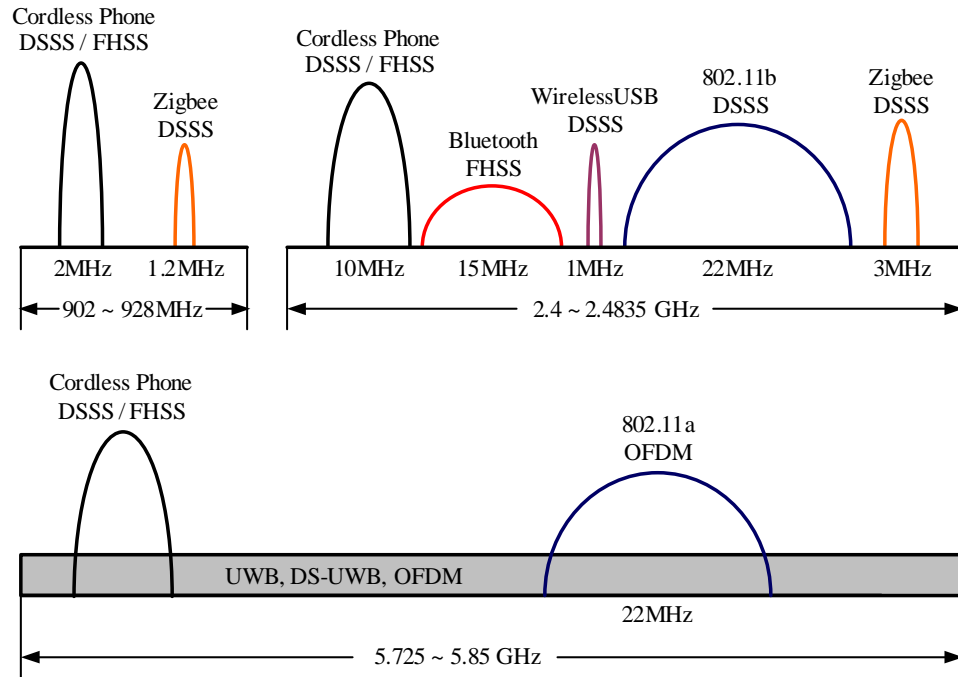
Figure 1.2: Radio systems in ISM bands.

1.2 Dissertation Motivation

The anatomy of a typical sensor node is shown in Fig. 1.3. The power source of a node can be a battery or stored energy harvested from the environment. A power management unit supplies power to the whole node. The desired data is acquired by the sensor and then converted to a digital signal through an analog-to-digital converter (ADC). The CPU either gets data from the ADC and sends it to the transmitter (TX) or receives data from the receiver (RX) for processing. The memory block may be used for either program code or data storage. The transceiver (TX/RX) is the wireless interface responsible for the communication between the nodes or between a node and the hub. Awake from the sleep mode with a small duty cycle, the average power consumption of the sensor
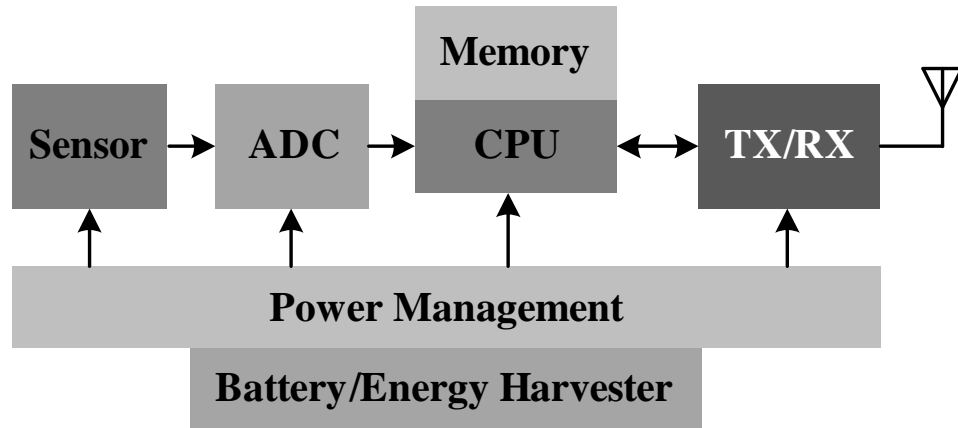
Figure 1.3: Block diagram of a typical wireless sensor node.

nodes is significantly reduced.

To maximize the battery life of a sensor node, low power consumption is a high priority in the design of sensor nodes. In all the building blocks shown in Fig. 1.3, the wireless transceiver is the most power hungry block [7]. Therefore, it is critical for the transceiver to consume the lowest amount of power while still maintaining the required performance. This dissertation focuses on low power consumption for receivers in wireless sensor networks.

1.3 Dissertation Organization

This dissertation develops and demonstrates two architectures for low power wireless receivers in WSNs. Chapter 2 provides a review of the state-of-the-art low power receivers for WSNs, with a discussion on their advantages and disadvantages. A 2.4 GHz hybrid polyphase filter based BFSK receiver is presented in Chapter 3, which achieves

low power consumption, high frequency offset tolerance, and high adjacent channel rejection. To further improve the energy efficiency, a new 900 MHz mixer-less BFSK receiver with Q-enhanced frequency-to-amplitude conversion is developed in Chapter 4. This receiver achieves excellent sensitivity as well as energy efficiency without the use of local oscillators and mixers. Finally, conclusions are drawn in Chapter 5.

Chapter 2: A Review of Low Power Receivers for Wireless Sensor Network

In recent years, many architectures have been developed or improved for WSNs tailored to different applications. Even though the requirements are different to meet various application requirements, they share some commonalities to achieve low power consumption. In this chapter, the features and design specifications that are general to low power WSN receivers will be discussed. Afterwards, the state-of-the-art receivers for WSN applications will be reviewed along with a discussion of their advantages and disadvantages.

2.1 Design Specifications

2.1.1 Modulation Scheme

To minimize the power consumption of the receiver, simple modulation schemes such as on-off keying (OOK) or binary frequency shift keying (BFSK) are widely adopted. Despite a poor spectral efficiency, the modulation and demodulation of OOK or BFSK signals are simpler and more power efficient.

An OOK transmitter consumes less power than a BFSK transmitter due to the duty cycling of the power amplifier (PA). However, the finite on-off time of the PA limits

the maximum data rate for OOK modulation schemes. Furthermore, BFSK transmitters radiate constant envelope waveforms which relaxes the linearity requirement of the PA, therefore improving the power efficiency of the PA and transmitter. Finally, BFSK modulated signals are less vulnerable to channel noise compared with OOK modulated signals.

2.1.2   Data Rate

The data rate in wireless communication systems is determined by multiple factors. Different applications require different data throughput. For example, home automation WSNs monitoring indoor temperatures normally have a data rate smaller than 100 kb/s, since the desired data to be transmitted is small. On the other hand, higher data rates (typically larger than 1 Mb/s) are necessary for WSNs that transmit video or audio information or in applications that require minimum latency, e.g., fire or chemical detection.

From the standpoint of circuit design, the data rate is a trade-off between the energy efficiency and sensitivity of the receiver. The energy efficiency (defined as energy per bit, E_b) is given by

$$E_b = \frac{P_{RX}}{DR}, \tag{2.1}$$

where P_{RX} and DR are the power consumption and data rate of the receiver, respectively. This improves with increased data rate. The receiver sensitivity is

$$P_{sen} = kT \cdot NF \cdot SNR_{min} \cdot BW, \tag{2.2}$$

where k is the Boltzmann constant, T is the absolute temperature, NF is the noise figure of the receiver, SNR_{min} is the minimum signal-to-noise ratio (SNR) required by the demodulator, and BW is the signal channel bandwidth. A larger data rate will increase both SNR_{min} and BW, thereby degrading the receiver sensitivity. A data rate that provides a balance between E_b and P_{sen} is selected through system level analysis and simulation.

2.1.3   Sensitivity

In wireless sensor network applications, the radiated power from the transmitter is approximately 0 dBm [8]. The path loss (*PL*) of RF signal propagation comprises free space loss, attenuation, and scattering, which can be modelled as

$$PL = (\frac{4\pi}{\lambda})^2 \cdot d^n \cdot A \tag{2.3}$$

where $\lambda = c/f$ is the wavelength of the signal ($c = 3\times10^8 m/s$ is the speed of light), d is the communication distance, $n = 2\sim5$ is the scattering exponent, and $A = 0\sim30dB$ is the attenuation when the RF signal passes through solid objects [9]. In most applications, $n = 3.5$ and $A = 15dB$ represents the worst case, whereby the path loss for signals in 900 MHz and 2.4 GHz ISM bands is shown in Fig. 2.1. If a transmitted power of 0 dBm is assumed, the required sensitivity is approximately -80 dBm and -90 dBm for 915 MHz and 2.45 GHz radio systems, respectively.
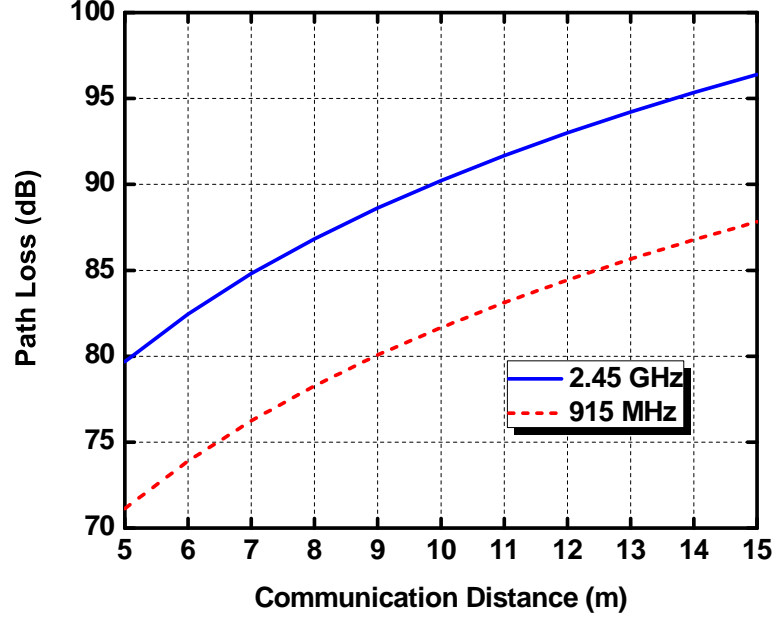
Figure 2.1: Typical path loss of RF signals in 900 MHz and 2.4 GHz ISM bands.

2.1.4 Start-up Time

The start up time is the time between when the receiver is powered on until it is ready to receive data. It includes the settling time of the local oscillators (LOs), the operating time of the calibration circuits, and the settling time of the biasing circuits. This incurs energy consumption overhead in addition to the energy consumed to receive data. Therefore, the effective energy efficiency for one data packet is

$$E_b = E_{b,start} + E_{b,on} = \frac{P_{start}}{N_{bit}} + \frac{P_{on}}{DR}, \tag{2.4}$$

where P_{start} is the power consumption of the receiver during the start-up time, N_{bit} is the packet size, P_{on} is the power consumption of the receiver when receiving data. $E_{b,start}$

is the energy consumption overhead due to start-up, while $E_{b,on}$ is the useful energy consumption for receiving data. $E_{b,start}$ is a concern when the packet size N_{bit} is small, because $E_{b,start}$ will be comparable to $E_{b,on}$. As a consequence, the start-up time should be minimized to improve the total energy efficiency.

2.2 State-of-the-Art Low Power Receivers

2.2.1 Power-Detection Receivers

The system architecture of power-detection receivers [10–14] is shown in Fig. 2.2. The received signal is amplified at the radio frequency followed by an envelope detector (ED). Afterwards, the amplitude of the envelope is compared with a reference voltage to retrieve the data. This structure is one of the most energy efficient receiver architectures because it doesn't need power hungry LOs and mixers. However, only the OOK modulation scheme can be used with this architecture. Also, without high Q filtering in the radio frequency band, the interference rejection is poor.

Frequency selectivity and interference rejection have been improved by using thin-
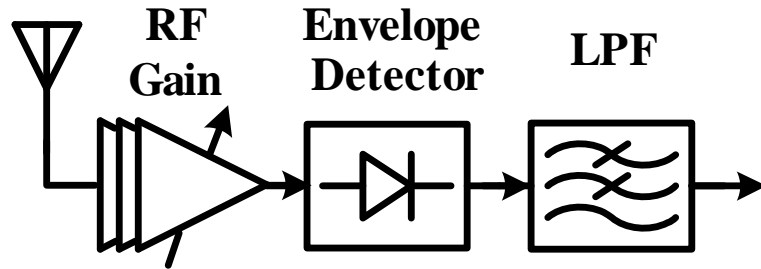
Figure 2.2: Power detection receiver.

film bulk acoustic wave (FBAR) resonators inside RF amplifiers [10] or surface acoustic wave (SAW) filters before RF amplification [11]. The FBAR resonator or SAW filter considerably increases the sensor node size and cost.

2.2.2 Super-regenerative Receivers

The super-regenerative receiver is another energy efficient receiver architecture widely used in WSNs. As shown in Fig. 2.3, it is based on a super-regenerative oscillator (SRO), which is quenched between two sequential bits and starts oscillating with a build-up time determined by the input RF signal. The difference in build-up time is used to retrieve the data. Both OOK [15–18] and BFSK [19, 20] modulated signals can be received by a super-regenerative receiver. However, the maximum data rate, limited by the build-up time of the SRO, is about 1 Mb/s. Also, the frequency selectivity is determined by that of the SRO, which is normally similar to that of the power detection receivers.
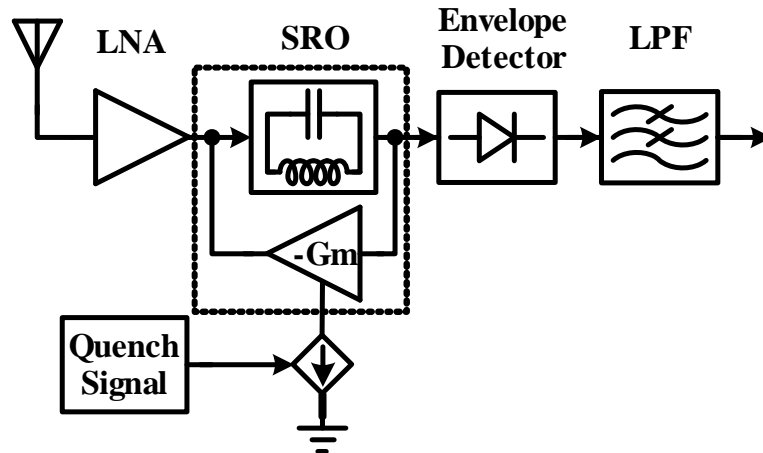
Figure 2.3: Super-regenerative receiver.

A high-Q bulk acoustic wave (BAW) [15] resonator in the SRO provides a narrow intrinsic bandwidth. However, this reduces the quench frequency and increases the cost. Q-enhancement techniques presented in [16, 20] utilize successive approximation register (SAR) logic to calibrate the quench current signal which enhances the selectivity of the filtering.

2.2.3 Injection-Locked Receivers

Two types of injection-locked receivers have been developed for BFSK wireless sensor networks. One is the phase-locked loop (PLL) based injection-locked receiver [21] as shown in Fig. 2.4(a). The VCO is injection locked to the frequency of the input signal, and data can be retrieved by monitoring the output of the charge pump. The other injection-locked receiver is based on envelope detection [22] as shown in Fig. 2.4(b). When injection locked by the input signal at different frequencies, the amplitude of the oscillation is different and is used for data discrimination.

There are two main drawbacks for injection-locked receivers. First, the injection locking range ω_L is [23]

$$\omega_L = \frac{\omega_0}{2Q} \cdot \frac{v_{inj}}{v_{osc}}, \tag{2.5}$$

where ω_0 and v_{inj} are the radian frequency and amplitude of the injecting signal, respectively. Q and v_{osc} are the loaded quality factor and oscillation amplitude of the injection-locked oscillator, respectively. To guarantee that the oscillator is injection-locked, a relatively large ω_L is required. This translates to a larger input power, i.e., a degraded sensitivity. Second, the injection-locked receiver is sensitive to an interferer

Date Out

Reference

CP2

CP1

PFD

Lock
Detector

**Leakage
Buffer**

VCO

LNA

1/N

(a)

LNA

**Injection-
Locked
Oscillator**

**Envelope
Detector**

Comparator

Data

V_{REF}

(b)
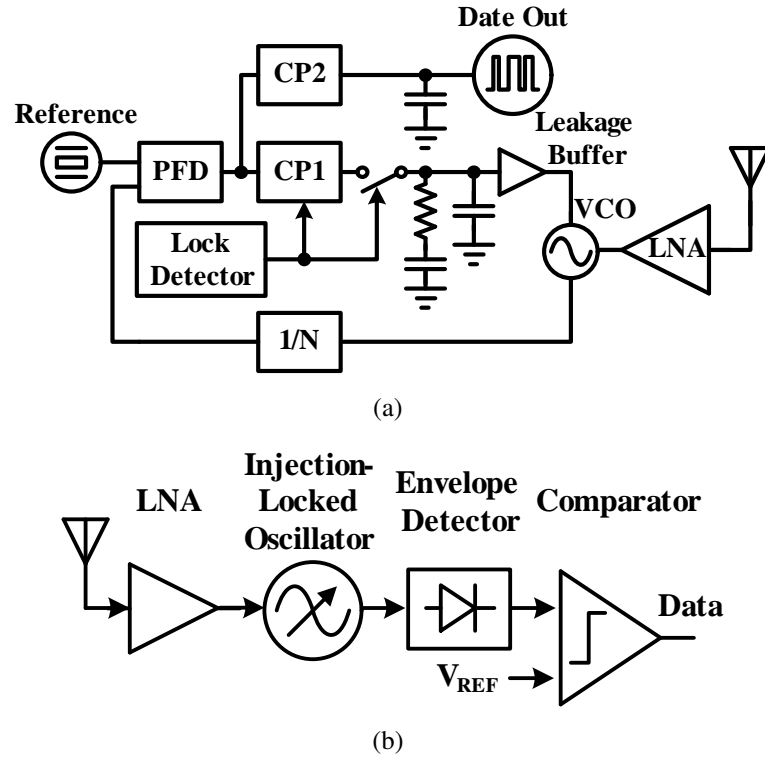
Figure 2.4: Injection-locked receivers. (a) PLL based. (b) Envelope detector based.

near its locking range. Once injection locked or pulled by a strong interferer, the receiver sensitivity is significantly degraded.

2.2.4 Low-IF/Zero-IF Receivers

Low-IF/zero-IF receivers [24–34], as shown in Fig. 2.5, downconvert the RF signal to baseband where channel filtering and signal demodulation occur at low frequency. While excellent frequency selectivity can be achieved by virtue of the high Q filtering from baseband filters, the power consumption of low-IF/zero-IF receivers is usually

Mixer **Filter**
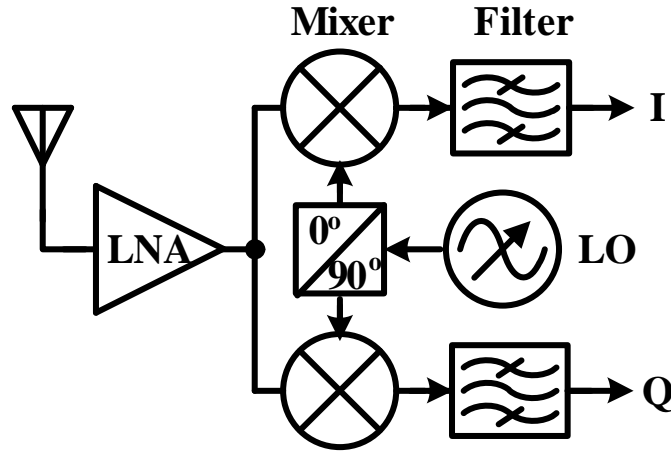
Figure 2.5: Low-IF/zero-IF receiver.

higher than that of the aforementioned architectures. Low-IF/zero-IF receivers need power hungry LO generation circuits and mixers. However, the achievable sensitivity is better than that of the aforementioned architectures due to the excellent noise filtering.

Various techniques have been developed to reduce the power consumption of low-IF/zero-IF receivers without significantly impacting the performance. In [27], a fully passive RF front-end utilizing an integrated resonant matching network between antenna and passive mixer achieved ultra-low power and good linearity from a 0.4 V supply voltage. Current-reuse was extensively used in [28] to minimize the current drawn from the supply. [34] proposed a receiver with an uncertain-IF architecture, which combined MEMS-based high-Q filtering and a free-running CMOS ring oscillator as the RF LO.

2.2.5 Ultra-wide Band Receivers

Ultra-wideband (UWB) receivers have also recently been used to achieve low energy data reception. In these receivers, a super-regenerative or low-IF/zero-IF front end is used along with a FSK, phase-shift keying (PSK), or pulse position (PPM) modulation scheme [35–39]. The instantaneous power consumption is normally higher than that of the narrow-band receivers. However, the maximum data rate is larger, therefore the resulting energy efficiency E_b is similar to that of the narrow-band receivers. For this reason, UWB is a good choice when a high data rate is necessary in certain applications. In-band interference rejection is inherently improved for UWB radios due to the frequency spreading modulation schemes. Nevertheless, the communicate range for UWB radios is severely limited, because FCC mandates that UWB transmitters can radiate no more than -41.3 dBm/MHz effective isotropically radiated power (EIRP) in the UWB band (from 3.1 GHz to 10.6 GHz) [40].

2.3 Performance Summary and Comparison

The performance of the state-of-the-art low power OOK and BFSK receivers for WSNs is summarized in Table 2.1. This dissertation focuses on narrow-band receiver design for WSNs with a data rate of approximately 1 Mb/s and a communication distance of about 10 meters. Therefore, UWB receivers are not included within comparison. Referring 2.1, the mixer-less structures (power-detection, super-regenerative, and injection-locked receivers) are preferred for ultra-low power operation due to the absence of power hungry LOs and mixers. However, the sensitivity and interference rejection is limited

Table 2.1: Performance Summary of State-of-the-Art Low Power Receivers for WSNs

Ref.	Arch.	Tech. (m)	Freq. (GHz)	Mod.	DR (kb/s)	Power (mW)	E_b (nJ/b)	Sen. (dBm)	Select. (dB)
[10]	PD*	0.13	1.9	OOK	40	3.6	90	-78	-3@3M
[11]	PD	0.18	0.9	OOK	1000	2.6	2.6	-65	N/A
[12]	PD	0.09	1.9	OOK	100	0.065	0.65	-48†	-3@7M
[13]	PD	0.09	0.9	OOK	10	0.051	5.1	-80	N/A
[14]	PD	0.09	0.9	OOK	10	0.123	12.3	-86	N/A
[15]	SR*	N/A	1.9	OOK	5	0.4	80	-100.5	-3@5M
[16]	SR	0.13	2.4	OOK	500	2.8	5.6	-80	-3@0.9M
[17]	SR	0.09	0.4	OOK	120	0.4	3.3	-93	-25@0.5M
[18]	SR	0.18	1.3	ASK	156	0.91	5.83	-80	N/A
[19]	SR	0.18	0.9	BFSK	1000	0.4	0.4	-80	N/A
[20]	SR	0.18	2.4	BFSK	2000	0.35	0.175	-75	-12@5M
[21]	IL*	0.13	5.2	BFSK	5	5.5	1100	N/A	N/A
[22]	IL	0.18	0.9	BFSK	5000	0.42	0.084	-73	-10@30M
[24]	IF*	0.5	0.434	BFSK	24	1	41.7	-95	-50@1M
[25]	IF	0.25	0.9	BFSK	20	1.2	60	-94	-55@5M
[26]	IF	0.18	0.87	BFSK	25	2.52	101	-108	N/A
[27]	IF	0.13	2.4	BFSK	300	0.33◇	1.1	N/A	N/A
[29]	IF	0.13	0.9	BFSK	50	2.5	50	-102	-47@1M
[30]	IF	0.13	0.9	BFSK	45	1.92	42.7	-89	N/A
[31]	IF	0.18	0.4	BFSK	200	8.5	42.5	-76	40@300k
[31]	IF	0.18	0.05	BFSK	2500	5.7	2.28	-65	30@1.5M
[32]	IF	0.18	0.075	BFSK	10000	3.7	0.37	-65	N/A
[33]	IF	0.18	0.4	BFSK	250	0.49	1.96	-70	13@300k
[34]	IF	0.09	2	OOK	100	0.054	0.54	-72	-8@20M

* PD: Power Detection.   SR: Super-Regenerative.
    IL: Injection-Locked.   IF: Low-IF/Zero-IF.
† For a detection probability of 90%.
◇ VCO included, without phase-locked loop or frequency-locked loop.

due to the absence of high-Q filtering in the radio frequencies. On the other hand, mixer-

based low-IF/zero-IF receivers inherently demonstrate larger data rates, better sensitivity

and interference tolerance at the cost of a larger power consumption. With these observations in mind, two new receiver architectures are presented in this dissertation. One is a mixer-based zero-IF BFSK receiver achieving high frequency offset tolerance and excellent interference rejection at a reduced power consumption. The other is a mixer-less Q-enhanced BFSK receiver demonstrating improved sensitivity and higher data rates.

Chapter 3: A 2.4 GHz Hybrid Polyphase Filter Based BFSK Receiver with High Frequency Offset Tolerance

A low power 2.4 GHz hybrid polyphase filter (PPF) based BFSK receiver with high frequency offset tolerance (FOT) at small modulation indexes (MIs) is presented for medium data rate wireless sensor network (WSN) applications. A high FOT at low MI is achieved by a frequency-to-energy conversion architecture using PPFs without any frequency correction circuits. Channel selection and interference rejection are performed simultaneously by the PPFs without any extra hardware and power consumption. Furthermore, the proposed hybrid topology of the PPFs provides an improved adjacent channel rejection (ACR) at reduced power. The prototype receiver fabricated in a 0.13-μm CMOS process, including the RF and analog front-ends, consumes 1.97 mW from a 1 V supply. With a data rate of 1 Mb/s, a sensitivity of -84 dBm, a FOT of $\pm$450 kHz ($\pm$180 ppm), and an ACR of 40 dB are achieved for a MI of 2.

3.1   Introduction

Most of the early WSN transceivers were optimized for low data rates (typically less than 100 kb/s) for applications with low average data throughput [15, 24, 25, 29, 30]. However, a medium data rate in the range of Mb/s is preferred in applications with large amounts of data for improved energy efficiency [41] and reduced latency. Examples of

these applications include wireless multimedia sensor networks [42], multi-point body area networks [43], and patients' biomedical monitoring [44].

A zero-IF receiver architecture achieves a good compromise between interference rejection and power consumption. Therefore, it is widely used in low-power receiver designs operating in the ISM bands. BFSK modulation is preferred over OOK as it is more robust to interferers and allows for high efficiency nonlinear power amplification in the transmitter. The conventional zero-IF BFSK receivers based on D flip-flops (DFFs) [45, 46] or cross differentiate and multiply (CDM) [47, 48] demodulators are widely used in WSNs because of simple hardware requirements and low power consumption. The receiver architecture is shown in Fig. 3.1(a). The MI is $2\Delta f/f_m$ (Fig. 3.1(b)), where Δf is the peak deviation frequency from the carrier frequency (f_c) and $f_m = 1/T$ (T is the data period) is the frequency of the baseband modulating signal. Figure 3.1(c) shows the ideal input waveforms to the DFF/CDM based demodulator with MI = 2. No noise or filter-introduced inter-symbol interference (ISI) are included. The data is retrieved by detecting the phase (zero-crossing) lead/lag of the in-phase and quadrature (I/Q) signals.

Conventional low power BFSK receivers utilize data rates less than 100 kb/s and MIs greater than 6 to ease the demodulation [24, 25, 30]. However, a MI as small as 2 is required in medium data rate applications for reduced power consumption, reasonable spectral efficiency and improved interference rejection. With a data rate of 1 Mb/s and a MI smaller than 2, the sensitivity of the conventional DFF/CDM based receivers degrades dramatically with the frequency offset, f_{off}, between the transmitter and receiver local oscillators (LOs). This mandates the use of an accurate frequency
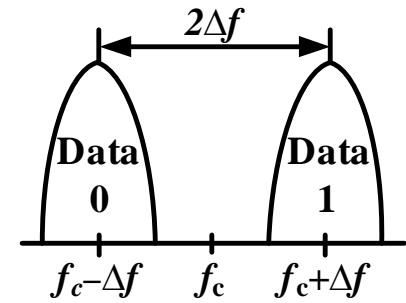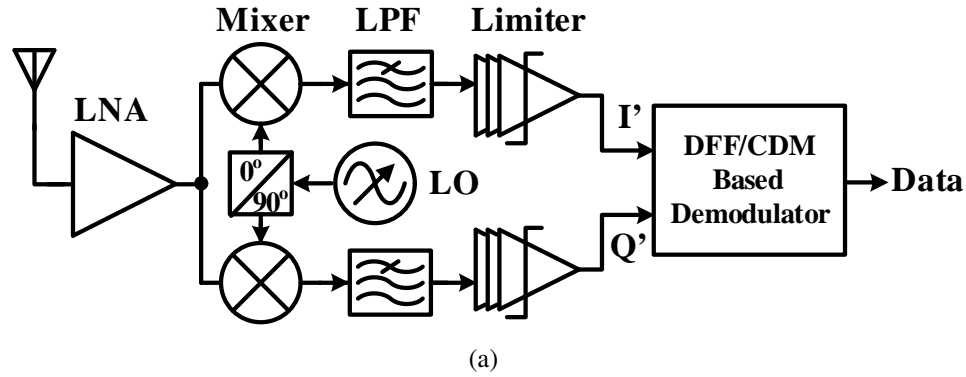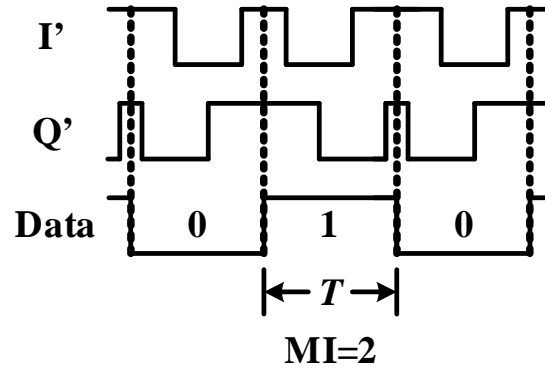
Figure 3.1: (a) Conventional DFF/CDM based zero-IF BFSK receiver using zero-crossing detection. (b) Definition of BFSK modulation index. (c) Ideal I'/Q' waveform input to the DFF/CDM based demodulator with MI = 2. No noise or ISI is included. Data is retrieved by detecting the zero-crossing lead/lag of the I'/Q' signals.

source [17] or extra automatic frequency correction circuits [29, 49]. The power overhead and hardware complexity for both solutions are prohibitive for low power medium data rate WSN applications.

This chapter presents a low power PPF based zero-IF BFSK receiver with low MI, high FOT and high ACR [50]. Unlike the conventional frequency-to-phase DFF/CDM

based demodulators, the proposed topology converts data detection from frequency to energy domain. This significantly improves the FOT without the use of any automatic frequency correction circuits. PPFs were originally utilized to reject image signals in low-IF receivers [51, 52], but are seldom used in zero-IF receivers. Although a PPF was used as a demodulator in a zero-IF BFSK receiver in [24], extra filters were required for channel selection and interference rejection. Furthermore, the receiver in [24] had a low data rate (24 kb/s) and a large MI (8.3). The hybrid PPF based receiver architecture proposed in this work simultaneously achieves frequency-to-energy conversion, channel selection, and interference rejection within the PPFs. This leads to a reduction in the hardware and power consumption. In addition, an improved ACR is obtained at reduced power consumption with the hybrid topology of the PPFs.

The rest of the chapter is organized as follows. Section 3.2 describes the receiver architecture. In Section 3.3, the FOT of the receiver is analyzed, simulated and compared with those of conventional receivers. The bandwidth and order of the PPF is optimized for maximum FOT, and the hybrid topology for PPFs is described. Details of the circuit implementation are explained in Section 3.4, while Section 3.5 shows the experimental results and the summary is provided in Section 3.6.

3.2   Receiver Architecture

The architecture of the proposed BFSK receiver is shown in Fig. 3.2(a). The received
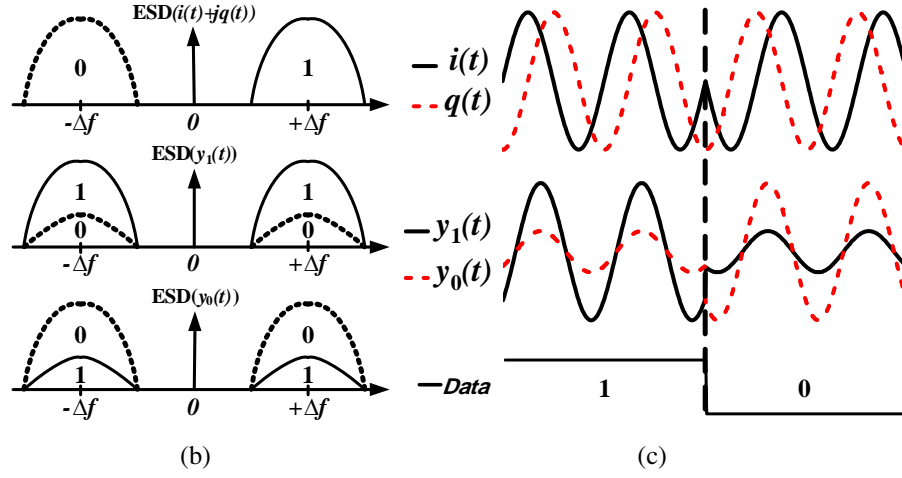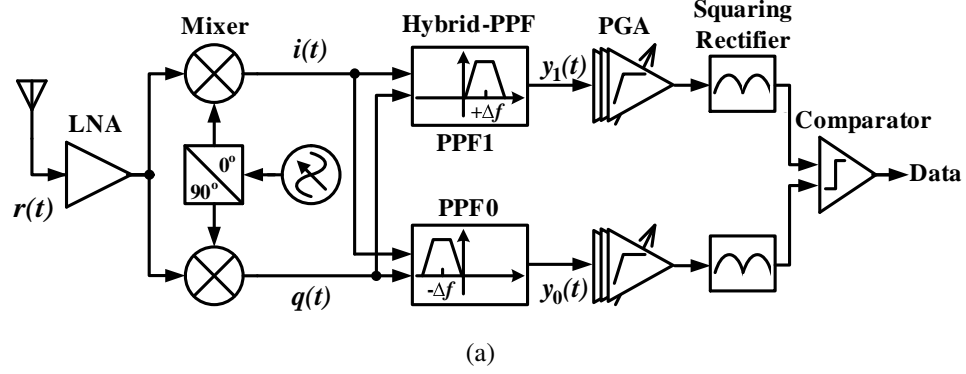
Figure 3.2: (a) Hybrid PPF based receiver architecture using frequency-to-energy conversion. (b) Input and output energy spectral density (ESD) for the PPFs. (c) Ideal input and output waveforms for the PPFs. Data is retrieved by detecting the squared amplitude (energy) of the y_1/y_0 signals.

RF signal from the antenna is

$$r(t) = A_{RF}\cos(2\pi f_i t + \varphi) \quad 0 \ll t \ll T, \ i = 1, 2 \tag{3.1}$$

where A_{RF} is the amplitude of the RF signal, $f_1 = f_c - \Delta f$ and $f_2 = f_c + \Delta f$ are the modulated frequencies for a transmitted data "0" and "1", respectively. φ is an arbitrary constant. After amplification by a low noise amplifier (LNA) and down-conversion to DC by a quadrature mixer, the complex baseband signal is

$$X(t) = i(t) + jq(t) = r(t) \cdot CG_{RF} e^{-j2\pi f_c t} = \begin{cases} A_{Mixer} e^{j(-2\pi\Delta f t + \varphi)} & \text{data is 0} \\ A_{Mixer} e^{j(+2\pi\Delta f t + \varphi)} & \text{data is 1} \end{cases} \quad 0 \quad t \quad T$$

$$(3.2)$$

where $i(t)$ and $q(t)$ are signals of the I/Q path, respectively, CG_{RF} is the conversion gain of the RF front-end, and A_{Mixer} is the signal amplitude at the mixer output. Therefore, in the frequency domain, the data "0" and "1" are centered at $-\Delta f$ and $+\Delta f$, respectively. In the time domain, the frequencies of both I/Q signals are Δf, and the phase of I lags and leads that of Q by 90° for a data of "0" and "1", respectively. In the baseband, two identical hybrid poly-phase filters with opposite I/Q input sequences (Hybrid PPF1 and Hybrid PPF0) accomplish frequency-to-energy conversion by passing $+\Delta f$ $(-\Delta f)$ and stopping $-\Delta f$ $(+\Delta f)$, respectively. The spectrum and waveforms of PPF inputs and outputs are shown in Fig. 3.2(b) and 3.2(c), illustrating the frequency-to-energy conversion. The discriminated signals are then amplified by programmable gain amplifiers (PGAs) and rectified by a squaring full-wave rectifier. The squared amplitude of the signal is proportional to the signal energy and is used for the data detection. This reduces circuit complexity and power consumption without loss of sensitivity as well as FOT compared with the conventional intergrate-and-dump energy detection [53]. The oversampled data stream is generated by a latched comparator, and time integration over

a bit period is performed off-chip to retrieve the original data.

There are three reasons for low power consumption in this new architecutre. First, the automatic frequency correction circuit is eliminated and the LO frequency accuracy requirement is relaxed. Therefore, the proposed receiver can work with a significantly relaxed LO source. There is no need for an accurate LO with extensive calibration [17] or expensive crystal oscillator with electrical compensation. This structure also relaxes the frequency accuracy requirements of the BFSK transmitter which improves the energy efficiency of the radio link. As an example, a BFSK modulator based on an open-loop phase-locked loop [54], where the frequency drift is within the tolerance range, can be utilized instead of a more power hungry closed-loop phase-locked loop. Second, frequency-to-energy conversion, channel selection, and interference rejection are achieved simultaneously within the PPFs. This reduces the power and hardware cost in the baseband. Third, the new hybrid topology for PPFs achieves an improved ACR with a lower order active PPF as shown in Section 3.3.

The receiver is optimized for a data rate of 1 Mb/s, and the center frequency and bandwidth of the PPFs are reconfigurable to accommodate a variable MI between 1 and 2. The frequency plan is shown in Fig. 3.3. With a MI of 2 (shown in Fig. 3.3(a)), the signal bandwidth for one channel is 4 MHz. With a 1 MHz guard band, the channel spacing is 5 MHz, which means the 2.4 GHz ISM bands can accommodate 16 co-existing channels. When MI = 1 is chosen (shown in Fig. 3.3(b)), the channel bandwidth is 3 MHz and the channel spacing is 4 MHz, allowing for 20 co-existing channels.

DC offset and flicker noise problems in this zero-IF receiver can be solved by high pass filtering since negligible baseband signal power is around DC with MI between 1

$\Delta f_{\text{channel}} = 5\text{MHz}$

f_{c1} f_{c2} f_{c16}

0   1

$f_{c1}–1\text{MHz}$ $f_{c1}+1\text{MHz}$

2.4 GHz ISM band , 16 channels

(a)

$\Delta f_{\text{channel}} = 4\text{MHz}$

f_{c1} f_{c2} f_{c20}

0   1

$f_{c1}–0.5\text{MHz}$ $f_{c1}+0.5\text{MHz}$

2.4 GHz ISM band , 20 channels

(b)
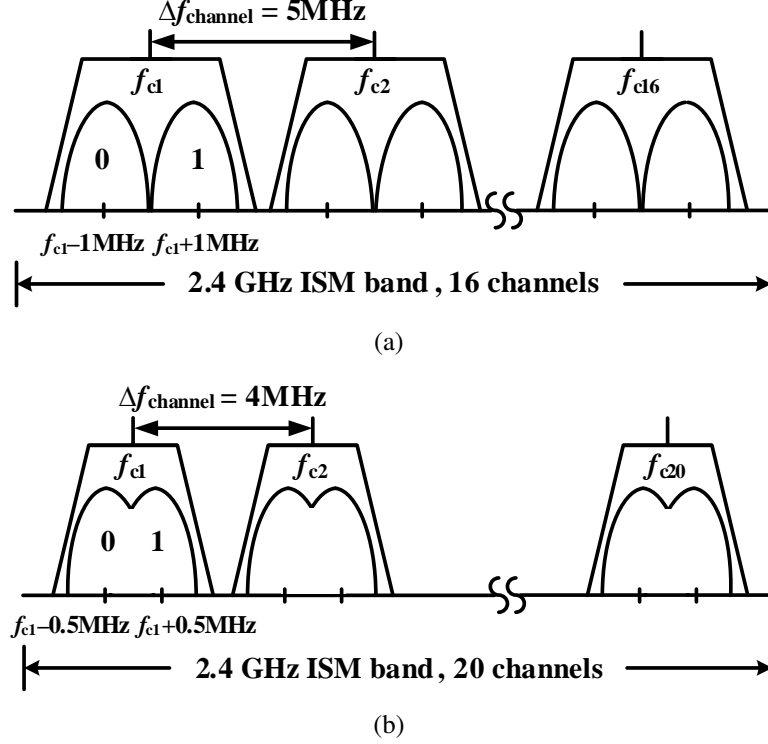
Figure 3.3: Proposed frequency plan in the 2.4 GHz ISM band. (a) MI = 2. (b) MI = 1.

and 2. System simulations show that a first-order high pass filter with a corner frequency of approximately 30 kHz degrades the system sensitivity by less than 0.5 dB. The high pass filtering is distributed along the baseband chain, one before the hybrid PPF to eliminate the DC offset caused by LO self-mixing, and the others within the PGA to prevent signal saturation due to the DC offset. The settling time corresponding to this high pass filtering is 18 μs for a settling error of 0.01%, and it is negligible compared with that of the local oscillators. Hence, it is not a concern for a receiver with a medium data rate of about 1 Mb/s.

3.3   Frequency Offset Tolerance Analysis and Optimization

3.3.1   Frequency Offset Tolerance of the PPF-Based Receiver

When a frequency offset, f_{off}, exists between the transmitter and receiver LOs, the spectrum of the complex signal described in (3.2) is shifted by the amount of this offset. That is

$$
\begin{aligned}
X(t)' &= i(t)' + jq(t)' = r(t) \cdot CG_{RF} e^{-j2\pi(f_c + f_{off})t} \\
&= \begin{cases} A_{Mixer} e^{j[-2\pi(\Delta f + f_{off})t + \varphi]} & \text{data is 0} \\ A_{Mixer} e^{j[+2\pi(\Delta f - f_{off})t + \varphi]} & \text{data is 1} \end{cases} \quad 0 \quad t \quad T \quad (3.3)
\end{aligned}
$$

The frequency-to-energy conversion with frequency offset is illustrated in Fig. 3.4. When a "1" is transmitted, as shown in Fig. 3.4(a), the I/Q frequency is $+(\Delta f - f_{off})$. The signal energy passing through PPF1, E_{Pass}, decreases with increased f_{off}, while the signal energy leaking through PPF0, $E_{Leak,10}$, increases with increased f_{off}. When a "0" is transmitted, as shown in Fig. 3.4(b), the I/Q frequency is $-(\Delta f + f_{off})$. The signal energy passing through PPF0, E_{Pass}, and the signal energy leaking through PPF1, $E_{Leak,01}$, decrease with increased f_{off}. The energies used for data decision are $E_{Dec1} = E_{Pass} - E_{Leak,10}$ and $E_{Dec0} = E_{Pass} - E_{Leak,01}$ for a transmitted "1" and "0", respectively. Therefore, a reduction of E_{Pass} and an increase in $E_{Leak,10}$ and $E_{Leak,01}$ degrade the sensitivity of the receiver as they lower the signal-to-noise ratio for detection.

From Parseval's theorem, the total energy of a signal $x(t)$ is equal to the total energy of the signal's Fourier transform $\mathcal{F}(x(t))$. Therefore the total energy of $X(t)$ is related
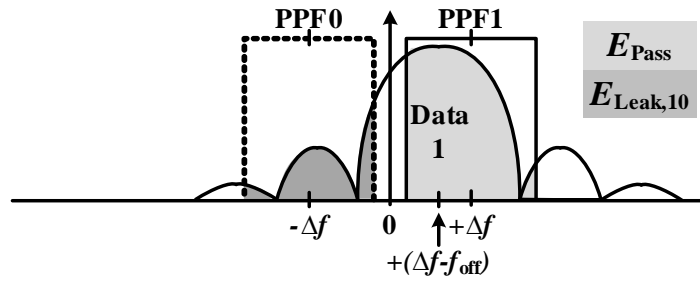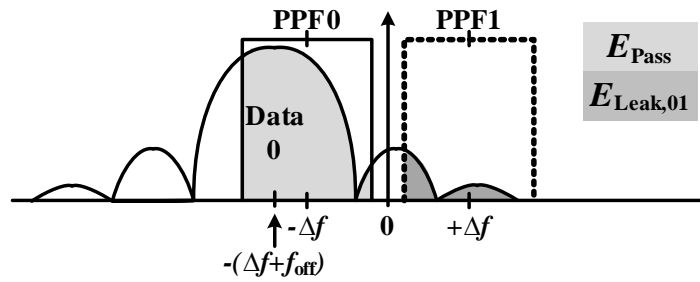
Figure 3.4: Frequency-to-energy conversion with frequency offset. (a) When a "1" is transmitted. (b) When a "0" is transmitted.

to its energy spectral density $\psi(f)$ as follows

$$E_{X(t)} = \int_{-\infty}^{+\infty} |X(t)|^2 \, dt = \int_{-\infty}^{+\infty} |\mathcal{F}(X(t))|^2 \, df = \int_{-\infty}^{+\infty} \psi(f) \, df. \qquad (3.4)$$

Here, the energy spectral density $\psi(f)$ is given by

$$\begin{aligned} \psi(f) &= |\mathcal{F}(X(t))|^2 \\ &= |A_{Mixer}Te^{j\varphi}e^{-j\pi(f-\Delta f)T} sinc(f-\Delta f)T|^2 \qquad (3.5) \\ &= (A_{Mixer}T)^2 sinc^2(f-\Delta f)T \end{aligned}$$

where data = 1 and $f_{off} = 0$ are assumed without loss of generality [55]. The energy

spectral density is plotted in Fig. 3.5(a), where 78% and 90% of the signal energy is con-

(a)

(b)
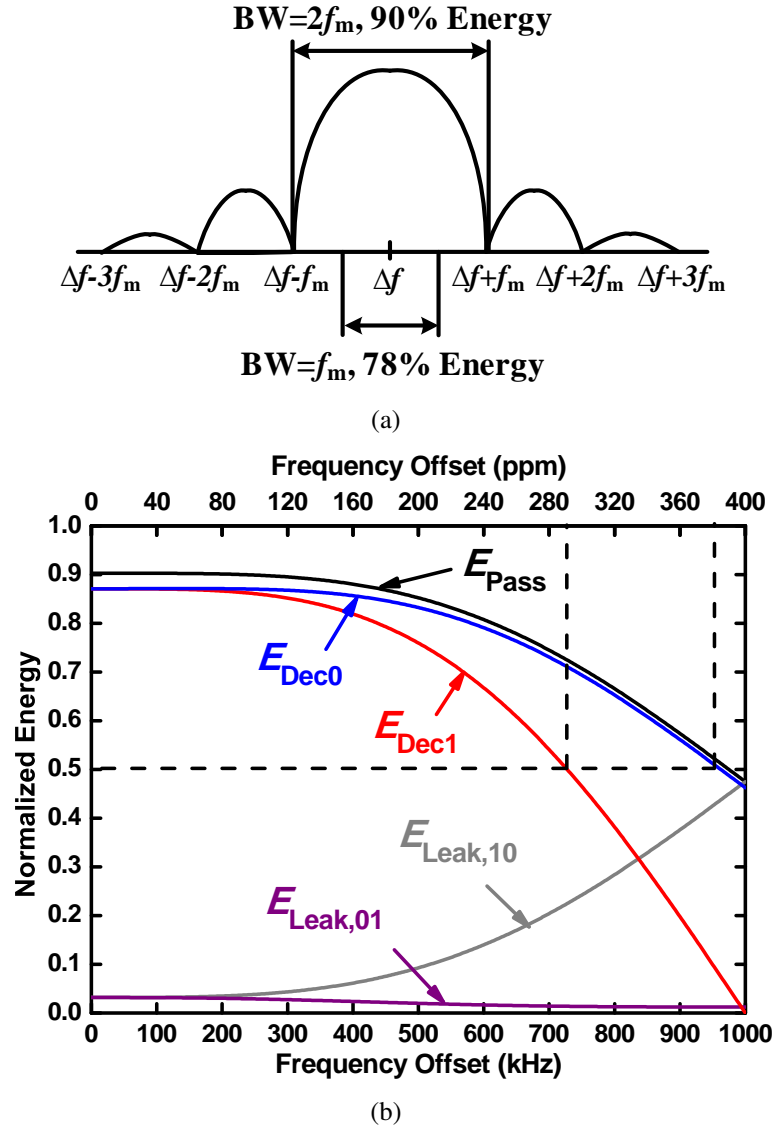
Figure 3.5: (a) Energy spectral density of the rectangular pulsed signal $X(t)$, assuming data = 1 and $f_{off} = 0$. (b) Normalized values of E_{Pass}, $E_{Leak,10}$, $E_{Leak,01}$, E_{Dec1} and E_{Dec0} through an ideal PPF with a bandwidth of $2f_m$.

centrated within a bandwidth of f_m and $2f_m$ around the center frequency, respectively. This characteristic results in a small sensitivity of the energy loss due to the frequency offset and, therefore, a good frequency offset tolerance as described below.

Assuming an ideal brick-wall PPF and an infinite integration time, E_{Pass}, $E_{Leak,10}$, and $E_{Leak,01}$, shown in Fig. 3.4, can be calculated from (3.4) using an integration window defined by the passband of PPF:

$$E_{Pass} = \int_{\Delta f - f_{BW}/2}^{\Delta f + f_{BW}/2} (A_{Mixer}T)^2 sinc^2(f - (\Delta f - f_{off}))T \, df. \tag{3.6}$$

$$E_{Leak,10} = \int_{-\Delta f - f_{BW}/2}^{-\Delta f + f_{BW}/2} (A_{Mixer}T)^2 sinc^2(f - (\Delta f - f_{off}))T \, df. \tag{3.7}$$

$$E_{Leak,01} = \int_{\Delta f - f_{BW}/2}^{\Delta f + f_{BW}/2} (A_{Mixer}T)^2 sinc^2(f + (\Delta f + f_{off}))T \, df. \tag{3.8}$$

where data = 1 is assumed without loss of generality, and f_{BW} is the passband width of the ideal PPF. The resultant energy used for decision, E_{Dec1} and E_{Dec0}, can then be obtained. Figure. 3.5(b) shows E_{Pass}, $E_{Leak,10}$, $E_{Leak,01}$, E_{Dec1} and E_{Dec0} normalized to the signal energy, for an ideal PPF with a bandwidth of $2f_m$ and a MI of 2. As most of the energy is confinced around the center frequency, the nomalized values of E_{Dec1} and E_{Dec0} remain large with increased f_{off}, demonstrating a FOT greater than 290 ppm for a 3-dB degradation in the sensitivity in this ideal case. The sensitivity with real PPFs is dependent on the filter bandwidth, the finite transition bandwidth and intersymbol interference. These can be modeled and simulated at the system level to determine the optimal PPF bandwidth and order for the maximum FOT.

3.3.2 Optimization of PPF for Maximum Frequency Offset Tolerance

The most important system parameters that determine the frequency offset tolerance are the bandwidth and order of the PPFs. Recall that the energy used for data decision is $E_{Dec1(0)} = E_{Pass} - E_{Leak,10(01)}$ for a transmitted "1" ("0"). Referring to Fig. 3.4, with a fixed order of the PPF, both E_{Pass} and $E_{Leak10(01)}$ increase when the bandwidth of the PPF increases. The trend of $E_{Dec1(0)} = E_{Pass} - E_{Leak,10(01)}$ depends on which one of E_{Pass} and $E_{Leak,10(01)}$ increases at a faster rate. When the bandwidth is very small, E_{Pass} increases at a faster rate than $E_{Leak,10(01)}$ with increased bandwidth. Therefore the sensitivity and FOT also increase. When the bandwidth is very large, E_{Pass} already contains most of the signal energy and doesn't change considerably with increased bandwidth. On the other hand, $E_{Leak,10(01)}$ increases at a much faster rate. Therefore, the sensitivity and FOT start to degrade with increased bandwidth, indicating that an optimal bandwidth exists for a PPF with a specific order. This is verified through system level simulations.

In the system level simulation, the complete PPF-based receiver is modeled in Agilent Advanced Design System (ADS), along with a continuous-phase BFSK modulator and additive white Gaussian noise (AWGN) channel. A pseudo random rectangular data stream is used to run bit error rate (BER) simulations and the sensitivity is determined for a 0.1% BER. The PPFs are Butterworth filters configured with different bandwidths and orders. FOT, which is defined as the frequency offset with a 3dB degradation in sensitivity, is adopted as the performance metric. The simulated FOT variations with PPF bandwidth for several orders of the PPF are shown in Fig. 3.6. Without considering channel filtering and interference rejection requirements, there exists an optimal band-
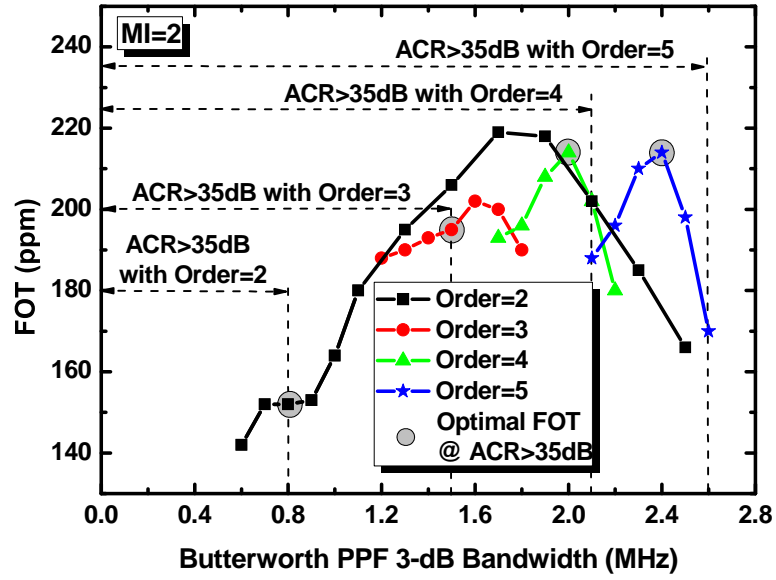
(a)
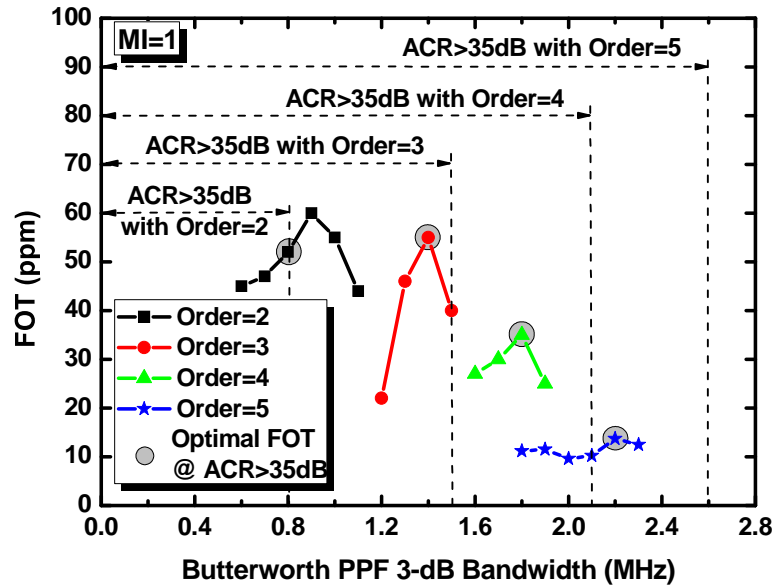
(b)

Figure 3.6: Optimal 3-dB bandwidth for Butterworth PPFs with different orders, with the constraint of ACR > 35 dB. (a) MI = 2. (b) MI = 1.

width with the maximum FOT for each order. Furthermore, as shown in Fig. 3.6(a), the optimized FOTs with a MI of 2 remain similar for several filter orders. The variation is less than 10% (within 200∼220 ppm). On the other hand, when MI decreases to 1, the optimized FOT degrades considerably with increased order as shown in Fig. 3.6(b). When MI decreases, the sensitivity and FOT are more sensitive to the filter-introduced ISI which increases with the filter order.

With an ACR greater than 35 dB, the optimal FOT for each order is highlighted by circles in Fig. 3.6. A bandwidth of 1.4 MHz with an order of 3 is chosen for both MIs. These are the optimized values for a MI of 1, and the same filter can be reused for a MI of 2 without a degradation of the FOT. With a MI of 2, further increase of the order results in only 10% improvement in FOT at the expense of more than 30% extra power consumption.

3.3.3   Comparison with Conventional BFSK Receivers

To demonstrate the improved FOT with the proposed PPF-based receiver, the two other conventional BFSK receivers (as shown in Fig. 3.1(a)) are also modeled and simulated. One uses a DFF-based demodulator similar to [45], and the other uses a CDM-based demodulator similar to [47]. Again, all the filters in the receivers are Butterworth filters with an ACR greater than 35 dB. The PPF bandwidth and order in the PPF-based receiver are optimized as discussed in Section 3.3.2. For the DFF and CDM based receivers the low pass filter (LPF) bandwidth and order are also optimized for sensitivity and FOT. The simulated sensitivity with frequency offset is shown and compared in

Fig. 3.7. When MI = 2, the FOT for the DFF-based receiver degrades dramatically, and it is unable to work for a frequency offset greater than 50 ppm. Compared with the CDM-based receiver, the PPF-based receiver has 2 dB better sensitivity around zero frequency offset and also behaves much better beyond a frequency offset of 200 ppm. This performance advantage of the PPF-based receiver is even more remarkable when MI decreases to 1. The DFF-based receiver no longer works and the CDM-based receiver degrades dramatically beyond 50 ppm.

The reason for an inferior FOT in DFF/CDM based receivers is that they use zero-crossings (phase) of the signal for data detection, which is much more sensitive to the frequency offset at low MIs. With frequency offset, the frequency of the I/Q signals, $+(\Delta f - f_{off})$, is reduced, and fewer zero-crossings can occur within one bit period. When MI decreases below 2, $+(\Delta f - f_{off})$ is smaller than the baseband modulating frequency f_m. In this case, no or erroneous zero-crossings may occur in one bit period due to the noise and filter-introduced ISI, whereby the data being received is lost.

3.3.4   Hybrid PPF Topology

From the system simulations in Section 3.3.2, a Butterworth PPF with a bandwidth of 1.4 MHz and an order of 3 gives optimal sensitivity and FOT with a MI of 1 and 2. Furthermore, a hybrid topology is proposed for the PPFs which achieves an improved ACR at reduced power consumption. The block diagram of the hybrid PPF is shown in Fig. 3.8(a). It consists of an active PPF based on second-order Chebyshev LPFs, and two passive RC PPFs with nulls at $\pm f_{AC}$, the center frequency of the adjacent channel
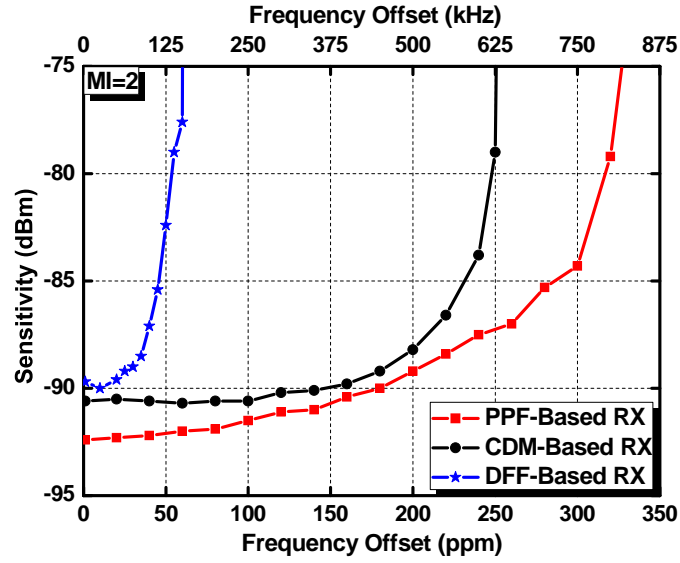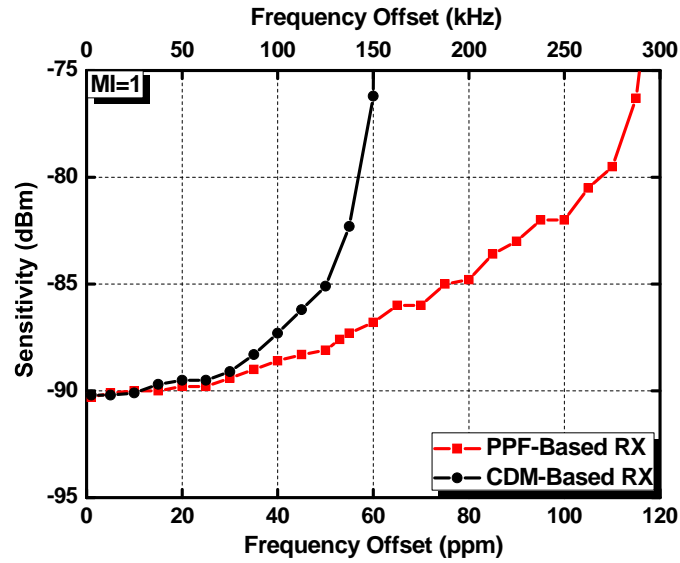
Figure 3.7: Comparison of frequency offset tolerance with conventional BFSK receivers. (a) MI = 2. For PPF-based RX, optimal PPF bandwidth = 1.4 MHz, order = 3. For CDM/DFF based RX, optimal LPF bandwidth = 2.05 MHz, order = 6. (b) MI = 1. For PPF-based RX, optimal PPF bandwidth = 1.4 MHz, order = 3. For CDM-based RX, optimal LPF bandwidth = 1.55 MHz, order = 5.
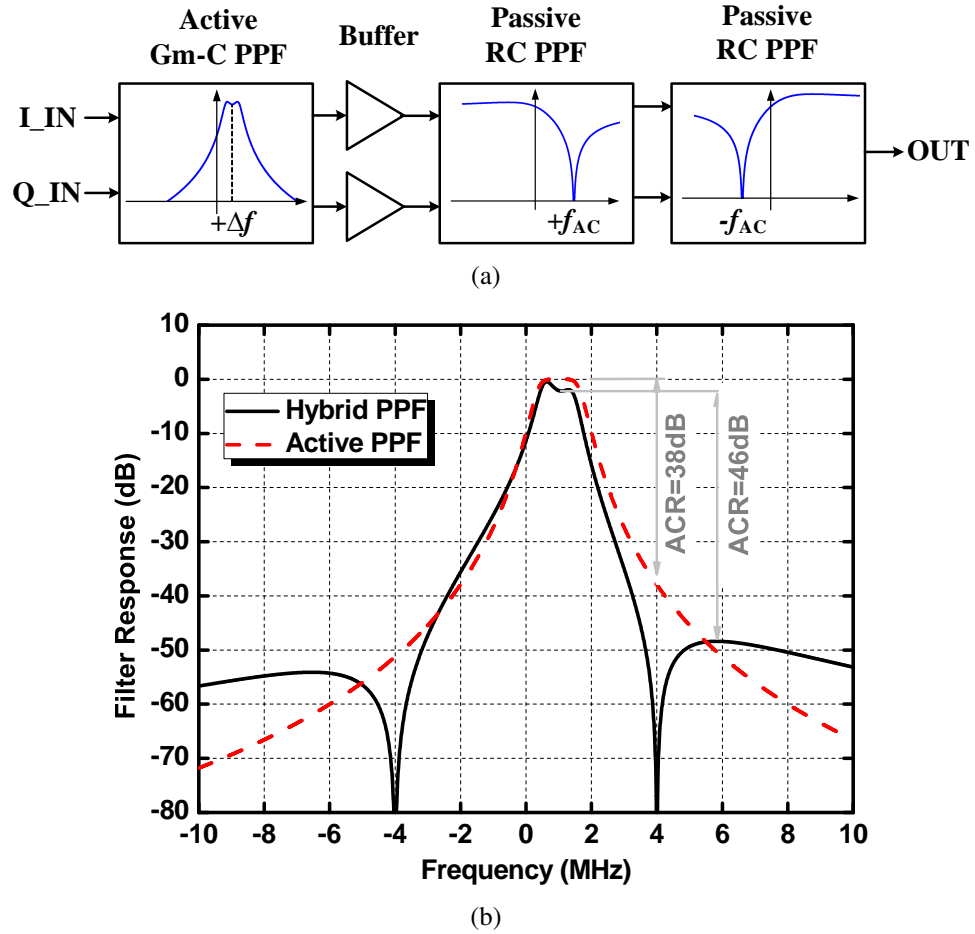
Figure 3.8: Hybrid PPF. (a) Block diagram. (b) Frequency response compared with an active PPF with 8 dB improvement in ACR.

signal (f_{AC} = 4 MHz and f_{AC} = 3.5 MHz for a MI of 2 and 1, respectively, referring to Fig. 3.3). The system level simulations yield an optimal 1-dB bandwidth for the active Chebyshev filter as 1 MHz and 0.9 MHz for MI = 2 and MI = 1, respectively.

The hybrid topology has two advantages over an active one. First, power is reduced by using an active filter of a lower order. One reason is that the active PPF requires less out-of-band attenuation because extra attenuation is provided by the RC PPFs. The

other reason is that a Chebyshev implementation is feasible because the PPF-based energy detection is less sensitive to phase distortion compared with the conventional zero-crossing based detection. The Chebyshev implementation requires a lower order and, therefore, a lower power consumption for the same amount of stopband attenuation. The noise penalty from the passive PPFs is mitigated by the high gain in the RF front-end. Second, as shown in Fig. 3.8(b), due to the nulls placed at the center frequency of the adjacent channels, the hybrid PPF achieves 46dB ACR, an improvement of 8 dB over the active Butterworth PPF.

Component mismatches affect the transfer function of the filter and, therefore, the ACR. By choosing a Gm-C implementation for the active PPF to save power consumption, the sources of mismatch include the transconductance (Gm) mismatch between the Gm cells, and R and C mismatches. Monte Carlo simulations have been performed to show the effect of mismatch on the hybrid PPF and the results are shown in Fig. 3.9. The worst case ACR is 43 dB and 40 dB, respectively, for 2% and 5% mismatch in Gm, R and C. Layout techniques were utilized to improve the component matching. The measured ACR of 46 dB verifies the excellent matching achieved after fabrication.

3.3.5   I/Q Mismatch

Due to the gain and phase mismatch in I/Q LOs and mixers, the signal at $+\Delta f$ passes through PPF1 as a desired signal, and leaks through PPF0 as an image signal (A transmitted data "1" is assumed without loss of generality.) Therefore, the ratio of the signal power at the PPF outputs due to I/Q mismatch, $(P_{y1(t)}/P_{y0(t)})|_{I/Q}$, equals the image re-
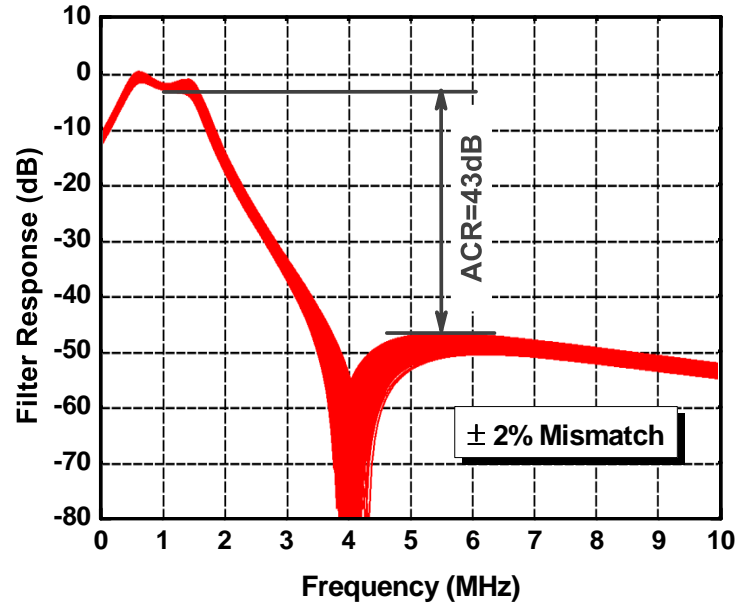
(a)
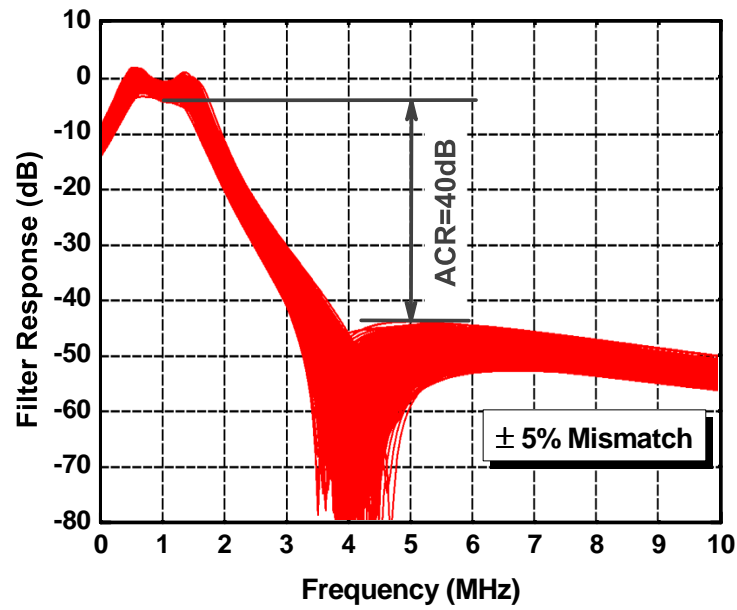
(b)

Figure 3.9: Monte Carlo simulations of the hybrid PPF frequency response. (a) With ±2% mismatch. (b) With ±5% mismatch.

jection ratio (IRR) which can be shown to be [56]

$$IRR = \frac{1 + 2\alpha\cos\theta + \alpha^2}{1 - 2\alpha\cos\theta + \alpha^2} \tag{3.9}$$

where the I/Q mismatch is equivalent to the LO gain (α) and phase (θ) mismatch, i.e., quadrature LOs of $A_{LO}\cos(2\pi f_c)$ and $-\alpha A_{LO}\sin(2\pi f_c + \theta)$. Figure 3.10(a) shows $(P_{y1(t)}/P_{y0(t)})|_{I/Q}$ with different gain and phase mismatches. Fig. 3.10(b) shows the gain response of the hybrid filter used in this work. It shows that the ratio of the signal power at the PPF output due to the filter's finite stopband attenuation, $(P_{y1(t)}/P_{y0(t)})|_{PPF}$, is 23 dB. To make the contribution from I/Q mismatch negligible compared with that from the PPF, $(P_{y1(t)}/P_{y0(t)})|_{I/Q} = (P_{y1(t)}/P_{y0(t)})|_{PPF} + 10dB$ is assumed whereby an IRR of 33 dB is required. This translates into an α of 0.3 dB and a θ of 2°, and can be achieved with typical matching in integrated circuits [56].

3.4   Circuit Implementation

3.4.1   RF Front-End

3.4.1.1   Low Noise Amplifier

A high gain is preferred in the RF front-end to suppress the noise from the baseband. The current-reuse [28] two-stage LNA (Fig. 3.11, biasing circuits not shown) consists of an inductor-degenerated input stage and a common-source PMOS amplifier that shares
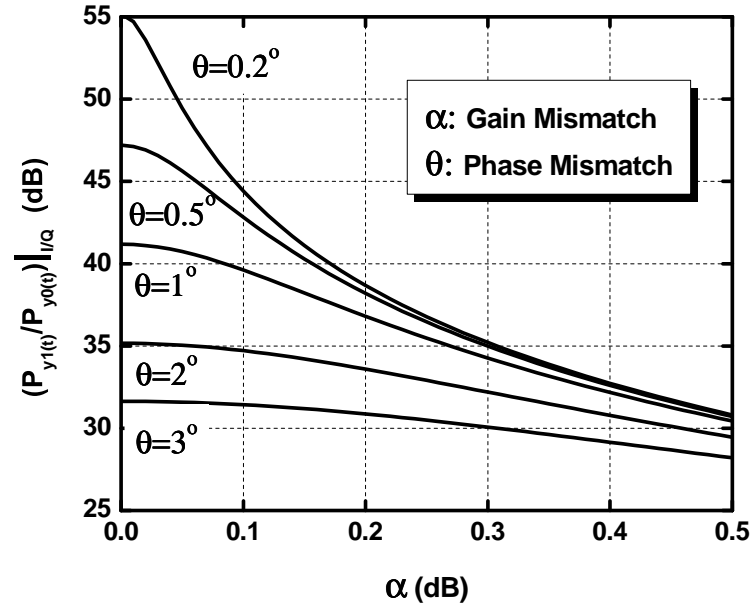
(a)
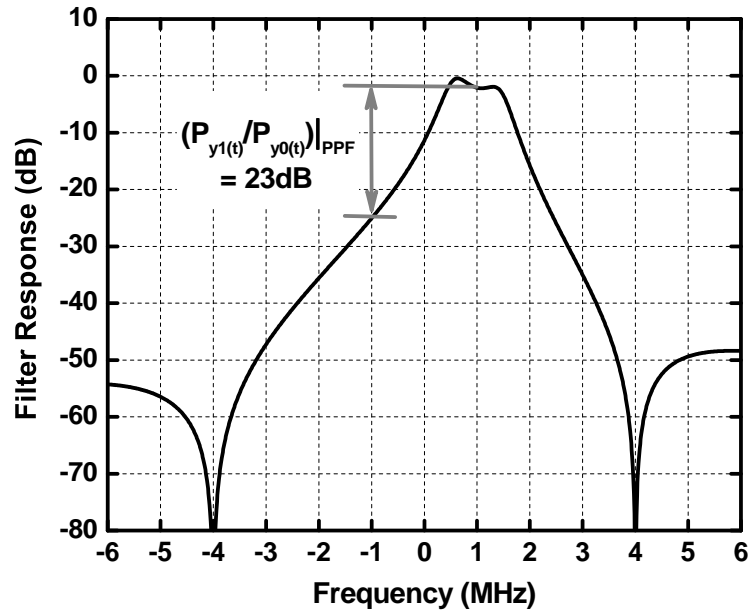
(b)

Figure 3.10: (a) $(P_{y1(t)}/P_{y2(t)})|_{I/Q}$ with I/Q gain (α) and phase (θ) mismatch. (b) $(P_{y1(t)}/P_{y2(t)})|_{PPF}$ of the hybrid PPF.
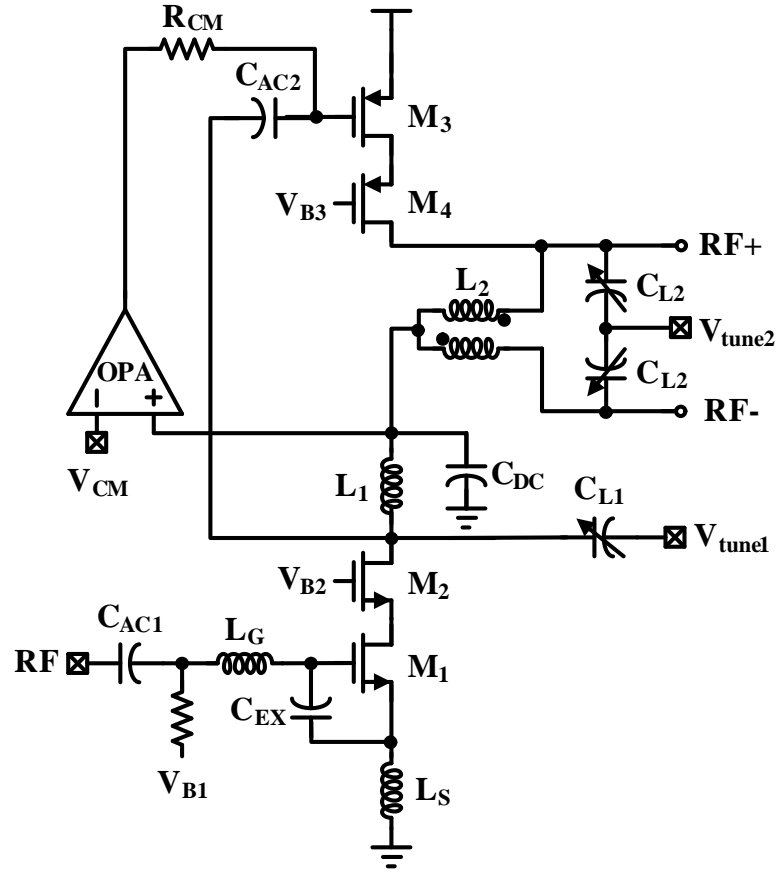
Figure 3.11: Schematic of the two-stage current-reuse LNA.

the DC current with the first stage. A single-ended input to differential output is accomplished through a symmetrical inductor (L_2) with a center tap acting as a transformer. This conversion not only eliminates the external balun at the LNA input, which reduces gain and degrades noise figure (NF), but also saves power by a factor of two compared with the differential structure. Separate power supplies with extensive on chip decoupling, along with good layout isolation between RF, analog and digital domains minimize the noise coupled to the LNA. A single-stage operational amplifier (OPA) is used

in the feedback loop to set the desired DC voltage, and C_{DC} provides an ac ground.

Inductive degeneration with an additional gate-source capacitance, C_{EX}, is adopted to achieve simultaneous noise and input matching at low power consumption [57]. The gate and source inductors, L_G and L_S, as well as the load inductors, L_1 and L_2, are integrated spiral inductors with stacked top metals. M_1 works in weak inversion for an optimized $g_m f_T / I_{DS}$, and cascode transistor M_2 is inserted to improve the reverse isolation. To accommodate process variations, varators implemented with N-MOSFETs in accumulation mode, C_{L1} and C_{L2}, are used to tune the LC tanks to the desired frequency.

3.4.1.2 Quadrature Down-Conversion Mixer

The quadrature down-conversion mixer, as shown in Fig. 3.12 (only one of the I/Q mixers is shown), is a double balanced CMOS exponential-law mixer with the RF signal input at the gate while the LO signal is applied at the source of a MOSFET operating within subthreshold region. This structure achieves a high gain at a low LO swing and low power consumption. We define the current efficiency of the conversion transconductance $\eta = CG_m / I_{DS} = i_{IF} / (v_{RF} \cdot I_{DS})$ as a measure of high-gain oriented low power design. Here, i_{IF} is the IF output current, v_{RF} is the RF input voltage, and I_{DS} is the DC bias current. Neglecting short-channel effects, the MOSFET in saturation and subthreshold region has an I_{DS} to V_{GS} relation and g_m / I_{DS} as shown in Table 3.1 [59]. Therefore, η of the CMOS Gilbert mixer [58], the CMOS square-law mixer [58] and CMOS exponential-law mixer presented here can be derived and these expressions
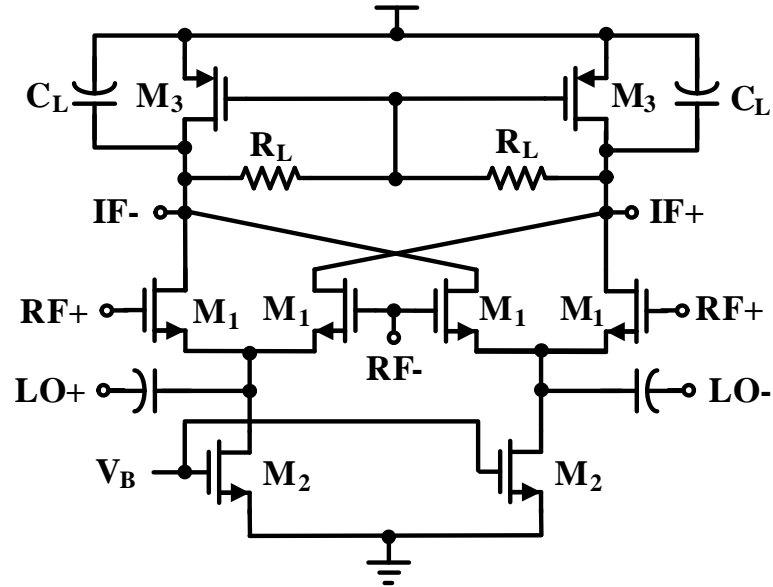
Figure 3.12: Schematic of the CMOS exponential-law down-conversion mixer.

are also shown in Table 3.1. The RF transconductor MOSFETs in CMOS Gilbert and CMOS square-law mixers operate in the saturation region, and hard switching of the LO switching pairs is assumed in the CMOS Gilbert mixer. As a typical MOSFET has a much larger g_m/I_{DS} in the subthreshold region, we can conclude that the CMOS exponential-law mixer requires a smaller biasing current and/or smaller LO swing to provide the same conversion gain, as shown in Table 3.1. Drawing a 200 μA current from a 1 V supply, the I/Q mixers achieve a 13 dB conversion gain with a -12 dBm 1-dB compression point at a peak amplitude for the LO as low as 40 mV. This eliminates the need for power hungry LO buffers.

Table 3.1: Current Efficiency of Conversion Transconductance for Different Mixers

	CMOS Gilbert Mixer [58]	CMOS Square-law Mixer [59]	CMOS Exponential -law Mixer
MOSFET Operation Region	Saturation		Subthreshold
I_{DS}	$\frac{1}{2}\mu C_{OX}\frac{W}{L}V_{OV}{}^2$		$\frac{W}{L}I_{DS0}\exp\left(\frac{V_{OV}}{nV_T}\right)$
$\frac{g_m}{I_{DS}}$	$\frac{2}{V_{OV}}$		$\frac{1}{nV_T}$
$\eta = \frac{i_{IF}}{v_{RF}I_{DS}}$	$\frac{g_m}{I_{DS}}\cdot\frac{2}{\pi}$	$\frac{g_m}{I_{DS}}\cdot\frac{v_{LO}}{2V_{OV}}$	$\frac{g_m}{I_{DS}}\cdot\frac{v_{LO}}{nV_T}$
$\eta@n = 1.5$ $V_T = 26\ mV$ $V_{OV} = 100\ mV$ $v_{LO} = 100\ mV$	12.7	10.0	**65.7**

1: μ is the carrier mobility in the channel, C_{OX} is the gate oxide capacitance per unit area, W is the channel width, L is the channel length, $V_{OV} = V_{GS} - V_{TH}$ is the overdrive voltage.

2: I_{DS0} is the drain current with $V_{GS} - V_{TH} = 0$ and $W/L = 1$. $n > 1$ is the non-ideality factor. $V_T = kT/q$ is the thermal voltage and $V_T = 26\ mV$ at $T = 300\ K$.

3: v_{LO} is the single-ended peak amplitude of the sinusoidal LO signal.

3.4.2 Analog Baseband

3.4.2.1 Hybrid Polyphase Filter

The block diagram of the hybrid PPF is shown in Fig. 3.8(a). The active PPF is implemented with two Chebyshev LPF prototypes cross-coupled to each other as shown in

Fig. 3.13(a) [60, 61]. A Gm-C realization is chosen for low power consumption. The transconductor cell (shown in Fig. 3.13(b)) is based on a linearized transconductor using varying bias-triode transistors [62], whose transconductance G_m can be tuned over process variations by changing the bias current. The input pairs M_0 and M_1 are implemented using NMOSFETs in a deep N-well to eliminate the body-effect introduced nonlinearity, and cascode transistors are added to increase the output impedance. A phase margin of 70° is guaranteed in the common-mode feedback (CMFB) loop.

The schematic of the two-stage RC PPF is shown in Fig. 3.14. R_2 is set equal to $2R_1$ to reduce the gain loss due to the loading effect. The capacitor banks employ 3 bits of digital control to calibrate the RC time constants, placing different nulls as the channel spacing is different with different MIs. The buffer is realized with a linearized input stage followed by a source follower output stage.

3.4.2.2 Programmable-Gain Amplifier

A five-stage PGA with feedforward DC-offset cancellation is designed to maintain a good dynamic range. As shown in Fig. 3.15, two kinds of PGAs, PGA1 with offset cancellation and PGA2 without offset cancellation, are interleaved to suppress the DC-offset. The RC low pass network in PGA1 extracts the DC voltage from the input, which is subtracted from the signal by an auxiliary differential pair in parallel [47]. It has no impact on the settling time because C_{LP} behaves as a floating common mode component when the circuit is powered on. A low corner frequency is achieved on-chip by use

(a)

(b)

Figure 3.13: (a) Block diagram of the Gm-C active PPF, with two second-order LPF prototypes cross-coupled to each other. (b) Schematic of the Gm cell.
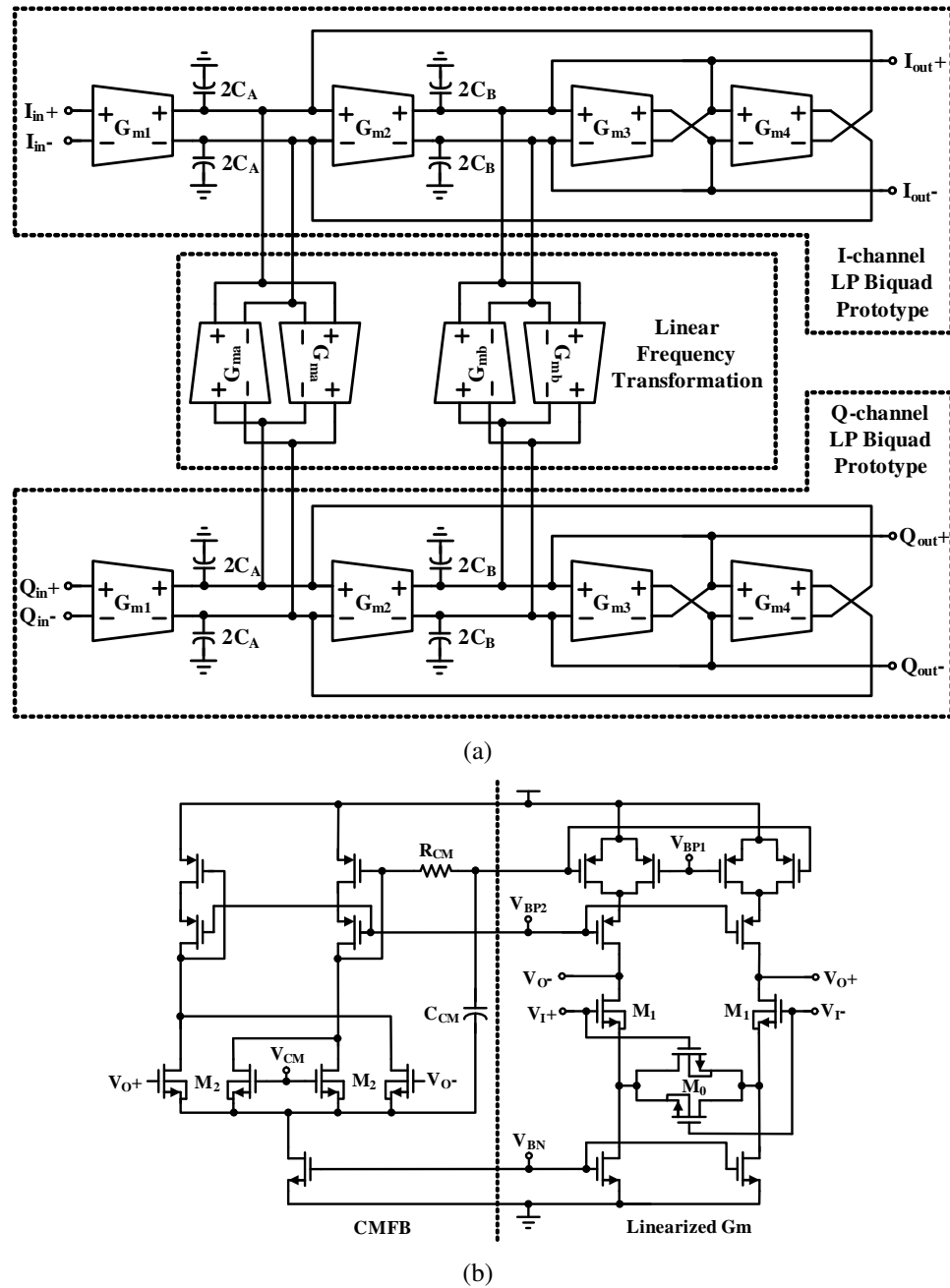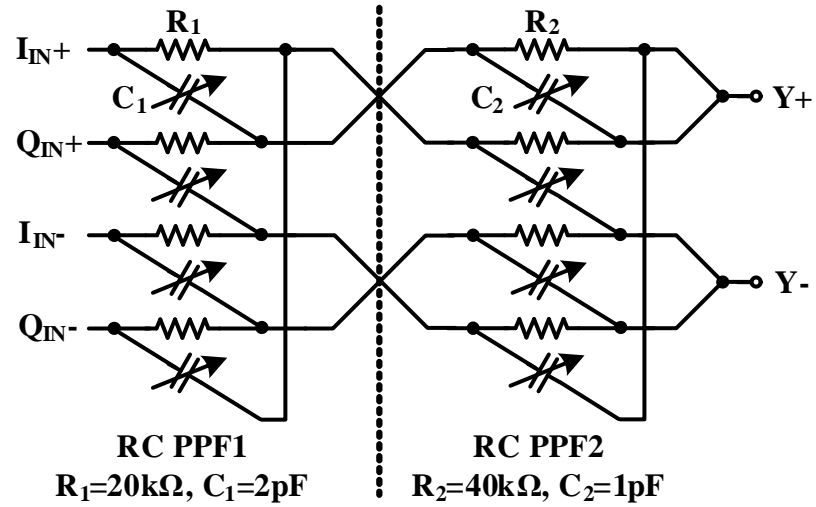
Figure 3.14: Schematic of the two stage RC PPFs.
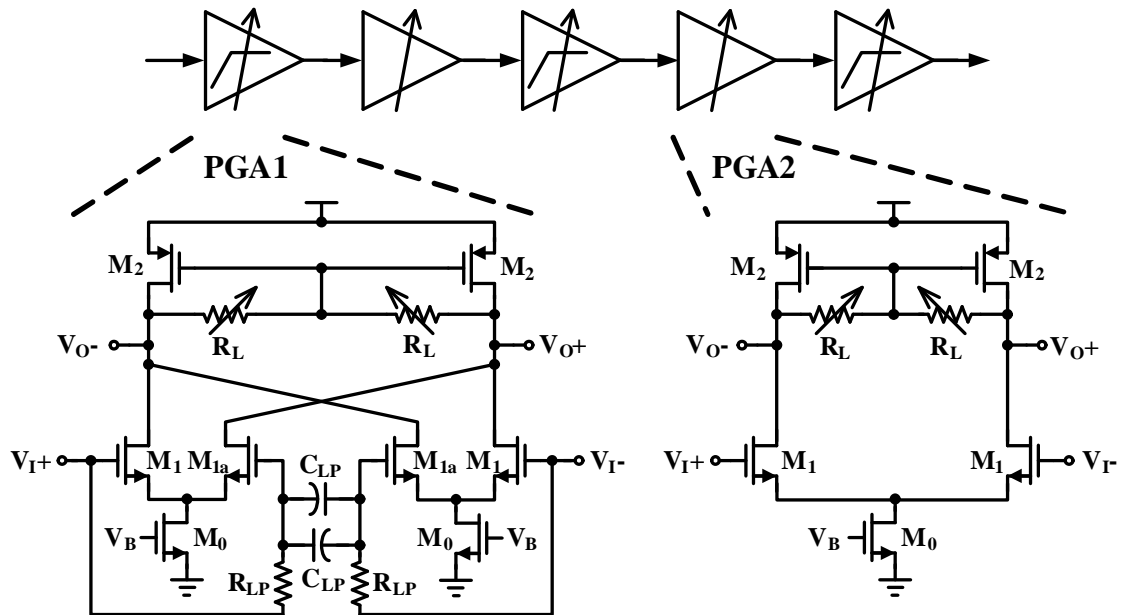
Figure 3.15: Five-stage PGA with feedforward offset cancellation.

of high-resistance poly resistors and high density dual-layer MIM capacitors. Gain is controlled by digital control of the load resistance, ranging from 10 dB to 50 dB with a 10 dB step. Local CMFB is used to maintain a fixed output common mode voltage over various gains.

3.4.2.3 Full-wave Rectifier and Latched Comparator

A CMOS rectifier consisting of unbalanced source-coupled pairs with a cross-coupled input stage and a parallel-connected output stage [63] is used, where differential signals are converted to a single-ended output with square-law full-wave rectification. This is followed by a latched comparator consisting of a two-stage preamplifier, a dynamic latch and a SR latch. In the preamplifier, the size of the input pair is made large to reduce the input-referred offset voltage, and a gain of 30dB is assigned to suppress the large offset from the latches.

3.5 Experimental Results

The receiver prototype has been fabricated in a 1P8M 0.13-μm CMOS process. The microphotograph of the chip is shown in Fig. 3.16, with all pins fully ESD protected. The chip was bonded in a standard QFN package and tested with a standard four-layer FR4 PCB board. For the purpose of testing, a three-stage RC PPF has also been designed on chip to generate the quadrature LO signals. All the measurements have been performed
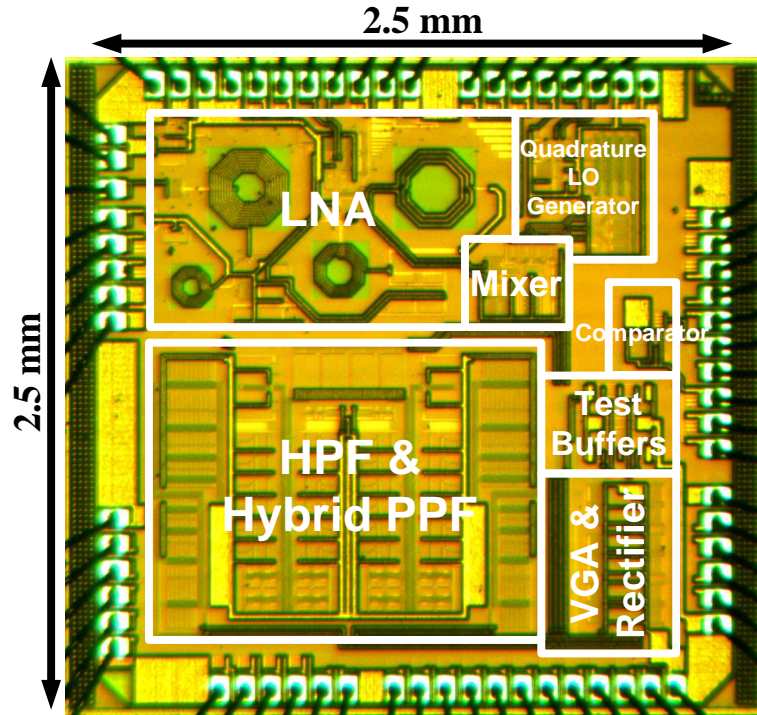
Figure 3.16: Chip microphotograph.

with a 1 V supply. With a data rate of 1 Mb/s, the receiver has been measured with two modulation indexes, MI = 1 and MI = 2, to demonstrate trade-offs in the system performance.

The LNA input matching is shown in Fig. 3.17(a). Within the 2.4 GHz ISM band, the measured S11 is better than -15 dB. Referring to Fig. 3.17(b), the RF front-end, including LNA and I/Q down-conversion mixers, achieves a conversion gain of 38.8 dB and a double-sideband (DSB) NF of 6 dB, with a power consumption of only 1.3 mW including all the biasing circuits.

The frequency response of the hybrid PPF along with the preceding high pass filter is shown in Fig. 3.18. With the nulls at ±4 MHz and ±3.5 MHz, the filter ACR is 46
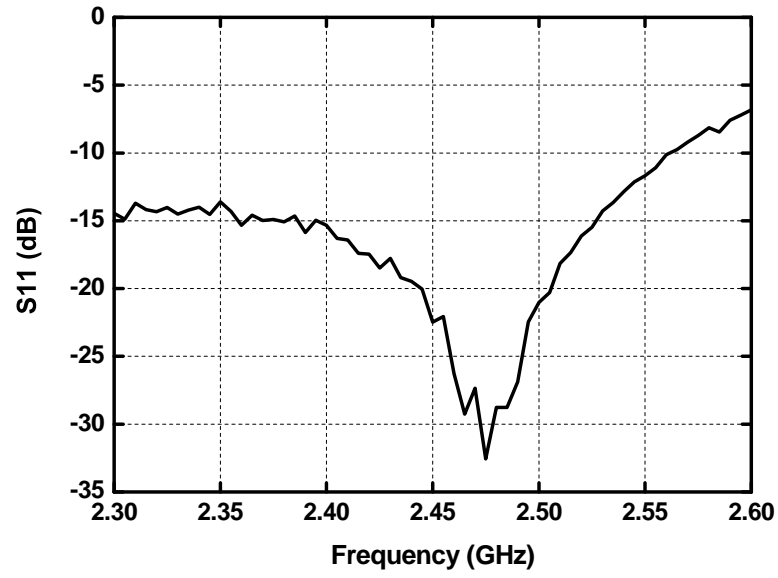
(a)
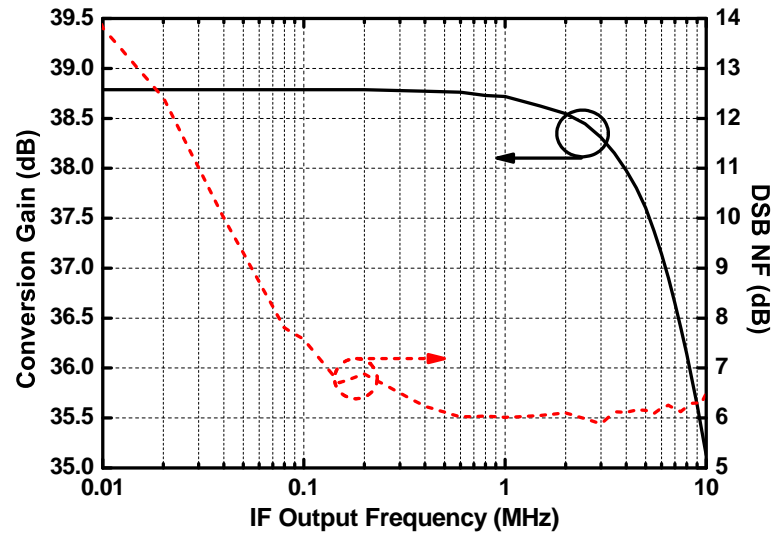
(b)

Figure 3.17: Measured performance of the RF front-end. (a) Input matching. (b) Conversion gain and noise figure.
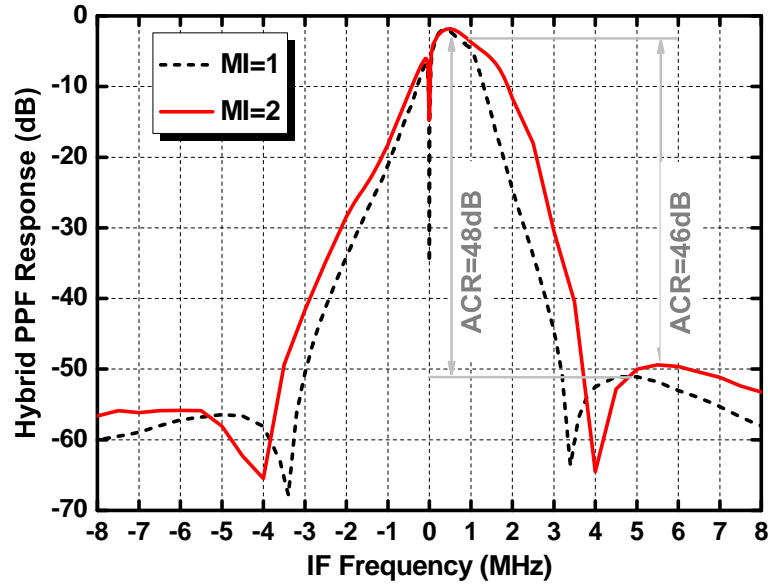
Figure 3.18: Measured frequency response of the hybrid PPF.

dB and 48 dB for MI = 2 and MI = 1, respectively, which agrees well with the simulated results shown in Fig. 3.8(b).

The sensitivity has been tested for a BER of 0.1%. A DC offset (approximately 20 mV) was observed between the two rectifier outputs in the measurement which degraded the BER. Additional DC offset cancellation at the output stage of the rectifier or in the comparator fixes this problem. For this prototype measurement, an off-the-shelf comparator is used. The sensitivity variation with frequency offset is tested for two MIs and is shown in Fig. 3.19. Allowing for a 3-dB degradation in the sensitivity, FOTs of ± 450 kHz (± 180 ppm for 2.4 GHz LOs) and ± 110 kHz (± 44 ppm for 2.4 GHz LOs) are achieved with MI = 2 and MI = 1, respectively. A trade-off between FOT and spectral efficiency can be made to accommodate different applications by choosing different MIs.
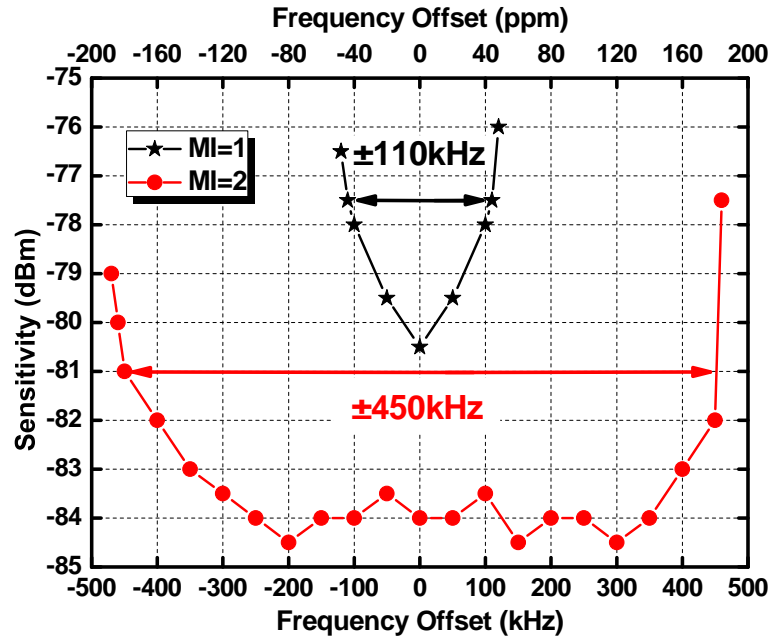
Figure 3.19: Measured sensitivity degradation with frequency offset.

Interference measurements demonstrate the receiver performance in the presence of large blocking signals. The input signal to the receiver is set at +3 dB above the sensitivity, and the blocker power is swept until the BER is degraded to 0.1%. The interference rejection is taken as the ratio of the blocker to signal power. Fig. 3.20 illustrates the out-of-band blocker rejection of the receivers configured for different MIs. The LO source used for measurement exhibits a flat phase noise of -125 dBc/Hz beyond a 2 MHz offset frequency. With the sharp transition at the signal bandedge, the adjacent channel rejection is better than 40 dB and 33 dB for MI = 2 and MI = 1, respectively. Further rejection at larger offset frequencies is limited by the nonlinearity of the RF front-end.

Table 3.2 summarizes the power consumption and measured performance of the re-
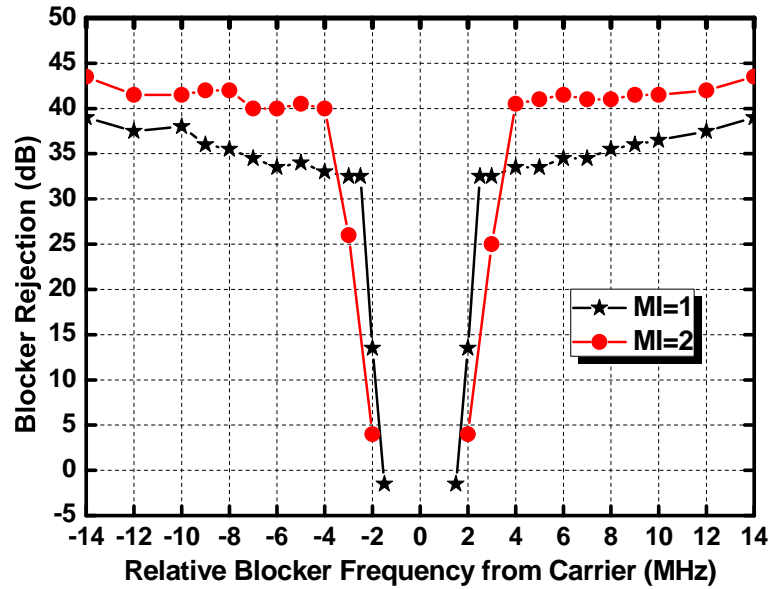
Figure 3.20: Measured out-of-band blocker rejection.

ceiver. Table 3.3 compares the performance with the state-of-the-art BFSK receivers for low data rate or medium data rate sensor network applications. With this new receiver architecture, high FOT and large ACR are achieved simultaneously due to the hybrid PPFs with excellent baseband efficiency. Furthermore, the energy FOM (as defined in Table 3.3) of this receiver is better than others except for [29], where the ACR is much lower compared with this work. The experimental results and comparison demonstrate that this new receiver architecture is a promising candidate for low-power medium data rate WSN applications.

Table 3.2: Measured Performance Summary

MI	2	1
Power Consumption @ 1 V Supply		
RF	1.3 mW	
Baseband	0.65 mW	0.52 mW
Total	1.95 mW	1.82 mW
Measured Performance		
RF Front-end	Frequency	2.4 GHz $\sim$ 2.5 GHz	
	S11	< -15 dB	
	Conversion Gain	38.8 dB	
	DSB Noise Figure	6 dB	
	1-dB Compression Point	-38 dBm	
	IIP3	-25 dBm	
Receiver	Data Rate	1 Mb/s	
	Maximum Gain	82 dB	
	IIP3	-27.5 dBm	-26 dBm
	ACR	40 dB	33 dB
	Sensitivity @ 0.1% BER	-84 dBm	-80.5 dBm
	FOT @ 3-dB Sensitivity Loss	$\pm$450 kHz ($\pm$180 ppm)	$\pm$110 kHz ($\pm$44 ppm)

3.6   Summary

A hybrid PPF based receiver is presented for medium data rate WSN applications, with a MI less than or equal to 2 to improve the spectral and energy efficiencies. The frequency offset tolerance of the PPF-based receiver is analyzed and optimized. Using frequency-to-energy conversion through PPFs, the new receiver achieves high FOT without any complex and power hungry frequency correction circuits. Excellent ACR is also attained at reduced power through the hybrid topology in the PPFs.

Table 3.3: Comparison of the State-of-the-Art BFSK Receivers for Sensor Applications

Reference	[24]	[30]	[29]	[31]	[31]	[32]	This Work	
Technology	0.5 μm	0.13 μm	0.13 μm	0.18 μm	0.18 μm	0.18 μm	0.13 μm	
Supply	1 V	1.2 V	1 V	1.8 V	1.8 V	1 V	1 V	
Architecture	Zero-IF	Zero-IF	Zero-IF	Low-IF	Zero-IF	Zero-IF	Zero-IF	
Frequency (f_{RF})	434 MHz	900 MHz	900 MHz	403 MHz	30~70 MHz	30~120 MHz	2.45 GHz	
Data Rate (DR)	24 kb/s	45 kb/s	50 kb/s	200 kb/s	2.5 Mb/s	10 Mb/s	1 Mb/s	
MI	8.3	8	2	-	1	1	**2**	**1**
Power (P_{RX})	1 mW	1.92 mW	2.5 mW	8.5 mW	5.7 mW	3.7 mW	3.45 mW[1]	3.32 mW[1]
Sensitivity (P_{SEN})	-95 dBm	-89 dBm	-102 dBm	-76 dBm	-65 dBm	-65 dBm	-84 dBm	-80.5 dBm
FOT	±34 kHz		±55 kHz[2]			-	±450 kHz	±110 kHz
Baseband Power (P_{BB})	0.135 mW	0.092 mW	0.42 mW	-	-	-	0.65 mW	0.52 mW
Baseband Energy[3]	5.63 nJ/b	2.04 nJ/b	8.4 nJ/b	-	-	-	**0.65 nJ/b**	**0.52 nJ/b**
ACR @ $2(\Delta f + f_m)$[4]	25 dB	-	9 dB	20 dB	32 dB	-	**40 dB**	**33 dB**
FOM_{FOT}[4]	-1.75	-	1.1[2]	-	-	-	**0.45**	**0.61**
FOM_{Energy}[5]	285.2 dB	282.2 dB	294.6 dB	265.8 dB	259.9 dB	270.1 dB	**292.4 dB**	**289.1 dB**

[1] Power of 1.5 mW is estimated for a 2.4 GHz frequency source.
[2] Automatic frequency correction is used to improve FOT.
[3] Baseband Energy=P_{BB}/DR.
[4] $FOM_{FOT} = [FOT - (\Delta f - f_m)]/f_m = FOT/f_m - (MI/2 - 1)$.
[5] $FOM_{Energy} = -10 \cdot \log_{10}[(P_{RX} \cdot P_{SEN})/(DR \cdot f_{RF})]$.

A 2.4 GHz prototype receiver, including RF and analog front-ends, is implemented for a data rate of 1 Mb/s, demonstrating measured FOTs of ±180 ppm and ±44 ppm, and measured ACRs of 40 dB and 33 dB for a MI of 2 and 1, respectively. The high FOT relaxes the frequency accuracy requirement of the LOs in transmitters and receivers, reducing the cost and power of the WSN links. The small MI combined with a large ACR improves the spectral efficiency and radio co-existence in the presence of interferers. A sensitivity of -84 dBm is achieved with a power consumption of only 1.97 mW. This makes it one of the most energy efficient receivers for low-power WSN applications.

Chapter 4: A 900 MHz Mixer-less BFSK Receiver with Q-enhanced Frequency-to-Amplitude Conversion

A new mixer-less low energy binary frequency shift keying (BFSK) receiver is presented for wireless sensor networks. High gain frequency-to-amplitude conversion is achieved with a linear amplifier with a Q-enhanced LC tank, eliminating the need for local oscillators and mixers. Sensitivity is improved due to the high center-frequency gain and conversion gain provided by the Q-enhancement. Furthermore, a higher data rate is enabled due to the linear amplification, leading to excellent energy efficiency. Fabricated in a 0.13-μm CMOS process and consuming 500 μW from a 0.7 V supply, the prototype chip achieves a sensitivity of -90 dBm and -76 dBm for data rates of 0.5 Mb/s and 6 Mb/s, respectively. The energy consumption is as low as 80 pJ/b when operating at 6 Mb/s.

4.1 Introduction

With the need for observing and monitoring data in the information age, wireless sensor networks (WSNs) provide a mechanism to easily communicate data in a wide variety of applications. They allow efficient and accurate data collection and communication. WSNs consist of a hub usually powered by a reliable power source and sensor nodes powered by a small battery or integrated energy harvester. As a result, the sensor node

requires a low power transceiver with a short start-up time to extend its useful life-time [7]. Furthermore, while the early WSNs required a data rate no larger than 100 kb/s, a data rate above 1 Mb/s is now necessary due to the increased complexity and data size of the WSN applications [42–44]. Although a lower data rate provides a better receiver sensitivity, a higher data rate leads to improved energy efficiency and reduced communication latency. Therefore, a scalable data rate from 100 kb/s to 10 Mb/s is preferred for various applications.

Due to a stringent power budget for the sensor nodes, on-off-keying (OOK) and binary frequency-shift-keying (BFSK) modulation schemes have been commonly used in WSNs for their simple and power efficient modulation and demodulation. In the transmitter, BFSK modulation is superior to OOK modulation for both data rate and linearity requirements. The maximum data rate of an OOK transmitter is limited by the turn-on/turn-off time of the power amplifier (PA) or oscillator. Also, the linearity specifications of the PAs are more strict for an amplitude-modulated signal. On the other hand, the constant envelope characteristic of a BFSK modulated signal makes it possible to achieve a higher data rate with a relaxed PA linearity requirement.

On the receiver side, OOK demodulation is power efficient due to its simple power-detection [11–14] or super-regenerative [15–18] architectures. As shown in Fig. 4.1(a) and Fig. 4.1(b), these architectures eliminate the need for power hungry local oscillators (LOs) and mixers, with only an RF amplifier or a super-regenerative oscillator operating at the radio frequency. BFSK demodulation normally requires a low-IF/zero-IF archi-tecture [24–27, 29, 30] as shown in Fig. 4.1(c). Significant power is consumed in the LO. The performance of recent OOK and BFSK receivers is summarized and compared
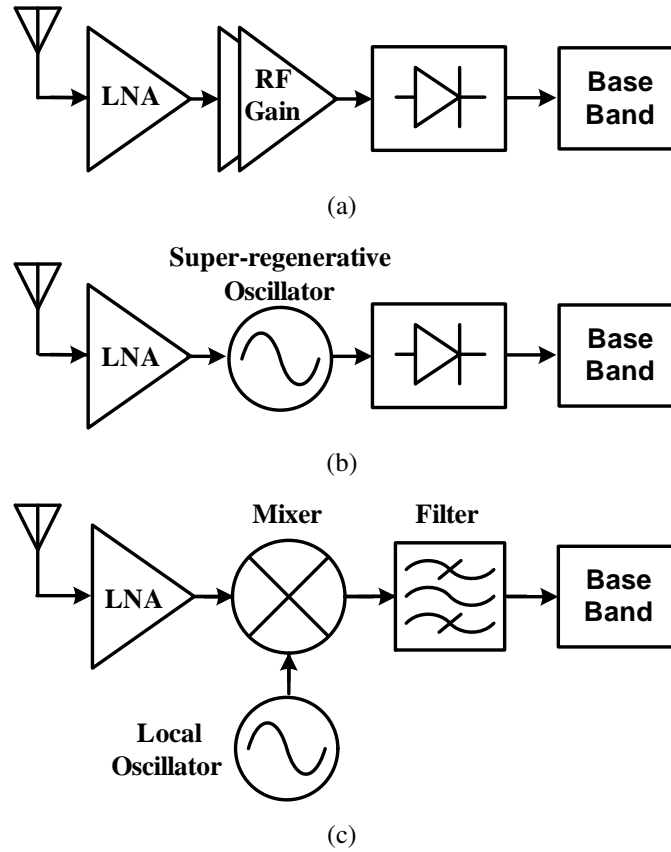
Figure 4.1: Conventional receiver architectures for wireless sensor networks. (a) OOK receiver with power-detection and (b) super-regenerative architectures. (c) BFSK receiver with low-IF/zero-IF architecture.

in Fig. 4.2. Most OOK receivers achieve a power consumption lower than 1 mW, while most of the BFSK receivers operate with a power consumption of several mWs.

To accommodate the energy efficient BFSK transmitters, mixer-less architectures which eliminate the frequency conversion and LO generation have been developed for ultra-low power BFSK receivers. References [19, 20] have demonstrated BFSK super-regenerative receivers. The resonant frequency of a super-regenerative oscillator is tuned to f_1, and the time-to-build oscillations is different for input signals with frequencies of
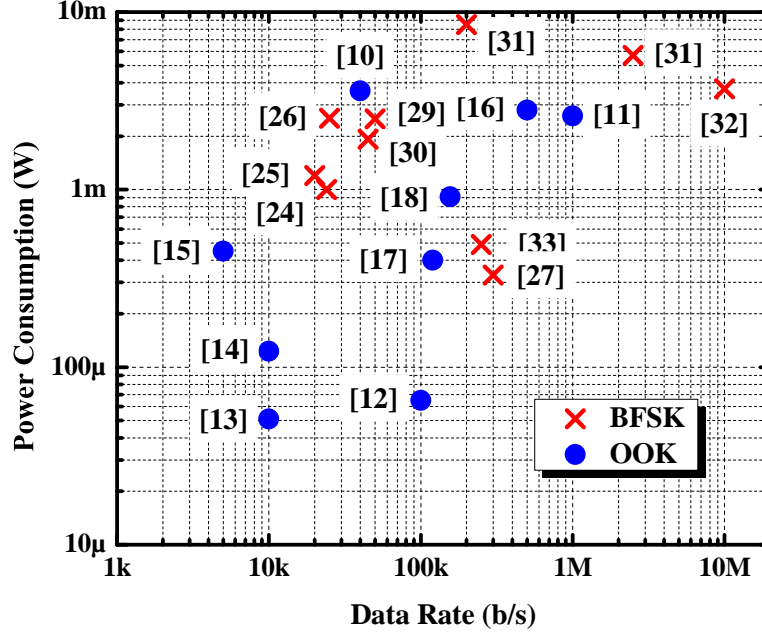
Figure 4.2: Comparison of data rate and power consumption for recent power-detection/super-regenerative OOK receivers and low-IF/zero-IF BFSK receivers.

f_1 and f_2. The difference in time-to-build oscillations is then converted to a voltage difference using energy detection. By eliminating an isolation low noise amplifier, the super-regenerative oscillator with a large non-linear gain is the only block that operates at radio frequencies, therefore, ultra-low power operation is demonstrated. However, a relatively large deviation frequency ($\Delta f = |f_1 - f_2|$) is required to maintain a reasonable sensitivity, leading to a large channel bandwidth of 16 MHz. Also, the maximum data rate is limited by the on-off time of the oscillation. In [22], an injection-locked frequency divider is utilized to convert the frequency modulated signal to an amplitude modulated signal by virtue of its bandpass transfer function in the locking range. A higher data rate is achieved due to the continuous operation of the oscillator. However,

the interference rejection is degraded because the injection-locked frequency divider is prone to injection-locking or pulling by blockers near the locking range.

This chapter presents a new mixer-less low energy BFSK receiver. A linear RF amplifier with a Q-enhanced LC tank is adopted to implement frequency-to-amplitude conversion. The receiver sensitivity is improved by virtue of the large center-frequency gain and conversion gain provided by the Q-enhancement. The required Δf is reduced due to the large conversion gain. A higher data rate is achieved due to the linear operation of the RF amplifier, leading to excellent energy efficiency. Interference rejection is also improved through the Q-enhanced bandpass filtering. Section 4.2 describes the system architecture and operation of the receiver. In Section 4.3, the principle of Q-enhancement is discussed and the design considerations and trade-offs with Q-enhancement are analyzed. Details of the circuit implementation are given in Section 4.4, followed by the experimental results in Section 4.5. Finally, Section 4.6 provides a summary of this work.

4.2 Receiver Architecture

The system architecture of the proposed receiver is shown in Fig. 4.3. The first stage is a tuned RF amplifier with a Q-enhanced LC tank (QAmp). By changing the bias current I_Q, the QAmp can work as an amplifier or an oscillator. When receiving data from the antenna, the QAmp is configured as a bandpass amplifier with an enhanced Q. Due to the high Q bandpass filtering, the frequency modulated signal is converted to an amplitude modulated signal at the output of the QAmp, whereby simple envelope detection can
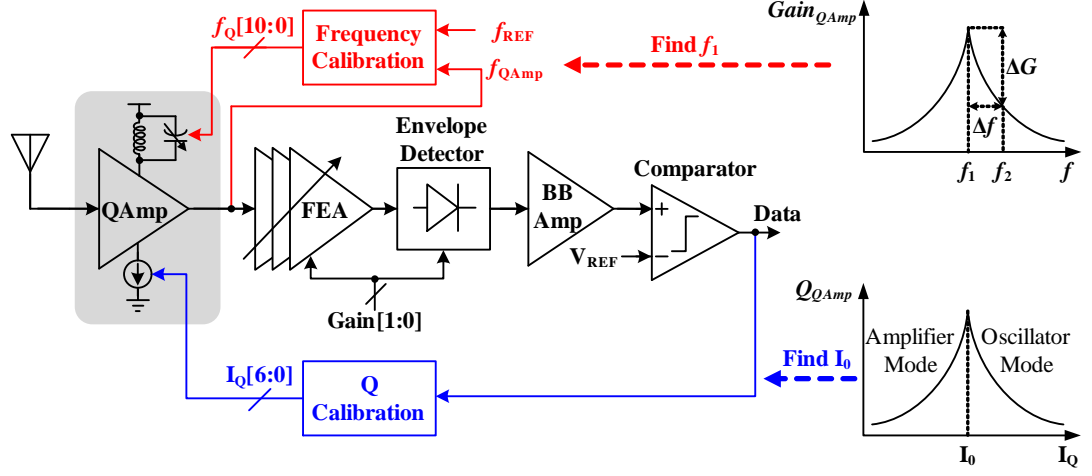
Figure 4.3: System architecture.

be utilized for demodulation. The front-end amplifier (FEA) offers additional gain to suppress the noise contribution from the envelope detector that follows [64]. The gain of the front-end amplifier is variable to improve the dynamic range of the receiver. In the baseband, after amplification through a differential baseband amplifier (BB Amp), the oversampled data stream is generated by a latched comparator and time integration over a bit period is performed off-chip to retrieve the original data. The reference voltage of the comparator, V_{REF}, is the average voltage of the BB amp output stored on a large capacitor when the receiver is receiving equal-probability "0"s and "1"s in the packet preamble.

There are several advantages for this Q-enhanced frequency-to-energy conversion architecture. With an enhanced Q, the gain of the QAmp is boosted at the center frequency (f_1). Additionally, the conversion gain (CG), which is defined as $\Delta G / \Delta f$ as shown in Fig. 4.3, is increased with an enhanced Q. The boosted center-frequency gain

and the increased conversion gain improve the sensitivity of the receiver. Furthermore, a smaller Δf is required for the same ΔG due to a larger conversion gain, leading to an improved spectral efficiency. Finally, frequency-to-amplitude conversion is performed by a linear amplifier, therefore, the maximum data rate is not limited and the energy efficiency can be improved through a higher data rate.

Two calibrations are performed when the receiver is powered on (Fig. 4.3). Initially, by monitoring the envelope of the QAmp output, the current calibration utilizes a successive approximation register (SAR) logic to find the critical current (I_0) where QAmp starts to oscillate. Afterwards, with QAmp in the oscillator mode, the frequency calibration loop calibrates the capacitor array of the LC tank until the center frequency of the tank is aligned to f_1. Finally, QAmp is set in the high Q amplifier mode and the receiver starts to retrieve data. A fast frequency calibration technique is utilized to minimize the start-up time.

4.3   Q-enhanced Frequency-to-Amplitude Conversion

4.3.1   Two Modes of QAmp

The conceptual model of the QAmp is shown in Fig. 4.4, which contains the effective transconductance (G_{mi}), the equivalent parallel resistor modeling the loss of the LC tank (R_p), inductor (L), capacitor (C), and the effective negative conductance added by the active devices ($-G_{mn}$). The sign of the total parallel resistance, $R = 1/(1/R_p - G_{mn})$, determines the operating mode of the QAmp. When the bias current of the QAmp is
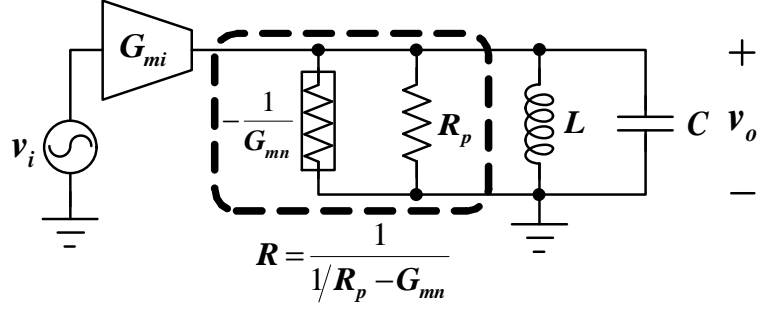
Figure 4.4: Conceptual model of the QAmp.

smaller than I_0 (the critical current where QAmp starts to oscillate), $R > 0$. Therefore, the QAmp behaves as a linear amplifier with an effective transconductance of G_{mi} and an RLC load. When the bias current is increased beyond I_0, $R < 0$ whereby the QAmp starts oscillating. In both modes, a larger $|R|$ indicates a higher Q.

4.3.2   Q-enhanced RLC Bandpass Filtering

When receiving data, the QAmp is configured in the amplifier mode with $R > 0$. The enhanced Q of the RLC load is

$$Q_e = R\sqrt{\frac{C}{L}} = \frac{1}{1/R_p - G_{mn}} \cdot \sqrt{\frac{C}{L}}. \tag{4.1}$$

$Q_e \rightarrow +\infty$ when $1/(R_p - G_{mn}) \rightarrow 0_+$, indicating an enhanced Q for the RLC load. The effect of Q-enhancement on the performance of the QAmp is analyzed next.

4.3.2.1   Center-frequency Gain and Conversion Gain

The impedance of the RLC tank is

$$Z_{tank} = \frac{s/C}{s^2 + s/(RC) + 1/(LC)} = \frac{s/C}{s^2 + s\omega_n/Q_e + \omega_n^2}, \tag{4.2}$$

where

$$\omega_n = 2\pi f_n = \frac{1}{\sqrt{LC}} \tag{4.3}$$

is the natural frequency of the RLC tank. Therefore, the gain of the QAmp is

$$G = |G_{mi}Z_{tank}| = G_{mi}\frac{Q_e}{\omega_n C} \frac{1}{1 + Q_e^2\left(\frac{\omega_n}{\omega} - \frac{\omega}{\omega_n}\right)^2} = G_{mi}\frac{Q_e}{2\pi f_n C} \frac{1}{1 + Q_e^2\left(\frac{f_n}{f} - \frac{f}{f_n}\right)^2}. \tag{4.4}$$

The gain response in dB is shown in Fig. 4.5 and the center-frequency gain G_{f_n} is the maximum gain. Assuming the frequencies are $f_1 = f_n$ and $f_2 = f_n + \Delta f$ for a received "0" and "1", respectively, the gain of the QAmp for "0" and "1" input signal are

$$G_{f_1} = G_{f_n} = G_{mi}\frac{Q_e}{2\pi f_n C} \tag{4.5}$$

and

$$G_{f_2} = G_{mi}\frac{Q_e}{2\pi f_n C} \frac{1}{1 + Q_e^2\left[\frac{(2f_n + \Delta f)\Delta f}{(f_n + \Delta f)f_n}\right]^2}, \tag{4.6}$$
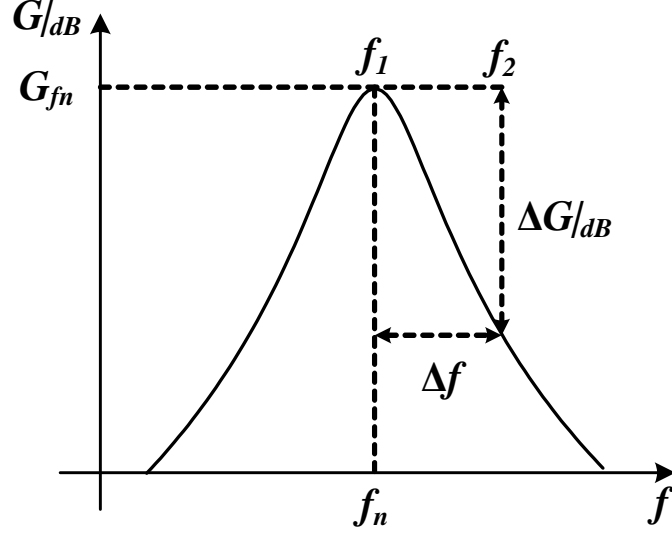
Figure 4.5: Gain response of the QAmp, with the center-freuqency gain G_{f_n} (=G_{f_1}) and the conversion gain $CG = \Delta G|_{dB}/\Delta f$.

respectively. A performance metric for the frequency-to-amplitude conversion, $CG = \Delta G|_{dB}/\Delta f$, is defined to characterize the achievable output gain difference $\Delta G|_{dB}$ with a certain input deviation frequency Δf (Fig. 4.5). A larger conversion gain (CG) corresponds to a better sensitivity and a smaller required Δf. Referring to (4.5) and (4.6), CG is given as

$$CG = \frac{\Delta G|_{dB}}{\Delta f} = \frac{20\log_{10}\frac{G_{f_1}}{G_{f_2}}}{\Delta f} = \frac{10\log_{10}\left(1 + Q_e{}^2\left[\frac{(2f_n+\Delta f)\Delta f}{(f_n+\Delta f)f_n}\right]^2\right)}{\Delta f}. \tag{4.7}$$

Considering $f_n \gg \Delta f$, (4.7) can be simplified as

$$CG \approx \frac{10\log_{10}\left(1 + (2Q_e\Delta f/f_n)^2\right)}{\Delta f}. \tag{4.8}$$

From (4.5) and (4.8), an enhancement in Q_e increases both the center-frequency gain G_{f_1} $(=G_{f_n})$ and conversion gain CG. A larger G_{f_1} suppresses the noise contribution from the following stages, and a larger CG increase the signal-to-noise ratio (SNR), both of which improve the receiver sensitivity. Using f_n=900 MHz, Δf=5 MHz, $C = 4$ pF and G_{mi}=1 mS, the change of G_{f_1} and $\Delta G|_{dB}$ with Q_e is shown in Fig. 4.6. While G_{f_1} is linearly proportional to Q_e, $\Delta G|_{dB}$ increases at a rate of approximately 20 dB/dec for $Q_e > 100$.

4.3.2.2   Noise Figure

The noise sources in the QAmp include the thermal noise currents of the input transistor
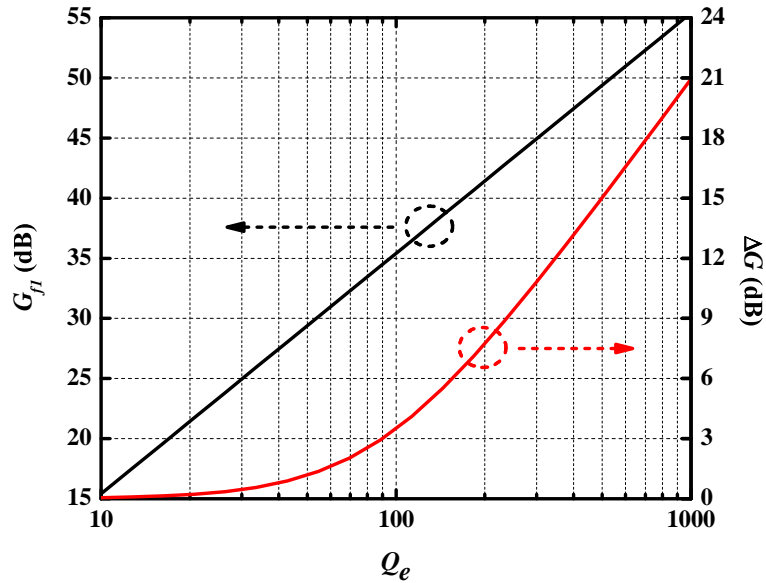
Figure 4.6: The change of G_{f_1} and ΔG with Q_e.

$(4kT\gamma g_{mi})$, the transistor providing the negative conductance $(4kT\gamma g_{mn})$, and the LC tank $(4kT/R_p)$. Assuming the input impedance is matched to $R_s = 50\ \Omega$, the noise figure (NF) of the QAmp can be derived as

$$NF = 1 + 4\frac{\gamma(\beta_i g_{mi} + \beta_n g_{mn}) + 1/R_p}{(\alpha g_{mi})^2 R_s} = 1 + \frac{4}{\alpha^2 R_s}\left[\frac{\gamma\beta_i}{g_{mi}} + \frac{\gamma\beta_n g_{mn}}{g_{mi}^2} + \frac{1}{g_{mi}^2 R_p}\right], \quad (4.9)$$

where the coefficients $\alpha = G_{mi}/g_{mi}$, β_i and β_n are noise scaling factors that depend on the circuit implementation. A larger Q_e requires a larger g_{mn}, increasing the noise contribution from the transistor providing the negative conductance. However, in implementations where the input transistor shares the bias current with the transistor providing the negative conductance, g_{mi} increases at the same rate as g_{mn}. In this case, the NF is improved with an enhanced Q_e.

4.3.2.3 Data Rate

The maximum data rate of the receiver is also affected by Q_e. When the input data changes at time $t = 0$, the transient response of the QAmp consists of a natural response and a forced response as given by

$$v(t) = v_n(t) + v_f(t). \quad (4.10)$$

While the forced response v_f is the desired signal with the QAmp in steady state ($v_f(t) = v(t \to +\infty)$), the natural response v_n will cause peaking and ringing at the output, there-

fore, increasing the settling time of the signal. The natural response of the second-order RLC tank in the QAmp is governed by the following differential equation

$$\frac{d^2v_n(t)}{dt^2} + 2\zeta\omega_n\frac{dv_n(t)}{dt} + \omega_n{}^2v_n(t) = 0, \tag{4.11}$$

where $\zeta = 1/(2Q_e)$ is the damping ratio [65]. The initial conditions are the value of $v(t)$ at $t = 0_+$ and the derivative of $v(t)$ at $t = 0_+$ which are defined as

$$v_0 = v(t)|_{t=0_+} \tag{4.12}$$

and

$$v_0' = \frac{dv(t)}{dt}|_{t=0_+}. \tag{4.13}$$

Because $\zeta = 1/Q_e < 1$ for the Q-enhanced RLC tank, the natural response of the QAmp is underdamped with a solution given by

$$v_n(t) = e^{-\zeta\omega_n t}\left[\frac{v_0' + \zeta\omega_n v_0}{\omega_d}\sin(\omega_d t) + v_0\cos(\omega_d t)\right], \tag{4.14}$$

where $\omega_d = \omega_n\sqrt{1 - \zeta^2}$ is the damped natural frequency. The natural response is a decaying sinusoid which is superimposed on the desired signal, leading to peaking and ringing in the output signal. The decay rate $e^{-\zeta\omega_n t}$ for several values of Q_e is plotted in Fig. 4.7(a). Note that a larger Q_e (corresponding to smaller ζ) results in a slower decay rate. The sinusoid persists for a longer time duration for a larger Q_e. To ensure correct reception of data, the natural response should decay significantly at the end of
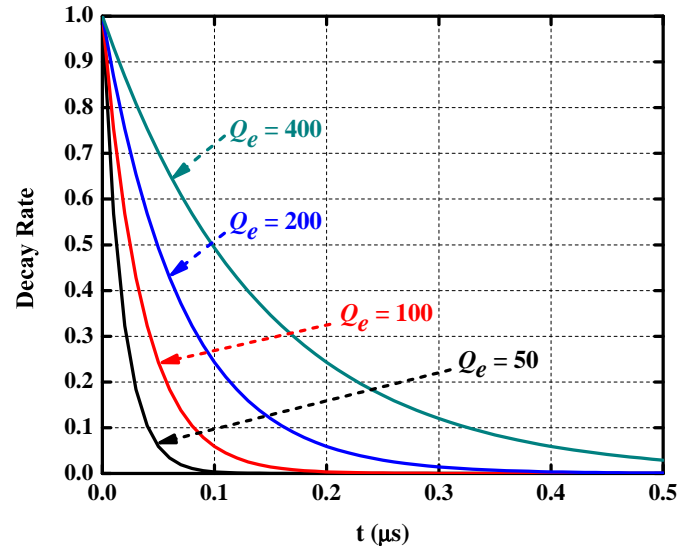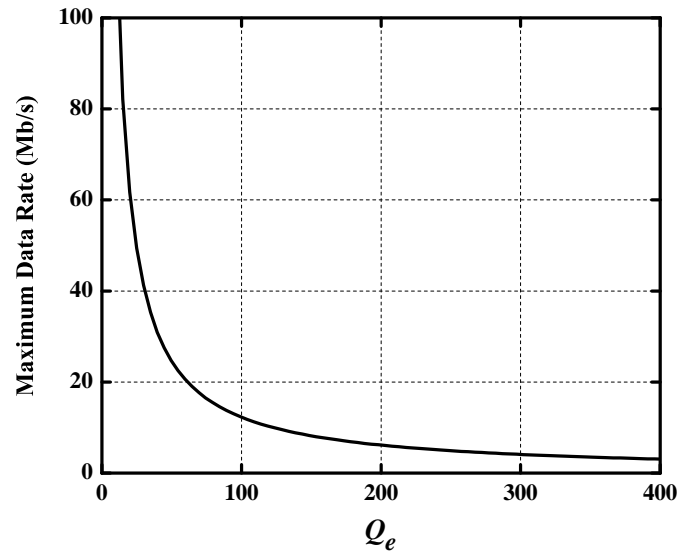
Figure 4.7: (a) Decay rate of the natural response of the QAmp for different Q_es. (b) The relation between maximum data rate and Q_e. Assuming $f_n = 900$ MHz and the natural response decays below 10% of its initial amplitude at the end of one bit period.

one data period. This limits the maximum data rate for a particular Q_e. Assuming f_n = 900 MHz and the natural response decaying below 10% of its initial amplitude at the end of one bit period, the maximum data rate is $DR_{max} = -\zeta\omega_n/\ln(0.1)$ which is plotted in Fig. 4.7(b). Without Q-enhanced, the maximum data rate is approximately 60 Mb/s with a Q_e of around 20. Then it decreases with an incresed Q_e, which sets an up limit of Q_e for a certain application.

4.3.3   Trade-Offs in Choosing Q

According to the aforementioned analysis, an increase in Q_e improves the receiver sensitivity with a boosted center-frequency gain and conversion gain, but degrades the energy efficiency due to the limited data rate. The appropriate value of Q_e should be a reasonable trade-off between sensitivity and data rate. In this work, a data rate of 10 Mb/s is targeted. From Fig. 4.7(a), a Q_e no larger than 100 is required to make the effect of ringing negligible and allow the transient response to settle within one bit period of 0.1 μs. Furthermore, the stability of the QAmp should also be taken into account. When a very high Q_e is chosen, the Q-enhancement circuit will be more sensitive to the circuit parameters and the QAmp may start oscillating due to a large input signal. Therefore, a Q_e of approximately 100 is chosen for this work. This corresponds to a ΔG of 4 dB with a Δf of 5 MHz (Fig. 4.6). The sensitivity is further improved with the additional gain contributed by the following front-end amplifier.

4.4 Circuit Implementation

4.4.1 QAmp

The schematic of the QAmp is shown in Fig. 4.8. A single-ended structure based on the Colpitts oscillator is chosen to eliminate the need for an external balun and allow for a power efficient single-ended front-end amplifier in the following stage. The bias current I_Q which determines the working mode of the QAmp is controlled by a 7-bit thermometer-code current digital-to-analog converter (DAC). In oscillation mode, M_0, M_1, and M_2 act as a cascode current source, while M_3 provides the negative conductance to the LC tank. In the amplification mode, L_G, C_{EX}, L_S and M_1 constitute the input transconductance with inductive degeneration narrow-band input matching, and the cas-
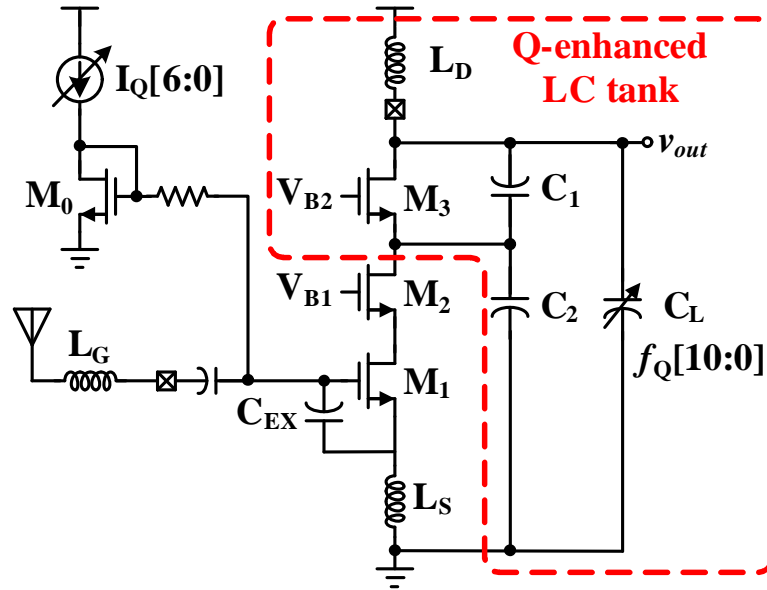
Figure 4.8: Schematic of QAmp.

code transistor M_2 improves the reverse isolation and stability. M_3 along with L_D, C_1, C_2, and C_L form a Q-enhanced RLC tank. The capacitors C_1 and C_2 are implemented with MIM capacitors and C_L consists of varactors with N-MOSFETs in accumulation mode. C_L is controlled by 11 digital bits, with the 7 most significant bits (MSBs) binary-weighted varators and a single varator controlled by the 4 least significant bits (LSBs) DAC. The frequency resolution is better than 200 kHz, which is significantly smaller than a Δf of 5 MHz.

Through small-signal analysis, the values of the parameters (as shown in Fig. 4.4) in this circuit implementation are

$$G_{mi} = Q_{in}g_{m1}\frac{g_{m3}+sC_1}{g_{m3}+s(C_1+C_2)} \approx Q_{in}g_{m1}\frac{C_1}{C_1+C_2}, \tag{4.15}$$

$$G_{mn} = g_{m3}\frac{C_1C_2}{(C_1+C_2)^2}, \tag{4.16}$$

$$L = L_D, \tag{4.17}$$

$$C = \frac{C_1C_2}{C_1+C_2} + C_L. \tag{4.18}$$

In (4.15), $g_{m3}/(C_1+C_2) < g_{m3}/C_1 \ll |j\cdot2\pi\cdot900\text{MHz}|$, and Q_{in} is the quality factor of the input matching network. As $G_{mn} > 1/R_P$ is required for oscillation, $g_{m3} > (C_1+C_2)^2/C_1C_2R_P$ is obtained according to (4.16). $C_1 = C_2$ is chosen to minimize the required g_{m3} which equals $4/R_P$.

Referring to (4.9) and considering $C_1 = C_2$, the NF of this QAmp is given as

$$
\begin{aligned}
NF &= 1 + \frac{4}{\left(Q_{in}\frac{C_1}{C_1+C_2}\right)^2 R_s}\left[\frac{\gamma\left(\frac{C_1}{C_1+C_2}\right)^2}{g_{m1}} + \frac{\gamma\left(\frac{C_2}{C_1+C_2}\right)^2 g_{m3}}{g_{m1}^2} + \frac{1}{g_{m1}^2 R_p}\right] \\
&= 1 + \frac{4}{Q_{in}^2 R_s}\left(\frac{\gamma}{g_{m1}} + \frac{\gamma g_{m3}}{g_{m1}^2} + \frac{4}{g_{m1}^2 R_p}\right) \quad .
\end{aligned}
\tag{4.19}
$$

A large R_P (high Q load inductor and capacitors) and a large Q_{in} (high Q input matching network) should be used to improve the NF. As g_{m1} and g_{m3} increase at a similar rate when the bias current is increased, the NF will be improved with an enhanced Q_e in this design.

4.4.2   Front-end Amplifier and Baseband Circuits

The variable gain front-end amplifier is implemented through multiple gain paths as shown in Fig. 4.9. The variable gain improves the dynamic range of the receiver, with a higher gain set for a weaker input signal power and a lower gain set for a stronger input signal power. A 2-bit digital gain control enables only one of the four paths at a time. The input stage of the four paths are the same, therefore, the load impedance seen from the preceding QAmp remains the same. Compared with variable gain control implemented in a single-stage amplifier [66], this multi-path structure achieves optimal energy efficiency. One reason is that a multi-stage amplifier is more energy efficient than a single-stage amplifier to achieve the same gain [67]. The other reason is that each front-end amplifier is optimized for maximum energy efficiency and is enabled only

when necessary.

The schematic of the front-end amplifier is shown in Fig. 4.10. M_1 and M_2 consti-

Figure 4.9: Multipath front-end amplifier (FEA) and envelope detector (ED) with gain control.

Figure 4.10: Schematic of front-end amplifier with an active inductor.

tutes the cascode input transconductor. A biasing current source with AC decoupling at the source of M_1 is used to accommodate DC coupling between stages and minimize the parasitics. An active inductor comprising M_3, M_4 and M_5 is used as the load to achieve high Q with a much smaller area compared with a passive LC tank [68]. The noise penalty from the active inductor is mitigated by the boosted gain in the preceding QAmp.

The envelope detectors, as shown in Fig. 4.11, are common source amplifiers with a shared RC load. The input transistors M_1 and M_2 are biased in the weak-inversion region to function as a bipolar transistor. Only one of the four envelope detectors is enabled along with its preceding front-end amplifier at any given time. Compared with the common drain envelope detector [69], this common source envelope detector offers
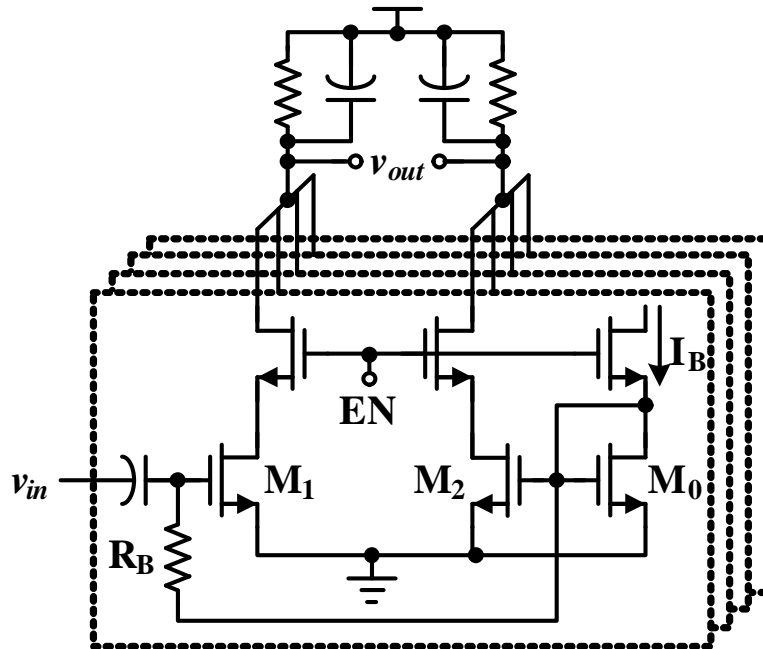
Figure 4.11: Schematic of common-source envelope detectors with shared RC load.

a much higher gain which outweighes the extra noise from R_B. The value of R_B should be chosen carefully, as a smaller R_B introduces less noise but degrades the loading Q of the preceding front-end amplifier.

In the baseband, a common source differential amplifier is used to further amplify the output voltage from the envelope detector. Finally, an ultra-low power differential comparator [70], which consumes no static power, is used to compare and oversample the data.

4.4.3   Frequency and Current Calibration

When the receiver is powered on, it will go through a digital calibration cycle before receiving data to find the correct center frequency and Q for the QAmp, as shown in Fig. 4.12. First, the 5 MSBs of I_Q are found through the SAR logic. Beginning from $I_Q[6]$, each bit is set to "0" if oscillation of the QAmp is detected, or "'1' if no oscillation is detected. Next, frequency calibration calibrates f_Q to lock the resonant frequency of the QAmp to f_1. Finally, fine calibration is carried on the 3 LSBs of I_Q to increase the resolution of the bias current so that a larger Q_e is achievable. Note that the current calibration is split into coarse and fine calibrations. This is because the critical current required for oscillation, I_0, changes with the frequency control bits, f_Q, due to the limited Q of the varators. Therefore, coarse current calibration should be carried out before frequency calibration to ensure the QAmp is oscillating during frequency calibration. Fine current calibration should be carried out after the frequency calibration to ensure the correct I_0 is obtained at the desired frequency f_1.

To minimize the start-up time, a fast frequency calibration is adopted as shown in Fig. 4.12 [71]. The frequency of the QAmp oscillation output f_{QAmp} is divided by a programmable divider with a division ratio N. An identical programmable divider with division ratio set to 1 is inserted after the reference signal f_{REF} to mimic the delay introduced by the divider. The programmable divider will give a rising edge when N is reached, and a rising edge comparator will detect which rising edge occurs earlier. The result will be evaluated by the digital SAR logic to set the frequency control bit $f_Q[10:0]$. The timing diagram for one cycle of frequency calibration is shown in Fig. 4.13. The programmable divider for f_{REF} starts counting between 3 μs and 5 μs, so the rising edge of f_{REF} at 5 μs will give a rising edge of f_{REF}/N with the delay of the programmable divider. Meanwhile, the programmable divider for f_{QAmp} starts counting at the time of 1
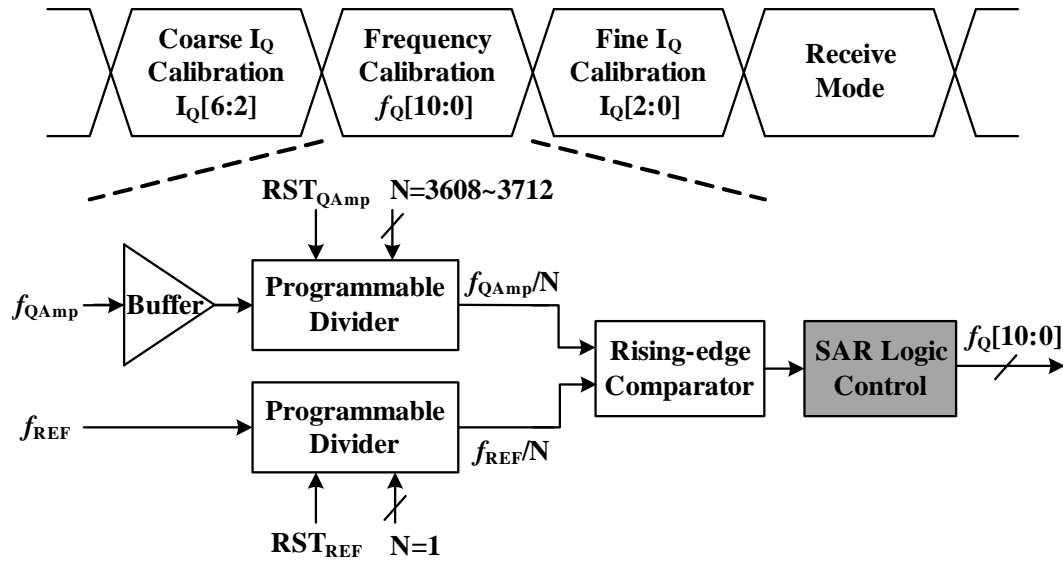
Figure 4.12: Timing diagram of the digital calibration and block diagram of the frequency calibration circuits.
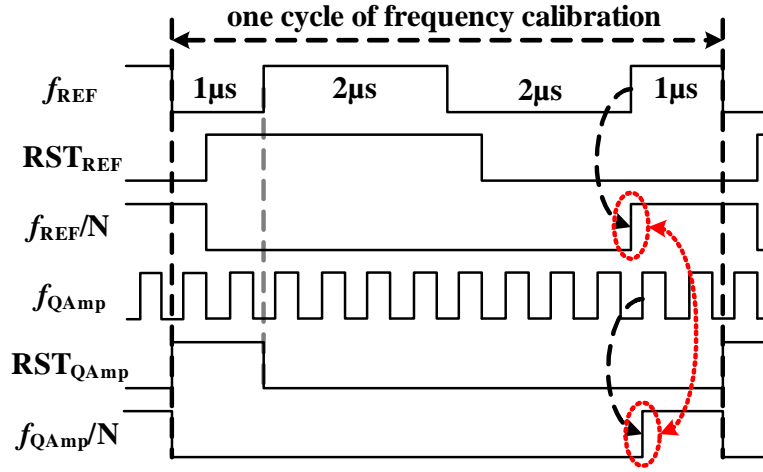
Figure 4.13: Timing diagram of one cycle of frequency calibration.
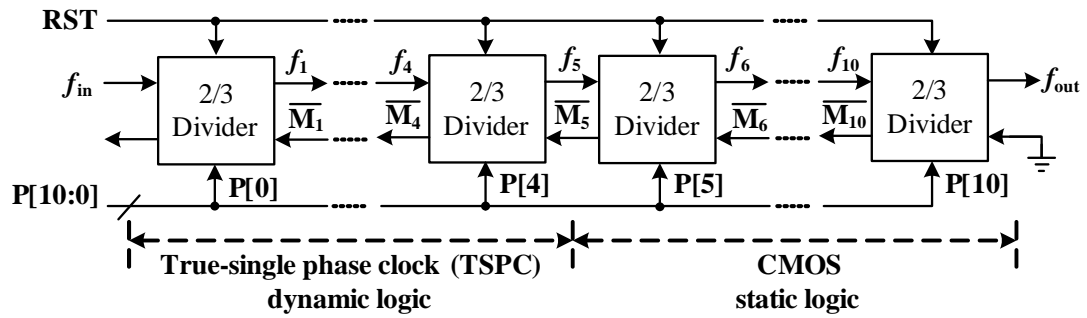
Figure 4.14: Truly modular programmable divider.

μs, and gives a rising edge of f_{QAmp}/N when $N = f_1 \cdot (4\mu s)$ is reached. If the rising edge of f_{QAmp}/N occurs first, $f_{QAmp} > f_1$ is detected. Otherwise, $f_{QAmp} > f_1$ is detected. Due to the phase uncertainty of f_{QAmp} when counting starts, the frequency resolution of this calibration is $1.5/(4\mu s) = 375$ kHz [71]. The total calibration time is 98 μs, including 32 μs for the current calibration and 66 μs for the frequency calibration.

The programmable divider is a truly modular programmable divider as shown in Fig. 4.14 [72]. It consists of a cascade of 11 stages of 2/3-divider cells. The first 5

2mm

1.5mm

Dividers & Digital Control

Qamp & Buffer

Base band Test Buffers

FEAs & EDs
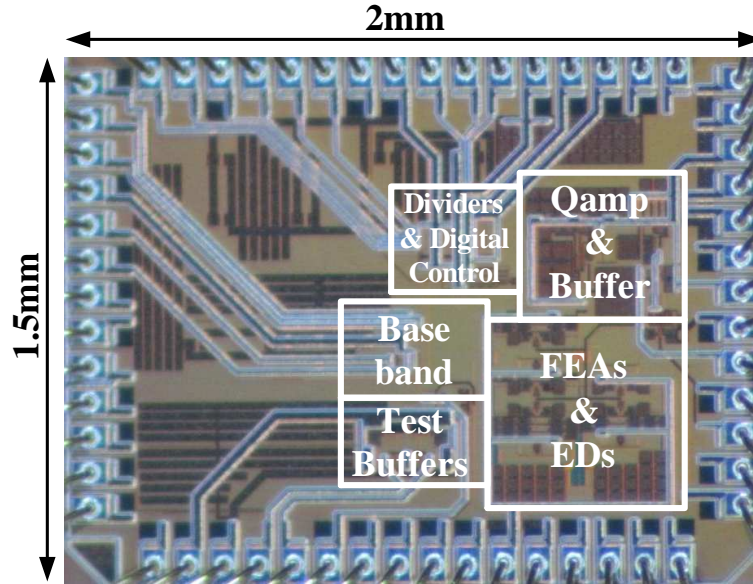
Figure 4.15: Chip microphotograph.

stages of the 2/3 dividers work at high frequencies and are implemented using true-single phase clock (TSPC) dynamic logic to minimize the number of transistors and the power consumption. The last 6 stages of the 2/3 dividers utilize CMOS static logic since the operating frequency is low.

4.5 Experimental Results

The receiver prototype has been fabricated in a 1P8M 0.13-μm CMOS process. The microphotograph of the chip is shown in Fig. 4.15, with all pins fully ESD protected. The chip was bonded in a standard QFN package and tested with a standard four-layer FR4 PCB board. All the measurements have been performed with a 0.7 V supply.

Figure 4.16 plots the relative gain of the QAmp which is normalized to the center-
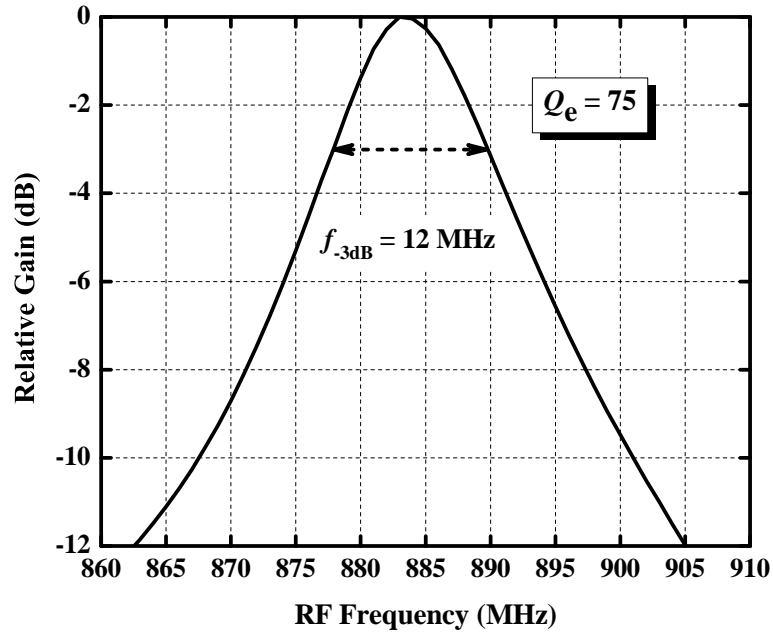
Figure 4.16: Measured Q_e of the QAmp.

frequency gain. With a power consumption of 350 μW, the Q_e of the QAmp is measured as 75.

The bit error rate (BER) of the receiver for different data rates is measured and the results are shown in Fig. 4.17. The data rates are measured in the range from 0.5 Mb/s to 6 Mb/s to fully characterize the performance of the receiver. For a BER of 0.1%, the sensitivity and energy efficiency of the receiver with different data rates are plotted in Fig. 4.18. A sensitivity of -90 dBm is achieved at a data rate of 0.5 Mb/s. The energy efficiency is as low as 80 pJ/b for a data rate of 6 Mb/s. This plot demonstrates the performance trade-off between sensitivity and energy efficiency.

The dynamic range of the receiver was measured for a data rate of 1 Mb/s and a BER of 0.1%. The dynamic range for each gain setting of the front-end amplifier is shown
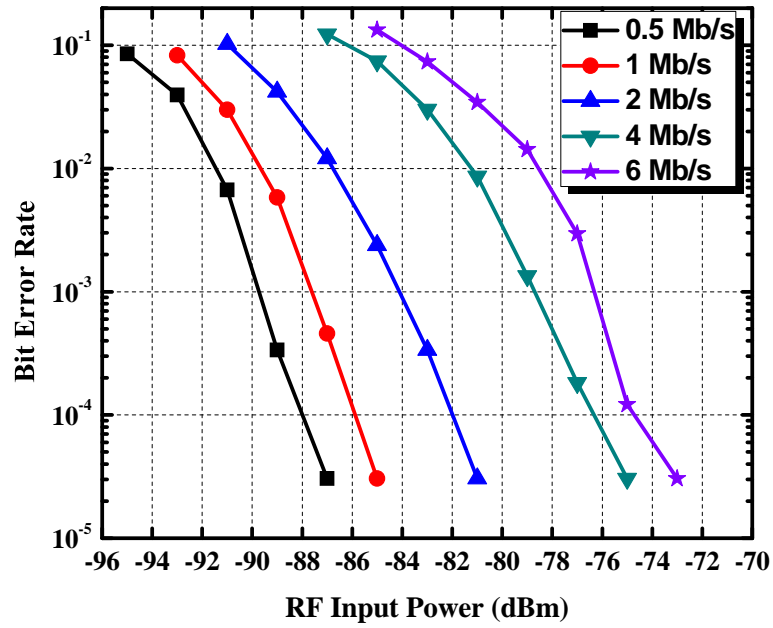
Figure 4.17: Measured BER of the receiver with different data rates.
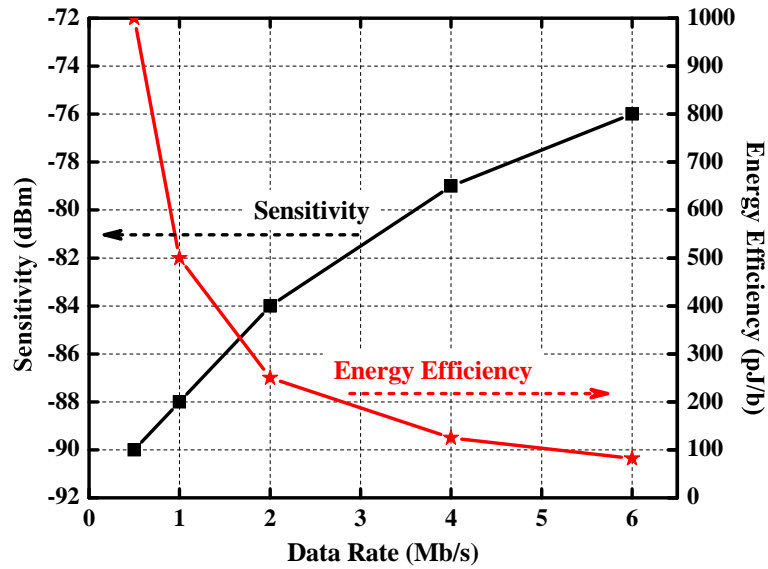
Figure 4.18: Measured sensitivity and energy efficiency with different data rates.
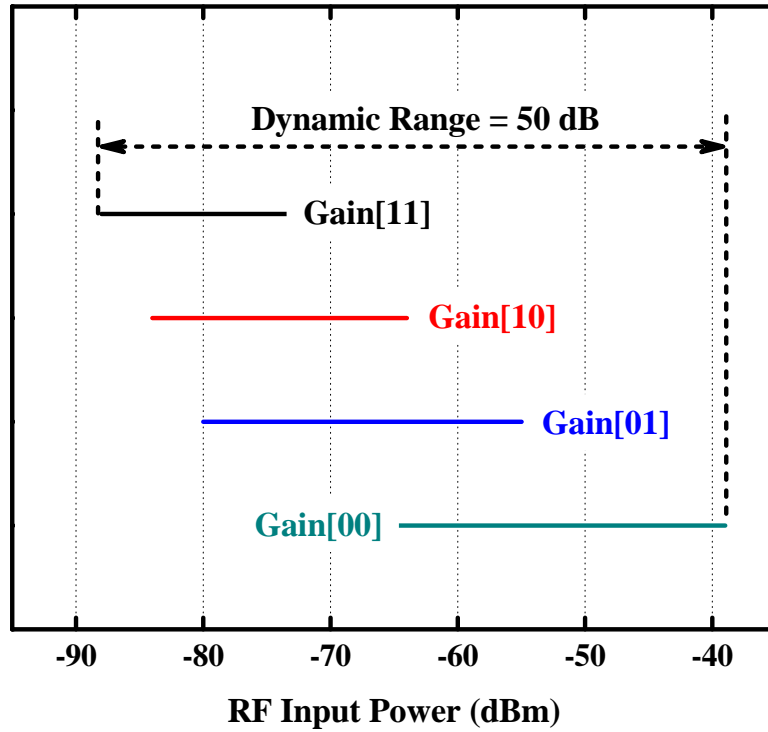
Figure 4.19: Measured dynamic range of the receiver.

in Fig. 4.19. For each gain setting, the lower bound of the input power is determined by the sensitivity of the receiver, and the upper bound is limited by the saturation of the baseband amplifier. The total dynamic range is 50 dB obtained as a result of the variable gain mechanism.

Interference tolerance measurements were also conducted to demonstrate the receiver performance in the presence of large blocking signals. The data rate is set to 1 Mb/s, the input signal to the receiver is set at +3 dB above the sensitivity, and the blocker power is swept until the BER is degraded to 0.1%. The signal-to-interference ratio (SIR) is taken as the ratio of the signal to blocker power, which is shown in Fig. 4.20. The
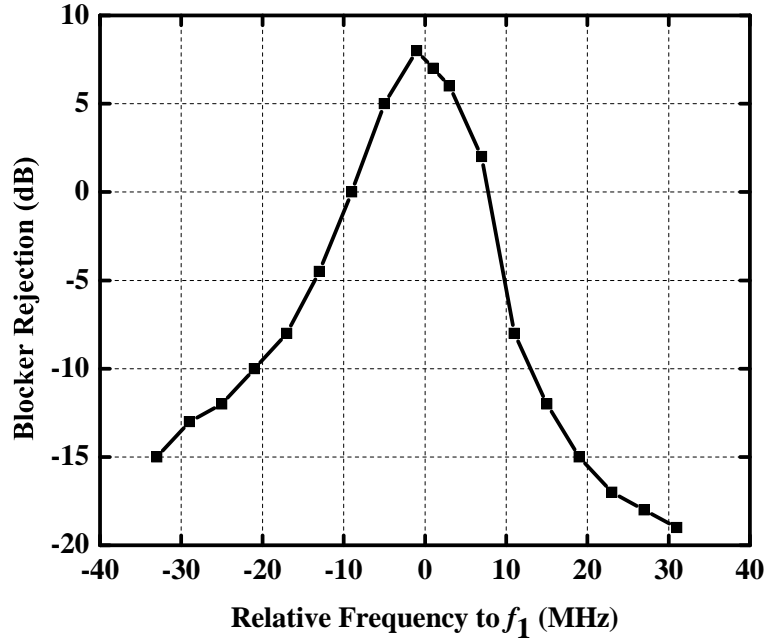
Figure 4.20: Measured blocker rejection.

interference tolerance, mainly determined by the RF bandwidth, is enhanced by the Q_e of the QAmp, demonstrating a SIR greater than -10 dB at 20 MHz offset frequency.

Table 4.1 summarizes the power consumption and measured performance of the receiver. Table 4.2 compares the performance with the state-of-the-art low power BFSK receivers for sensor network applications. The best sensitivity is achieved at a data rate of 500 kb/s and the best energy efficiency is obtained at a data rate of 6 Mb/s with an ultra-low power consumption. Furthermore, this work achieves the best figure of merit (FOM) as defined in [20]. This comprehensive FOM includes all of the main receiver parameters, i.e., power consumption, data rate, and sensitivity. Figure 4.21 compares the energy efficiency and FOM of this work with recently published low power OOK and BFSK receivers for WSN applications. Better FOMs are achieved for this work at

Table 4.1: Measured Performance Summary

Power Consumption @ 0.7 V Supply		
QAmp	350 μW	
Front-end Amplifier	42 $\sim$ 112 μW	
Envelope Detector	17 μW	
Baseband Amplifier	24 μW	
Total	430 $\sim$ 500 μW	
Measured Performance		
RF Frequency	900 MHz	
Dynamic Range	50 dB	
Data Rate	0.5 Mb/s	6 Mb/s
Sensitivity	-90 dBm	-76 dBm
Energy Efficiency	1 nJ/b	80 pJ/b

different data rates while maintaining excellent energy efficiencies. This makes the new receiver architecture a promising candidate for ultra-low power WSN applications.

4.6   Summary

A new mixer-less low energy BFSK receiver is presented. High gain frequency-to-amplitude conversion is achieved using a linear amplifier with a Q-enhanced LC tank, eliminating the need for LOs and mixers. The high center-frequency gain and conversion gain provided by the Q-enhancement improves the sensitivity as well as the interference rejection. A smaller deviation frequency for BFSK modulation is achieved by virtue of the high conversion gain, thereby improving the spectral efficiency. Furthermore, a higher data rate is realized due to the linear amplification, leading to excellent energy

Table 4.2: Comparison of the State-of-the-art BFSK Receivers for WSN Applications

Reference	[30]	[31]	[33]	[19]	[20]	[22]	This Work		
Architecture	Zero-IF	Low-IF	Low-IF	Super-regenerative	Super-regenerative	Injection-Locked	Q-enhanced		
Technology	0.13 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.18 μm	0.13 μm		
Frequency	900 MHz	400 MHz	400 MHz	900 MHz	2.4 GHz	900 MHz	900 MHz		
Supply	1.2 V	1.8 V	0.7 V	1.3 V	0.65 V	0.7 V	0.7 V		
Power (P_{RX})	1.92 mW	8.5 mW	490 μW	400 μW	350 μW	420 μW	500 μW	500 μW	480 μW
Data Rate (DR)	45 kb/s	0.2 Mb/s	0.25 Mb/s	1 Mb/s	2 Mb/s	5 Mb/s	0.5 Mb/s	2 Mb/s	6 Mb/s
Energy Efficiency	42.7 nJ/b	42.5 nJ/b	1.96 nJ/b	400 pJ/b	175 pJ/b	84 pJ/b	1 nJ/b	250 pJ/b	**80 pJ/b**
Sensitivity (P_{SEN})	-89 dBm	-76 dBm	-70 dBm	-69 dBm	-75 dBm	-73 dBm	**-90 dBm**	-84 dBm	-76 dBm
***FOM*†**	193 dB	180 dB	187 dB	193 dB	203 dB	204 dB	**210 dB**	**210 dB**	**207 dB**

† $FOM = -10 \cdot \log_{10}(P_{RX} \cdot P_{SEN}/DR)$.
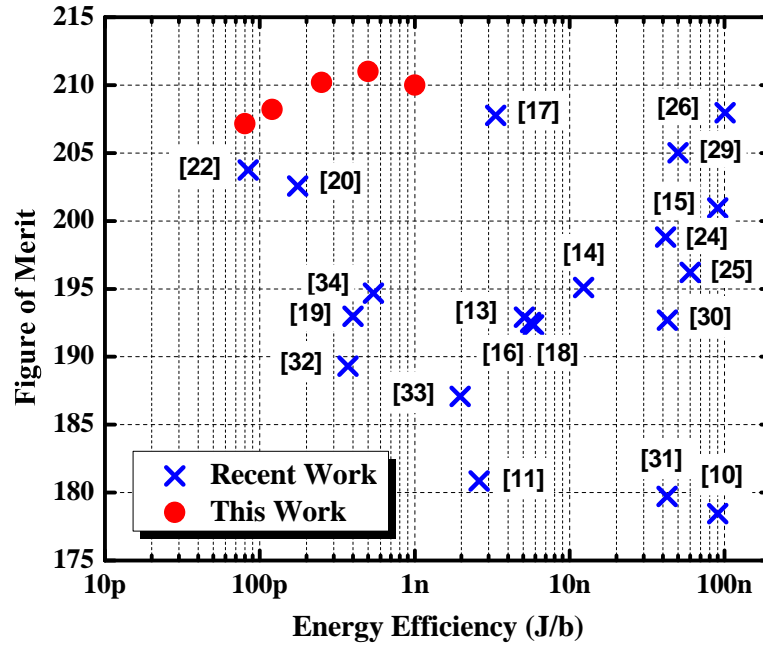
Figure 4.21: Performance comparison with recently published low power OOK/BFSK receivers for WSN applications.

efficiency.

A 900 MHz prototype receiver, including digital-assisted frequency and current calibration, is implemented using a 0.13-μm process. With a power consumption of 500 μW, a sensitivity of -90 dBm and -76 dBm is demonstrated for a data rate of 0.5 Mb/s and 6 Mb/s, respectively. The energy efficiency is 80 pJ/b for a data rate of 6 Mb/s. The excellent sensitivity combined with the compelling energy efficiency renders the receiver the best FOM compared with state-of-the-art work published to date.

Chapter 5: Conclusion

Wireless sensor nodes (WSNs) are being seamlessly integrated in various applications. These include home automation, medical monitoring, industrial control, and military surveillance. The key performance requirements for a sensor node are cost, battery life, and reliability. This work presents two new receiver architectures for sensor node communications that address different performance characteristics.

A hybrid polyphase filter (PPF) based receiver is presented for medium data rate WSN applications, with a modulation index (MI) less than or equal to 2 to improve the spectral and energy efficiencies. The frequency offset tolerance (FOT) of the PPF-based receiver is analyzed and optimized. Using frequency-to-energy conversion through PPFs, the new receiver achieves high FOT without any complex and power hungry frequency correction circuits. Excellent adjacent channel rejection (ACR) is also attained at reduced power through a hybrid topology in the PPFs. A 2.4 GHz prototype receiver, including RF and analog front-ends, is implemented for a data rate of 1 Mb/s, demonstrating measured FOTs of ± 180 ppm and ± 44 ppm, and measured ACRs of 40 dB and 33 dB for a MI of 2 and 1, respectively. A sensitivity of -84 dBm is achieved with a power consumption of only 1.97 mW.

The high FOT relaxes the frequency accuracy requirement of the LOs in transmitters and receivers, reducing the cost and power of the WSN links. The small MI combined with a large ACR improves the spectral efficiency and radio co-existence in the pres-

ence of interferers. This receiver is suitable for WSN applications that operate in the presence of other radios, such as building automation, intra-vehicle connectivity, and medical monitoring. WiFi, Bluetooth, and Zigbee radios may exist and good interference tolerance of this zero-IF architecture guarantees reliable communication without frequent retransmissions.

An additional reduction in power consumption is achieved with a novel low energy mixer-less BFSK receiver. Frequency-to-amplitude conversion is achieved by a linear amplifier with a Q-enhanced LC tank, whereby envelope detection can be used to retrieve the data. This structure provides excellent energy efficiency as it eliminates the need for a local oscillator and a mixer. The sensitivity and interference rejection are improved by use of high Q filtering. Operating in the 900 MHz ISM band, the fabricated prototype demonstrates a sensitivity of -90 dBm and -76 dBm for data rates of 0.5 Mb/s and 6 Mb/s, respectively. An energy efficiency of 80 pJ/b is achieved when operating 6 Mb/s, making it the most power efficient receiver to date.

This mixer-less receiver architecture is ultra-low power and extends the battery life. The data rate can be scaled from several kb/s up to 6 Mb/s, which makes it suitable for applications with different data throughputs. This receiver is well suited for applications where there is a small number of interferers. Examples include outdoor temperature or humidity sensor networks in fields, forests, and greenhouses. In these applications, the possibility of other radio systems interfering with the WSNs is significantly reduced.

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