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Title: Design of CMOS Switched-Current Filters

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Dr. David J. Allstot

The design and implementation of Switched-Current (SI) ladder filters is described. SI filters require only a standard digital CMOS process and the power supply voltage requirement is low. SI circuits also can be potentially operated at higher frequencies than Switched-Capacitor (SC) filters due to the low-impedance wideband nodes of the current mirrors. A simple method has been developed to design SI ladder and biquadratic filters with maximum dynamic range that leverages the well-established design methodologies of SC filters. A standard digital 2-micron n-well CMOS process has been used to implement two high-order ladder filters and two biquadratic filters. Simulations accurately predict the measured results of the first integrated SI filters. The area and power dissipation are comparable to the switched-capacitor technique.

Analysis of the factors that effect dynamic range in SI filters is presented. The factors that contribute to harmonic distortion in the current-mode circuits are characterized and the relationships to maximum signal size are established. Using measurements of the input-referred noise from SI filters, the dynamic range is obtained.

Design of CMOS Switched-Current Filters

by

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CHAPTER 1

INTRODUCTION

Integrated circuit design has progressed from a very simple flip-flop in 1958 [1] to today's integration of a system on a chip. A majority of today's systems are integrated using a CMOS process due to its relatively low cost and high reliability. Currently designed systems typically consist of both analog and digital circuitry with the digital circuitry consuming 80% of the area and the analog circuitry consuming 20% of the area. While the analog circuitry takes a small percentage of the die area, it typically requires up to 90% of the design effort. The analog circuitry allows interfacing the digital circuitry to the external world. Efforts are continually focused on improving the analog circuit accuracy and performance with the continued scaling of CMOS processes [2].

In the 1980's, the MOS Switched-Capacitor (SC) technique proved to be an efficient, accurate method for performing filtering and other signal processing operations [3]. This technique exploits the terminal characteristics of the voltage operational amplifier, the excellent matching properties of capacitors and the nearly ideal switch present in MOS processes. It provided a breakthrough for CMOS analog circuit design performance and it was the advent of mixed-mode CMOS integrated circuits. This trend toward mixed analog/digital systems has continued with much of the analog circuitry using the voltage operational amplifier as a critical

circuit block. While the voltage operational amplifier is a very useful circuit block, circuit designers should not be confined to using voltage techniques alone.

There is a need for continued improvement in analog circuit performance in order to meet the emerging system design specifications. Recently there has been growing interest in using current-mode circuits to improve analog circuit performance [4]. Current-mode circuits have current signal inputs and outputs. Although current-mode circuits do offer some advantages over voltage-mode circuits, they are not the solution to improving the performance of every analog system design. Ideally, a combination of voltage-mode and current-mode circuits will produce the highest system performance. Below are some examples of the advantages and disadvantages of using current-mode versus voltage-mode circuits.

The first consideration in designing an integrated circuit is how to interface the circuit to the external circuitry and test equipment. Most measurement equipment measures voltage signals. The measurement device has a high impedance level so that it can be placed in parallel with the circuit under test without loading the circuit and degrading the circuit performance. To measure a current signal requires that the measurement device be placed in series with the circuit under test and consequently, the measurement device must have a low impedance level. Hence, measuring a voltage signal is much more convenient because the test instrument can be placed in parallel with the circuit. Therefore, it is desirable to make the chip inputs and outputs voltage signals.

One on-chip master reference current is designed in the analog system and this precision current is then replicated across the die. Reproducing this precision reference inaccurately across the die defeats the efforts of designing the precision

reference. To reproduce the current accurately across the die, a current bias can be routed to localized areas and then multiple current references can be generated there. This technique eliminates errors due to transistor process mismatches and voltage drops across the die.

The accurately reproduced reference current provides the bias for many of the analog operations. One critical operation of many analog circuits is amplification. Both current and voltage signal amplification can be performed. The common-source amplifier, Fig. 1.1, performs a simple voltage amplification, while the simple current mirror, Fig. 1.2, performs current amplification. Voltage amplification is more area efficient than current amplification. For example, the common-source amplifier with bias current of 100 μA and W/L=100μ/10μ amplifies the voltage by approximately 100. To obtain a current gain of 100 in Fig. 1.2 would require that the aspect ratio of M_2 to M_1 be 100. For $(W/L)_1$=10μ/10μ, the aspect ratio of M_2 would have to be $(W/L)_2$=1000μ/10μ. To obtain the same current as voltage gain would require approximately an order of magnitude more area. Thus, for signal amplification, voltage rather than current amplification is preferred.

Conversely, comparison of these two circuits reveals wider bandwidth circuits are obtained using the current mirror. The *-3 dB* bandwidth of the common-source amplifier is (assuming a similar stage as the load):

$$BW_v = g_{ds}/C_{gs}, \tag{1.1}$$

while the *-3 dB* bandwidth of the current mirror is:

$$BW_i = g_m/C_{gs}. \tag{1.2}$$

Thus, the *-3 dB* bandwidth of the current mirror is approximately two orders of magnitude higher than the bandwidth of the voltage amplifier. The wideband characteristics of the current mirror are used in the current operational amplifiers [5]. The current op amp has a bandwidth independent of the closed loop gain (assuming a fixed unity current gain) unlike voltage operational amplifier bandwidths which are always a function of the closed loop gain.

As a final example, the operation of addition and subtraction of signals is considered. From Kirchhoff's Current Law (KCL), it is obvious that currents can be summed by a simple connection of the wires at a low-impedance node. Thus, current subtraction and addition are very efficient operations.

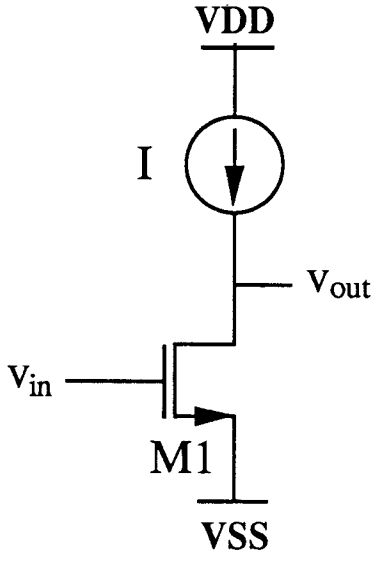


Fig. 1.1 Common-source voltage amplifier

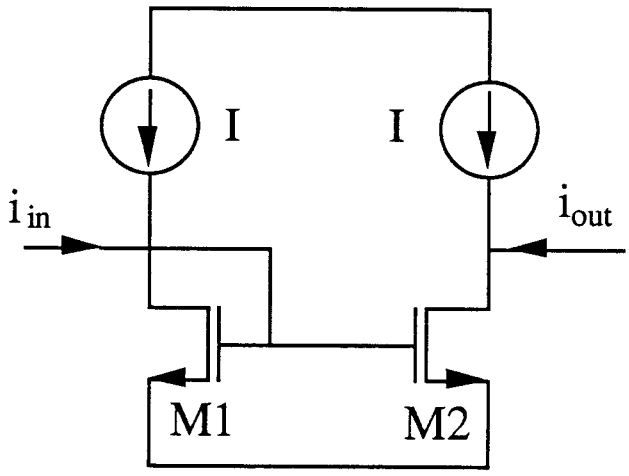


Fig. 1.2 Simple current amplifier.

In the following chapters, the design techniques of sampled-data current-mode filters are presented. The current-mode filtering technique called Switched-Currents (SI) complements the voltage-mode switched-capacitor technique. SC circuits use voltage operational amplifiers as the basic building block and require high power supply voltages to obtain low distortion, wide dynamic range voltage output signals. SI circuits employ current mirrors as current amplifiers and can operate at power supply voltages as low as 1.5V with a standard digital CMOS process. SC circuits require precision linear capacitors to accurately store charge that is then processed at the next time period. SI circuits use only the noncritical gate capacitance of the MOS transistor to store charge and therefore, no additional processing steps are needed to fabricate the precision storage element. The bandwidth capability of SI circuits is potentially much higher than SC circuits because wideband unity-gain current mirrors rather than high-gain voltage amplifiers are used. Although SI circuits offer potential benefits over SC circuits, at this time SI circuits are not as accurate as SC circuits. However, since SI circuits are in their infancy, it is expected that in time they will have accuracy comparable to SC circuits.

In this thesis, the design and integration of the first switched-current filters are discussed. In chapter 2, the design of SI filters using the signal flowgraph synthesis is described. The non-ideal characteristics of SI filters are analyzed and the experimental results from several SI filters are given. In chapter 3, the dynamic range limitations of SI filters are discussed. The harmonic distortion due to device mismatches and clock-feedthrough voltage is analyzed and several schemes are proposed to reduce the nonlinearities. The input-referred noise current of current-

mode circuits is also analyzed. The final chapter summarizes the work herein and discusses possible future areas of research.

CHAPTER 2

DESIGN CONSIDERATIONS FOR SWITCHED-CURRENT FILTERS

2.1 Abstract

The design and implementation of Switched-Current ladder filters is described. SI filters require only a standard digital CMOS process and the power supply voltage requirement is low. SI circuits can be potentially operated at higher frequencies than SC filters due to the low-impedance wideband nodes of the current mirrors. A simple method has been developed to design SI ladder and biquadratic filters with maximum dynamic range that leverages the well-established design methodologies of SC filters. A standard digital 2-micron n-well CMOS process has been used to implement two high-order ladder filters and two biquadratic filters. Simulations accurately predict the measured results of the first integrated SI filters. The area and power dissipation are comparable to the switched-capacitor technique.

2.2 Introduction

The switched-current circuit technique for analog sampled-data signal processing was recently introduced and demonstrated in CMOS technology [6, 7]. Unlike switched-capacitor circuits that require additional processing steps to fabricate precision linear capacitors [8], SI circuits can be integrated in a standard digital CMOS process. The SI circuit technique also has a low power supply voltage requirement since it uses wideband current mirrors as amplifiers as opposed to SC circuits which employ voltage operational amplifiers. In the SI sampled-data technique, the noncritical MOS transistor gate capacitance is used to store charge. The MOS transistor gate voltage corresponding to this charge produces the square-law output signal current.

In this chapter, the design of SI filters is described. In Section 2.3, the basic current-mode circuits are developed including the SI differential integrator/summer. The SI integrator/summer is shown to be directly analogous to the SC integrator/summer and thus, all the synthesis techniques developed for the design of SC filters can be used to synthesize SI filters. In Section 2.4, signal flowgraph synthesis of SI ladder filters is presented. In Section 2.5, the synthesis of SI biquadratic filters is described. The nonideal characteristics of SI filters that limit the filter accuracy are evaluated in section 2.6. Finally, in Section 2.7, the experimental results from the first integrated SI filters will be described.

2.3 Switched-Current Signal Processing

Signal processing requires four basic operations: 1) signal inversion, 2) summation, 3) scaling and 4) delay. Each signal processing operation can be implemented using current-mode circuits. A current amplifier, Fig. 2.1, performs the operations of summation, inversion and scaling. In the current amplifier, the AC signal currents, i_1 and i_2, are summed at the diode-connected node by connecting the wires. The diode-connected input node provides a low impedance current summation point. Multiple input currents can be summed at the amplifier input with negligible loading effects provided that the total peak signal current does not exceed the bias current. The summed input currents of the amplifier are inverted at the output. To scale the output current, the aspect ratio of M_2 to M_1 and the output bias current are scaled by a factor of K. For the current amplifier circuit, Fig. 2.1, the drain-source current of M_1 is the sum of the DC bias current, I, and the AC signal currents:

$$I_{ds_1} = I + i_1 + i_2. \tag{2.1}$$

The current in transistor M_1 is reflected to transistor M_2 and scaled by the aspect ratio K:

$$I_{ds_2} = K (I + i_1 + i_2). \tag{2.2}$$

The output current is the difference of I_{ds_2} and the output DC bias current:

$$i_{out} = - K (i_1 + i_2). \tag{2.3}$$

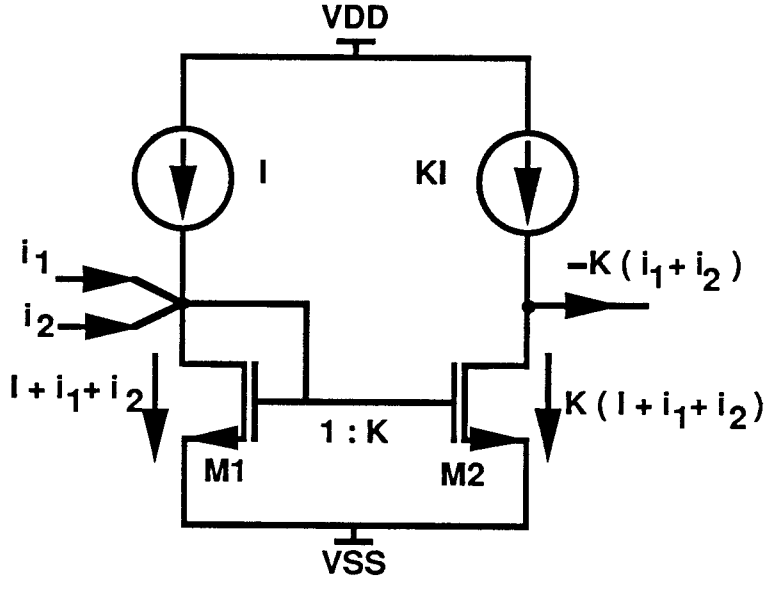


Fig. 2.1 A switched-current summing, inverting amplifier with scale factor K.

Therefore, the current amplifier efficiently performs summation, inversion and scaling of the input signals.

The final signal processing operation, signal current delay, is performed by the current track-and-hold (T/H), Fig. 2.2. The current T/H has two modes of operation: the track operation and the hold operation. In the track operation, Fig. 2.3(a), the switch is closed ideally shorting together the gates of M_1 and M_2. In the current amplifier of Fig. 2.3(a), the gate-source voltages of M_1 and M_2 change as a function of time as i_{in} varies with time:

$$V_{gs_1}(t) = V_{gs_2}(t). \tag{2.4}$$

The output current correspondingly changes as a function of time:

$$i_{out}(t) = i_{in}(t). \tag{2.5}$$

Therefore, the output current *tracks* the input current.

In the hold operation, Fig. 2.3(b), the switch is opened at time=T. The transistor gate capacitance of M_2 stores the charge corresponding to the voltage at time, T, when the switch opened. Thus, the output signal current is *held* at the value corresponding to the time when the switch opened:

$$i_{out}(t) = i_{in}(T)\,. \tag{2.6}$$

The current T/H operation is similar to that of dynamic circuits in digital circuit design. The non-critical MOSFET gate capacitance stores a charge that corresponds to a constant output until the gate voltage is updated.

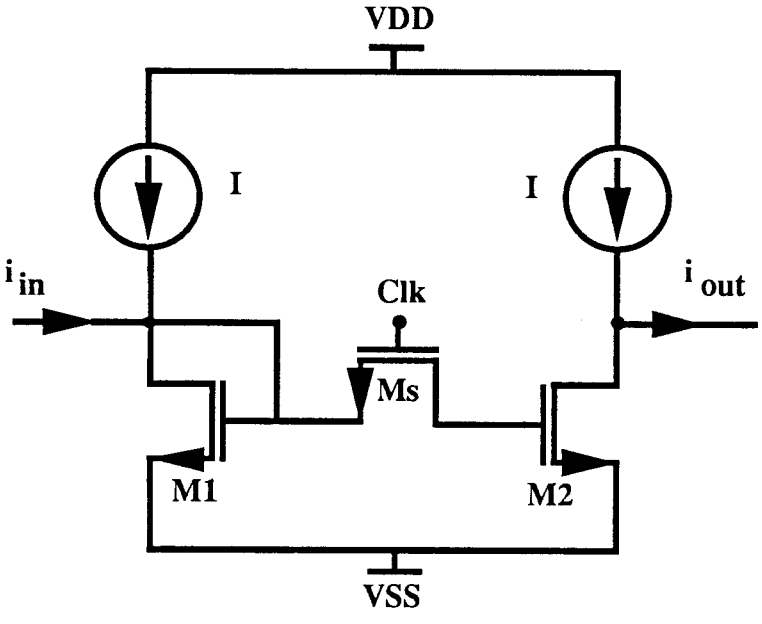


Fig. 2.2 An inverting switched-current track-and-hold circuit.

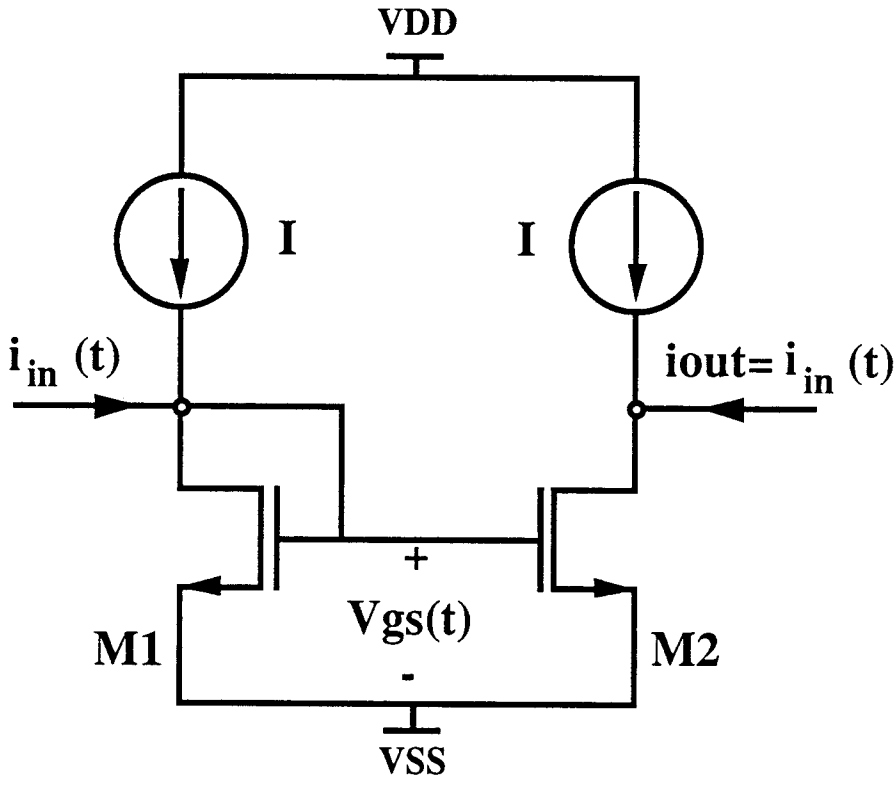


Fig. 2.3(a) Current T/H performing track operation.

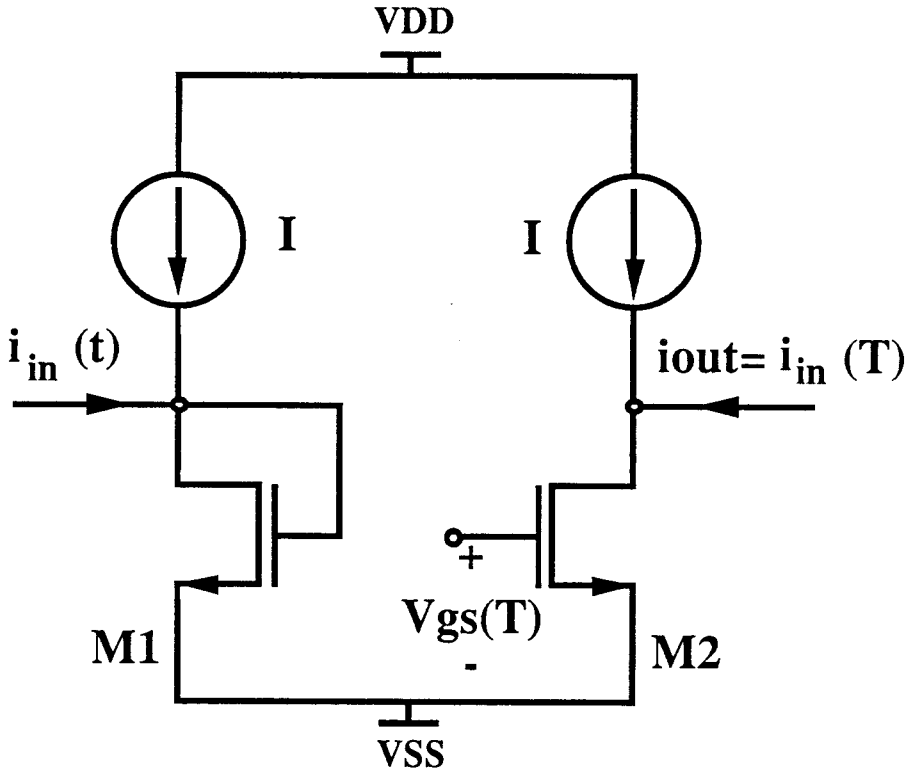


Fig. 2.3(b) Current T/H performing hold operation.

One form of the SI integrator, Fig. 2.4, is constructed using the four basic processing operations. The SI integrator is composed of two cascaded current T/H circuits. The switches are controlled by two-phase nonoverlapping clocks (all current mirror transistor pairs are assumed to be matched). There is one inversion through each T/H circuit. The non-inverting terminal is *at the input* of the first T/H. The inverting terminal is *after* the first T/H. Breaking the feedback path, the expression for the SI integrator output sampled on Clk1 is:

$$i_f(z) = (i_1 + i_f) z^{-1} - i_2 z^{-1/2}. \tag{2.7}$$

Rearranging this expression:

$$i_f(z) = \frac{(i_1 z^{-1} - i_2 z^{-1/2})}{(1 - z^{-1})}. \tag{2.8}$$

The $1 - z^{-1}$ term in the denominator represents discrete-time integration. In the numerator, the input at the non-inverting terminal, i_1, is delayed by one-period to the output, and the input at the inverting terminal, i_2, is delayed by one-half period to the output.

To employ the SI integrator as the basic building block for active filter design, the output current must be scaled. The integrator output is weighted by scaling the aspect ratio of M_5 to M_3 and the output bias current by a factor of K, Fig. 2.4. The output current is:

$$i_{out}(z) = K\, i_f(z). \tag{2.9}$$

Substituting the expression for i_f, Eqn. (2.8):

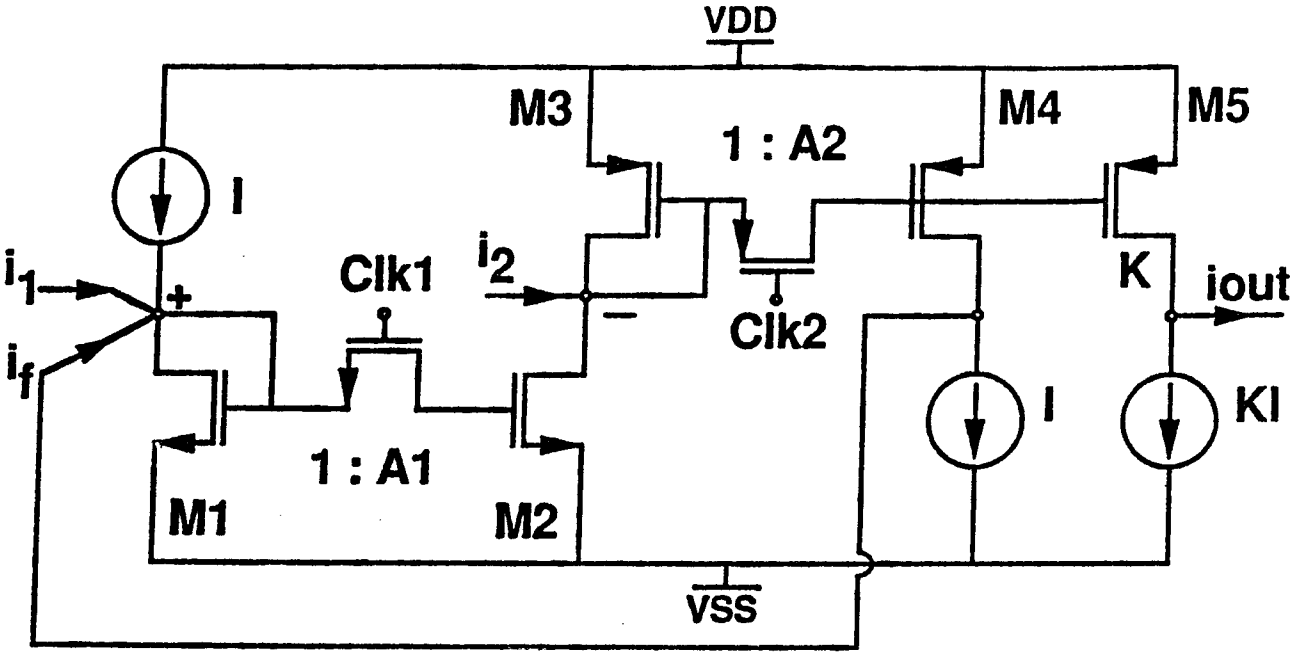


Fig. 2.4 A simplified schematic of a differential switched-current integrator. The circuit uses a two-phase non-overlapping clocking scheme.

$$i_{out}(z) = K \frac{(i_1 z^{-1} - i_2 z^{-1/2})}{(1 - z^{-1})} \tag{2.10}$$

where, K represents the integrator scale factor.

The SI integrator current output is directly analogous to the switched-capacitor integrator voltage output, Fig. 2.5, where:

$$V_{out}(z) = (C_U / C_I) \frac{(v_1 z^{-1} - v_2 z^{-1/2})}{(1 - z^{-1})}. \tag{2.11}$$

There are many analogies of the SC integrator to the SI integrator. In the SC integrator, a capacitor ratio, (C_U / C_I), determines the integrator scale factor. In the SI integrator, the integrator scale factor is determined by a transistor aspect ratio, K. In the SC integrator, unique input summing capacitors are required for each voltage input. While in the SI integrator, unique output branches are required for each current output. Only one output voltage is required in SC integrators, while currents are summed by connecting the wires at a single input of the SI integrator. Because of the direct correspondence of the SC and SI integrator transfer functions, all the existing SC filter synthesis techniques can be applied to the synthesis of SI filters. In the following section, the synthesis of SI ladder filters will be described.

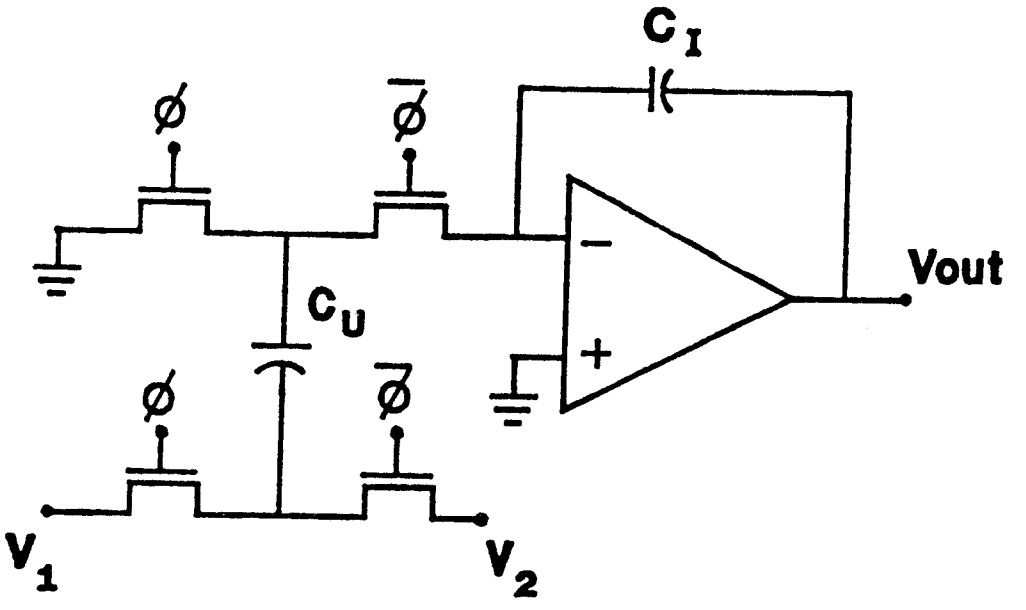


Fig. 2.5 A switched-capacitor integrator. The circuit requires a voltage operational amplifier, MOSFET switches, and precision capacitors.

2.4 Synthesis of SI Ladder Filters

The signal flowgraph synthesis of SI ladder filters requires the conversion of an RLC prototype filter into a signal flowgraph [9,10]. The signal flowgraph is then used to synthesize the SI ladder filter. The fifth-order lowpass all-pole doubly-terminated LC prototype is shown in Fig. 2.6(a). The doubly-terminated structure provides minimum sensitivity to component variations [11]. Voltage and current variables are assigned to each branch in the prototype, and then the signal flowgraph is constructed to satisfy Kirchhoff's loop and node equations.

Switched-current circuits process current signals, and as such, all of the signal flowgraph nodes must be transformed to current variables using a scaling resistor (chosen to be 1Ω for convenience). All the internal vertical branches are represented as integrations, and the output of each integrator is expressed as:

$$I_1' = \frac{1}{sC_1}(I_{in} - I_1' - I_2) \tag{2.12a}$$

$$I_2 = \frac{1}{sL_2}(I_1' - I_3') \tag{2.12b}$$

$$I_3' = \frac{1}{sC_3}(I_2 - I_4) \tag{2.12c}$$

$$I_4 = \frac{1}{sL_4}(I_3' - I_5') \tag{2.12d}$$

$$I_5' = \frac{1}{sC_5}(I_4 - I_5) \tag{2.12e}$$

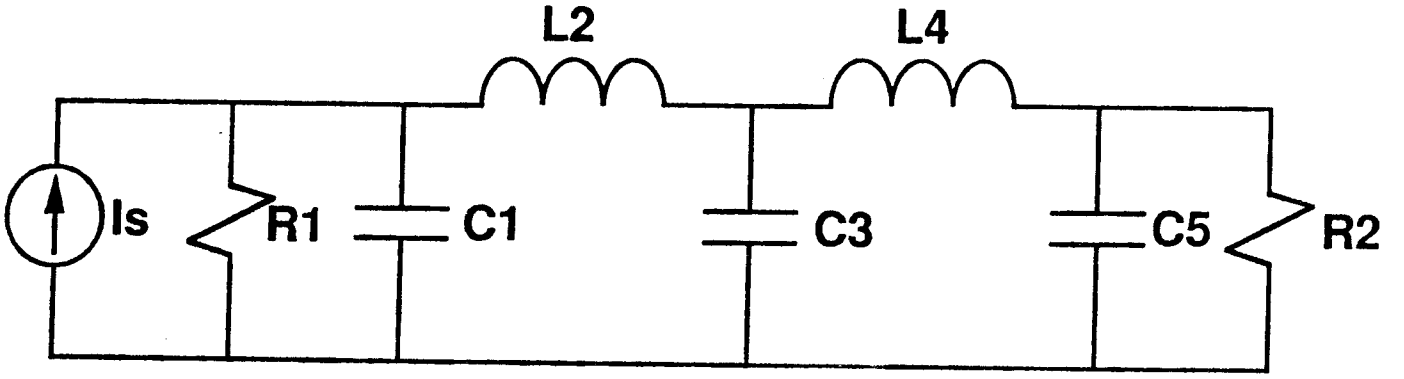


Fig. 2.6(a) Doubly-terminated LC lowpass prototype for the fifth-order filter.

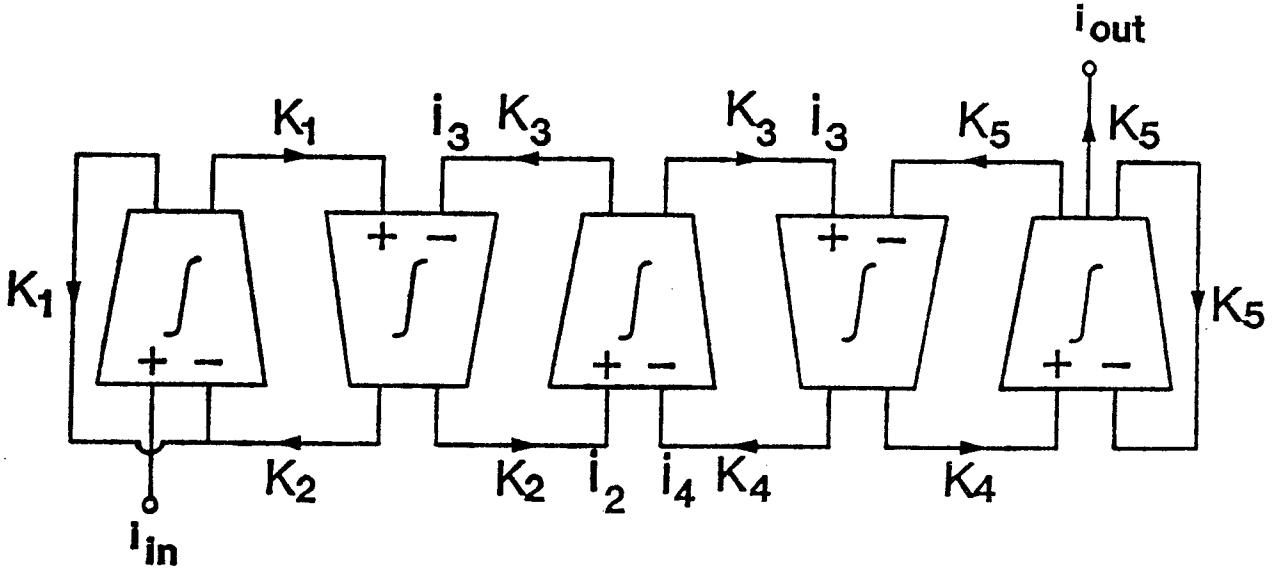


Fig. 2.6(b) A schematic of a five-pole lowpass SI filter.

The integrator scale factors, K_i, are determined by:

$$K_i = \frac{\omega_{co}}{f_s X_i} = \frac{C_U}{C_I} \tag{2.13}$$

where, X_i represents the component value of that branch, ω_{co} is the filter cutoff frequency, and f_s is the sampling frequency.

The one-to-one correspondence of the transistor ratio to the capacitor ratio (C_U/C_I) allows for the extension of the SC ladder filter synthesis to the synthesis of SI ladder filters. The symbolic representation of the fifth-order lowpass SI ladder filter is shown for the expressions presented above, Fig. 2.6(b). Although the input and output signal medium is current, the symbolic representation is analogous to the SC representation. The termination loops around the first and last integrators correspond to the terminating resistors in the doubly-terminated LC prototype. Currents are summed by the connection of the wires at the input of the integrators, and multiple output currents are generated for each output required. K_1 through K_5 represent the integrator scale factors obtained from Eqn. (2.13).

In addition to all-pole filters, SI techniques can also be employed in the design of ladder filters with transmission zeros. The doubly-terminated LC prototype for the third-order lowpass elliptic filter and the transformed prototype are shown in Figs. 2.7(a),(b), respectively. In the SC elliptic filter signal flowgraph synthesis, the resonator capacitance is transformed using a Thevenin equivalent. The resonant series capacitor is transformed to a branch to ground consisting of a series capacitance and scaled voltage source. In the SI filter signal flowgraph synthesis, a Norton transformation is used to represent the resonant capacitance as parallel

branches consisting of a capacitor and scaled current source to ground. The symbolic representation of the SI elliptic filter is shown in Fig. 2.7(c). S1 and S3 represent the currents summed in parallel i.e. the resonant loop. Although the third integrator has five current outputs, the die area required for implementation in CMOS is not excessive because the coefficients are typically of the order of 0.1.

Once the filter design is complete, it is necessary to scale each output for maximum dynamic range. An SC filter is scaled for maximum dynamic range by scaling the peak output voltage of each stage relative to the total power supply voltage. Node voltage scaling is often used to independently adjust all peak output voltages to be equal. By analogy, the maximum dynamic range of SI filters is determined by the ratio of the peak output signal current relative to the DC bias current of that stage. To equalize this ratio for each stage, either the signal current and/or the DC bias current can be scaled.

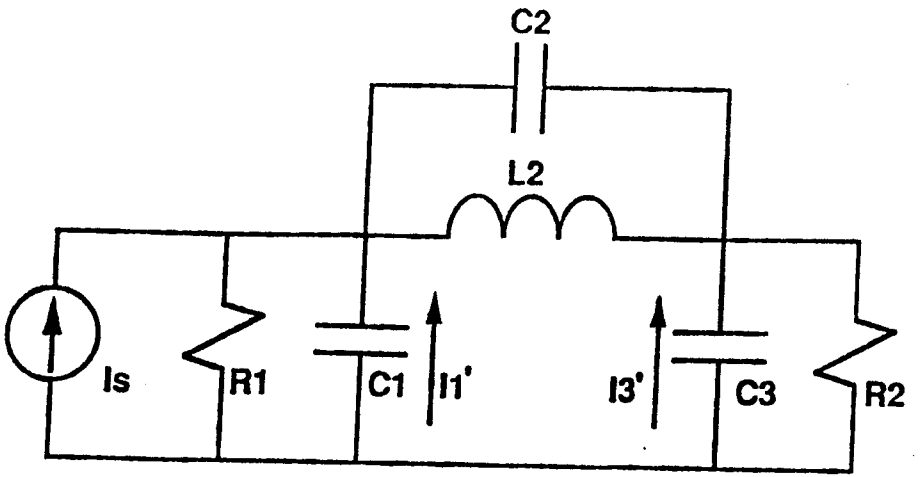
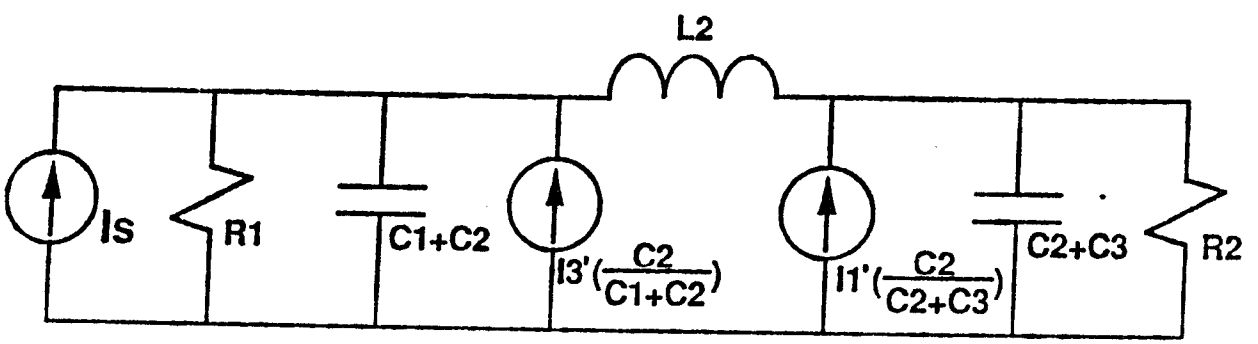


Fig. 2.7(a) Doubly-terminated LC lowpass prototype for the third-order Elliptic filter.



(b) Transformed RLC prototype.

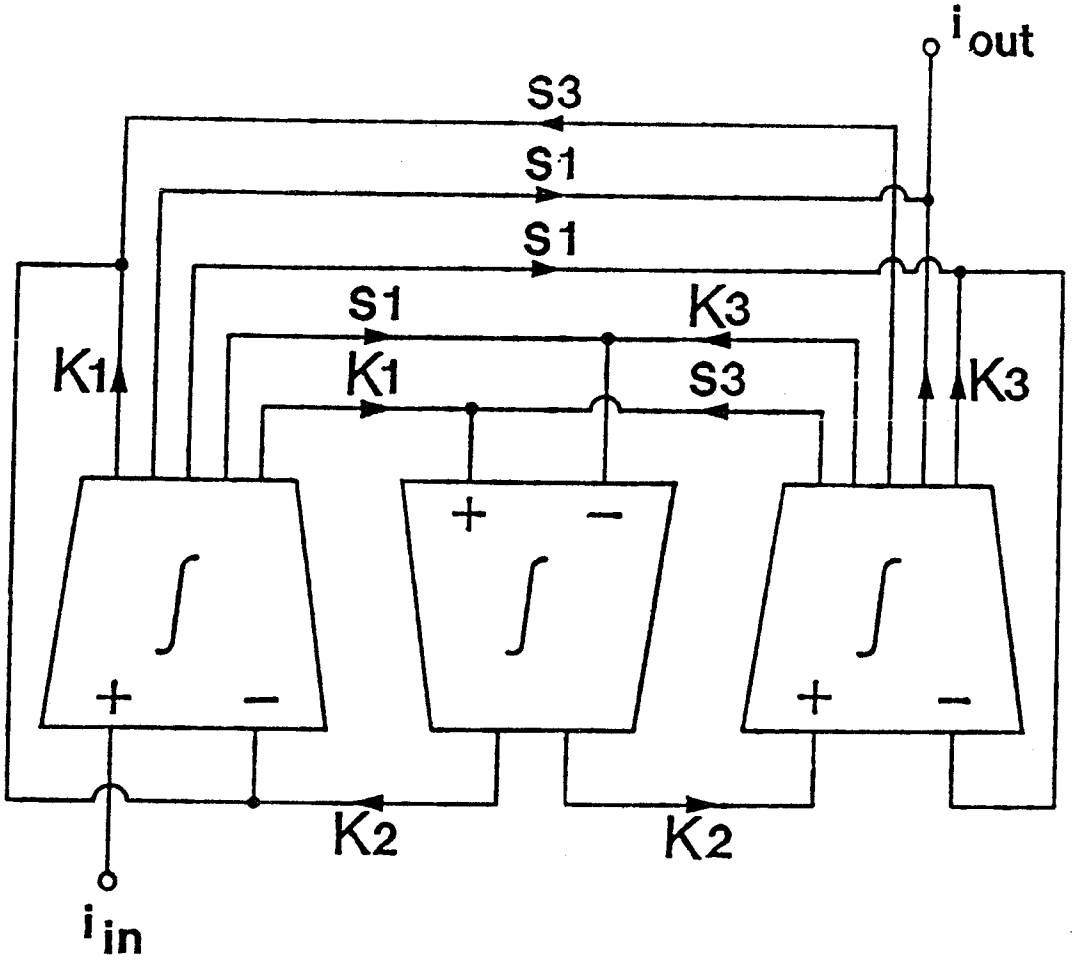


Fig. 2.7(c) A schematic of a three-pole lowpass Elliptic SI filter.

2.5 Synthesis of SI Biquadratic Filters

Another filter configuration that is useful in many applications is the biquadratic filter. The universal biquadratic filter is an especially versatile filter building block [12]. It can be used to generate all types of filter responses with the same general structure. The general biquadratic transfer function is:

$$\frac{v_o}{v_i} = \frac{Q + Uz^{-1} + Zz^{-2}}{1 + Az^{-1} + Bz^{-2}} \tag{2.14}$$

By choosing appropriate numerator coefficients, different filter types such as lowpass, highpass and bandpass can be derived. The Fleischer-Laker SC biquad [13] is shown in Fig. 2.8. The bilinear transformation is used to transform the universal biquad continuous-time transfer function into the discrete-time transfer function. Below is a simplified SC biquad transfer function where the letters represent the capacitor values in Fig. 2.8:

$$T = \frac{v_o}{v_i} = \frac{I + (G\text{-}I\text{-}J)\, z^{-1} + (J\text{-}H)\, z^{-2}}{1 + (C+E\text{-}2)z^{-1} + (1\text{-}E)\, z^{-2}} \tag{2.15}$$

The desired SC filter can now be implemented starting with the correct universal transfer function, then deriving the SC transfer function and finally choosing the capacitor values to meet these requirements.

The same procedure can be used for the SI biquadratic filter design. The transfer function is transformed from voltage to current by scaling the numerator and denominator of Eqn. (2.15) by R_s. By setting $R_s=1$, the transfer function of

i_{out}/i_{in} is equivalent to v_{out}/v_{in}. Thus, the capacitor ratios directly map to current mirror ratios in the SI integrator.

Once the filter design is complete, it is necessary to scale for maximum dynamic range. For each of the biquad filters, the signal current was scaled relative to the DC bias current. This requires only that the scale factor K of each integrator be multiplied by the dynamic range scale factor. A generalized schematic of the SI biquadratic filter with current mirror ratios and dynamic range scale factors are shown in Fig. 2.9.

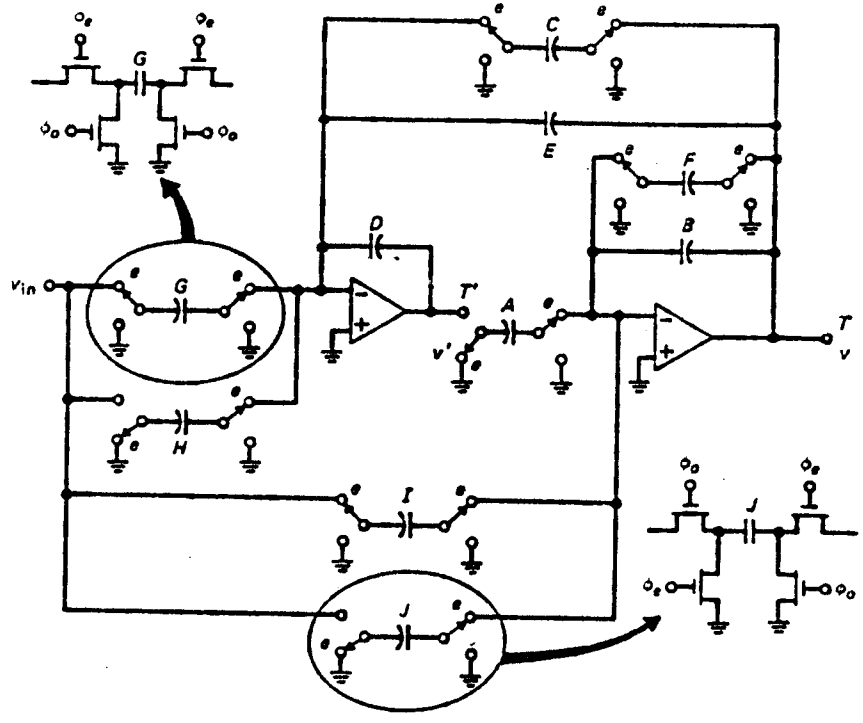


Fig. 2.8 General Fleischer-Laker SC biquadratic filter from [12].

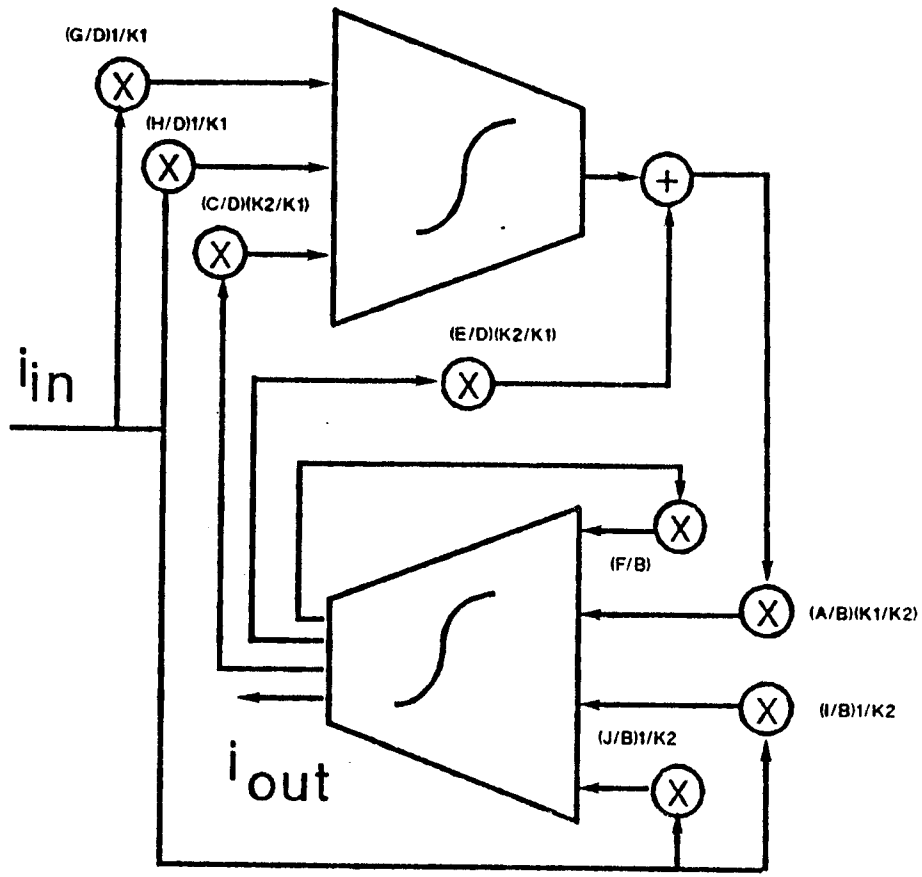


Fig. 2.9 General switched-current biquadratic filter. K1 and K2 represent the dynamic range scaling factors. Alpha charactor factors represent current mirror ratios used to scale signal currents.

2.6 Practical Design Considerations

SI ladder filters and biquadratic filters are composed of scaled differential SI integrators. As presented above, the SI integrator is composed of two cascaded current-mode track-and-hold circuits. Thus, the performance of SI ladder filters is determined by the accuracy of the current-mode T/H function. In this section, the nonidealities in switched-current filters will be presented.

2.6.1. The Effects of Gain Errors on the SI Filter Response

The SI differential integrator of Fig. 2.4 is re-evaluated with T/H gains, A_1 and A_2, included in the integrator output expression:

$$i_{out}(z)_{nonideal} = \frac{(KA_I)\, i_1\, z^{-1} - (KA_2)\, i_2\, z^{-1/2}}{(1 - A_I\, z^{-1})} \tag{2.16}$$

where, $A_I = A_1 \cdot A_2$ is the integrator gain in the forward path.

The current gains, A_1 and A_2, account for gain errors in the T/H amplifier. In the ideal SI integrator, the current gains, A_1, A_2 and A_I all equal one. Nonideal current gains have two effects on the integrator output that, in turn, affect the filter performance: integrator coefficient errors and integrator quality factor, Q, errors. The integrator coefficient errors are a result of K, the ideal integrator scale factor, being scaled by the T/H current gains. The effective integrator coefficients are (KA_I) and (KA_2) for the inverting and noninverting inputs, respectively. The effect of the integrator coefficient errors on the SI ladder filter performance is minimized by using a doubly-terminated LC prototype. These structures have minimum sensitivity to component variations, or as in this case, minimum sensitivity to integrator coefficient errors provided Lossless Discrete Integration (LDI) clock phasing is employed in the filter [14].

Gain errors in the numerator of $i_{out}(z)_{nonideal}$ determine the integrator coefficient errors; similarly, gain errors in the denominator of $i_{out}(z)_{nonideal}$ determine the integrator Q-errors. The integrator Q is:

$$Q = \frac{Im(D)}{Re(D)} \tag{2.17}$$

where, D is the denominator of Eqn. (2.16).

The SI integrator quality factor is evaluated by considering the half-delay integrator. The clock phasing errors are excluded by using LDI clocking so only the errors due to integrator gain errors are examined. The SI integrator Q is:

$$Q_{SI} = \frac{1+A_I}{1-A_I} \tan\left(\frac{\omega_{co}T}{2}\right) \tag{2.18}$$

where, $\omega_{co}T$ is the filter cutoff frequency divided by the sampling frequency.

An integrator gain value, A_I, of one produces an infinite integrator quality factor and therefore, the integrator performs an ideal discrete-time integration. However, if A_I is greater or less than one, the integrator has integrator Q errors. To illustrate the effect of integrator gain errors on the overall filter frequency response, a fifth-order filter with various integrator gains has been simulated, Fig. 2.10. For $A_I<1$, the integrator is lossy and the filter response exhibits droop. While for $A_I>1$, the integrator output is gain enhanced and there is peaking in the filter frequency response. For AI not equal to its ideal value of one, reducing the f_s/f_{co} ratio increases Q_{SI}. However, reducing the f_s/f_{co} ratio requires tighter design specifications on the anti-aliasing filter.

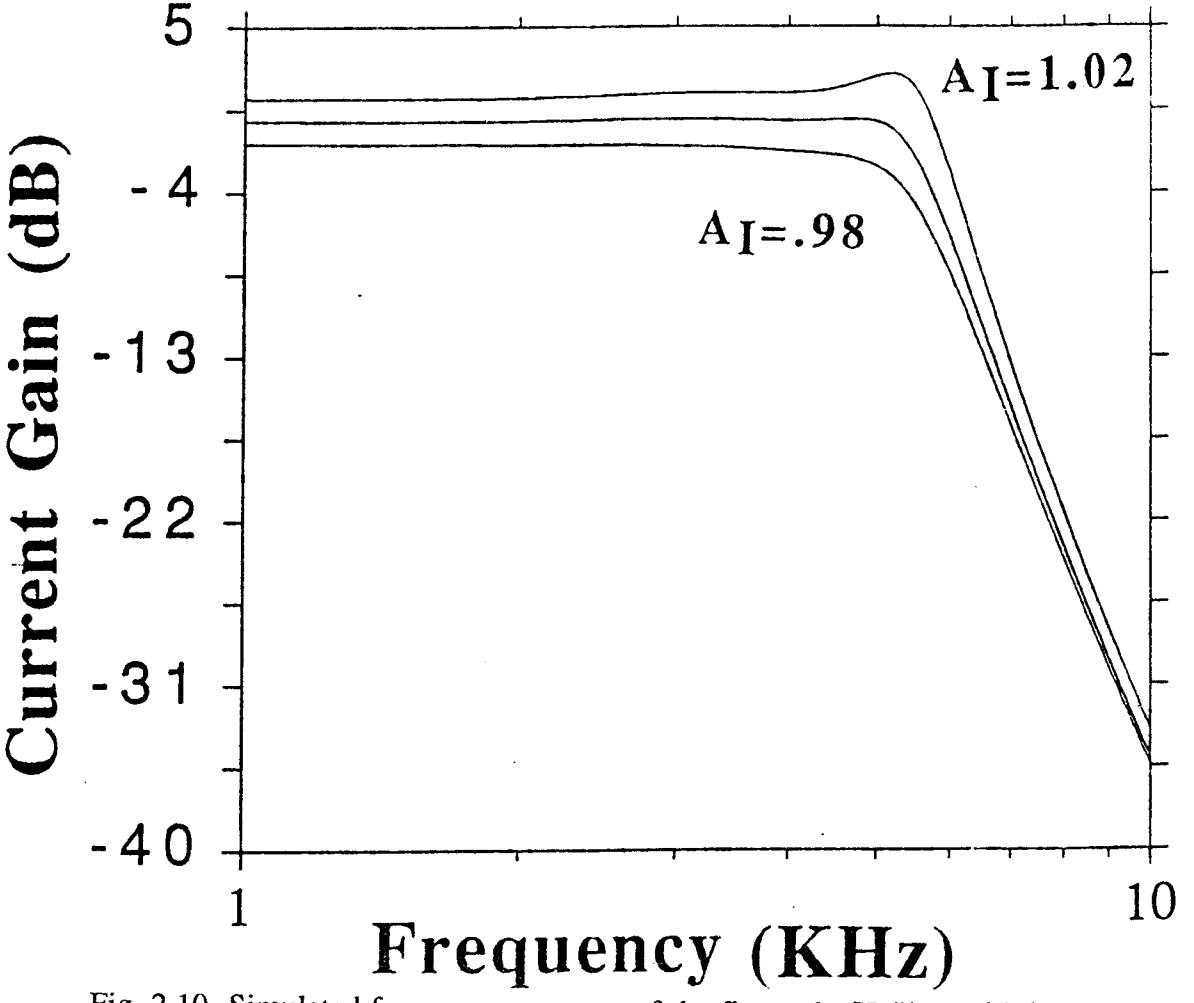


Fig. 2.10 Simulated frequency response of the five-pole SI filter with integrator gain, A_I, errors.

2.6.2. Sources of SI Gain Errors

In this section, the two sources of distortion in the current T/H are examined:

(1) process mismatches between the current mirror transistors and,

(2) switch clock-feedthrough effects.

The simple current mirror will first be analyzed to determine the effects of process mismatches between the current mirror transistors on the output current. Then, the clock-feedthrough effects in the current T/H will be evaluated.

In the simple current mirror, Fig. 2.1, mismatches in the transistor parameters of threshold voltage, V_t, device aspect ratio, (W/L), transconductance parameter, K', and the channel-length modulation parameter, λ, cause errors in the output current [15,16]. First, the current distortion caused by only threshold voltage mismatches is considered, that is, $\Delta V_t = V_{t1} - V_{t2}$. Assume M_1 and M_2 are identical except for the threshold voltage mismatch. The output current, i_{out}, is ideally identical to the signal current, i. The expression for the output current with threshold voltage mismatch between the current mirror transistors is:

$$i_{out} = i + \frac{2\,\Delta V_t\, I}{(V_{GS_1} - V_{t1})}\sqrt{\left(1 + \frac{i}{I}\right)} + \frac{\beta}{2}\Delta V_t^2 \qquad (2.19)$$

where $\beta = K'(W/L)$.

We define,

$$V_{GS_1} + V_{gs_1} = V_{t1} + \left[\frac{2(I+i)}{K'(W/L)}\right]^{1/2}. \qquad (2.20)$$

Substituting Eqn. (2.20) into Eqn. (2.19) and applying the binomial expansion, the terms for the output current are:

$$i_{out,\,DC} = \frac{\beta}{2}\Delta V_t^{\,2} + \frac{2\,\Delta V_t\, I}{(V_{GS_1} - V_{t_1})} \tag{2.21a}$$

$$i_{out,\,AC} = i\left[1 + \frac{\Delta V_t}{(V_{GS_1} - V_{t_1})}\right] +$$

$$\frac{2\,\Delta V_t\, I}{(V_{GS_1} - V_{t_1})}\left[-\frac{1}{8}\left(\frac{i}{I}\right)^2 + \frac{1}{16}\left(\frac{i}{I}\right)^3 - \frac{5}{128}\left(\frac{i}{I}\right)^4 + \ldots\right] \tag{2.21b}$$

It is seen from Eqn. (2.21) that threshold voltage mismatch in the current mirror transistors distorts the output current. The current is separated into a DC term, Eqn. (2.21a), and an AC polynomial term, Eqn. (2.21b). In the presence of threshold voltage mismatch, DC offset current, AC gain error and harmonic distortion are introduced. The DC offset shifts the bias point as indicated by the $i_{out,DC}$ term, Eqn. (2.21a). The magnitude of the AC gain error and harmonic distortion are determined by the $i_{out,AC}$ term. The harmonic distortion is a strong function of the signal current to bias current ratio, (i/I), and therefore, harmonic distortion is minimized by reducing the (i/I) ratio. The DC offset and AC gain error distortion due to threshold voltage mismatch are summarized in Table 2.1. For ΔV_t=10 mV, the gain error is 2.5% and the DC offset is 5% (where, $(W/L)_1=(W/L)_2$=100 μm/10 μm, and $V_{GS}-V_t$=500 mV). Using a similar analysis, the effect of mismatches in W, L, K' and λ are also computed. The results are also summarized in Table 2.1. Mismatches in these parameters do not introduce harmonic distortion, they only contribute to DC offset and AC gain error.

The device mismatch distortion analysis performed above for the simple current mirror also applies directly to the current T/H. In addition to process mismatch induced errors, the T/H also has switch clock-feedthrough voltage distortion.

Clock-feedthrough effects in the current track-and-hold, Fig. 2.2, are due to the nonideal characteristics of the switch transistor, Ms. During the switch turnoff period, the finite drain-source resistance in conduction and the gate-drain overlap capacitance in cutoff enable charge to be injected onto the data holding node. As the gate voltage decreases, but is still greater than the switch threshold voltage, the channel conductance also decreases. The excess channel charge exits through the source and drain terminals of the switch transistor to the gate capacitances of M_1 and M_2. Once the switch is nonconducting, the channel no longer exists. The coupling of the switch gate-drain overlap capacitance to the gate capacitance of transistor, M_2, provides a path for charge injection onto the data holding node [17-20]. The combination of these two sources of charge injection produces errors in the voltage held on the gate capacitance of M2. The amount of injected charge, and therefore, the error voltage held on the data holding node is a function of the switch turn-off rate, the aspect ratio of Ms to M_2, the source to load capacitance ratio and the switch to source resistance ratio.

The switch charge injection creates an error voltage on the data holding node. This voltage causes, to a first order, the same distortion as threshold voltage mismatch in the current mirror transistors. A graph of the total harmonic distortion,

TABLE 2.1 Distortion due to device mismatch in the simple current mirror.

Parameter	DC Offset	AC Gain Error
$\Delta V_t=V_{t1}-V_{t2}$	$2\Delta V_t/(V_{GS}-V_t)$	$\Delta V_t/(V_{GS}-V_t)$
$\Delta W=W_1-W_2$	$\Delta W/W$	$\Delta W/W$
$\Delta L=L_1-L_2$	$-\Delta L/L$	$-\Delta L/L$
$\Delta K'=K'_1-K'_2$	$\Delta K'/K'$	$\Delta K'/K'$

THD, of the clock-feedthrough voltage plus the threshold voltage mismatch versus the excess DC voltage, (V_{GS1}-V_{t1}), is shown in Fig. 2.11. The THD is greatly reduced as i/I is reduced. For a threshold voltage mismatch plus clock-feedthrough voltage of 30 mV, the THD is −58 dB with i/I=0.5. Reducing the i/I ratio to 0.1 for the same bias current level reduces the THD to -72 dB.

Harmonic distortion can be more severe in SI than SC circuits. In SI circuits, the current is proportional to (V_{GS}-V_t)^2. Hence, clock-feedthrough and threshold voltage mismatch produce square-law current that contributes directly to harmonic distortion.

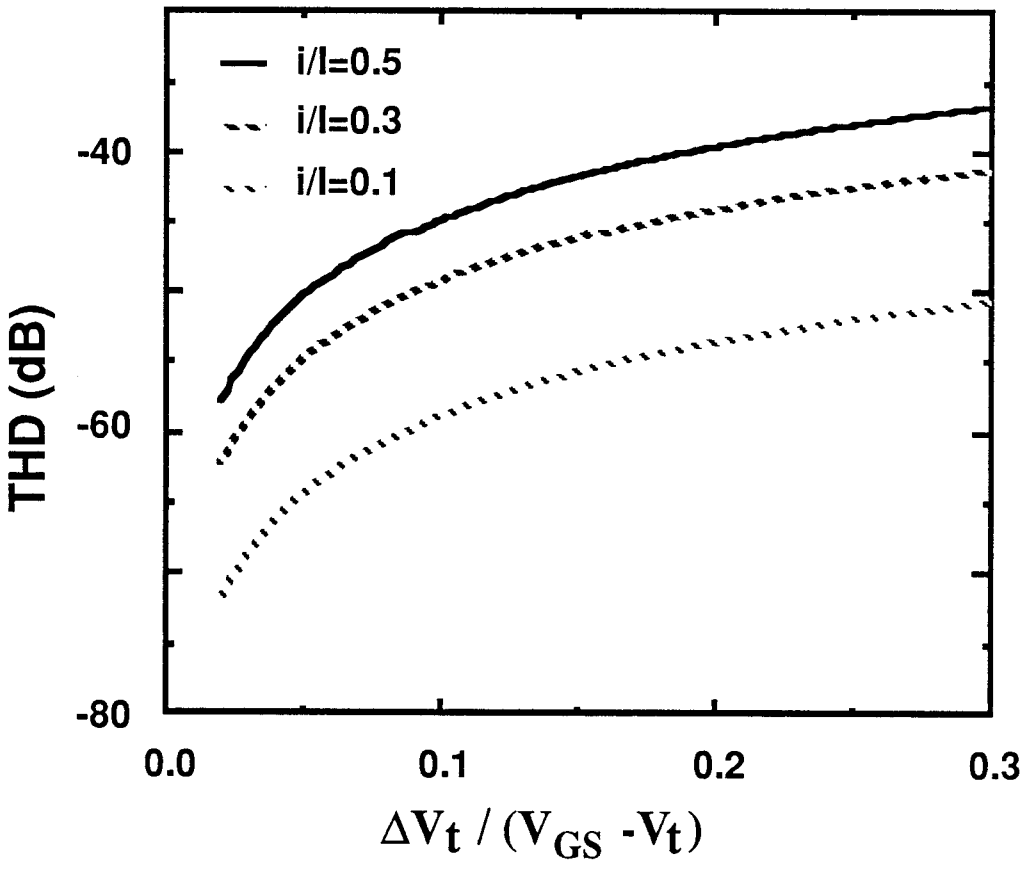


Fig. 2.11 Plot of total harmonic distortion for increasing i/I ratios (ΔV is the sum of the threshold voltage mismatch plus the clock-feedthrough voltage.)

2.6.3. Finite Impedance Effects

In Section 2.2, the summation of the currents at the diode-connected input of the current amplifier was described. This description did not include the effects of the finite output impedance of the input current source. The finite output impedance of the input current source loads the input of the SI current amplifier causing a change in the current summed at the input. In Fig. 2.12, the input conductance of the current amplifier is g_{in} (g_{m3}) and the output conductance of the input signal current source is g_{out} (g_{ds2}). Consider that voltage change at the input to the current amplifier is ΔV and thus,

$$\Delta V = \frac{i}{g_{in}} \ . \tag{2.22}$$

Assuming that the current amplifier has a gain of one, the change in it's output current is:

$$\Delta i = \Delta V \ g_{out}. \tag{2.23}$$

Substituting into Eqn. (2.22), the change in the desired output current is:

$$\Delta i = i \ (\frac{g_{out}}{g_{in}}). \tag{2.24}$$

For the current amplifier of Fig. 2.11, the g_{out}/g_{in} ratio is approximately g_{ds2}/g_{m3} or of the order of 1/100. This results in a 1% gain error. Therefore, to reduce the error in the output signal current due to loading effects, a high input to output conductance ratio is desirable. This is achieved by using a high performance current source such as a cascode or a high-swing cascode current source where the

input to output conductance ratio is typically 10,000 and the resulting gain error is less than 0.01%.

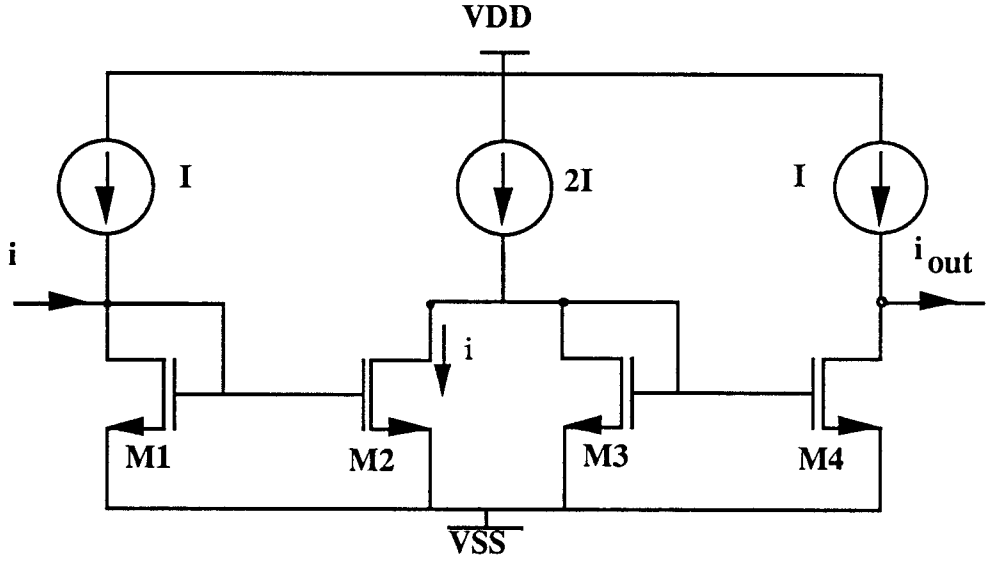


Fig. 2.12 Cascaded simple current mirrors illustrating the effects of finite output impedance.

2.7 Experimental Results

A fifth-order lowpass Chebychev SI filter was fabricated using a 2-μm N-well standard digital CMOS process. The die microphotograph is shown in Fig. 2.13. High-swing cascode current sources are used throughout the filter, Fig. 2.14. The integrator core transistors are all 100 μ/10 μ. A unit cell layout was used with the current mirror transistors segmented into ten 10μ/10μ smaller transistors. The top row of transistors in Fig. 2.13 are p-channel high-swing cascode current mirror transistors and the next row are n-channel high-swing cascode current mirror transistors. There are 5 rows of these pairs with each row representing one pole of the filter.

Signal flowgraph synthesis was used to obtain the integrator scaling factors and the symbolic representation was previously shown in Fig. 2.6(b). The SI ladder filter was designed for 0.1 dB ripple bandwidth and a cutoff frequency of 5 kHz with a sampling frequency of 128 kHz. The measured magnitude response and a table of results are shown in Fig. 2.15 and Table 2.2, respectively.

All the measured parts were virtually identical; however, the measured cutoff frequency was approximately 20% less than the designed value. When the clock-feedthrough voltage effects on gain were considered, the simulated results agreed very closely with the experimentally measured results. The filter area was approximately 200 mil^2 per pole. The noise is comparable to the noise in SC filters with the equivalent input-referred noise voltage of 133 $nV/\sqrt{Hz}$. The dynamic range is greater than 12 bits in the filter bandwidth and the filter power dissipation is approximately 1 mW/pole.

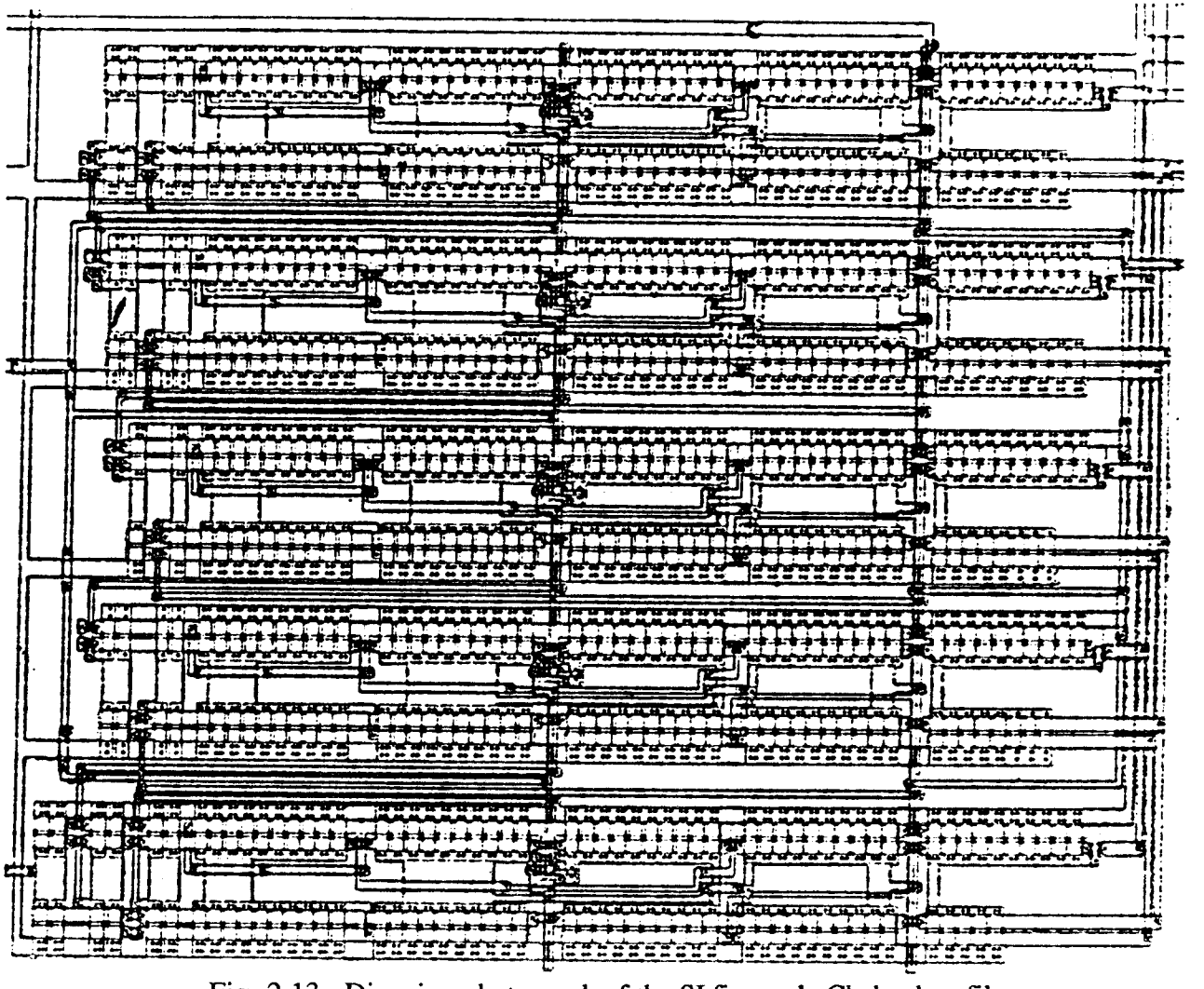


Fig. 2.13 Die microphotograph of the SI five-pole Chebychev filter.

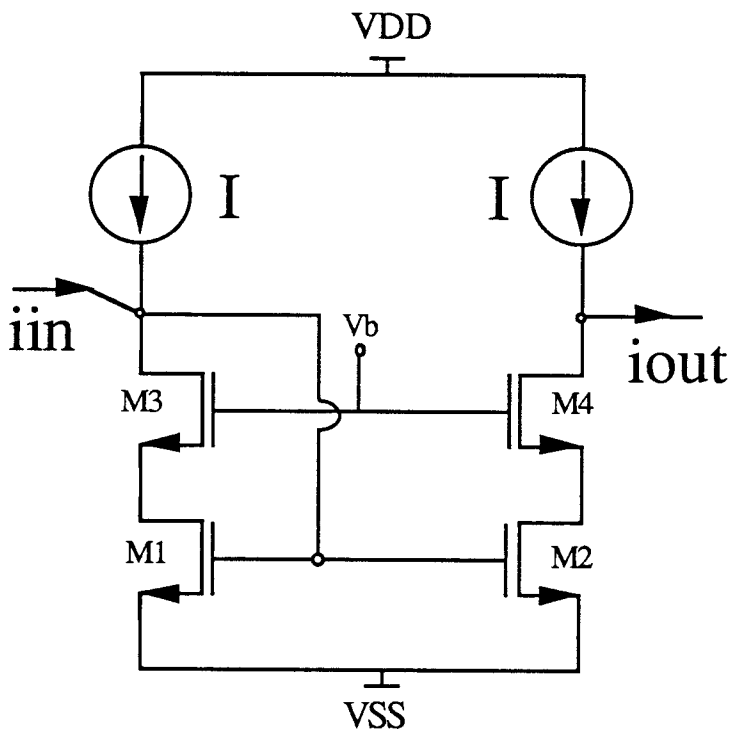


Fig. 2.14 High-swing cascode current mirror.

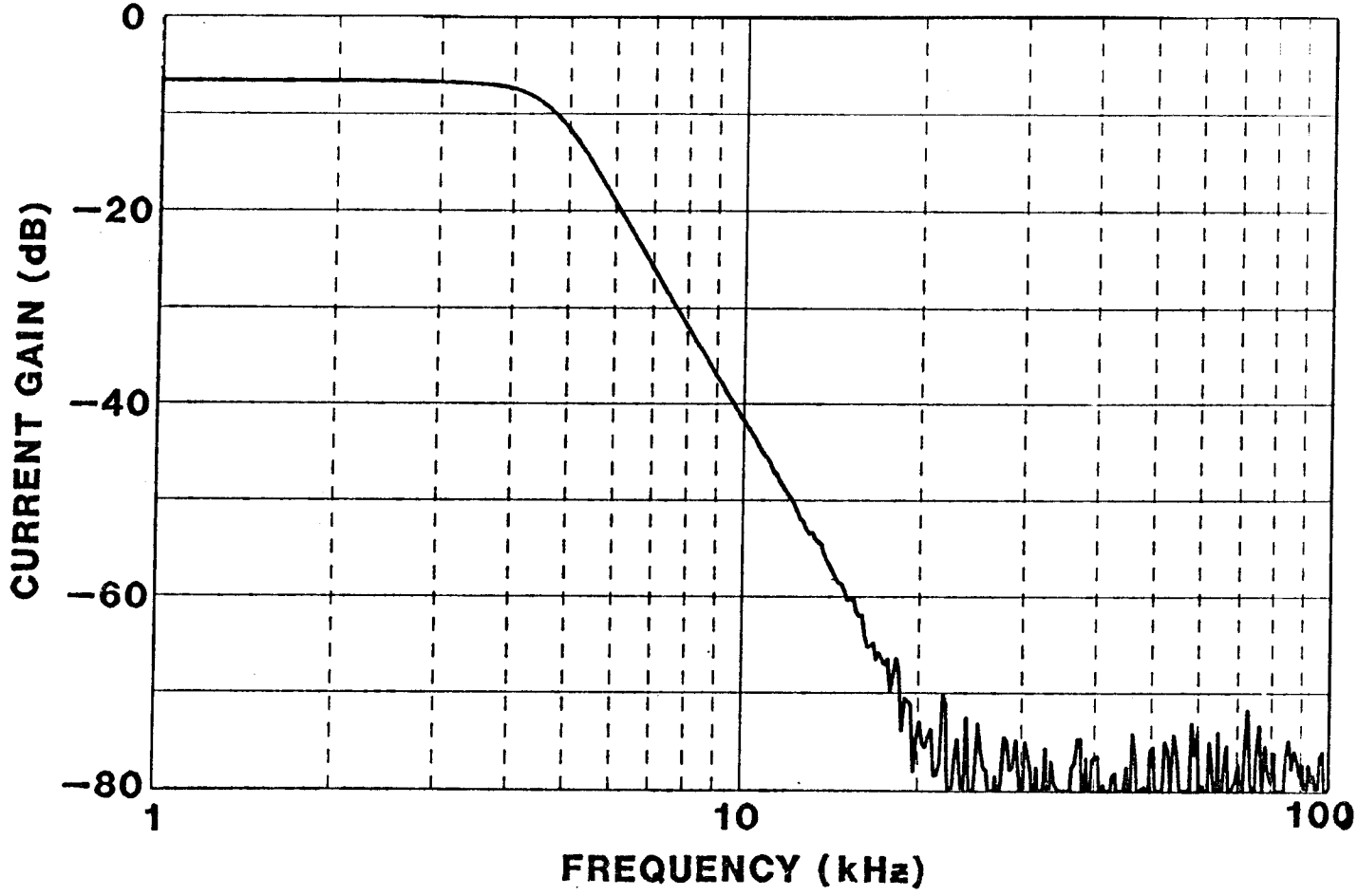


Fig. 2.15 Measured frequency response of the five-pole SI filter.

TABLE 2.2 Measured results of the five-pole SI filter.

Clock Frequency	128 kHz
3 dB Bandwidth	4.7 kHz
RMS Noise (300-4.7 kHz)	4.1 nA_{RMS}
(300-64 kHz)	6 nA_{RMS}
Dynamic Range (300-4.7 kHz)	72.6 dB
(300-64 kHz)	69.3 dB
Power Dissipation	5 mW
Filter Die Area	1 x 0.75 mm^2

A third-order Elliptic SI filter was also fabricated with the measured gain response and table of results shown in Fig. 2.16 and Table 2.3, respectively. This 3-pole, 2-zero SI filter demonstrates the feasibility of using the SI technique for ladder filters with zeros of transmission.

Using the design techniques presented above, several switched-current biquadratic filters have also been designed and fabricated. For each of the filters fabricated, high-swing cascode current sources were also used. The transistors were segmented into unit cells to reduce the effect of systematic errors, however no common centroid layout techniques were employed. Figure 2.17 is the measured frequency response for the biquadratic lowpass filter where the general form of the numerator polynomial is Kz^{-2}. The sample frequency is *50 kHz* and the designed *3 dB* bandwidth is *2.5 kHz*. The measured frequency response does not exactly match the ideal response. However, when the effects of clock-feedthrough on the current amplifier gain is taken into account, the response agrees closely with the simulated response.

The measured frequency responses for another biquadratic lowpass filters is shown in Fig. 2.18. Again, the simulated response with the clock-feedthrough gain error included agrees very closely with the measured results.

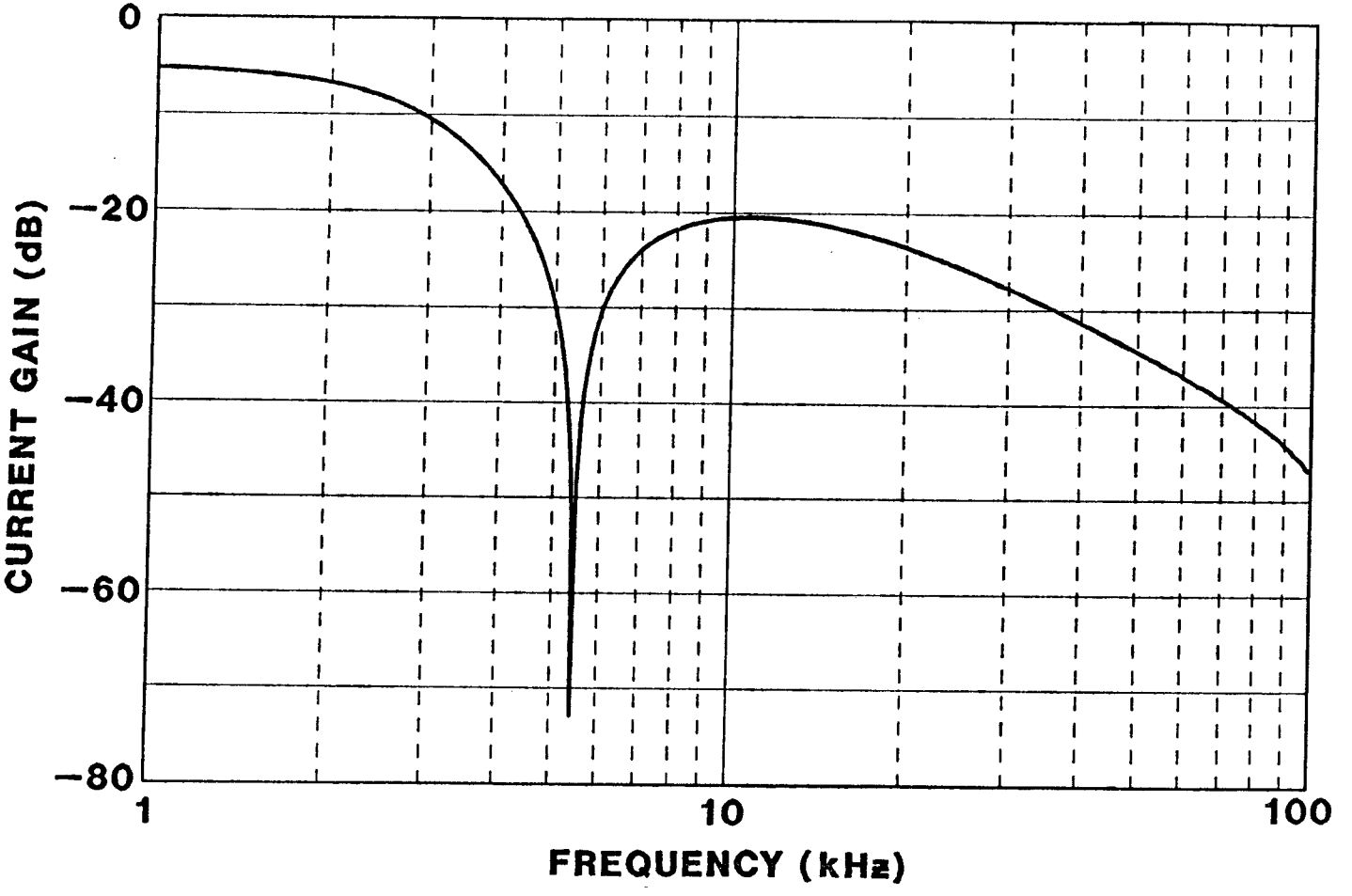


Fig. 2.16 Measured frequency response of the three-pole Elliptic SI filter.

TABLE 2.3 Measured results of the three-pole SI filter.

Clock Frequency	128 kHz
3 dB Bandwidth	2.9 kHz
RMS Noise (300-2.9 kHz)	1.7 nA_{RMS}
(300-64 kHz)	4.8 nA_{RMS}
Dynamic Range (300-2.9 kHz)	80.3 dB
(300-64 kHz)	71.3 dB
Power Dissipation	3 mW
Filter Die Area	1050 mil^2

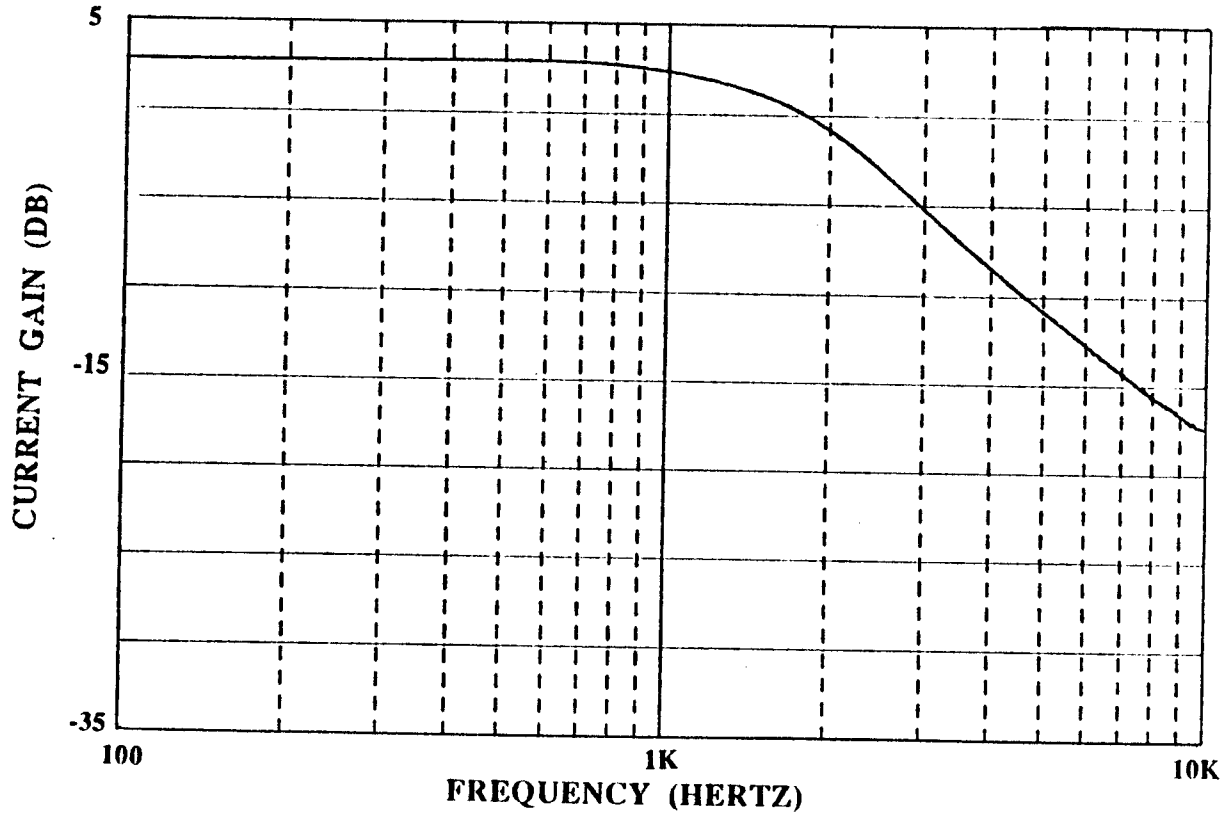


Fig. 2.17 Biquadratic lowpass filter measured frequency response with numerator polynomial of Kz^{-2} (f_s=50kHz, designed f_c=2.5kHz).

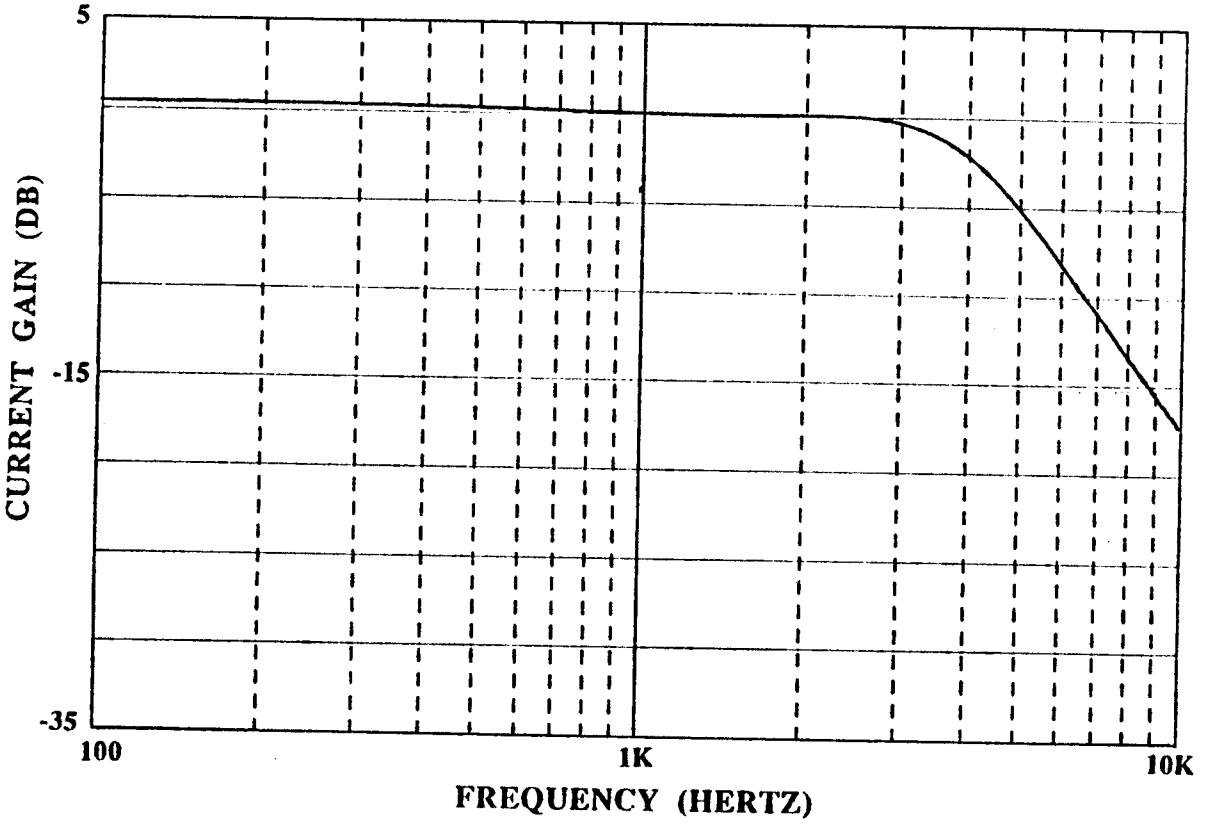


Fig. 2.18 Biquadratic lowpass filter measured frequency response with numerator polynomial of $K(1+z^{-1})^2$ (bilinear transformation), (f_s=25kHz, designed f_c=5kHz).

2.8 Conclusion

The first integrated CMOS SI filter results have been described. The SI filter synthesis leverages the previously developed SC filter synthesis techniques. The measured frequency responses were virtually identical from part to part. However, the measured response was in error due to clock-feedthrough voltages and current mirror transistor device mismatches. Clock-feedthrough and device mismatch induced errors are more severe in the present SI circuit configurations than in SC circuits. Future work will be concentrated on resolving these limitations. Current copier schemes have been proposed to eliminate device mismatch effects in SI circuits [21]. This technique in combination with reduction of the clock-feedthrough errors could make the SI approach very accurate.

CHAPTER 3

DETERMINATION OF DYNAMIC RANGE IN SI FILTERS

3.1 Abstract

The factors that influence the dynamic range in SI filters are presented. The sources of harmonic distortion in current-mode circuits are characterized and the relationships to maximum signal size are established. Using noise measurements, the dynamic range in SI filters is obtained.

3.2 Introduction

Dynamic range in analog circuits is a measure of the range of signal resolution. In an analog system, 6 dB of dynamic range is equivalent to 1 bit of resolution in a digital system. For example, in digital audio systems, the dynamic range is typically 90 dB or equivalently, 15 bits. Dynamic range is defined as the maximum RMS signal amplitude for a given level of total harmonic distortion (THD) divided by the RMS value of the minimum detectable signal (MDS). The MDS is equal to the input-referred total RMS noise within a specified bandwidth.

In this chapter, the dynamic range of SI circuits is examined. In section 3.3 and 3.4, the sources of distortion that limit the maximum signal size are presented. A current clock-feedthrough cancellation technique is introduced in section 3.5. The input referred-noise of current-mode circuits is examined to evaluate the minimum detectable signal size . Measurements from integrated SI filters are given and the dynamic range of the SI filters is determined in section 3.6.

3.3 Distortion in the Simple Current Mirror

Switched-current circuits use a switched current mirror as the basic building block. Although the current mirror itself has been commonly used in voltage-domain signal processing circuits (e.g. op amps) [22, 23], its current distortion characteristics, which are important for SI circuits, have not been investigated. Understanding the sources of distortion in the switched current mirror is essential to the design of low power, wide dynamic range SI circuits. In this section, analysis of the distortion due to device mismatches in a simple current mirror is performed. Next, in section 3.4, the clock-feedthrough distortion effects in the switched current mirror are analyzed.

In the simple current mirror circuit, Fig. (3.1), the output AC signal current, i_{out}, is distorted relative to the input AC signal current, i_{in}, due to mismatches in the transistor threshold voltage, V_t, device aspect ratio, (W/L), transconductance parameter, k', the channel-length modulation parameter, λ, and the field-dependent mobility degradation, Θ, [24,25]. The general expression for the current in the MOS transistor is:

$$I_{ds} = \frac{k'/2}{1+\Theta(V_{gs}-V_t)} (W/L) (V_{gs}-V_t)^2(1+\lambda V_{ds}) . \qquad (3.1)$$

First, the current distortion caused by V_t mismatches (neglecting all other mismatches) is considered, that is, $\Delta V_t = V_{t1} - V_{t2}$. Assume M_1 and M_2 are identical except for the threshold voltage mismatch. The drain current of M_2, I_2, is ideally identical to the drain current of M_1, I_1, where I_1 is equal to the DC bias current, I, plus the AC signal current, i_{in}. The expression for the current in M_2 is:

$$I_{ds_2} = (k'/2)(W/L)_2 (V_{gs_2}-V_{t_2})^2 \tag{3.2}$$

where, $V_{gs_1} = V_{gs_2}$ and:

$$V_{gs_1}=V_{t_1} + \left[\frac{2(I+i_{in})}{k'(W/L)}\right]^{1/2} \tag{3.3}$$

substituting Eqn. (3.3) into (3.2) and applying the binomial expansion, the expression for i_{out} with threshold mismatch between M_1 and M_2 is:

$$i_{out} = I\left[\frac{2\Delta V_t}{V_{gs}-V_{t_1}} + \left(\frac{\Delta V_t}{V_{gs}-V_{t_1}}\right)^2\right] +$$

$$\left[i_{in}\left(1 + \frac{\Delta V_t}{V_{gs}-V_{t_1}}\right) + \frac{2\Delta V_t}{V_{gs}-V_{t_1}}\left[-\frac{(i/I)^2}{8} + \frac{(i/I)^3}{16} - \frac{5(i/I)^4}{128} \ldots\right]\right] \tag{3.4}$$

It is seen from Eqn. (3.4) that threshold voltage mismatch in the simple current mirror transistors distorts the output current. The current is separated into a DC term (top line of Eqn. (3.4)) and an AC polynomial term (second line of Eqn. (3.4)). The total ΔV_t DC offset is the sum of the DC term in Eqn. (3.4) and the DC offset caused by the even harmonics. The offset causes a DC level shift in the AC signal current. The AC polynomial term introduces both AC gain error (first term in bottom line) and harmonic distortion. The AC gain error compresses or expands the AC signal and is produced by the odd harmonics of Eqn. (3.4). The form of the threshold voltage mismatch AC gain error is shown in Table 3.1. By evaluating the AC polynomial term in Eqn. (3.4), the total harmonic distortion due to threshold voltage mismatch is typically dominated by second-harmonic distortion and is therefore approximately:

$$\mathrm{THD}(\Delta V_t) \sim -\frac{1}{8}\frac{\Delta V_t}{V_{gs}-V_{t_1}}\frac{i}{I} \tag{3.5}$$

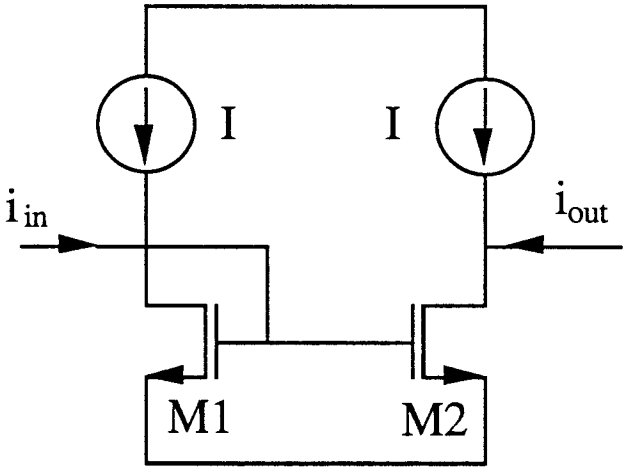


Fig. 3.1 Simple current mirror with DC bias current I and AC signal current i_{in}.

A plot of the total harmonic distortion versus normalized threshold mismatch is shown in Fig. 3.2. For a typical threshold voltage mismatch of *10 mV* and V_{GS}–V_{t_1} of *500 mV*, a THD level of - *58 dB* is achieved for an *i/I* current ratio of *0.5*. Reducing the *i/I* current ratio from 0.5 to 0.1 decreases the THD level to -*72 dB*.

A similar analysis to that performed above may be used to evaluate the effects of mismatches in *W, L, k'*, λV_{DS} and Θ. The results are also summarized in Table 3.1. Mismatch in any one of these terms introduces DC offset and AC gain error, but no harmonic distortion is produced. These parameters typically vary by 10% across the wafer.

TABLE 3.1 Distortion of output current (Fig. 3.1) due to W, L, k', λV_{DS} and Θ mismatches.

Parameter	DC Offset	AC Gain Error
$\Delta V_t = V_{t1} - V_{t2}$	$2\Delta V_t/(V_{GS}-V_t)$	$\Delta V_t/(V_{GS}-V_t)$
$\Delta W = W_1 - W_2$	$\Delta W/W$	$\Delta W/W$
$\Delta L = L_1 - L_2$	$-\Delta L/L$	$-\Delta L/L$
$\Delta K' = K'_1 - K'_2$	$\Delta K'/K'$	$\Delta K'/K'$
$\Delta(\lambda V_{DS}) = (\lambda V_{DS})_1 - (\lambda V_{DS})_2$	$\Delta(\lambda V_{DS})/(\lambda V_{DS})$	$\Delta(\lambda V_{DS})/(\lambda V_{DS})$
$\Delta\theta = \theta_1 - \theta_2$	$-\Delta\theta/\theta$	$-\Delta\theta/\theta$

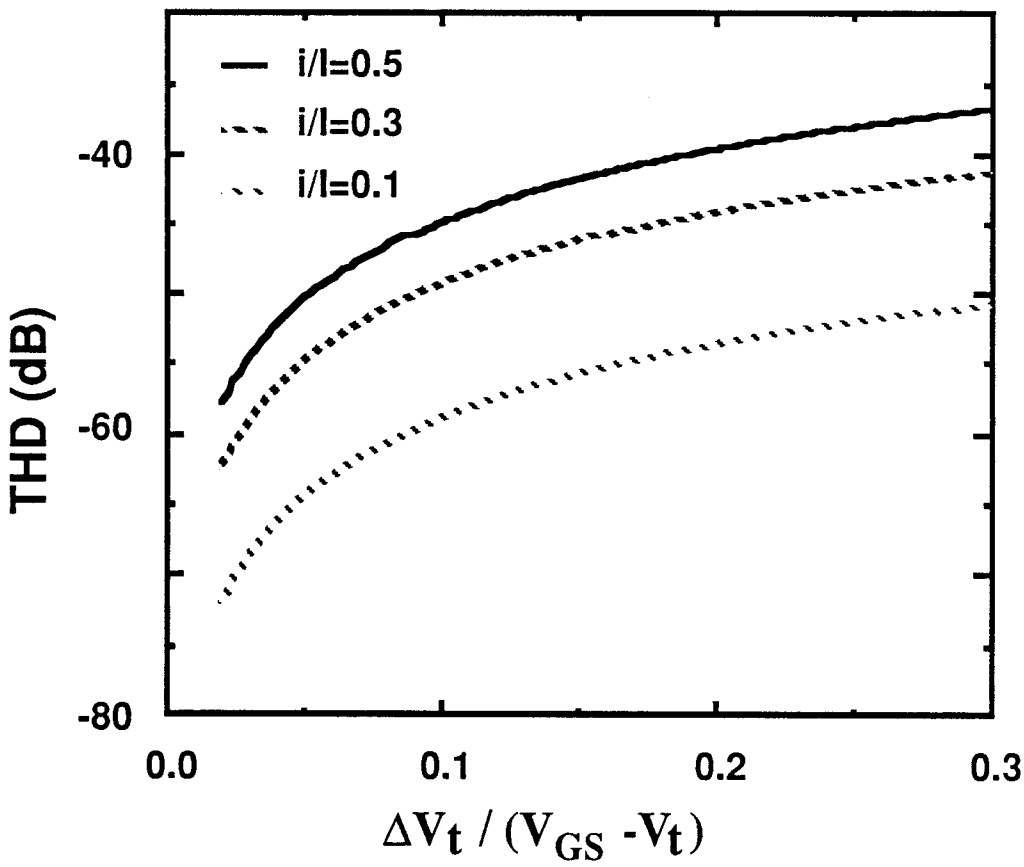


Fig. 3.2 Plot of total harmonic distortion versus $\frac{\Delta V_t}{V_{GS}\text{-}V_{t_1}}$ for increasing i/I ratios.

To minimize the process-induced current mirror transistor mismatches, precision layout strategies such as common-centroid and unit-cell approaches can be used. In the common-centroid layout approach, the transistors are arranged about a centroid such that effects of directional linear gradients in the processing of the die are minimized. The unit-cell layout approach breaks the large aspect ratio current mirror transistors into many smaller sized transistors, and thus, the edge effects are, to a first order, cancelled.

3.4 Distortion in Current T/H Circuit

The device mismatch distortion analysis performed above for the simple current mirror also applies directly to the switched current mirror. In this section, the effects of clock-feedthrough in the switched current mirror are analyzed.

Figure 3.3(a) shows a simple switched-current track-and-hold circuit -- the basic building block for the SI circuits. With the switch M_S ON, the circuit ideally performs current inversion and amplification. The input signal, i_{in}, is mirrored to M_2 resulting in an inverted output signal, $i_{out} = -i_{in}$. (Assume M_1 and M_2 operate in saturation and are identical.) When the switch turns OFF, charge stored on the gate capacitance of M_2, C_{g_2}, holds a voltage commensurate to the current signal at the instant when the switch opened. Hence, this basic circuit performs a *track-and-hold* function in the current domain.

A major potential problem of the circuit of Fig. 3.3(a) is the clock-feedthrough effect due to the non-ideal characteristics of the NMOS switch, M_S. To illustrate the adverse effects of clock-feedthrough, the switched-current mirror in Fig. 3.3(a) was simulated using SPICE. The simulation conditions are listed in Table II and the results are plotted in Fig. 3.3(b). In this example, the peak clock-feedthrough current is about 6 μA versus a peak output signal current of 20 μA. This is an unacceptable level for high-accuracy analog signal processing applications.

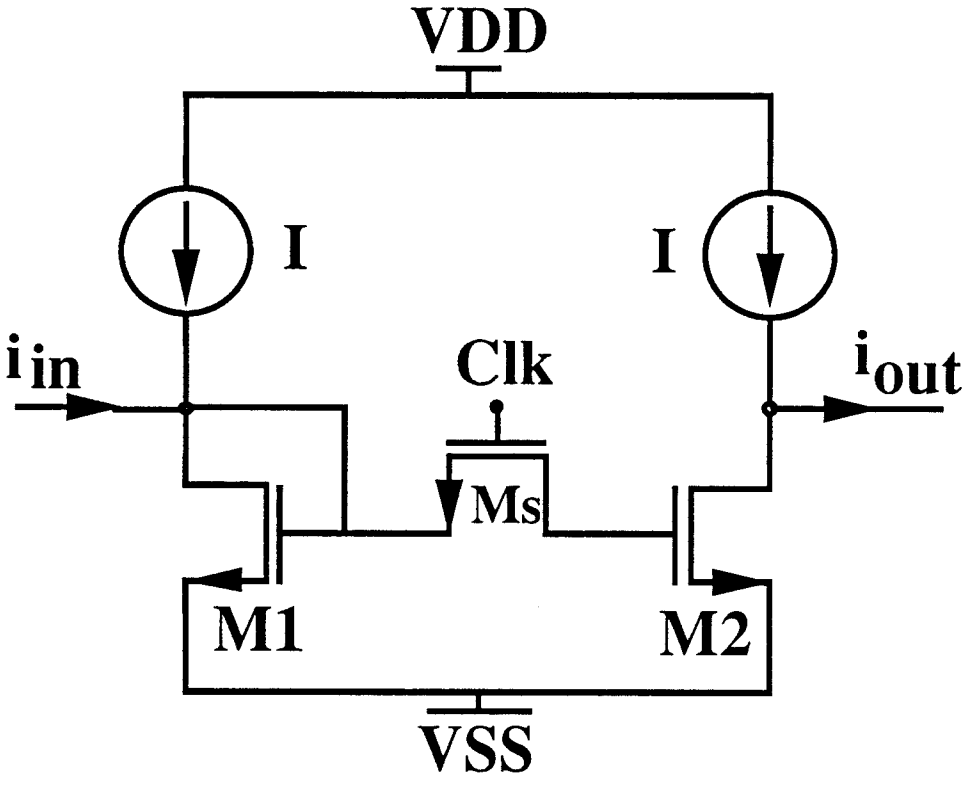


Fig. 3.3 (a) Current track-and-hold used in SI circuits.

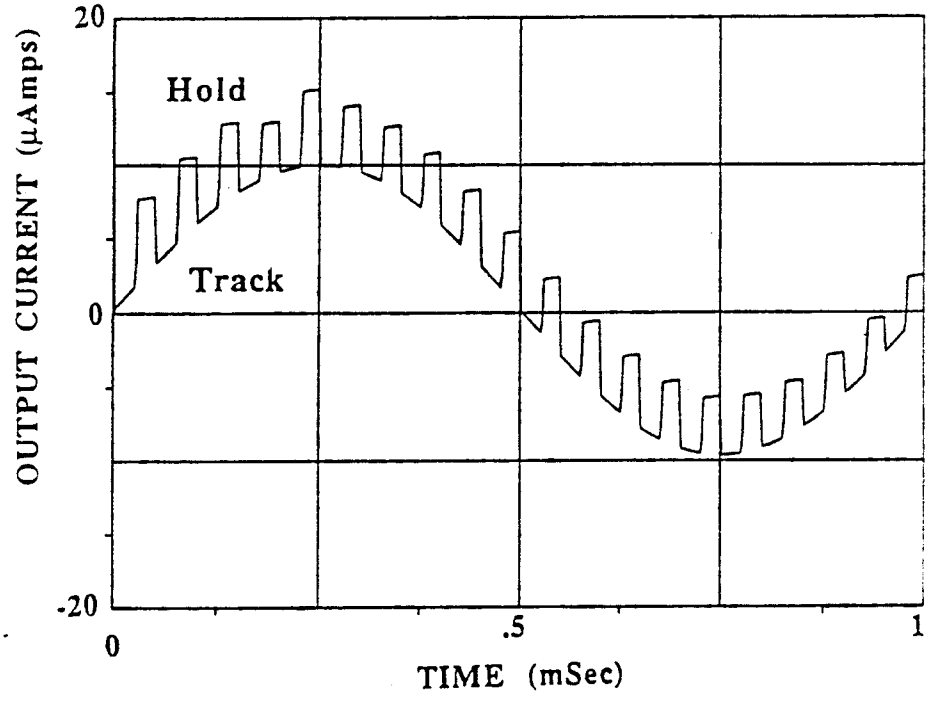


Fig. 3.3(b) Simulation of the circuit in Fig. 3.3(a)

TABLE 3.2 Simulation parameters for Fig. 3.3(b).

	I	i	Clock
Magnitude	200μA	20μA	0 - 5 Volts
Frequency (kHz)	DC	1	50

The clock-feedthrough effects in SC circuits have been studied extensively [18-20]. In this work, the clock-feedthrough mechanisms have been characterized and the voltage induced on the data holding node has been quantified. Generally for SC applications, the source resistance driving the T/H is assumed infinite and analytical solutions can be found. In the current T/H circuit, however, the source resistance represented by the diode-connected MOSFET varies as a function of the signal level and hence, only numerical solutions can be found. Additionally, the harmonic distortion in the output current has not been previously determined for the SI T/H circuit.

Charge injection onto the data holding node occurs as the clock is brought from its high voltage (on) to low voltage (off). As the switch transistor, Ms, is turned off, charge is injected onto the data holding node, the gate capacitance of M_2 in Fig. 3.3(a). There are two phases of operation resulting in charge injection: during phase a, the switch is conducting and during phase b, the switch is nonconducting. The models for the T/H circuit, Fig. 3.3(a), in these two phases are shown in Fig. 3.4(a) and (b), respectively. In phase a, as the clock on the gate of Ms is falling, the switch channel conductance is decreasing as a function of time:

$$g(t) = k' (W/L) [Vgate(t) - Vs - V_t] \tag{3.6}$$

where, $Vgate(t)$ = gate voltage of the switch decreasing at a rate, α in *Volts/sec.*

Vs = DC voltage at drain and source of the switch.

V_t = switch threshold voltage (including backgate effects due to variation in Vs).

Partial differential equations can be written for the circuit and they are:

$$\frac{\delta v_s}{\delta t} C_{in} = g(t) (v_d - v_s) - \frac{v_s}{R_s} - i_{inj} \tag{3.7}$$

$$\frac{\delta v_d}{\delta t} C_L = g(t) (v_s - v_d) - i_{inj} \tag{3.8}$$

$$i_{inj} = \frac{\delta(v_s - v_{gate})}{\delta t} C_{g(switch)} \tag{3.9}$$

where, v_d and v_s are the clock-feedthrough voltages on the drain and source of the MOS switch. The DC voltage *Vs* applied to the source and drain is assumed to be constant as the switch turns off (this assumption is valid for slowly changing signals relative to the clock edge). In this expression, the injection current is due to the coupling of the switch capacitance to the load capacitance:

$$i_{inj} = \alpha (C_{ol} + 1/2\ C_{ox} W_{eff} L_{eff})_{switch} \tag{3.10}$$

where, α is the rate-of-change of the clock voltage in *Volts/sec*. The excess charge in the channel as the conductance decreases is deposited on the gate capacitances, C_{in} (C_{gs1}) and C_L (C_{gs2}.) The switch transistor is turned off when $Vgate=V_t + Vs$. The model for the turn-off condition is shown in Fig. 3.4(b) where the equivalent circuit is a simple capacitor divider. The equation to determine clock-feedthrough voltage in this condition is:

$$\frac{\delta v_s}{\delta t} C_{in} = - \frac{v_s}{R_s} - i_{inj} \tag{3.11}$$

$$\frac{\delta v_d}{\delta t} C_L = - i_{inj} \tag{3.12}$$

In this expression, $i_{inj} = C_{ol\ (switch)}\,\alpha$.

Solving the expressions using numerical methods, the amounts of clock-feedthrough voltage on the source and data holding nodes are determined. A three-dimensional plot of the clock-feedthrough voltage on the data holding node is shown in Fig. 3.5. The feedthrough voltage is a function of the aspect ratio of the switch to mirror transistors, the clock slope, the source resistance and the transistor ratio of the current mirror transistors. For increasing switch turn-off rate, there is more clock-feedthrough voltage. When the switch turns off slowly, the channel charge can leak to the source side of the T/H. This reduces the amount of clock-feedthrough voltage on the data holding node. Based on a first-order analysis, the clock-feedthrough voltage, V_{cf}, on the data holding node is proportional to the ratio of the switch overlap capacitance to the load capacitance. Since C_L (C_{gs_2}) is substantially smaller than the load capacitance in SC circuits, the ratio C_{switch} $/C_{load}$ is larger for SI circuits. This indicates a larger value of clock-feedthrough voltage, V_{cf}.

The clock-feedthrough voltage has a similar effect on the current T/H performance as the threshold voltage mismatch. Therefore, the ΔV in Fig. 3.2 can represent the threshold voltage mismatch plus the clock-feedthrough voltage and a first-order evaluation of THD for a given i/I ratio can be determined. A 3-D plot of the THD due to clock-feedthrough is shown in Fig. 3.6. The signal current to bias current ratio, i/I, is 0.3. To minimize the THD of the output current due to clock-feedthrough effects, a high bias voltage on the current mirror is necessary. In this plot, for Vs = 1.8 Volts, THD = -50dB while increasing Vs to 2.5 Volts reduces the THD by 10 dB.

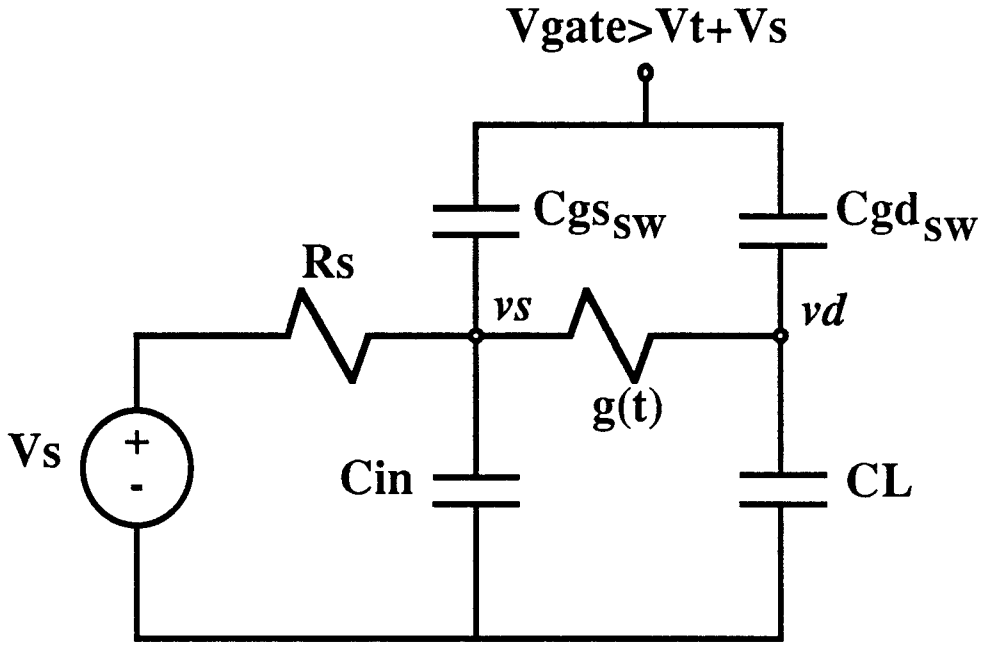


Fig. 3.4(a) Model of current T/H with switch in conduction (Vgate-Vs>Vt)

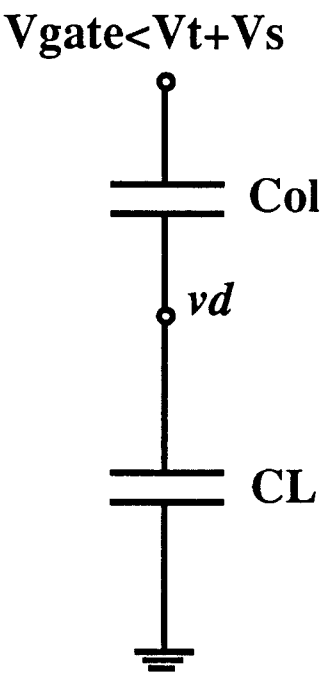


Fig. 3.4(b) Current T/H model for switch nonconducting.

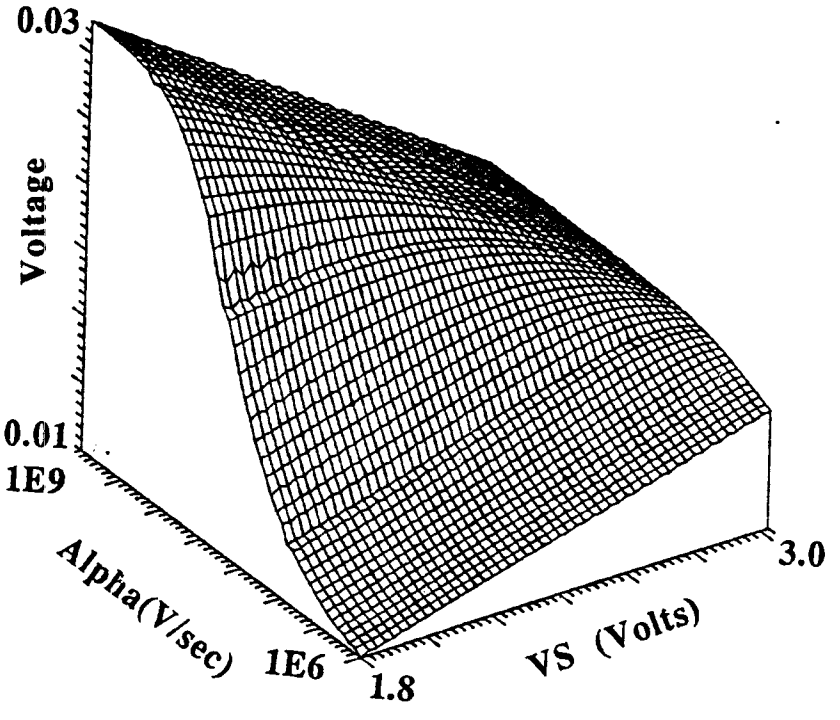


Fig. 3.5 Plot of clock-feedthrough voltage to data holding node of Fig. 3.3(a). The transistor sizes are $(W/L)_1=(W/L)_2=100\mu/10\mu$, $(W/L)_{switch}=5\mu/2\mu$.

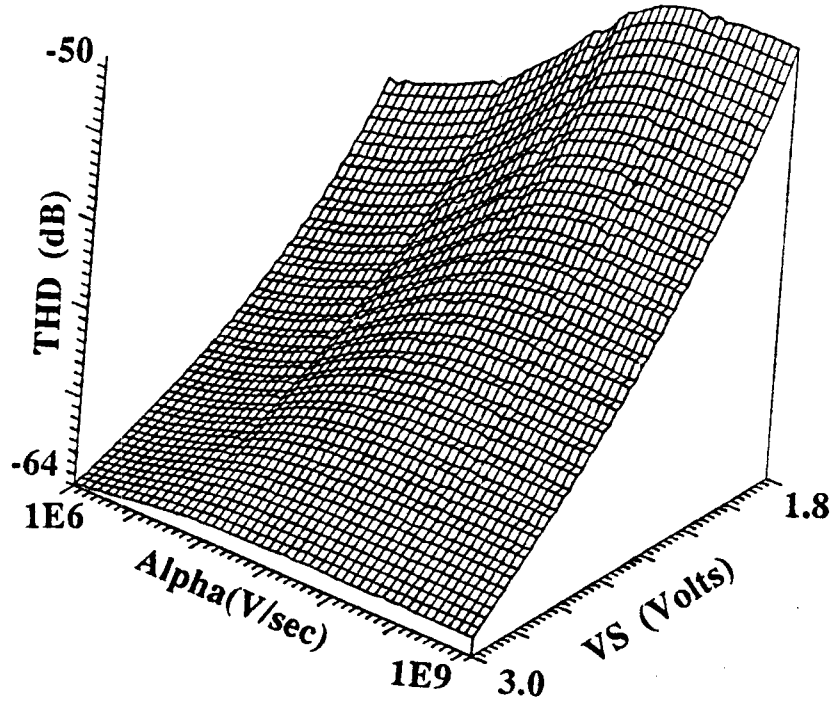


Fig. 3.6 Plot of THD of the output current in Fig 3.3(a) due to clock-feedthrough.

3.5 Distortion Cancellation in the Current T/H Circuit

To minimize harmonic distortion due to threshold mismatch in the current mirror transistors, the gate-source voltage of the mirror transistors can be increased. The threshold voltage mismatch then becomes a smaller percentage of the total voltage $(V_{GS}-V_t)$. The maximum gate voltage, however, is limited to the power supply voltage minus the voltage to maintain the current source loads in saturation. For a 5 volt supply, the gate voltage will be limited to approximately 4.5 volts. A circuit technique that eliminates the distortion due to transistor mismatches in the current mirror is the the dynamic current mirror [26], or current copier [27]. Under two-phase clock control, the dynamic current mirror, shown in Fig. 3.7, uses only one transistor that serves as both the diode-connected transistor and the mirror transistor. When the (1) switches are closed and the (2) switches are open, the transistor is diode-connected. The transistor current is the sum of the bias and signal currents. A voltage corresponding to this current level is induced across the non-critical gate capacitance of the transistor. When the (1) switches are open and the (2) switches are closed, the gate capacitance holds the voltage corresponding to when the diode connection was opened. The output current is the current sampled during clock 1 minus the bias current, I. Thus, the current has been replicated or mirrored to the output. This technique eliminates any mismatch distortion, but still has the problem that it introduces clock-feedthrough distortion. One potential problem of this circuit is the "hold-and-float" nature rather than track-and-hold type operation. During phase 1, the voltage corresponding to the current is stored on the gate capacitance. When both clock 1 and 2 are low, during the non-overlapping region, the transistor drain current is $I+i_{in}$, and the current source

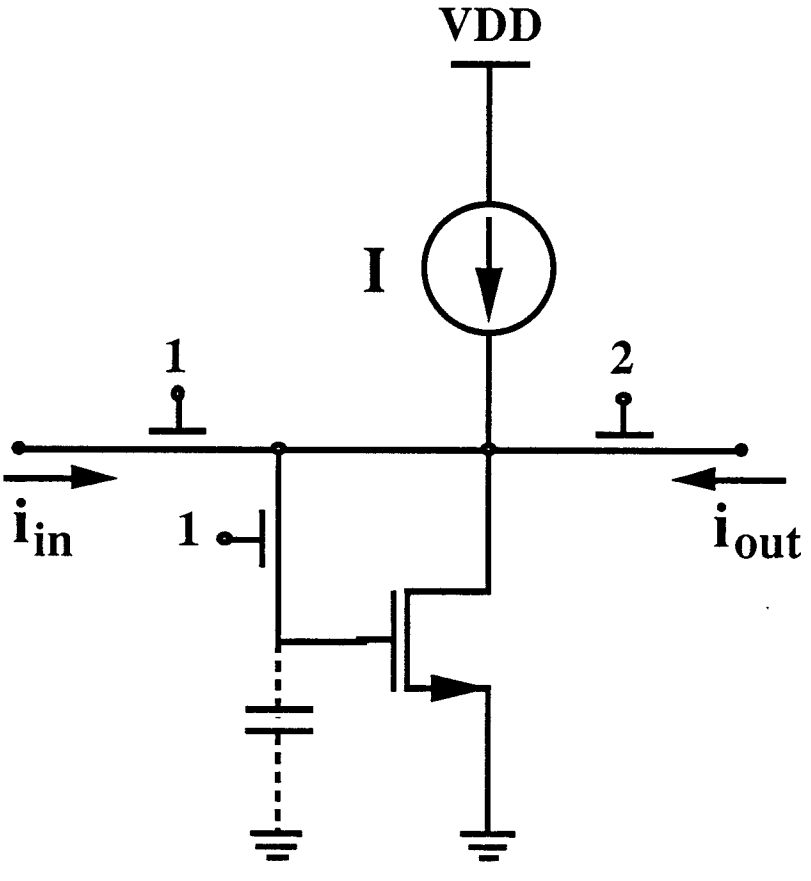


Fig. 3.7 Dynamic current mirror

supplies the current I. This forces the drain voltage to compensate for the mismatches in current. As a result, when the switch 2 is closed, the output current must settle to its final value. This may produce severe nonideal circuit operation.

To reduce clock-feedthrough effects, different charge cancellation (or compensation) schemes have been proposed for SC circuits [28,29]. A disadvantage of charge cancellation techniques is that they usually require more than one critically-timed clock phase. Charge cancellation accuracy depends strongly on interactions between clock phase edges which are very difficult to control precisely in practice; thus, complete cancellation is not achievable. A commonly-used dummy MOSFET cancellation technique for gate voltages is applied to the switched-current mirror, Fig. 3.8. The dummy MOSFET is one-half the size of Ms, and as Ms is turned off, the dummy MOSFET is turned on and collects the clock-feedthrough charge. It is clear that this technique is not totally successful for SI circuits due to the signal-dependent source impedance associated with the diode-connected MOSFET and the precise control of clocks that is necessary.

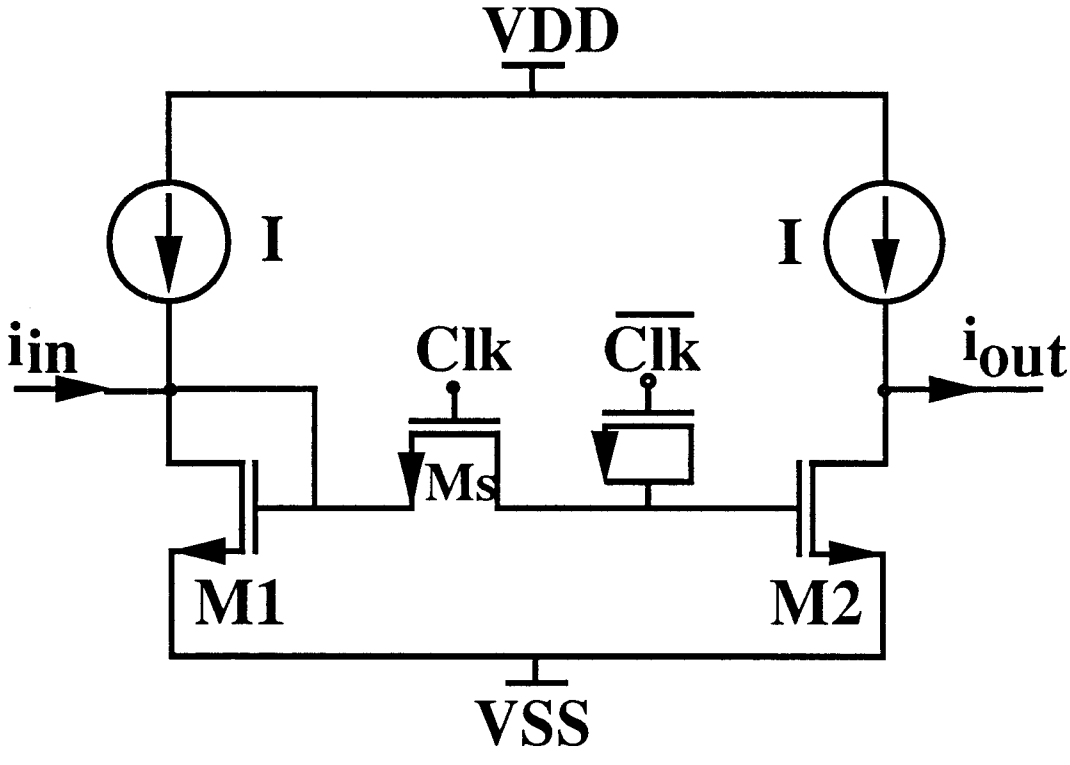


Fig. 3.8 Charge cancellation of clock-feedthrough using dummy MOSFET.

Based on the above analysis, a current-domain clock-feedthrough cancellation technique has been developed for SI circuits. Such a cancellation technique is illustrated in Fig. 3.9. M_1, M_2 with Ms_2 form a switched-current mirror (*SCM1*), and MR_1, MR_2 and Ms_1 (*SCM2*) are replicas of M_1, M_2 with Ms_2, respectively. At node A, *SCM2* generates a pure clock-feedthrough current without carrying the signal, and *SCM1* generates both the sampled-data signal and the clock-feedthrough currents at node B. Since Ms_1 and Ms_2 are controlled by the same clock, the clock-feedthrough currents at node A and B are in phase. The feedthrough current of node A is inverted by the PMOS current mirror and summed at node B to cancel the non-signal dependent feedthrough current generated by *SCM1*. The output current, therefore, contains only the sampled-data signal current and signal dependent clock-feedthrough. A salient feature of this technique is that it requires no additional controlling clock. Figure 3.10 shows SPICE simulation results for this circuit. The circuit successfully cancels the first-order clock-feedthrough effect and provides an excellent sampled-and-held output signal current. The small amount of remaining clock-feedthrough current (a peak value of about 0.6 mA) is due to the signal dependent clock-feedthrough.

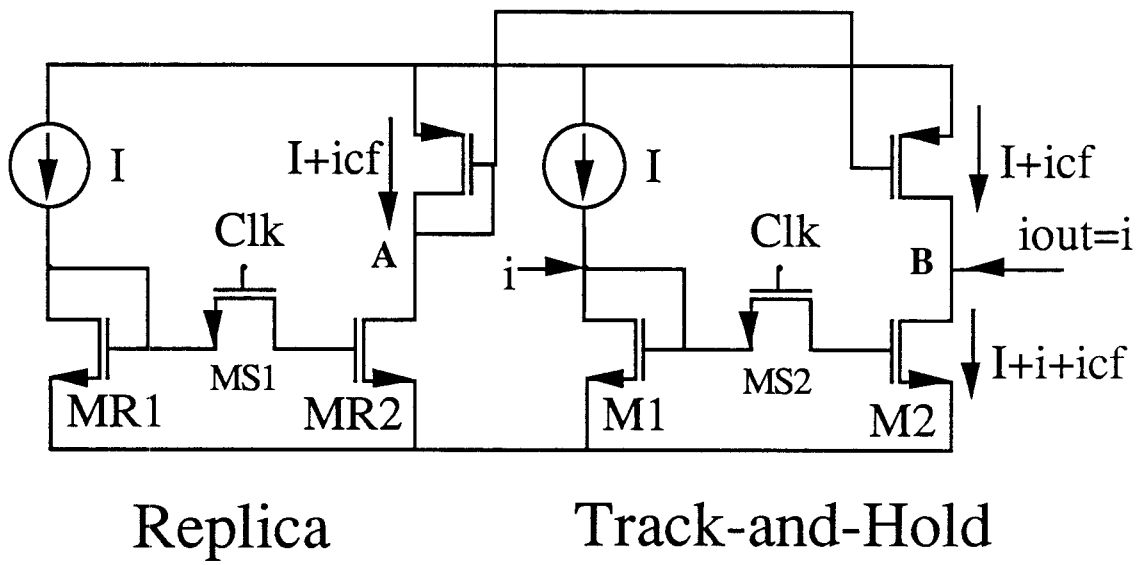


Fig. 3.9 Schematic of current cancellation of clock-feedthrough.

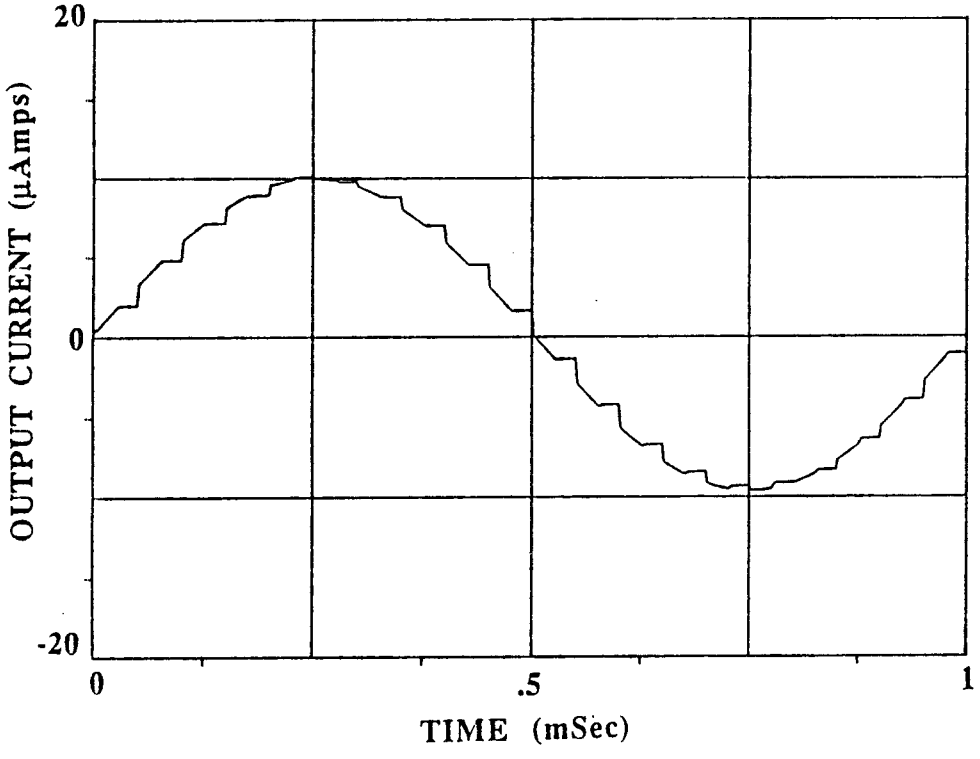


Fig. 3.10 Simulation of current cancellation of Fig. 3.9. Compared to Fig. 3.3(b) nearly all of the clock-feedthrough effects have been cancelled.

Another circuit that can be used to give first order cancellation of the clock-feedthrough is shown in Fig. 3.11 [21]. Each T/H generates clock-feedthrough output current. The clock-feedthrough output current in the first T/H is inverted with a gain near unity and added to the feedthrough of the second T/H and thus, the non-signal dependent clock-feedthrough is cancelled. With no signal input applied to the drain of M1, all the clock-feedthrough output current is cancelled. However, with a peak input signal of $I/2$, the cancellation is approximately only 30% better than the previous current cancellation scheme.

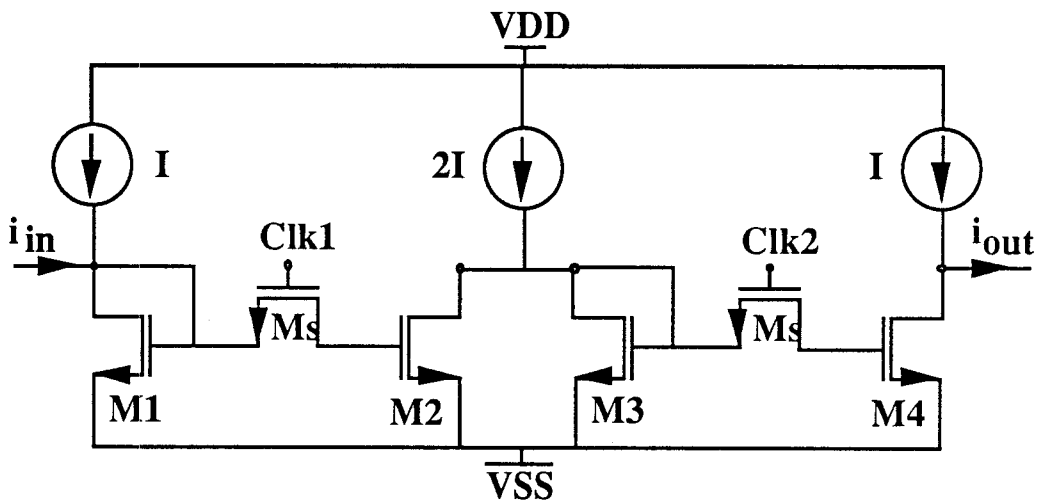


Fig. 3.11 Cascaded current T/H circuit gives first order cancellation of clock-feedthrough.

3.6 Dynamic Range in SI circuits

The magnitude of the RMS noise over the bandwidth of interest that is present in an analog circuit determines the minimum detectable signal level. In this section, the input-referred noise current in current-mode circuits is examined. There are two dominant noise sources in the MOS transistor: flicker noise (often referred to as 1/f noise) and thermal noise [30]. The flicker noise is concentrated at low frequencies and arises from the surface states present in the channel of the MOS transistor. The flicker noise power spectral density of an MOS transistor is:

$$S_{v(1/f)} = \frac{\overline{v}^2}{\Delta f} = \frac{1}{CoxWL}\,\frac{1}{f}\,K_F\,I^{AF-1}. \tag{3.13}$$

where K_F and AF are process dependent parameters. The flicker noise is inversely proportional to the transistor area and frequency, and is directly proportional to the gate oxide thickness. Thermal noise spectral density in an MOS transistor is constant across the frequency spectrum. Thermal noise arises from the resistance of the channel and is:

$$S_{v(th)} = \frac{\overline{v}^2}{\Delta f} = 4KT\left(\frac{2}{3g_m}\right) \tag{3.14}$$

where K = Boltzman's constant and T = absolute temperature.

Since $g_m = \sqrt{2k'(W/L)I}$, thermal noise is inversely proportional to the square root of the transistor aspect ratio, (W/L), and the bias current, I. The total RMS noise voltage is the RMS sum of these two noise sources times the square root of the bandwidth and is represented by a noise voltage source in series with the gate of the transistor, Fig. 3.12(a) or as a noise current source across the drain-source

terminals, Fig. 3.12(b). Using the equivalent noise voltage source or current source, circuits can be evaluated to determine the total input referred noise voltage or current. Below is the calculation of the input-referred noise current of the basic SI circuits

The most basic current-mode circuit is the simple current mirror with noise sources v_{n1}^2 and v_{n2}^2, Fig.3.13. The input-referred noise voltage is transformed to current by multiplying by the transistor transconductance, g_{m1}^2:

$$\overline{i_{ni}}^2 = g_{m1}^2 (\overline{v_{n1}}^2 + \overline{v_{n2}}^2). \tag{3.15}$$

Considering only the thermal noise, the input-referred current spectral density, $\bar{i}/\sqrt{\Delta f}$, is $3.7\ pA/\sqrt{Hz}$ for $(W/L)_1=100\mu/10\mu$, $(W/L)_2=20\mu/10\mu$ and $I_{bias}=50\mu A$. Doubling the widths of both M1 and M2, doubles the total noise current. In SI circuits, two current amplifiers are cascaded to obtain very small coefficients. The input-referred noise current will be increased due to the increase in the number of devices. In Fig. 3.14, the first current mirror has gain, A and the second has gain, B. The input-referred noise current is:

$$\overline{i_{ni}}^2 = [(\overline{v_{n1}}^2 + \overline{v_{n2}}^2)\frac{g_{m2}^2}{g_{m3}^2} + \overline{v_{n3}}^2 + \overline{v_{n4}}^2]\frac{g_{m4}^2}{AB} \tag{3.16}$$

This is the output-referred noise current divided by the gain of the amplifier, AB. For the SI filter designs presented in this thesis, all the current amplifiers are high-swing cascode current mirrors, Fig. 3.15. The input-referred noise is:

$$\overline{i_{ni}}^2 = (\overline{v_{n1}}^2 + \overline{v_{n2}}^2)\, g_{m1}^2 + (\overline{v_{n3}}^2 + \overline{v_{n4}}^2)\, g_{m3}^2. \tag{3.17}$$

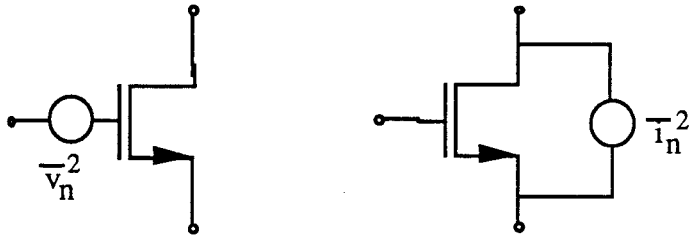


Fig. 3.12 (a) Noise voltage source in MOS transistor and (b) noise current source in MOS transistor.

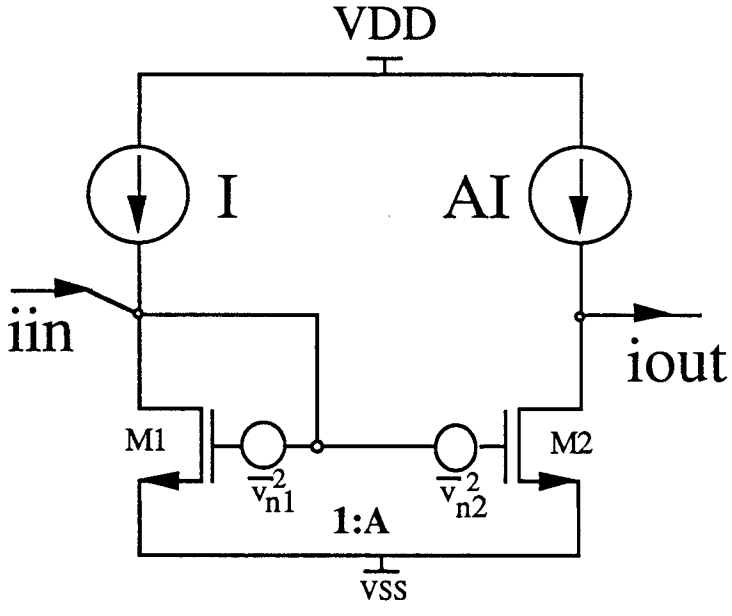


Fig. 3.13 Current amplifier (gain=A) with noise sources shown.

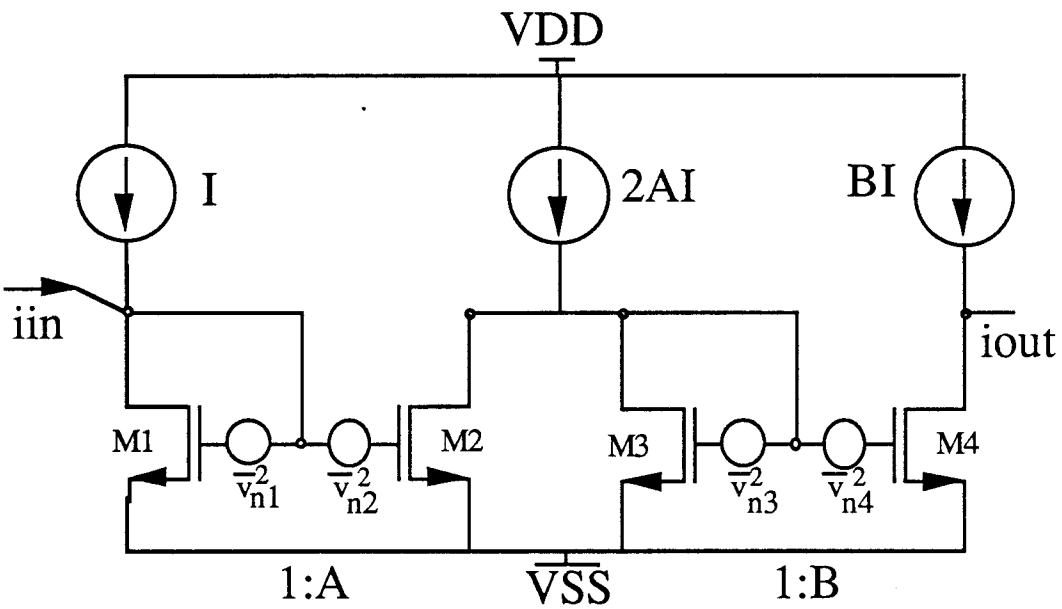


Fig. 3.14 Cascaded current amplifiers with gain A and B.

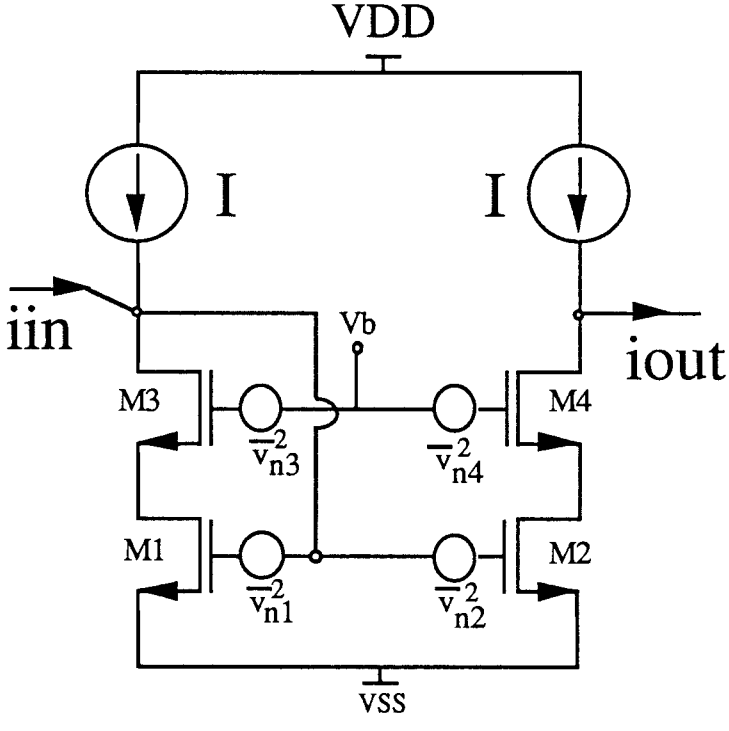


Fig. 3.15 High-swing cascode current amplifier.

This is twice the noise current of the simple current mirror with all the transistors the same (W/L).

In addition to current mirror circuits, the current T/H is also a critical block in SI circuits. The switch transistor thermal noise is evaluated by considering a noiseless source and noiseless load capacitance, Fig. 3.16. The equivalent noise bandwidth of a one-pole filter is $\Delta f = \frac{\pi}{2} f_1$, where the filter -3 dB bandwidth is $f_1 = \frac{1}{2\pi R_{on} C}$. Using the equivalent noise bandwidth, the switch thermal noise power is:

$$\overline{v_{ntot}}^2 = 4KTR_{on}\Delta f = 4KTR_{on}\left[\frac{1}{4R_{on}C}\right] = \frac{KT}{C} \tag{3.18}$$

The total RMS noise voltage is $\sqrt{\frac{KT}{C}}$. Thus, the switch thermal noise is independent of the switch on resistance. As expected this is the same as the limiting factor of noise in SC circuits [31].

Using the results from above, the final basic current-mode circuit, the current T/H, is evaluated. In this circuit, the broadband thermal noise is sampled at f_s, the clock frequency. The sampling frequency is assumed to be much less than the bandwidth of the noise and thus, the noise folds back into the sampling bandwidth. The effects of under-sampling the noise must be included in the computation of the noise. In general, the output-referred noise of the current T/H is:

$$\overline{i_{no}}^2/\Delta f = \overline{i_{n2}}^2/\Delta f + g_{m2}^2 S_{io}(\omega) \tag{3.19}$$

where, $\overline{i_{n2}}^2 = g_{m2}^2\,\overline{v_{n2}}^2$ *and,* $S_{io}(\omega) = S_i(\omega)\,H(z)\,(2N+1)\,sinc^2(\pi\omega/\omega_s)$.

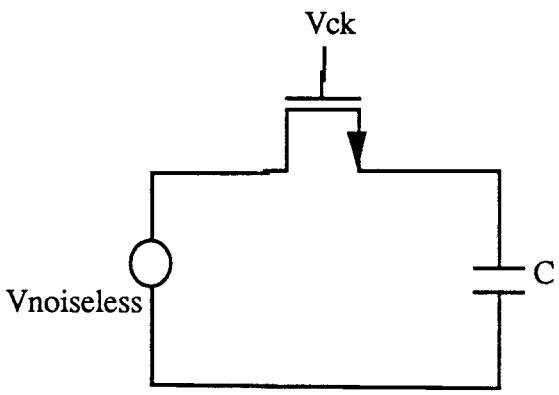


Fig. 3.16 Model for determination of thermal noise in switch.

In this expression, $S_i(\omega)$ is the sum of the switch thermal noise and the noise current spectral density of M1, $H(z)$ is the transfer function from the input to output, N is the number of sidebands and the last term takes into account the square sample shape. This general expression can be used to evaluate SI filters, however, it rapidly becomes very complicated due to the feedback contained in the filter.

The output-referred noise voltage spectral density of a fifth-order Chebychev SI filter and a third-order Elliptic SI filter were measured. The noise plots are shown in Fig. 3.17 and 3.18, respectively. The outputs were measured across a 100 kΩ resistor with no input current applied. The input-referred noise currents and equivalent noise voltages are shown in Table 3.3. The input-referred noise voltages are comparable to SC circuits.

Using the results from above, the dynamic range in the SI filters is determined, Table 3.3. The maximum signal level is one-half the bias in order to have less than 1% THD and the minimum signal is determined by the input-referred noise current. The dynamic range of the Elliptic filter is greater than 13 bits in the filter bandwidth and approximately 12 bit in the Nyquist bandwidth. The Chebychev filter has a dynamic range of approximately 12 bits for both the filter bandwidth and the Nyquist bandwidth. The results of these first SI filters are of the same order as the early SC filters.

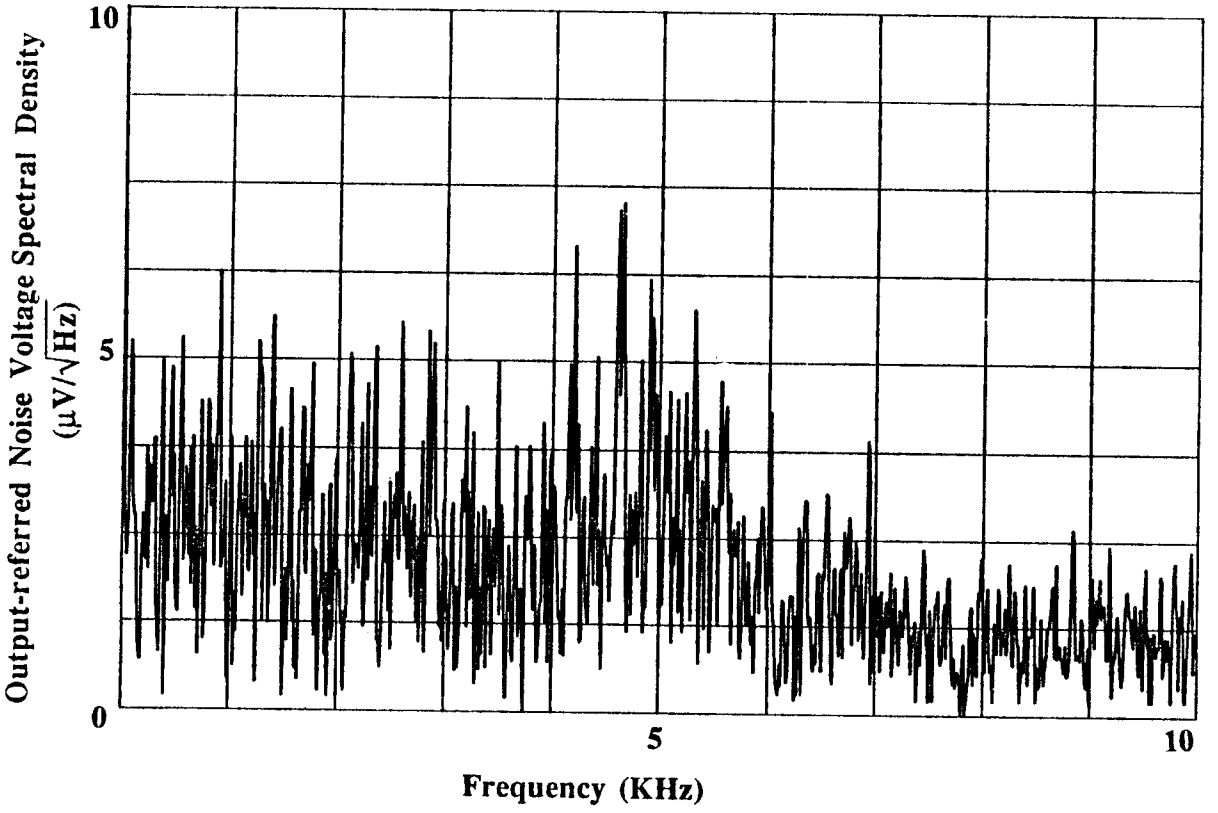


Fig. 3.17 Measurement of output referred-noise in Chebychev SI filter with R_{out}=100 KΩ.

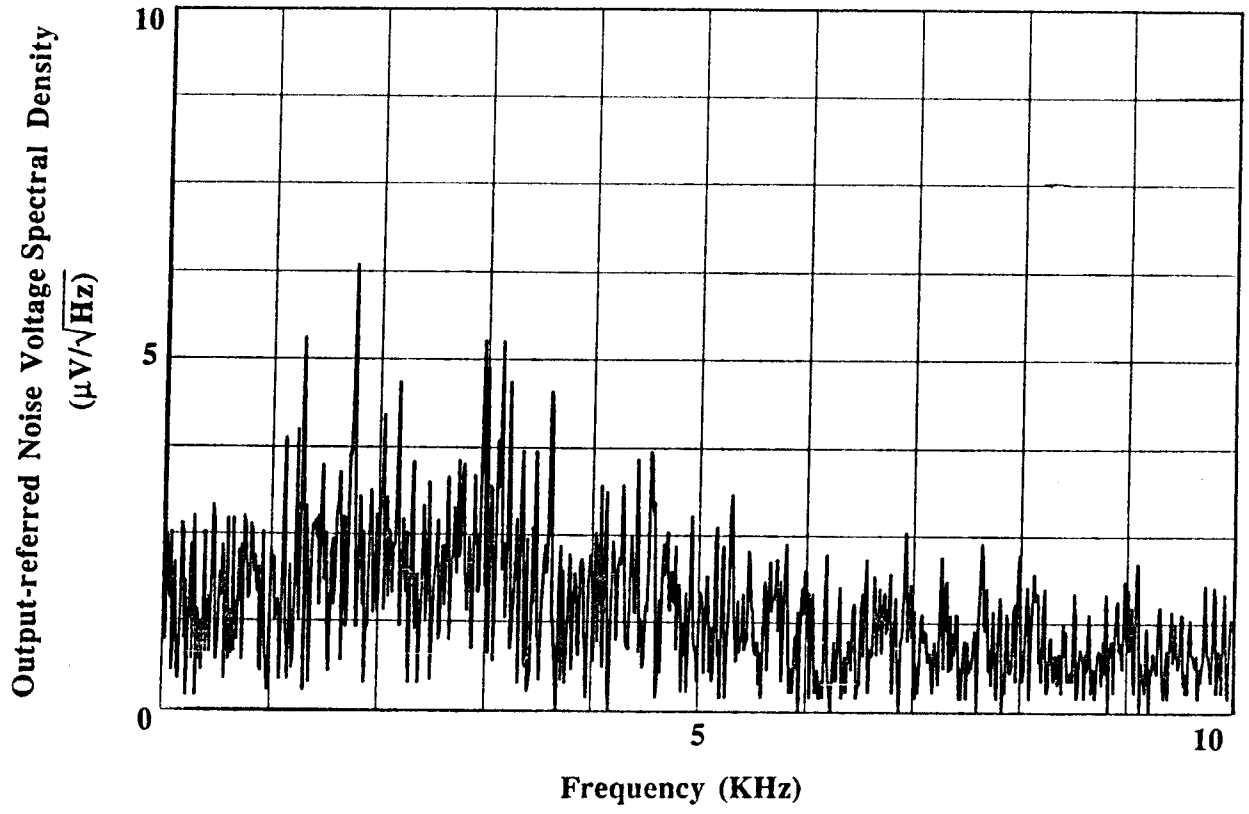


Fig. 3.18 Measurement of output referred-noise in Elliptic SI filter with R_{out}=100 KΩ.

Table 3.3 Measurements from integrated SI filters (f_{co} (Chebychev)=4.7KHz, f_{co} (Elliptic)= 2.9KHz).

	Chebychev	Elliptic
RMS noise (300-f_{co})	4.1 nA_{RMS} (284 nv/$\sqrt{Hz}$)	1.7 nA_{RMS} (150 nv/$\sqrt{Hz}$)
RMS noise (f_{co}-64K)	6 nA_{RMS}	4.8 nA_{RMS}
Dynamic range (300-f_{co})	72.6 dB	80.3 dB
Dynamic range (f_{co}-64K)	69.3 dB	71.3 dB

3.7 Conclusion

In this chapter, the distortion due to device mismatches and clock-feedthrough effects in SI circuits has been analyzed. Using the results of this analysis, the relationship between signal size and total harmonic distortion has been characterized. The maximum signal size is found from this relationship and is used in conjunction with noise measurements to obtain the dynamic range of the integrated SI filters.

CHAPTER 4

CONCLUSION

This thesis has presented the analysis and design of CMOS SI filters. Synthesis techniques of SI ladder and biquadratic filters have been described that leverage the previously developed SC filter synthesis techniques. The feasibility of these synthesis techniques has been demonstrated with the integration of fifth-order Chebychev and third-order Elliptic SI lowpass filters in a standard digital CMOS technology. Simulations accurately predict the filter frequency responses when the clock-feedthrough effects are taken into account. The results from the "first generation" SI filters are very promising; however, performance improvements are necessary to make this a widely-accepted, easily manufacturable circuit technique.

Significant reduction of elimination of the clock-feedthrough effects in SI circuits will yield the greatest overall performance improvements. The SI filter accuracy, speed, PSRR and dynamic range will be significantly increased. In the SI filters presented here, the clock-feedthrough voltage produced approximately a 5% integrator gain error which causes droop in the filter frequency response. Predistortion of the filter poles and zeros can compensate for the droop in the frequency response, but the low sensitivity properties are lost. The current cancellation and cancellation by cascading current mirrors improves the accuracy significantly only if the signal dependent clock-feedthrough (low harmonic distortion) is small. This requires that the area of the mirror transistors be much greater, approximately 25 times greater, than the area of the switch. Increasing the aspect ratio of the mirror transistors to the switch transistor, however, reduces the

bandwidth of the circuit. Therefore, to improve the speed, accuracy and dynamic range of SI filters, a complete elimination of the clock-feedthrough is desirable.

The power supply rejection of a current mirror circuit is very good. The noise from the positive power supply that couples into the signal path is attenuated by the ratio of the impedance of the diode-connected transistor divided by the impedance of the current source. For a simple current mirror, this ratio is approximately 0.01. Using a high-swing cascode current mirror improves the attenuation by two orders of magnitude. Power supply noise on the negative supply is projected to the gate of the transistor. However, the gate-source voltage of the current mirror transistors remains unchanged because of the constant current, and therefore, the signal is unaffected by noise on the negative power supply. The current T/H power supply noise immunity is limited by the clock noise coupling into the signal path. The coupling is determined to a first-order by the ratio of the switch overlap capacitance to the mirror transistor gate capacitance. Thus, eliminating the clock-feedthrough will likely also significantly improve power supply noise immunity.

As presented in chapter 3, process mismatches in the current mirror transistors cause distortion in the signal current. Although the dynamic current mirror eliminates these mismatches by using only one transistor, it has potentially poor settling characteristics. This approach has potential if this effect can be eliminated. Further work should be done here to adapt this technique to SI filter design.

Once the clock-feedthrough and process mismatch effects are eliminated, it will be possible to demonstrate the speed capabilities of this technique. High-speed SI circuits require small devices that will most likely introduce speed-accuracy trade

offs. To obtain optimal high-speed performance, the minimum settling time conditions must be analyzed.

Another area that needs further work is the design of low-noise SI circuits. Chopper stabilization techniques have been used in SC applications to obtain low noise circuits [32]. In this technique, the flicker noise is modulated up in frequency beyond the bandwidth of interest. The thermal noise is then minimized by design.

Many applications require low power and low voltage operation. Using subthreshold operation, SI circuits that are very low power and operate at low power supply voltages can be designed.

In addition to improving the SI filter performance, many other functions can be developed to make a complete current-mode system. Some function that this technique could be applied to are PLL, multipliers, current-controlled oscillators and analog-to-digital converters. Finally, the current-mode system requires a voltage-to-current converter on the input and a current-to-voltage converter on the output. Once the SI circuits are low distortion, wide dynamic range, it will require very high performance conversions at the input and output. Therefore, efforts should be focused on improving the signal conversions.

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