

Fabrication and Characterization of Nanoscale Devices made from Molybdenum Disulfide

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Abstract

Using a simple dry transfer process, I construct and characterize three nanoscale MoS₂ devices with current-voltage curves as well as Raman spectroscopy, optical and atomic force microscopy. I compare these devices, the thinnest of which was few layer (≤ 10 nm) MoS₂ capable of producing a photocurrent whose magnitude is affected by a split gate bias voltage. The thinnest device's results show mechanical exfoliation paired with a dry transfer is an economical and effective way to fabricate ultrathin gate-tunable devices.

Part 1: Introduction

1.1 Transition Metal Dichalcogenides

Over the last decade research on graphene and similar ultrathin materials, particularly transition metal dichalcogenides (TMDs) including molybdenum disulfide (MoS₂) has increased dramatically. To effectively build and test either thin film devices or 'stacked' heterostructures (multi-layered devices constructed of differing few layer sheets), researchers must isolate and transport ultra-thin or 2D materials without damaging them. Most reliable transfer processes involve wet chemistry and sacrificial polymers, which can be lengthy, require additional lab stations and expertise, while potentially damage other features on the device.

Recently the Steele group at Delft University^[1] developed a method of utilizing viscoelastic properties of polydimethylsiloxane (PDMS) gel sheets to reliably transfer 2D materials. This breakthrough showed the potential of this inexpensive and widely accessible transfer method, which could lead to faster and more widespread progress in the field. Considering the great potential for TMD-based optoelectronic devices, particularly in photovoltaics and wearable electronics, further research surrounding them will likely only become more prominent in coming years^[2].

TMDs, because of their strong planar bonds and weak inter-layer bonds, can be easily mechanically exfoliated into few layer sheets. Figure 1.1 shows an example of two TMD layers with a separation distance of 0.7 nm, the approximate distance between layers in MoS₂.

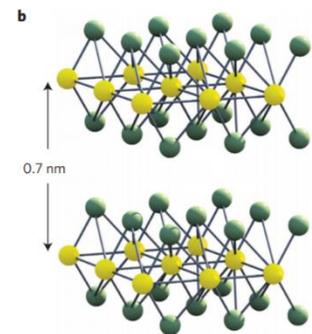


Figure 1.1: Example of TMD layered structure^[4]

1.2 Project Scope

I worked with Mitchell Senger, a graduate student, in setting up and developing a procedure for a transfer station over the first few months of the project. Additionally, he assisted me with the microscopy methods in which I am not yet trained. The transfer process allows us to transfer tiny flakes of a MoS₂ from a PDMS exfoliation site to a silicon chip. The chips we used have platinum electrodes for suspending devices above a trench with split gate wires. The surrounding substrate is 500 nm silicon dioxide on silicon. The goal was to transfer ultra-thin MoS₂ flakes to the chips so that the flakes bridge the source and drain electrodes while placing a flake so that it is under the influence of the gate's electric field. I created and tested these devices in an attempt to characterize the devices thickness and observe a photocurrent in a device thin enough to be substantially electrically doped by the split gates.

1.3 P-N Junctions

P-N junctions are the key interface determining a diode's behavior and are fundamental components of almost all electronics. The combination of a p-type (hole-doped) and n-type (electron doped) material creates a device which allows current to flow easily only in one direction_[11]. This is a vital characteristic for devices studied in photovoltaic applications so finding signs of this behavior in MoS₂ devices is one of my project goals.

P-N junctions can also be formed through altering the electric potential in a device via gating. My samples are un doped so used this principle of electric doping to created p-n junctions within my devices, controlling the electric field through split gates. This creates an electric field within the device, promoting charge flow in only one direction depending on the orientation of the field. Un doped MoS₂ is n-type, so electrons are the overwhelmingly dominant charge carrier_[14].

1.3.1 Schottky Barrier

A Schottky barrier is formed where a metal and semiconductor come into contact, allowing current to flow far more easily in one direction than the other_[10]. The differing work functions of the two materials promote electron flow from the higher Fermi level material to the lower one_[10]. Schottky barriers form on both sites where the TMD flake contacts the source and drain electrodes. Ideally these two Schottky barriers will be roughly equivalent in their effect on photocurrent measurements because the laser source we used illuminates a 1 micron spot in the middle of the device. However, illuminating one side of the

devices (with the focused laser spot covering the boundary between metal and MoS₂) would produce a photocurrent without an externally applied electrical bias due to this the Schottky effect.

1.4 Photoelectric Effect

Adequately thin TMD flakes connected to source and drain electrodes and placed in a variable electric field (being electrically gated) will exhibit transistor behavior. This means at a certain field strength the field overwhelms electrostatic forces within the material, allowing a current to flow from source to drain with significantly less impedance. When incident light strikes the material, it generates electron-hole pairs. In a sufficiently strong electric field these charges are unable to recombine and contribute to the net current of the device. The direction of current flow depends on the electric field's direction. Both photoelectric and photothermoelectric effects have been previously shown to be significant in MoS₂ devices_[12].

1.4.1 Device Band Diagram

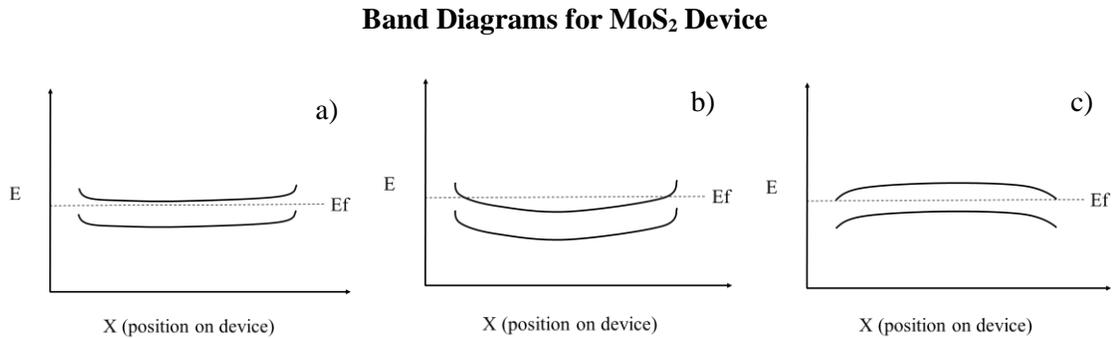


Figure 1.2: Real-space cross-section band diagram for devices, (a) Zero gate voltage, (b) positive gate voltage, (c) negative gate voltage.

In Figure 1.2 (a) we see the band diagram of a typical un doped MoS₂ device, ending on the left and right where the MoS₂ reaches the platinum contacts. This is a cross-section band diagram of the device, meaning the left and right ends of the band lines end where the left and right platinum contacts start. The Fermi energy at each contact will be altered by the source-drain bias.

At a positive gate voltage Figure 1.2 (b), more electrons (the dominant charge carriers in MoS₂) are pulled onto the device. The conduction and valence bands are lowered as the required energy to transport an electron decreases. The conduction band is partially filled allowing, theoretically, for greatly increased electron transport.

Conversely a negative gate voltage, Figure 1.2 (c), will increase the amount of energy required to transport an electron, raising the bands. This makes the device's resistivity increase, provided it still conducts at zero gate voltage.

1.5 Device Architecture

Figure 1.3 below shows the build of a typical suspended MoS₂ device. The trench depth is 700 nm and the width between source and drain electrodes is 2 μm. The cross-section shows an MoS₂ flake bridging grey source and drain electrodes, suspended above the trench. The gating wires are at the bottom of the trench, under a layer of SiO₂.

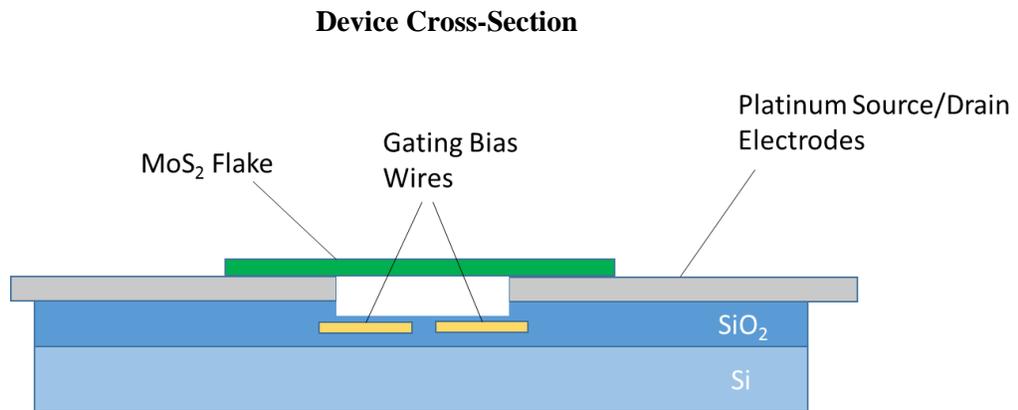


Figure 1.3: A cross-section diagram of a silicon chip with source/drain electrodes and gating wires built onto it. The source and drain electrodes are bridged by the transferred MoS₂ flake.

Part 2: Methods

2.1 MoS₂ Exfoliation

Graphite and TMDs can be easily split into thin sheets using a mechanical exfoliation process. I created ultra-thin MoS₂ devices by mechanically exfoliating MoS₂, then dry transferring flakes to circuit printed, suspended electrode silicon chips. The exfoliation process I used requires only a bulk MoS₂ sample and some scotch tape. I begin by applying the tape to the flat surface of a bulk MoS₂ sample. I peel off the tape, then place it on the sticky side of another new piece of tape. By repeating this process multiple times (generally 3-5) I can create flakes of few layer material.

Too many tape separations will tend to tear the MoS₂ flakes into unusably small pieces^[6], while too few is unlikely to reach the desired flake thinness. I typically do this three times before using the resulting piece of tape (now holding only faint specs of MoS₂) for the PDMS exfoliation.

To exfoliate directly onto PDMS I start by cutting a roughly two square centimeter rectangle of a Gelpak® PDMS sheet, and lay it on a clean standard 75 x 26 mm glass microscopy slide. I place the prepared MoS₂ flake carrying piece of Scotch tape down on top of the PDMS and again rub the surface to eliminate any small bubbles.

The removal of the tape is the physically significant part of this method. This dry transfer process works due to the viscoelastic properties of PDMS. Specifically, this means removing the MoS₂ laden tape from the PDMS quickly increases its adhesive strength (due to the strain force applied by the withdrawing tape). Conversely the slow, controlled removal of the PDMS from a silicon substrate will let the material “relax,” lessening the MoS₂-PDMS adhesive force compared with that of the SiO₂-MoS₂ interaction. In future sections I refer to this group of materials; a glass slide, with a piece of PDMS stuck to it, carrying an MoS₂ exfoliation, as a transfer slide (shown below in Figure 2.1).

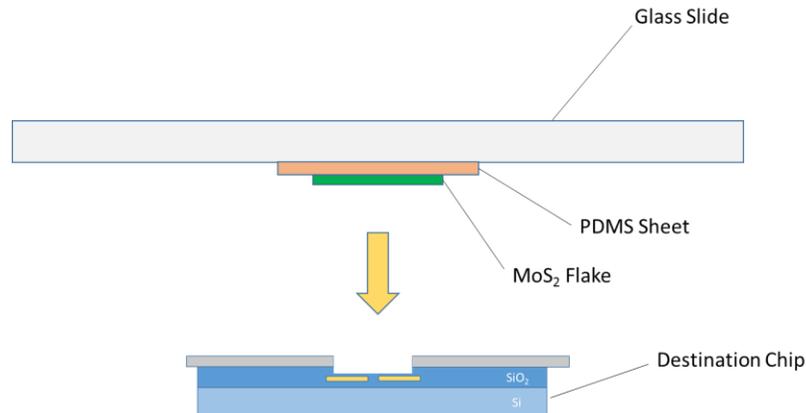


Figure 2.1: A diagram of the transfer slide lowering over a trench chip.

2.2 Transfer Process

Once a transfer slide is prepared, the MoS₂ flakes are ready to be transferred to the silicon chip. First I secure the silicon chip to the Peltier device on the base of the transfer station, directly under the microscope objective. Next, I mount the transfer slide (the PDMS side facing down as shown in Figure 2.1) on the manipulator mount beside the microscope base. I then adjust the microscope baseplate till the desired trench location appears in the lens' reticle.

At this point I focus the microscope on the PDMS, now suspended just above the target location on the chip, and try to identify viable thin MoS₂ flakes by optical contrast. In this setup, few layer MoS₂ appears as a faint translucent gray region. Once I have selected a flake that looks promising, I adjust the manipulator mount until that flake is positioned over the desired trench.

Refocusing on the chip, I lower the manipulator mount until flakes on the PDMS begin to come into the same focal plane as the silicon surface. The PDMS should be no more than a few millimeters above the chip.

I set the proportional-integral-derivative (PID) controller for the Peltier device (Figure 2.2) to 60° Celsius, the temperature at which we have found highest successful transfer rates. Stamping at higher temperatures causes the PDMS to become less “sticky” risking the whole sheet peeling off the slide mid-transfer. I slowly lower the transfer slide until the PDMS touches down on the chip. The PDMS areas in contact with the chip are clearly identifiable by optical contrast between contact and non-contact regions. Using our objective and viewing 500 nm silicon chips, the contact regions appear yellow in color. I leave the flake touching the chip at 60° C for 5 minutes, then raise the mount again, very slowly. If done correctly, the flake should let go of the PDMS, which adheres less to the MoS₂ when peeled off slowly due to its aforementioned viscoelasticity. Ideally the flake is now bridging the platinum contacts on either side of the trench and is ready for annealing.

After a 150° C annealing the device is ready for electrical and optical measurements. The annealing generally decreases the resistivity of the devices, making for better electrical data.

We made several modifications to the transfer station throughout the course of these experiments. The most notable are described in the sections below.

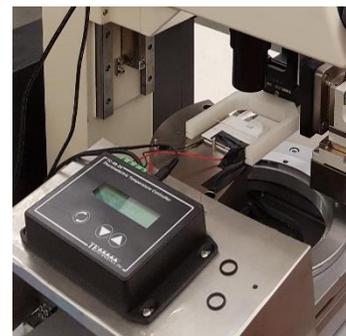


Figure 2.2: Close-up of digital PID (black box), Peltier thermal plate, objective, and manipulator mount.

2.3 Annealing

After constructing my devices, I anneal them to reduce their resistance by roughly three orders of magnitude prior to taking electrical measurements. Our annealing, or heat treating, process involves heating the device chip inside a tube of flowing hydrogen and argon (0.45 Liters/minute and 1 Liter/minute respectively) for 5 minutes at 30° C, then 30 minutes at 150° C.

2.4 Thermal Plate

Thermal plate annealing proved beneficial to higher yield graphene exfoliations for an alternate wet-transfer method studied in our lab previously, so we decided to try the Delft transfer method at higher temperature. Trials at 60° C typically were more likely to be successful and resulted in higher yield. The Peltier device is controlled by a PID voltage supply (Figure 2.2).

2.5 Optics

The transfer station is built around a microscope with a 10X objective (Figure 2.3). Alone, it is not powerful enough to locate and identify MoS₂ flakes, so I use a separate confocal zoom lens to study the chips more closely before and after transfers. The lab acquired some donated optical equipment partway through my research in Summer 2016 and we were able to incorporate an additional lens which allowed a slightly closer magnification. We also mounted a digital camera hooked up to a monitor, useful for a wider angle view for use observing a larger area when making a transfer.

Senger and I briefly experimented with colored filters in our objective setup. We noticed that our red filter made differentiating regions of silicon and MoS₂ or graphene flake coated silicon easier. The filter's drawback however, was its tendency to make differentiating the thicknesses of MoS₂ flakes more difficult. This made it ineffective for our purposes, but it may be of use to others who wish to quickly identify a known-thickness transfer on an optically similar backdrop.



Figure 2.3: Transfer station.

2.6 Transfer Slide Mounting

Originally the transfer slide was mounted directly onto the aluminum clamp on the manipulator arm. This created problems due glass slides flexing when a torque was applied to one end, creating uneven contact areas on transfers as well as breaking multiple slides. To remedy this, I 3D printed a PLA plastic alternative mount that held the slides from both ends, more gently and with a better range of motion, shown in Figure 2.4.

Transfer Station Mounts

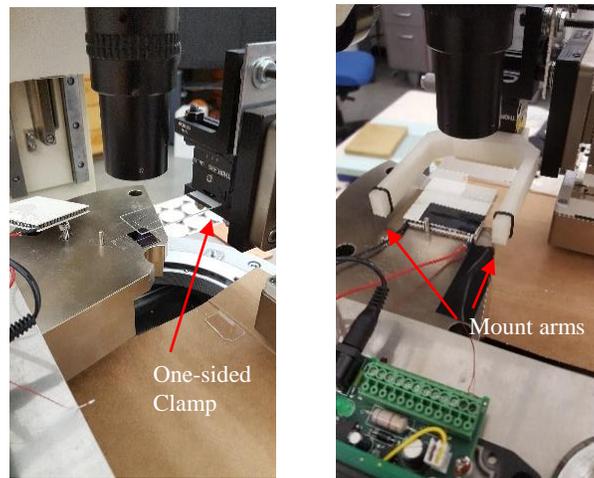


Figure 2.4: Original mount (left) and 3d printed mount (right).

2.7 Verification of Transfer Material and Thickness

I used several techniques to determine flake thickness and verify the material composition of transferred flakes. I primarily used Raman spectroscopy and atomic force microscopy (AFM) for these ends, with the help of Mitchell Senger. We used Raman spectroscopy in comparison with preexisting spectral data^[5] to first identify transferred exfoliated graphite (due to its more distinct peak signatures) then for MoS₂. This is a relatively quick way to determine the composition of a flake as well as whether or not it is few layer.

AFM is more time consuming, but allows us a much more detailed height map of transferred flakes. Sometimes the majority of a transferred flake is too thick for to display gate dependency, but it is possible to locate a thin enough patch to be studied.

2.7.1 Characterization Methods

In addition to an optical objective this project entailed the use of three other forms of microscopy; atomic force microscopy, Raman spectroscopy, and scanning photocurrent microscopy. Each having their own particular uses.

Atomic force microscopy relies on a nanoscale piezoelectric needle which sweeps device architecture, creating precise topographic maps. This method is fairly time consuming, however for experimentally determining the region to region thickness of a thin film device, it is extremely practical.

Raman spectroscopy consists of shining a monochromatic light onto a material and analyzing the resulting, emitted light, a minority of which will be shifted by its interaction with the material^[7]. Different materials and material thicknesses create distinct Raman spectral signatures. Experimental Raman spectra can be easily compared with other predetermined results for desired samples (i.e. a patch of bilayer graphene, a flake of monolayer MoS₂, etc.) Raman spectroscopy is significantly less time consuming than AFM and can quickly gauge the approximate thickness of devices.

Scanning photocurrent microscopy (SPCM) involves using a small laser spot to locally excite electron-hole pairs in a semiconductor. These excitons can generate a photocurrent if the electrostatic environment enables them to reach the connected electrodes before recombination occurs. For my purposes SPCM is the best way to experimentally determine if a device has photovoltaic or photothermoelectric properties^[13]. We used a 632 nm He-Ne laser for our tests, focused to a 1 micron spot size.

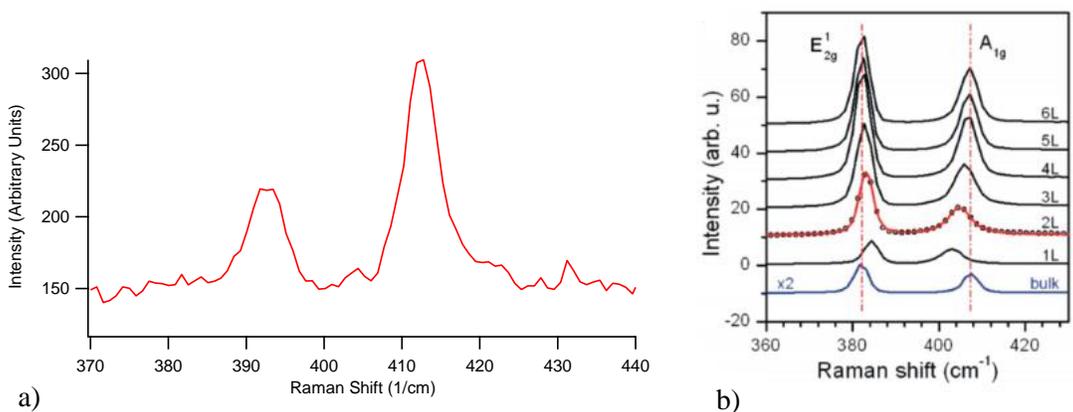


Figure 2.5: (a) Raman data from one of my MoS₂ samples. (b) Documented Raman data for few layer MoS₂ from another research group for comparison^[15].

Figure 2.5 shows the experimental Raman spectra for exfoliated MoS₂ which we compared with published Raman curves to from a related paper^[15]. The composition and thickness of graphite and MoS₂ flakes can be easily determined with this method and we used it primarily when developing the transfer process to insure MoS₂ and graphite flakes were successfully transferring and to gauge their approximate thickness.

2.7.2 Electrical Probing

We carried out the electrical measurements of my devices using an electrical probing station with tungsten contact pins. There are four pins; two for the gating bias and two for the source and drain electrodes. We additionally took SPCM current data for device 2 because it had by far the most prominent gate response, making it the best candidate for creating a photocurrent. Below in Figure 2.6 are the circuit setups for both standard electrical tests.

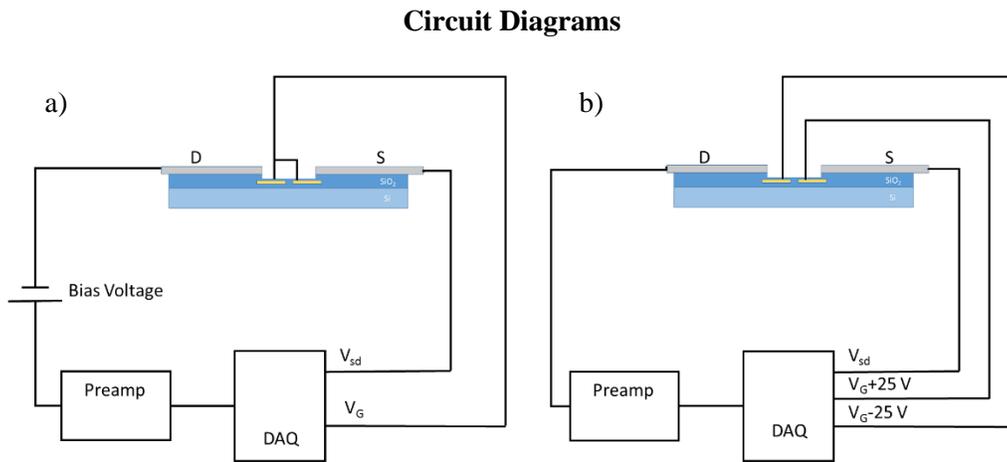


Figure 2.6: Probe station electrical diagrams for (a) transistor curves and (b) diode curves.

Part 3: Results and Discussion

Results include $I-V_{sd}$ curves, $I-V_G$ curves, and AFM images for both devices. Additionally, there are optical microscope images of both devices, and scanning electron images of similar devices for physical comparison.

Note: All figures in this section were created with the use of an Igor program written by Lee Aspitarte.

3.1 Images

Below in Figure 3.1 are two of the devices Senger and I made toward the beginning of the project. Note these are not the devices analyzed below as we were still developing our transfer process. However, they are useful in showing the precise device geometry. In Figure 3.1 (a), it is possible to see the very thin, transparent edge on the close side of the device, which is few layer MoS_2 . Figure 3.1 (b) is entirely bulk MoS_2 .

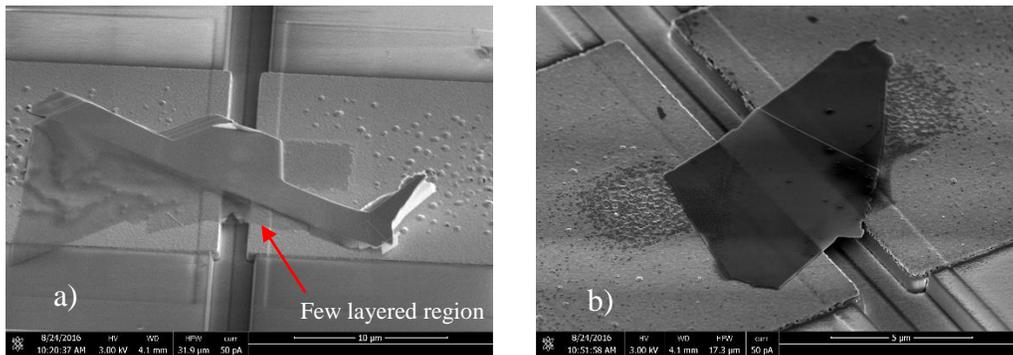


Figure 3.1: Scanning electron microscope images of early MoS_2 devices. The scale bars in the bottom right are (a) 10 microns and (b) 5 microns.

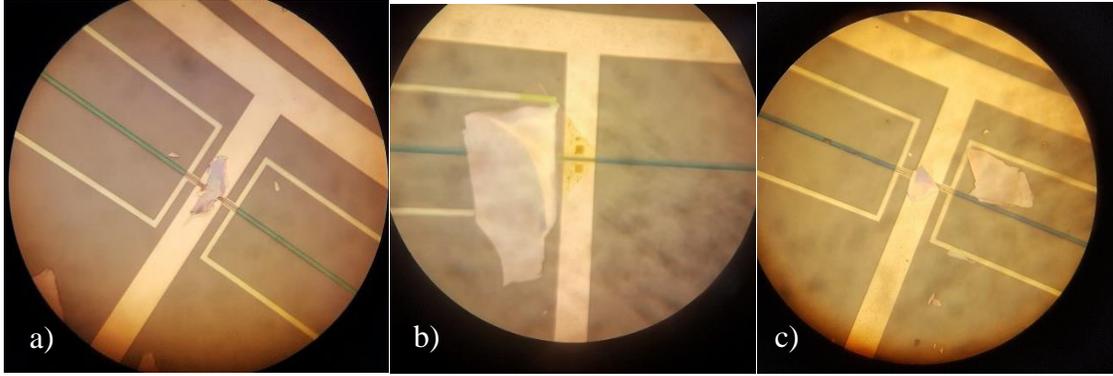


Figure 3.2: Optical images of MoS₂ device 1 (a), device 2 (b) device 3 (c).

Figure 3.2 shows devices 1, 2, and 3, in (a), (b), and (c) respectively, bridging the wide platinum source-drain electrodes. The flakes used in device 1 and 3 are small enough to fit entirely on top of the platinum, whereas device 2 was constructed with a much larger flake, of which only the thinnest triangular portion on the right is covering the contacts. We do not expect the conductivity of the bulk material to the left of device 2 to be sufficiently higher than the few layer patch as to redirect the current crossing the source-drain contacts.

3.2 I-V_G (Transistor) Curves

The resistivity of thin MoS₂ flakes can be affected significantly by their surrounding electric field. A strong enough electric field acting on a suspended flake of MoS₂ can effectively switch its resistance “on” and “off” creating a transistor through electrostatic doping. The electric field created by a gate voltage is typically only strong enough to affect the surface layers of a bulk TMD sample, generally causing insignificant change to the total device conductance. However, few layer devices, having a much larger surface area to volume ratio, are much more drastically affected by their electrical environment. Due to the strong light absorption qualities of many TMDs they are often useful in building photovoltaic devices. In these figures source-drain current response is plotted against gate voltage, where the two split gates are set at a constant potential.

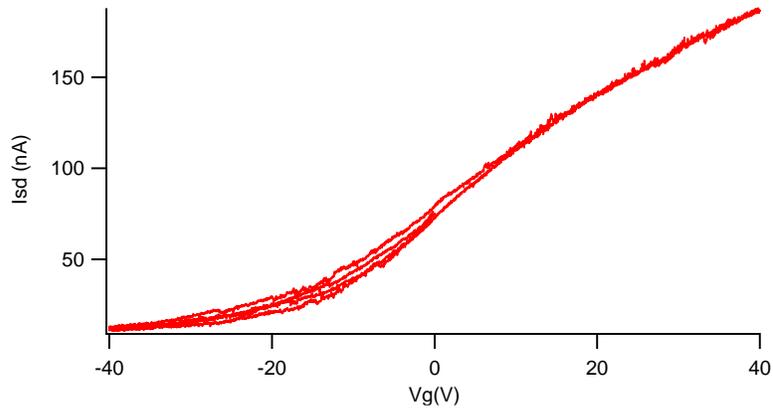


Figure 3.3: I- V_G curve of device 2 at 100mV source-drain bias. Both split gates are at equal voltage.

The I- V_G curve for device 2 is shown in Figure 3.3. The gate voltage was cycled between a plus and minus 40 V gating bias multiple times with a source drain bias of 100mV. The current roughly doubles at a +40 V gate voltage showing strong gate dependence compared to $V_G = 0$. Ideal conductivity would go to zero at zero gate voltage, making for a transistor curve, which is not the case here. Although at -40 V current drops to just a few nanoamps.

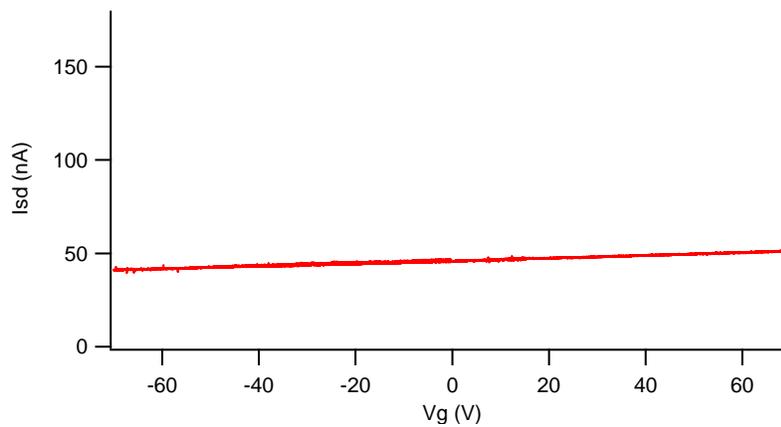


Figure 3.4: I- V_G curve for device 3 at 100 mV source-drain bias.

Device 1 failed to produce good electrical results, so to provide contrast with the few-layer nature of device 2 I constructed a third device to display the electrical behavior of bulk MoS_2 for contrast. Device 3 was constructed of a flake similar in color to device 1's, implying roughly equivalent thickness. This

device had a linear and very small I - V_G response shown in Figure 3.4. The device's conductivity changed very little, with current only increasing by about 4 nA, less than a 9% increase, at a high gate voltage ($V_G = 60$ V).

3.3 I - V_{sd} Curves

This section includes device's source-drain current response vs the split-gate potential difference across the source-drain electrodes (electrostatic doping). The ideal shape of this curve for a photovoltaic device is a diode curve, with source-drain current equal to zero for negative source-drain bias, and sharply increasing at a specific positive bias. Device 2 was the only device with strong enough field dependency shown in its I - V_G curve to be compared to a diode curve.

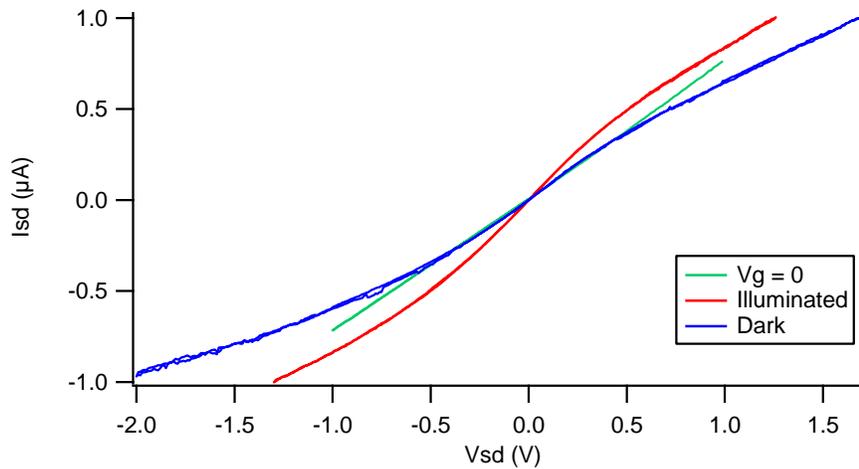


Figure 3.5: I - V_{sd} curves for device 2. The illuminated (laser 632 nm laser spot) and dark trials were at split gate voltage ± 25 Volts. The green curve is a control test at zero gate voltage

In Figure 3.5 above we see current increases as the bias voltage creates higher potential pushing charge carriers in larger numbers toward the source-drain electrodes. The illuminated I - V_{sd} curve for device 2 shows higher current than the dark I - V_{sd} as expected. Generally, in similar devices we expect incident light to excite electron-hole pairs, with holes and electrons to the upper conduction band and valence band respectively. In the presence of an electric field, the holes and electrons separate, electrons and holes moving toward opposite electrodes and increasing overall current.

In illuminated MoS₂ devices when electron-hole pairs are separated electrons become the dominant charge carriers while holes tend to become “trapped,” immobile in the material^[3]. This phenomenon is called a photodoping effect. Although not fully understood it results in higher photocurrents as trapped holes affect the flow of electrons through the material with a net gain of conductivity.

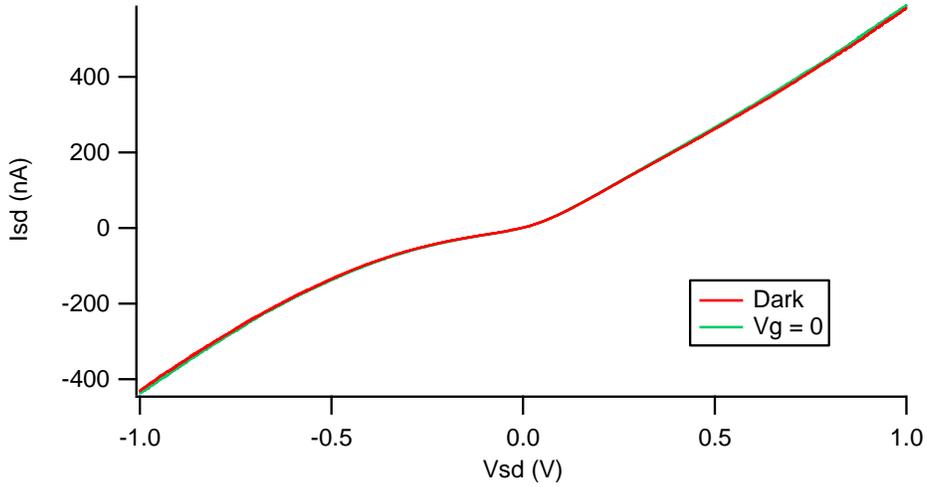


Figure 3.6: A dark (ambient light) I- V_{sd} curve for device 3 with split gate voltage is +/- 25 Volts and control test at zero gate voltage.

The dark I- V_{sd} curve for device 3 with one split gate at +25 V and the other at -25 V (Figure 3.6) is almost identical to its control test at $V_G = 0$. Because the current is almost imperceptibly affected by gate voltage, it is likely the difference between the two trials is only due to experimental uncertainty. The current appears marginally higher on the control test, which further supports the idea that this difference is only due to trial to trial error. There is no indication of a diode curve.

3.4 AFM Data

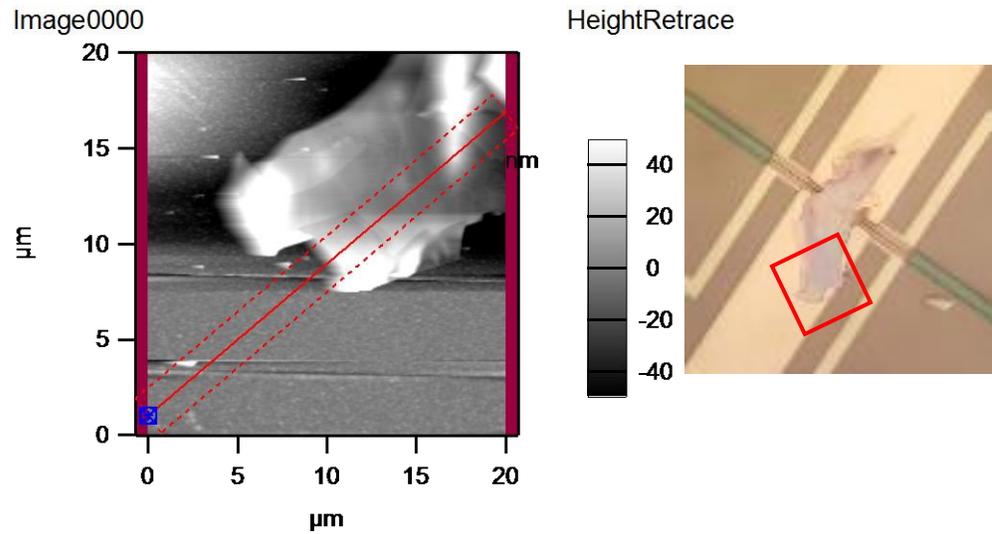


Figure 3.7: Atomic force microscope image of MoS₂ device 1. To the right is the optical image highlighting the approximate scan region for this AFM image.

The height of device 1, shown in Figure 3.7 averages around 40 to 50 nm above the substrate. This flake is thick enough that it has significantly varying topography (up to 110 nm above the substrate).

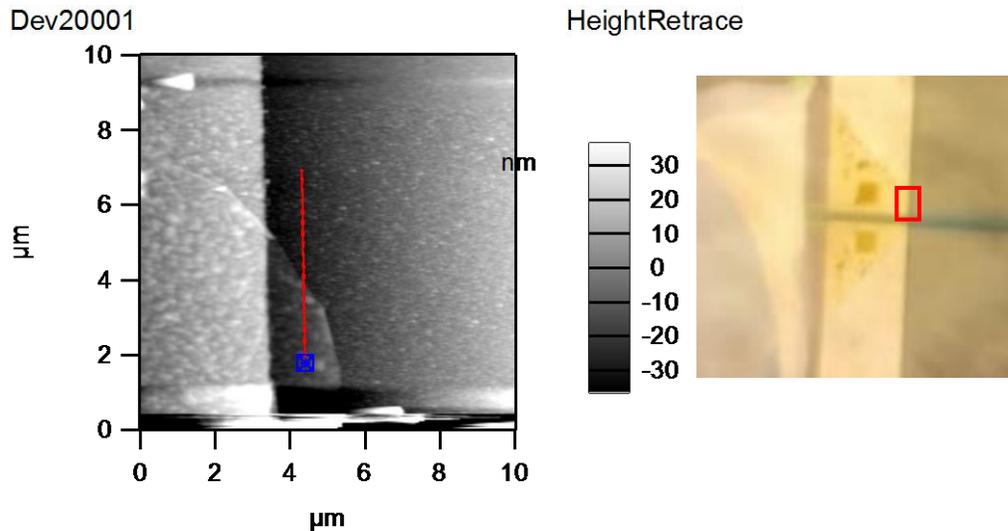


Figure 3.8: Atomic force microscope image of MoS₂ device 2 (right edge). The optical image on the right shows the approximate region of the AFM image.

Figure 3.8 is an AFM image of the right edge of device 2. The fin shaped region is where the MoS₂ flake extends beyond the platinum contact (the light gray leftmost third of the image). We took a height cross-section of this location because the SiO₂ is significantly smoother than the platinum contact, providing an easier height comparison.

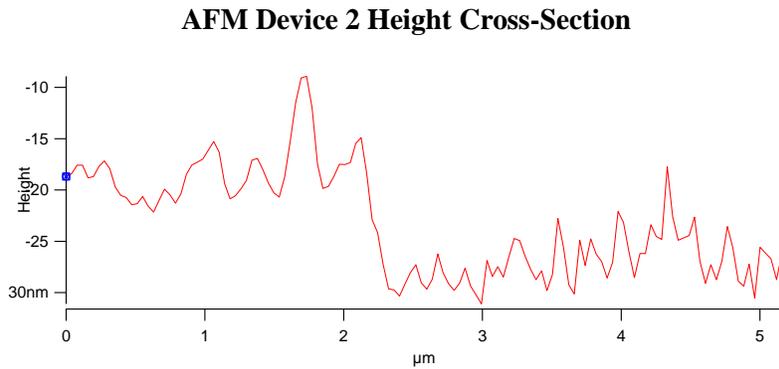


Figure 3.9: Cross sectional height map from Figure 3.8

Figure 3.9 shows the height plot directly mapping the red marking line from Figure 3.8. I took local height averages on and off of the MoS₂ and compared them to estimate flake thickness. This is how I made all my height estimates between both devices. In this height map I observed an approximate height drop of 5 to 10 nm from MoS₂ to SiO₂ substrate corresponding to device thickness. At 0.7 nm per layer this translates to 7 to 14 atomic layers of MoS₂.

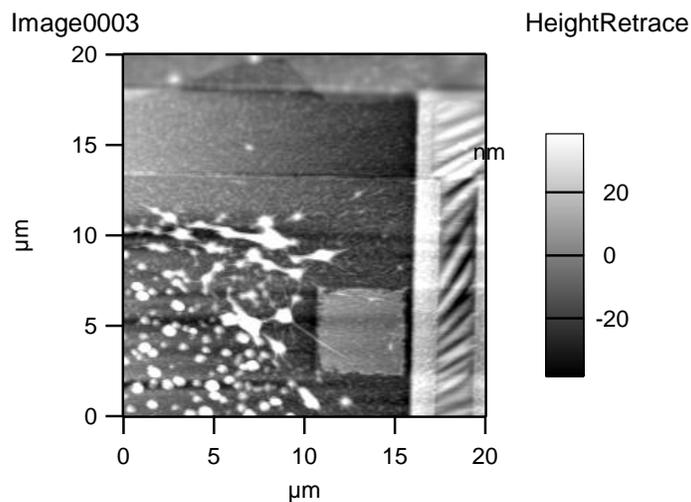


Figure 3.10: Atomic force microscope image of device 2 trench

Figure 3.10 shows a wider view of the left side of device 2. The vertical bar on the right edge of the image is the chip trench bridged with MoS₂. From this image, we can see that MoS₂ at this thickness (5 to 10 nm) is flexible enough to wrinkle like fabric when under strain. Although the boundary between the exposed platinum area and that covered in MoS₂ is not obvious in Figure 3.10, the bubbles on the platinum's surface on the upper right side of this contact appear more continuous (as if covered a sheet), compared with the discrete round shapes in the lower left corner.

Based on our combined electrical and AFM findings I estimate suspended MoS₂ flakes must be under 50 nm thickness begin to display gate-tunable resistance.

Part 4: Conclusion

4.1 General Findings

Throughout this project I successfully showed that it is possible to construct gated suspended MoS₂ devices using a simple dry transfer process. I found an approximate threshold thickness for the electric field's effect on device resistivity by comparing my devices. Device 2 showed strong gate dependence through a transistor curve as well as exhibiting a laser induced photoresponse. Based on AFM data device 2 is between 7 and 14 atomic layers thick.

4.2 Future Research

Given the time and resources, constructing many MoS₂ devices with ranging thicknesses would be a good method of discovering a more precise thickness threshold for gate dependency. That information could be useful in designing photovoltaic devices or heterostructures using MoS₂ or other TMDs.

The nature of hole trapping in illuminated MoS₂ devices still requires much further research. Researchers have yet to determine both the mechanism by which hole trapping occurs and its precise contribution to the photodoping effect.

The fabric-like characteristics of few layer MoS₂ shown in Figure 3.10 could use further study as well. I did not determine whether or not different transfer methods could avoid strain wrinkles, but it is possible that the MoS₂ could stay un-strained by removing the transfer PDMS from the destination substrate more symmetrically could. Qualitative information relating the wrinkling of MoS₂ of different thicknesses under different approximate strains could be useful in constructing layered devices without folds or air pockets.

4.3 Advantages and Disadvantages of the Dry Transfer Method

The dry transfer process offers an economical, deterministic, and time efficient method of assembling simple gated photovoltaic devices such as I have constructed. It also has potential for building simple heterostructures, however due to the uncontrolled nature of the transfers (roughly half of them being unsuccessful) it may be difficult to create a heterostructure of more than two layers.

The major drawback of this method is the reliance on TMD exfoliation yields, which vary widely on exfoliation conditions and are difficult to predict. Sometimes many exfoliations are required to optically identify transfer flakes suitable for transfer.

The flakes themselves can be precisely positioned for device construction, however it is impossible to deliberately construct devices of specific shape or thickness, this being a luck-of-the draw process.

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