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Title: Digitally-Programmable Switched-Current Filters

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David J. Allstot

Digitally-programmable filters have been an ongoing research topic for a number of years. The first such filters were FIR transversal filters using Charge-Coupled Devices (CCD's) and IIR recursive filters using switched-capacitor (SC) techniques. Although both techniques achieve excellent results, they require non-standard and/or additional IC fabrication steps. Low substrate doping is often essential to obtain high charge-transfer efficiency in CCD filters. This is contrary to the trend towards higher doping levels as MOSFETs are scaled. Switched-capacitor circuits require floating linear capacitors that add processing complexity. SC circuits also use voltage operational amplifiers which limit the maximum operating frequency and the minimum power supply voltage.

The recently introduced switched-current (SI) technique [1] is an attractive alternative for implementing digitally-programmable filters. SI circuits may be viewed as charge processors where Q = It as opposed to SC circuits wherein Q = CV. Hence, in SI circuits, current rather than voltage is the working variable, and time rather than a capacitance ratio is the precision quantity. No precision circuit elements are required. Therefore, a standard low-voltage scaled digital VLSI CMOS process may be used to implement analog sampled-data SI filters. As current is the working quantity in SI circuits, current signal amplification may be realized using simple current reflection techniques. Because of the low impedance nodes associated with CMOS current mirrors, higher operating frequencies are expected as compared with SC circuits. The low impedance nodes associated with the current amplifiers also suggest reduced power-supply coupling for precision mixed-mode applications.

In this study, we present design techniques for digitally programming a second-order SI filter section. While providing similar capabilities to the programmable SC filters [2], the SI circuits have an additional degree of flexibility for optimization in that AC signal currents and/or DC bias currents are programmable. In order to directly compare the SI and SC techniques, the programmable SI filter has been designed to the same specifications as the programmable SC filter of [2]. The programmable second-order section has 63 possible gain (G) values, 63 possible selectivity (Q) values, and 8 possible logarithmically-spaced center frequencies (ω_0) per octave.

Digitally-Programmable Switched-Current Filters

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

DIGITALLY-PROGRAMMABLE SWITCHED-CURRENT FILTERS

1. INTRODUCTION

There are several areas in analog signal processing requiring programmable filters. Vibrational analysis, adaptive filters, music synthesizers, formant speech synthesizers and tracking filters are a few of the applications. Namely, programmable filtering techniques are used where time-varying responses are required.

In the literature, there are many studies on designing programmable filters spanning more than a decade. Apparently, the techniques used for providing a controllable response for the filter under inspection have changed a lot following technology improvements and new circuit techniques. The very first studies were aimed at fulfilling the requirements of a relatively small market. The designs were constructed with discrete active filters or hybrid universal active filters, and usually required precision components and component trimming. This approach was not a cost-effective solution to the problem, and was time-consuming in the sense of spending engineering time on design of filters instead of on overall system design. Second generation solutions came out with the CCD (Charge-Coupled Devices) technique, allowing us to design transversal filters on a chip [3],[4]. In the late 70's and the early 80's, the SC (Switched-Capacitor) techniques were introduced [5]. This brought a new aspect to the whole discussion with their suitability of integrating both analog and digital functions on one chip, wide frequency range, excellent temperature stability, and significant reduction in chip area. The first programmable design employing SC techniques was an electrically-programmable switched-capacitor filter which is also the inspiration of this work [2]. In this study, the input gain (G), selectivity (Q), and center frequency (ω_0) of a second-order lowpass filter were programmed by digital control signals. In chronological order, it was followed by a real-time programmable switched-capacitor filter which basically provided four independent real-time programmable second-order SC filters on a single chip with digitally programmable Q and ω_0 [6]. Another

example was dealing with a digitally-programmable SC universal active filter/oscillator [7]. The device was able to perform all five basic filter types (lowpass, bandpass , highpass, bandreject and allpass) as well as providing a sine wave oscillator.

The purpose of designing a SI digitally-programmable filter in this study is mainly to compare its performance with the one designed with SC technique, and to investigate methods which would allow us to provide a direct mapping between these techniques. Another goal is to point out the advantages and disadvantages of SI techniques, and hopefully to propose solutions to any problems.

In the second chapter, the SI technique is introduced and discussed in terms of realizing essential analog signal processing blocks, such as inverting current amplifiers, summers, subtractors, and integrators. The advantages and disadvantages are also examined.

The third chapter includes an analysis of a singly-terminated second-order RLC lowpass filter. The signal flowgraph technique which is also applied to SC circuit synthesis is introduced from the SI point of view. The criteria which are observed in determining the component values of the prototype are given.

The fourth chapter summarizes the design considerations. We also present the basic functional blocks used in implementing the prototype such as the input gain programming block, the selectivity programming block, and the center frequency programming block in which two methods, ω_o programming with transistors and sampling frequency programming are employed concurrently.

Conclusions are given in the fifth chapter.

2. THE SWITCHED-CURRENT CIRCUIT TECHNIQUE

2.1. Advantages of SI Circuits

Switched-Current (SI) Circuits are attractive to use in analog signal processing for several reasons. First, they promise a lower-voltage operation because of their simple current mirroring nature. Second, the limitations in achieving high-frequency operation are decreased by having low impedance nodes due to diode-connected transistors. Third, providing a better power-supply immunity does not require as much effort as in the other techniques due to the low-impedence nodes. Finally, elimination of the need for using extra steps in standard CMOS process to implement precise components such as capacitors in SC circuits is much more convenient. All of these features of SI circuits will be examined in this section.

2.1.1. Low Voltage Operation

The general trend to scale the sizes of MOSFET devices down to sub-micron levels leads engineers to design circuits operating with very low power supplies. In this manner, the SI technique is very advantageous since its basic block, a simple current mirror, requires very low power supplies to function as desired. In fact, the essential voltage difference between its power supplies is determined using Fig. 2.1 by the sum of the gate-source voltage of M_1, which provides the gate-source voltage sufficient to bias M_2 in the saturation region. Assuming that the drain-source saturation voltages of the p and n transistors are equal, the minimum power supply voltage is equal to the threshold voltage of the NMOS devices plus twice V_{DSsat} ($V_{TH}+2V_{DSsat}$) which is typically about 1.5 Volts.

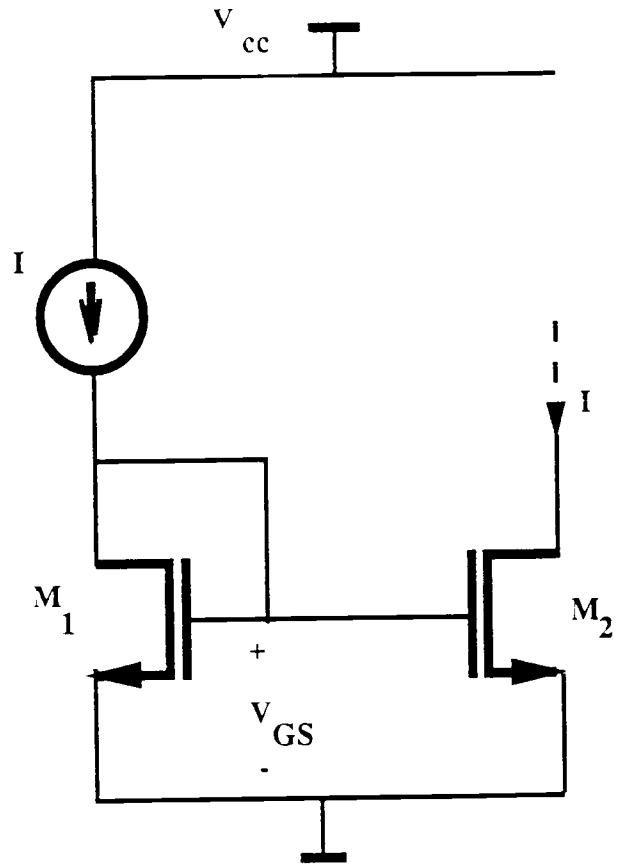


Fig. 2.1. Basic Current Mirror Structure in SI Circuits.

2.1.2. High-frequency Operation

One of the most important properties of SI circuits is their potential capability to operate at higher frequencies. This is expected since the SI circuits consist of simple current mirroring blocks with wide small-signal bandwidths . A comparison of a simple current mirror frequency response with a typical opamp used in designing integrators in SC circuits is demonstrated in Fig. 2.2. As seen from the figure, an opamp provides higher gain in the passband, but drops 3 dB down at a cutoff frequency ω_{c1}, whereas a current mirror maintains a gain of 1 in the passband up to the unity-gain bandwidth (ω_{c2}).($\omega_{c2} >> \omega_{c1}$)

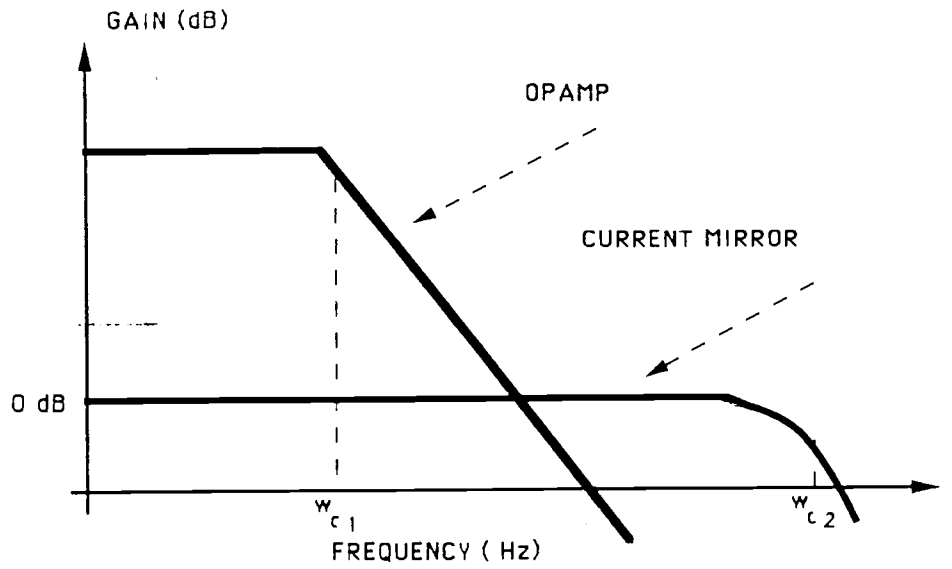


Fig. 2.2. Comparison of Frequency Responses of a Simple Current Mirror and an Opamp.

2.1.3. Power-supply Immunity

One of the difficult problems in opamp design is to improve the power-supply rejection ratio (PSRR) of the circuit. In SI circuits, this problem is reduced significantly. An examination of a track-and-hold sub-block (Fig. 2.3) shows the decreased effect of the noise which is coupled from the power supplies.

There are two mechanisms involved in this phenomena. The first is the noise coupling from the reference current mirror side. Assuming that the current source connected to the M_1 transistor is ideal, it can be shown that the noise on the positive power supply does not reach the gate of M_1 because of the infinite impedance looking up into the ideal current source from the drain of M_1. The noise on the negative power supply is also ineffective

due to the fixed gate-source voltage of the diode-connected transistor which varies only as a function the drain current which is in this case set by the ideal current source. As the noise forces the source of the transistor to shift up and down, the gate node of M_1 also shifts simultaneously to keep V_{GS1} constant. Hence, the drain current is unaffected by the source noise voltage.

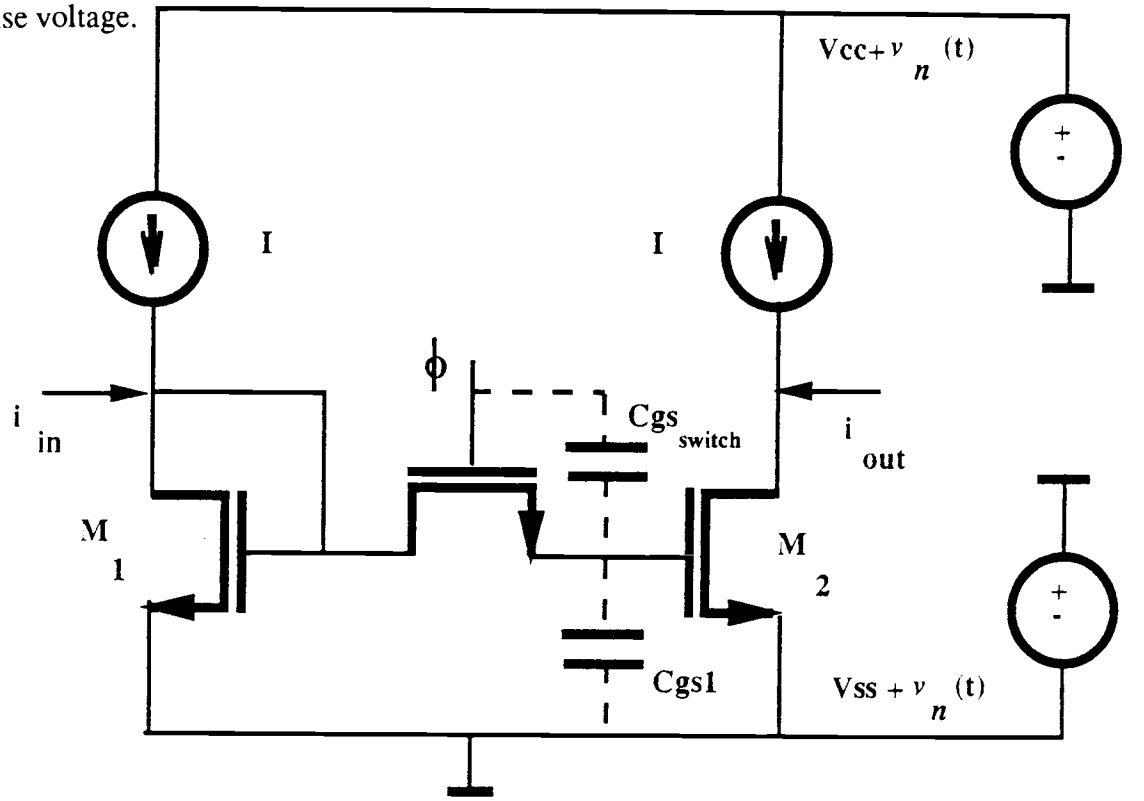


Fig. 2.3. Simple Current Mirror with the Noisy Power Supplies.

The second noise coupling path is due to the switch whose gate is connected to the power supplies depending on whether it is on or off. The gate-source parasitic capacitance (Cgs) of the switch forms a capacitive divider network with the gate-source parasitic capacitance of the mirroring transistor M_2. Therefore, the noise voltage on the power supplies can modify the gate-source voltage of M_2. Since these two gate-source capacitances are comparable, the impact of this power supply coupling mechanism is most significant. One of the ways to achieve better PSRR results is to use separate, regulated power supplies for the gates of the switches. In other words, the clocks should be produced by a separate circuit whose power supplies are different than the ones used in the

track-and-hold circuit. Another way to increase PSRR is to increase the area M_2 of relative to the switch transistor which results in decreased frequency capability.

2.1.4. Standard CMOS process

Another important advantage of SI circuits is their suitability for use with conventional digital technologies. As opposed to the need for implementing precise linear capacitors on the chip in SC circuits which requires a couple of extra masks in addition to a regular CMOS process, SI circuits can be implemented by using regular CMOS transistors as in a standard digital technology.

2.2. Switched-Current Techniques

2.2.1. Simple Current Mirror

Fig. 2.4 shows the simple current mirror of interest. Basically, as M_1 and M_2 are operated in saturation, the drain current of I_1 sets a gate-source voltage of M_1 and consequentely the gate-source voltage of M_2, and then is mirrored to the drain of M_2 according to the ratio of $(W/L)_2/(W/L)_1$. The relationship between the I_1 and I_2 can be written as follows

$$I_1(W/L)_1 = I_2(W/L)_2$$

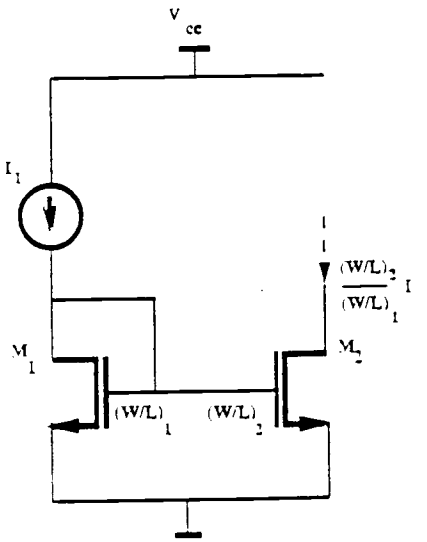


Fig. 2.4. Simple Current Mirror.

2.2.2. Inverting Current Amplifier, Summer and Subtractor

A switched-current block summarizing the basic arithmetic operations of inversion, summation and subtraction required in general signal processing operation is shown in Fig. 2.5 using currents as the input and output variables.

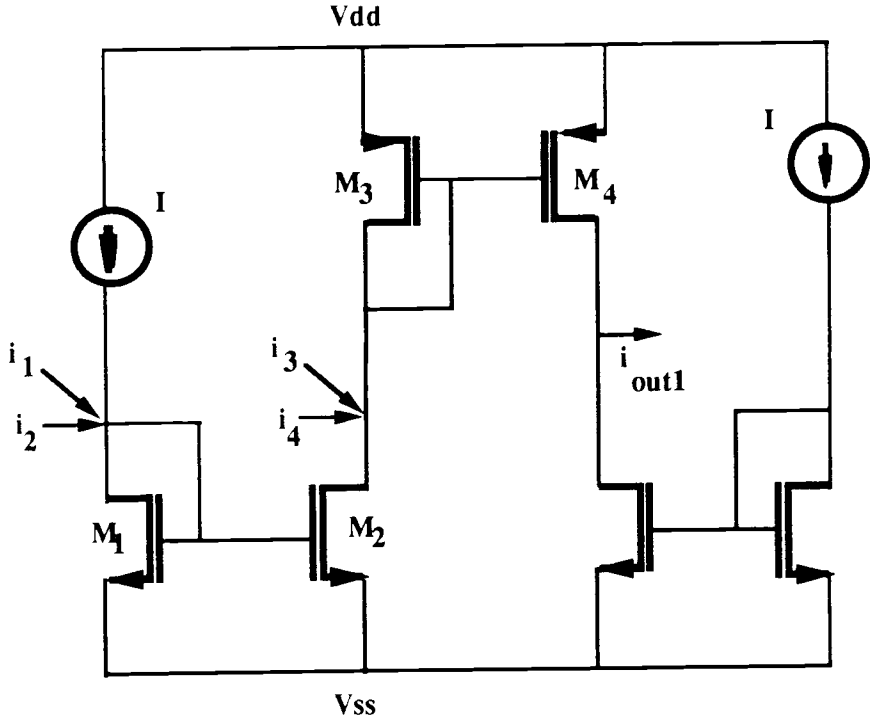


Fig. 2.5. Current Amplifier for Inversion, Summation and Subtraction in SI Circuits.

The configuration differs from a simple current mirror by the injected small signal currents transmitted between the modules. This additional current modifies the gate-source voltage of the diode-connected transistors (M_1 and M_3) and is taken out into the next stages. Obviously, signal currents larger than the biasing currents cannot be processed since M_1 is no longer turned on when V_{GS1} is lower than V_{TH}.

The total signal current at the output is given as

$$i_{out1} = i_1 + i_2 - i_3 - i_4 \qquad \text{(Summation and subtraction)}$$

2.2.3. Current Amplification and Scaling

In SI circuits, scaling is reduced to the simple task of changing the ratios of the mirroring transistors (Fig. 2.6). It should be mentioned that the biasing currents should also be scaled with the same ratio to provide constant current density for operating each transistor in the saturation region.

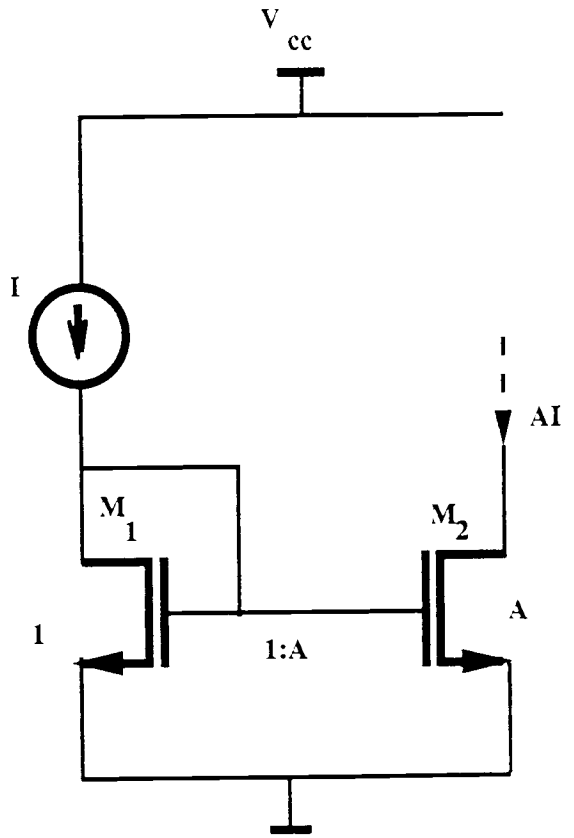


Fig. 2.6. Scaling in a Simple Current Mirror.

Fig. 2.7 shows a current amplifier used to obtain a scaled replicas of a signal current i_{in}. This configuration is used to achieve programmability in this design. As transistors of different scale factors from A_1, A_2 to A_n are switched in, the biasing currents are also

changed by the same scale factor. The output current is available in a scaled and inverted version from the common drain of the scaling transistors.

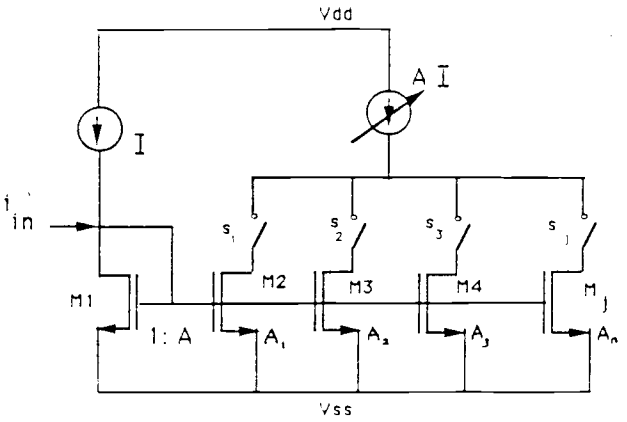


Fig. 2.7. A Current Amplifier with Scaled Mirroring Transistors.

2.2.4. Track-and-Hold Circuit

To complete the set of operations included in analog signal processing, another essential operation is the track-and-hold function. In SC circuits, this is accomplished by processing precise charge packets, and consequently setting up precise voltages according to the equation Q=CV. In SI circuits, signal currents controlled by precise clocks are used to assign charge packets (Q=It) for transmission.

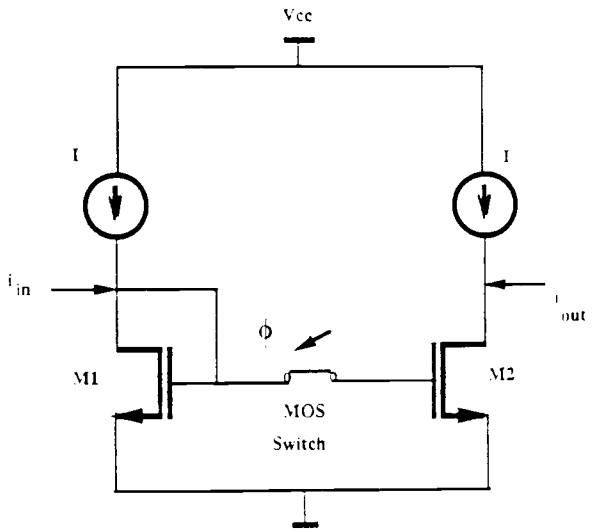


Fig. 2.8. Tracking Mode in an SI Circuit.

"Track" Mode: In Fig. 2.8, suppose that the W/L ratios of M_1 and M_2 are equal. At phase ø, the switch which is simply an NMOS transistor, is closed, and the signal current sets a V_{GS} voltage which also charges the input parasitic capacitance C_{gs2} of M_2. Hence, $i_{out}(t) = - i_{in}(t)$; i.e., the output current follows or "tracks" the input signal current with signal inversion.

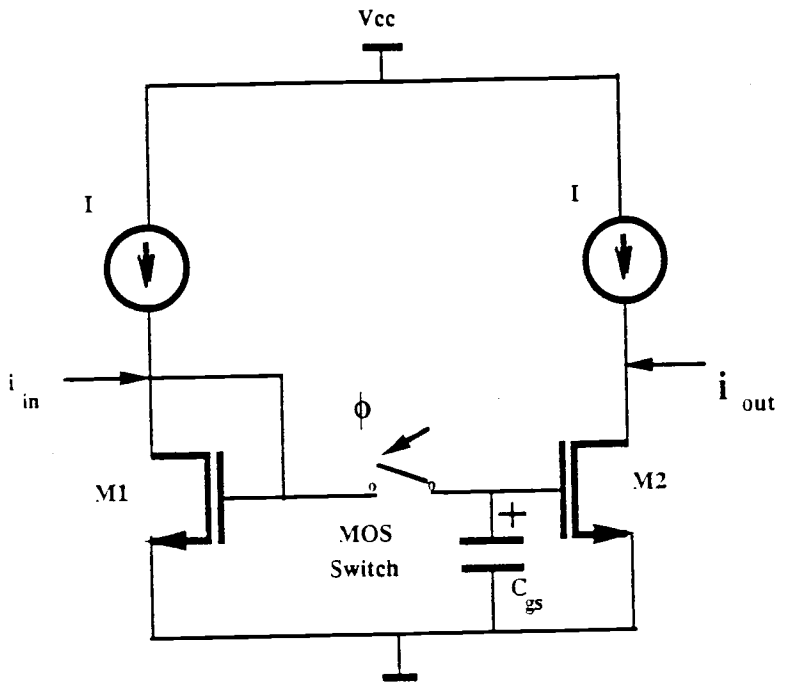


Fig. 2.9. Holding mode in an SI Integrator.

"Hold" Mode: As shown in Fig. 2.9, at time=T at the end of phase ø. the switch is turned off to disconnect the signal path between M_1 and M_2, and the output current is held constant as a result of the constant gate-source voltage stored on the non-critical capacitance, Cgs2. Assuming that there is no leakage current discharging Cgs2, and consequently no change in the stored charge, the drain current of transistor M_2 becomes a superposition of its biasing current and the signal current sampled at time=T and stored on Cgs2 at the end of phase ø. Hence, $i_{out}(t) = - i_{in}(T)$.

2.2.5.Basic Current Integrator

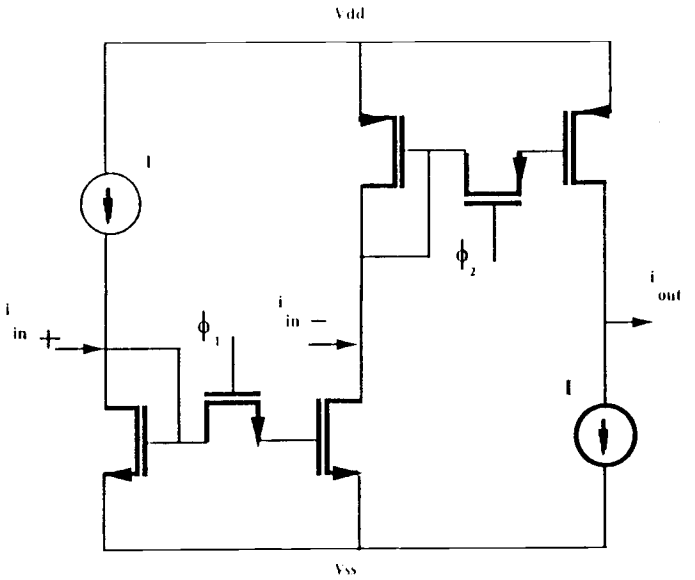


Fig. 2.10. Half-Delay and Full-Delay Realization in SI Circuits.

In this section, a basic current integrator is examined by emphasizing the similarities and dualities between the SC and SI techniques. First of all, for realizing an integrator, both half and full-delay integrations must be provided. Fig. 2.10 demonstrates the realization of these two functions using the SI technique. The transfer function of a differential input SI integrator with a scaled output given in Fig. 2.11 can be written as follows: First, the feedback loop is broken, and the feedback current is considered as a delayed input signal. Then, the scaled output is expressed as a function of feedback current (i_f):

$$i_O = A\, i_f$$

$$i_O = A\,[\, z^{-1}(i_{pos} + i_f) - z^{-1/2}\, i_{neg}]$$

By inspection and assuming that i_f is sampled on ϕ_1,

$$i_O = \frac{A\, z^{-1}}{1 - z^{-1}}\, i_{pos} - \frac{A\, z^{-1/2}}{1 - z^{-1}}\, i_{neg}$$

where A is the scaling factor.

As can be seen from the equation above, the current applied to the positive input of the differential-input SI integrator is delayed by one period (Full Delay), whereas the current applied to the negative input is delayed by half of a period (Half Delay).

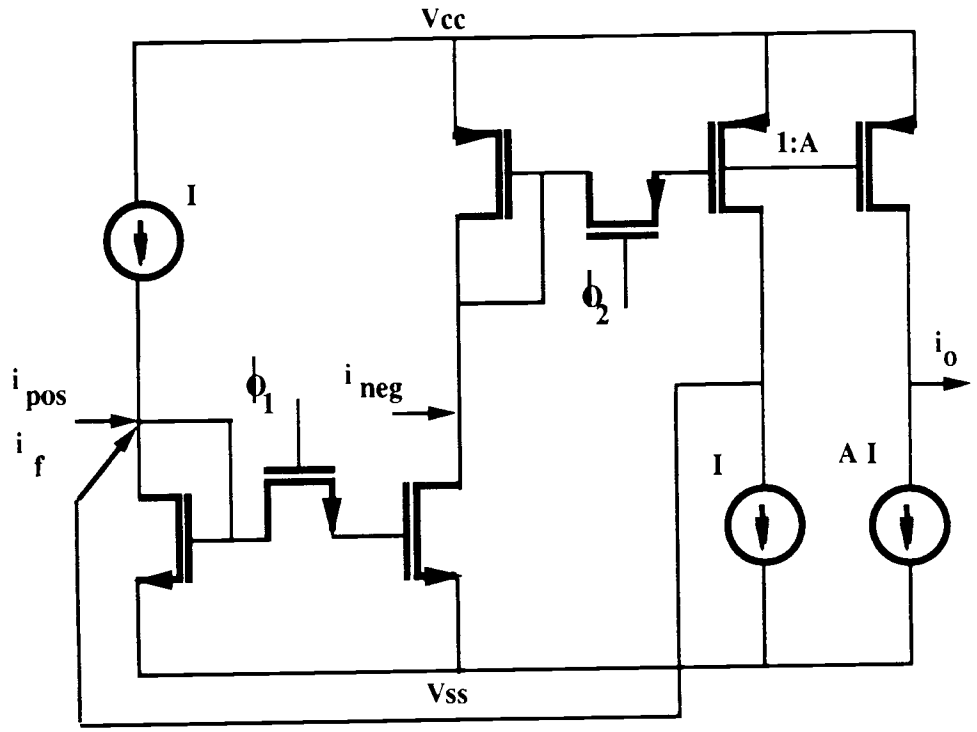


Fig. 2.11. Differential input-switched current integrator with scaled outputs.

Observing the structure of the transfer function above of an SI integrator, one can conclude that there are many dualities between SI and SC techniques. In fact, the derived transfer function is not really different than the one for an SC integrator except that current are the input and output variables in an SI integrator, whereas voltages are in an SC integrator.

The equation for a differential input SC integrator is given below as the output voltage is sampled on $\emptyset_1$ (Fig. 2.12).

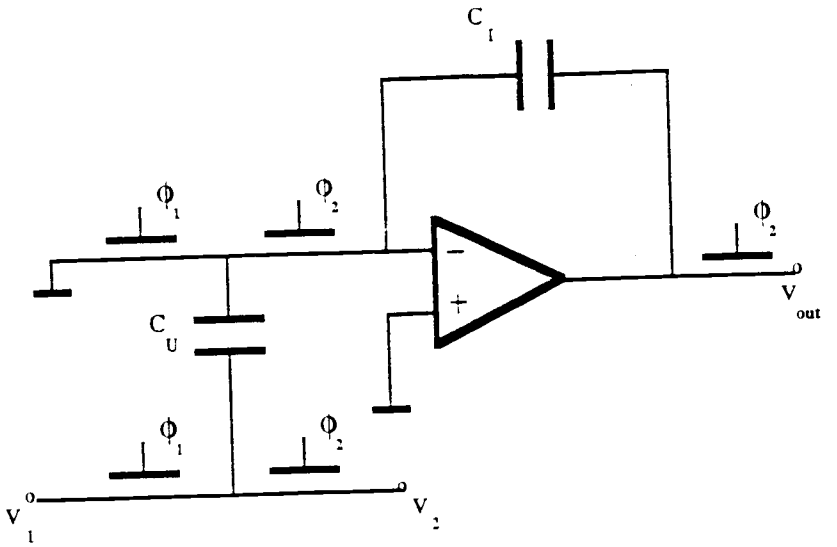


Fig. 2.12. A parasitic-insensitive differential input SC integrator .

$$V_{out} = \frac{(C_U/C_I)\, z^{-1}}{1 - z^{-1}} V_1 - \frac{(C_U/C_I)\, z^{-1/2}}{1 - z^{-1}} V_2$$

By comparing these two equations, it can be observed that there is a direct mapping between SC and SI circuits. The scaling factor in SI circuits corresponds to the (C_U/C_I) capacitance ratio of SC circuits. As a result of this mapping, one can conclude that all the studies which have been done in the SC domain could be transferred to the SI domain.

However, there are certain differences between these techniques due to the use of voltage or current as the working medium. It should be emphasized that in the SI integrator, the feedback output current is not used more than once as another input. Instead, each output signal current is reproduced through mirroring transistors so that separate currents are transmitted to each of the other blocks. Namely, all the output currents must be obtained separately whereas, in a SC integrator, the opamp output can drive many inputs simultaneously. On the other hand, while summation requires a lot of circuitry in SC

integrators, this can be performed in SI integrators by simply connecting the inputs to the summing nodes.

2.3. Disadvantages of SI Circuits

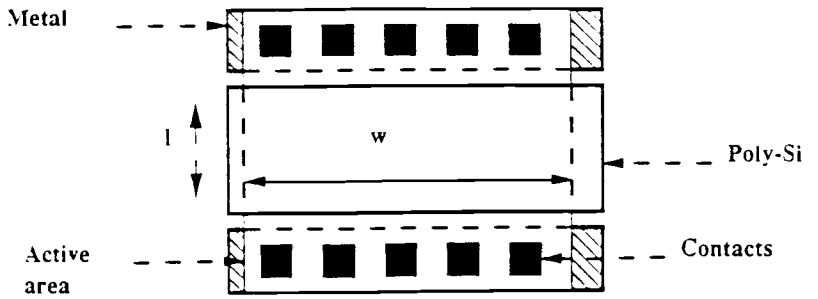
2.3.1. Mismatches

One of the significant factors determining the achievable accuracy in SI circuits is the success in matching the MOSFET transistors. Geometrical resolutions, edge effects, and temperature dependency of the process parameters, etc., are some of the reasons for the mismatches.

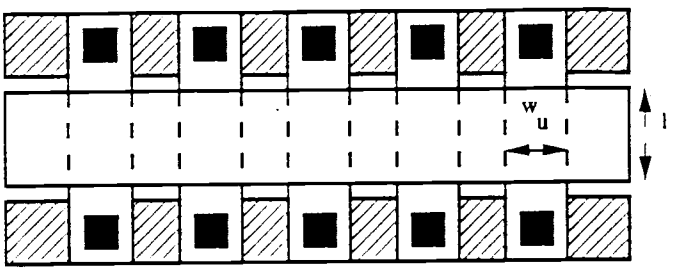
In the simple current mirror which is repeatedly used in the SI technique, the drain current of M_1 is mirrored according to the ratio given below

$$\frac{I_2}{I_1} = \frac{k_2'(W_2/L_2)\ (V_{GS} - V_{T2})^2\ (1+\lambda_2 V_{DS2})}{k_1'(W_1/L_1)\ (V_{GS} - V_{T1})^2\ (1+\lambda_1 V_{DS1})}$$

The first thought is to bias two transistors so that they have the same drain-source voltages, ($V_{DS1} \approx V_{DS2}$). Secondly, the impact of the lambda terms is minimized by using longer devices and cascoding techniques. It is not a surprise to obtain better matching in larger devices, yet the speed versus accuracy tradeoff appears as a disadvantage in most cases. Based on previous studies on MOS capacitors [8], for a comparable accuracy with the SC circuits, the length of the mirroring devices in the SI circuits should be chosen as 25 μm [8], which is impractical in many applications due to the area, power, and speed constraints. Thus, as a compromise between speed and accuracy, the lengths of the mirroring transistors are selected as 10 μm for this particular design.



Regular layout of a transistor



Layout of the same transistor with the unit-sized parallel transistors

$w = 5w_u$

Fig. 2.13. Common-Centroid techniques.

Lastly, unit-cell and common-centroid layout techniques may be used to help reduce systematic edge-effects. In processing, impacts of the etching resolutions vary for different geometries. Therefore, there is a potential problem in precise scaling of mirroring transistors, which limits the accuracy which can be achieved by SI techniques. In this design, as a precaution to minimize edge-effects, all mirroring transistors are formed as parallel-connected combinations of "unit-cell" transistors with a (W/L) ratio of 6 μm / 10 μm. Another method aims to solve the problems of the threshold voltage and other process parameters variations due to the oxide thickness linear gradients on the wafer surface. To cancel the variations due to linear gradients, the active regions are formed in two pieces surrounding the same core. This common-centroid technique is not used in this design because of its complexity and area constraints.

2.3.2. Clock Feedthrough

In general, clock feedthrough voltage is the error voltage at the output sampling node due to overlap capacitors of the switching transistor (Fig. 2.14) and channel-charges accumulated in the canal of the on-switch.

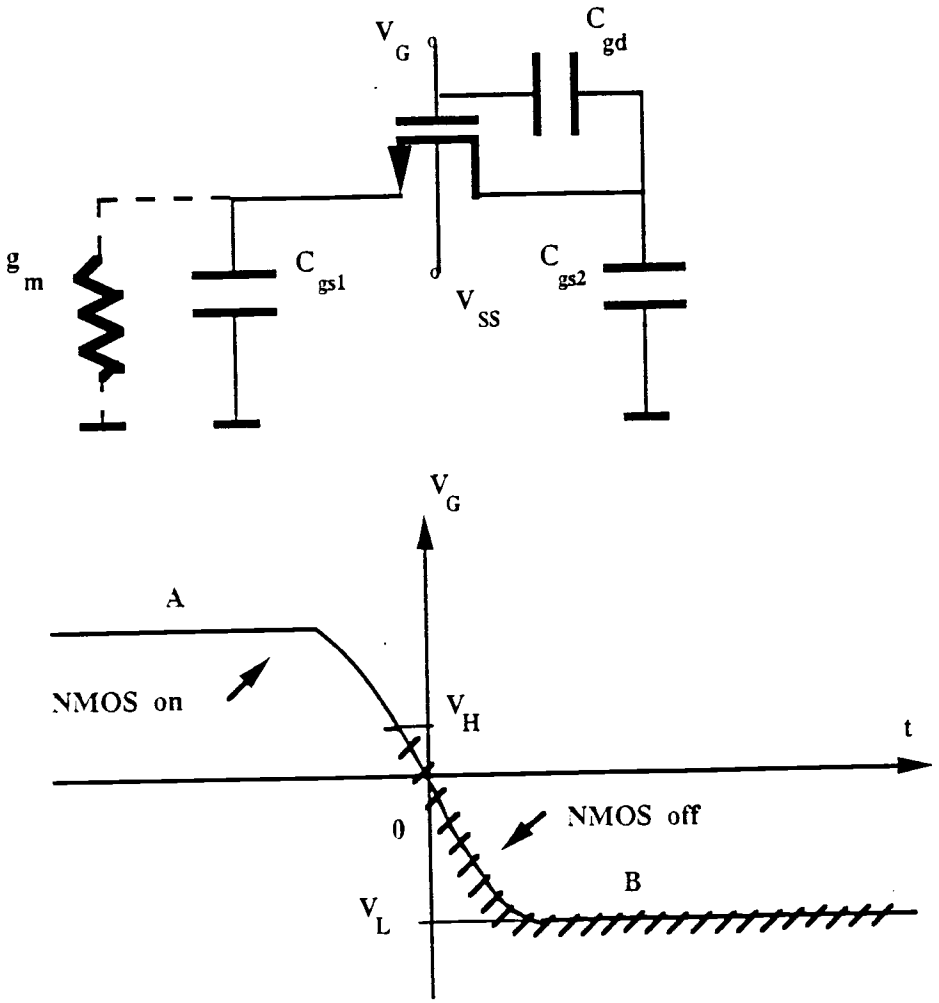


Fig. 2.14. Clock Feedthrough.

During interval A, when the switch is turned on in Fig. 2.14, the total induced channel charge is

$$Q = C_{ox}WL\,(V_{GS} - V_T)$$

If $V_G(t)$ turns off slowly, then almost all of the channel charge flows into the high conductance (g_m) node resulting in no feedthrough error due to channel charge on C_{gs2}. If $V_G(t)$ turns off quickly, then the channel charge divides equally between C_{gs1} and C_{gs2} resulting in a feedthrough voltage due to channel charge of

$$V_{fc} = \frac{Q}{2C_{gs2}} = (1/2)\,C_{ox}WL\,(V_{GS}-V_T)$$

As $V_G(t)$ is reduced, the switch turns off at the point where $V_G(t)=V_H$ and remains off until $V_G(t)= V_L$ as shown. In this case, the feedthrough voltage is due only to the overlap capacitance [9],[12]-[13].

$$V_{fo} = \frac{C_{gd}}{C_{gd} + C_{gs2}}\,(V_H-V_L)$$

In the general case, the total clock feedthrough voltage is given as

$$V_{fe} = V_{fo} + V_{fc}$$

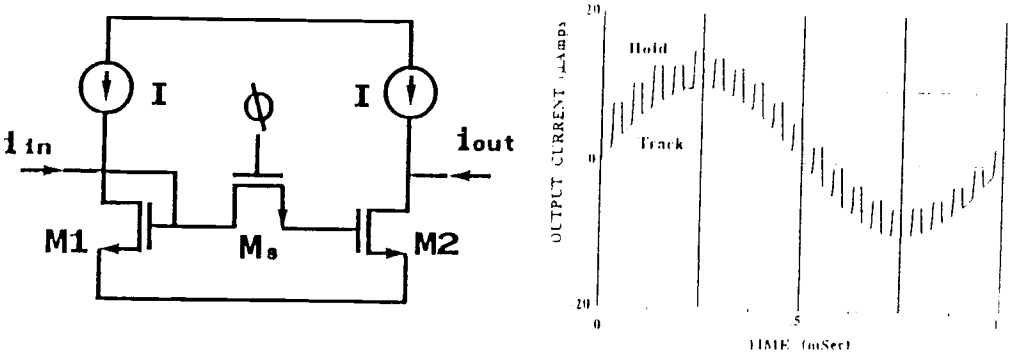


Fig. 2.15. Clock feedthrough in a track-and-hold circuit and SPICE results.

In SI circuits, the effect of the switch channel-charge (Fig. 2.15) is not a serious concern because the impedance looking into diode-connected M_1's gate is much lower than the impedance looking into M_2's. This can be noted as an advantage of SI circuits since diode-connected devices create low-impedance nodes. Nevertheless, the comparability between C_{gd} and C_{gs2} introduces a disadvantage to the SI circuits. The clock voltage couples to the signal path thru the capacitive network consisting of parasitic capacitances of the switching transistor and the mirroring transistors. The impacts of clock feedthrough to the total harmonic distortion will be examined in Section 2.3.3 with the other factors causing distortion.

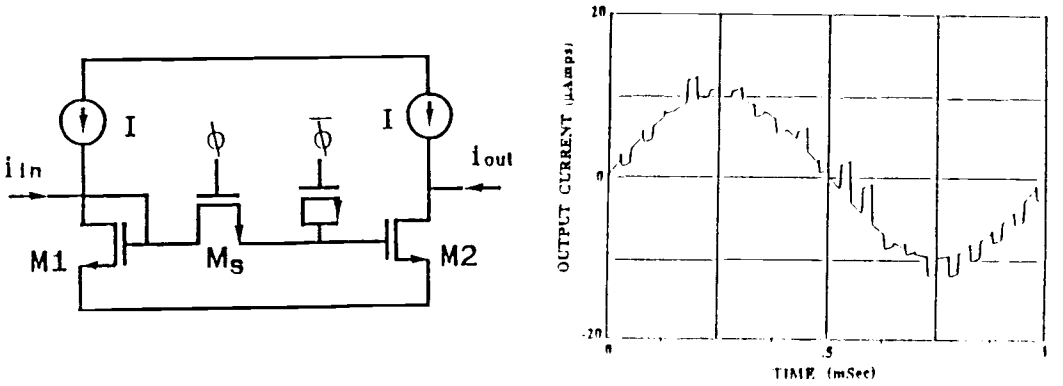


Fig. 2.16. Suggested Circuits for Clock Feedthrough Cancellation with Dummy Switches and SPICE results.

Some techniques have been suggested to solve the clock feedthrough problems in SC circuits such as using dummy switches [12]-[13] (Fig. 2.16), and by adding additional clock phases and controlling them in a way to cancel out the clock feedthrough. Unfortunately, these techniques do not result in complete cancellation because of difficulties in precisely controlling interactions between clock phase edges. However, ongoing studies [9] have shown that the clock feedthrough problem exists but may be solvable in SI circuits. Fig. 2.17.a and Fig. 2.17.b demonstrate a cancellation technique and SPICE results for SI circuits which is different than the ones for SC circuits which require more than one critically-timed clock phase. This replication and subtraction technique is able to reduce feedthrough currents in a track-and-hold SI circuit more than 30 dB. Unfortunately, it helps only the cancellation of the DC offset error term, but not the AC gain error since there is no signal current involved in this technique.

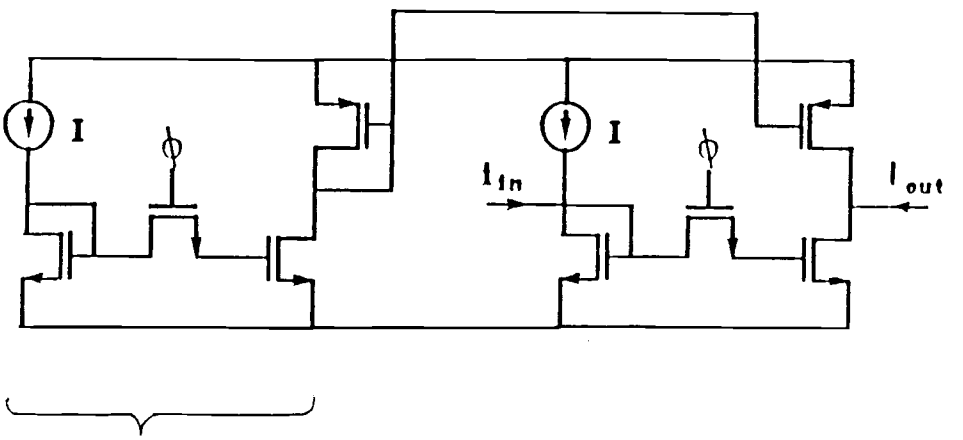


Fig. 2.17.a. Clock Feedthrough Cancellation Technique with the Proposed Circuit.

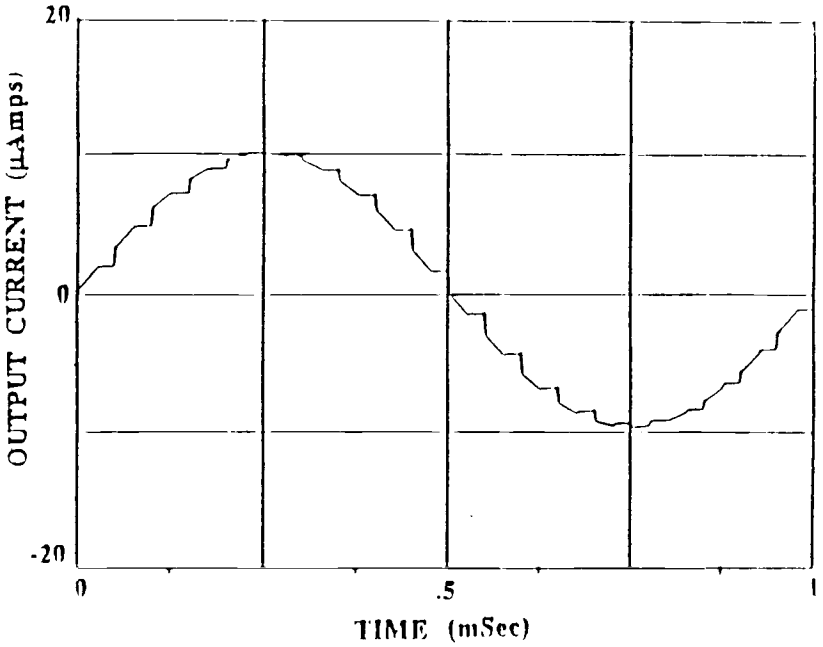


Fig. 2.17.b. SPICE Results of the Proposed Circuit.

The clock feedthrough voltage and current equations are examined as Section. 2.3.3 as they related to the different sources of harmonic distortion.

2.3.3. Harmonic Distortion

Harmonic Distortion in a Simple Current Mirror: As a result of the mismatches in threshold voltages, V_T, the W/L ratios, transconductance parameters, k', and channel-length modulation parameters, λ, the drain current equation for a simple current mirror where both transistors are in saturation exhibits harmonic distortion. For a first-order estimation, assuming that the difference between the threshold voltages is given as ΔV_T, the harmonic distortion products can be derived from the following equations as

$$I_2 = (k_2'/2)\,(W/L)_2\,(V_{gs2} - V_{T2})^2 \text{ where } V_{gs2} = V_{GS2} + \upsilon_{gs2}$$

By setting V_{gs} to

$$V_{gs} = V_{T1} + \left[\frac{2(I+i)}{k'(W/L)}\right]^{1/2}$$

and substituting in the first equation,

$$I_2 = (I_1+i) + (k_2'/2)\,(W/L)\,(\Delta V_T)^2 + \frac{2\Delta V_T\, I\,(1 + i/I)^{1/2}}{(V_{gs}-V_{T1})}$$

Using the binomial expansion, the expression for I_2 can be rearranged as follows

$$I_2 = I\left(1+\frac{\Delta V_T}{V_{gs}-V_{T1}} + \frac{2\Delta V_T}{V_{gs}-V_{T1}}\right)$$

$$+ I\left[\,1+\frac{\Delta V_T}{V_{gs}-V_{T1}}\,(i/I) + \frac{2\Delta V_T}{V_{gs}-V_{T1}}\left[\,-\frac{(i/I)^2}{8} + \frac{(i/I)^3}{16} - \frac{5(i/I)^4}{128}\cdots\right]\right.$$

It can be observed that the drain current of M_2 is harmonically distorted. The first term shows the DC offset error, whereas the second line shows the polynomial exhibiting the AC gain error and harmonic distortion terms. Analyzing the second term, the total harmonic distortion is plotted in Fig. 2.19 as a function of mismatch error and the error due to clock feedthrough [9]. For a typical mismatch of about 10 mV and a typical bias current of 25 μA, a total harmonic distortion level of -55 dB is obtained for an i/I ratio of 0.5.

The AC gain error can be written as

$$\text{AC Gain Error} = \frac{\Delta V_T}{V_{gs}-V_T}$$

and the DC offset error can be expressed as

$$\text{DC Offset Error} = I\,\frac{2\Delta V_T}{V_{gs}-V_T}$$

Using the same analysis method, the effects of W, L, and k' mismatches can also be examined. The results of this study are given in the Table 2.1. As can be seen from the table, these three errors do not contribute to harmonic distortion, but do contribute to DC offsets and AC gain errors.

		DC OFFSET	AC GAIN ERROR
$W = 0.5\ (W_1 + W_2)$	$\Delta W = W_1 - W_2$	$(\Delta W/W)I$	$\Delta W/W$
$L = 0.5\ (L_1 + L_2)$	$\Delta L = L_1 - L_2$	$-(\Delta L/L)I$	$-\Delta L/L$
$k' = 0.5\ (k_1' + k_2')$	$\Delta k' = k_1' - k_2'$	$(\Delta k'/k')I$	$\Delta k'/k'$

Table 2.1. The DC offset and AC gain errors of W, L, and k' mismatches.

Harmonic Distortions in Switched-Current Track-and-Hold Circuit: Besides the harmonic distortion introduced as a result of mismatches of the two transistors, it is essential to analyze the effects of clock feedthrough voltage which is also known as one of the major limitations in Switched-Capacitor Circuits.

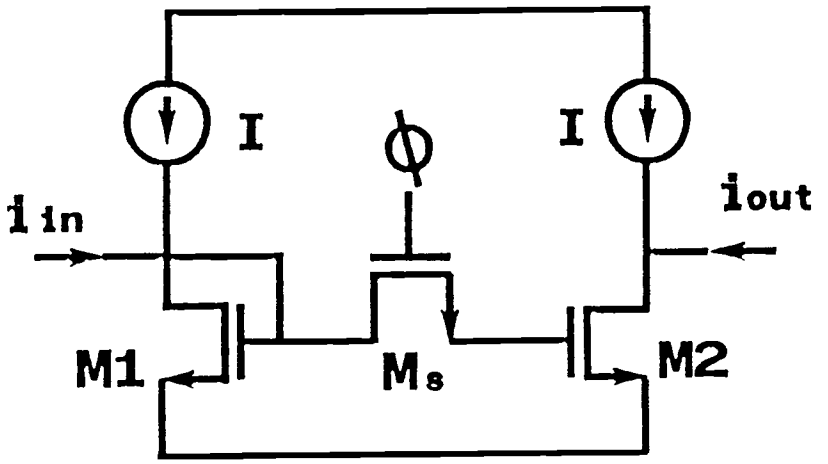


Fig. 2.18. Clock Feedthrough in a Track-and-Hold Circuit.

The total clock-feedthrough current in the circuit given in Fig. 2.18 can be written as:

$$i_{cf} = \frac{k'}{2}\frac{W}{L}V_{cf}^2 + k'\frac{W}{L}V_{cf}\left[\frac{2I\,(1+i/I)}{k'(W/L)}\right]^{1/2}$$

After manipulations, two terms representing the DC offset current and AC current gain error can be obtained from the expression above. The DC offset term is

$$i_{cf,\,DC} = \frac{k'}{2}\frac{W}{L}V_{cf}^2 + V_{cf}\left[\ 2I\,k'(W/L)\ \right]^{1/2}$$

and the AC current gain error is

$$i_{cf,\,DC} = V_{cf}\left[\ 2I\,k'(W/L)\ \right]^{1/2}\left[\ \frac{(i/I)}{2} - \frac{(i/I)^2}{8} + \frac{(i/I)^3}{16} - \frac{5(i/I)^4}{128}\cdots\right]$$

While the DC term indicates an offset error, the polynomial AC term indicates harmonic distortion. The total harmonic distortion which is defined as the R_{ms} sum of the individual distortion products is plotted in Fig. 2.19.

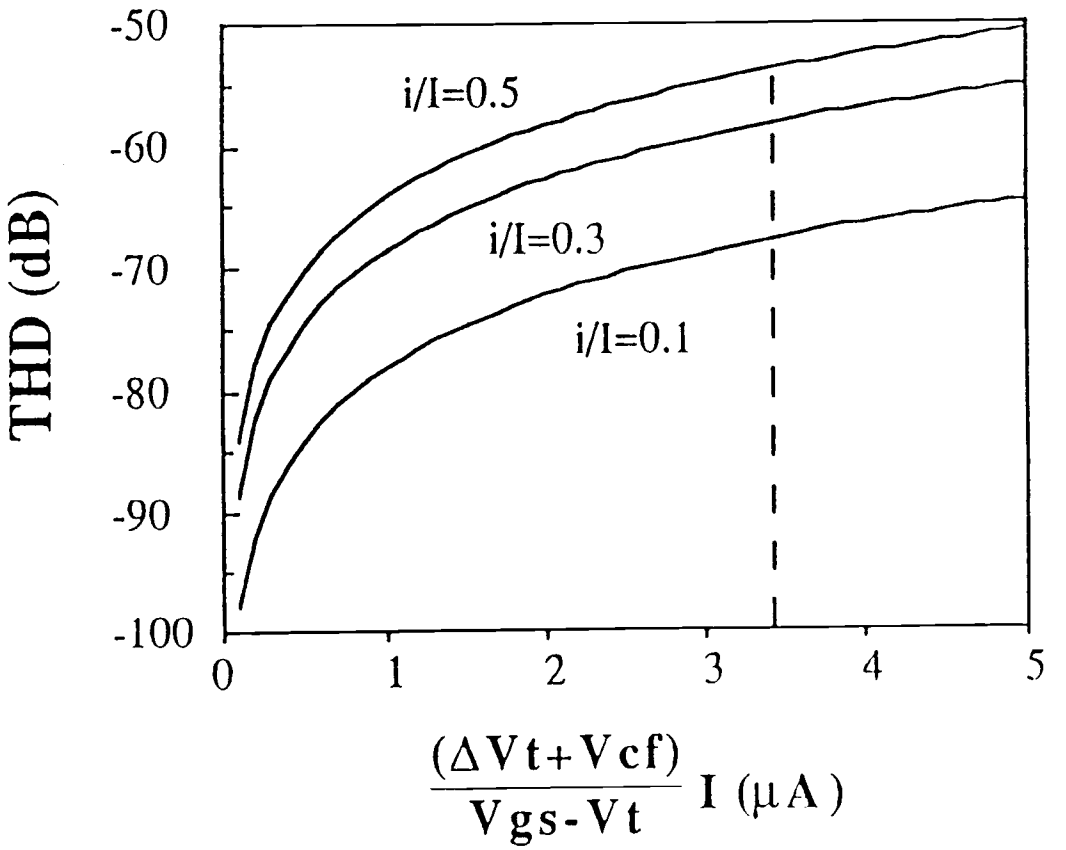


Fig. 2.19. Total harmonic distortion due to the clock-feedthrough and mismatches.

3. FILTER DESIGN USING THE SI TECHNIQUE

3.1. Singly-Terminated RLC Second-Order Lowpass Filter Prototype

Because of the independent programmability of its selectivity and center frequency, and its insensitivity to the component values, a singly-terminated RLC second-order lowpass filter shown in Fig. 3.1 is chosen as the passive prototype for the design.

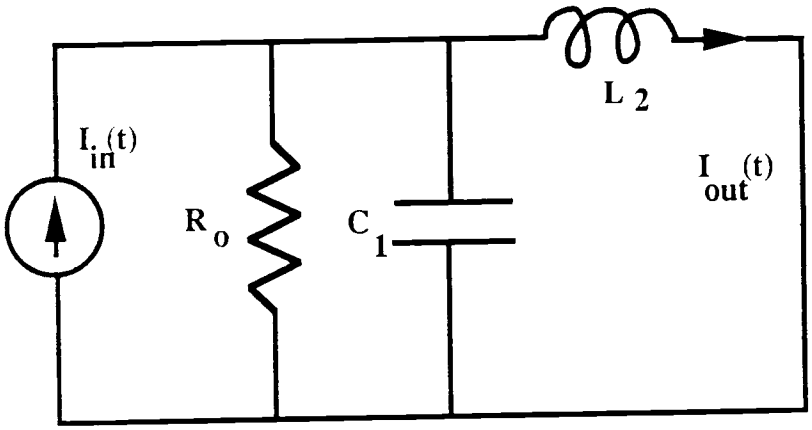


Fig. 3.1. A Singly-Terminated RLC Second-Order Lowpass Filter.

In this section, the transfer function of the prototype circuit is examined to be able to control independent programmability of the selectivity, and center frequency.

Using Kirchhoff's current and voltage laws in the s-domain, the loop and the node equations given below are obtained with $G_0 = 1/R_0$

$$I_{in}(s) = I_{Ro} + I_{C1} + I_{L2}$$

and $$V_{C1}(s) = V_{L2}$$

Using the definition equations of the components,

$$I_{in}(s)=[\ sC_1\ (sL_2 + R_o\ ) +1]\ I_{out}(s)$$

$$H(s) = \frac{I_{out}(s)}{I_{in}(s)} = (1/L_2C_1)/\ [s^2 + sG_o/C_1 + 1/L_2C_1]$$

Comparing the result above with the canonical form of the second-order transfer function,

$$H(s) = K / [\ s^2 + s(\omega_o/Q) + \omega_o^2\ ]$$

it is concluded that,

$$K = 1/L_2C_1$$

$$\omega_o^2 = 1/\ L_2C_1$$

$$G_o/C_1 = \omega_o/Q$$

From these two equations, by selecting the values of the L and C equal, it can be shown that

$$R_o = Q \quad \text{and} \quad K = \omega_o^2$$

where $L_2 = C_1 = 1/\omega_o$.

In the active synthesis of the passive prototype given above, the signal flowgraph technique can be applied similarly to switched-capacitor circuits. However, it should be noted that the signal flowgraphs used in the SI designs are modified to be able to represent input and output variables in the current-domain.

3.2. Signal Flowgraph Technique in the Synthesis of SI and SC circuits

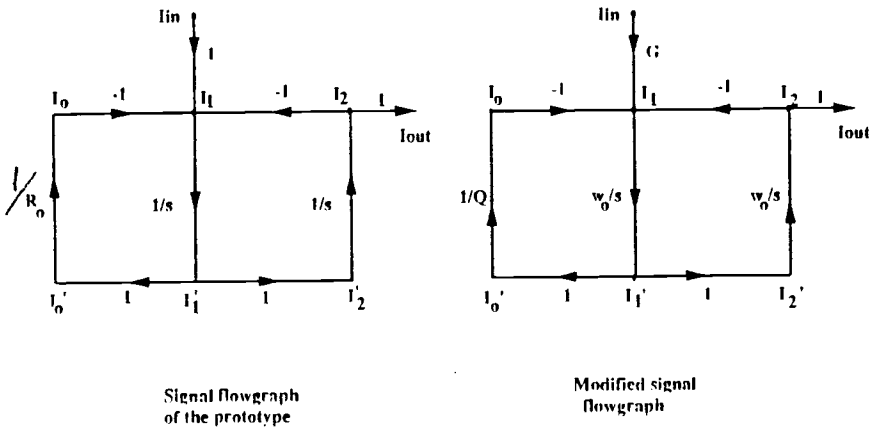


Fig. 3.2. Signal Flowgraphs of the Prototype Before and After Modification.

Fig. 3.2 shows the current signal flowgraph of the prototype given above. It actually carries all the necessary information about the SI circuit schematic from the defining equations of the components.

$$V_o=R_oI_o$$

$$V_1=(1/sC_1)I_1$$

$$V_2=sL_2I_2$$

From the loop and node equations which are used to find the transfer function of the prototype

$$GI(s) = I_{Ro}(s) + I_{C1}(s) + I_{L2}$$

$$I_{out} = I_{L2}$$

$$V_{C1}(s)= V_{L2}(s) + V_{Ro}(s)$$

The transfer of the information given above to the flowgraph is done by replacing the arrows and the scaling factors on each branch of the flowgraph. Then the voltages are replaced by defining new current variables as follows:

$$V_o = R_o I_o'$$

$$V_1=(1/sC_1)I_1'$$

$$V_2= sL_2 I_2'$$

$$V_3=R_3 I_3'$$

And

$$I_o'= V_o/R_o$$

$$I_1'= sC_1 V_1$$

$$I_2'= V_2/sL_2$$

$$I_3'= V_3/R_3$$

After adding the scaling information, the new flowgraph completed is also shown in Fig. 3.2.

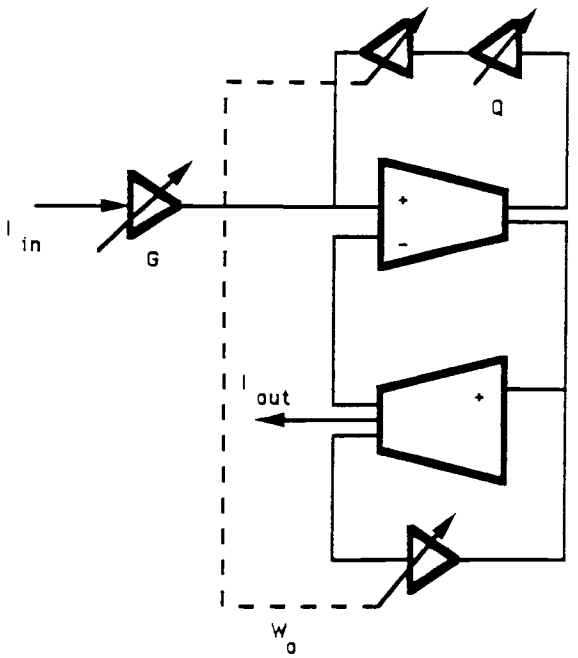


Fig. 3.3. Realization of the Prototype.

From the signal flowgraph, the resulting SI circuit will perform as a programmable second-order RLC low-pass filter as shown in the block diagram of Fig. 3.4.

4. DESIGN CONSIDERATIONS

4.1. Programming the Input Gain

The derivation of the transfer function of the RLC prototype shows that the input gain defined as the value of the H(s) at s=0 is independent of the center frequency and selectivity. The input gain programming in the SI technique involves the binary-weighted amplification of the input signal current. By switching the binary-weighted transistor branches on or off, the input signal current can be amplified and subsequently transmitted to the other modules over a range of 1 to 63 times.

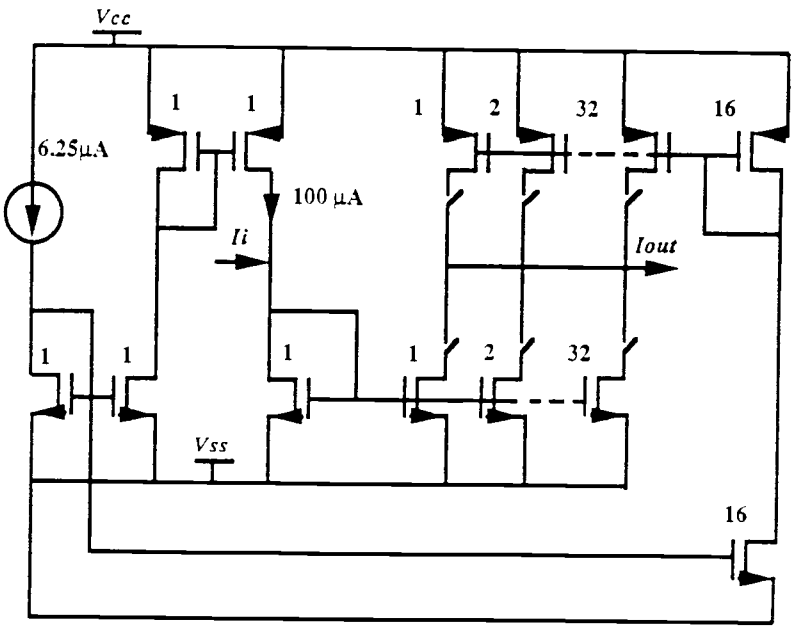


Fig. 4.1. Input Gain Programming Block.

Fig. 4.1 shows the configuration used to program the input gain. The transistors indicated with "1" represent the "unit-cell" sized transistors with a W/L ratio of 6 μm / 10 μm. This particular size was chosen to obtain a reasonable chip area while trying to provide an acceptable accuracy and frequency capability for this design. At the input stage, the signal current is mirrored to various binary-weighted transistor branches through a unit size current amplifier. NMOS and PMOS switches control the connections between the p- and n- transistors and the common output node, I_{out}. Setting the gate voltages of the NMOS and PMOS switches to 2.5V and -2.5V, respectively results in the branch being turned on with a binary-weighted increase in the size of the parallel-connected transistors. For disabling the branches not in use, the NMOS and PMOS switches are held in the cutoff region simply by applying -2.5V and 2.5V to their gates, respectively.

To save chip area, the programmed signal current is taken out as an inverted signal to avoid the necessity of duplicating the binary-weighted n and p transistors in case of a noninverted output current. Two different values are selected as current sources to bias the current mirroring blocks. The first one, providing the biasing current for the "1" transistor branches, is chosen as 6.25 μA which is about twice as the peak input signal current allowed according to the results of harmonic distortion studies. To avoid the ratio of signal current to bias current varying over a large range which would lead to dramatic signal/noise ratio changes as the scaling factor is programmed, an average bias current of 100 μA is chosen for the programmed branches.

4.2. Selectivity Programming

Similar to the input gain programming, the Q programming also involves five binary-weighted transistor branches. However, because of the practical difficulties arising in the realization of a 1: (1/Q) ratio as Q increases, it is preferred to design a programmable current amplifier with a ratio of Q:1. In addition to eliminating the need for very large "1"

devices for obtaining a reasonably accurate 1/Q division, the Q:1 conversion eliminates the extra required polarity change.

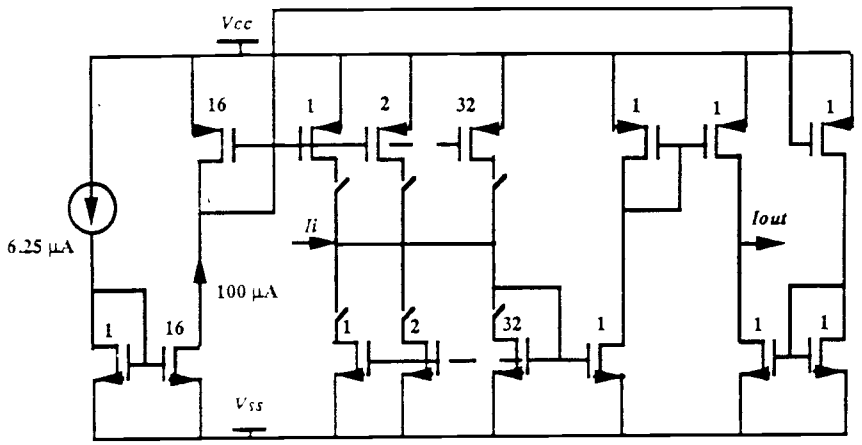


Fig. 4.2. Selectivity Programming Block.

In the programming configuration shown in Fig. 4.2, "1" devices are used at the output side of the block whereas the programmable branches are at the input side. In the input side gain programming block, "1" sized transistors correspond to W/L = 6 μm / 10 μm, "2" to a W/L = 12 μm / 10 μm, "4" to W/L = 24 μm / 10 μm, and so on. The same strategy of implementing the larger transistors by connecting the minimum sized devices in parallel is also used. The input biasing current is chosen as 100 μA, which is generated from the reference current source of 6.25 μA, to maintain the average of the signal current to the biasing current ratio about the same order for as the gain programming as the programming of Q continues from 1 to 63.

4.3. Center Frequency Programming

In order to program the center frequency over a broader range, two different programming techniques are employed . It is desirable to have the center frequency logarithmically sweeping the one octave frequency range provided for a given sampling frequency. This method is based on logarithmic programming of the feedback gain around the integrators. The programmed relationship between two adjacent frequencies is

$$f_{i+1} = 1.0905\ f_i$$

Table 4.1 gives the center frequencies when 2.5 kHz is chosen as the sampling frequency. The corresponding feedback gain is calculated from the formula given below,

$$A = 2\pi f_o/f_s$$

where A is the feedback loop gain of the integrator.

Center frequency (Hz)	Feedback loop gain
200.0	0.1109
218.1	0.1209
237.8	0.1318
259.3	0.1437
282.8	0.1567
308.4	0.1709
336.3	0.1863
366.7	0.2032

TABLE 4.1

Center frequency versus required loop gain.

It should be pointed out that the realization of the feedback loop gain programming can be accomplished by simply incorporating the 1:A to 1/ (A:1) equivalence. Therefore the table will change to

Center Freq.(Hz)	(1/A)	Programming tran.(W/L) (μm / μm)
200.0	9.01	54/10
218.1	8.27	50/10
237.8	7.58	45/10
259.3	6.95	42/10
282.8	6.38	38/10
308.4	5.85	35/10
336.3	5.36	32/10
366.7	4.92	30/10

TABLE 4.2

Realization of A:1 scaling.

The "1" device size is chosen as 6 μm / 10 μm to be able to provide a distinguishable geometry difference of 2 μm in width between the programming mirror transistors. The realization of the logarithmic programming block is given in Fig. 4.3. The one-branch-at-a-time switching distinguishes this block from the previous ones.

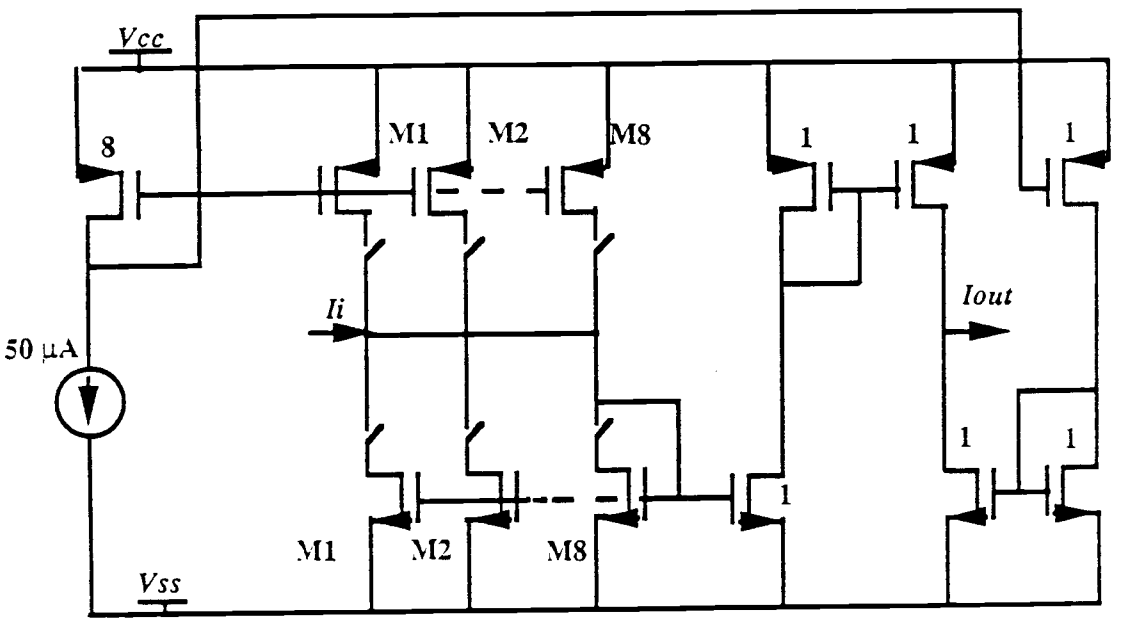


Fig. 4.3. Center Frequency Programming Block.

Besides the logarithmically-spaced frequencies achievable by programming the feedback loop gain, the accessible frequencies can be extended by binary factors by changing the sampling frequency concurrently. In the design, a range of 200 Hz to approximately 330 kHz in center frequency programming is accomplished by varying the sampling frequency between 2.56 kHz and 10.24 MHz in factors of two.

In selecting the bias currents, the harmonic distortion variations as a function of the ratio of the signal currents to biasing currents in the input and output sides are considered.

An input biasing current of 100 μA which is mirrored from the reference current source of 6.25 μA is used at the input, and a current source of 6.25 μA is used at the output.

4.4. SI Integrator

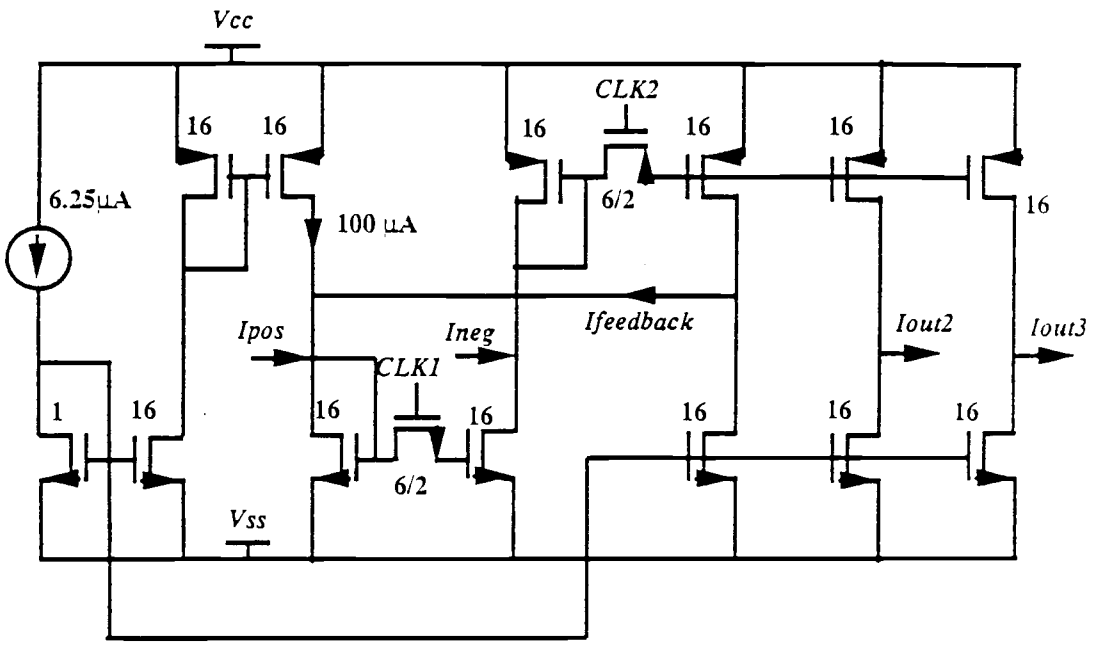


Fig. 4.4. SI Integrator with differential inputs and two outputs.

The integrators are designed by using the SI technique [1]. All of the transistors forming the current mirrors have a W/L ratio of 96 μm / 10 μm and are implemented as parallel combinations of the unit-sized (6 μm / 10 μm) transistors. The bias current sources of 100 μA are mirrored from the reference current source to maintain 0.5 ratio between signal and bias currents.

4.5. Bias Current Sources

All of the bias current sources are generated from an off-chip reference current source. One of the facts which should be considered is the unavoidable current mismatches due to threshold voltage mismatches of the diode-connected devices far from each other. One way to overcome this problem is by using a larger W/L ratio for the mirroring transistor at the reference current source side which is biased at the edge of the saturation. In this case, the variation of threshold voltage (ΔV_{th}) is small relative to the gate-source voltage V_{gs} - V_{th} of the transistor so that its current does not vary significantly. Hence, even though V_{th} mismatches occur, the gate-source voltage of the mirroring transistor is not affected much. Another method is to transmit replicas of the reference current source as current instead of as voltage conversion before it is mirrored and scaled (Fig. 4.5). The second method is used in this design to improve the accuracy of biasing currents.

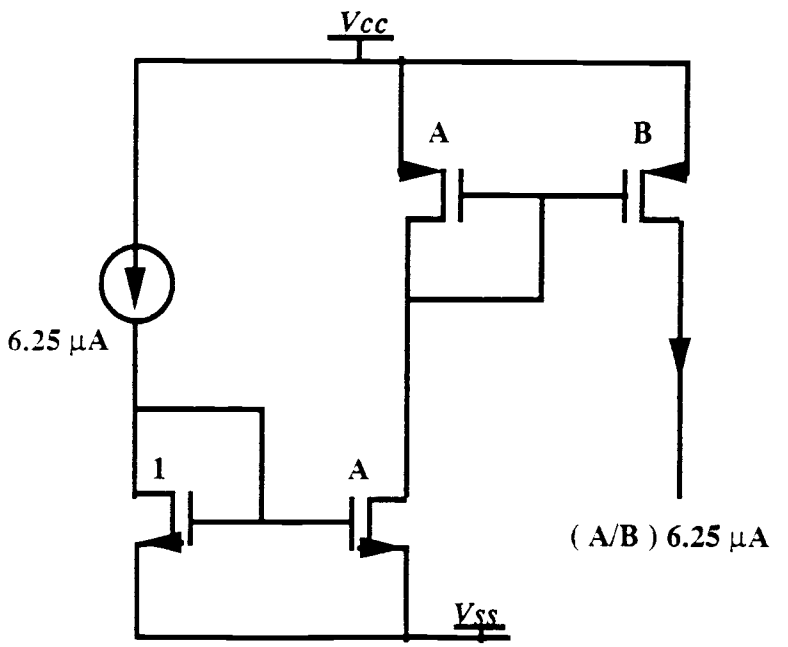


Fig. 4.5. Current Carrying Before Mirroring.

4.6. Frequency Bandwidth Improvement Techniques

The simulations show that the bandwidth of the programmable current amplifier tends to decrease as the size of the programming transistors is increased for achieving the higher scaling factors. This problem affects the frequency response severely where the smaller bias current sources support the large-width transistors since the amount of the gate-source parasitic capacitances hanging on the common gate node becomes very large.

To increase the bandwidth, the configuration given in Fig. 4.6 is suggested. The aim in using the transistor M_1 as a source follower is to provide sufficient current to bias the large devices without loading the biasing current source which causes limitations in higher frequencies. The simulations demonstrating the problem and improved results are given in Fig. 4.7.

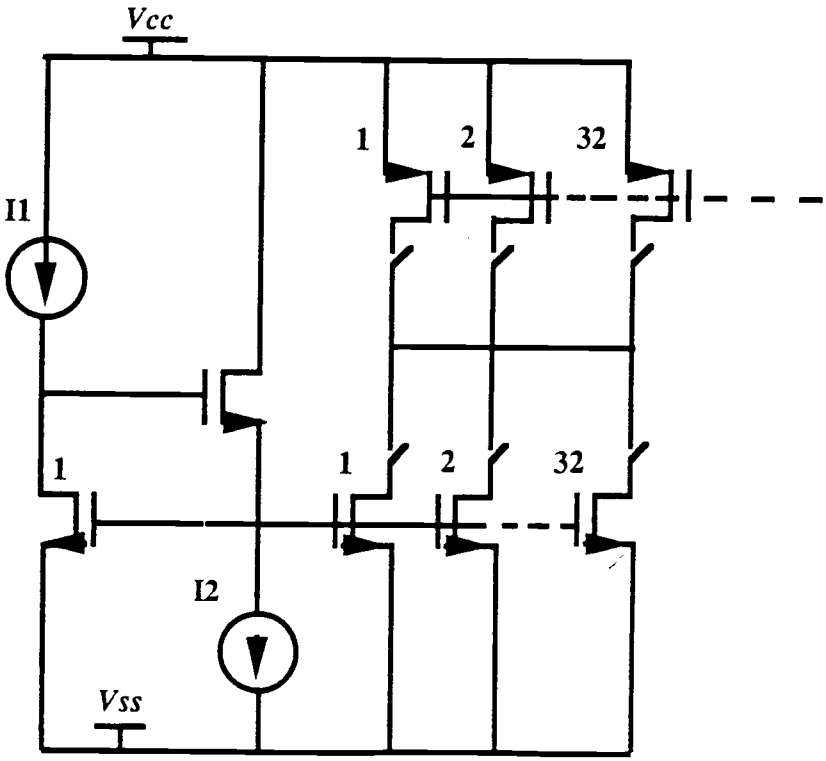


Fig. 4.6. Frequency Bandwidth Improvement with Source Follower.

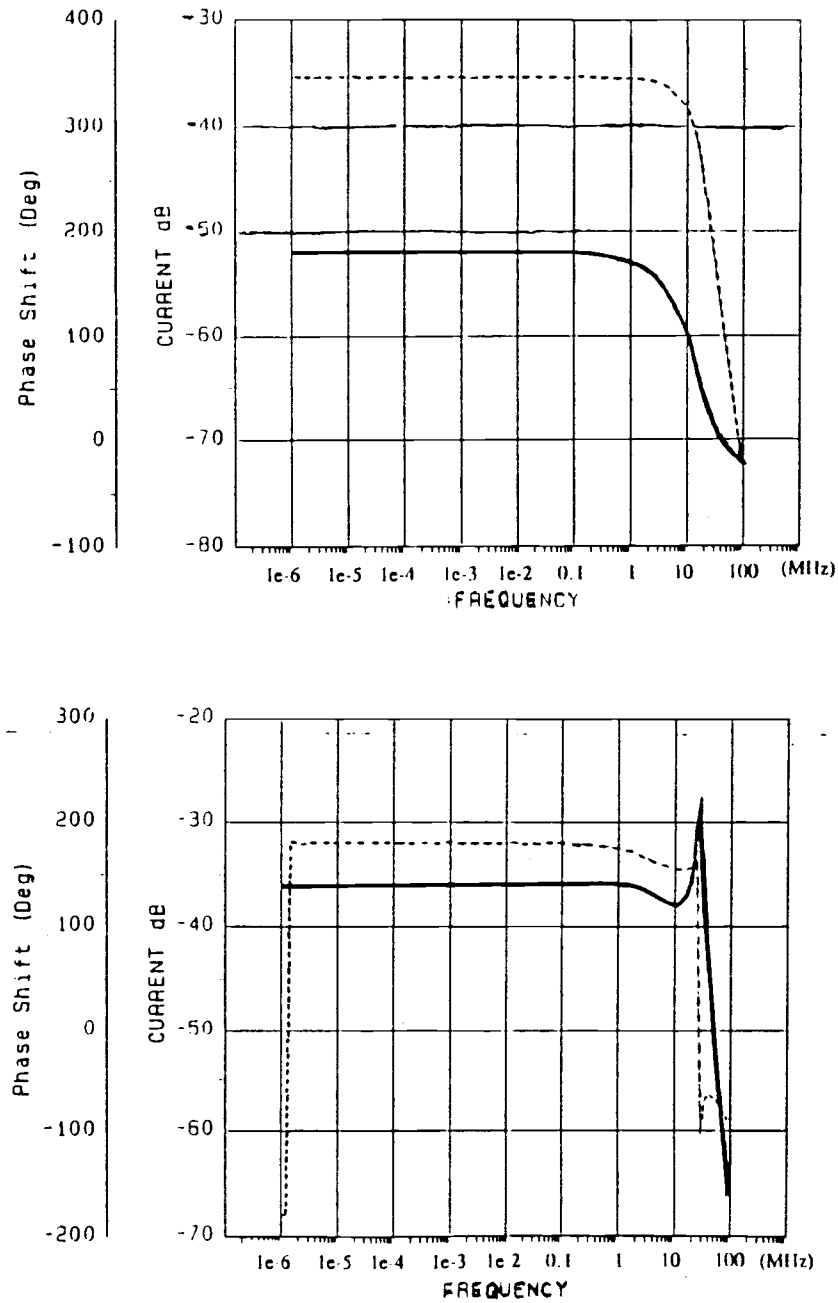


Fig. 4.7. Simulations of Frequency Responses of a Current Amplifier with the Source Follower.

4.7. Chip Layout

The final layout of the chip is given in Fig. 4.8. The tiny chip is implemented thru MOSIS in a 2 μ, Double-Metal, N-Well standard CMOS process. The area of a tiny chip is 2222 μm x 2252 μm where the usable area excluding the pads and the connections to them is 1917 μm x 1950 μm. Out of 40 pins available in a tiny chip, 18 of them are used as the digital control inputs. An external reference current source input is also provided. The input signal and the output signal are carried in and out as currents. Two non-overlapping clock inputs are used to perform the integration operation. The sampling frequency, which is another control in programming the center frequency is adjusted externally.

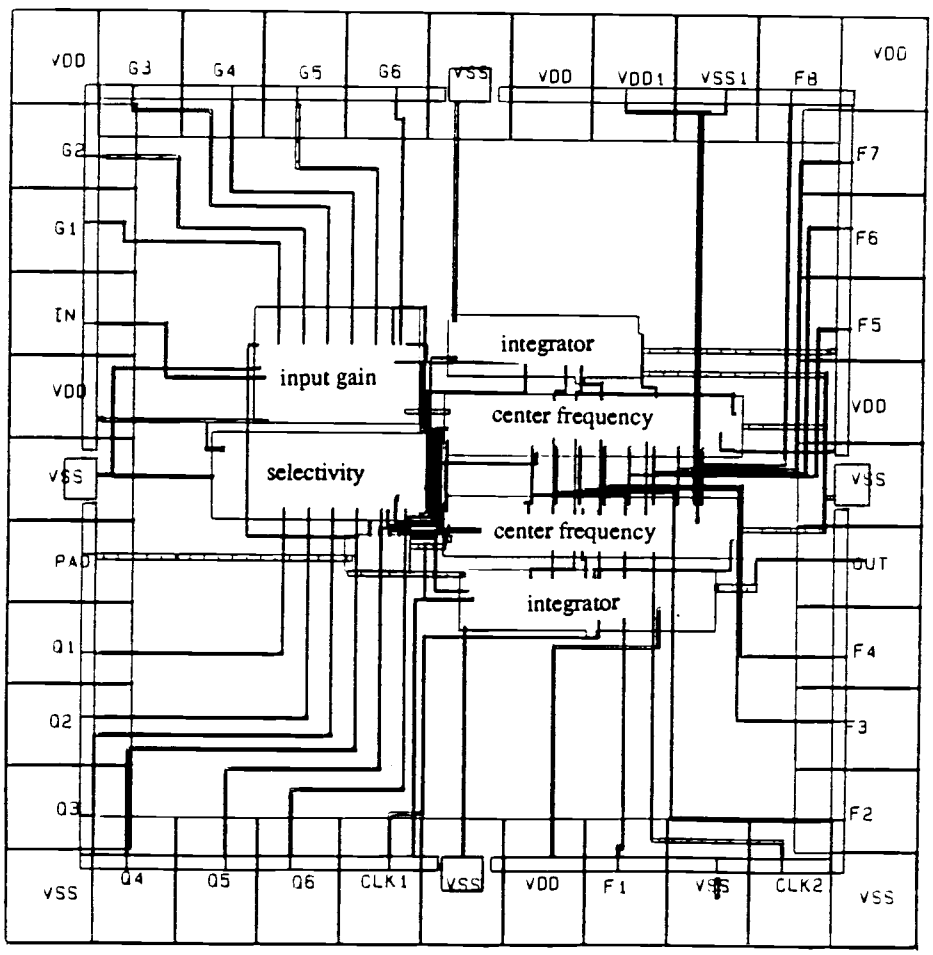


Fig. 4.8. Main blocks of the circuit and the chip layout.

5. CONCLUSIONS

A programmable filter design implemented by using 2 μm Double-Metal, N-well technology through MOSIS on a 40-pin tiny chip is presented as one of the possible applications of the SI circuits [14]. This technique has become very interesting for analog signal processing because of its low-voltage, high-frequency, low power-supply noise potentials, and standard CMOS technology suitability. Although some disadvantages are also acknowledged such as clock feedthrough, mismatches between the mirroring transistors, and distortion, studies are going on to overcome the inconveniences of the SI circuits.

6. REFERENCES

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