AN ABSTRACT OF THE DISSERTATION OF

Qingdong Meng for the degree of Doctor of Philosophy in Electrical and Computer Engineering presented on January 5, 2007.

Title: Low-Voltage Data Converters

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With the growing demand for portable/consumer electronics, such as digital audio/video (AV), the downscaling of device dimensions, which enables the integration of an increasing number of transistors in a single chip, is mandatory. This trend also continuously pushes the power supply voltage down to reduce the power consumption and improve the reliability of gate dielectrics. While the reduction of power supply voltage is of great benefit to the essential digital blocks in the system like data storage and digital signal processing, it makes it hard to operate the important and indispensable analog building blocks such as data converters and drivers.

In this thesis, the novel structures for the low-voltage digital-to-analog converter (DAC) and analog-to-digital converter (ADC) are presented. The research contributions of this work include (1) a sub-1V audio $\Delta\Sigma$ DAC with one opamp used per channel to implement D/A conversion, 1st-order FIR and 2nd-order IIR filtering, as well as power amplification for the headphone, (2) a sub-1V pipelined ADC with the novel MDAC based on a low-voltage track-and-hold

amplifier. Two prototypes, one is a 0.8V, 88dB dual-channel audio ΔΣ DAC with headphone driver, the other one is a 0.8V, 10-bit, 10MS/s pipelined ADC were fabricated to verify the functionality of the proposed structures in standard CMOS processes.

Low-Voltage Data Converters

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Director of the School of Electrical Engineering and Computer Science

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Dean of the Graduate School

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LOW-VOLTAGE DATA CONVERTERS

CHAPTER 1: INTRODUCTION

1.1 Motivation

The world itself is analog in nature, which means that data converters are always necessary components in any system which has interface with the real world. With the continuing growth on demand for portable/consumer electronics, such as digital audio/video (AV), the downscaling of device dimensions, which enables the integration of an increasing number of transistors in a single chip, is mandatory. This trend also continuously pushes the power supply voltage down to reduce the power consumption and improve the reliability of gate dielectrics. As predicted by International Technology Roadmap for Semiconductors (ITRS), for low operating power, the power supply voltage and gate length of digital CMOS will continue to scale down to as low as 0.5V in the next decade as shown in Figure 1.1 [1]. While the reduction of power supply voltage is of great benefit to the essential digital blocks in the system like data storage and digital signal processing, it makes it hard to operate the important and indispensable analog building blocks such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and drivers.

Delta-sigma data converters and pipelined ADC have been popular in both industrial application and academic research. The former are traditionally used

widely for high resolution medium-to-low speed applications such as digital audio and now also gaining popularity in wideband application. The pipelined ADC may

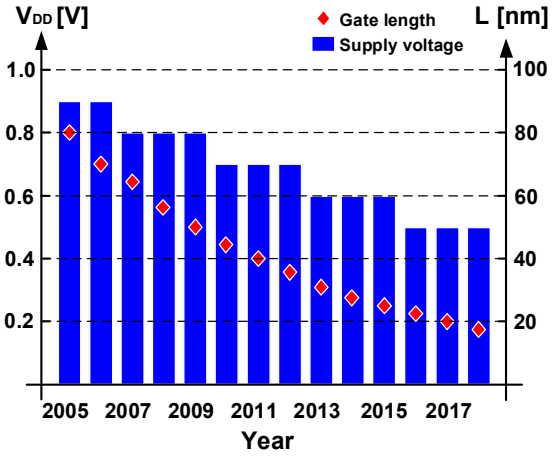

Figure 1.1 CMOS scaling.

be the most popular architecture with sampling rates from a few mega samples per second (MS/s) up to 100MS/s+, and resolutions from 8 bits at the faster sample rates up to 16 bits at the lower rates. It has a wide range of applications, including CCD imaging, ultrasonic medical imaging, digital receiver, base station, digital video, xDSL, cable modem, and fast Ethernet. This thesis focuses on finding novel architectures that are inherently suitable for low-voltage application without any boosting techniques in the standard CMOS process. Specifically, efforts are put on the low-voltage architectures for the audio ΔΣ digital-to-analog converter and pipelined analog-to-digital converter.

1.2 Contributions

The research contributions of this work include:

- A novel structure for the sub-1V audio ΔΣ DAC with one opamp used per channel to implement D/A conversion, 1st-order FIR and 2nd-order IIR filtering, as well as power amplification for the headphone [2].
- Development of a sub-1V pipelined ADC with a novel MDAC based on a low-voltage track-and-hold amplifier.

These proposed structures are inherently suitable for low-voltage (sub-1V) application. Two prototypes, one is a 0.8V dual-channel audio ΔΣ DAC with headphone driver, the other one is a 0.8V pipelined ADC were fabricated to verify the functionality of these proposed structures in standard CMOS processes.

1.3 Thesis organization

Chapter 2 gives a brief introduction of data converter fundamentals. Two architectures, delta-sigma data converters and pipelined ADC, are discussed in detail. State-of-the-art audio Delta-Sigma DACs are reviewed.

Chapter 3 discusses the low-voltage circuit design issues, and techniques proposed to resolve these issues are reviewed.

Chapter 4 presents a 0.8V, 88dB dual-channel audio delta-sigma DAC with headphone driver. It requires only one amplifier per channel to implement D/A conversion, 1st-order FIR and 2nd-order IIR filtering, as well as power amplification for the headphone.

Chapter 5 presents a 0.8V 10-bit 10MS/S pipelined ADC. The low-voltage pipelined ADC uses the novel MDAC based on a low-voltage high-accuracy track-and-hold amplifier.

Chapter 6 concludes this thesis.

CHAPTER 2: DATA CONVERTER FUNDAMENTALS

A signal processing system that has interface with the real world can be generally illustrated as Figure 2.1. Nyquist theorem states that any signal components with frequency higher than one-half of the sampling frequency ($0.5f_s$) will inevitably result in aliasing when it is sampled. If aliasing occurs, it becomes impossible to recover the original signal. So the anti-aliasing filter is required to remove or suppress the unwanted signal out of the band-of-interest and prevent aliasing. The analog signal is continuous in time and amplitude, while the digital signal is discrete in both. Sample-and-hold amplifiers (SHA) provide interface between continuous-time and discrete-time blocks. Conceptually, sampling can convert the continuous-time signal to the discrete-time signal, holding gives time for analog/digital signal processing. Analog-to-digital conversion further converts the continuous amplitude to discrete amplitude. The analog-to-digital converter generally includes the process of both sampling and quantization. The dominant block in almost any modern signal processing system is digital signal processing which manipulates the signal in digital domain. Digital-to-analog converters then convert the digital signal back to the analog signal. Finally, the images will be attenuated by the anti-imaging filter (it is also called reconstruction filter, or just analog low-pass filter), and ideally, the analog output will be faithful replica of the analog input.

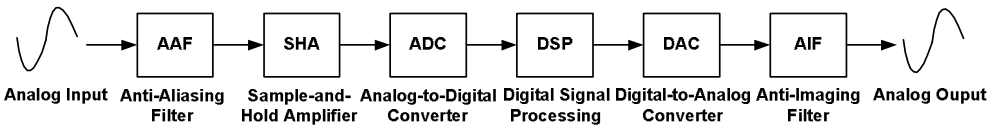

Figure 2.1 Signal processing system.

2.1 A/D converter

The A/D converter contains two processes: sampling and quantization. It is illustrated in Figure 2.2. The samples of the signal are first taken sufficiently close with regard to the highest frequency present in the signal, and then these samples are further quantized to have 3-bit resolution. If the sampling frequency satisfies the Nyquist theorem, the signal can be reconstructed perfectly afterwards.

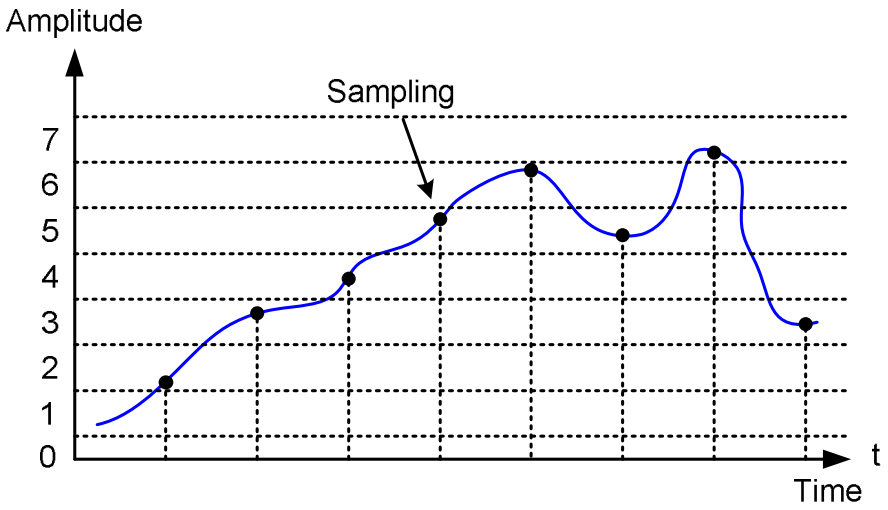

Figure 2.2 Sampling and quantization.

The transfer function of the quantizer in this example is shown in Figure 2.3. For a range of analog input values, the digital output code can be the same. This introduces the quantization error and is given by

$$(\frac{V_{in}}{V_{ref}} - \frac{B_{out}}{2^N})V_{LSB}\,2^N \qquad (2.1)$$

where N is the resolution of the quantizer. The quantization itself is highly non-linear. However, it can be linearized by assuming that the quantization error is signal independent, uniformly distributed, and white additive noise source. This assumption is a good approximation to the reality if 1) the input signal does not overload the quantizer, i.e., the quantization error is within the range of $\pm V_{LSB}/2$, 2) the quantizer has a large number of levels, 3) the quantization step is small, and 4) the input samples have a smooth probability density function [3]. Under this condition, the power of the quantization noise can be proved to be $V_{LSB}^2/12$, and the sine wave input can give maximum 6N+1.76 dB signal-to-quanization-noise-ratio (SQNR).

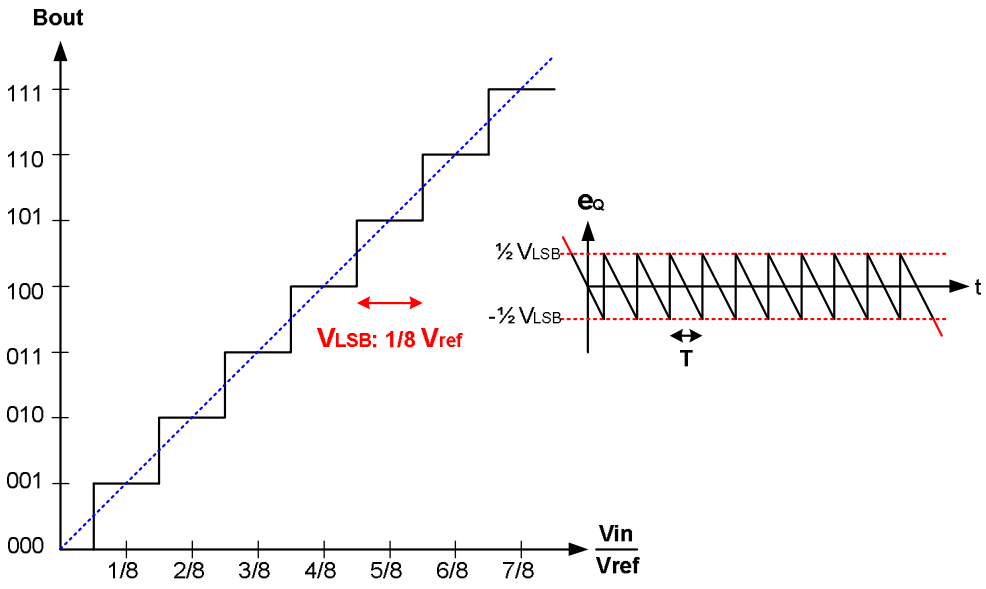

Figure 2.3 Transfer function of 3-bit quantizer.

If signal bandwidth keeps unchanged, and the assumption that quantization noise can be modeled as additive white noise holds, then the SQNR will have a $10\log n$ dB increase if the sampling frequency is increased by n times. In other words, oversampling will result in reduced inband quantization noise. This is illustrated in Figure 2.4.

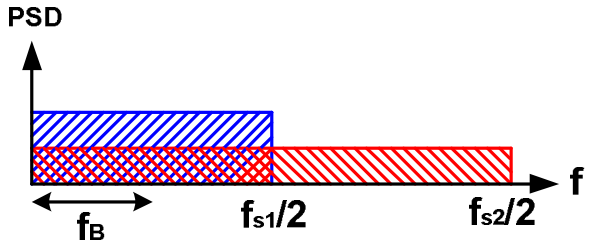

Figure 2.4 Oversampling.

2.2 D/A converter

As it is the case for the A/D conversion, the D/A conversion also contains two processes: digital codes to analog quantity conversion and discrete time to continuous time transformation. The digital code is related to the analog quantity by the following

$$V_{out} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \cdots + b_N 2^{-N}) = V_{ref} B_{in} \qquad (2.2)$$

The transfer curve for a 3-bit D/A conversion example is shown in Figure 2.5(a). It is seen that the analog output is well-defined with respect to digital codes. There is no ambiguity for D/A conversion compared to A/D conversion where a family of analog inputs can generate the same digital code. The discrete-time analog quantity can then be transformed to continuous-time analog signal by a

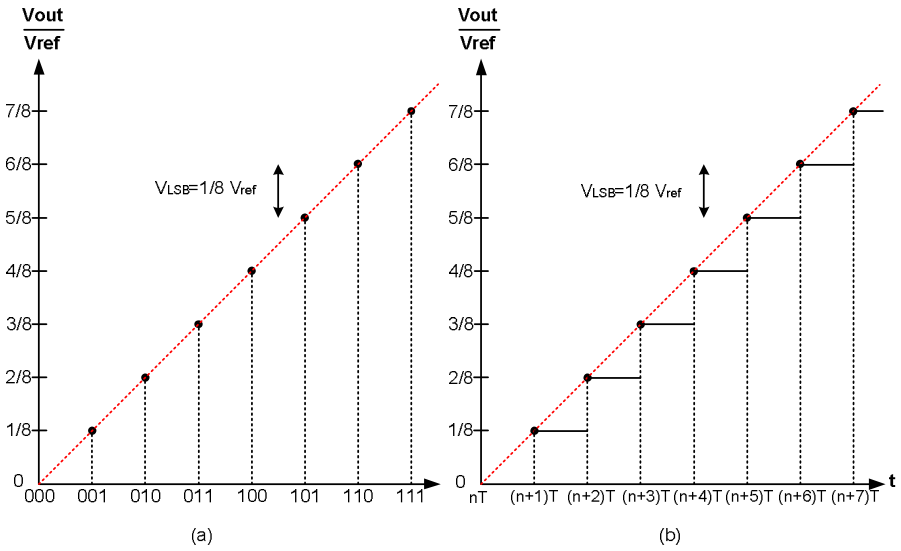

Figure 2.5 Digital-to-analog conversion.

zero-order hold as shown in Figure 2.5(b). The example spectra for the digital input and for the analog output are given in Figure 2.6. The suppression of the high frequency components in the analog output signal is caused by the zero-order hold which is a sinc function in frequency domain. The images need to be further attenuated by an analog low-pass filter in most applications.

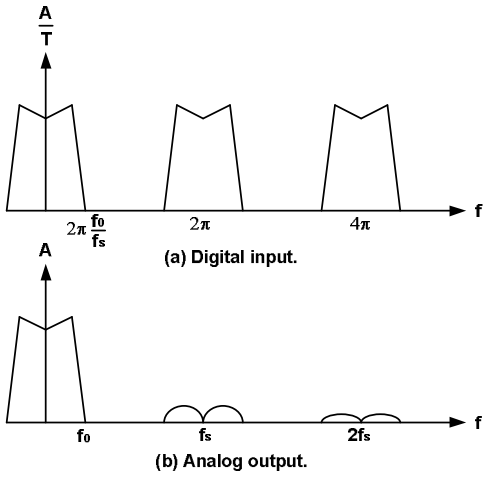

Figure 2.6 Spectra of D/A converter.

2.3 Delta-sigma D/A converter

Delta-sigma data converters employ noise shaping and oversampling to achieve a wide dynamic range in the band-of-interest. It has become a technique of choice for applications that require moderate conversion rate and high accuracy. It is extremely suitable for the audio application. In hi-fi audio applications, 16-bit accuracy performance is mandatory. Using laser trimming or calibration process for Nyquist rate data converters can improve the conversion accuracy, but this adds significantly to the cost. On the other hand, ΔΣ DACs trade the speed and digital complexity for the desired insensitivity to analog nonidealities, which results in high dynamic range with low cost digital circuitry. Figure 2.7 shows its system block diagram [4] [5].

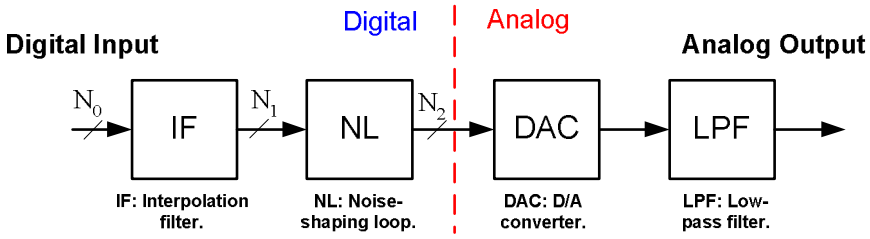

Figure 2.7 Delta-signal D/A converter.

The interpolation filter effectively raises the sampling frequency of the digital input and suppresses images in signal spectra. This reduces the noise power in the noise-shaping loop, improving its dynamic range. The noise shaping loop passes the input signal from the interpolation filter; and shapes the truncation noise caused by the bits reduction from N_1 to N_2 in such a way that the huge quantization noise

will be moved out of the band-of-interest. Generally, N_2 is much smaller than N_1. These truncated bits then enter the low-resolution high-accuracy DAC, the linearity of this DAC should at least meet the whole accuracy requirement of the ΔΣ DAC. Hence, some kinds of calibration techniques are needed to achieve the linearity requirement if the DAC is a multi-bit one. Finally the image in the output of DAC will be removed by the following analog low-pass filter. The signals spectra for each stage are illustrated in Figure 2.8.

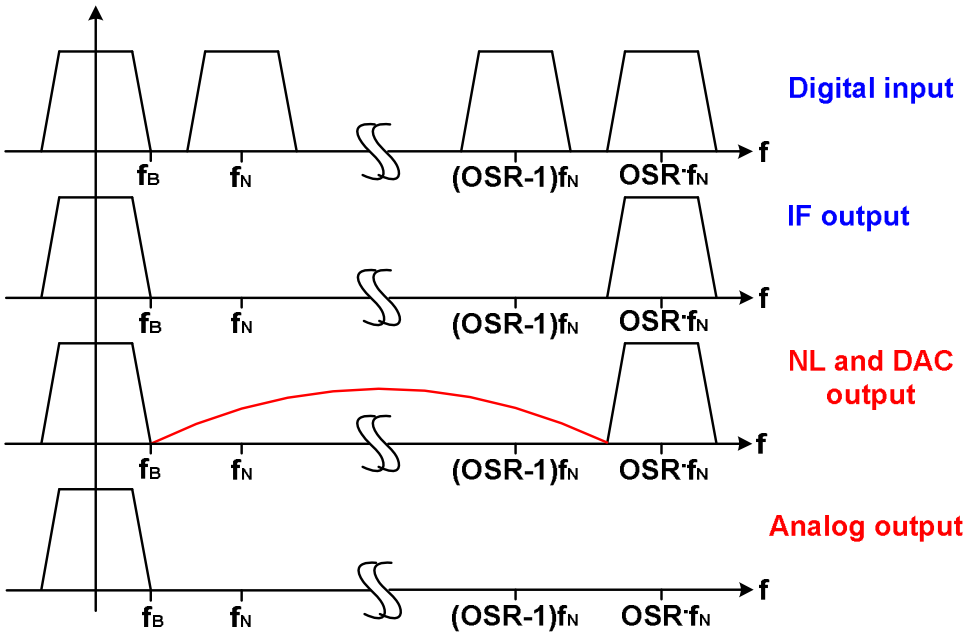

Figure 2.8 Spectra for the signal and noise in a ΔΣ DAC.

2.3.1 Interpolation filter

As was mentioned earlier, the interpolation filter is to remove images of the base band signal that exists in the sampled data signal. The architecture of the filter is designed to minimize arithmetic and hardware complexity. By implementing the

filter as a cascade of several linear-phase stages, the ratio of the input rate to the width of the transition band is dramatically reduced for each of the individual stages. This results in a significant reduction in overall hardware complexity as compared to a general single-stage design [4], [5]-[7]. Half band filter (HBF) has the advantage that every other coefficient is zero; hence, the hardware to implement it will be saved around 50%. Due to this, it is used widely in the interpolation filter design [4], [5]-[7]. A typical implementation of the interpolator is shown in Figure 2.9. It contains four stages with the first three HBF stages raising the sampling frequency by 2 and the last stage a zero-order hold [8], [9]-[10].

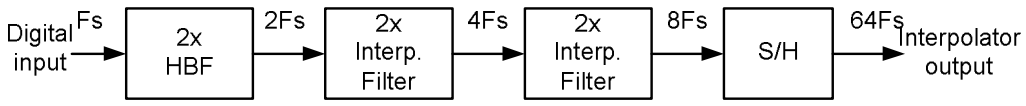

Figure 2.9 A typical implementation of the interpolation filter.

Note that although the frequency content of the images is above the band-of-interest, the first stage still need a steep roll-off to avoid inter-modulation of the signals above inband. The post-filter following the DAC has the most difficulty in removing noise in this band. The complete interpolation filter provides less attenuation for higher frequencies than for frequencies just outside the band-of-interest. There are two reasons for this: first, the analog filter will easily attenuate signals at higher frequencies; second, the $\Delta\Sigma$ modulator will add noise into the band of higher frequency thereafter.

In the SRAM based implementation [7], data is not moved as in the registers based approach. Only the index of address need to be updated. Hence it is power

efficient if the power supply voltage is not an issue in realizing SRAM; it is also area efficient if the order of FIR filter is high. However, when the power supply voltage goes down to sub-1V, it is difficult to design the SRAM with low power. Finally, for audio applications, the interpolation filters for left and right channels can be shared to reduce the area [6], [8]-[11].

There is another approach to implement the interpolation filter proposed in [5]. Five SINC filters, one FIR filter, and one Saramaki [12] halfband filter are used to suppress the unwanted images. However, a low pass signal transfer function for the ΔΣ modulator is assumed. If this is not the case, the already high order of the first stage FIR filter and the second stage Saramaki halfband filter will become even higher.

2.3.2 Delta-sigma modulator

2.3.2.1 Introduction

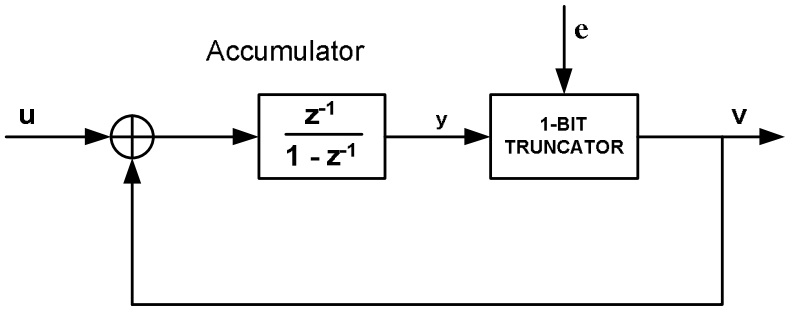

Figure 2.10 A first-order noise-shaping with 1-bit truncator.

The first order ΔΣ modulator is shown in Figure 2.10 (the linear model for the truncator is used in this figure). The error introduced by the 1-bit truncator is given by

$$e(k) = v(k) - y(k) \tag{2.2}$$

where v is the modulator output and y is the quantizer input; and the 1-bit output signal from the first order noise-shaper is

$$v(k) = u(k-1) + e(k) - e(k-1) \tag{2.3}$$

The equation above shows that the output is a summation of the input signal and the difference between the current error and the previous error. For low frequency components of error *e*, the result of subtraction of e(k) – e(k-1) is very small. For example, for the DC component of e(k), e(k)-e(k-1) = 0. Hence v(k) accurately represents u(k) at low frequency.

Assuming the truncation noise satisfies the condition that it is white, the SQNR for the ΔΣ modulator can be found by

$$\text{SQNR} = 12 + 10(2N+1)\log_{10}\left(\frac{\text{OSR}}{\pi}\right) + 6.02(M-1) \tag{2.4}$$

where N is the order of the modulator, M is the bits of the truncator, and OSR is the oversampling ratio. Several observations can be made from (2.4). First, 6N+3 dB SQNR improvement can be achieved by doubling OSR. Second in-band noise can be suppressed by using a higher order modulator with a sacrifice of the loop stability. Finally, a multi-bit truncator can be used to get a 6 dB SNQR increase

with one more bit added to the quantizer, which also improves the dynamic range of the loop with the requirement to calibrate the multi-bit DAC.

2.3.2.2 Architectures for delta-sigma modulator

1) Error feedback architecture

This structure is shown in Figure 2.11. The quantization error is passed through a linear filter before being added to the quantizer input [13].

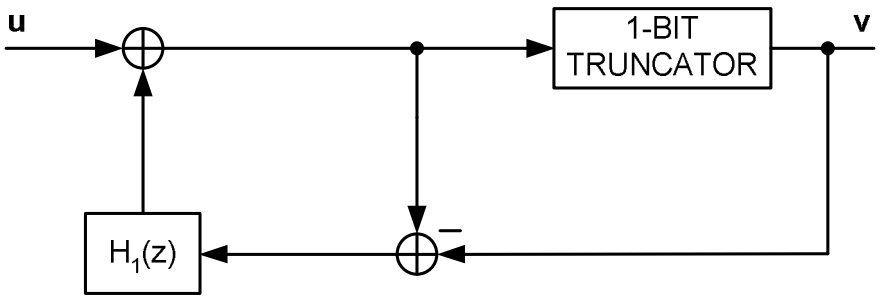

Figure 2.11 Error feedback ΔΣ modulator.

The transfer function of this loop can be given by

$$v(z) = u(z) + [1 - H_1(z)]E(z) \qquad (2.5)$$

This structure often leads to a simpler implementation of the desired transfer function. For example, second-order noise shaping can be realized by implementing the loop filter transfer function of

$$H_1(z)=z^{-1}(2-z^{-1}) \qquad (2.6)$$

This is more efficient than directly realizing the second-order function by cascade of accumulators. To prevent overflow, a limiter can be inserted between the 1-bit truncator input and the feedback summer [13].

2) Dual-truncation DAC structures

Dual-truncation structure was introduced in [14] and [15]. The error feedback architecture was used in the dual-truncation MASH noise-shaping loop as shown in Figure 2.12. One-bit truncator is used in the first stage to keep the high linearity of the signal and the multi-bit truncator is used in the second stage to improve the SQNR. The non-linearity of the multi-bit DAC will be suppressed by second-order differentiator. An accurate transmission zero at dc for the differentiators can be easily implemented by a switched-capacitor delay. The disadvantage for this architecture is that the subtractor needs be accurate enough so that there will no quantization noise leakage and the extra power is required for the analog differentiator to keep the thermal noise low.

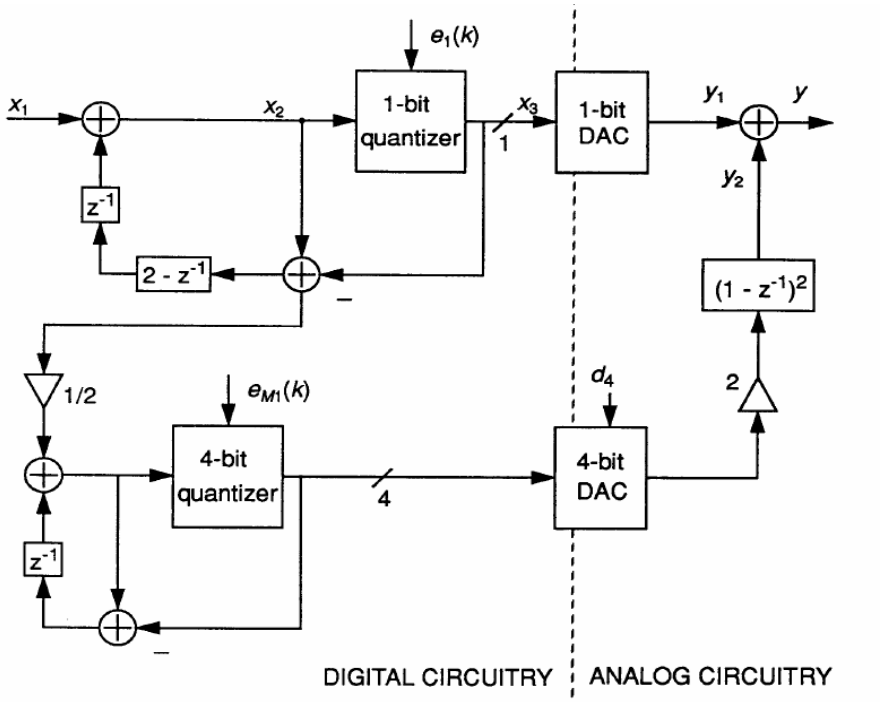

Figure 2.12 Dual-truncation ΔΣ structures.

3) Low-distortion architectures

The distinguishing feature of this structure [16] shown in Figure 2.13 is the direct feedforward path from the input to the quantizer and the single feedback path from the digital output. Analysis gives

$$U(z)-V(z) = -(1-z^{-1})^2E(z) \quad (8)$$

This means the loop filter only processes the errors between the input and the output, the signal does not go through the loop. Hence, it is less susceptible to coefficients truncation than that of the competing architectures.

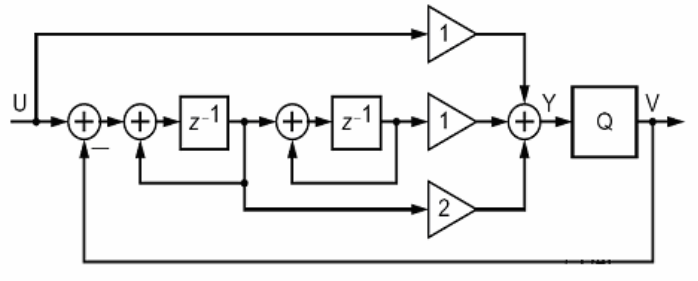

Figure 2.13 Silva-Steensgaard structure.

The low distortion architecture is generalized as cascaded integrator/resonator feedforward (CIFF/CRFF) and cascaded integrator/resonator feedback (CRFB/CIFB and $b_i=a_i$ is required for this case) shown in Figure 2.14 and Figure 2.15 [5]. Note that if the feedforward path from the input to the truncator in Figure 2.15 does not exist [6], [8]-[9], the modulator is not a low-distortion one, and more bits will be required for the accumulators. The resonator will introduce non-DC zeros for the modulator, which will improve SQNR. These zeros are poles for the resonator inside modulator. For cascade integrator architecture, these poles are

outside the unit circle; hence the resonator itself is unstable. But the unstable resonator is within a stable loop, so the whole loop is stable. This property is actually desirable and it helps to suppress the idle tones [17].

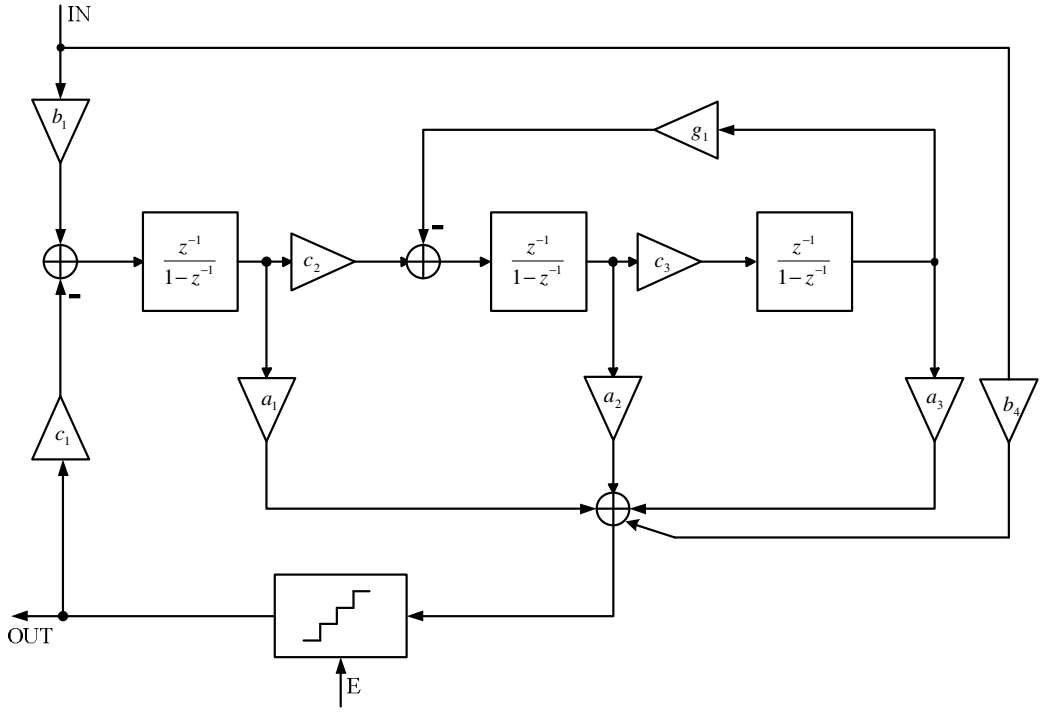

Figure 2.14 CIFF (CRFF if the second accumulator is delay free).

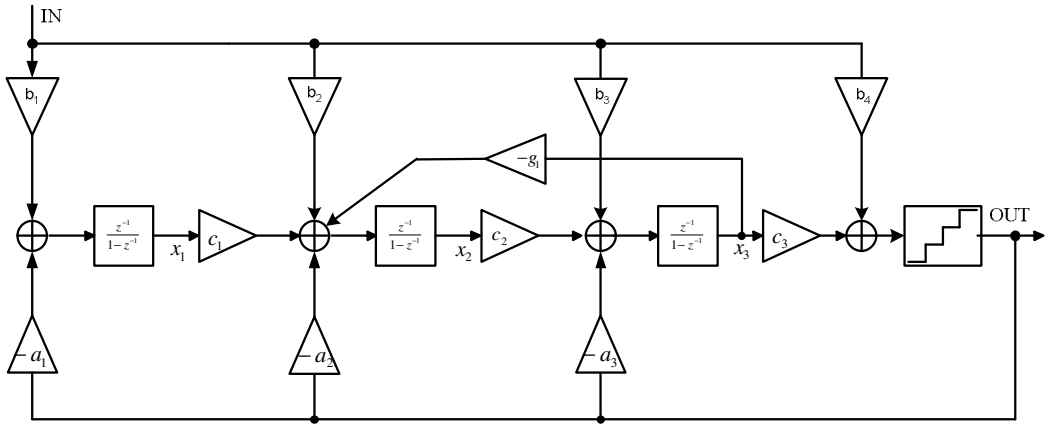

Figure 2.15 CIFB (CRFB if the second accumulator is delay free).

4) Single-bit or multi-bit truncator

In the early years of ΔΣ modulator design, the single-bit was popular [6] [15] because of its inherent infinite linearity. But the assumption of the white truncation noise does not hold if the order of the modulator is not high enough or without using the dither signal. Beside this, due to the huge out-of-band noise, the dynamic range of the modulator will be reduced and the analog reconstruction filter design becomes very difficult [4] [5]-[6]. On the contrary, for the multi-bit truncation, noise-shaping loop can be simpler, sensitivity to clock jitter is reduced, less or no dithering is required, and a much simpler analog smoothing filter can be realized since both the slewing and the out-of-band noise in the DAC output are reduced. Note that in audio application, an odd level truncator is preferred because it helps to suppress the idle tones [9].

2.3.3 Internal low-resolution high-accuracy DAC

2.3.3.1 Discrete-time or continuous-time DAC

The DAC could be implemented in discrete-domain or in continuous-time domain. The choice of circuit implementation involves two main factors: SNR decided by analog noise, and the distortion generated at the discrete-time to continuous-time interface [18]. In conventional switched-capacitor (SC) implementation shown in Figure 2.16, the noise is limited by kT/C noise, and thus achieving very high dynamic range requires large on-chip capacitance [4] [19]. Also, opamps with large UGBW are required to achieve adequate settling. These

both will lead to bigger die size and larger power dissipation to achieve the same passband SNR. On the other hand, in SC implementation, only the final value within the sampling period matters. As long as the analog value settles within the period, it is immune to clock jitter. Another advantage is that the post filter transfer function can be realized accurately.

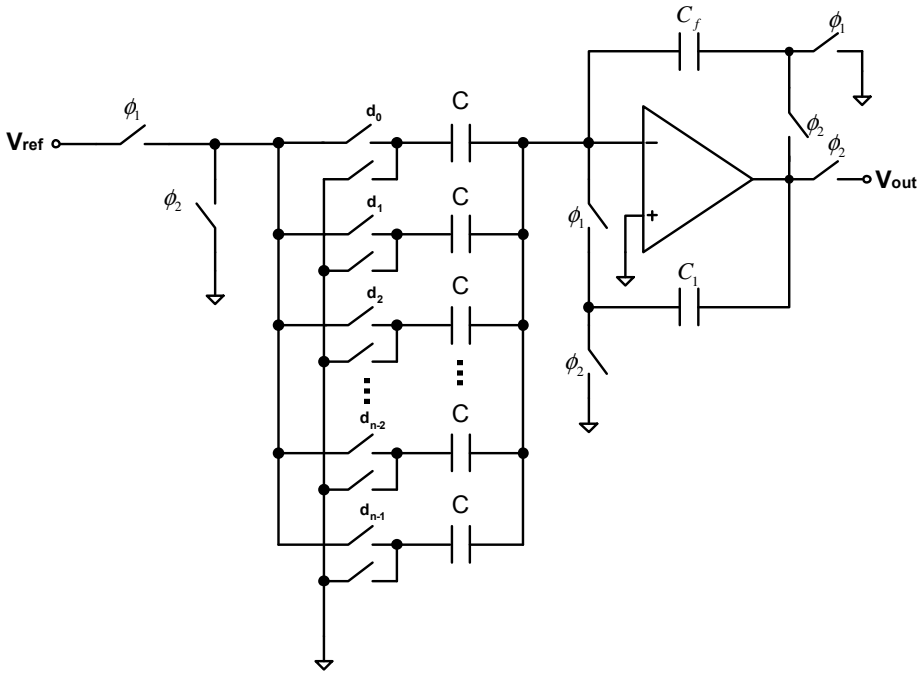

Figure 2.16 Switched-capacitor DAC.

As far as the continuous DAC is concerned, it has no thermal noise aliasing, which often results in power efficient implementation for a given SNR target compared to SC implementation. The drawback of the continuous-time approach is the distortion and passband noise generated by the unequal rise and fall times of the DAC pulse. In a continuous-time implementation, the analog signal in the entire sample period decides quality of the signal.

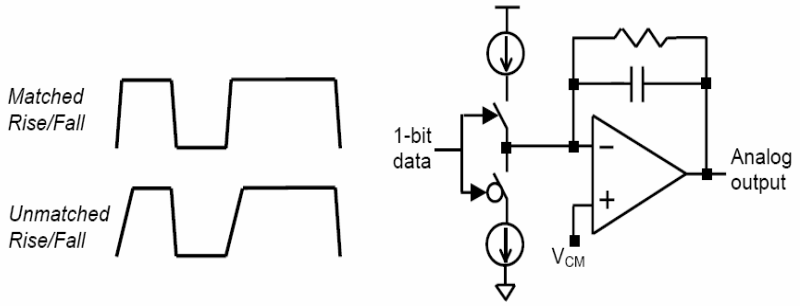

Figure 2.17 One-bit continuous DAC with RC-LPF.

As shown in Figure 2.17, the slower rise time in a 1-bit DAC will cause the area of analog signal of two consecutive "1"s to be larger than the area of two separate "1" pulse. Return-to-Zero (RTZ) coding can solve this problem. However, this approach introduces large steps in the DAC output voltage, which causes problems with jitter sensitivity and linearity in the output stage [19]. Dual RTZ shown in Figure 2.18 was proposed in [19] to relieve the requirement of the large output voltage. Another disadvantage of the continuous approach is that it is sensitive to the clock jitter. Clock jitter will modulate high frequency quantization back to passband. Six-bit DAC was used in [19] to deal with this issue.

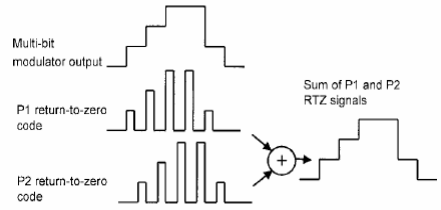

Figure 2.18 Dual return-to-zero.

In conclusion, in audio application, the discrete-time DACs are more favorable than the continuous-time counterparts.

2.3.3.2 Calibration techniques for multi-bit DAC

For multi-bit DAC, the linearity of the DAC needs to be improved by some calibration techniques. Generally, they are categorized into mismatch error shaping, self-calibration, and digital correction. Digital correction is used mostly in high speed ΔΣ ADCs; its implementation is complex and is not popular in ΔΣ DACs. Hence it is not covered in this thesis.

1) Mismatch Error Shaping

Dynamic element randomization chooses the unit elements randomly [19] [20], the noise introduced by element mismatch will be de-correlated and whitened. This is also called zero-order shaping [21]. Six bits were used in the ΔΣ modulator to reduce the sensitivity of clock jitter [19]. To perform D/A conversion and calibration directly is very difficult. Hence, the segmentation based on 1st-order ΔΣ modulator was first used to partition the six bits into 4 bits and 3 bits separately. By doing so, the shaped noise spectra will be preserved for these two bit streams. The block diagram for this scheme is shown in Figure 2.19. The scrambler was then used to randomize the element selection.

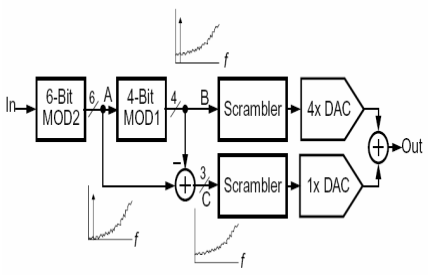

Figure 2.19 Noise-shaped segmentation.

Individual level averaging (ILA) keeps track of all past conversions and makes average usage of each element the same [22]; data-weighted averaging (DWA) starts where the previous conversion ended [23]. These two perform the first-order noise shaping. Compared to DWA method, ILA converges more slowly, which is inefficient when a large number of unit elements is used. On the other hand, it is less affected by any correlation between the mismatch shaping and the DAC input signal, and is less likely to generate tones even for dc or periodic inputs. Tone generation is a major problem for the DWA algorithm. This problem could be resolved by not including a few MSB bits [8] or MSB itself [10] in the DWA routine rotation. Bi-DWA is also proposed to deal with this issue. In this scheme, the direction of the rotation is inverted in every cycle [24]. Each directional rotation proceeds independently from the other. Note the efficiency of both ILA and DWA will be degraded if the OSR is reduced.

Finally, the 2nd-order mismatch error shaping is also possible by using vector-based or tree structure [5] [25], however it is not economical in audio application.

2) Self-Calibration Technique

One self-calibration approach [26] [27] is shown in Figure 2.20. Assume the switches are in the state shown in the figure. Only the first current cell is connected to the reference source I_{ref}. The difference between I_{ref} and the first main current source I_{m1} is supplied by transistor M_1 as it is connected as a diode. The switch S_{11} which is in series with the gate of M_1, is opened, and the two-way switch S_{21}

changes its state. The intrinsic gate-source capacitance C_{gs} of the transistor M_1 stores the voltage corresponding to the current difference, and the absolute value of the calibrated current remains unchanged. Thus a duplicate of the reference source is created which can be applied to the output line I_{out}. The second cell is then connected to the reference source and calibrated, and so on, until all 15 current cells of the D/A converter and the current cell needed for reference adjustment are calibrated. A switched-capacitor DAC is calibrated in a similar way in [28].

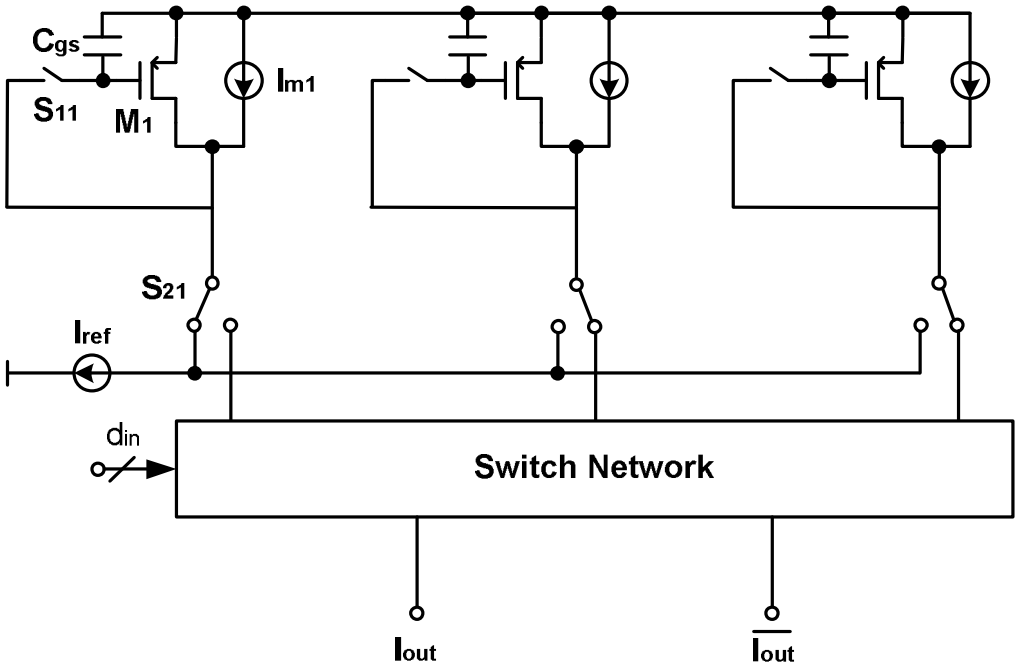

Figure 2.20 Self-calibration technique based on current source.

2.3.4 Analog post-filters for delta-sigma DACs

The purpose of the analog post filter is to filter the out-of-band noise. If the one-bit truncator is used in the ΔΣ modulator, although the quantization noise in

such a converter is shaped in frequency so that most of its energy lies well above the audio frequency range, this noise must be attenuated by a carefully designed analog low-pass filter in order to avoid inter-modulation and phase distortion. If the multi-bit truncator is used in the delta-sigma modulator, as mentioned earlier, the design of the analog reconstruction filter can be relaxed. The requirement for the passband performance also affects the selection of filter topology. In most applications, a flat passband response is preferred. This requirement prevents use of high-Q filters such as Chebyshev filters. A Butterworth transfer function is a common choice, because of the low Q. The cut-off frequency is usually set significantly higher than passband to reduce passband droop [18].

2.3.4.1 Analog post-filter for the single-bit delta-sigma DACs

The fourth-order Butterworth SC filter shown in Figure 2.21 is used to suppress the out-of-band noise before the discrete-time to continuous time interface [6]. This structure, called inverse follow-the-lead (IFL) [5] [29], is different from the conventional cascade of biquads. The kT/C noise from the second to the fourth integrator will become negligible because of the noise shaping by the preceding integrators. This realizes a high-order filter that has only one integrator with significant kT/C noise contribution. In other words, all integrators other than the first one can be designed with high noise, which means low power and small area in SC implementation. However, this architecture has no finite transmission zeros, which means that selectivity is not good [5].

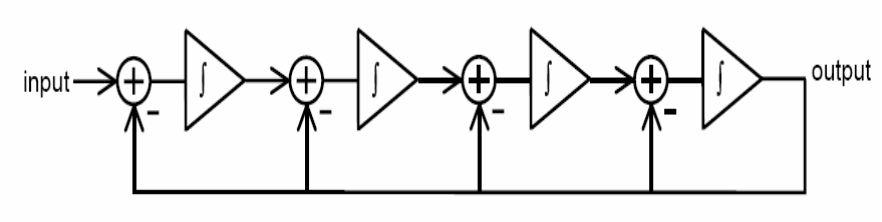

Figure 2.21 4th-order IFL Butterworth SC Filter.

Another key concern for the single-bit DAC is the discrete time to continuous time interface. At the discrete time to continuous time interface, any deviation from the ideal stair-wave output of a zero-order hold will generate non-linearity. Figure 2.22 illustrates nonlinearities generated at the discrete time to continuous time interface.

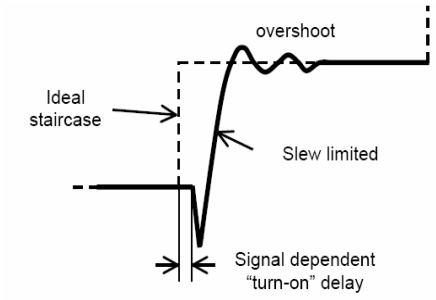

Figure 2.22 Ideal staircase and the non-ideal staircase.

The most severe distortion among the nonlinearities is slew-rate limiting. The direct charge transfer (DCT) [6] [30] stage can be used to make the interface free of such transients. Figure 2.23 gives the DCT circuit. It samples the input signal x(t) at the end of phase ϕ_1, storing it in c_1. As ϕ_2 goes high, c_2 is switched across c_1, and the two capacitors share charges passively. Signal dependent variation of the turn-on delay will also cause distortion. In SC circuits, this can be

caused by slow rise time of the control clock combined with common-mode variation of the switch. Because of this, fast rise time of the SC clock is required in ΔΣ DACs [18]. Another source of distortion is the overshoot caused by ringing. This can be avoided by having phase margin greater than 70 degrees [20] [31].

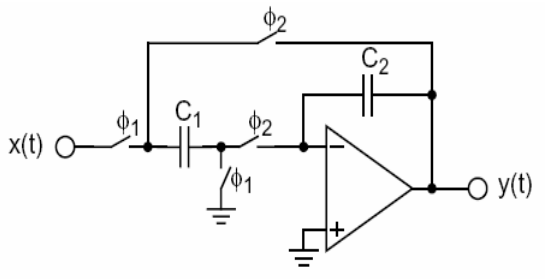

Figure 2.23 A direct charge transfer stage.

The error caused by the clock jitter is proportional to both the voltage step ΔV, and timing error Δt. In a ΔΣ DAC, the error consists of both the high frequency quantization noise and fundamental signal modulated by the clock jitter. High-frequency noise can fold down to the band-of-interest and degrades the signal-to-noise-ratio (SNR). Modulation of the fundamental signal will cause side-lobes around the fundamental. In case of 1-bit quantization, the voltage step ΔV is equal to the reference voltage. To reduce the amount of error, it is required to have as much filtering as possible at discrete domain to reduce ΔV before the discrete time to continuous time interface.

An analog FIR filter shown in Figure 2.24 is used to filter the 1-bit output data from the ΔΣ modulator [32]. The 1-bit data is shifted through an n-tap delay line implemented by shift registers. The weighting of the current sources controlled

by the 1-bit output of each tap realizes the FIR coefficients. Errors in the analog coefficients (current weights) do not introduce nonlinearity into the analog output; they simply degrade the stopband response and phase linearity of the filter. Hence as long as the summing operation is data independent, no distortion will be generated.

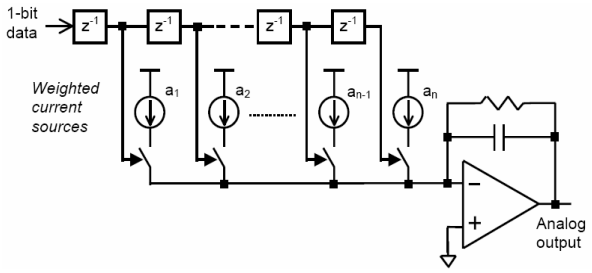

Figure 2.24 Analog FIR filter.

2.3.4.2 Analog post-filter for the multi-bit delta-sigma DACs

For multi-bit ΔΣ DACs, the out-of-band noise is greatly reduced due to smaller step size; hence the design of the post-filter can be much easier. Figure 2.25 shows the single switched-capacitor stage to perform the 1st-order FIR and IIR filtering and D/A conversion for the 31-level truncation in the ΔΣ modulator [8]. The FIR filter before the DCT DAC can improve the insensitivity to the clock jitter. Since it is a DCT circuit, an off-chip analog low pass filter can be connected to the output directly without the extra discrete to continuous time interface. In this circuit correlated double sampling (CDS) technique can also be added to achieve the offset and gain compensation [33].

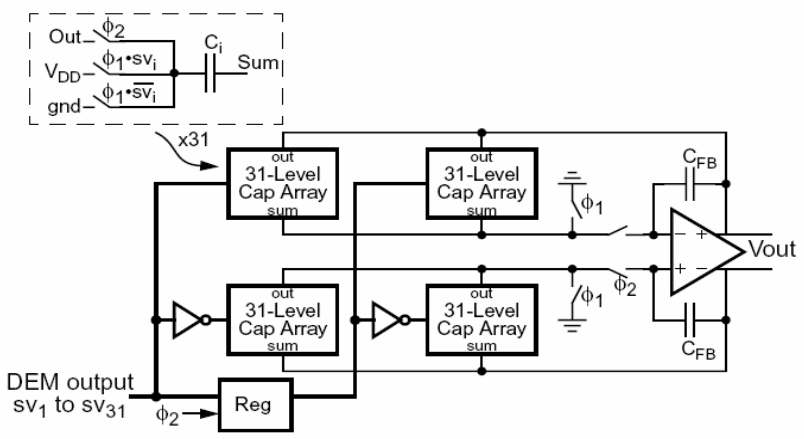

Figure 2.25 DCT-DAC with 1st-order FIR filter.

A DCT-DAC was also used in [9], where the output of the DAC was followed by the 2nd-order Sallen-Key filter as shown in Figure 2.26. Figure 2.27 shows the circuit merging the 13-level DAC and the low pass filter [10]. This saved one amplifier. Third-order SC Chebyshev filter was used to strongly reduce the out-of-band noise and a 1st-order continuous time filter was then followed.

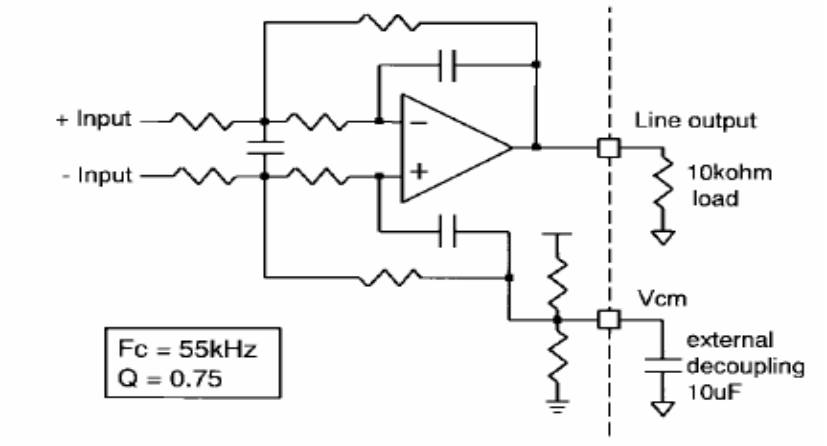

Figure 2.26 Sallen-Key RC filter.

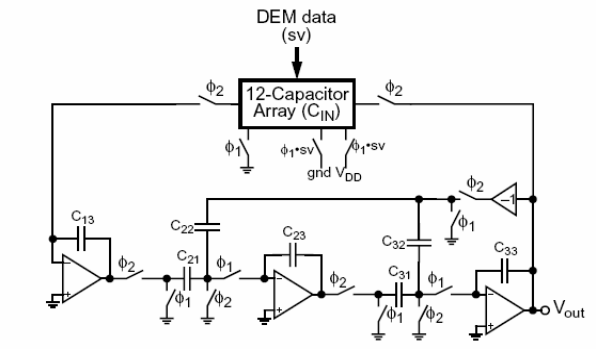

Figure 2.27 13-level SC DAC and the 3rd-order SC LPF.

2.4 Pipelined A/D converter

The pipelined ADC is widely used in applications where a relatively high bandwidth and a high resolution are required. The speed of the pipelined ADC does not depend on the number of stages. Each stage can be optimized separately to reduce the power and area without sacrificing the speed. The number of stages only increases the latency, which is not an issue in most applications. Figure 2.28 shows an example of a pipelined analog-to-digital converter. It contains 9 stages and a digital correction circuitry. Each stage samples and holds the input signal by the sample-and-hold amplifier (SHA), the held signal is converted into a low-resolution digital code by the sub-ADC and the digital code is then converted back to analog signal by the DAC. Finally the output of the DAC is subtracted from the held input, generating the error that enters the gain amplifier. The residue, which is the output of the gain amplifier, is sent to the next stage for further conversion.

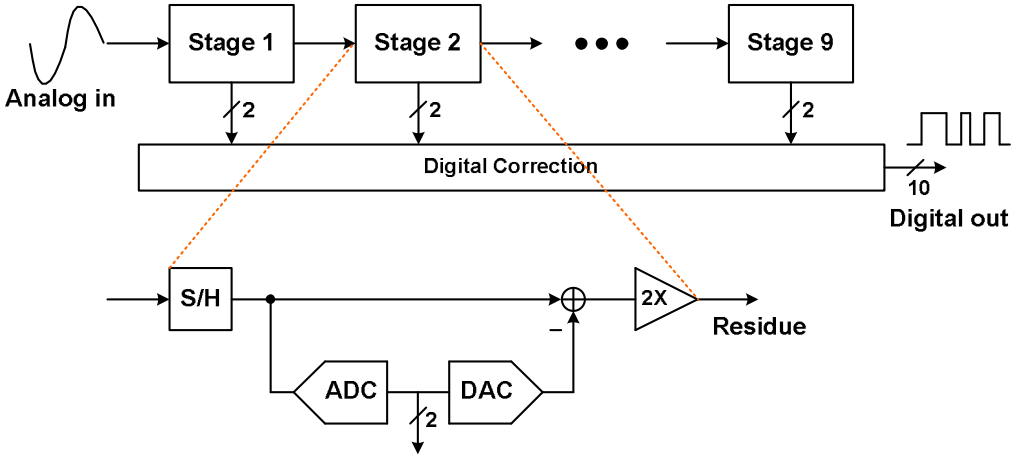

Figure 2.28 Pipelined ADC.

It is demonstrated that digital correction logic relaxes the sub-ADC design by introducing redundancy bits in between stages [34] [35]. The correction logic is simplified by introducing an offset before and after the sub-ADC [35]. It is a difficult optimization problem to get the optimum bits for each stage [34] though. Generally speaking, a multi-bit first stage eases the requirement of matching and amplifier design for the following stage with the sacrifice of the bandwidth of the input signal due to the smaller feedback factor. However, the interstage gain of the first need to be at least as linear as the whole pipelined ADC is. This puts a stringent requirement of the component matching and opamp's DC gain for the first stage.

CHAPTER 3: LOW-VOLTAGE CIRCUIT DESIGN ISSUES

3.1 CMOS scaling

The reduction of power supply voltage is driven by several factors: reduction of power dissipation, reduced transistor channel length, and reliability of gate dielectrics. The power consumption of digital circuits mainly contains two factors: dynamic power and static power. It can be shown as

$$P=CV_{DD}^2f+I_{leak}V_{DD} \quad (3.1)$$

where C is the parasitic capacitance that the transistor need to drive, f is the clock frequency, and I_{leak} is the leakage current of transistors. The effective and straightforward way to reduce the power consumption is to reduce the power supply voltage. For a NMOS transistor, the cutoff frequency f_t is given by

$$f_t=\frac{\mu_n v_d}{2\pi L^2} \quad (3.2)$$

With a reduced transistor channel length, the cutoff frequency of transistor will increase greatly. Beside this, the transconductance of transistor will become bigger because of the reduced channel length and smaller parasitic capacitance. All these factors result in a faster operation of the circuit with shrinked transistor channel length. The gate dielectric reliability is a big issue in deep sub-micro and nanometer process. The channel hot carrier (CHC) effects, which are roughly shown in Figure 3.1, can cause drain-to-substrate current and gate current. To suppress this effect, the drain-to-source voltage needs to be scaled down

accordingly. The gate-to-source voltage also needs to be reduced to avoid gate oxide breakdown which will cause unrecoverable damage to transistors.

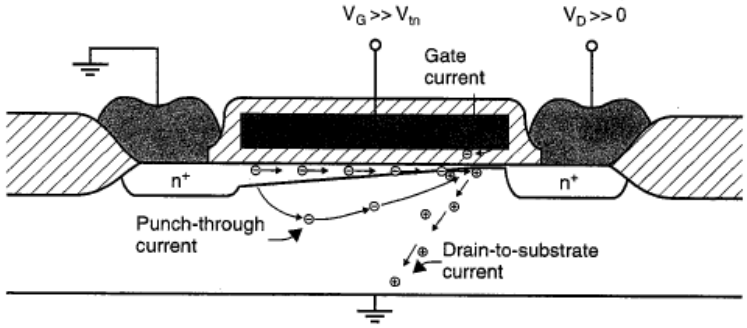

Figure 3.1 Hot carriers effects.

3.2 Noise

With the reduced power supply voltage, the signal swing at the output is always reduced to get an acceptable distortion level. While thermal noise for resistors and capacitors due to sampling somehow stays unchanged, and they are given by (3.3) and (3.4), respectively.

$$4kTR\Delta f \qquad (3.3)$$

$$kT/C \qquad (3.4)$$

Where k is Boltzman constant, T is temperature, and Δf is the bandwidth. To maintain the high dynamic range (DR), the smaller resistor or bigger capacitor is required. This poses a stringent load requirement for the amplifier and more power need to be burned.

It is not uncommon for the flicker noise to have a corner frequency at a few mega hertz for the deep sub-micron process and at the order of giga hertz for the

nanometer process. Increasing the area of transistors to reduce the flicker noise is not always effective and practical. There are some circuit techniques proposed to deal with this issue. Correlated double sampling (CDS) cancels any offset and strongly reduces the 1/f noise by introducing one zero at the origin of the frequency [33]. Chopper stabilization (CHS) uses the modulation to move the signal to the high frequency where there is no 1/f noise or lower 1/f noise and then to move the signal back to the baseband [36]-[38]. The principle of chopper stabilization is illustrated in Figure 3.2.

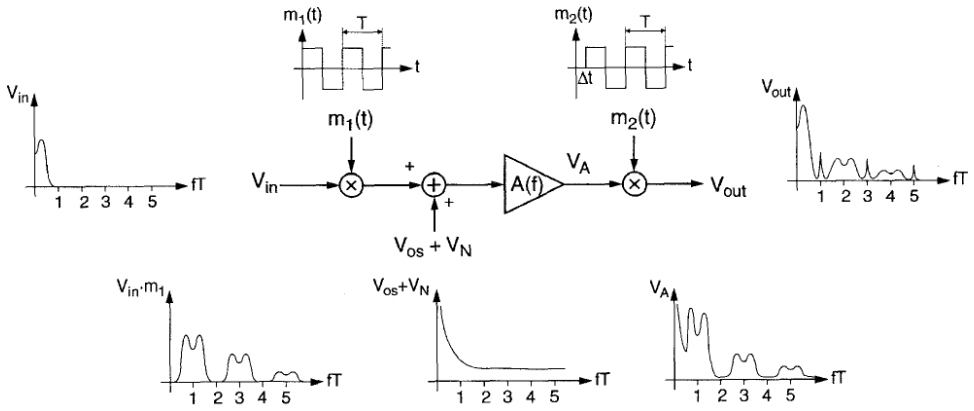

Figure 3.2 Principle of chopper stabilization.

CDS reduces the offset and 1/f noise by highpass filtering and is inherently a sampled-data method. CHS moves the low frequency noise to the out-of-band frequency through modulation and can be used in continuous time system. Effectively, CDS can boost the amplifier's gain while the CHS needs to amplify the high frequency signal and its effective gain is actually reduced.

Recently, another technique, switched biasing attracts attention in mixers [39]. Figure 3.3 illustrates the principle of switched biasing and compares it to constant biasing. Instead of applying a constant gate-source bias, a MOS transistor is periodically switched between active state in which it contributes to the functional operation of a circuit and a rest state in which transistors are in accumulation state and the MOS transistor is not operational. The rest state is introduced to reduce the noise of the MOS transistor during its operational state. Furthermore it reduces the power consumption. However, not all circuits offer the freedom of switching transistors between an active state and accumulation without affecting the correct circuit operation.

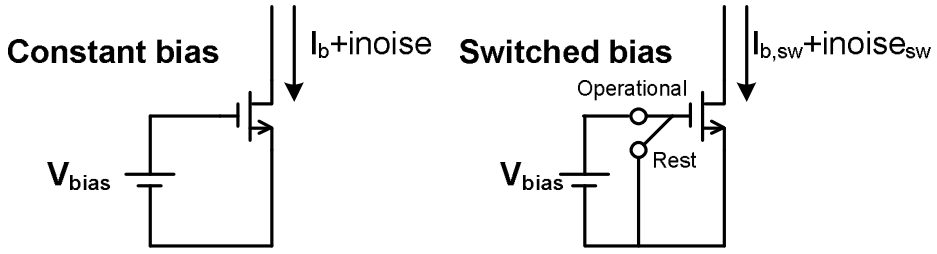

Figure 3.3 Switching bias technique.

3.3 floating switch

If one switch is neither connected to Vdd nor to ground, it is defined as a floating switch. The on-resistance for a MOS switch is

$$R_{on} = \frac{1}{\mu c_{ox} W / L(V_{GS} - V_t - V_{ds})} \tag{3.5}$$

For a floating switch, the on-resistance will be varying since V_{gs} is changing. This results in nonlinear sampling. For the integrator shown in Figure 3.4, one way to reduce the effect of the variable on-resistance is to choose big switch for S_1 and small switch for S_2. One important trade-off needs to be carefully made though. If the switch size of S_1 is too big, then the parasitic capacitance at node 1 may become significant, and it is highly voltage dependent. It always deserves careful simulation to determine the size of switch S_1 in reality and it is not unusual to use the bootstrapped switch in realizing S_1 to improve the sampling linearity.

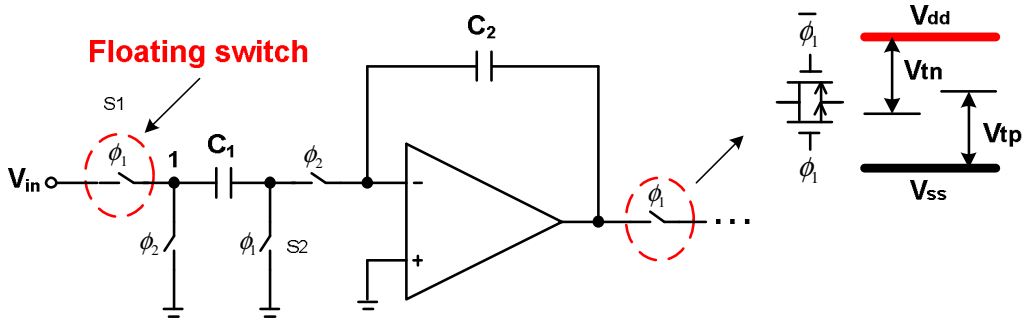

Figure 3.4 Switch-capacitor integrator.

The second problem is the charge injection. The channel charge of a transistor is given by

$$Q_{ch} = C_{ox}WL(V_{gs} - V_t - V_{ds}) \qquad (3.6)$$

And approximately one half of this charge will go to capacitor C_1 when switch S_1 changes from on to off. This charge is linearly proportional to Vgs, which depends on V_{in}. This is less likely to be a big issue if the fully differential circuit is used and a delayed clock phase is applied to control switches S_1.

The third problem which is also the biggest one is the difficulty turning on the floating switch when the power supply voltage is scaled down to be lower than the sum of the NMOS and PMOS threshold voltage. This is also illustrated in Figure 3.4. The existing techniques that deal with this issue are discussed in the following.

3.3.1 Lower transistors threshold voltage

The straightforward way to turn on the floating switch is to introduce extra mask layers [40] to reduce the threshold voltage in fabrication if the high cost is not an issue. However, reducing the threshold voltage too much results in significant sub-threshold conduction, and hence causes charge loss and nonlinearity occurs.

3.3.2 Voltage doubler

The basic idea of this technique is to generate a higher V_{dd} locally to get sufficient overdrive voltage to turn on the floating switch [41] [42]. However, in the deep submicron process, this will introduce long term reliability issue such as channel hot carrier effects (CHC) and gate oxide breakdown. Therefore, it is not a good choice in the modern COMS circuit design.

3.3.3 Clock bootstrapping

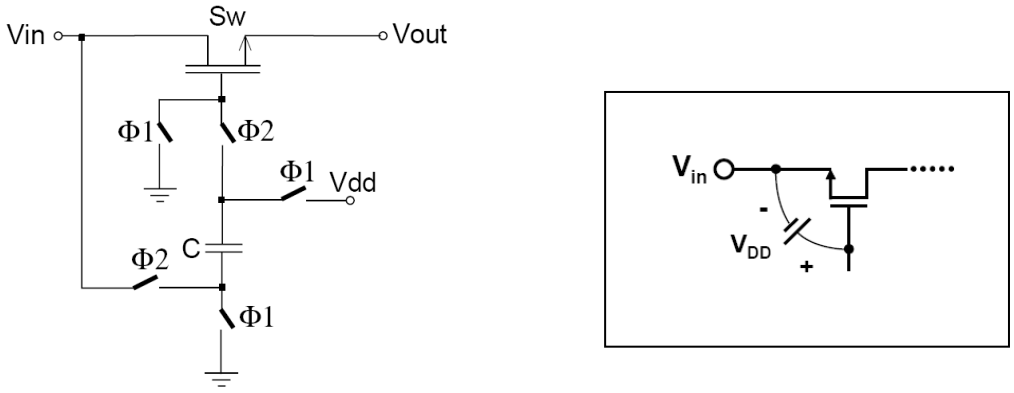

Figure 3.5 clock bootstrapping.

Figure 3.5 shows the conceptual diagram of clock bootstrapping [43] [44]. It works as follows. During clock phase 1, the gate voltage of the switch is pulled down to ground and the switch is turned off; and the capacitor is charged up to V_{dd}. During clock phase 2, the gate of the transistor is floating, since the bottom plate of the capacitor is connected to V_{in}, the gate voltage will be boosted to $V_{dd}+V_{in}$ and V_{gs} now becomes V_{dd}, which is constant. The voltage between any two terminals of transistor is lower than V_{dd}, which does not degrade the circuit reliability compared to voltage doubler. The constant V_{gs} makes the on-resistance of the switch constant; this feature is actually often used to introduce the linear sampling for the integrator shown in Figure 3.4 even when the power voltage is high enough to turn on a CMOS switch well.

3.3.4 Switched-opamp

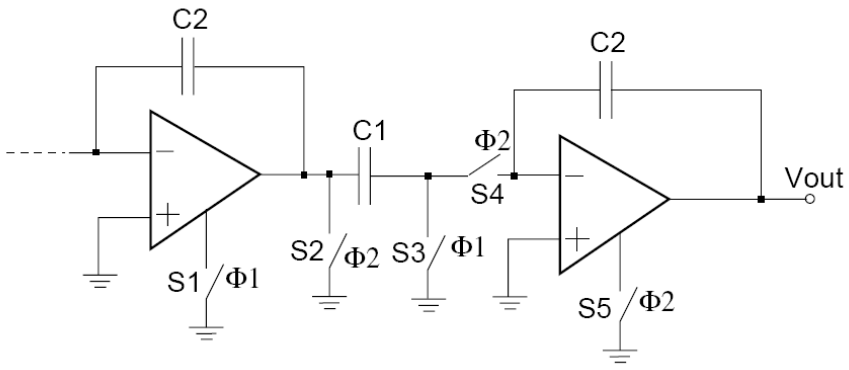

Figure 3.6 Switched opamp.

The main idea of switched-opamp technique (SO) [45]-[47] is to replace the floating switch with an opamp as shown in Figure 3.6. During clock phase 1, the opamp is turned on, capacitor C_1 samples the signal through the opamp and the switch S_3. During clock phase 2, the opamp at the previous stage is turned off, the charge stored in capacitor C_1 is transferred to capacitor C_2. The integrator now works well without suffering from the low power supply voltage. This technique is suitable for sub-micro CMOS technology. However, the speed limitation imposed by powering up and down the opamp restricts it to the relatively low speed application.

3.3.5 Opamp reset switching technique

Opamp reset switching technique (ORST) [48]-[50] also replaces the floating switch with an opamp. But this technique is not based on turning on and off the amplifier during the sampling and integrating phases of the integrator; instead, the opamp is always kept active. This incapacitates the high speed operation of the integrator. Figure 3.7 shows the simplified circuit of this scheme. Capacitor C_s samples the input signal, which is the output of the previous stage, during clock phase 1. The charges stored in this phase are transferred to capacitor C_I during clock phase 2 by resetting the amplifier in the previous stage through a unity gain feedback configuration. The amplifier undergoes the integration and reset phases with different feedback factors, this may cause settling issue. In the reset phase, the dc output of the amplifier is equal to the input common mode voltage; and in the sampling phase, the output common mode is set independent of the input common mode level. Since it is not uncommon to use different common-mode levels for the input and the output of the amplifier when the power supply voltage goes to sub-1V, this complicates the common mode feedback circuit design.

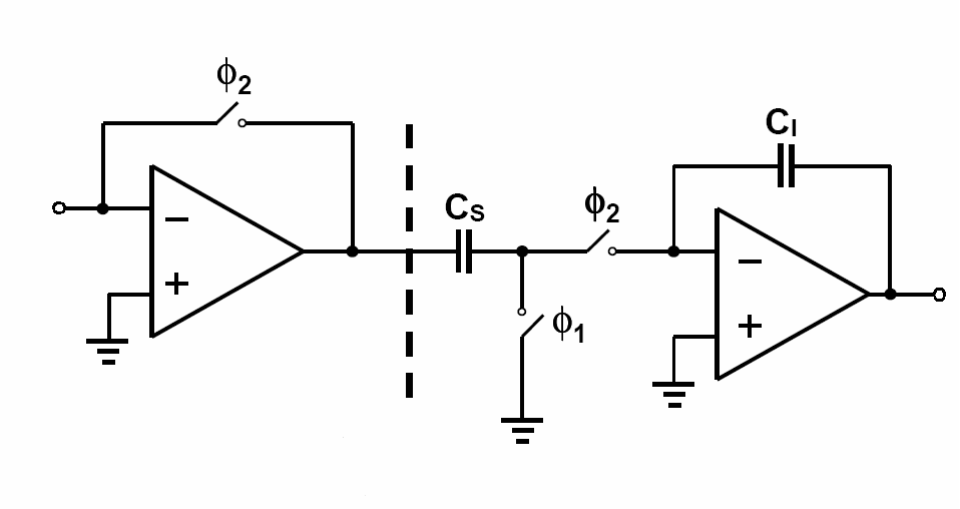

Figure 3.7 Opamp reset switching technique.

3.3.6 Switched-RC technique

The switched-RC technique was proposed in [51] [52]. In this scheme, the floating switch is replaced directly by a resistor as shown in Figure 3.8. This greatly improves the sampling linearity without using the clock bootstrapping. The integrator works as following: during clock phase 1, capacitor C_{s1} samples the input through resistor R_1 and switch S_2, during clock phase 2, charges stored in capacitor C_{s1} will be transferred to the integrating capacitor C_{I1}. During the integrating phase, the resistor R_1 and switch S_1 will form a resistor divider through which the input signal will have a leakage at node X given by

$$Vx(n+\frac{1}{2}) = Vin(n+\frac{1}{2})\frac{R_{on}}{R_1 + R_{on}} \tag{3.7}$$

This input leakage at node X will result in a gain error which is given by

$$\frac{C_{S1}}{C_{I1}}\frac{R_{ON1}}{R_1+R_{ON1}}Vin(n+\frac{1}{2}) \qquad (3.8)$$

If the clock frequency is sufficiently high than the input signal so that $V_{in}(n+1/2)$ is very close to $V_{in}(n)$, the gain error can be approximately given by

$$\frac{C_{S1}}{C_{I1}}\frac{R_{ON1}}{R_1+R_{ON1}} \qquad (3.9)$$

The ratio of R_{on} and R_1 can be sized carefully to give a small gain. However, if the clock frequency is not sufficiently high, the leakage signal at node X will cause nonlinearity.

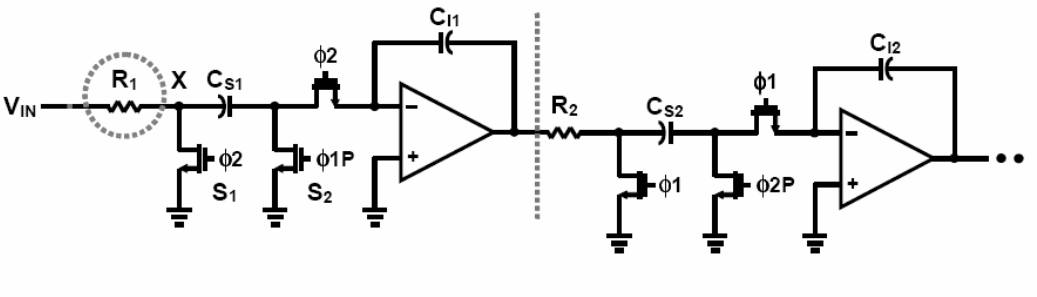

Figure 3.8 Switched-RC technique.

3.4 Opamp

The output common-mode voltage of the amplifier is necessarily kept at $V_{dd}/2$ to have the large signal swing especially when the supply voltage goes down to sub-1V. If assuming the input common-mode voltage is equal to the output common-mode voltage (this may be true in most cases), the minimum supply voltage for the amplifier shown in Figure 3.9 will be

$$V_{DD} = V_{ICM} + V_{th} + 2\Delta = \frac{V_{DD}}{2} + V_{th} + 2\Delta \tag{3.10}$$

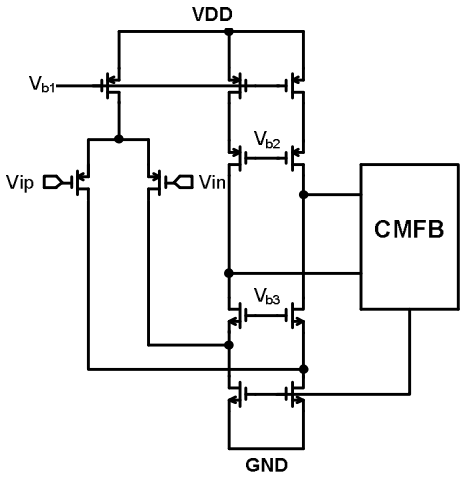

Figure 3.9 An amplifier schematic.

where Δ is the overdrive voltage of transistors. This equation implies that

$$V_{DD-Min} = 2V_{th} + 4\Delta \tag{3.11}$$

For example, for 0.4V threshold voltage and 0.1V overdrive voltage, the minimum supply voltage need to be 1.2V. If the power supply voltage goes down to sub-1V, it becomes extremely difficult to design an amplifier with the input common mode voltage to be mid-way of the power supply voltage.

The parallel connected complementary input differential pair shown in Figure 3.10 was proposed [53] trying to extend the input common-mode range. However, the zone in which both input differential pairs is cut-off still exists when the power supply voltage is further reduced. This structure also suffers from reduced common-mode rejection as the input differential pair is changed from NMOS to PMOS or when both complementary pairs are active. Since the input

offset voltages of the n-channel and p-channel differential pairs likely have different values, the effective input offset voltage of the amplifier may vary when the input differential pair changes dynamically.

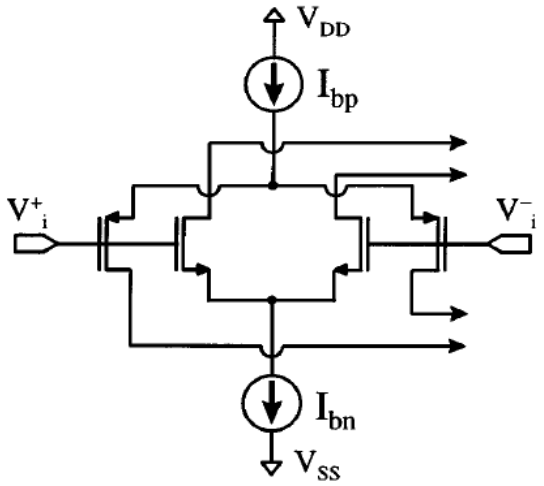

Figure 3.10 Complementary input stage of the opamp.

Another proposed technique [54] uses the back-gate transistor terminals of the amplifier differential pair to apply the input signals as shown in Figure 3.11, as in this way the signals do not have to be higher than the transistor threshold voltage. The main drawback of this approach is that some important amplifier parameters, such as dc gain and gain-bandwidth product, turn out to be rather low as a consequence of the low values of the MOS transistor substrate trans-conductance. Another issue for this structure is the large voltage-dependent input junction capacitance.

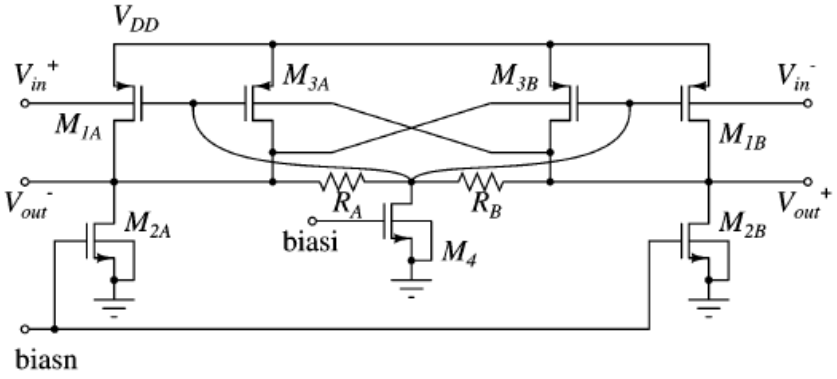

Figure 3.11 Body input structure.

To mitigate the lower dc-gain and narrower UGBW, the body effect was used [55] [56] to change the threshold voltage of the transistors as shown in Figure 3.12, so the input signal can still be applied to the gate of transistors instead of the bulk. However, it is not possible to apply this technique to the single well process, and the forward biasing between the body and source could also be problematic due to current leakage.

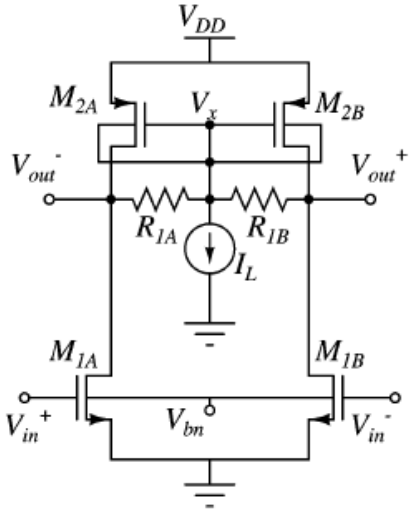

Figure 3.12 Body bias technique.

Finally, the input common-mode level of the amplifier can be level shifted to a lower level if the input stage is PMOS differential pair, or a higher level if the input stage is NMOS differential pair [57]. Two schemes are shown in Figure 3.13 The first one uses one current source to sink the dc current, and the second one attaches one resistor to the input node of the amplifier. The feedback factors for these two schemes are given by

$$\beta_i = \frac{R_{eq} // r_{ds}}{R_{eq} // r_{ds} + R_f} \tag{3.12}$$

$$\beta_r = \frac{R_{eq} // R_B}{R_{eq} // R_B + R_f} \tag{3.13}$$

Where R_{eq} is equal to $R_1//\ldots/R_n$, and r_{ds} is the output resistance of the current source. Since R_B is usually smaller than r_{ds}, the scheme using the current source will be faster. However, this method injects 1/f noise, as well as white noise, from the current source directly to the input of the amplifier. The scheme using the resistor will track with process variation directly, and one more amplifier may be needed to make the current source track the resistor variation.

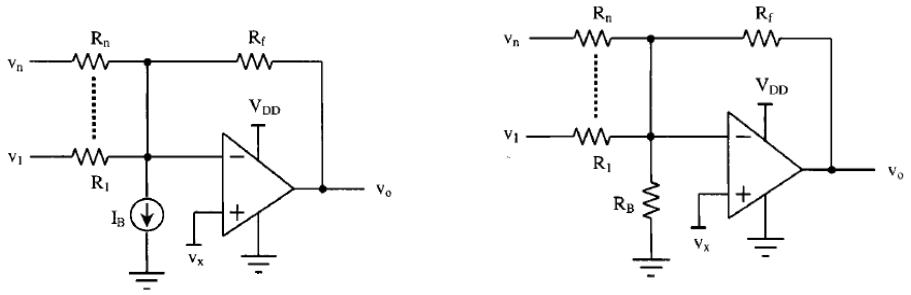

Figure 3.13 Input common-mode level adjustment scheme.

Another two design approaches have been described [58]. The first one shown in Figure 3.14a is based on an amplifier input stage made up by complementary differential pairs, and uses the dynamic level-shifting technique to extend the amplifiers input range up to the rails. By contrast, the second approach in Figure 3.14b relies on an input stage based on a single differential input pair. Rail-to-rail operation is achieved through a closed-loop common mode adapter, which keeps the input common-mode voltage of the input differential pair at an appropriate constant voltage, while leaving the input differential signal unaffected. The second approach bias the input differential pair at a fixed voltage, ensures that the amplifier offset is maintained roughly constant over the entire input voltage range, thereby providing better offset and THD performance. However, the input current in both schemes need to be sufficiently small to make the load effect on the preceding stage negligible.

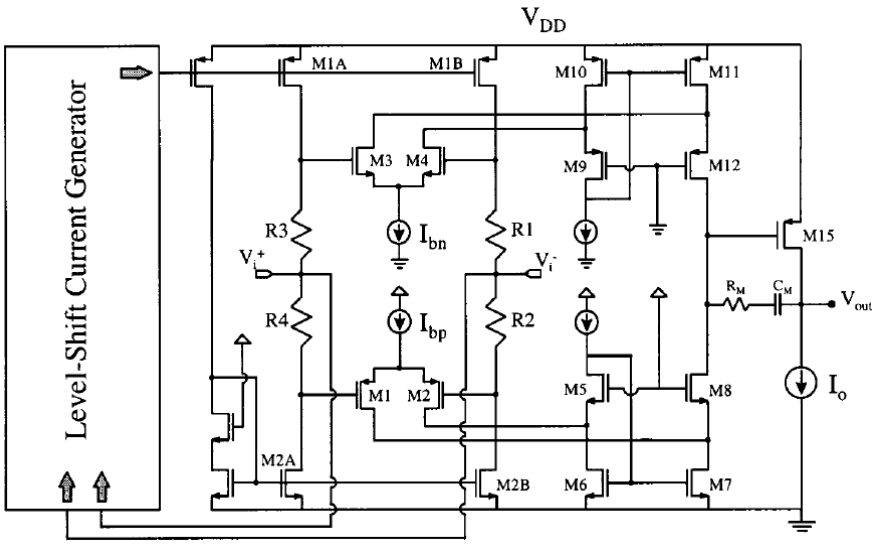

Figure 3.14a Dynamic level-shifting to extend the amplifiers input range.

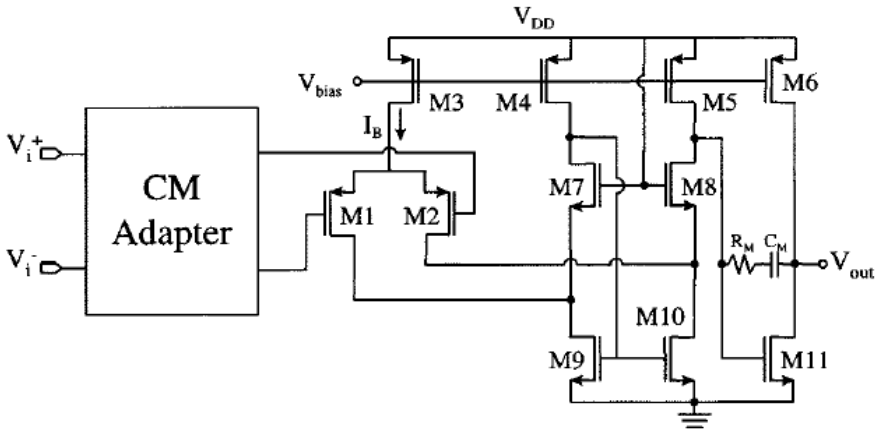

Figure 3.14b closed-loop CM adapter to extend the amplifiers input range.

CHAPTER 4: A 0.8V, 88DB DUAL-CHANNEL AUDIO DELTA-SIGMA DAC WITH HEADPHONE DRIVER

A 0.8V 3rd-order ΔΣ DAC with headphone driver is presented. The circuit requires only one opamp per channel, shared by the internal DAC, the FIR and second-order Sallen-Key low-pass filter, as well as by the headphone driver. The prototype IC implemented in a 0.35μm CMOS process achieved 88dB DR, while consuming 2.5mW from a 0.8V supply.

4.1 Delta-sigma modulator

4.1.1 Quantizer resolution and delta-sigma noise-shaping order selection

The basic criterion to select the order of $\Delta\sum$ modulator and the quantizer resolution is as following

- Criterion 1

  Make the pass band quantization noise negligible so that the analog noise (thermal noise and 1/f noise) dominate in the noise budget.

- Criterion 2

  Make the out-of-band noise low enough to use the low order CT low pass filter as the post filter.

- Criterion 3

  Make clock jitter sensitivity as low as possible in the DT to CT interface.

Based on these criterions, a 3-bit and 7-level quantizer and 3rd-order DSM is chosen. The advantages of the use of a multi-bit DSM are:

1) Smaller idle channel tones and less sensitivity to clock jitter.
2) The reduced quantization noise allows a lower OSR. Therefore the speed of the analog circuit can be relaxed and the power can be saved.
3) More stable.
4) Simpler smoothing filter, since the slewing and the out-of-band noise in the DAC are both reduced.

A tradeoff between the input range and the SNQR is made in determining the noise transfer function (NTF) and the NTF peak gain of 1.8 is chosen to give a $110dB$ SQNR and $-1dBFS$ input range as shown in Figure 4.1. The designed NTF is given by

$$NTF(z) = \frac{(z-1)(z^2-1.999z+1)}{(z-0.5621)(z^2-1.296z+0.5483)} \tag{4.1}$$

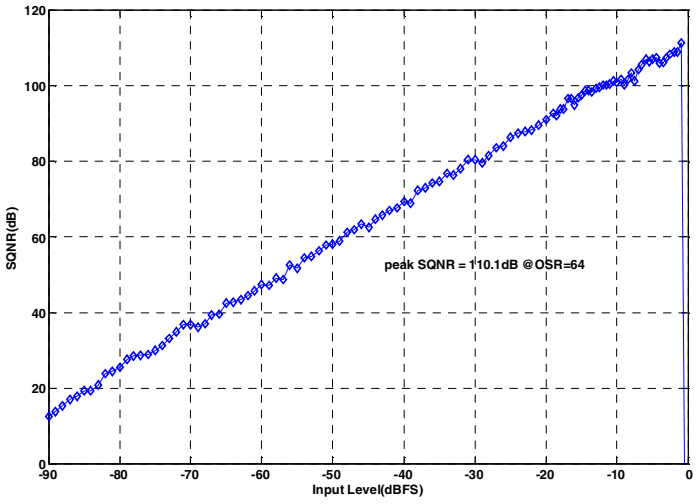

Figure 4.1 SQNR versus input amplitude.

This NTF introduces one zero at DC and two other complex zeros near the edge of the band of interest. This results in 8dB SQNR improvement.

4.1.2 Architecture design of the delta-sigma modulator

In this section, two structures, i.e., cascaded integrated feedback (CIFB) and cascaded integrated feedforward (CIFF), are designed and simulated. The conclusion is made at the end of this section.

4.1.2.1 CIFB

The structure of CIFB is shown in Figure 4.2. Based on the NTF given in (4.1), for CIFB structure, we get the signal transfer function (STF) and NTF as shown in (4.2) and (4.3) with the quantized coefficients shown in Table 1.

$$STF_{cifbq}(z) = \frac{0.10938}{(z-0.5933)(z^2-1.313z+0.5819)} \tag{4.2}$$

$$NTF_{cifbq}(z) = \frac{(z-1)(z^2-2z+1.001)}{(z-0.5933)(z^2-1.313z+0.5819)} \tag{4.3}$$

The purpose of quantizing coefficients is to reduce hardware complexity by eliminating multipliers without degrading the SQNR performance.

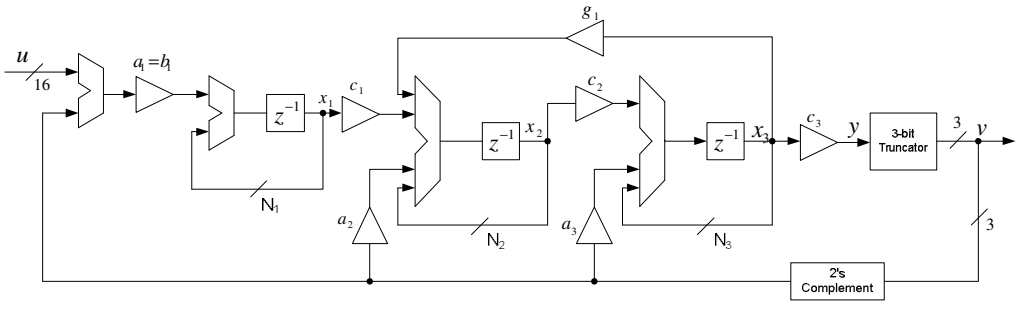

Figure 4.2 Structure of CIFB.

Coefficient	Quantized value
$a_1 = b_1$	$\frac{1}{32}$
a_2	$\frac{1}{16}+\frac{1}{64}$
a_3	$\frac{1}{8}+\frac{1}{32}$
c_1	$\frac{1}{2}$
c_2	1
c_3	4+2+1
g_1	$\frac{1}{1024}+\frac{1}{2048}$

Table 4.1 CIFB Modulator coefficients.

If N_1, N_2, and N_3 are required to quantize the first, second, and third accumulator in the modulator loop, for a desired SNR better than 110dB caused by the finite word length of the accumulator and a full-scale sine wave with power of $M^2/2$, N_1, N_2, and N_3 are given by

$$\frac{1}{a_1^2}\frac{(2^{-N_1})^2}{3}\frac{1}{OSR} < 10^{-11}\frac{M^2}{2} \tag{4.4}$$

$$\frac{1}{(a_1c_1)^2}\frac{(2^{-N_2})^2}{3}\frac{\pi^2}{3(OSR)^3} < 10^{-11}\frac{M^2}{2} \tag{4.5}$$

$$\frac{1}{(a_1c_1c_2)^2}\frac{(2^{-N_3})^2}{3}\frac{\pi^4}{5(OSR)^5} < 10^{-11}\frac{M^2}{2} \tag{4.6}$$

The idea behind (4.4), (4.5), and (4.6) is that the input referred in-band noise power related to quantization is directly coupled into the input for the first accumulator, while for the second and the third accumulator, the quantization noise

is 1st-order and 2nd-order shaped. Solving (4.4), (4.5), and (4.6) gives $N_1 = 17.39$, $N_2 = 13.25$, and $N_3 = 8.53$. However, g_1 is $\frac{1}{1024} + \frac{1}{2048}$ in Table 4.1. To avoid using a zero g_1, at least 11-bit precision is required for the third accumulator. In conclusion, 18, 14, and 11 bits will be used for accumulators in the modulator loop.

4.1.2.2 CIFF

The 3rd-order CIFF structure is shown in Figure 4.3. According to (4.1), the STF and NTF are obtained as the following with the quantized coefficients in Table 4.2.

$$STF_{ciffq} = 1 \tag{4.7}$$

$$NTF_{ciffq} = \frac{(z-1)(z^2 - 2z - 1.001)}{(z-0.5901)(z^2 - 1.285z + 0.5558)} \tag{4.8}$$

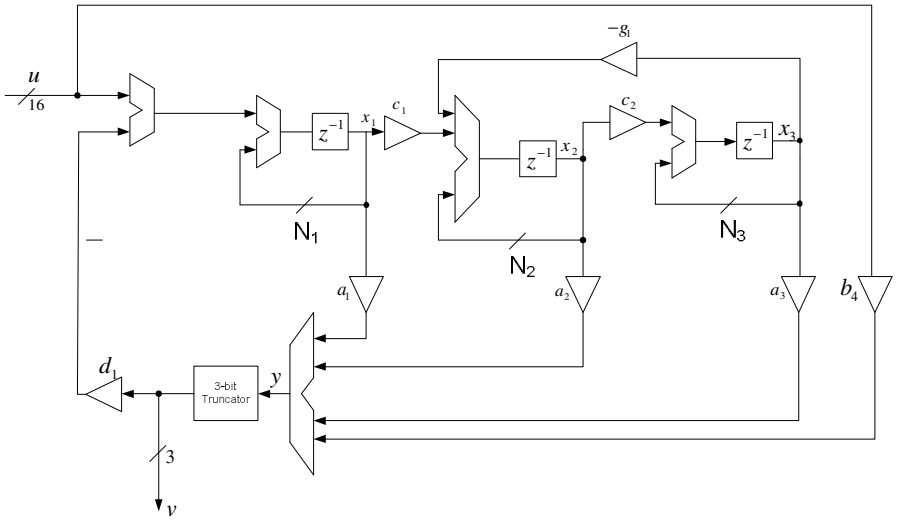

Figure 4.3 CIFF structure

Coefficients	value
a1	1/2+1/16
a2	1/2+1/16
a3	1/2-1/16
c1	1/2
c2	1/4
b1	1
b4	1/2
g1	1/256+1/512
d1	2

Table 4.2 CIFF Modulator coefficients.

Similar to the analysis for the CIFB modulator, for N_1-bit x_1, N_2-bit x_2, and N_3 -bit x_3, we get

$$\frac{1}{b_1^2}\frac{(2^{-N_1})^2}{3}\frac{1}{OSR} < 10^{-11}\frac{M^2}{2} \tag{4.9}$$

$$\frac{1}{(b_1c_1)^2}\frac{(2^{-N_2})^2}{3}\frac{\pi^2}{3(OSR)^3} < 10^{-11}\frac{M^2}{2} \tag{4.10}$$

$$\frac{1}{(b_1c_1c_2)^2}\frac{(2^{-N_3})^2}{3}\frac{\pi^4}{5(OSR)^5} < 10^{-11}\frac{M^2}{2} \tag{4.11}$$

Solving (4.9), (4.10), and (4.11) gives $N_1 = 14.39$, $N_2 = 10.25$, and $N_3 = 7.53$. Therefore, it is required to use 15, 11, and 9 (to avoid changing the coefficients of the resonator) bits for the first, second, and third accumulator in the modulator.

4.1.2.3 Summary

Table 4.3 summarizes the discussion so far. For accumulators in the CIFF structure, less bits are required to achieve the desired SQNR. This should not come as a surprise. For the loop filter in the CIFF structure, it only processes the errors between the input and the output. It is this property that makes it less susceptible to coefficients truncation than that of the competing architectures.

Type	1st accumulator	2nd accumulator	3rd accumulator	STF	SQNR(-6dBFS)
CIFB	18bits	14bits	11bits	LPF	105dB
CIFF	15bits	11bits	9bits	APF	103dB

Table 4.3 Word length for accumulators in CIFB and CIFF modulators.

4.2 DAC, analog LPF, and headphone driver

A low-voltage and low-power DAC architecture is proposed. The DAC is combined with the 1st-order FIR, 2nd-order Sallen-Key filter, and the headphone driver as shown in Figure 4.4. It uses one opamp per channel to implement D/A conversion, 1st-order FIR and 2nd-order IIR filtering, as well as power amplification for the headphone. The opamp provides a virtual ground at nodes A and B for the DAC. An analog 1st-order FIR filter is also integrated into this DAC by duplicating the original DAC elements with control signal delayed by one clock cycle. This introduces one zero at one-half of the sampling frequency, and reduces the clock jitter sensitivity. The embedded 2nd-order Sallen-Key low-pass filter has a -3dB cutoff frequency at 150kHz, and its pole Q is 0.707. The values of all

resistors and capacitors were optimized to achieve the minimum capacitor area for the given pole-Q, cutoff frequency, and the targeted SNR. Four extra resistors were added to make the output common-mode voltage $V_{dd}/2$.

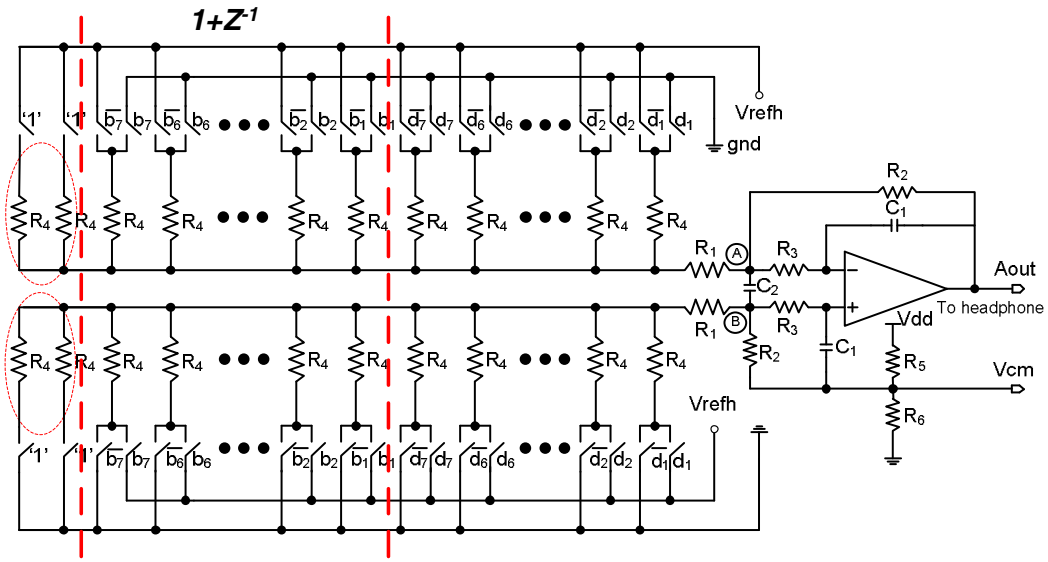

Figure 4.4 Proposed DAC structure.

4.2.1 DAC

Switched capacitor DAC is widely used because of its excellent matching between capacitors and immunity to clock jitter. However, it is difficult to turn on floating switches and capacitor size needs to be big to reduce kT/C noise when the power supply voltage goes down to sub-1V. A current steering DAC requires a relatively big overdrive voltage to achieve good matching. This poses a stringent requirement for the low power supply voltage. In the resistor array DAC shown in Figure 4.5, all switches are connected either to the high reference (V_{dd}) or to the low reference voltage (ground). This avoids the problem with floating switches.

The value of R_1 is chosen carefully to reduce the size of R_4 without sacrificing matching between them. Data weighted averaging (DWA) technique is used to provide first order noise shaping for the mismatch between DAC elements. Seven elements are used for the 7-level quantizer. This helps to suppress the spurs caused by DWA when the input signal is small. Figure 4.6 shows the PSD of the DAC output with seven and six-element DAC respectively. The input is a 1.03kHz -80dB sine wave with -60dB dc offset and 1% resistor mismatch. Although the SNDR is almost the same for the seven and six-element DAC, the tone level for the six-element DAC is at least 10dB higher. In audio application, tones are detrimental even they are 20dB below the noise floor [4].

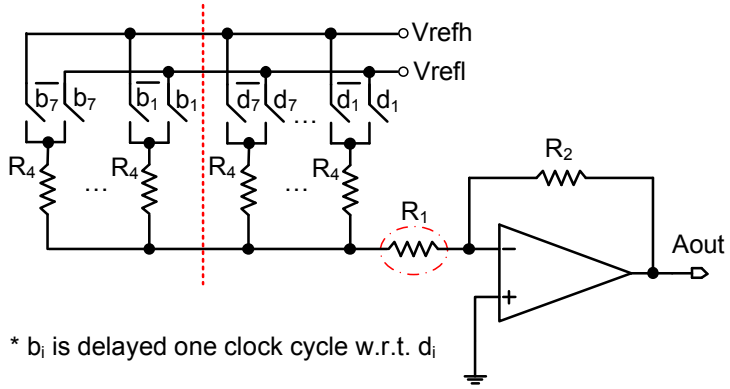

Figure 4.5 Resistor array DAC with first-order FIR filtering.

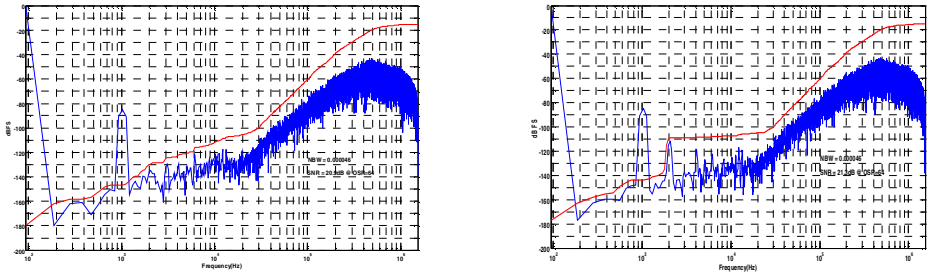

Figure 4.6 PSD for 7-element and 6-element DAC.

Return-to-zero (RZ) signal is good at reducing the effect of inter symbol interference (ISI), but it has poor jitter performance. For non-return-to-zero (NRZ) signal shown in Figure 4.7, assuming x(n) is the ideal DAC output, the DAC error due to clock jitter is given by

$$e_{dac-jitter} = (x(n) - x(n-1))\frac{\Delta t(n)}{T_{clk}} \tag{4.12}$$

Note that if the DAC sequence keeps unchanged, clock jitter has no effects on DAC output. The inband RMS value of the DAC error due to clock jitter can then be written as

$$N_{dac-jitter} = \frac{Jitter_{RMS}}{T_{clk}\sqrt{OSR}}\sqrt{\int_0^{0.5}\frac{\Delta^2}{12}\,|\,NTF(e^{j2\pi f})(1-e^{-j2\pi f})\,|^2\,df} \tag{4.13}$$

where $\Delta^2/12$ is the quantization noise. If the 1st-order FIR filter is taken into consideration, it becomes

$$N_{dac-jitter} = \frac{Jitter_{RMS}}{T_{clk}\sqrt{OSR}}\sqrt{\int_0^{0.5}\frac{\Delta^2}{12}\,|\,NTF(e^{j2\pi f})(1-e^{-j2\pi f})(1+e^{-j2\pi f})\,|^2\,df} \tag{4.14}$$

The simulated SNR due to clock jitter (only random cycle-to-cycle jitter is considered) with and without the 1st-order FIR is shown in Figure 4.8. It is seen that SNR has at least 6dB improvement with FIR filter included. In Figure 4.5, an analog 1st-order FIR filter is realized by duplicating the original DAC elements with control signal delayed by one clock cycle. It introduces a zero at one half of the sampling frequency and hence reduces the clock jitter sensitivity.

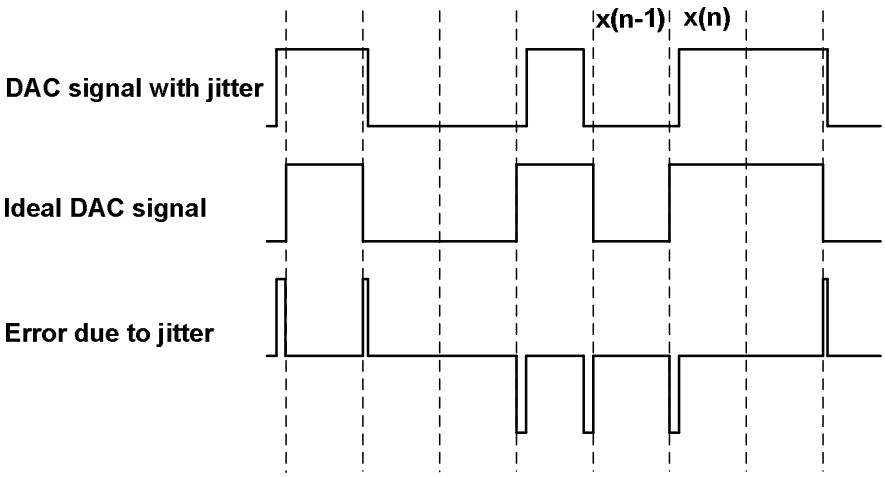

Figure 4.7 DAC error due to clock jitter.

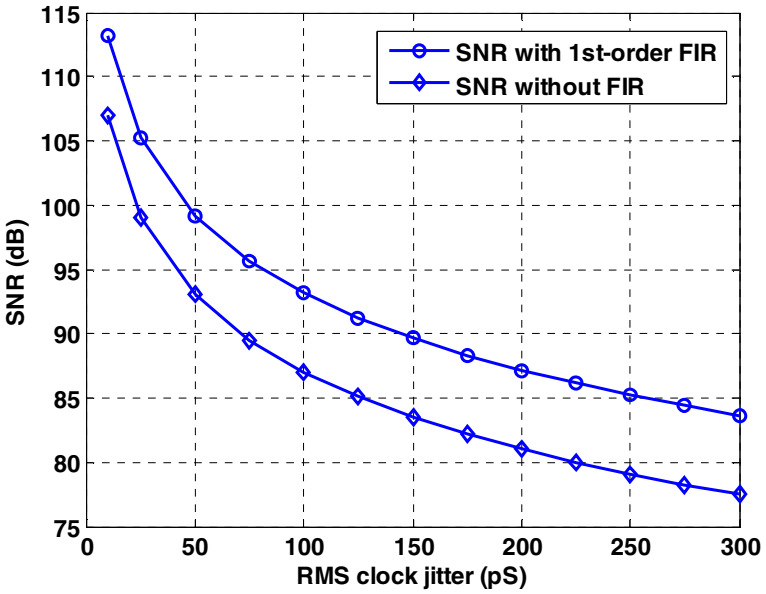

Figure 4.8 SNR with and without FIR filtering.

4.2.2 Analog LPF and headphone driver

Sallen-Key type filter shown in Figure 4.9 requires one amplifier to implement 2nd-order low-pass filtering. The pole frequency is sloppily defined due

to RC variation. However, in audio application, the cut-off frequency can be around 10 times higher than the audio bandwidth. Hence the variation of pole frequency will not affect the frequency response of the band-of-interest.

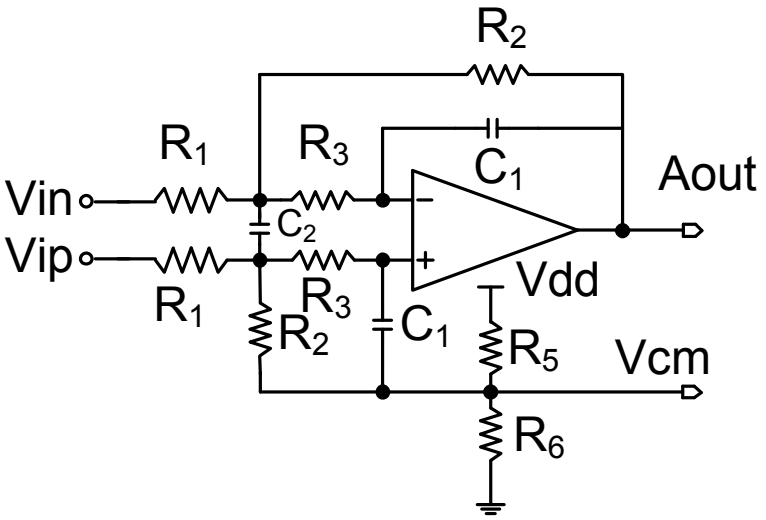

Figure 4.9 2nd-order Sallen-Key low-pass filter.

The transfer function for the 2nd-order Sallen-Key filter is given by

$$H(s) = \frac{-R_2/R_1}{2R_2R_3C_1C_2S^2 + (R_2 + R_3 + R_2R_3/R_1)S + 1} \tag{4.15}$$

Instead of using the unity DC-gain, -6dB DC gain is chosen for this filter when both the negative and positive input of this filter are full-scale. Assuming $R_3=mR_2=mR$, $C_2=nC_1=nC$, The 3dB cutoff frequency and pole-Q are

$$\omega_{-3dB} = \frac{1}{\sqrt{2mnRC}} \tag{4.16}$$

$$Q = \frac{\sqrt{2mn}}{1+1.5m} \tag{4.17}$$

The total capacitor area is

$$C_{total} = (1+n)C = (1+\frac{Q^2(1+1.5m)^2}{2m})C \tag{4.18}$$

If the derivative is taken for (4.18), the minimum capacitor area is achieved when m is equal to 2/3. If pole Q is 0.707, then n will be 1.5.

The output referred noise density for the filter is then

$$V_{on} / \sqrt{Hz} = \sqrt{2kTR(8+9m)} / \sqrt{Hz} = \sqrt{28kTR} / \sqrt{Hz} \qquad (4.19)$$

According to the noise budget for the filter, the resistor value can be calculated according to (4.19). Substitute the resistor value into (4.16) will get the capacitor value. Table 4.4 summarizes the nominal values for components in the 2nd-order Sallen-Key filter.

R1	30k ohm
R2	15k ohm
R3	10k ohm
R4/R5	45k ohm
C1	50 pF
C2	75 pF

Table 4.4 Components values for the 2nd-order Sallen-Key filter.

The amplifier in the filter is also the headphone driver. Although Class-D output stage has higher power efficiency and is used widely in audio application, it requires further off-chip filtering and has the IM signal around the switching frequency. Class-AB output stage is well-known for its good linearity and power efficiency. For amplifier with class-AB output stage, multi-stage implementation with complex compensation to guarantee stability and achieve high gain is not unusual [59-62]. When the power supply voltage goes down to sub-1V, regulating

the bias current of the output drive transistor becomes extremely difficult. The output stage of the opamp [63] incorporates a minimum current selector in the feedback loop, which contains the split output transistors of the first stage of the opamp. The loop regulates the bias current of the output transistors. The simulated loaded voltage gain of this opamp is 65dB; and the UGBW is 7MHz.

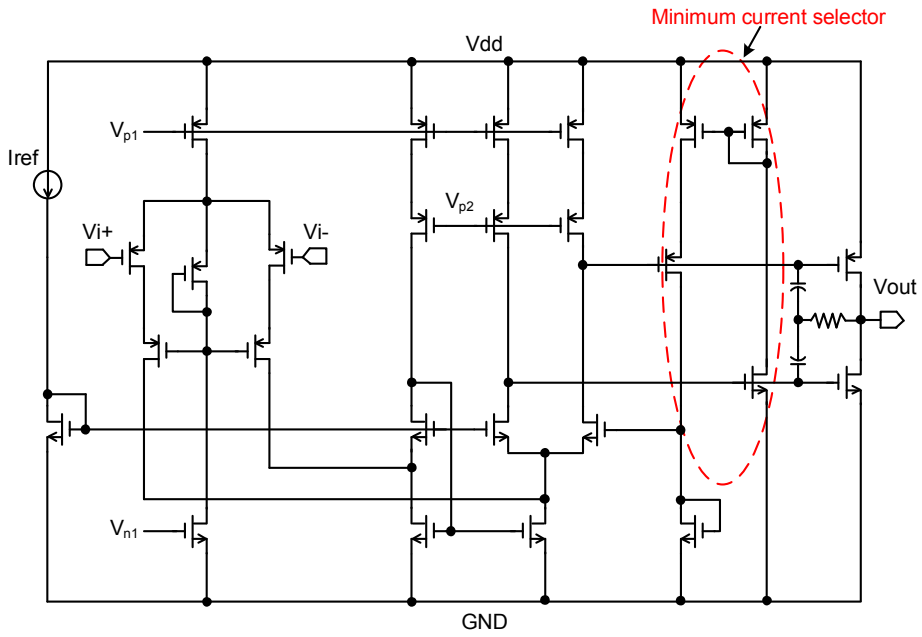

Figure 4.10 Opamp with class-AB output stage.

4.3 Measurement Results

The DAC was fabricated in Asahi Kasei Microsystem's 0.35μm CMOS technology, and occupies 1.6 × 1.3mm^2 active die area. The measurement setup is shown in Figure 4.11. AWG 520 (arbitrary waveform generator) was used to generate the digital input, the output of the digital chip (developed by Kyehyung

Lee) includes the 6.144MHz clock and the output from DWA module. The DWA data are shared by the left and right channel. Figure 4.12 shows the measured overall output spectrum for a 1.17kHz, -60dB sine-wave input using a 0.8V power supply.

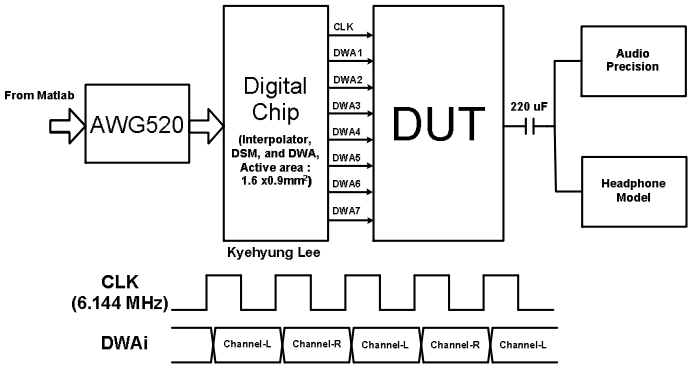

Figure 4.11 Measurement setup.

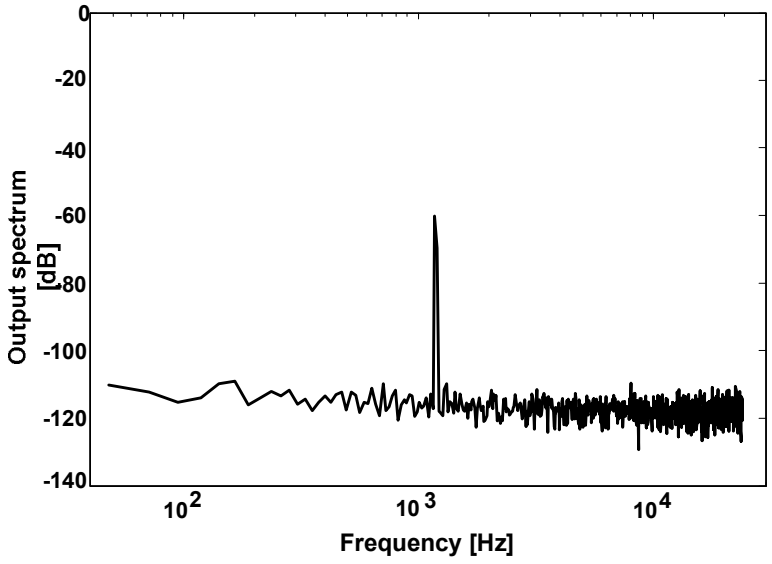

Figure 4.12 Measured output spectrum.

There are no idle tones present in the quantization noise. The spurs caused by DWA rotation are also negligible (below -109dB). The SNDR versus input level from -85dB to 0dB (relative to 56% of the supply voltage) is shown in Figure 4.13, for a supply voltage of 0.8V. The SNDR was measured over a 24kHz wide audio band. Without A-weighting, the prototype achieves 69dB peak SNDR and 88dB dynamic range with a 0.8V supply voltage. Using a 0.7V supply, the peak SNDR and the dynamic range are reduced to 68dB and 87dB, respectively.

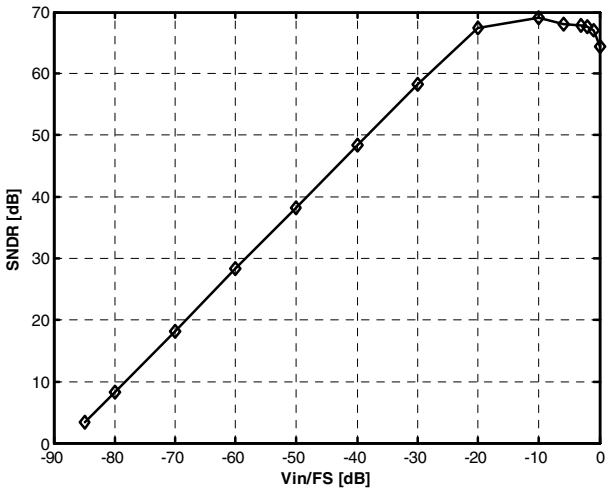

Figure 4.13 Measured SNDR.

The chips consume 2.5mW power at 0.8V supply. The peak SNDR is limited by the second harmonic distortion of the single-ended opamp for large input signal swings. The dynamic range and the peak SNDR gradually improve for supply voltages from 0.7V to 1.5V with minimum power consumption penalty as shown in Figure 4.14. The die photograph is shown in Figure 4.16. Table 4.5 summarizes the performance of the chip.

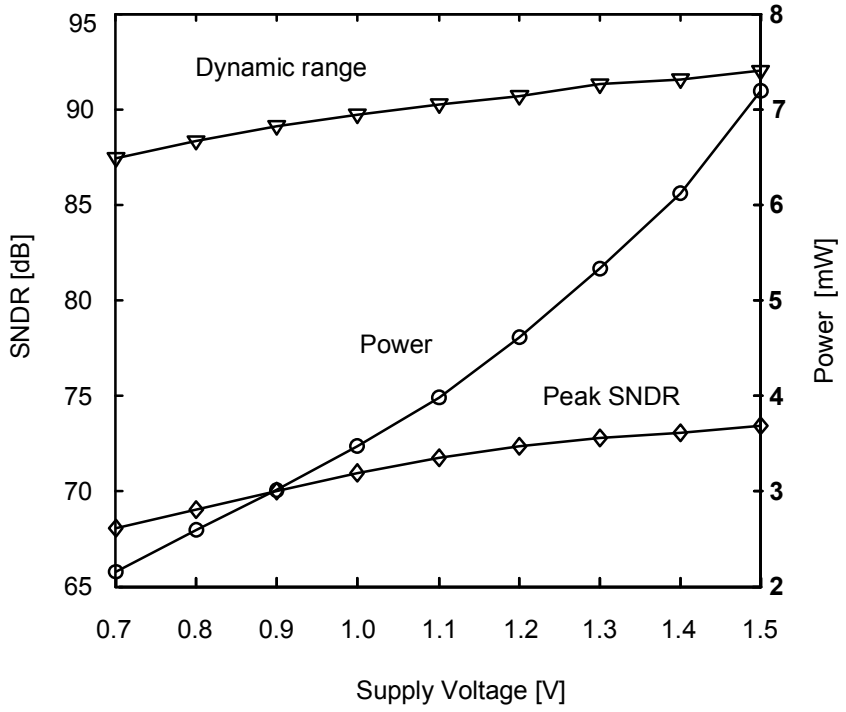

Figure 4.14 Performance versus supply voltage.

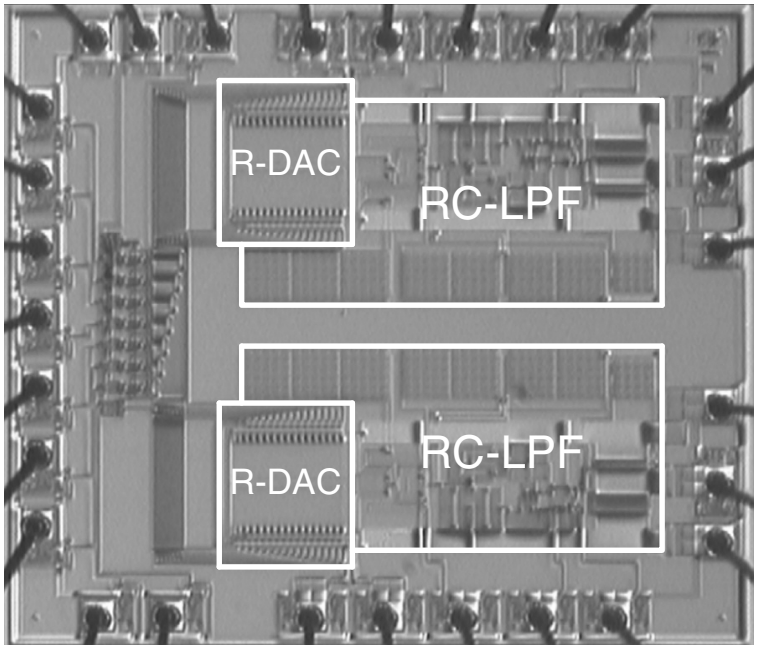

Figure 4.15 Die photograph.

Power supply voltage	0.8 V
Signal bandwidth	24 kHz
Clock frequency	3.072 MHz
Oversampling ratio	64
Load	Headphone (16 Ω ll 300 pF)
Total power consumption	2.5 mW
Output range	0.45 V_{PP} (single-ended)
Peak SNDR	69 dB @ Vdd = 0.8 V 68 dB @ Vdd = 0.7 V
Dynamic range	88 dB @ Vdd = 0.8 V 87 dB @ Vdd = 0.7 V
Active die area	1.6 X 1.3 mm^2
Technology	0.35μm CMOS

Table 4.5 Performance summary.

4.4 Conclusion

A 0.8V 3rd-order ΔΣ DAC with headphone driver is presented. The circuit requires only one opamp per channel, shared by the internal DAC, the FIR and second-order Sallen-Key low-pass filter, as well as by the headphone driver. The prototype IC implemented in a 0.35μm CMOS process achieved 88dB DR, while consuming 2.6mW from a 0.8V supply.

Compared to the other reported audio delta-sigma DACs, this dual-channel DAC has the lower supply voltage of 0.8V, lower power consumption of 2.6 mW and the heaviest load, which is 16 ohm in parallel with 300pF. This is actually the first published sub-1V audio DAC with headphone driver in the world.

Refs	DR/SNDR [dB]	Supply [V]	Load	Power [mW]	Process [um CMOS]
[Fuj98]	87/81	1.5	10 kΩ	4.1	0.6
[Ada98]	113/100	5.0	1 kΩ	250	0.6
[Fuj00]	120/102	5.0	0.6 kΩ	310	0.5
[Ann02]	98/86	3.3	15 kΩ	56	0.35
[Ann05]	97/88	3.3	40kΩ	14.5	0.35
This work	88/69	0.8	16Ω	2.6	0.35

Table 4.6 Performance comparison.

Chapter 5: A 0.8V 10-bit 10MSPS pipelined ADC

A 0.8V pipelined ADC based on a novel high-performance track-and-hold amplifier (THA) is presented. The track-and-hold amplifier employs the continuous-time (CT) correlated double sampling (CDS) scheme, which makes it insensitive to the nonidealities of the amplifier, including dc offset, 1/f noise, and the finite dc gain [33] [64].

5.1 Pipeline architecture

The architecture of the pipelined ADC is shown in Figure 5.1. The analog signal is first sampled by a track-and-hold amplifier (THA). Then the held signal goes into the pipelined stage. The 1.5-bit sub-ADC is used to relax the comparator requirements. The MDAC is based on the high-performance THA which will be explained in detail. The targeted specification of the pipelined ADC is given in Table 5.1.

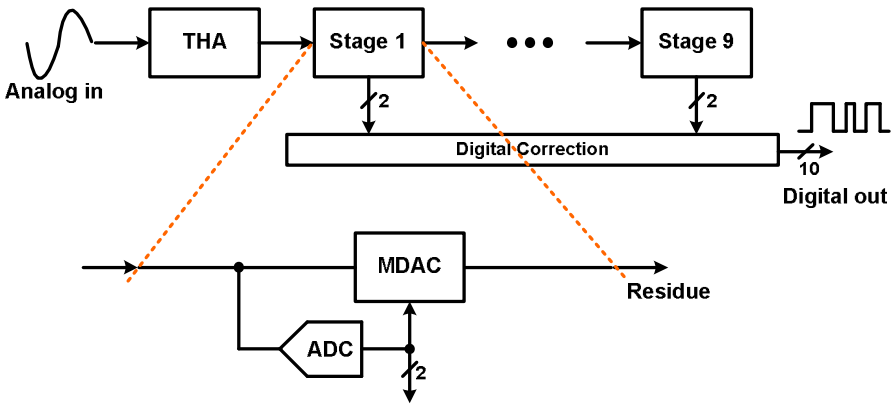

Figure 5.1 Pipeline architecture.

Resolution	10 bits
Conversion Rate	10 MSPS
Technology	0.18 μm CMOS
Supply Voltage	0.8V

Table 5.1 Target specification.

5.2 Circuit implementation

5.2.1 Low-voltage THA

The low-voltage THA with CDS is shown in Figure 5.2. During hold phase ($\phi_2 = 1$), capacitor C_3 across the amplifier holds the output voltage; switch S_1 provides the shunt path for the input signal, and capacitor C_2 stores the opamp's input error signal, including dc offset and noise of the opamp, as well as the signal voltage -Vout/A (A is the dc gain of the opamp). Capacitor C_1 and switch S_2 forms a highpass filter which suppresses the input signal leakage further at node B. During the tracking phase, the input signal goes through the improved virtual ground, which makes this THA insensitive to the nonidealities of the opamp. The voltage at node A is

$$V_{cm} + v_i(T)R_{on}/(R_1+R_{on}) + v_o(T)R_{on}/(R_2+R_{on}) + (v_o(T)-v_o(t+T))/A \qquad (5.1)$$

where A is the DC gain of the opamp, and $v_i(T)$ and $v_o(T)$ are input and output voltages at the end moment of the hold phase. If R_1 equals R_2, the second and third term in (5.1) will cancel out, otherwise, the ratio between R_{on} and R_1+R_{on} needs to be sufficiently small in order not to cause second-order harmonic.

The input common-mode voltage of the opamp is shifted to the analog ground in this circuit by the integrated CDS circuitry. This greatly eases the low-voltage opamp design, where input common-mode voltage is generally a limiting factor to reduce the supply voltage. Switch S_1 in the conceptual block diagram in Figure 5.2 is connected to the output common-mode level $V_{dd}/2$. Resistor R_1, R_2,and capacitor C_1 are split in the actual circuit implementation, so switch S_1 becomes two switches, one is connected to Vdd, the other is conncted to ground. All switches in the proposed low-voltage THA are connected either to Vdd or ground, which avoids the problem of floating switches.

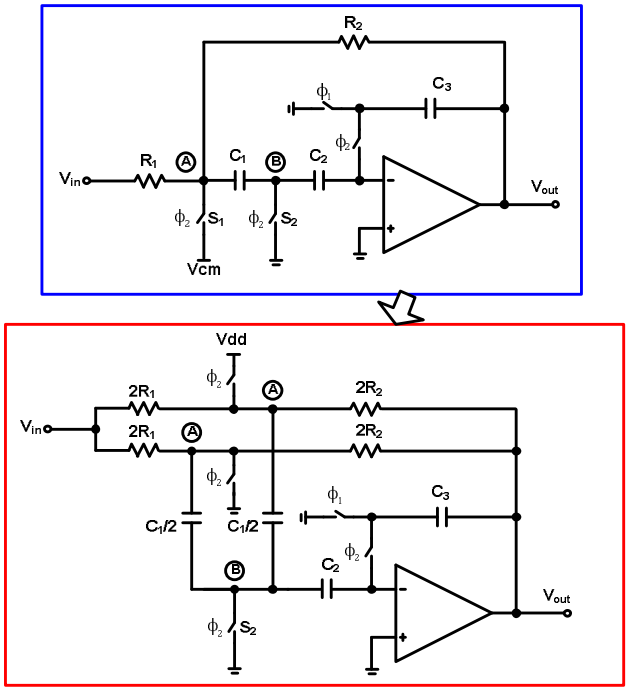

Figure 5.2 Low-voltage THA.

The amplifier is shown in Figure 5.3. Internally compensated two-stage fully-differential amplifier was used to achieve moderate gain and large output

swing with a low power supply voltage. The input common-mode level of the CMFB amplifier is shifted to be within its input common-mode range by adding two current sources at the input nodes of the CMFB amplifier [65].

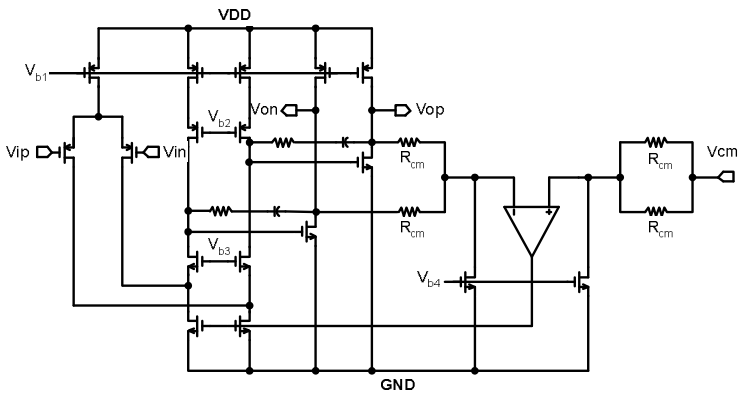

Figure 5.3 Two-stage opamp.

Figure 5.4 shows the simulation result of the low-voltage THA using a 0.8V power supply voltage. The THD is 92dB below the signal level. The clock frequency is 10MHz, the input signal has a frequency of 1MHz, and peak-to-peak voltage 0.4V.The simulated opamp dc gain is 68dB, and UGBW is 109MHz.

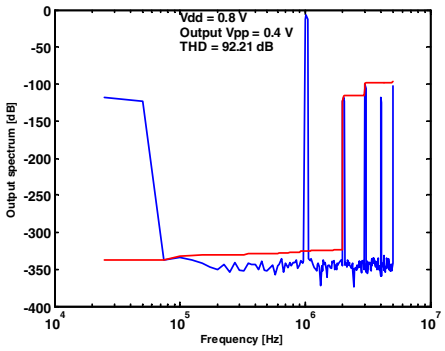

Figure 5.4 Simulated THA output spectrum.

5.2.2 MDAC

The MDAC (multiplying DAC) in the pipelined ADC uses both R and C elements, as shown in Figure 5.5. The MADC is built based on the aforementioned low-voltage THA. During clock phase ϕ_2, the circuit works as an inverting amplifier with a gain set by the ratio of R_2/R_1, and the input signal charges go through the improved virtual ground at nodes A, which makes them insensitive to the nonidealities of the opamp. The stage residue will be determined by connecting resistors R_3 to V_{refp} (V_{dd}), V_{refn} (ground), or keeping them floating at this period. The matching accuracy between resistors R_2 and R_1 needs to be at least 10-bit linearity. This could be problematic in some processes, and some kind of calibration techniques may be required [66]-[68]. The signal leakage at node A results in inaccurate interstage gain, and is determined by the ratio of the on-resistance of switch S_1 and R_1, as well as R_2. The MDAC in the right side of Figure 5.6 has one more switch and two more clock phases, which makes CDS effective in both track and hold phases with shorter time period ϕ_1 and ϕ_2.

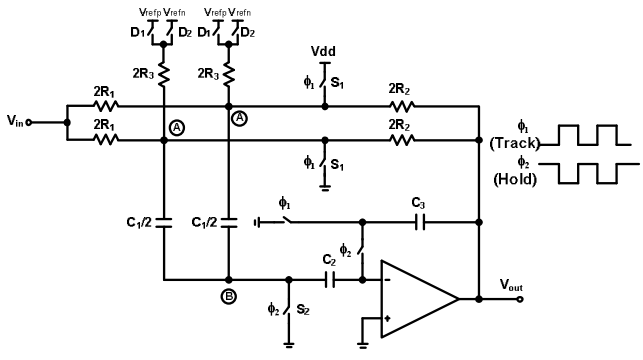

Figure 5.5 Low-voltage MDAC with CDS technique.

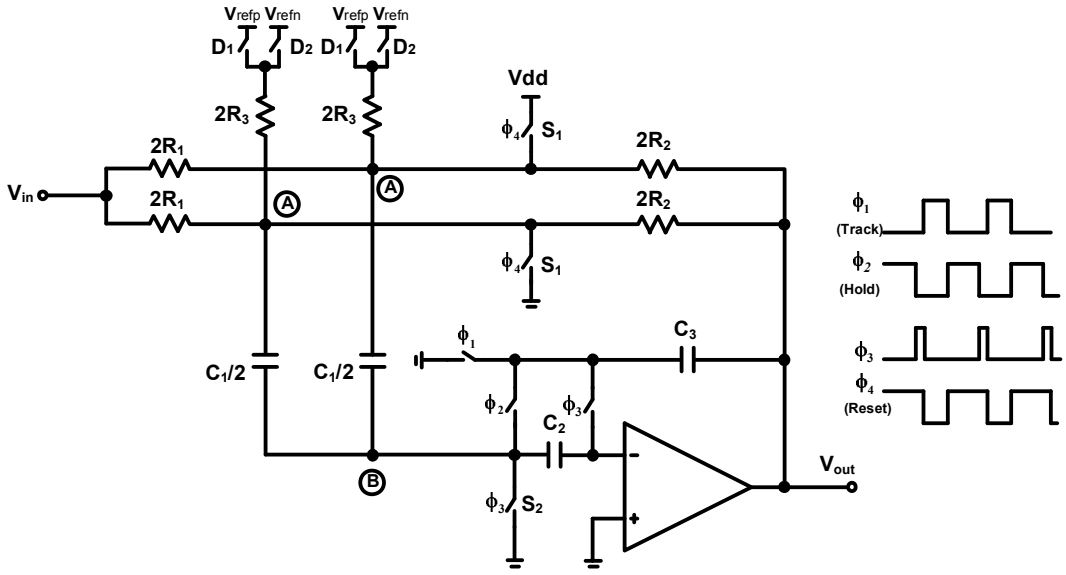

Figure 5.6 Low-voltage MDAC with CDS technique.

5.2.3 Sub-ADC

Switched-RC technique [51-52] is used to implement the low-voltage sub-ADC as shown in Figure 5.7. Applying charge conservation law at node V_{xp} and V_{xn} gives (assuming V_{REFP} is V_{dd} and V_{REFN} is ground)

$$v_{xp} - v_{xn} = \frac{2(v_{ip} - v_{in})C_1 - 2V_{dd}C_2}{2C_1 + C_2} \tag{5.2}$$

Two preamps are used to prevent the kickback from the latch and to reduce the offset. An open loop offset cancellation circuitry is also included.

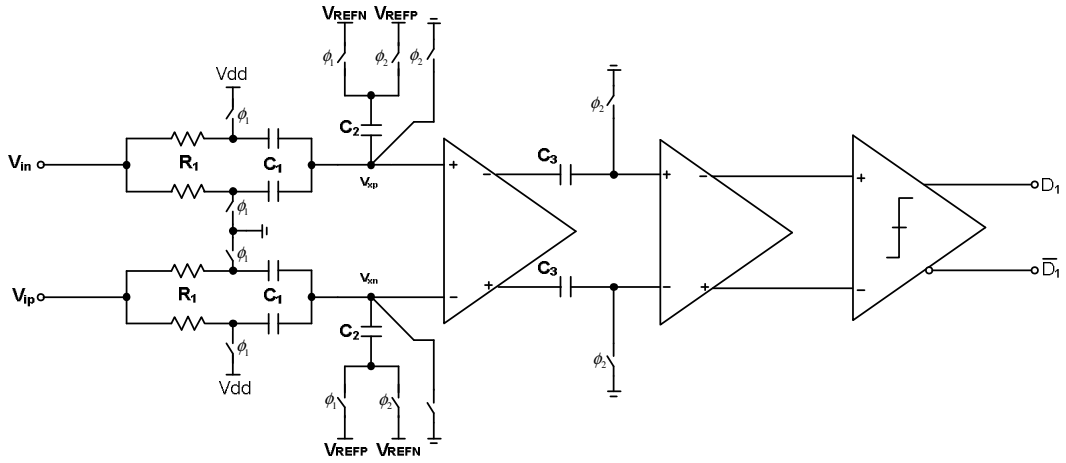

Figure 5.7 Low-voltage sub-ADC.

5.3 Simulation results

The 10-bit pipelined ADC was fabricated in a 0.18μm CMOS technology, and occupies 3.9 x 3.4 mm^2 active area. Figure 5.8 shows the output spectrum of the simulation result from a 0.8V power supply voltage. This ADC achieves 59 dB SQNR with a 1.1 MHz sine wave input at 10 MHz sampling frequency, and 57.5dB SQNR with a 4.9MHz sine wave input, while consuming 20 mW power. Figure 5.9 shows the die photograph of the prototype ADC.

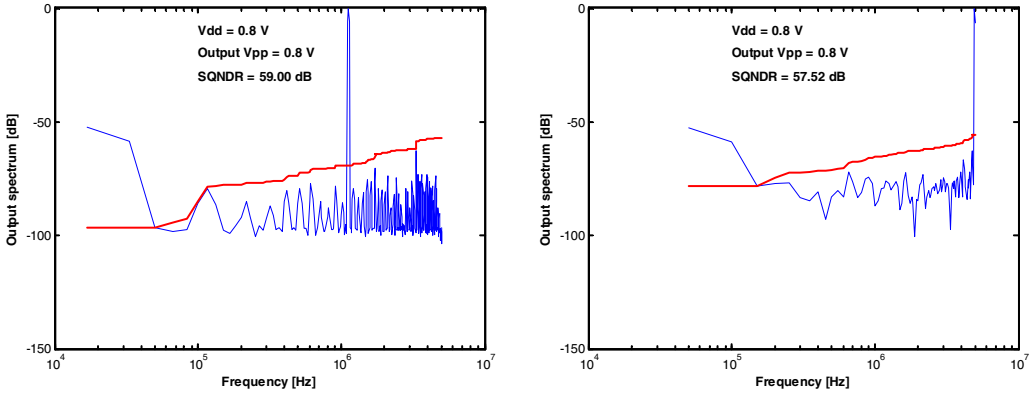

Figure 5.8 Simulated output spectrum of the 10-bit pipelined ADC.

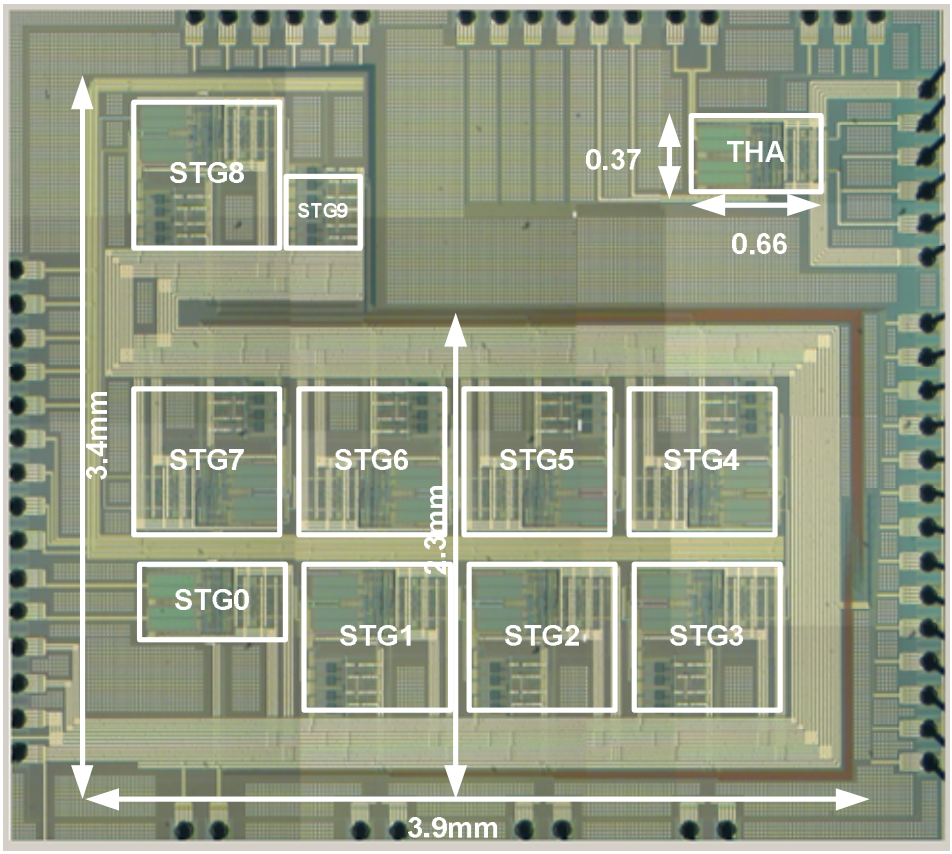

Figure 5.9 Die photograph.

CHAPTER 6: CONCLUSION

Two novel structures: one is a low-voltage audio Delta-Sigma DAC, the other one is a low-voltage pipelined ADC, are presented. The sub-1V audio ΔΣ DAC requires only one amplifier per channel to implement D/A conversion, 1st-order FIR and 2nd-order IIR filtering, as well as power amplification for the headphone. The low-voltage pipelined ADC uses the novel MDAC based on a low-voltage high-accuracy track-and-hold amplifier. This THA uses CDS and AC coupling to reduce the effects of opamp imperfections. Two prototypes, one is a 0.8V, 88dB dual-channel audio ΔΣ DAC with headphone driver, the other one is a 0.8V, 10-bit, 10MS/s pipelined ADC were fabricated in standard CMOS process. The effectiveness of the proposed techniques is demonstrated in simulation as well as in experiment.

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