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Material defect characterization has proved to be a valuable tool in today's submicron Metal-Oxide-Semiconductor Field Effect Transistor development. As the complexity of new processes grows, devices have to become more reliable in order to stand several levels of plasma etching, ion implantation and three or more layers of metallization. DLTS and photocapacitance have been used to characterize oxygen induced microdefects and stacking faults in silicon. Stacking faults in wafers with low carbon impurity were electrically active and an energy level E_c-E_t=.48 +/- .05 eV was detected. Wafers with a trace of carbon did not show any electrically active centers. From this observation, carbon

was implanted at $Si-SiO_2$ interface in MOSFET devices. Carbon implanted devices with an effective gate length of 0.8 micron were subjected to hot carriers degradation and a lower degradation was detected.

Characterization of Oxygen and Carbon Effects in Silicon Material and MOSFET Devices

by

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Typed by researcher for: Homayoon Haddad

To my mother, wife, and son

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1. INTRODUCTION

Silicon material and devices have continued to dominate the integrated circuit industry for the last three decades. Silicon is undoubtedly the most widely researched semiconductor. The projections of new investments on research and development on submicron CMOS and BICMOS processes and creation of SEMATECH show the commitment to this material for a long time in the future. Silicon has been through a history of continuing perfection. Improved perfection of silicon crystals will enhance device and circuit performance and reliability . There has been a constant interest in imperfections and impurities in the crystals and devices since early semiconductor diodes through today's ULSI circuits.

Resent submicron process developments have exposed the need for well understood materials characterization. Specifically the power supply scaling for submicron MOSFET devices from 5.0 volts to 3.3 or 2.2 volts due to hot carriers requires an in-depth defect characterization at the $Si-SiO_2$ interface. Since the subject of imperfections and defects tends to be a dynamic and rapidly changing, it is difficult to obtain a clear picture of the available data. One of the important considerations is the condition of each

individual industrial or university laboratory. Since the defects and imperfections are very closely related to the yield and cleanliness of the equipment set and the process, a unified and comprehensive theory is very difficult to obtain. For example, leakage currents of 4 pA to 500 uA per stacking fault have been reported, and for dislocations in silicon energy levels from 1.2 eV to 0.3 eV have been measured.

There are two main parts to this research work, the first part is related to the electrical characterization of oxygen induced microdefects and the other part is related to sub-micron device reliability. In both cases it has been found that the role of carbon is the determining factor.

1.1 ELECTRICAL CHARACTERIZATION ON OXYGEN INDUCED MICRODEFECTS

Oxygen in silicon was discovered by C.S. Fuller at Bell labs in 1954. He reported the observation of oxygen related thermal donors which appear on annealing at 450 C. This discovery marked the beginning of what we now know to be process-induced defects. However many other process-induced defects have appeared since then, e.g., metal related defects, oxide related defects, new thermal donors which appear at 650 C and ion-implantation defects. There has been considerable progress on the microscopic identification of defects with the use of better tools such as SEM and TEM;

however the electrical characterization has been limited.

In this work CZ-grown wafers with oxygen concentration of about $1.0x10^{18}$ cm^{-3} were heat treated to induce a large number of precipitates and stacking faults. Deep level transient spectroscopy (DLTS) and photocapacitance measurements indicated a correlation between the stacking fault size and trap density when the initial carbon level is below the measurement system's detection limit. An energy level of $E_c-E_t=.48ev$ has been detected with both DLTS and photocapacitance measurement systems. However, wafers with a small trace of carbon did not show any electrical activity, even in the presence of stacking faults.

1.2 SUBMICRON N-CHANNEL MOSFET DEVICE RELIABILITY

Device problems due to hot carriers have been recognized as one of the major constraints in submicron device scaling. The injection of hot carriers generated by impact ionization in the high field region degrades the device characteristics.

Submicron n-channel transistors were subjected to hot carriers aging to investigate the properties of electrically active defects in SiO_2 and at $Si-SiO_2$ interface. These defect are important because hot carrier cause instabilities in threshold voltage and drive current. Devices with effective gate lengths of .8 micron were subjected to hot electron (high V_d and medium V_g) and hot hole degradation condi-

tions (high V_d and low V_g) and then to high temperature to investigate the detrapping as a function of temperature.

Carbon was implanted at 15 Kev with concentrations of 1E16 to 1E20 /cm^3 and also was incorporated during growth of a silicon ingot at 2.4 PPMA. Carbon reduced the device's aging process. This suggests a new way to improve the $Si-SiO_2$ interface that with optimization might be able to provide of submicron devices with no hot carrier degradation.

2. TECHNICAL BACKGROUND

In this chapter, the theoretical background of oxygen induced micordefects and device hot carriers effects are described. The first section will discuss n-type silicon heat treatments, microprecipitates, stacking fault generation and their electrical activity. The second section will be on n-channel MOSFET transistor hot carrier reliability effects.

2.1 OXYGEN INDUCED MICRODEFECTS IN N-TYPE SILICON

The growth of high-purity silicon material and the fabrication of electronic devices and circuits uses a long series of complicated chemical, physical and thermal processes. Silicon is manufactured by refining silica sand through several carbon reduction steps. The result is known as polysilicon which is used for single crystal silicon production. Single crystal silicon is produced in the form of long cylindrical ingots. These ingots are sliced and chemically and mechanically polished to produce damaged-free surfaces. Throughout these processes the purity requirement are extremely high and normally in the part per billion range.

2.1.1 OXYGEN IN SILICON

Oxygen is incorporated in silicon during the crystal growth at a concentration of 10^{18} atom/cm^3 . The source of oxygen is the reaction of molten silicon with its container (quartz crucible). The oxygen concentration varies along a silicon ingot, from a high oxygen concentration at the seed section to a low concentration at the tang section. This is due to crucible-melt interface contact area. Other factor such as crucible rotation velocity affect the dissolution rate of oxygen from crucible into the melt and can be used to make an ingot with relatively uniform oxygen concentration. The solubility of oxygen in silicon decreases exponentially with temperature [1]. This means at temperature higher than 300 C oxygen becomes mobile and reduces its supersaturation via outdiffusion or formation of SiO_x (cluster precipitates). Kimerling and Patel [2] have summarized the behavior of oxygen in silicon with heating in various temperature regimes as following.

(1) 400-500 C: Electrically active, oxygen-related donors are formed, presumably due to oxygen aggregates. No direct evidence of such complexes exist.

(2) 600-700 C: First visible evidence of oxygen precipitation,rodlike structure identified (small 20 A amorphous precipitates.

(3) 800-1000 C: Platelike structures with {100} habit planes (presumably amorphous) in size ranges of 100-5000 A.

(4) 1000 C: Platelike precipitate accompanied by punched out prismatic dislocation loops and extrinsic stacking faults with the associated colonies.
(5) 1200 C: Large polyhedral precipitates identified as being amorphous and large extrinsic stacking faults.

In our work a two step heat treatment was used; a 750 C for the nucleation step and 1050 C for precipitate growth. The nucleation and growth of precipitates have been studied extensively since 1976 [3-8]. However, the nucleation kinetics is not yet well understood due to the variety of starting silicon specimens. In contrast, the growth kinetics of bulk stacking faults formed by oxygen precipitation has been modeled. A brief description of nucleation and growth mechanisms will be presented.

2.1.2 OXYGEN PRECIPITATION

Oxygen interstitials are supersaturated during cooling of crystal growth. They tend to cluster and form large precipitates (a few 1000 A), but most of them form small embryos of about 10-40 A at sites of oxygen interstitials which is called **HOMOGENEOUS NUCLEATION** or at other sites (other impurities such as carbon) which is **HETEROGENEOUS NUCLEATION**. Formation of embryos requires a certain length of time, i.e., induction time (long at low temperature and short at high temperature). Therefore, during the cooling

process of the silicon ingot more embryos are formed at high temperature. The size and density of large and small precipitates depends on concentration of oxygen interstitials, number of heterogeneous nucleation sites, and the growth and cooling condition of the starting wafer.

2.1.3 NUCLEATION MODEL

Homogenous nucleation can take place in silicon if there is a large driving force, i.e., a departure from equilibrium, such as supersaturation of solute atoms in the crystal. The embryos formed in homogeneous nucleation must become large enough to exceed a certain critical radius in order for precipitates to grow. This is based on the theory developed by Volmer et al [8] to explain the combination of surface energy and volume energy necessary for an object to grow. As a particle grows due to precipitation, a new surface is created; hence energy must be added, and thus the surface free energy is always positive. The volume free energy is negative, because as a precipitate grows it removes oxygen atoms from the silicon crystal and the overall material system becomes closer to equilibrium. Thus the two opposing free energies are added together and the free surface energy is initially larger than the free volume energy. As the radius of the particle grows in size, the sum of the free energies goes through a maximum at a radius r_o (called the critical radius). The condition of maximum free energy

corresponds to the state of minimum stability of the precipitate particle. Therefore, a particle with radius less than r_o can lower its free energy by decreasing its size, and thus will tend to dissolve; a particle with radius larger than r_o can decrease its overall free energy by growing [9].

Wada [8] used the Volmer theory and developed a general equation for the nucleation rate J as,

$$J = ZNW^* \exp\left(\frac{-\Delta G}{KT}\right)\exp\left(-\frac{t_i}{t}\right) \qquad (1)$$

where Z is the Zeldovich non-equilibrium factor, W* is the frequency factor, N the atomic nucleation site density, ΔG is the free energy for formation of the critical nucleus, and t_i the induction time. Figure 1 shows the nucleation rate of oxygen precipitates as a function temperature. Wada et al [8] also proposed the overall nucleation process as

$$J_{total} = J_{homo} + J_{hetero} \qquad (2)$$

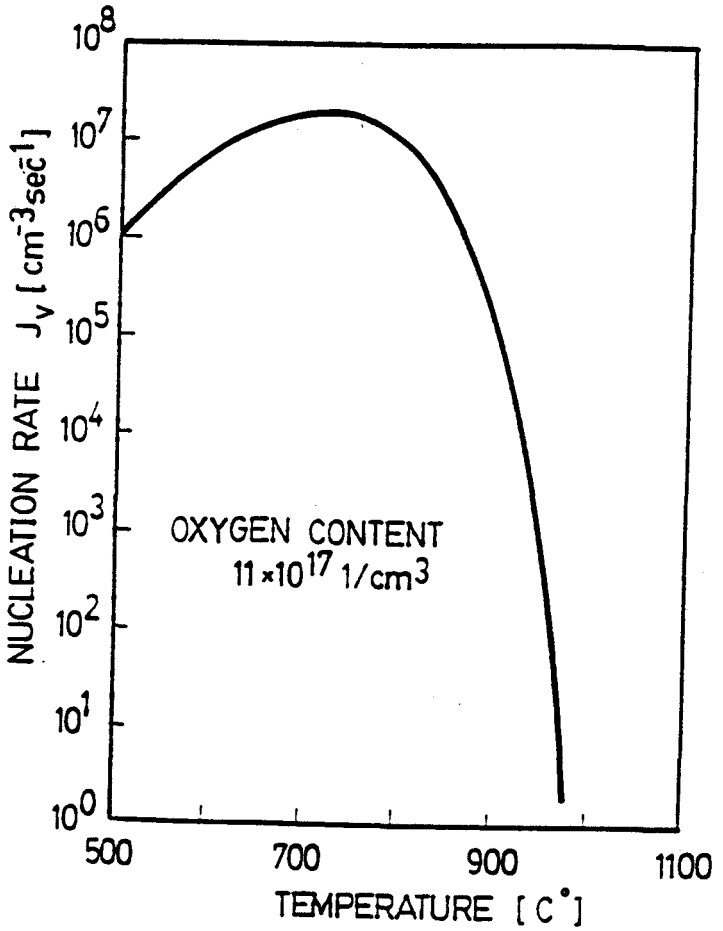


Figure 1) Nucleation rate of precipitates vs temperature after Wada et al [8].

2.1.4 GROWTH OF BULK STACKING FAULTS (BSF)

The formation of stacking faults involves the local accumulation of excess planes of atoms (extrinsic) or reduction planes of atoms (intrinsic). Stacking faults in silicon were initially found to be extrinsic in nature and were bounded by partial dislocation loops based on TEM studies [10]. Stacking faults can form in IC processes such as epitaxy growth , ion implantation, silicon oxidation and from oxygen micro-precipitate growth. The source of these extra atoms includes supersaturated self-interstitials and self-interstitials created during the growth of oxygen precipitates (This is referred to as the self-interstitial model). Recently, there have been some experimental evidence [11] that suggests both self-interstitials in supersaturation and vacancies in undersaturation coexist during oxidation. A model based on vacancies in undersaturation (referred to as the vacancy model) has been proposed for bulk stacking fault growth [12]. J. Patel [13] proposed a model for the formation of stacking faults in heat treated silicon containing oxygen (Fig. 2). During the nucleation of a precipitate (at 700 C), which is presumed to be SiO_2 a volume change associated with the growth of the precipitate occurs which is $V_{SiO_2} / V_{Si} = 2$; thus a dislocation is then generated around the precipitate. During subsequent heat treatments the particle grows by the diffusion of oxygen from the surrounding silicon matrix to its surface. The

large volume change associated with the growth of the precipitate is accommodated by the displacement of silicon atoms. These excess silicon atoms can either diffuse away and form a Frank loop or can cause the growth of bulk stacking faults.

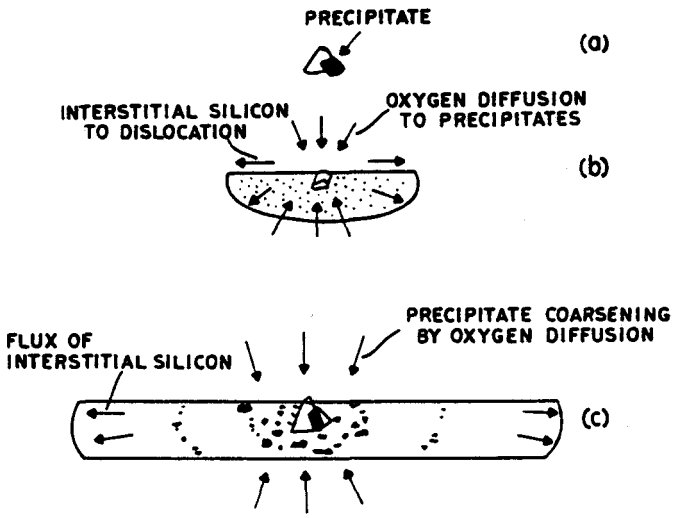


Figure 2) Schematic of the stages in the development of bulk staking faults after Patel [13]

Mahajan et al [4] propose a slightly different role for oxygen in their BSF growth model which is shown in Figure 3. It is assumed that the initial stage in the formation of a stacking fault is the formation of silicon-oxygen clusters on [111] planes. When the oxygen atoms occupy position between pairs of silicon atoms along <111> directions, a compression of the adjoining silicon matrix along <111> will

result. For the growth of the Si-O clusters silicon interstitials must be emitted into the silicon matrix. When these silicon interstitials reach a certain critical level, they can condense into Frank loops. Further growth of BSF occurs by repeating the Si-O formation process.

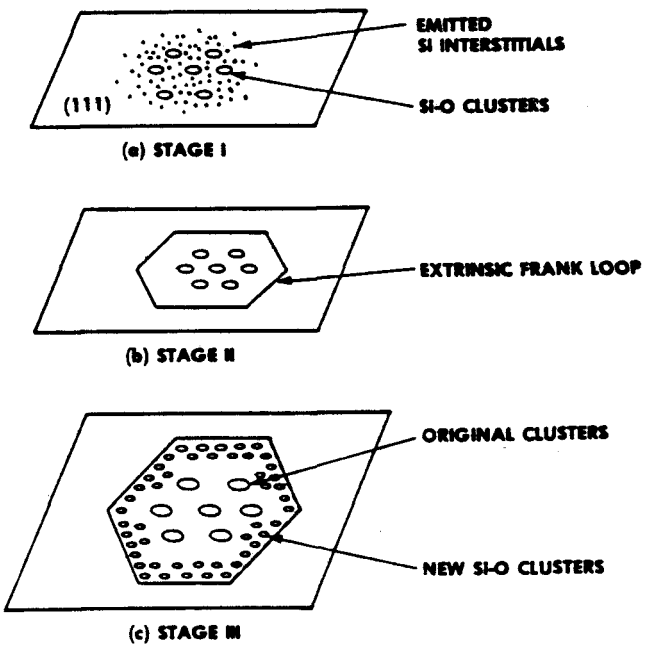
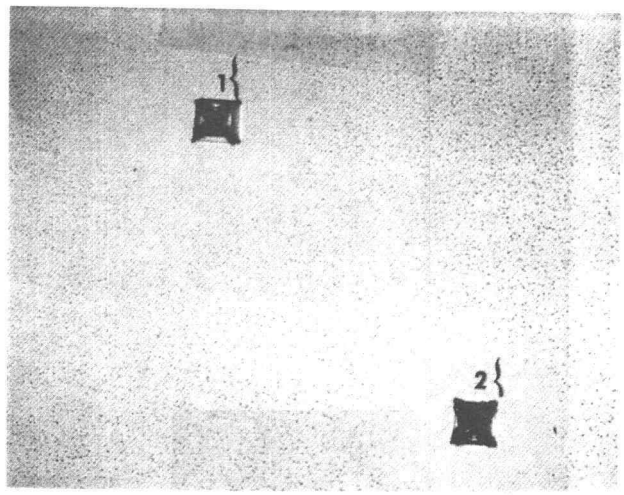


Figure 3) Schematic of the formation of an extrinsic stacking fault after Mahajan et al [4].

2.2 CARBON IN SILICON

Carbon is introduced into silicon as early as the polysilicon manufacturing during which the initial step is the reduction of silicon by reaction of quartz with carbon [14]. Carbon also can be introduced into silicon during the Czochralski process from the crystal growth chamber [15]. The concentration range of the carbon atoms can be from below measurement detection limits (for FTIR this is $10^{15}/cm^3$) to $2.5x10^{17}/cm^3$. The role of carbon on oxygen precipitation and its electrical activity in silicon has not been well understood. Seigo Kishino [5] argues that in the heterogeneous nucleation model the carbon atoms are the nucleation sites. However, Kung et al [16] did not find any correlation between a reduction in the carbon concentration and oxygen precipitation. Hahn et al [17] recently have shown that oxide precipitates (OP's) increase with increasing substitutional carbon concentration. They also found in samples with high carbon concentration the stress at Si/SiO_2 is lower through formation of SiC. The most interesting observation has been made by Bailey et al [18] who found that carbon can be gettered to damage sites such as dislocations, stacking faults and wafer surfaces. Figure 4 shows typical stacking faults with large dislocations and precipitates which are observed at the corners of the stacking

faults. Scanning Auger data also showed that the precipitates have a high concentration of carbon instead of the expected heavy metals.



Stacking Fault 1	Sputter Time (Min.)	Atomic Relative Percent C	O	Si
Corner-1	1.0	30.7	4.0	65.1
	5.0	13.9	1.5	84.4
Corner-2	1.0	24.9	4.1	70.8
	5.0	25.7	2.2	72.0
Corner-3	1.0	31.3	6.4	62.2
	5.0	43.0	2.7	54.1
Corner-4	1.0	37.4	9.0	53.5
	5.0	38.8	1.7	59.3
Clear Area Next To Fault	1.0	2.2	2.1	95.6
	5.0	0.0	1.9	98.0

Figure 4) Scanning Auger data showing a high concentration of carbon at stacking fault number 1 corners and no carbon in the clear area next to the faults after Bailey [18].

2.3 ELECTRICAL ACTIVITY OF MICRODEFECTS IN SILICON

The problem of electrical activity of silicon defects in general and oxygen induced microprecipitates and stacking faults in particular has been a complex and often confusing issue. No one better than Sokrates T. Pantelides has explained this problem in his recently edited published book [19], He wrote " With advent of the junction techniques in 1970's (deep level transient spectroscopy) quit often the results of different experiments or different researchers were in disagreement,but the origins of the discrepancies were not usually investigated. Typically, measured cross sections would be fit to a simple model to locate the energy levels in silicon bandgap. This type of work led to a proliferation of ***energy levels*** quoted in the literature for a given impurity. There was little effort spent on verifying whether the energy level thus reported indeed correspond to simple impurities or complexes. This confusion led to the often-mention quote: *the deeper the level, the shallower the understanding.*"

In this work, an energy level for stacking faults has been determined. However, the sole purpose is not the energy level, but rather a comparative study between samples with different concentrations of oxygen and carbon impurities. In the next sections, a review of current data about the

electrical activity of dislocations, silicon after deformation, oxygen induced precipitation, and stacking faults will be presented.

2.3.1 ELECTRICAL ACTIVITY OF DISLOCATIONS

A literature search for electrical activity of dislocations in silicon revealed the proliferation of energy levels reported for this defect. Dislocations have been extensively studied for their effect on transport properties such as mobility, lifetime, conductivity and their energy levels in silicon crystals. Glazer et al [20] found an acceptor level below conduction band (E_t-E_c= .52eV) for dislocations in silicon using lifetime measurements. Petal et al [21] found E_t-E_v= 1.2 +/- .2 eV using dislocation velocity measurement in 1968. Erofeev [22] found E_t=.58 eV with Patel's measurement method [21]. Jones [23] based on theoretical methods found E_t=.8 eV. Grazhuis [24] reported a E_t=.43 eV +/- .03 eV using the Hall Effect. Patel [25] again in 1977 reported a E_t=.63 eV using DLTS. Finally Weber et al [26] found a level at .68 eV with the electron paramagnetic resonance (EPR) measurement method. There were other reported energy levels for dislocations in silicon which vary from one laboratory to another. A schematic of the defect energy levels due to dislocations by a variety of different techniques is shown in Figure 5.

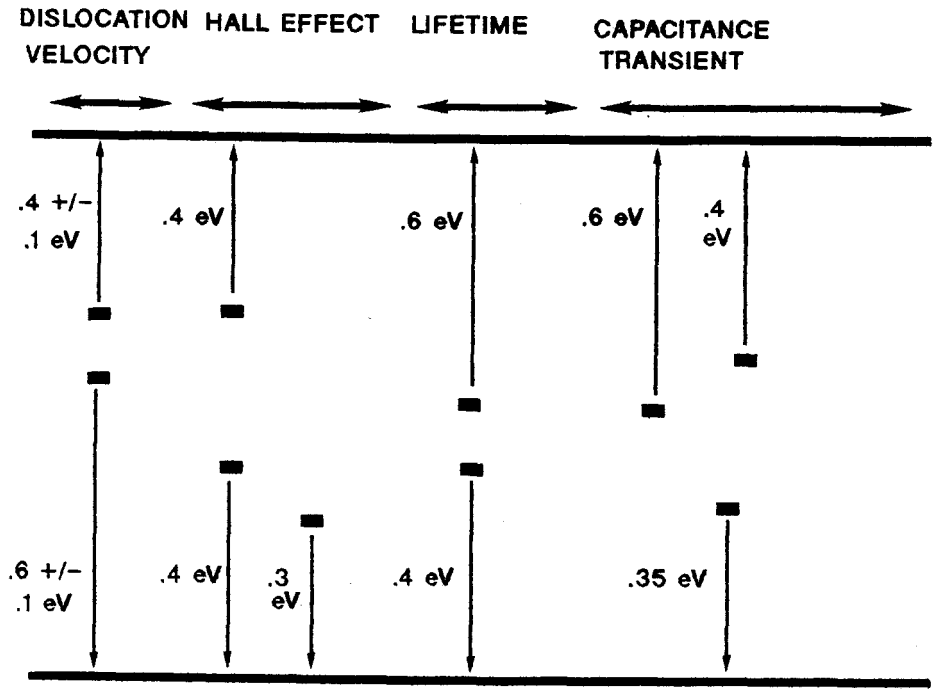


Figure 5) Schematic comparison of dislocation levels in silicon by a variety of experimental techniques Kimerling [2]

2.3.2 ELECTRICAL ACTIVITY OF DEFECTS IN SILICON AFTER DEFORMATION

Deep level defects are generated after silicon samples are plastically deformed. In deformed samples the dislocation density can reach 10^7-10^9 per cm^2. P. Omling et al [27] used deep level transient spectroscopy (DLTS) and electron-paramagnetic resonance (EPR) to investigate induced

deep level defects after plastically deforming n-type silicon samples at 650 C. Figure 6 shows the DLTS spectra for four traps,labeled A, B, C, and D. With different deformations the B and D traps are clearly resolved, however both A and C are more complicated and not easily resolved. Our results (chapter IV) also show a dominant level very similar to level D for samples with oxygen induced stacking faults and low carbon concentrations. Omling's EPR results show DLTS line D is dominant in strongly deformed silicon and shows characteristics which are comparable to Si-K1/K2. Photo-EPR shows a midgap level of this center (D level) and from a comparison of the DLTS lines with EPR centers, Omling suggested the D line is related to " dangling bond" centers.

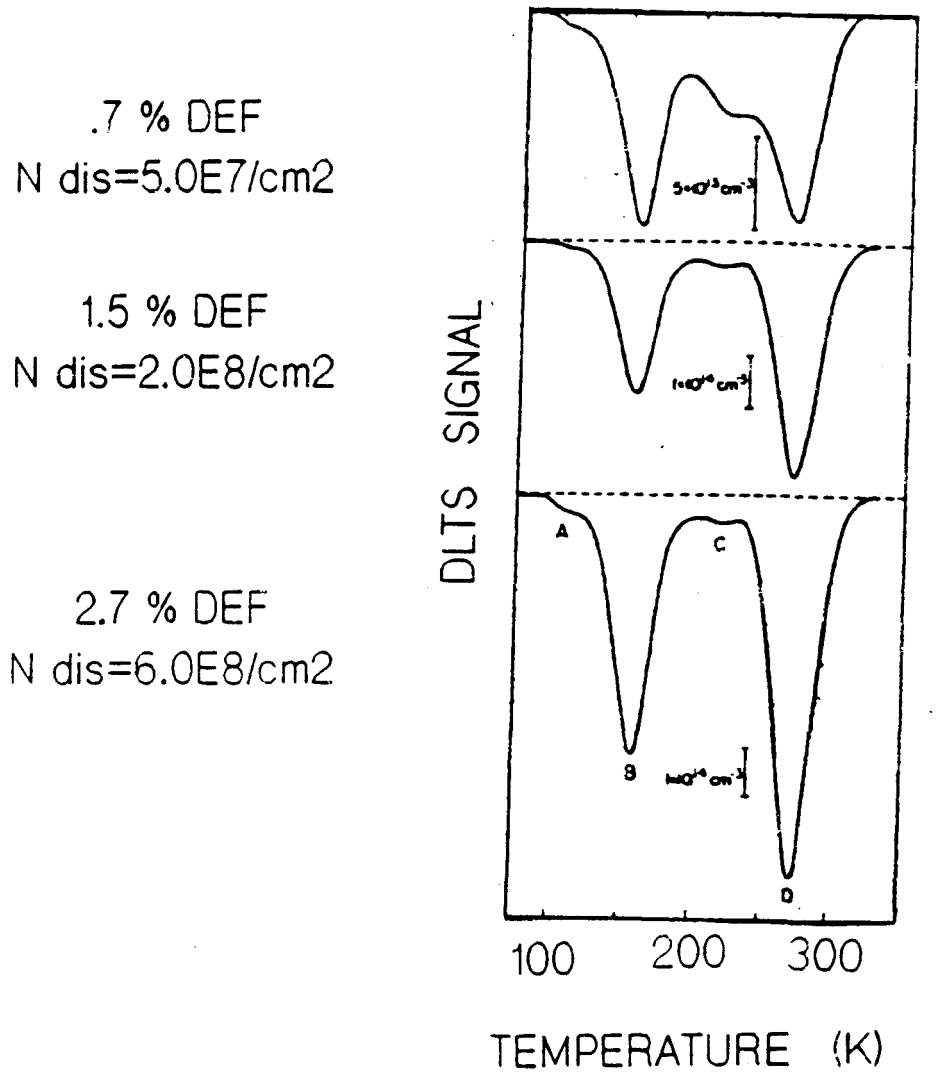


Figure 6) DLTS spectra for different deformations in n-type silicon after Omling [27]

2.3.3 ELECTRICAL ACTIVITY OF OXYGEN PRECIPITATES (OP'S)

J.M. Hwang and D.K. Schroder [28] proposed a model for the electrical activity of oxygen precipitates (OP) based on a Si and SiO_2 interface model. They observed that lifetime degradation is mainly due to OP's and that recombination at

OP's takes place through the Si/OP interface. They also observed that lifetime degradation is more severe in p-type silicon than n-type for similar densities and sizes of OP's. A model was presented based on a band bending around OP's which is caused by positive fixed charges similar to the Si/SiO_2 interface. Figure 7 illustrates that in p-type silicon samples a depletion region is formed around OP's providing a large collection volume for minority carriers,i.e. electrons. In n-type the positive charge causes an accumulation layer which could act as reflecting barrier to minority carriers or holes. M. Miyagi et al [29] also showed the effect of OP's on minority carrier lifetimes. They found that homogenous OP's decreased the lifetime when their length is greater than 100 A. Miyagi indicated that the heterogeneous nucleated OP's are about 1000 A in size and normally cause the lifetime degradation. Figure 8 illustrates the lifetime as function of OP density and annealing time.

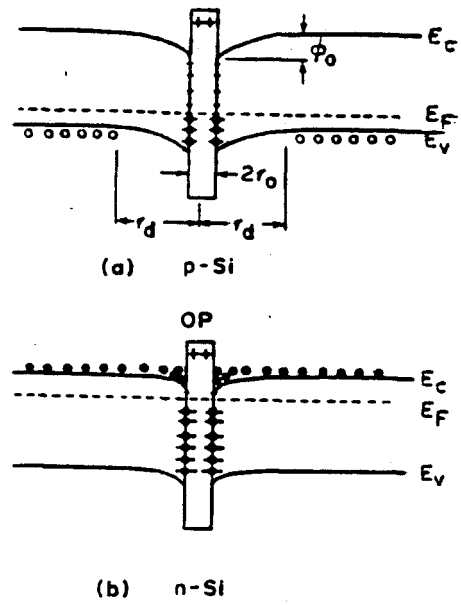


Figure 7) Schematic band diagrams with band bending due to positive fixed charges in OP's after Hwang and Schroder [28]

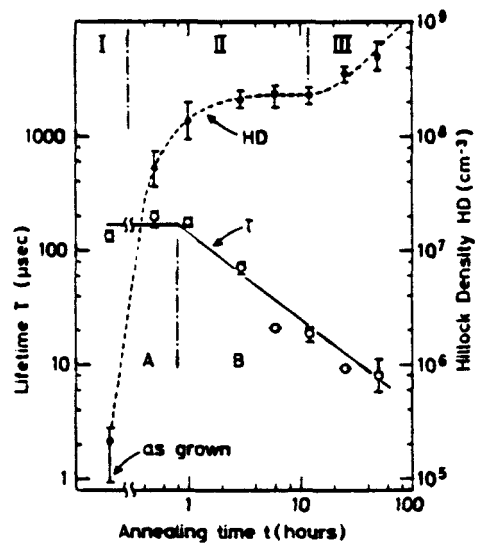


Figure 8) Lifetime and OP density as a function of annealing at 850 C after Miyagi [29]

2.3.4 ELECTRICAL ACTIVITY OF STACKING FAULTS (SF)

The perfect silicon lattice can be described as a sequence of planes such as AA'BB'CC'AA'BB'CC'.....(stacked in {111} directions).

In the case of intrinsic stacking faults a pair of planes, say BB' is missing then the lattice sequence becomes AA'|CC'AA'BB'CC'..... For extrinsic stacking faults an extra plane,say BB'is inserted between CC' and AA' such as AA'BB'CC'BB'AA'BB'CC'.....

Weigal et al [30] concluded that there is a only a minor charge distribution around a stacking fault. L.C. Kimerling et al [31] reported an energy level of Ec-Et=.1 ev for undecorated extrinsic faults using charge collection scanning electron microscopy. Ogden et al [32] compared data in the literature for leakage current per stacking fault. The calculations were from electrical measurements and stacking faults counts after preferential etching. Ogden found values ranging from 4 pA to 500 uA per stacking fault which is an eight order of magnitudes variation from one report to another one. A major part of this wide range of leakage current has been attributed to decorated stacking faults with impurities (primarily transition metals such as Ni,Co.,Pd,Cu,and Fe). Seidel et al [33] found that a clean stacking fault (no decoration) can contribute only in order of 0.1 to 10 pA to the reverse current of a diode. The discrepancies in the electrical activities of stacking

faults which are similar to those of dislocations could be due to different types of stacking faults, i.e., ion implantation stacking faults, oxidation induced stacking faults or oxygen precipitation induced stacking faults. Some of the differences also might be due to processing conditions and wafer thermal history.

2.4 N-CHANNEL HOT CARRIER RELIABILITY

MOSFET devices are being continuously scaled down in size while the power supply remains fixed at 5.0 volts (however for devices of gate length below half a micron it has to be reduced to 3.3 or less with current material limitations); as a result the maximum electric field in the channel increases. If the electric field in the channel becomes too large, hot carriers can be generated which could cause device degradation and reliability problems [34-35]. Figure 9 illustrates the three main hot carrier effects: hot carrier generation, injection and trapping.

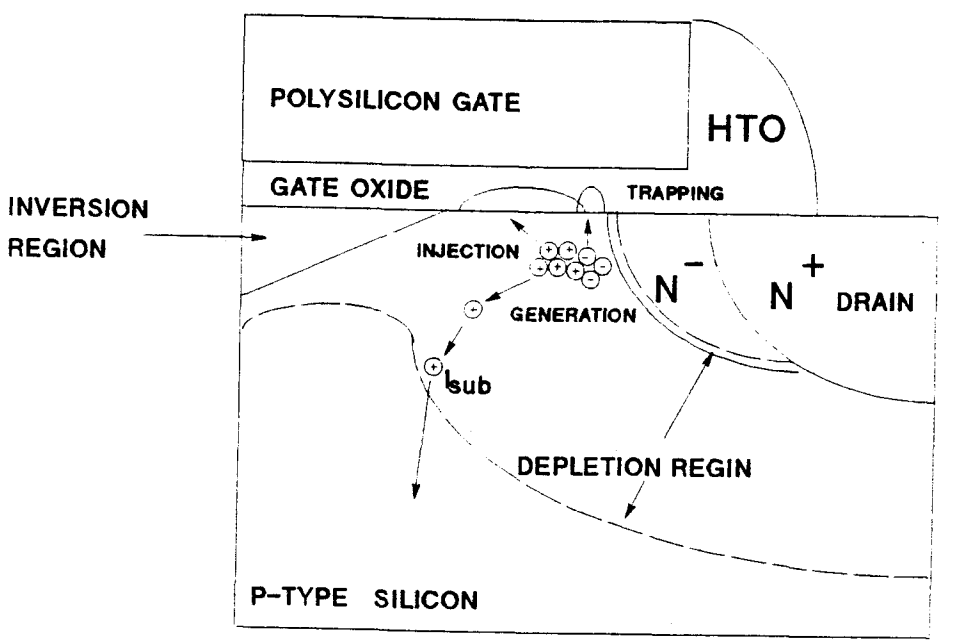


Figure 9) Hot carrier effects in n-channel devices

Since our work is focused on the material aspects of hot carrier effects, it is the trapping and detrapping of electrons and holes that will make up the major part of this section. However, hot carrier generation and injection will be discussed briefly.

2.4.1 Hot CARRIER GENERATION

In MOS transistor's the gate and substrate currents are referred to anomalous currents which are measured at backside and at gate contacts. These current are largest in short channel devices where the channel lengths, doping concentrations and junction depths have all been scaled. One parameter which is not usually scaled is the drain voltage which causes a high field of about 10^5 to 10^6 V/cm near the drain. This high field which is parallel to the channel, is the result of the scaling the channel lengths and doping concentration without scaling the drain voltage. Carriers which pass through this high electric field region are accelerated to the point of impact ionization which can result in formation of electron-hole pairs. These electron-hole pairs in turn can be accelerated by the electric field and if this multiplication continues without bound, then avalanche breakdown results.

IMPACT IONIZATION

Impact ionization imposes an upper limit on the reverse bias junction breakdown voltage. Zener [36] explained the high field breakdown mechanism, i.e. above 10^6 V/cm. McKay et al [37] have provided an explanation for electrical breakdown at lower fields by showing that carriers injected into depletion regions can create more carriers by impact ionization. If α is the ionization rate per unit length can be written as

$$\frac{dn_1}{dx} = (n_0 + n_1)\alpha = n_\alpha \alpha \tag{3}$$

where n_0 is the number of injected electron , n_1 is the number of electron produced between 0 and x by impact ionization . This expression can be integrated from x=0 where $n_1 - n_0$ to x =d where $n_1 - n_0 - n_0 M$. M is called the multipilication factor and for carriers created by impact ionization an expression is given as

$$\int_0^d (\alpha)\, dx = \int_{n_0}^{n_0 M} \left(\frac{dn_1}{n_\alpha}\right) = \ln M = 1 - \frac{1}{M} \tag{4}$$

The quantity 1- 1/M is the number of carriers created by impact ionization divided by the total number of carriers. For avalanche breakdown this ratio is equal one. The problem with the above impact ionization treatment is that it assumes the ionization rate for holes is the same as electron. For silicon the impact ionization for holes is an order of magnitude less than the rate for electrons. Experimentally,

the ionization rates for both electrons and holes vary with E-field as

$$\alpha = C\exp(-b/E) \quad (5)$$

where C and b are constant and E is the electric field.

2.4.2 HOT CARRIER INJECTION

The second major mechanism of device degradation is the injection of hot carriers into the interface or dielectric SiO_2. Ning et al [38] have studied the emission of hot carriers and mainly hot electrons from silicon into SiO2, where they had to make many simplifying assumptions, for example an energy independent mean free path and a parabolic band structure. At energies of 3.0 eV (hot carrier energy) the band structure is highly nonparabolic. Karl Hess [39] has taken a more realistic band structure and with a Monte Carlo simulation has shown a barrier lowering effect for hot electron emission. Note that both Ning and Hess have used the "lucky electron model" for their hot electron emission process. Shockley developed this model for explanation of avalanche multiplication in p-n junctions [40].

LUCKY ELECTRON MODEL

The model used for p-n junctions contained three adjustable parameters; threshold energy for pair production by impact ionization E_r, mean free path for electron-phonon

scattering L_P and the ratio $r = L_I/L_P$ where L_I is the mean free path for scattering due to impact ionization for carriers with energy greater than E_I. The ratio r is the number of phonons emitted between each ionizing collision. The probability of a carrier travelling a distance $L_P(E-E_I)/E_P$ without an ionizing collision is

$$P_a = A\exp\frac{-L_p(E-E_I)}{L_I E_P} \tag{6}$$

where A is a normalization constant. Therefore for a carrier with energy greater than E_I the probability of an ionizing collision is

$$P_b = 1 - P_a \tag{7}$$

This model can be used to account for the exp(-b/E) dependence of the ionization rate described previously.

Ning used the original lucky electron model to describe carrier injection at the $Si-SiO_2$ interface. At the $Si-SiO_2$ interface the critical energy is the barrier potential 3.1 eV for electrons and 3.7 eV for holes. Figure 10 illustrates the concept of the lucky electron as proposed by Ning. Electrons located a distance d away form the interface and having a potential energy equal to the barrier will overcome the barrier and go into silicon dioxide if they encounter no scattering events.

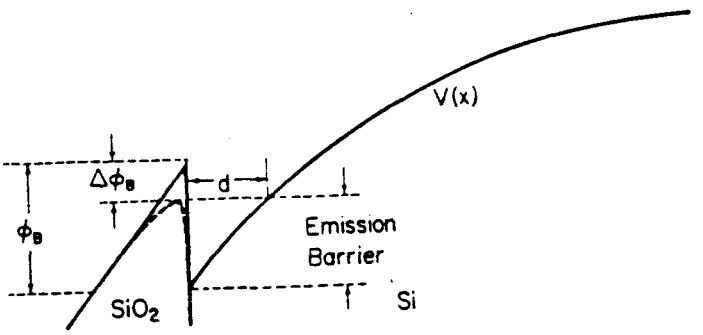


Figure 10) Band diagram for lucky electron model with barrier lowering after Ning [38]

Equation (6) can be written as

$$P = A\exp\left(-\frac{d}{\lambda}\right) \tag{8}$$

where λ is mean free path and A is the normalization constant. The barrier lowering according to Ning is due to the Schottky effect and tunneling which is approximated in the following form

$$\phi_B = 3.1eV - bE_{ox}^{1/2} - aE_{ox}^{2/3} \tag{9}$$

where 3.1 eV is the $Si-SiO_2$ interface barrier, E_{ox} is the oxide field, aE_{ox} comes from the Schottky lowering and bE_{ox} accounts for tunneling.

2.4.3 HOT CARRIER TRAPPING

The third part of the hot carrier degradation is the trapping which is the major focus of the device part of this

work. Most of original works have extensively been concentrated on hot electron trapping in the silicon dioxide. But recent experimental results suggest that hole trapping precedes electron trapping and can be the main degradation mechanism. Our work examines device aging (trapping) and subsequent temperature annealing (detrapping) with device DC measurements. From trapping and detrapping, it is possible to calculated the trap energy levels. Electrons and holes when injected into the interface or SiO_2 can be captured by sites which are called traps. Electrons can move rapidly with a mobility of 20-40 $cm^2/v\text{-}sec$ in SiO_2 and move toward the positively biased gate contact [41]. Holes are also mobile enough to drift significant distance in SiO_2, with a mobility determined from transit time measurements that is in the range $<2x10^{-5}$ $cm^2/v\text{-}sec$ [42-43]. Several models have been proposed as an explanation for device aging. However, the model proposed by R. Fair et al [44] to the author's belief is the one that could best explain most of the processes that are occurring at the $Si\text{-}SiO_2$. Fair's model proposes that the instability is caused by the trapping of hot-holes emitted into the $Si\text{-}SiO_2$ interface or gate oxide.

FAIR AND SUN MODEL

Fair used the Svensson's trivalent silicon model [45] to explain the the hot hole trapping process. Figure 11 illustrates the three forms of trivalent silicon, i.e., are

surface silicon Si_s, bonded to three other silicon, Si_o bonded to three oxygen and oxide trivalent silicon Si_{os} close to the surface.

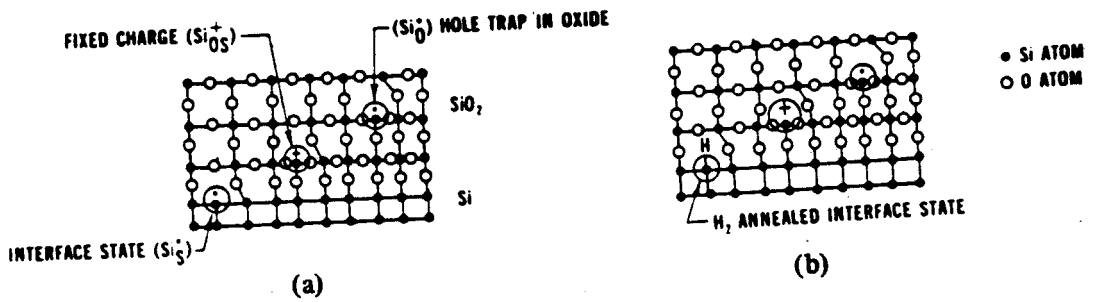


Fig.11 (a) The $Si-SiO_2$ interface defects after Svensson [12]. (b) H_2 anneal after Fair [44]

Sevensson postulated that Si_s is a surface trap or interface state,Si_o is a deep hole trap,and Si_{ox} is a deep hole trap which is easily ionized and is assumed to be the fixed surface charge Q_{ss}. Figure 12 shows the five step process of device degradation.

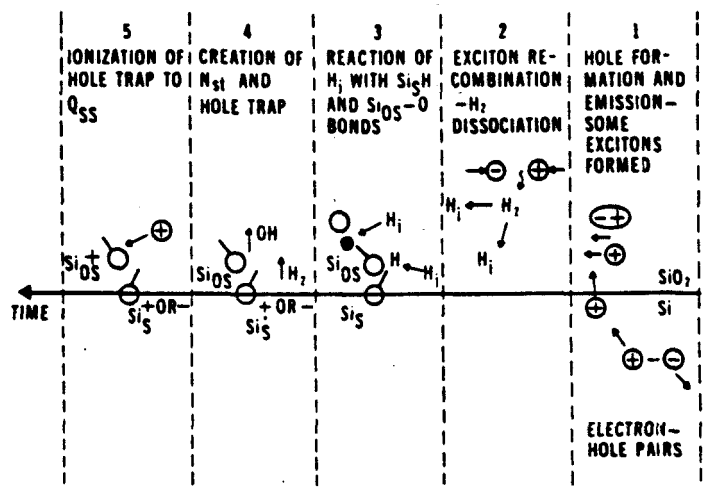


Figure 12) Model of interface and fixed charge formation after Fair [44]

The Fair model starts with hole formation in Si due to impact ionization and then proposes that the electric field normal to the Si-SiO_2 interface E_{normal} being maximum at the drain would make the hole injection likely close to drain. In most CMOS processes the final step is a H_2 or N_2 anneal at 400 C for radiation damage and interface trap density reduction through the reaction of H_i(interstitial hydrogen) and Si_s to form Si_sH. The production of interstitial hydrogen could be either from Si-H or H-H bond breakage. The source of breakage energy could come from the recombination of holes and electrons at hydrogen-related centers in the SiO_2. Energy release from recombination events is through

phonon-generation processes [46]. The following reaction shows the H-H dissociation

$h^+ + e^- + H_2 \text{ ---> } 2H_i$

In the presence of H_i, interface states Si_s can be created

$Si_sH + H_i \text{ ---> } Si_s + H_2$

Interstitial hydrogen can also create a hole trap Si_{os}

$Si_{os}\text{-O-}Si_o + H_i \text{ ---> } Si_{os} + Si_oOH$

The final reaction is the ionization of Si_{os} with another hole

$Si_{os} + h^+ \text{ ---> } Si_{os}$

The morphology and chemical structure of Si-SiO_2 interface defects have been under extensive investigation [47-49] because of their effects on MOSFET devices, we will present a more detailed picture of Si-SiO2 interface in chapter 7 of this work.

3. EXPERIMENTAL TECHNIQUES

In the semiconductor materials a variety of different techniques are used to investigate the defects in the forbidden gap. For example the carrier population can be changed thermally,optically and electrically and the resulting effects can be used in variety of ways to characterize material and device defects. Beginning at 1970 a new technique based on semiconductor junctions was developed by Sah et al [50]. In the junction technique the position of the Fermi level relative to the band edges is altered by an applied bias. For example in the reverse biased junction, the junction is depleted of mobile carrier. This condition can be treated using linearized rate equations. Any perturbation to the junction will decay exponentially with time and can be monitored with either capacitance or current and is a function of the charge-state of the defects in the junction. One of the most widely used versions of the junction method is deep level transient spectroscopy (DLTS) introduced by Lang [51] in 1974.

In this chapter, the measurement systems used for characterization of oxygen induced microdefects and hot carriers degradation are described. The first section is devoted to deep level transient spectroscopy and a brief description of both capacitance and current DLTS will be presented. In the

following sections photocapacitance measurement, fast fourier infrared spectrophtometry (FTIR), and MOSFET device measurement and aging systems will be presented.

3.1 DEEP LEVEL TRANSIENT SPECTROSCOPY (DLTS)

Deep level transient spectroscopy is an efficient method of evaluating deep level impurities in semiconductors. A Schottky diode or a p-n diode can be used as a junction. DLTS provides a rapid spectroscopic analysis method, a measurement taking less than an hour can give at least some information about all the deep levels in a sample. During a measurement an average is formed over a large number of transients and this can reduce the noise. The weak points of DLTS are its inability to determine accurately the temperature of DLTS peaks [52], and the energy level of nonexponential transients [53-54]. Figure 13 shows a DLTS system. It consists of a sensitive capacitance meter (Boonton 72B with a response time of ~1 ms), a pulse generator, and a dual-gated signal integrator which takes the difference between time t_1 and time t_2 and then averages this by means of a boxcar averager. An X-Y recorder or an HP9845B computer is used for plotting the boxcar averaged output versus temperature. The temperature was varied between 100K and 420K. Most of measurements were done in 200K to 350K range.

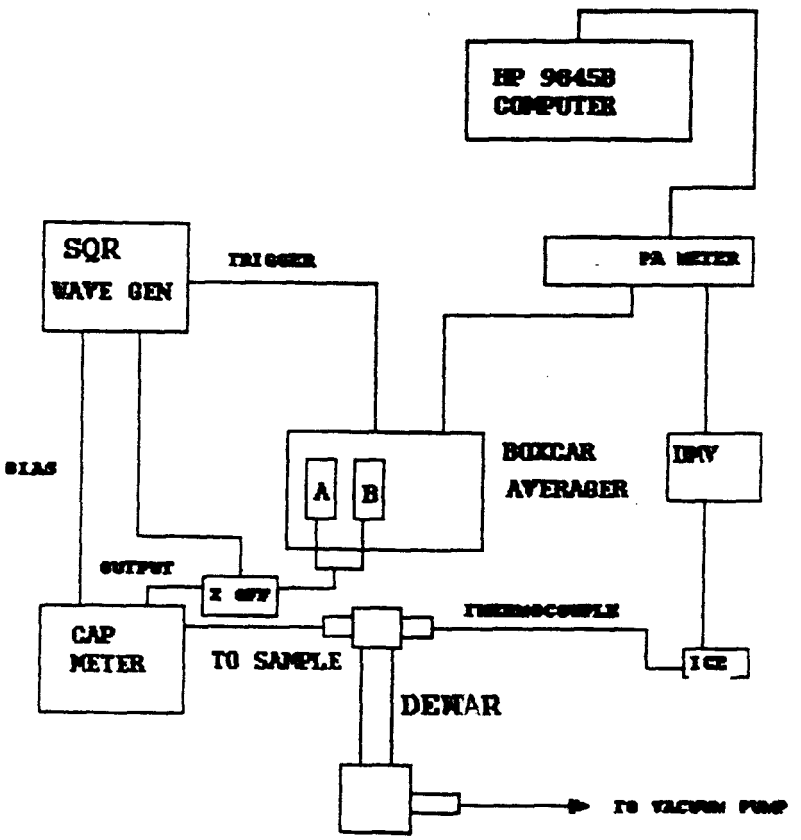


Figure 13) The OSU capacitance DLTS system diagram with detectability limit of 1.0E11 / cm^3

3.1.1 TRANSIENT ANALYSIS

When a defect is present in a semiconductor it normally gives rise to an energy level in the band gap. If the energy level is close to edge of the valence band or the conduction band (*SHALLOW* level), it can be ionized and determines the conductivity of the semiconductor. Levels positioned more centrally are *DEEP* levels. These levels could be due to crystal lattice defects or impurity atoms. Deep levels can act as a trap centers causing either electron or hole to bound to them. The emission of charge from the trap will occur only after a finite length of time t_c, the time constant of a trap. Emission rate of electrons e_n is a function of temperature of the material, and activation energy ΔE. Here the analysis is for electrons, there is an analogous emission and capture of holes. The emission rate can be expressed as

$$e_n = \frac{\sigma_n \langle v_n \rangle N_c}{g} \exp\left(\frac{-\Delta E}{KT}\right) \qquad (10)$$

where σ_n is electron capture cross section, v_n is thermal velocity of electron, and N_c is the effective density of states at the conduction band. The activation energy in equation (10) is a free energy, however the thermodynamic quantity derived from the temperature dependence of the emission rate is an enthalpy [52]. The enthalpy and the free energy are equal only at T=0. Therefore, the activation energy obtained from an Arrhenius plot is the free

energy obtained by a linear extrapolation to T=0 of the temperature dependent free energy at the measurement temperature. However, this is not always the same as the free energy at the measurement temperature. The inverse process of emission is capture and associated capture rate C_n. An expression for the time rate of change of electrons at a trap can be written using emission and capture rates

$$\frac{dn}{dt} = e_n n_T - C_n n p_T \qquad (11)$$

The rate of change for holes is

$$\frac{dp}{dt} = e_p p_T - C_p p n_T \qquad (12)$$

where n_T and P_T are the trap concentrations of electrons and holes respectively, and their sum equals N_T. n an p are untrapped electron and hole concentrations respectively. The rate equation for trapped electrons is,

$$\frac{dn_T}{dt} = (C_n n + e_p)(N_T - n_T) - (C_p p + e_n) n_T \qquad (13)$$

For an electron trap where we have only emission (C_n, e_p, $C_p \sim 0$) equation (13) can be written as

$$\frac{dn_T}{dt} = -e_n n_T \qquad (14)$$

where the solution to this differential equation (14) is

$$n_T(t) = n_T(0) e^{\frac{-t}{t_c}} \qquad (15)$$

3.1.2 CAPACITANCE DLTS

For an asymmetric p-n junction the space charge region (scr) is essentially on the side with lowest doping and for a Schottky diode is all in semiconductor. Figure 14 shows a Schottky diode with stacking faults and micorprecipitates.

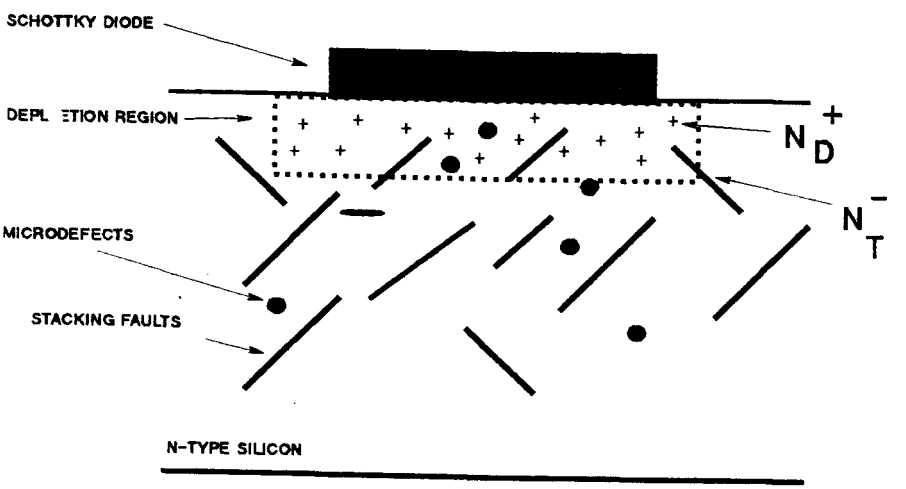


Figure 14) N-type silicon with Schottky diode

The capacitance for a plate capacitor is

$$C = \frac{\epsilon\epsilon_0 A}{W} \tag{16}$$

where $\epsilon\epsilon_0$ is the dielectric constant, A is the area of the capacitor, and W is space charge width. The capacitance expression for the diode Figure 14 is

$$C = \sqrt{\frac{q\epsilon\epsilon_0(N_D - n_T)}{2(V + V_{bi})}} \sim = C_0\left(1 - \frac{n_T}{2N_D}\right) \tag{17}$$

From equation 15 and 17 an expression for the capacitance transient is given by:

$$C = C_0\left(1 - \frac{n_T}{2N_D}\right) = C_0\left(1 - \frac{n_T(0)e^{\frac{-t}{t_c}}}{2N_D}\right) \qquad (18)$$

From Equation 18 the following equation follows at t=0.

$$\Delta C = \frac{N_T}{2N_D}C_0 \qquad (19)$$

3.1.3 TIME FILTERING TECHNIQUE OF DLTS

One way of determining the time constant of an exponential transient is to record the full transient and to plot logΔC versus time and calculate the slope of a line which results (this method will be used in the next section for the photocapacitance technique). This technique is very time consuming and since it uses only one transient, it does not have the noise reduction capability. DLTS uses a sampling technique to determine the time constant of an exponential transient. One sample is taken after a time t_1 and another after a time t_2, their difference can be plotted versus temperature. Figure 15 after Lang [52] shows that at low and high temperature the difference between t_1 and t_2 essentially goes to zero. The difference S(T) is given by:

$$S(T) = \Delta C(t_1) - \Delta C(t_2) = \Delta C(0)\left(\exp\left(\frac{-t_1}{t_c}\right) - \exp\left(\frac{t_2}{t_c}\right)\right) \qquad (20)$$

S(T) has a maximum for certain time constant t_{max}. the relation between the time constant t_{max} and t_1 and t_2 is determined by differentiating S(T) with respect to t_c and setting the result equal to zero which results in the following expression

$$t_{max} = \frac{(t_2 - t_1)}{\ln\left(\frac{t_2}{t_1}\right)} \qquad (21)$$

A peak will occur when t1 and t2 satisfy equation (20), at some particular temperature. The peak height is independent of the absolute value of t_1 and t_2, only the ratio between them is important. For all measurements in chapter Four we selected $t_2/t_1=4$ which is a reasonable choice for high sensitivity and a range of different time windows. The capacitance transient is always positive for a minority carrier trap and negative for majority carrier trap [52].

Figure 16a shows the capacitance transient caused by thermal emission from a majority carrier trap in a p^+n diode. At $t<0$, the junction is under reverse bias to establish space charge conditions in which states in the space charge region (scr) are empty because no mobile carriers are available for capture. At $t=0$, a biased pulse toward zero momentarily collapses the scr and making the majority carriers available for capture, the depletion region goes to zero and capacitance is large. At $t=0^+$, the pulse is turned off and reverse bias restablished the junction capacitance is reduced because the compensating majority carrier charge has been trapped in the space charge region. At $t>0$ the capaci-

tance goes back to its quiescent values due to thermal emission of trapped electrons. Figure 16b is an analogous process for thermal emission from a minority carrier trap.

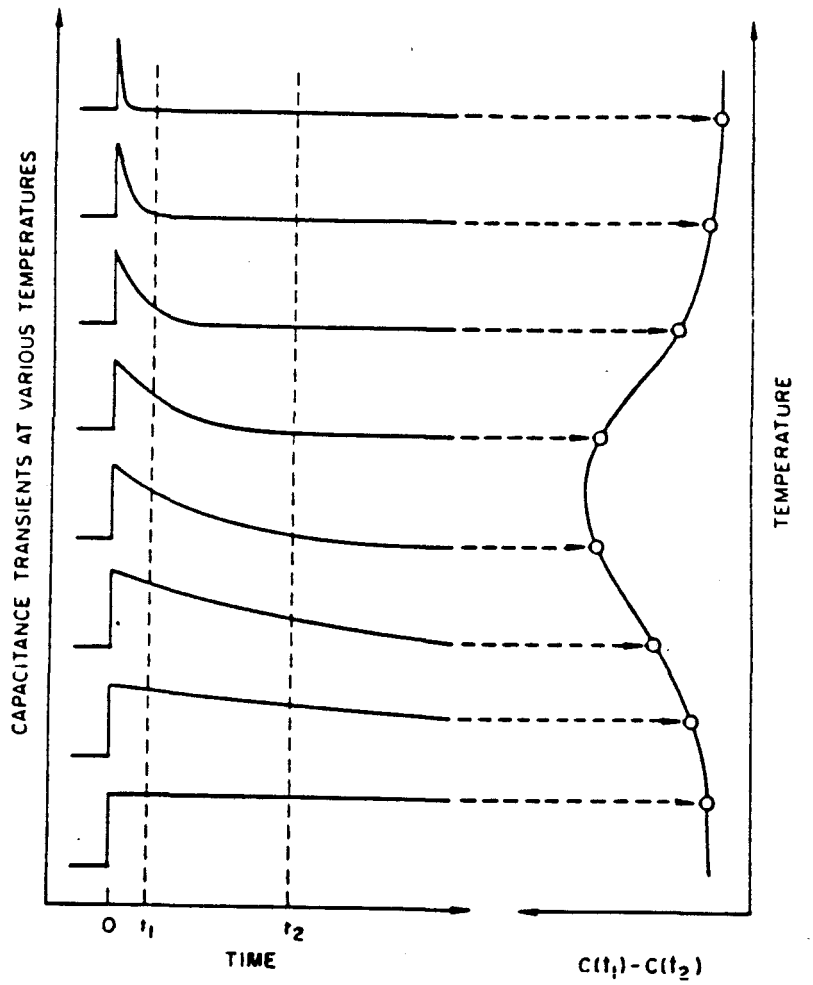


Figure 15) Implementation of time filtering by means of a double-boxcar. The output correspond to average difference at sampling time t_1 and t_2 after [52]

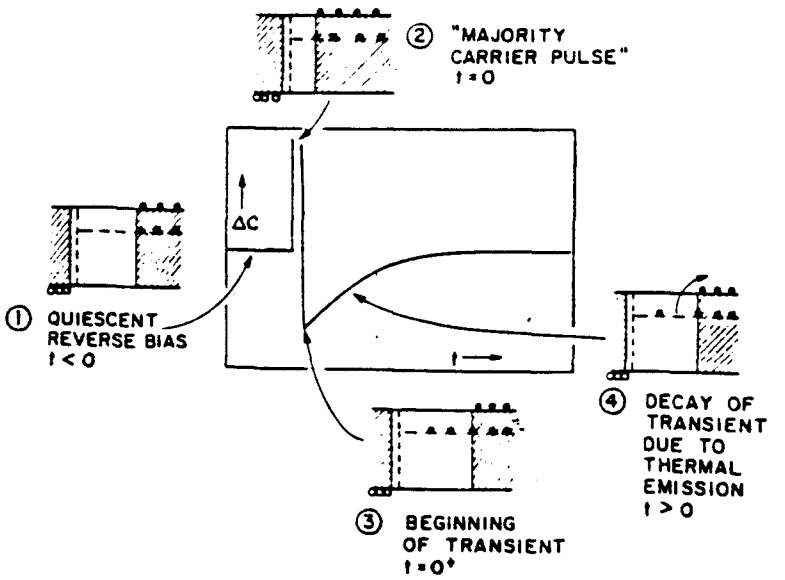


Figure 16a) The capacitance transient caused by thermal emission from a majority carrier trap.

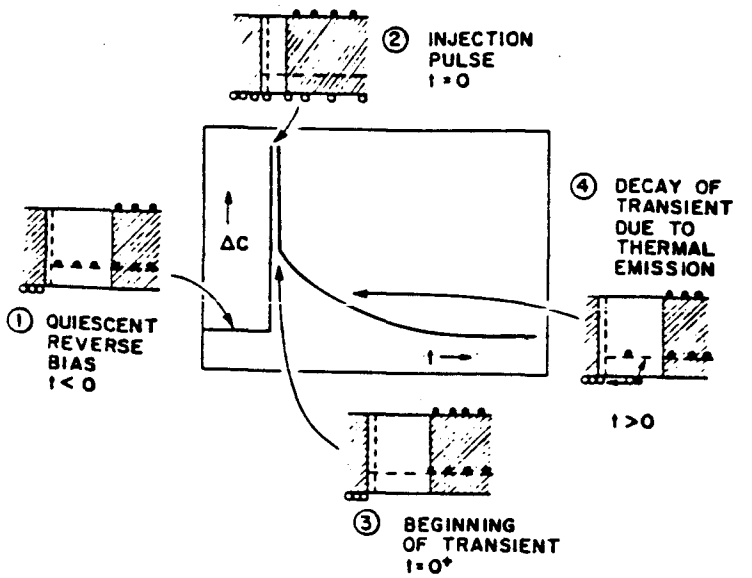


Figure 16b) The capacitance transient caused by thermal emission from a minority carrier trap after Lang [52].

3.2 CURRENT DLTS

The capacitance DLTS technique is limited in the case of small FET devices which have only very small capacitances. Instead, current DLTS is used for characterizing MOS. devices [55-60]. An schematic diagram of current DLTS can be seen in Figure 17. As shown, a pulse V_G is applied to the gate of a transistor which repeatedly turns the transistor "on" and "off". During the off state any trap at the interface of $Si-SiO_2$ and channel of MOSFET device will be filled, and during the on state the filled traps present in the resulting depletion layer will emit the captured carriers. Chen et al [57] have derived an expression for the resulting drain current from the emission rate and concentration of bulk traps. The expression is for linear region of the transistor operation where Vds is small, and is given as

$$I_{ds} = \mu C_0 \frac{W}{L}\left(V_{gs} - \left\{V_{FB} + 2\phi_F + \frac{Q_B}{C_0}\left(1 - \frac{N_T}{2N_A}\exp\left(\frac{-t}{\tau}\right)\right)\right\} - \frac{V_{ds}}{2}\right)V_{ds} \qquad (22)$$

N_T represents the trap concentration. Using the rate window concept, the same procedures are applied to the current transient measurements as were presented for capacitance deep level transient spectroscopy to obtain the position of the traps in the bandgap and the trap concentration.

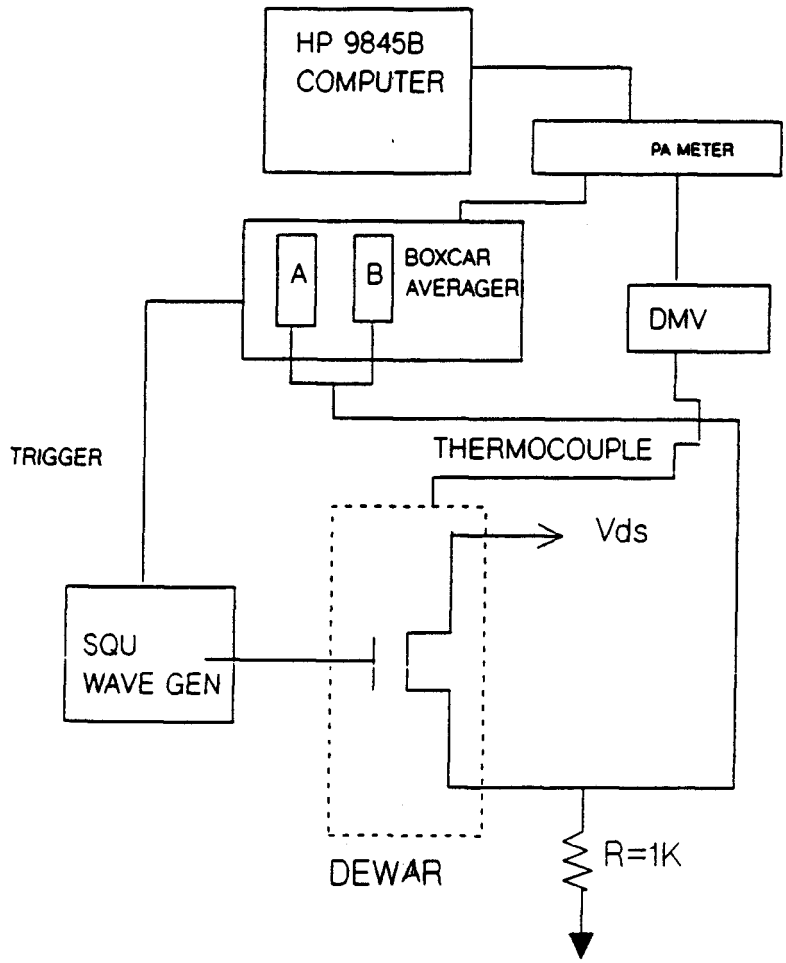


Figure 17) The current deep level transient spectroscopy system diagram.

3.3 PHOTOCAPACITANCE MEASUREMENT

Photocapacitance transient measurements have been used here to further investigate the oxygen induced microdefects. The measurements were made on the same samples used for DLTS measurements to ensure a correlation of the observations. Photocapacitance is related to DLTS and TSCAP (Thermally simulated capacitance). All these systems are parametric measurements, i.e., the effect of the filling and emptying of traps is monitored by the change in junction capacitance. Photon stimulated emission processes have been summarized by White [61] and Bois et al [62] where photocapacitance is a slowly varying function of the incident photon energy, and fitting parameters are needed to determine the threshold energy and optical cross section. The rate equation (13) can be modified to include the optical emission rate.

$$\frac{dn_T}{dt} = \left(C_n n + e_p + e_p^\circ\right)\left(N_T - n_T\right) - \left(C_p p + e_n + e_n^\circ\right) n_T \qquad (23)$$

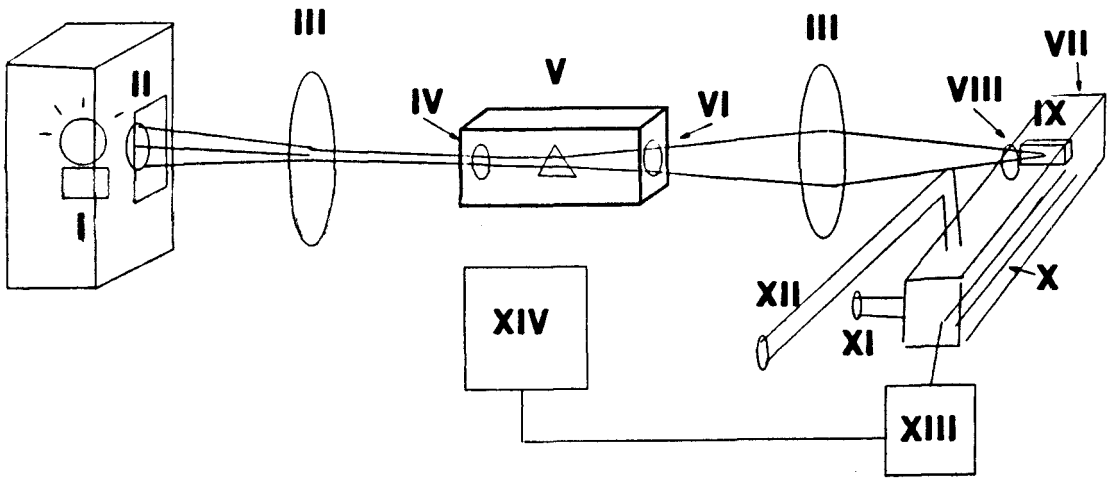
Where

$$e_p^\circ = \sigma_p^\circ S \qquad (24)$$

$$e_n^\circ = \sigma_n^\circ S \qquad (25)$$

e_n° and e_p° are the optical electron and hole emission rates, σ_n° and σ_p° are electron and hole capture rates respectively, and S is the optical flux in photons/cm^2 sec. The optical properties of a given defect can be defined by σ_n° and σ_p°, which are functions of photon energy. In n-type samples, $\sigma_n^\circ(h\nu)$ is

the optical absorption cross section. To obtain the $\sigma_n(h\nu)$ cross section, samples were maintained at steady low temperature of 120 K with an expander DE-2 and a Helium pump. A monochromatic light (tungsten halide source through a momochromator) is focussed on the sample with a wavelength such that $h\nu < \delta E$. The photon energy is then slowly increased. When the photon energy comes close to being equal to the defect energy level, trapped electrons are promoted to the conduction band by the photoelectric effect, which will produce a change in the junction capacitance. The photocapacitance method is complicated by the fact that above the photoionization threshold the capture cross-section is a function of photon energy. Furthermore, the optical cross sections are usually very small and the light sources are not very intense. The photocapacitance method overall is very slow and calculation of energy levels are very time consuming, i.e., the time constant of a photocapacitance exponential transient is obtained by plotting log δC versus time and calculate the slope of the line which results for one wavelength; this will be one point on the energy versus the cross-section plot. Other points are obtained by repeating the time constant calculation process. From the photon energy versus cross-section plot, the optical ionization energy is obtained. Figure 18 shows the photocapacitance system diagram.



I. Tungsten halide source

II. Silicon/Germanium filter

III. Convex lens

IV. Input grating of the monochromater

V. Jarrell-Ash Monochrometer

VI. Output Grating of the monochromater

VII. Expander DE-2

VIII. Quartz window

IX. Schottky diode

X. Temperature regulator

XI. Cryogenic vacuum pump

XII. Helium pump

XIII. HP 4280A Capacitance measurement system

XIV. HP9836 Computer

Figure 18) The Photocapacitance system diagram.

3.4 FAST FOURIER INFRARED SPECTROPHOTOMETRY (FTIR)

FTIR measurements were used before heat treatment to measure the oxygen and carbon concentration and after heat treatment to measure the reduction in these two concentrations. The infrared region starts at a wavelength 0.7 um and ends at 500 um. Normally infrared measurments are expressed in terms of wavenumber which is the inverse of wavelength in units of centimeters. Infrared absorption generally corresponds to changes in vibrational and rotational levels of a molecule. Infrared absorption occurs when the frequency of the alternating electric field associated with the incident radiation matches a possible change in the vibration or rotational freguency of the absorbing molecule. When a match occurs the incident frequency can be absorbed by the molecule causing a change in the amplitude of the vibration or a change in the rate of rotation. A change of dipole moment is necessary for a molecule in order to be able to absorb the incident electromagnetic radition. Otherwise, no energy transfer to molecule is possible. For example N_2 or O_2 which have symmetricl charge distributions can not be detected by the infrared method. Figure 19 shows a FTIR meaurement of absorbance vs wavenumber where the carbon absorption is at 604 cm^{-1} and oxygen at 1106 cm^{-1}. A correlation factor is defined based on ASTM standards and is used to calculate the concentration of oxygen and carbon in silicon.

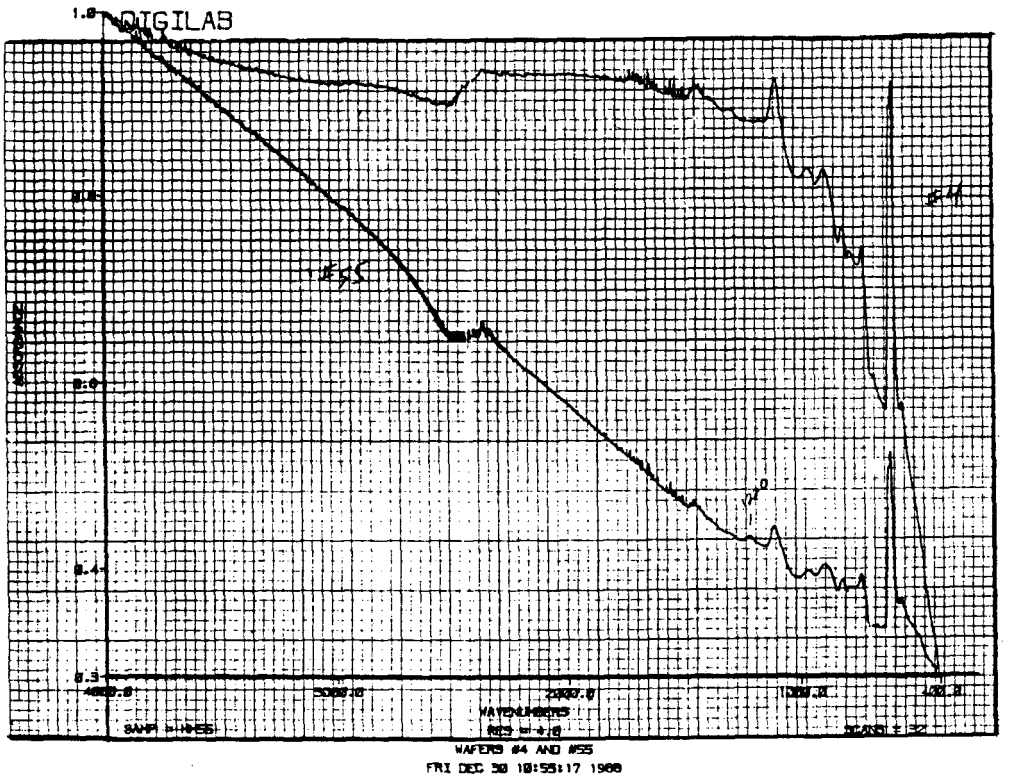


Figure 19) FITR measurements of absorbance vs wavenumber of heat treated wafers

3.5 MOSFET DEVICE AND AGING MEASUREMENT SYSTEMS

A TECAP (Transistor Electrical Characterization and Analysis Program) system was used to analyze MOSFET devices before and after aging. TECAP is a set of HP software which transforms measured data into transistor model parameters [63] which are used for circuit simulation systems. TECAP was used in this study to accurately measure device parameters such as threshold voltage, device currents and subthreshold currents before and after aging. The TECAP hardware consist of an HP9836 desktop comuputer, HP4145 semiconductor parameter analyzer, HP2671 thermal printer and a probe station. The communication between the hardware is through HP-IB. An HP4280A can be added to TECAP to measure C-V plots. Figure 20 shows the TECAP system. For the aging system a set of hardware similar to the TECAP system was used with an in-house developed software [64] to monitor automatically device parameters such as threshold, transconductance, substrate current, device linear and saturation currents at predefined times and calculate the degradation rate of these parameters. After aging n-channel devices, some of these were used for current-DLTS measurements and some for hot chuck measurements for studing the defect energy levels and detrapping processes.

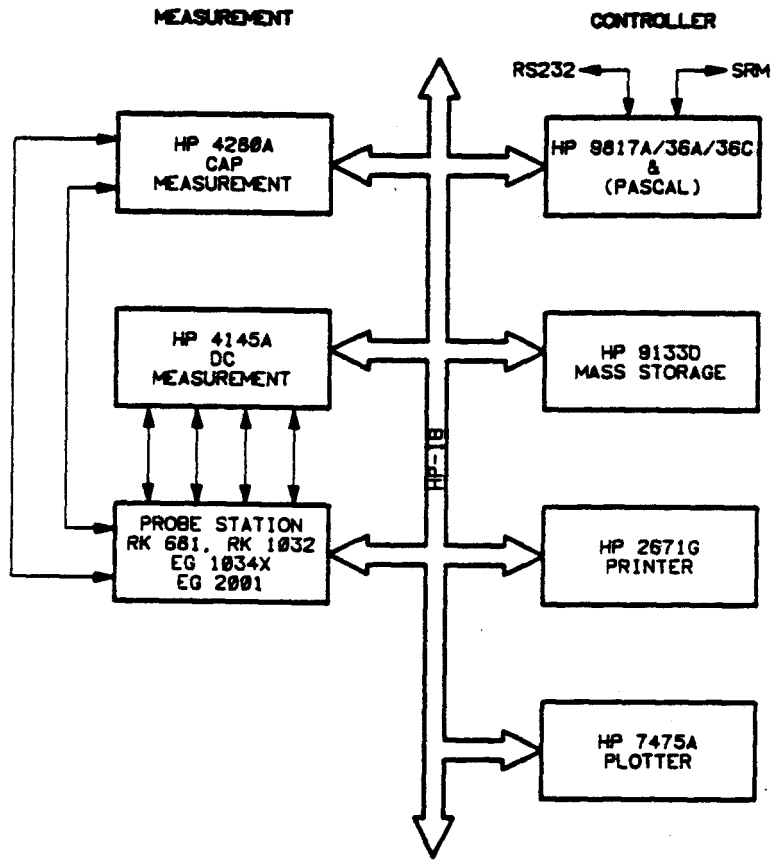


Figure 20) TECAP Transistor parameter measurement system [63]

4. EXPERIMENTAL PROCEDURES AND RESULTS

PART I. MATERIAL CHARACTERIZATION

In first section of this chapter different heat treatment cycles for inducing oxygen micordefects and stacking faults will be presented. In the second section a brief introduction to the fabrication of Schottky diodes on polished silicon surfaces will be discussed. The last section will be on DLTS and photocapacitance characterization of heat treated wafers with different initial concentrations of oxygen and carbon impurities.

4.1 HEAT TREATMENT CYCLES

The wafers used in this work were provided from two vendors and then numbered alphanumerically. They were phosphorus-doped, n-type, 100 mm diameter Czochralski (CZ) silicon of (100) orientation with resistivity of 5-7 ohm-cm. To induce microdefects and stacking faults various annealing cycles were carried out, as shown in Figure 21. Since, we are interested in studying the bulk stacking faults and microdefects, wafers were not subjected to the first high oxygen outdiffusion as is normally done in the three step (high-low-high) CMOS heat treatment cycle. Wafers were heat treated at 750 C for 16 hours in nitrogen to maximize the oxygen precipitation and then were subjected to various high temperatures in a nitrogen gas ambient for precipitate

growth. An hour oxidation was done after the low 750 C anneal to reduce surface pits.

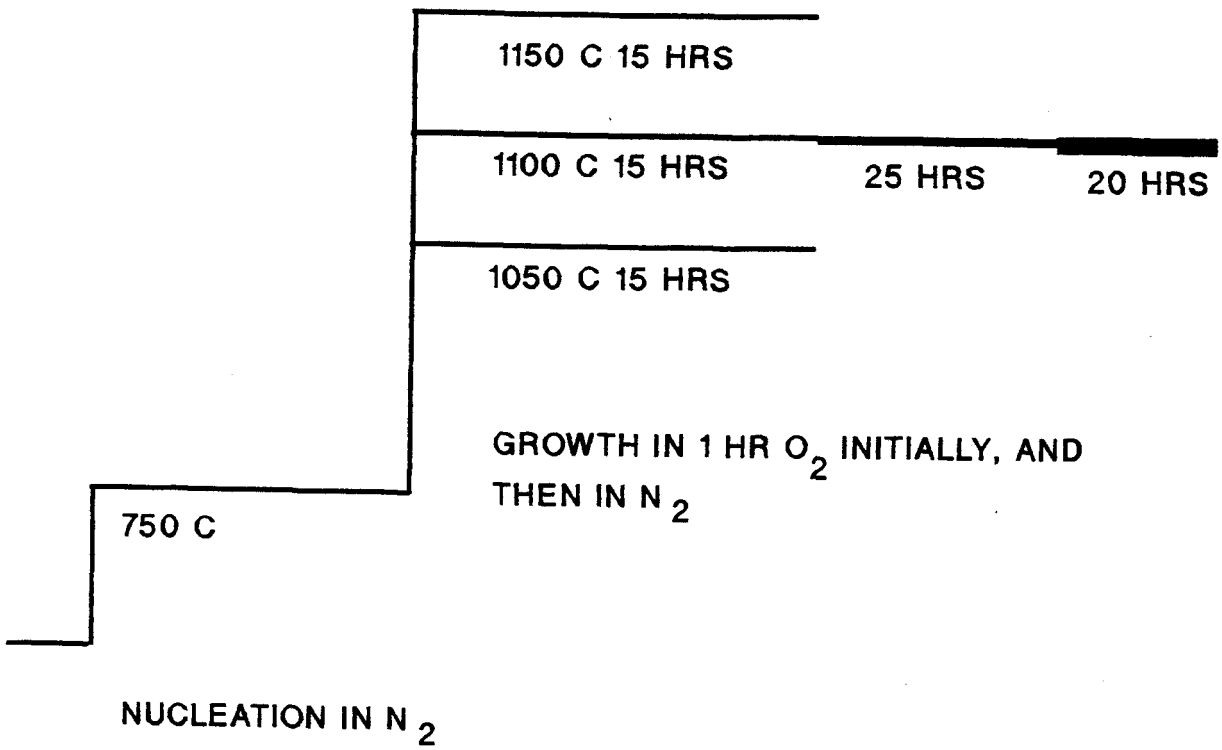


Figure 21) Heat treatment cycles for studying the bulk microdefects and stacking faults.

The oxygen and carbon concentrations were determined with FTIR measurements using either a Nicolet or Digilab instrument. All the measurements were based on 1979 ASTM standards. Table 1 shows the FTIR measurement of oxygen and carbon concentrations before and after a 750 C/ 16 hours and 1050 C/ 16 hours heat treatment cycle. Stacking faults were not detected optically on wafers 3,4,16,18,22,and 23.

WAFERS HEAT TREATED AT HEWLETT-PACKARD				
WAFER	O_F-O_I PPMA	C_I PPMA	C_F PPMA	STACKING FAULTS
3	20.879	.038	.032	NO
4	19.61	.096	.113	NO
9	20.195	.034	.053	YES
10	19.708	.096	.137	YES
16	21.84	0	.027	NO
17	20.373	0	0	YES
18	19.221	.103	.124	NO
19	16.332	.093	.073	YES
22	19.299	.043	.119	NO
23	19.45	.051	.105	NO
24	17.143	0	0	YES
26	17.535	0	0	YES
27	21.102	0	0	YES
31	19.618	0	0	YES
WAFERS HEAT TREATED AT OSU				
55	25.173	0	0	YES
71	26.010	0	0	YES
107	19.136	0	0	YES

Table 1) A summary of main wafers used for studying the bulk defect with DLTS.

The possibility that facility-related impurities play a role in this study is reduced by heat treatments at two different locations, at the Hewlett-Packard fabrication facility, and at Oregon State's silicon material processing laboratory.

4.2 SCHOTTKY DIODE FABRICATION

The theoretical models of metal-semiconductor interfaces have been described in several text books [65-66]. Investigation into the actual physical picture of the metal-semicondutor interface has been an active area of research due to the important effects on semiconductor device characteristics [67]. In this work, we will use various techniques to obtain low leakage diodes on n-type wafers. After a two steps heat treatment cycle, about 20 um was etched from the sample surface to remove any denuded zone that might have formed. Initially, a combination of mechanical polish and chemical (CP4 or Planar) etch was used. this technique resulted in a very poor yield (high leakage Schottky diodes). The second method was Plasma etch (SF6+O2) to etch silicon surface. The plasma method improved the silicon surfaces and resulted in a very repeatable process with low leakage Schottky diodes. Figure 22 shows a three steps process to fabricate Schottky diodes on an etched silicon surface. After the plasma etch, the wafers were processed in a HF tank for two minutes to remove any native oxide and then 5 mins in rinse and dry. Immediately, after these simple cleaning steps, the wafers were placed in a vacuum chamber for metal deposition. Back side contact were made initially with aluminum evaporation and then an alloy at 300 C to ensure ohmic contacts. Then, aluminum was evaporated through a metal dot mask to fabricate Schottky

diodes on the front side of the wafers. Capacitance-voltage (C-V) and current-voltage (I-V) characteristics were checked before any DLTS measurement to ensure low leakage (less than 1 um). I-V and C-V curves of a typical Schottky diodes are shown in Figure 23. The current density of a diode can be expressed as

$$J = J_s \exp\left(\frac{qV}{nKT}\right) \qquad for V > \frac{kT}{q} \qquad (26)$$

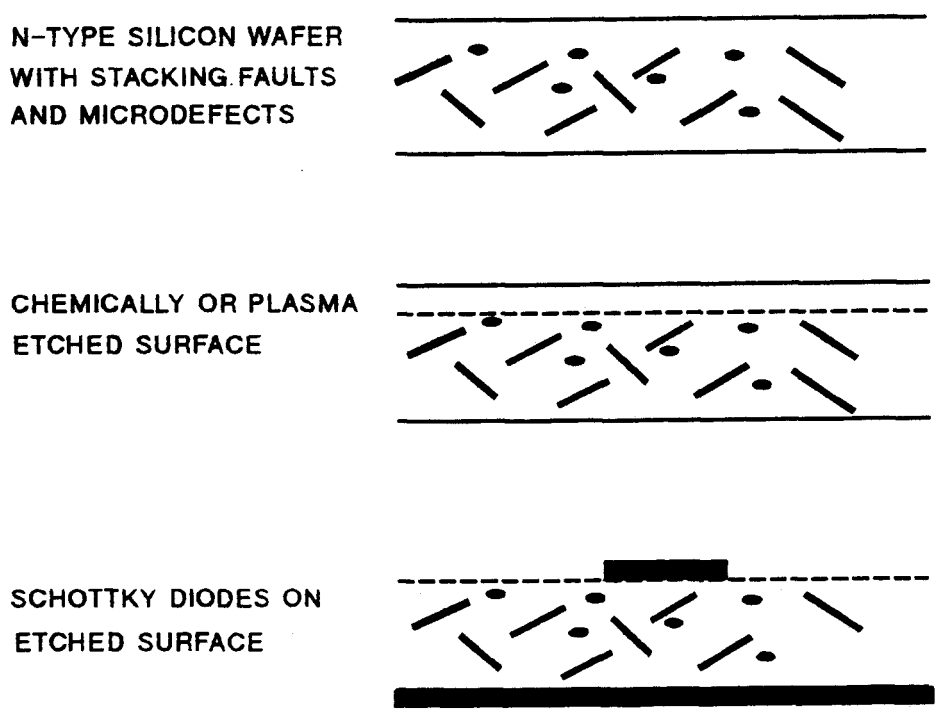
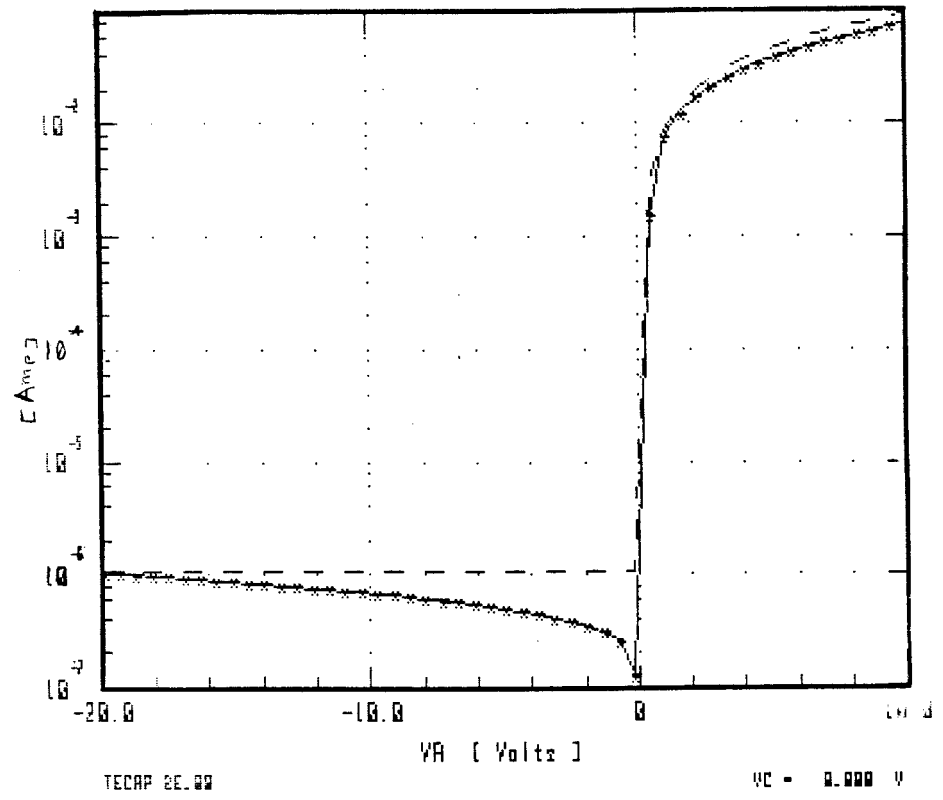


Figure 22) A three step process to make Schottky diodes on an etched silicon surface.



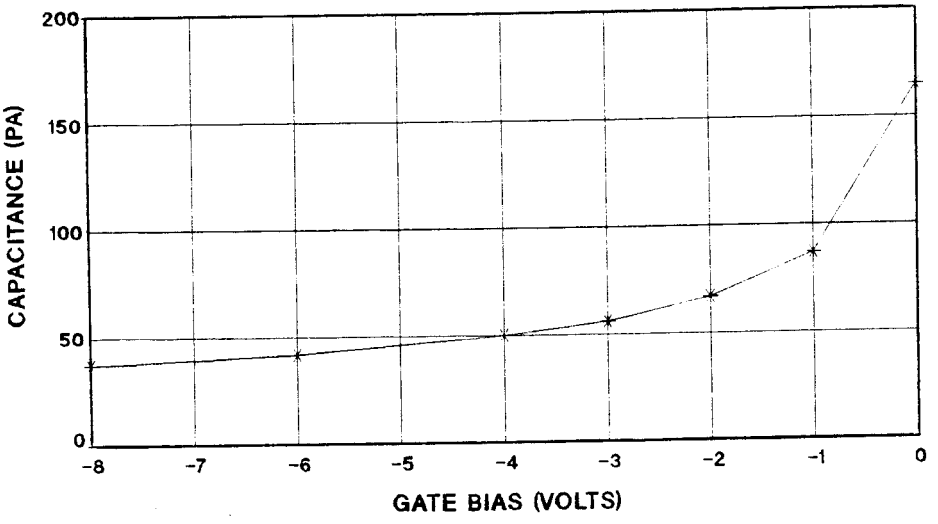


Figure 23) I-V and C-V characteristics of a heat treated and plasma etched wafer (#71)

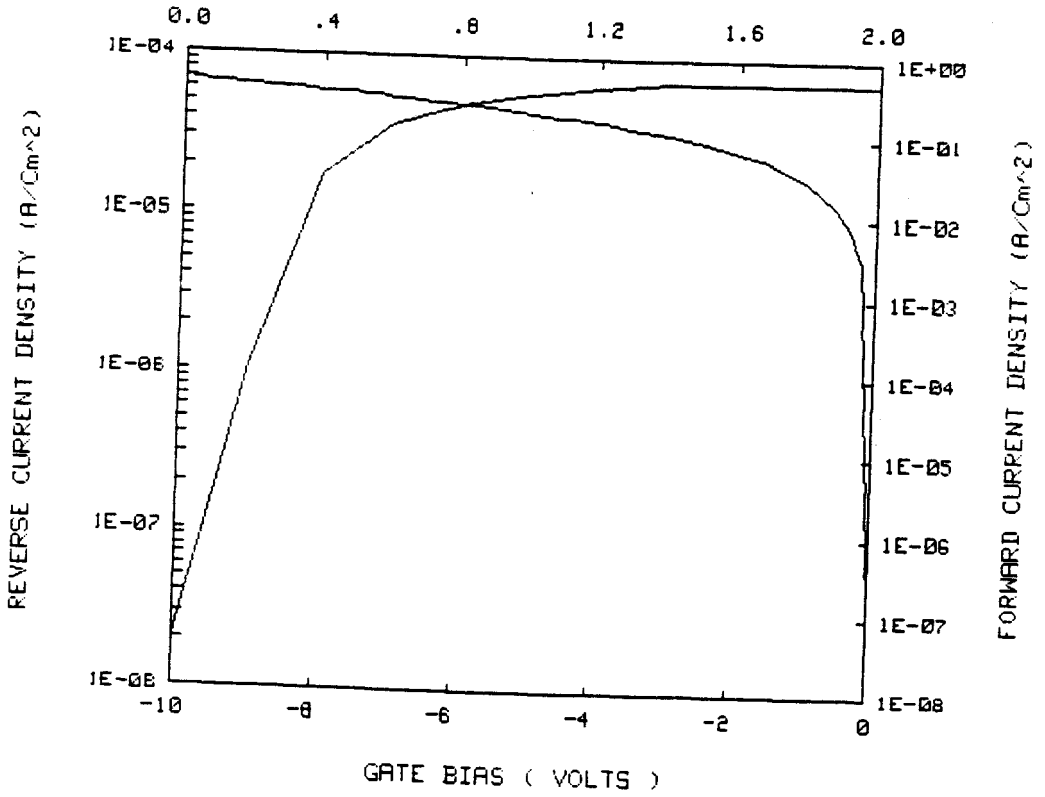


Figure 24) Saturation current and ideality factor can be obtained from log-linear I-V plot (wafer #25)

where Js is the saturation current density and can be obtained by extrapolating the current density from the a log-linear plot to V=0. Figure 24 shows the forward and reverse current densities of a Schottky diode on wafer #25. The parameter (n) is called the ideality factor. The ideality factors for Schottky diodes made for this study were very close to unity (n= 1.1).

4.3 DLTS CHARACTERIZATION OF HEAT TREATED WAFERS

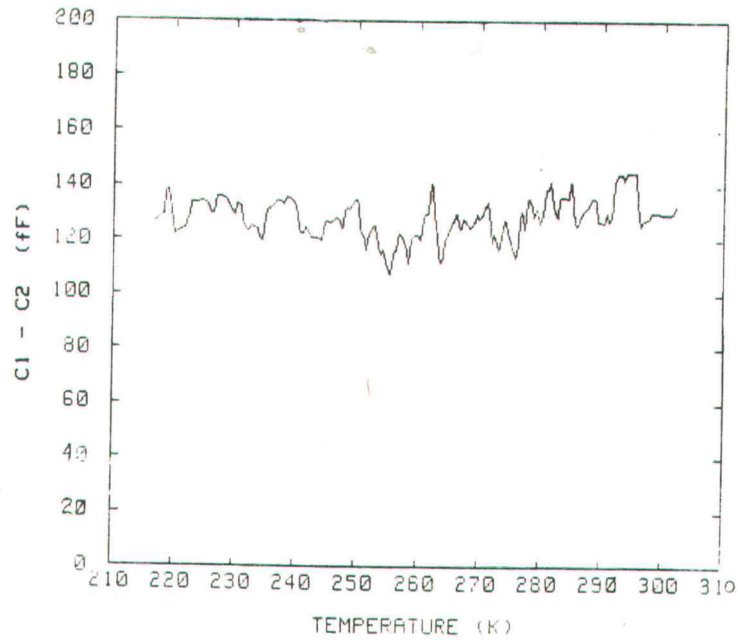
Schottky diodes on etched silicon surfaces with acceptable leakage currents (less than 50 uA at -2.5 volts reverse bias) were used for characterizing the oxygen induced microdefects. A C-V plot was done to ensure reasonable diode characteristics before any DLTS measurement. Schottky diodes are asymmetric junctions where the depletion region is primarily in the low doped silicon material side. DLTS signals are sensitive to only the defects in depletion region which is on the order of 2 um at the highest reverse bias. Therefore, a denuded zone of 5-20 um has to be etched off for DLTS characterization of bulk microdefects and stacking faults. Capacitance DLTS measurements initially were performed on both n- and p-type silicon wafers [68]. In order to correlate the DLTS results with the physical defects, a Wright etch [69] was used to preferentially etch the silicon surfaces under the Schottky diodes. A correlation was found between the stacking fault size and density and the DLTS trap concentration measurement when the initial carbon concentration in a wafer was below the FITR detection limit which is $1x10^{15}/cm^3$ [70]. Figure 25 shows the results for wafer #25 with no heat treatment and no surface etch. The DLTS spectra shows no peaks and there were no microdefects on the etched wafer surface after Wright etch with optical photo with magnification of about 1500X, as is shown in Figure 25. Plasma etch (SF_6+O_2) was used to etch of the

silicon surfaces since mechanical and chemical etches resulted in high leakage Schottky diodes . Figure 26 shows the DLTS measurement of a Schottky diode fabricated on a control wafer with no heat treatment but with 25 microns of the top surface etched off in a SF6+O2 plasma. No DLTS peak was detected on plasma etched control samples, and this method was used for etching off the denuded zone. Figures 27-37 show that wafers 3, 4, 9, 10, 16, 18, 19, 22, and 23 have no DLTS peak even in the presence of stacking faults (Wafers 9, 10, 19 have stacking faults). Wafers 17, 24, 26, 27, 31, 55, 71, and 107 all have a consistent DLTS peak at 260 K (for a DLTS rate window of t1/t2=10/40). The only difference between these two sets of wafers is the initial carbon. When a small trace of carbon is detected on a wafer, then the the oxygen induced micordefects show no electrical activity. Table 2 summarizes the DLTS measurement results. The wafers were heat treated in two different locations to minimize the the possibility that facility-related impurity concentrations play a role in this study. Figure 38 shows the Arrhenius plot of the emission rates vs temperature. A single dominant energy level at E_c-E_t=.48 +/- .05 ev was detected on wafers 17, 24, 26, 71, 55, and 107 independent of facility when the carbon concentration was below detection limits (figure 38).

Figure 39a shows DLTS the spectra of control wafer B with no heat treatment or plasma etch before any mechanical damage to silicon surface. No peak was detected as expected.

However, after an intentional mechanical damage to the silicon surface under the Schottky diode a peak very similar to that which was detected on wafers with stacking faults but with low carbon was obtained. The interesting point is this peak is also very similar to Omling's [27] DLTS level D (see page 17-18). Omling related the DLTS line D to "Dangling bond" centers using EPR.

We will discuss this subject in chapter 7 and will develop a model that might account for these experimental results [71].



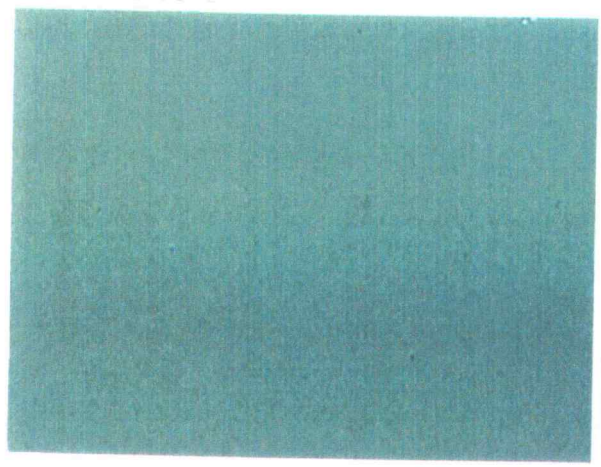
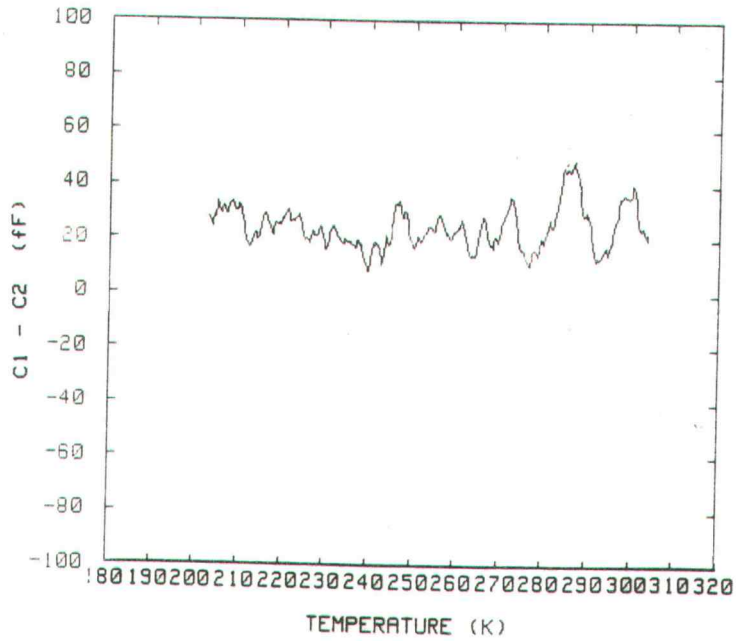


Figure 25) DLTS spectra of control sample #25 with no surface etch or heat treatment t1/t2= 10/40 mS, N_T=o and the optical photo of the etched silicon surface with magnification of 1500X



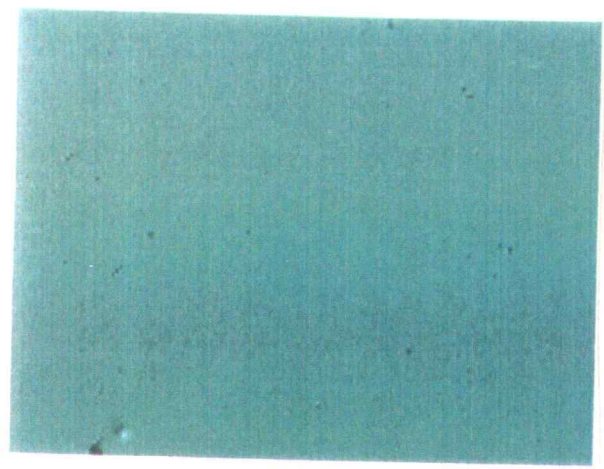
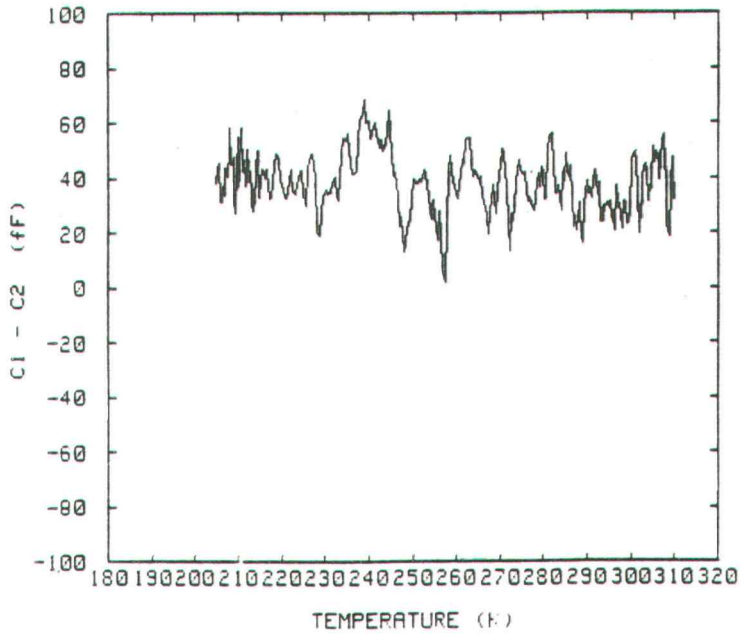


Figure 26) DLTS spectra of control sample #I with no heat treatment, but about 25 microns was plasma etched from the wafer surface to examine the plasma etching effect on the silicon surface. t1/t2 =10/40 mS, N_T=0 and the optical photo with magnification of 1500X



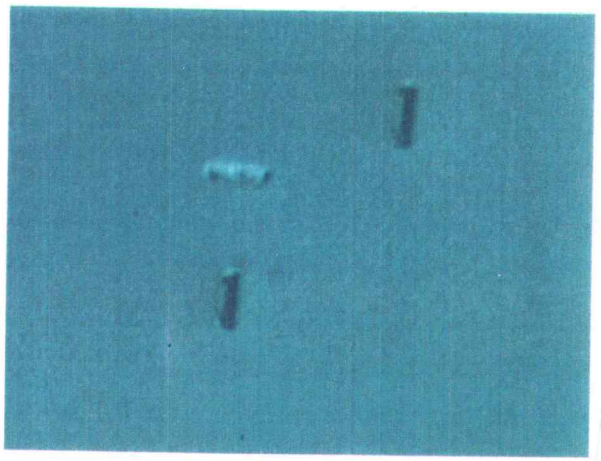
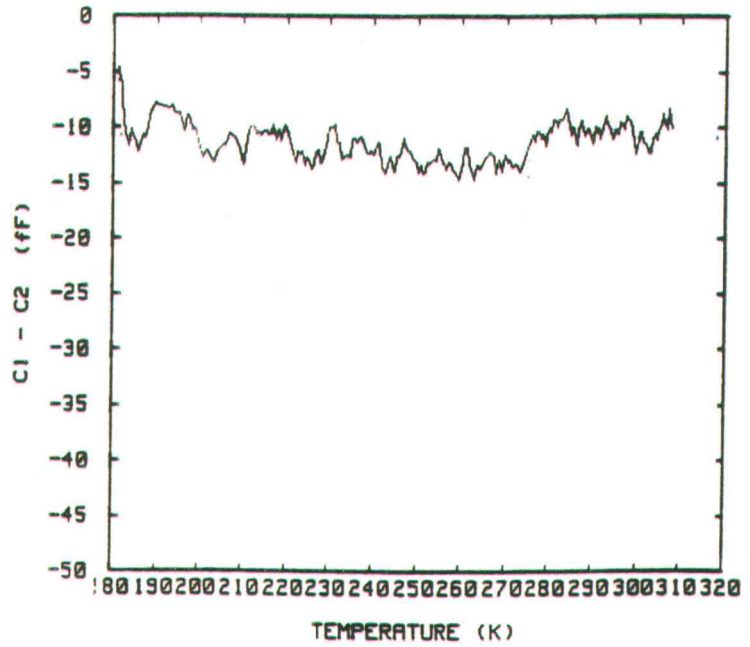


Figure 27) DLTS spectra of wafer #9. Carbon concentration is 2.56E15/cm^3. No electrical activity is detected. t1/t2=10/40 mS, N_T=0 and the optical photo of the etched silicon surface with magnification of 1500X



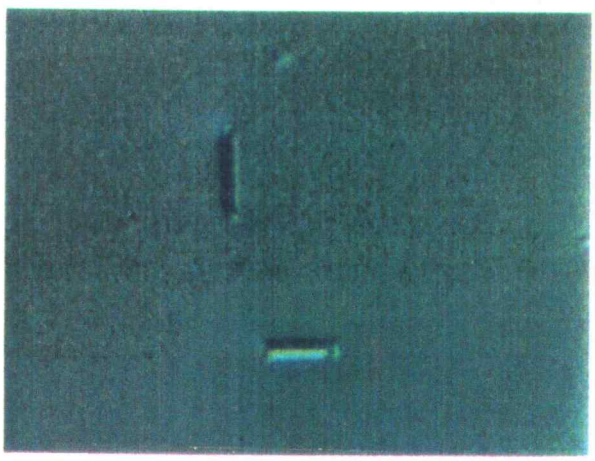


Figure 28) DLTS spectra of wafer #10. Carbon concentration is 6.8E15/ cm^3. No electrical activity is detected. t1/t2=10/40 mS, N_T=0 and the optical photo of the etched silicon surface with magnification of 1500X

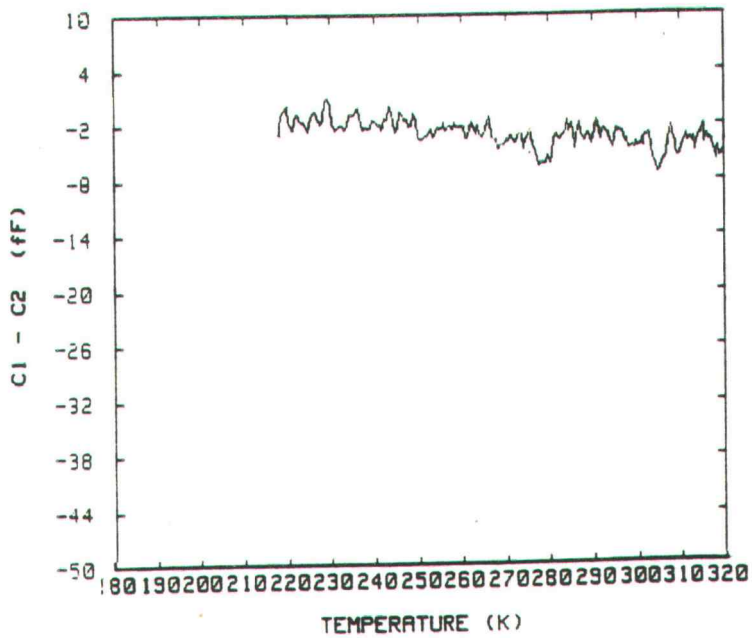
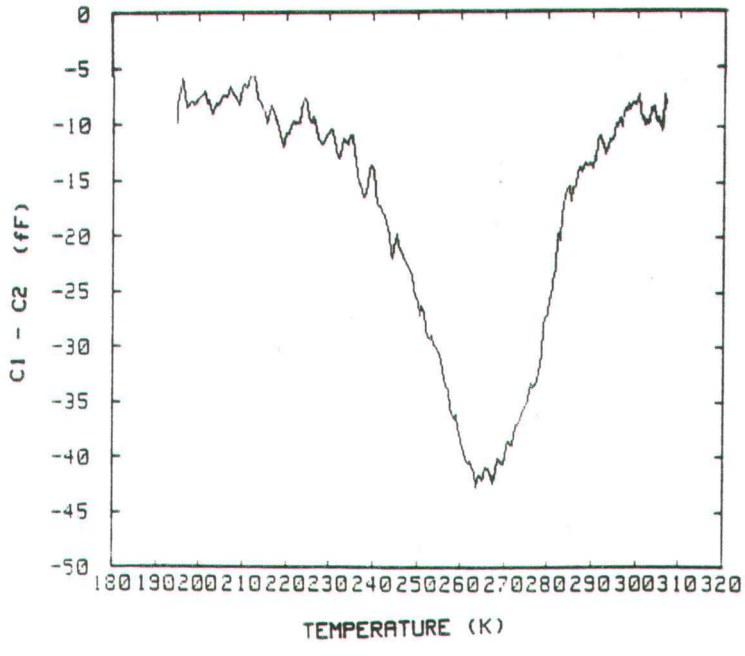


Figure 29) DLTS spectra of wafer #16 . Carbon concentration is 1.349E15 /cm^3. No electrical activity is detected. t1/t2=10/40 mS, N_T=0 and the optical photo of the etched silicon surface with magnification of 1500X



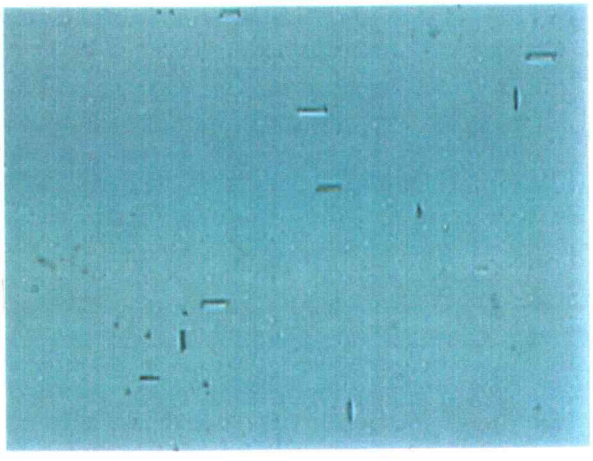


Figure 30) DLTS spectra of wafer #17. Carbon concentration is below detection limits. t1/t2=10/40 mS, N_T=2.0E12/ cm^3 and the optical photo of the etched silicon surface with magnification of 1500X

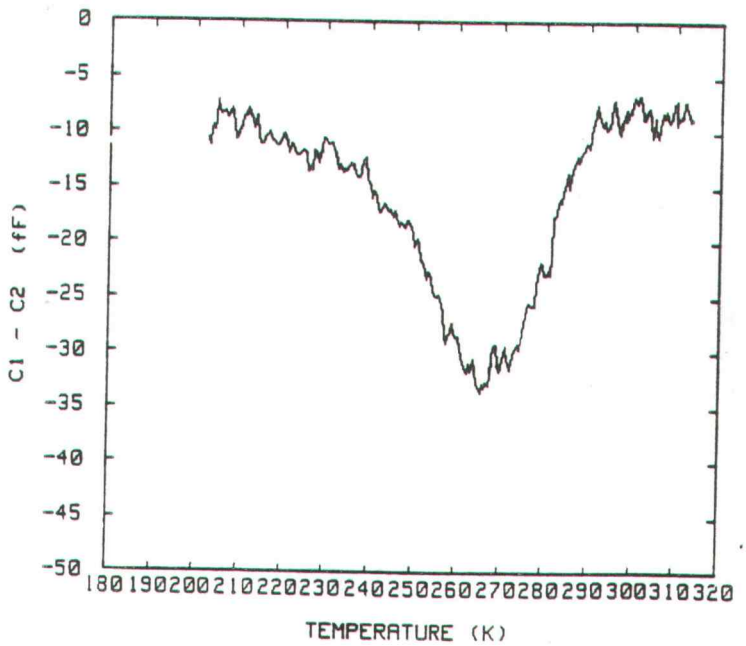


Figure 31) DLTS spectra of wafer #24. Carbon concentration is below detection limits. t1/t2=10/40 mS, N_T=7.0E11/ cm^3 and the optical photo of the etched silicon surface with magnification of 1500X

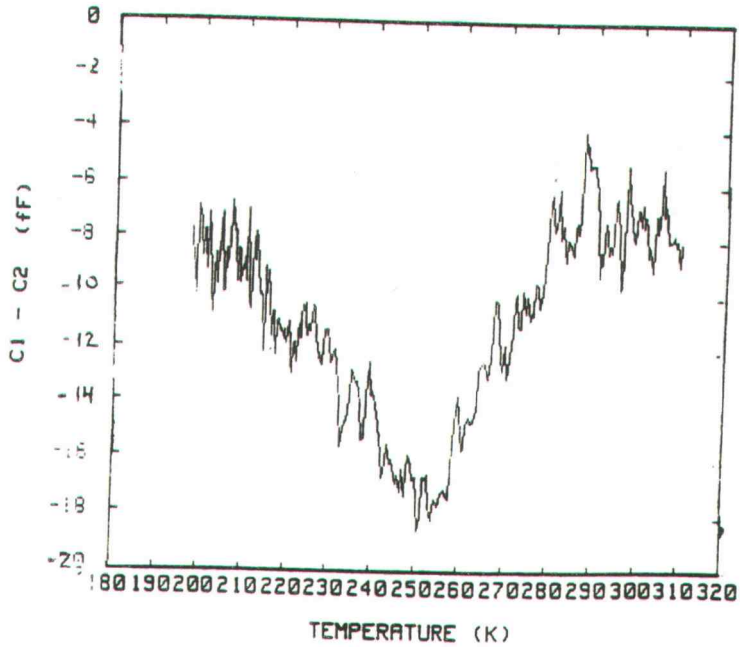
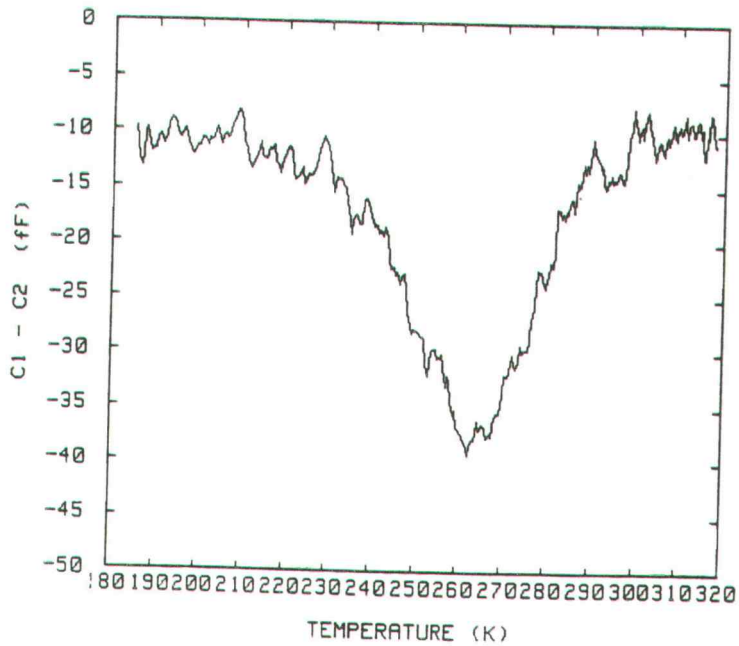


Figure 32) DLTS spectra of wafer #26. Carbon concentration is below detection limits. t1/t2=10/40 mS, N_T=3.69E11/ cm^3 and the optical photo of the etched silicon surface with magnification of 1500X



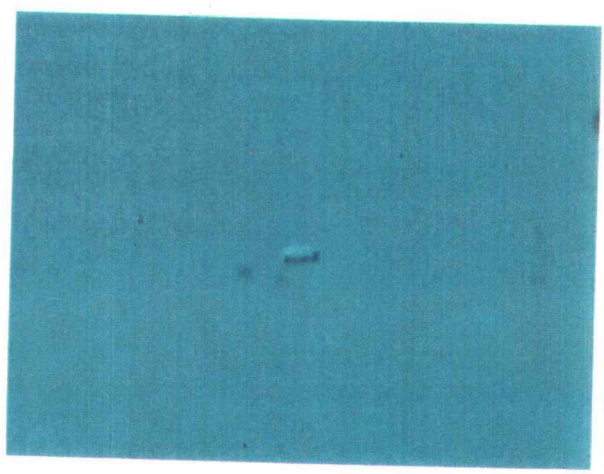
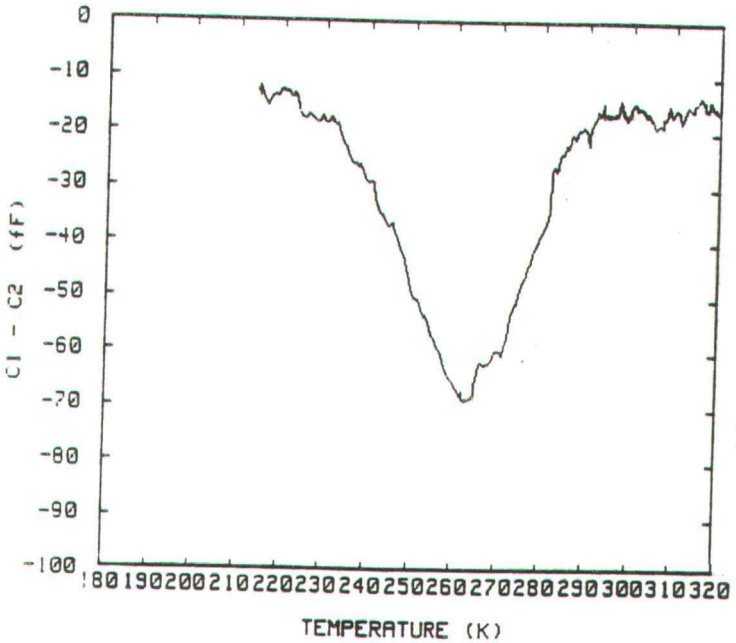


Figure 33) DLTS spectra of wafer #27. Carbon concentration is below detection limits. t1/t2=10/40 mS, N_T=8.1E11/ cm^3 and the optical photo of the etched silicon surface with magnification of 1500X



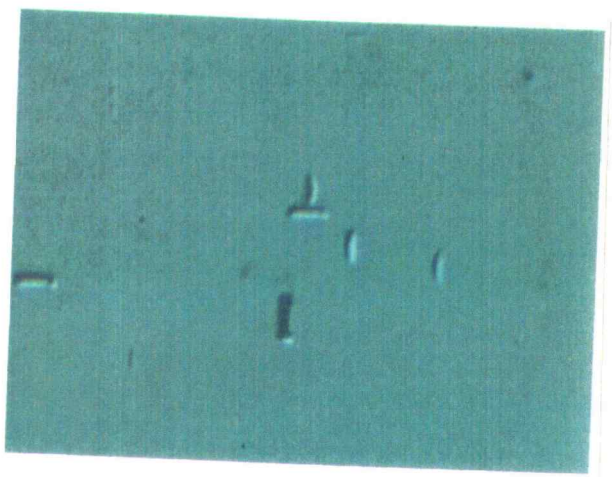
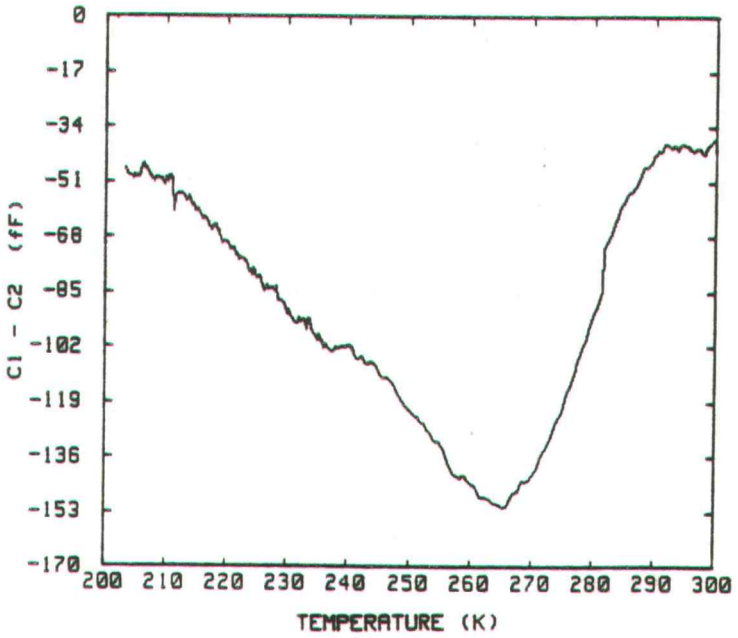


Figure 34) DLTS spectra of wafer #31. Carbon concentration is below detection limits. t1/t2=10/40 mS, N_T=6E11/ cm^3 and the optical photo of the etched silicon surface with magnification of 1500X



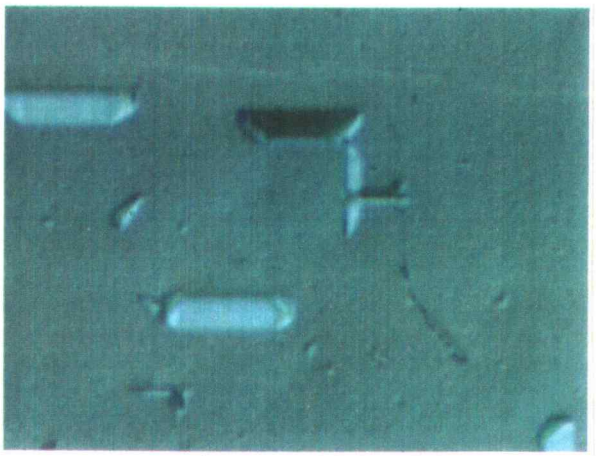
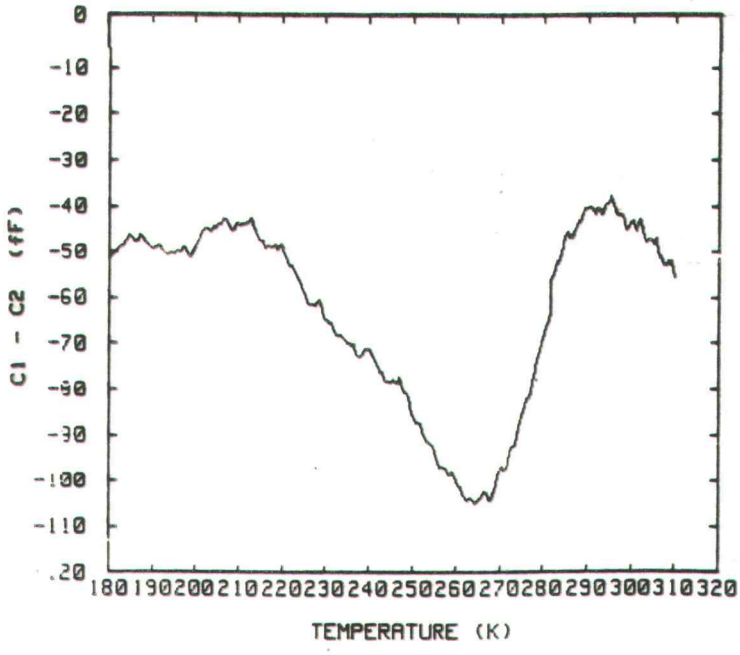


Figure 35) DLTS spectra of wafer #55. Carbon concentration is below detection limits. t1/t2=10/40 mS, N_T=2.9E12/ cm^3 and the optical photo of the etched silicon surface with magnification of 1500X



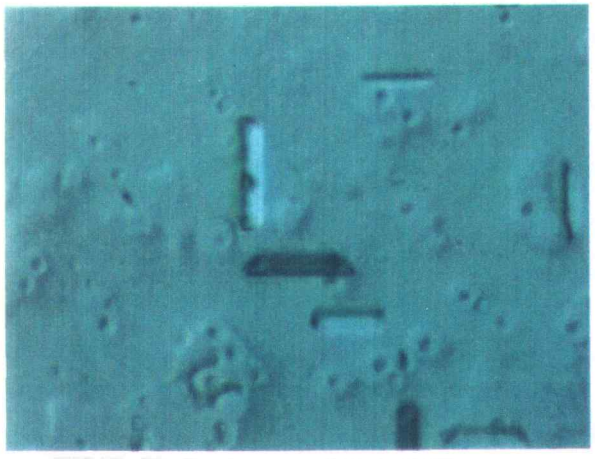
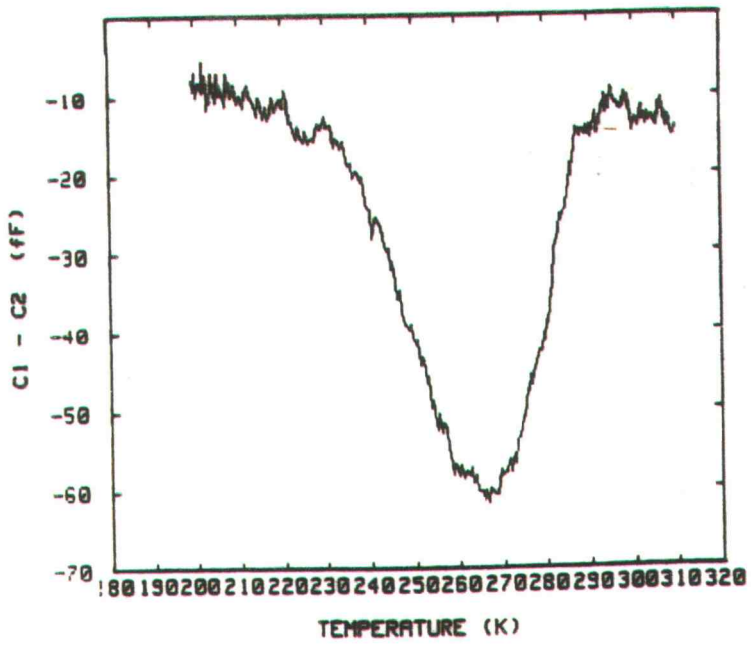


Figure 36) DLTS spectra of wafer #71. Carbon concentration is below detection limits. t1/t2=10/40 mS, N_T=3.2E12/ cm^3 and the optical photo of the etched silicon surface with magnification of 1500X



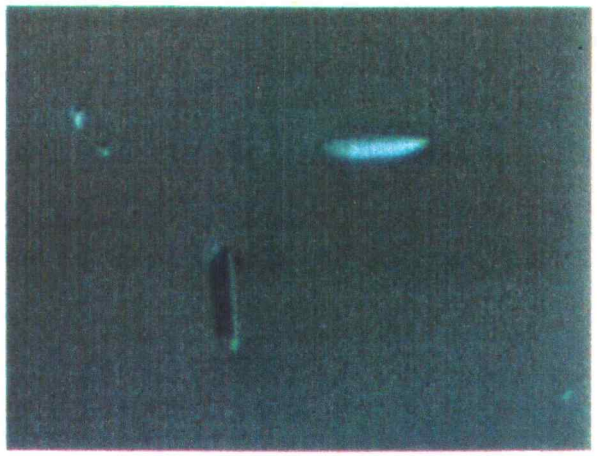


Figure 37) DLTS spectra of wafer #107. Carbon concentration is below detection limits. t1/t2=10/40 mS, N_T=7.7E11/ cm^3 and the optical photo of the etched silicon surface with magnification of 1500X

WAFERS HEAT TREATED AT HEWLETT-PACKARD					
WAFER	O_F-O_I PPMA	C_I PPMA	C_F PPMA	STACKING FAULTS	ELECTRICAL ACTIVITY /cm ^{3}
3	20.879	.038	.032	NO	0
4	19.61	.096	.113	NO	0
9	20.195	.034	.053	YES	0
10	19.708	.096	.137	YES	0
16	21.84	0	.027	NO	0
17	20.373	0	0	YES	2.0E12
18	19.221	.103	.124	NO	0
19	16.332	.093	.073	YES	0
22	19.299	.043	.119	NO	0
23	19.45	.051	.105	NO	0
24	17.143	0	0	YES	7.0E11
26	17.535	0	0	YES	3.69E11
27	21.102	0	0	YES	8.1E11
31	19.618	0	0	YES	6.0E11
WAFERS HEAT TREATED AT OREGON STATE UNIVERSITY					
55	25.173	0	0	YES	2.9E12
71	26.010	0	0	YES	3.2E12
107	19.136	0	0	YES	7.7E11

Table 2) A summary of the electrical activity of wafers used in this work with stacking faults. Wafers with detectable carbon concentration show no electrical activity.

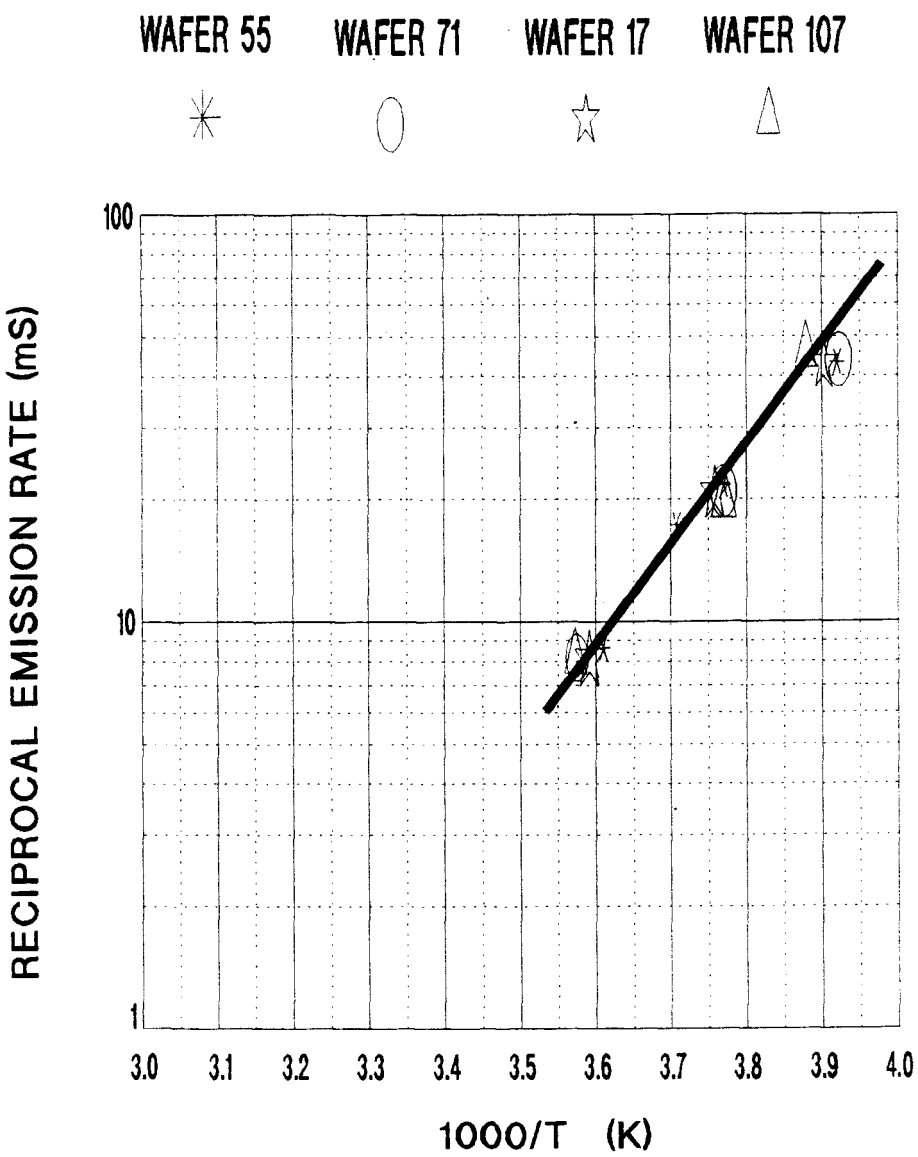


Figure 38) Arrhenius plots of emission rates for wafers 17, 55, 71, and 107. A single dominant energy level at E_c-E_t=.48 eV was detected on wafers with low carbon.

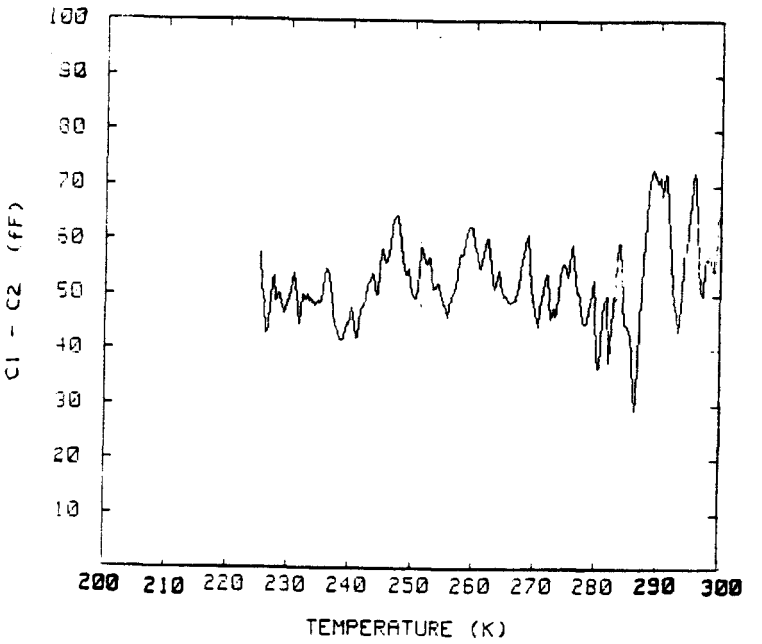


Figure 39a) DLTS spectra of control wafer B before mechanical damage.

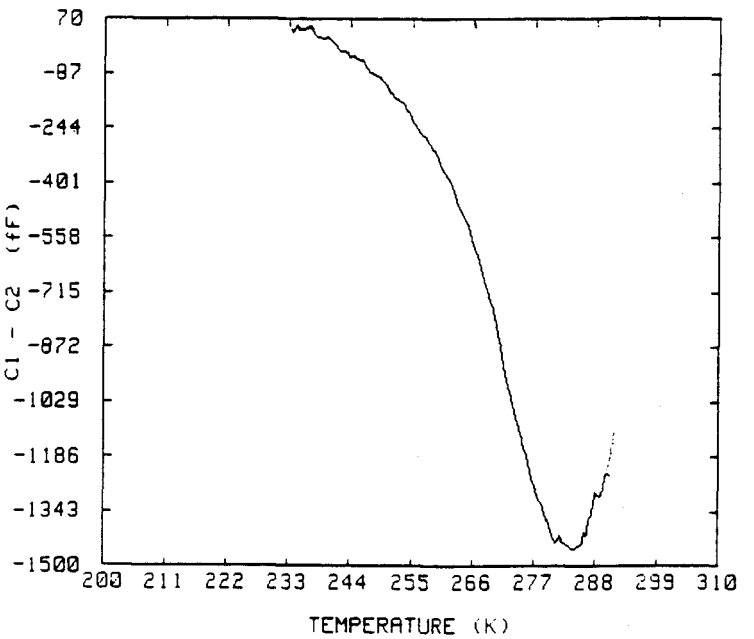


Figure 39b) DLTS spectra of control wafer B after mechanical damage.

4.4 PHOTOCAPACITANCE CHARACTERIZATION OF HEAT TREATED WAFERS

Photocapacitance measurements were done on approximately twenty different samples. The purpose of these measurements was to observe a correlation between DLTS and photocapacitance measurements. Photocapacitance measurements showed a clear correlation with DLTS signals on electrically active wafers such as 55, 71, 107 and a lack of response on electrically inactive wafers such as control and wafers 10 and 16. In terms of the prediction of energy levels of deep levels , DLTS predicted a dominant level on all heat treated wafers with stacking faults at .48 +/- .05 eV and photocapacitance measurements showed a spread of .1 eV centered around .46 eV. These measurements were consistent over several samples on a single wafer. A typical photocapacitance measurement involve the following three steps.

1. The Schottky diode is mounted in the expander (figure 18), and connected to the capacitance meter (HP 4280A) via two shielded probes. The diode has to be aligned to the tungsten light source. This alignment can be done when the monochromater is set to the visible light frequencies with two biconvex lenses.

2. After alignment, the diode is cooled down to 120 K by using a closed liquid helium pump system. A Xylene container is used to establish a vacuum in the expander DE-2 be-

fore the cooling process is initiated.

3. The capacitance transient needs to be obtained at regular intervals of a 100 nM starting at 1300 nM The monochromater is used to select the 1300 nM output. A silicon filter is inserted in front of the tungsten light source. A metallic shutter is inserted to block off the radiation ("dark" state). A program on the HP 9836 computer [72] that controls the data collection from HP 4280A is run to initialize the experiment. The shutter that has been blocking off the radiation is removed after the initialization is completed. The HP9836 computer starts to collects data based on the number of readings and intervals between each reading. Data can be plotted on the screen or be dumped on a printer.

This completes the measurements of the photocapacitance transient for one wavelength. The same three step procedure can be used to obtain transients at other wavelengths. Due to second or even third harmonics at 2000 nM or higher wavelength the silicon filter is replaced by a germanium filter.

A typical photocapacitance transient of a control sample with no heat treatment is shown in figure 40a. Wafer #55 with heat treatment shows the an exponential variation of the capacitance with time (Figure 40b). As previously mentioned, wafer #55 had stacking faults but the carbon

content was below detection limits of FTIR. Wafers 9,10,19,and 23 did not show any photocapacitance transients which confirms that the carbon content can reduce or eliminate the electrical activity of stacking faults. The time constant of each capacitance transient is extracted. A plot of log (Δ C versus time results a straight line confirming the exponential nature of the transient). The inverse of the slope of this line is the time constant of the transient. Figure 41a shows the optical cross-section vs the photon energy. Figure 41b shows that our experimental results closely follows the Lucovsky model [60]. The intersection with energy axis determines the energy level associated with the defect and the slight flattening out at the lower energies could be due to a spread of energy levels centered at .46 eV [73].

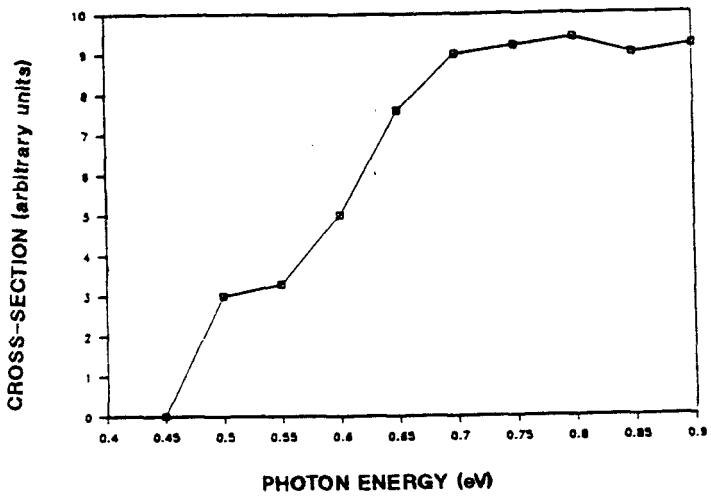


Figure 40a) Photocapacitance transient associated with the control sample (see figure 25).

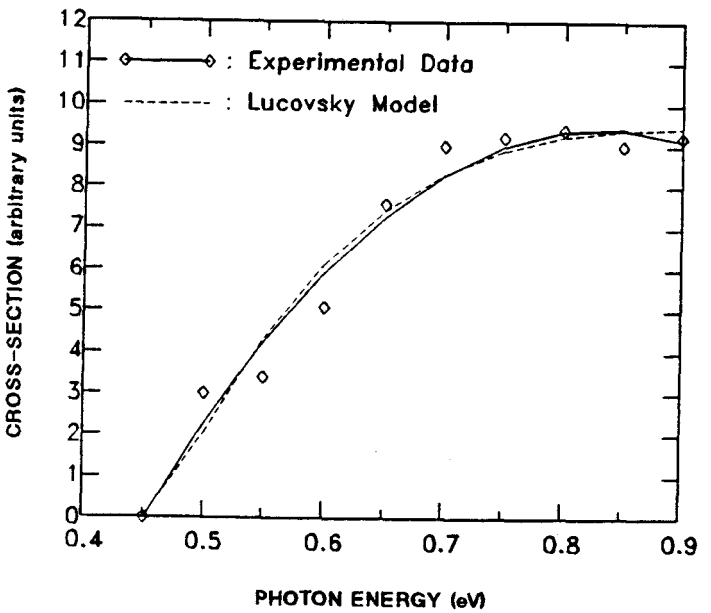


Figure 40b) Photocapacitance transient associated with wafer #55 (see figure 35)

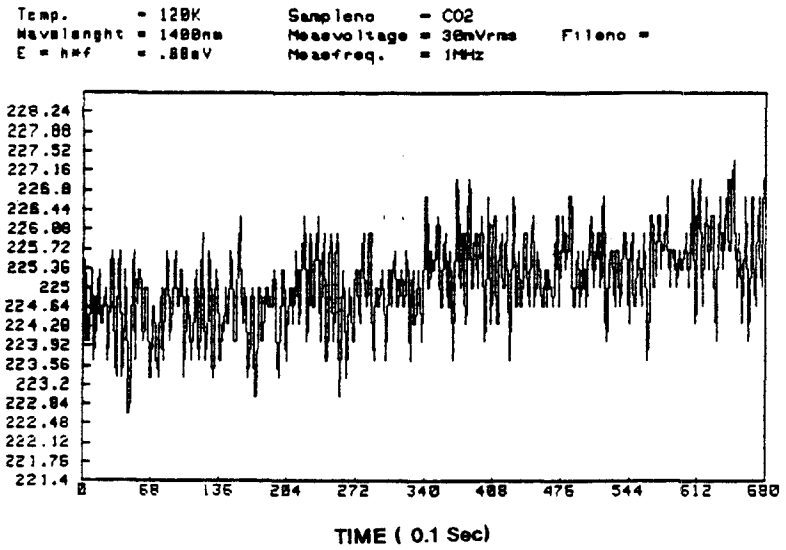


Figure 41a) Optical cross-section versus photon energy for wafer #55

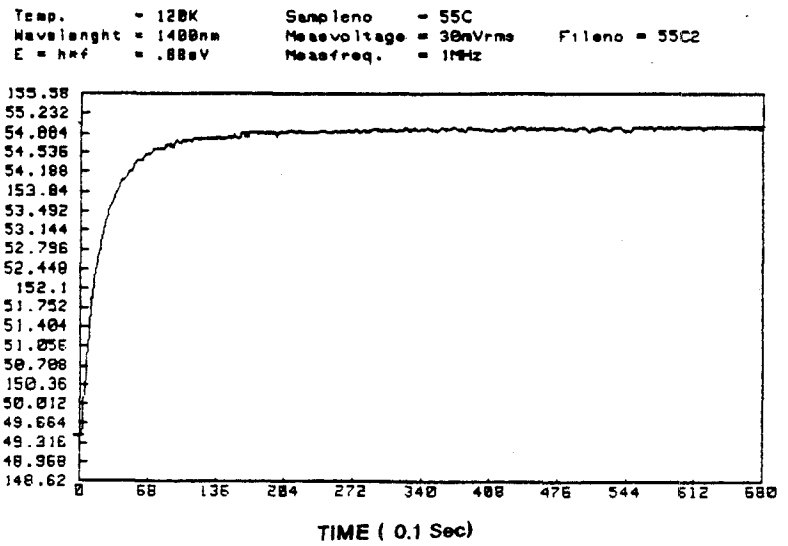


Figure 41b) Lucovsky model closely follows the experimental data for wafer #55.

5. EXPERIMENTAL PROCEDURE AND RESULTS

PART II. DEVICE CHARACTERIZATION

In this chapter n-channel MOSFET device reliability and hot carrier aging testing procedures will be discussed. Devices with an effective gate length of less than .8 micron were subjected to hot electron and hot hole degradation conditions. Then, these devices were subjected to high temperature to investigate detrapping of hot carriers as a function of temperature. In last part of this chapter the effect of carbon on the interface of $Si-SiO_2$ will be presented.

5.1 HOT ELECTRON AGING PROCEDURE AND RESULTS

As the MOSFET device dimensions continue to shrink to below 1 micron, departures from long channel behavior occur. Two main departures are:

1. In the long channel device gate and substrate voltages control the channel. However, in short channel devices gate and substrate voltage control of channel are weakened and velocity saturation and the influence of device boundaries can modify the current flow.
2. The high field effects can lead to carrier multiplication and injection of electrons and holes into the $Si-SiO_2$ interface and oxide .

The focus of this chapter is on high field issues. Hot electron related problems have become an important problem in CMOS and BICMOS technologies. One approach to manage hot carrier effects has been to reduce the operating voltage from the standard 5 Volts to 3.3 or even 2.5 Volts. However, this approach leads to the further problem of circuit compatibility and reduces device performance. In this section, procedures for measuring the hot carrier degradation of submicron devices is presented. N-channel devices were subjected the maximum aging stress, this was done by applying a high drain voltages (Vd=7.0 volts for devices with 200 A oxide) and gate voltage of about half of the drain voltage. From impact ionization electron-hole pairs are generated, electrons enter the oxide and the holes can be collected by either the oxide or the substrate terminal which is called the substrate current. Figure 42 shows the substrate current as a function of gate voltage. The substrate current increases first with VG to a maximum, and then start to decrease, the substrate current can be used to maximize the aging process. The maximum in substrate current can be explained [65] by assuming a uniform impact ionization in the pinch-off region where the substrate current can be written as

$$I_{sb} = I_d \alpha \Delta L \qquad (27)$$

where α is the ionization coefficient,and ΔL is the length of the pinch-off region.

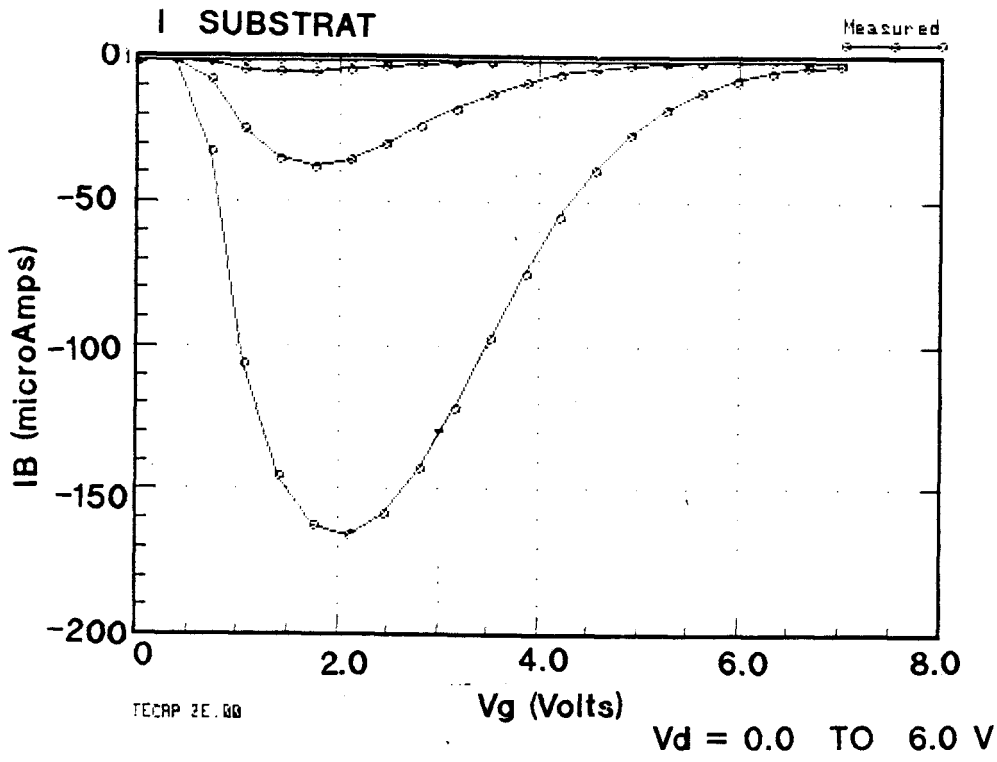


Figure 42) Substrate current as a function of gate voltage.

As gate voltage (V_g) increases, for a given V_d, both V_{dsat} and I_d increase. When V_{dsat} increases the lateral field deceases which cause a reduction in the impact ionization rate or α. The lateral field can be written as

$$E_{lateral} = \frac{(V_d - V_{dsat})}{L} \qquad (28)$$

For a given V_d, as V_g increases, both I_d and V_{dsat} increase. When V_{dsat} increases the lateral field $E_{lateral}$ decreases, causing a reduction α. Therefore, we have two conflicting factors I_d and α. The initial increase of I_{sb} is caused by

the increase of drain current with V_g, and at larger V_g the decrease of I_{sb} is due to the decrease of the ionization coefficient α.

Figure 42 shows that the maximum I_{sb} is at V_g=2.2 Volts and Figure 43 shows the IdVd and subthreshold curves which have been measured before the device is submitted to the aging process. These two measurements could indicate any problem with the device design or the process integrity. The subthreshold measurement is specifically an indication of long-channel behavior of submicron devices, i.e., for long channel devices, I_d is not a function of V_d in the subthreshold region [65]. Drain voltages from 5.5 to 7.5 volts, V_g=2.2 volts, and V_{bulk}=V_{source}=0 were applied to the four MOSFET terminals to measure the hot-carrier (electron) degradation as a function of time. An automated aging system [64] was used to measure the degradation of device parameters such as threshold, transconductance, saturation region currents (V_d=V_g=5.0 volts), and linear region currents (V_d=50 mV and V_g at a certain current level 5 uA/uM width) in both forward and reverse direction every 2^{t-2} mins where t is 2, 3, 4, etc. A lifetime criteria of a 10-percent degradation in threshold or saturation current at V_d=V_g=5.0 volts over 10 years of device operation has been used in industry. In this study, the threshold voltage shift has been used as a monitor to study the effect of detrapping as a function of temperature. Figure 44 shows

device T32 before aging and after 2800 mins of aging where the threshold degraded by 600 mV and the forward and reverse current by 16 and 19.55 percent respectively (stress conditions: V_d=6.5 and V_g=2.5 volts). Once an electron is captured by a trapping site, it can be detrapped by photon, field emission (tunneling) and thermal processes. Figure 44 shows device T32 after 120 mins at 110 C and 15 mins at 150 C where the saturation current and threshold voltage are returning close to their pre-aging values.

The drain current DLTS system was used to determine the defect levels and their concentrations. Figure 45 shows the current DLTS results for device T34 after it was aged for 2800 min at V_d=6.5 and V_g=2.5 volts. A pulse was applied at gate (V_g= 0 -0.9 - 0 volts) and the D.C. drain voltage was V_d=2.5 volts. A DLTS rate window of t_1/t_2 = 10/40 mS was used, a peak at 123 C was detected on all ten different devices with submicron gate length which were measured for this study. However, DLTS signals were weak for the second scan at t_1/t_2= 20/80 mS due to the detrapping of captured electrons at T=140 C. Figures 46a-c show the hot electron detrapping as a function of time at temperatures of 25, 70, and 150 C. Form these data an energy level E_c-E_t=1.1 eV was estimated for electron detrapping (Figure 46d).

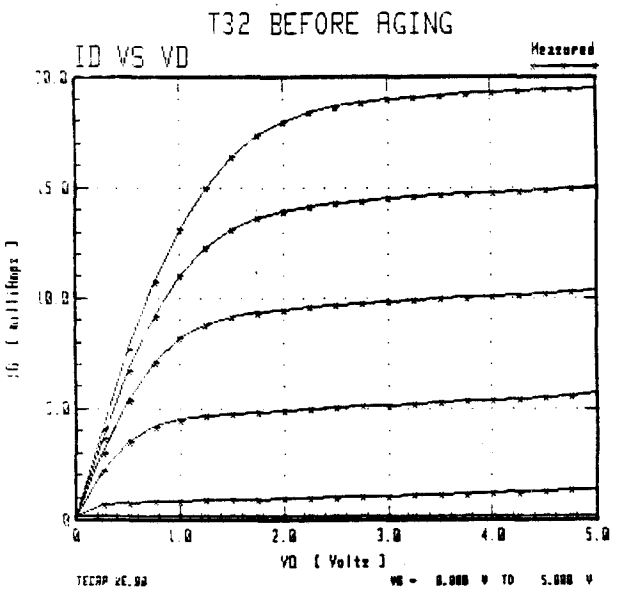


Figure 43a) TECAP measurement of transistor family curves. I_d as a function of V_d for V_g=0 to V_g=5.0 volts for device T32 with channel length of .75 micron.

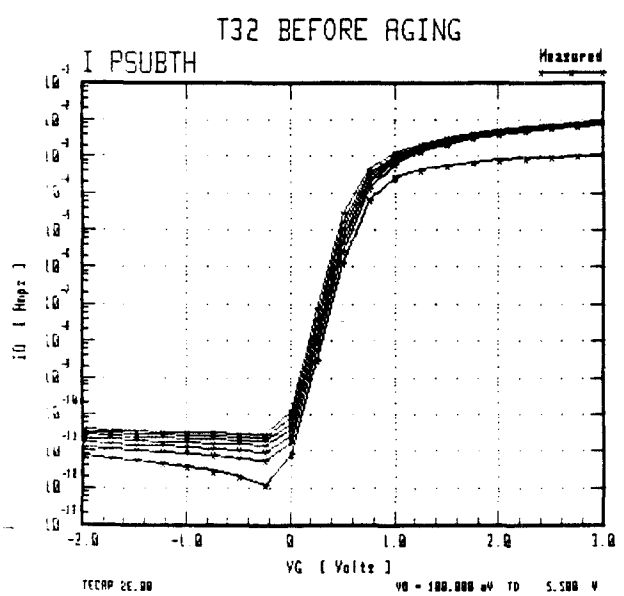


Figure 43b) TECAP measurement of subthreshold behavior of Device T32.

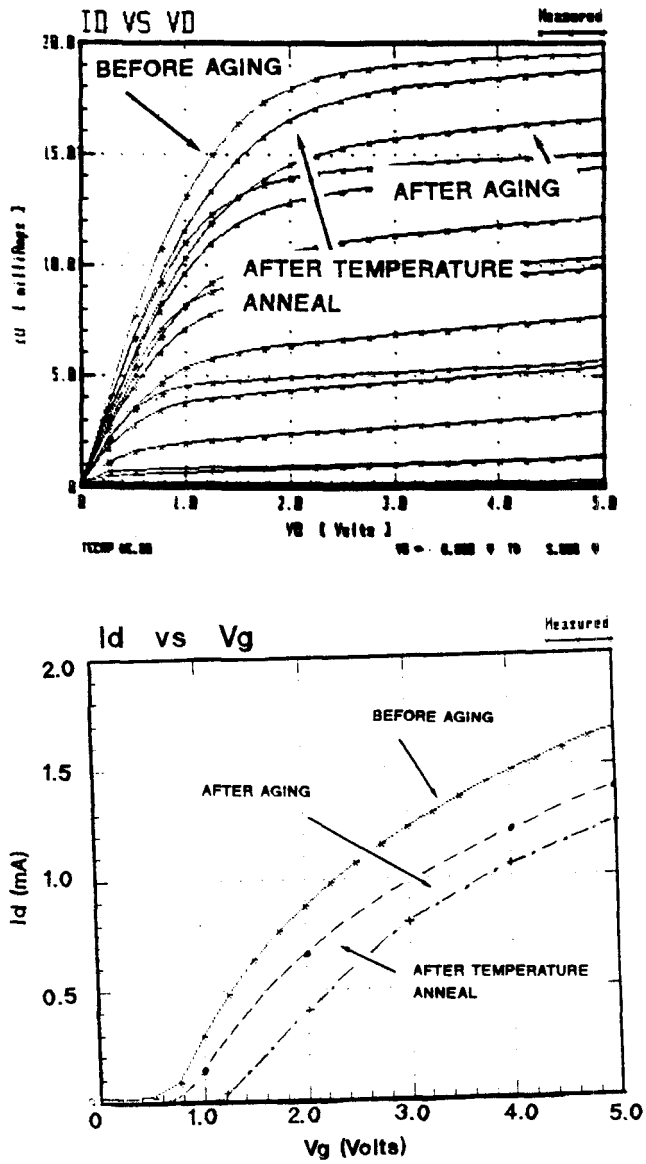


Figure 44) I_dV_d and I_dV_g curves for device T32. Before aging and after 2800 min of stress at V_d=6.5 and V_g=2.5 and also after temperature annealing at 110 C for 120 mins and at 150 C for 15 mins.

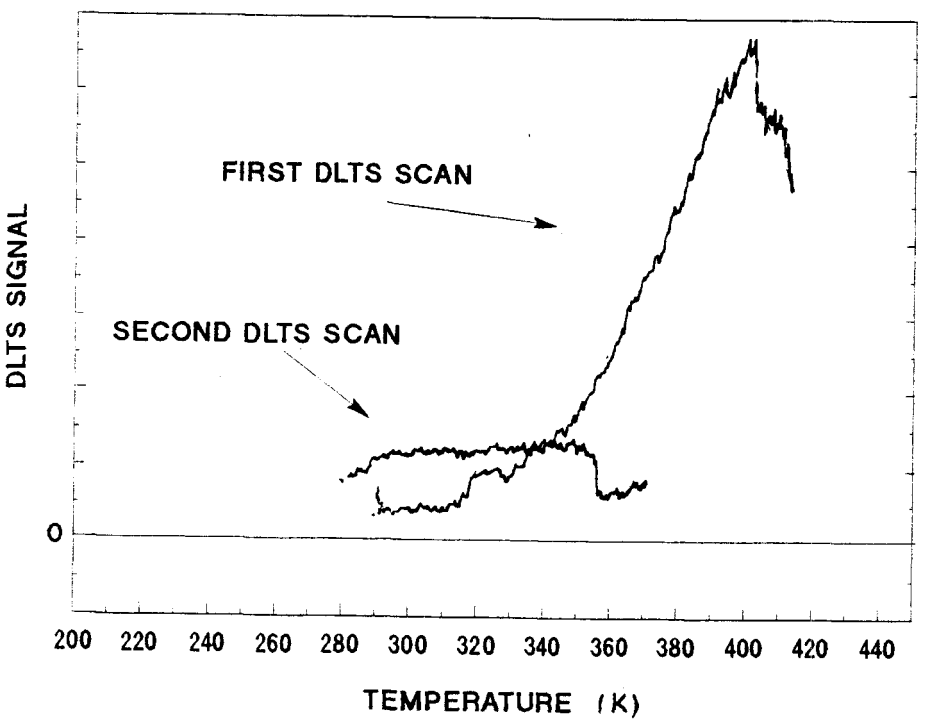


Figure 45) Drain current DLTS results of device T34. After the first DLTS scan,trapping centers are annealed which results in a weak second DLTS scan.

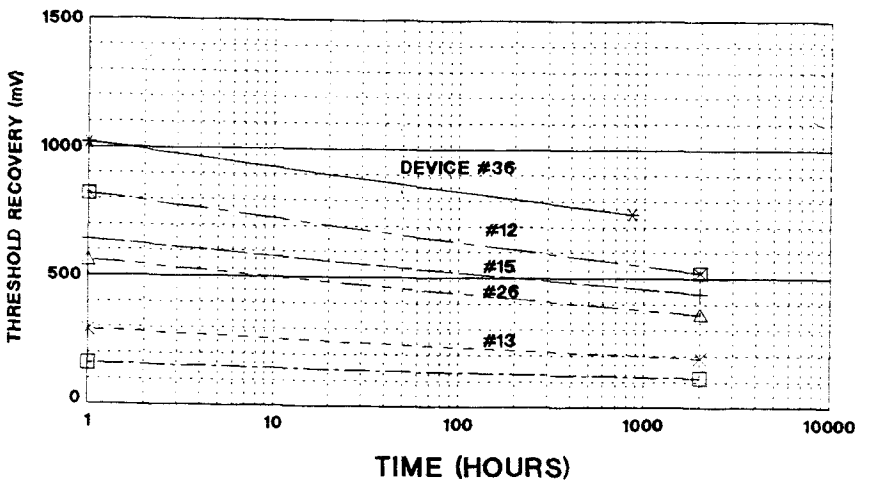


Figure 46a) Hot electron detrapping as a function of time at 25 C.

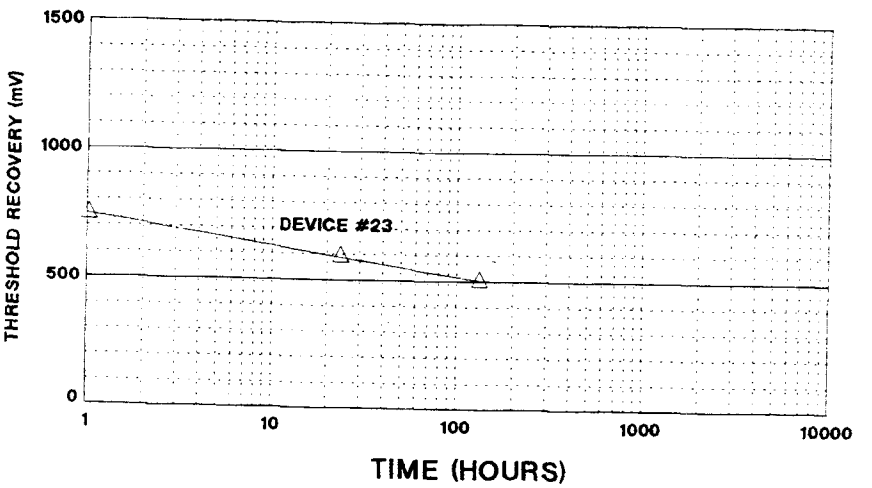


Figure 46b) Hot electron detrapping as a function of time at 70 C.

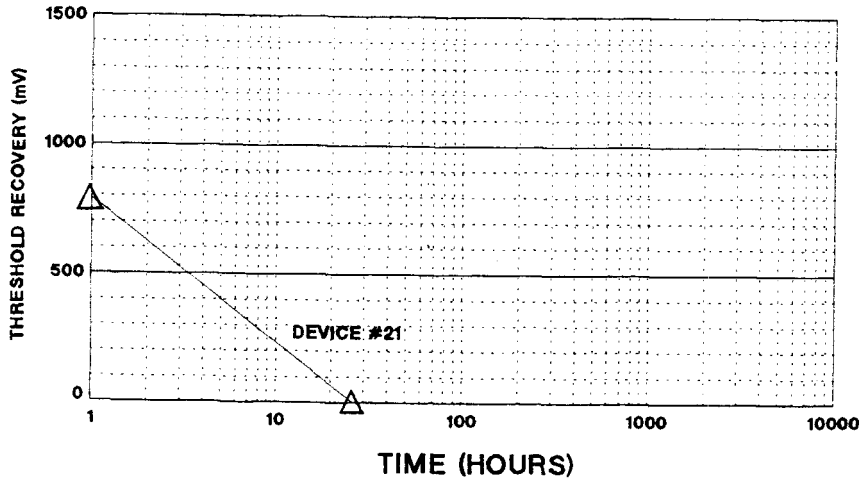


Figure 46c) Hot electron detrapping as a function of time at 150 C.

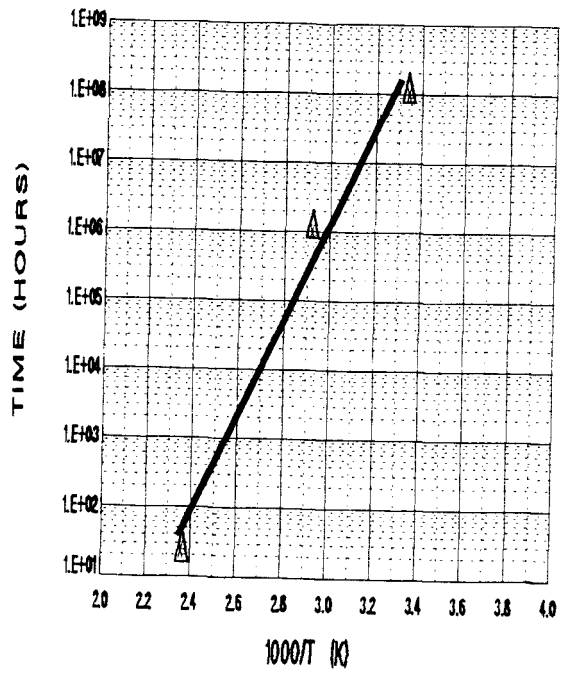


Figure 46d) Arrhenius plot of hot electron re-emission

5.2 HOT HOLE AGING PROCEDURE AND RESULTS

Fair 's model [44] predicted that holes are injected at drain ends of a device. The hole injection process is the first step of device degradation. Figure 47 shows the threshold shift for devices T39, T38, and T15. The initial negative shift in threshold indicates the hole injection into $Si-SiO_2$ interface or oxide. Device T39 with V_g=.9 has a threshold shift of about (-15 mV) after 100 mins due to hot hole injection. To study the detrapping process, several devices were aged at V_g=.7 and V_d=7.0 volts to maximize the hole injection. We stopped the aging process after 100 mins to minimize any electron injection. The detrapping has an extremely slow time constant at room temperature and data at higher temperature were not very consistent. In this case no defect level could be calculated from the data.

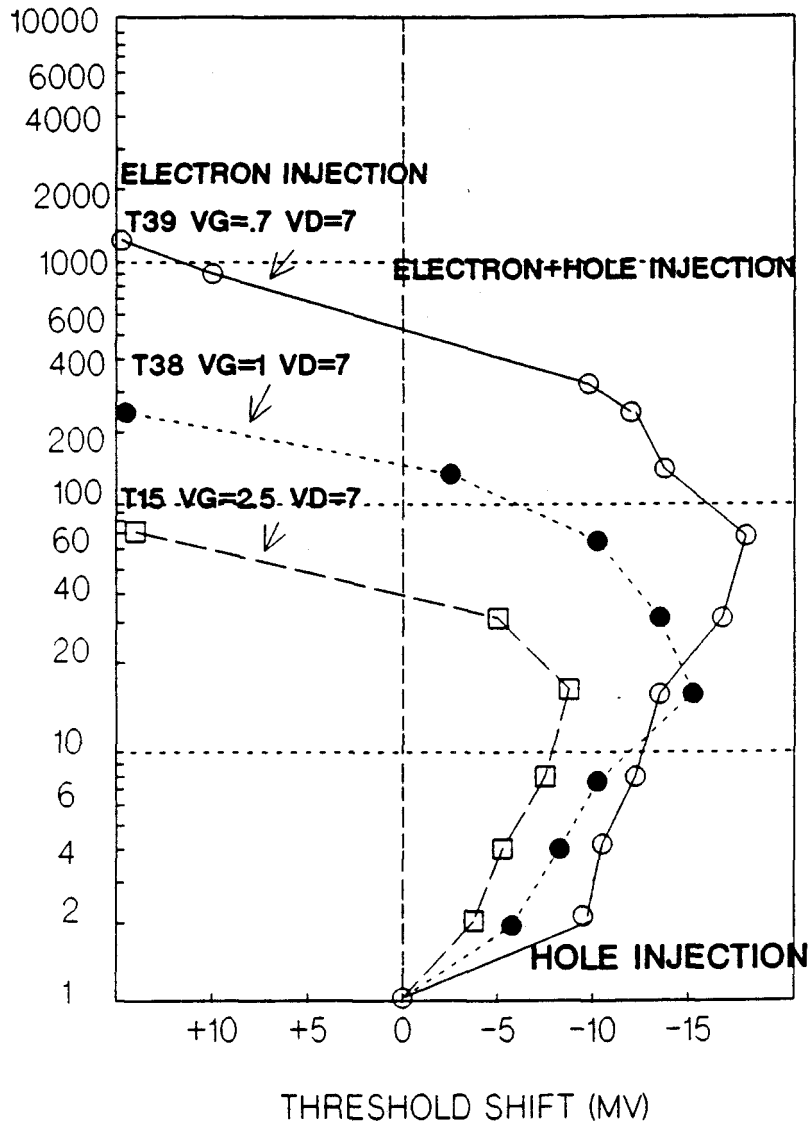


Figure 47) Hole injection process for devices T15, T38, and T39

5.3 CARBON EFFECTS ON Si-SiO_2 INTERFACE

DLTS and photocapacitance characterization of microdefects and stacking faults (Table 2) have revealed that electrically active defects become inactive in the presence of carbon impurities. Carbon was implanted at 15 Kev with 1E16 to 1E20/ cm^3 at Si-SiO_2 interface and also was incorporated during growth of a silicon ingot at 2.4 PPMA or 1.2E17/cm^3 [75]. The effect of carbon implantation on hot carrier trapping was studied. Figure 48 shows that the hot carrier degradation becomes more noticeable as the gate length decreases below 2 micrometer (threshold shift of about 2 mV at Vd=7.0 and Vg=2.5 volts for 24 hours) and becomes severe at gate lengths of one micrometers and below (1000 mV for gate length of .6 micron). Most of processes under development in the IC industry are about half a micron or below and are scheduled for release to production between now and year 2000. To overcome the hot carrier problem, one way is to reduce the power supply from the standard 5.0 volts, however this could lead to a circuit compatibility problem. Based on silicon our material characterization results, we have taken a new approach to silicon technology by introducing a carbon implant to harden the silicon interface with SiO_2. Figure 49 shows the threshold degradation versus aging time results of devices with carbon and control devices with carbon below detection limit of FTIR (1E15/cm3). Carbon atoms might form a very thin layer of SiC at the

silicon surface and reduces the Si-Si spacing to match the Si-O spacing and reduce the interface states. This in turn, leaves an $Si-SiO_2$ interface which is less susceptible to hot carriers degradation.

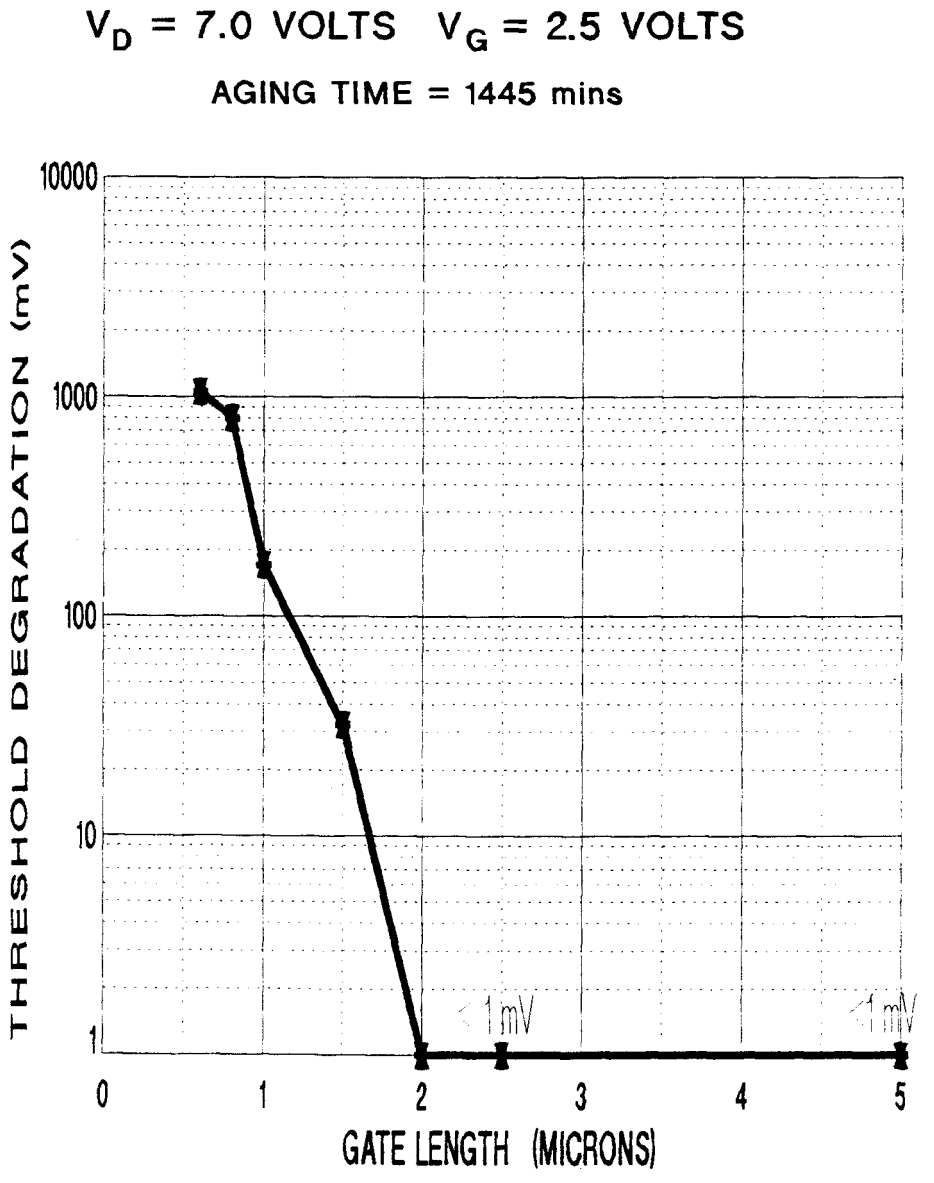


Figure 48) Threshold degradation versus gate length for devices from 5 micron to .6 micron [75].

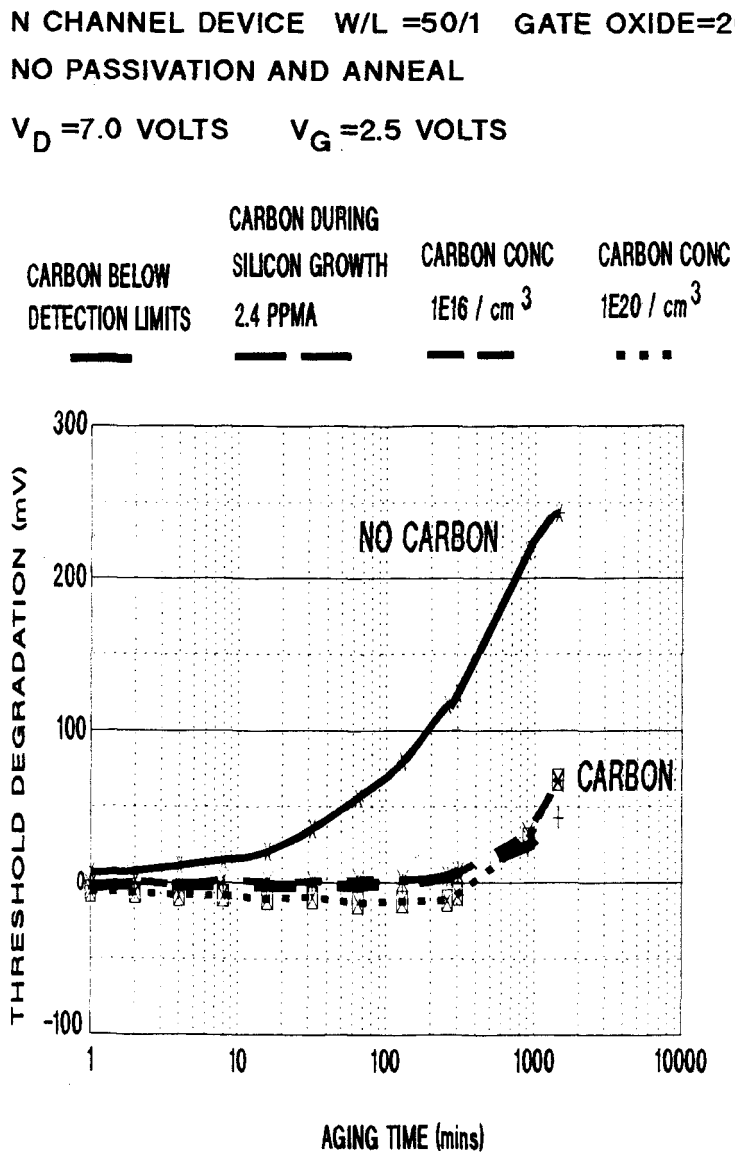


Figure 49) Threshold degradation versus aging time for device with carbon implanted or incorporated during silicon growth and control device [75].

6. A MODEL FOR THE EFFECT OF CARBON ON OXYGEN INDUCED STACKING FAULTS AND Si-SiO_2 INTERFACE TRAPS

Results of previous two chapters indicate that carbon can lower the electrical activity of oxygen induced precipitates and also can eliminate or decrease the interface trapped charges at Si-SiO_2. A model is presented for the effect carbon on the electrical activity of interface states between Silicon and SiO_x in general terms. It is called **"the carbon model"** . Stacking fault electrical activity and MOS device Si-SiO_2 interface defects can be explained in terms of this model.

Figure 50 shows the basic traps and charges associated with Si-SiO_2 [76].

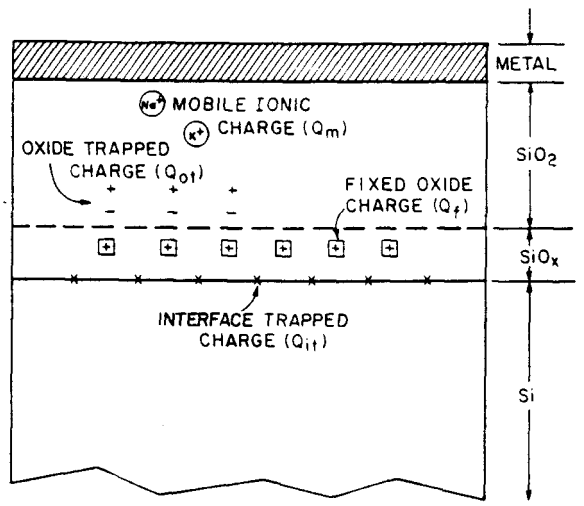


Figure 50) Interface charges associate with the Si-SiO_2 after Deal [76]

In order to develop "the carbon model", $Si-SiO_2$ and Si/OP (silicon and oxygen induced precipitate) interfaces have to be analyzed. In both systems, we have experimental results on the effects of the carbon impurity on the electrical activity of defects. At $Si-SiO_2$ interface carbon lowers hot carrier degradation and at stacking faults (Si/OP) carbon eliminates the electrical active centers. Therefore, the questions to be asked about the carbon are the following

1. What is the common factor between the Si-SiO2 interface and silicon/stacking fault interface?
2. How does carbon cause the elimination of electrically active centers?

We will try to propose an answer to the first question which is then the key to answering the second.

1. Interface trapped charges (Q_{it}) at silicon and silicon dioxide

These trapped charges are our main concern the at $Si-SiO_2$ interface in order to develop the "the carbon model". Interface trapped charges can be positive or negative and are due to structural defects mainly crystalline mismatch between the $c-Si/a-SiO_2$. Pantelides [77] has shown that the dangling bonds at $Si-SiO_2$ interface are due to lattice mismatch between silicon and silicon dioxide. Recent data from Ourmazd et al [78] show that the mismatch could be as high as 13.2 percent between the crystalline silicon (a=5.43) and SiO_2 with

a hexagonal structure (a=5.046 c=8.23). Based on Ourmazd's model the silicon oxidation is accompanied by a silicon diamond cubic transition to hexagonal SiO_2 crystalline and finally an amorphous SiO_2 layer. Laughlin et al [79] have developed a mathematical model for the Si-SiO_2 interface and established the following results:

1. If the interface is ideal (no broken or distorted bonds), then there would be no interface states in or near the silicon.
2. Bond-angle disorder in the oxide tends to generate a tail of states near the silicon conduction band edge, but not near the valence band edge.
3. The only bonding defect which causes a sharp state deep in the silicon gap is a dangling Si bond on the silicon side of the interface.
4. Both dangling silicon bonds and silicon-silicon bonds in the oxide can induce trap states near the conduction and valence band edges.

Electron paramagnetic resonance studies by Poindexter et al [80-81] suggest the presence of trivalent Si (P_{bo} centers) at the interface, that is, Si bonded to three Si atoms with the fourth one a dangling bond. The density of of the centers is strongly correlated with midgap Q_{it} states. Quasi-static CV and DLTS have been extensively used to characterize the interface trapped charges on MOS capacitors [82-85] and a

U-shaped continuum of interface states in the silicon forbidden energy band is obtained (Figure 51). Interface trapped charges which have energy positions within the band gap of the silicon substrate are able to affect devices in the same manner as the bulk traps. Several discrete levels have been associated with the $Si-SiO_2$ interface, E_c-.49 ev(σ_n =2.9X10^{-16} cm^2) [86-87], Ec-.50 ev [88], Ec-.40 [82], Ev+.30 [89].

In contrast to the interface trapped charges the **fixed and mobile charge centers** are located in the oxide and are not in communication with the silicon bulk except after they are injected across the high interface barrier.

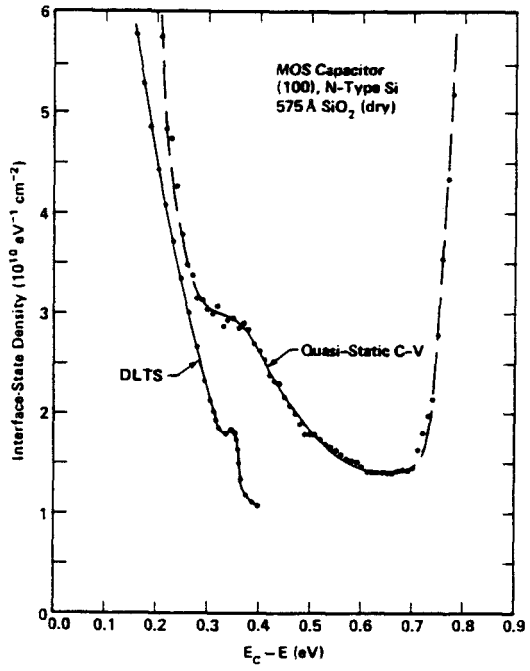


Figure 51) Quasi-static CV and DLTS analysis of MOS capacitor after N.M. Johnson [82]

2. Silicon and stacking fault interface

Schroder et al. [28] have measured the silicon/oxygen induced precipitate (Si/OP) interface states. They have concluded that Si/OP interface states are similar to conventional Si/SiO_2 interface states. There are also major generation-reconbination centers at the Si/OP interface which could cause lifetime degradation. Figure 53 shows Schroder's measurements of the Si/OP interface state density distributions with a localized state at E_c-0.45 eV on two n-type samples.

We can answer the first question on page 99 now. From Schroder [28], Johnson [82], Laughlin [79] and Poindexter [80, 81, 84], it can be concluded that silicon/oxygen precipitates and silicon/ silicon dioxide interfaces are similar with their U-shaped distribution of interface states density and the localized states due to dangling bonds which are called P_b centers.

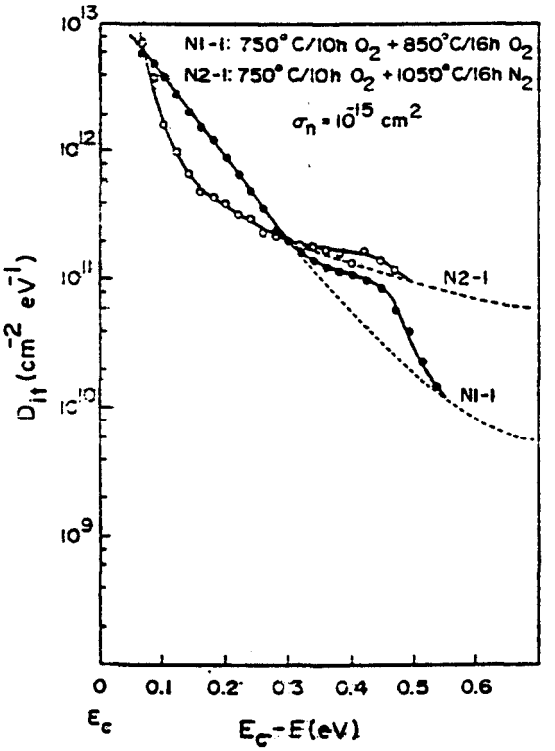


Figure 52) Density distribution of Interface states between silicon and oxygen induced precipitates for two n-type sample after Schroder [28]

CARBON MODEL

Table 2 summarized our DLTS characterization of oxygen induced microprecipitates and stacking faults. The presence of carbon affected the electrical activity of stacking faults, and implantation of carbon into the interface of $Si-SiO_2$ reduced the hot electron aging degradation [75] (figure 49). Whenever a silicon wafer contains oxygen impurities, the stacking faults induced are always associated with precipitates [3]. Our results show that these stacking faults are electrically active [68,70]; however the number is reduced by the presence of carbon.

Based on our DLTS and photocapacitance characterizations results with wafers containing a trace of carbon, we conclude that the electrical activity of stacking faults is due to the presence of oxygen precipitates. According to Weigal [30] stacking faults without precipitates cause only a very minor charge redistribution.

DLTS characterization of Omling's silicon deformation results [27], our mechanical damaging experiments (Figure 39), and electrically active stacking faults all showed a very similar DLTS peaks. Omling indicated that this DLTS peak

could be related to dangling bonds. At the $Si-SiO_2$ interface P_b centers (dangling bonds) which are related to trivalent silicon have been detected [80-81].

Carbon can be gettered to damaged sites such as dislocations, stacking faults and wafer surfaces [18]. Carbon might form a layer of SiC at the Si/OP and $Si-SiO_2$ interfaces which lowers the stress according to Hahn [17]. Even at low (.1 PPMA) concentrations, there is sufficient carbon to saturate the interfacial sites at the Si/OP interface [90]. Carbon incorporation in the silicon-oxide interface states can also serve to reduce the density of interface states and hot carrier trapping sites. The electrical activity and trapping is reduced either by a lower density of interface states as a result of a better lattice match at the $Si-SiO_2$ and the Si/OP interface or stronger bond strengths at the interface.

7. CONCLUSIONS AND FUTURE WORK

It has been shown that oxygen induced microdefects and stacking fault are electrically active when the carbon concentration is below detection limits of FTIR. A correlation between stacking fault size and density with DLTS was established. A single dominant energy level at E_c-E_t=.48 +/- .1 eV was detected with DLTS. Photocapacitance measurements showed a clear correlation with DLTS signals on electrically active wafers.

MOSFET devices were stressed and subsequently were annealed at different temperatures. An energy level was estimated for electron thermal detrapping process at E_c-E_t= 1.1 +/- .1 eV.

Carbon doping or ion implantation at Si-SiO_2 lowered aging process of MOSFET devices. Carbon atoms might form a very thin layer of SiC at Si-SiO_2 interface and reduce the lattice mismatch between thermal oxide and silicon to reduce the carrier trapping sites.

Electrical activity of oxygen induced stacking faults and microdefects is associated with oxide precipitate and silicon interface in these microdefects. Carbon incorporation in

these microdefects is similar to the effect of carbon on surface oxide-silicon interface. The presence of carbon reduced the electrical activity of oxygen induced defects.

Future work should focus on understanding of mechanisms of carbon incorporation at Si-SiO_2 and Si/OP interfaces and determine whether interface reduction is due to reducing the trap sites or formation of a thin SiC. It would also be an important step forward to optimize the carbon ion implantation dose, energy and any required temperature annealing to harden the silicon-oxide interface.

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