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Solid-state based lighting offers a number of advantages such as long life, high efficiency and compactness compared to a conventional halogen tube based lighting. Due to these advantages they are being increasingly used in a variety of lighting applications including portable devices, home, and automotive lighting. Consequently, there has been a slew of LED drivers catering to a variety of applications.

This thesis presents design techniques to improve the efficiency of high current LED drivers used in portable applications.The proposed LED driver achieves current regulation without using a series current-regulation-element. A novel, error averaged, sense-FET based current sensing technique is employed to improve the sensed current accuracy. Highly accurate and lossless current sensors and a current estimator, implemented on-chip, obviate the need for the current regulation element thereby greatly improving the converter efficiency and reducing the product cost. To maximize the efficiency and to drive the desired current over the entire battery range of a Li-Ion battery (3-5.5V), the converter operates in three different operating modes namely buck, buck-boost and boost modes. Fabricated in a 0.5μm CMOS process, the converter achieves an efficiency improvement of

over 13% compared to current-regulation-element based LED drivers. Measured LED current accuracy is better than 2.8% over the entire range of the battery and the standard deviation measured across 7 devices is less than 1.6%.

Design Techniques for High Efficiency High Current LED Drivers

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I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Sachin B Rao, Author

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CHAPTER 1. INTRODUCTION

Solid-state lighting has emerged as an attractive alternative to halogen tube lighting over the past decade. Improvements in solid-state lighting device technology have made light emitting diodes (LEDs) more efficient, compact, and long-lasting compared to their halogen tube counterparts. As a result, they are being increasingly used in a variety of lighting applications including portable devices, displays, automotive, and home lighting. Owing to the high efficiency and compactness properties, LED-based lighting is especially amenable to battery operated portable devices, such as cell phones where extending the battery life and reducing the board real-estate is of utmost importance. Consequently, over the last few years, there has been a slew of high current LED driver products catering to a variety of lighting applications [1]-[5].

LED driver differs from a conventional DC-DC voltage regulator in that its output quantity is a fixed current rather than a fixed voltage. To understand this, consider the luminous flux and forward voltage characteristics of a Flash-LED shown in Fig. 1.1 [6]. Figure 1.1(a) indicates that the LED brightness is controlled by its forward current while, Fig. 1.1(b) shows that the forward current is highly sensitive to the forward voltage. Because the voltage-to-current characteristics of the LED are sensitive to PVT variations, controlling the light output by regulating the forward voltage is impractical. In view of this, all the LED drivers regulate

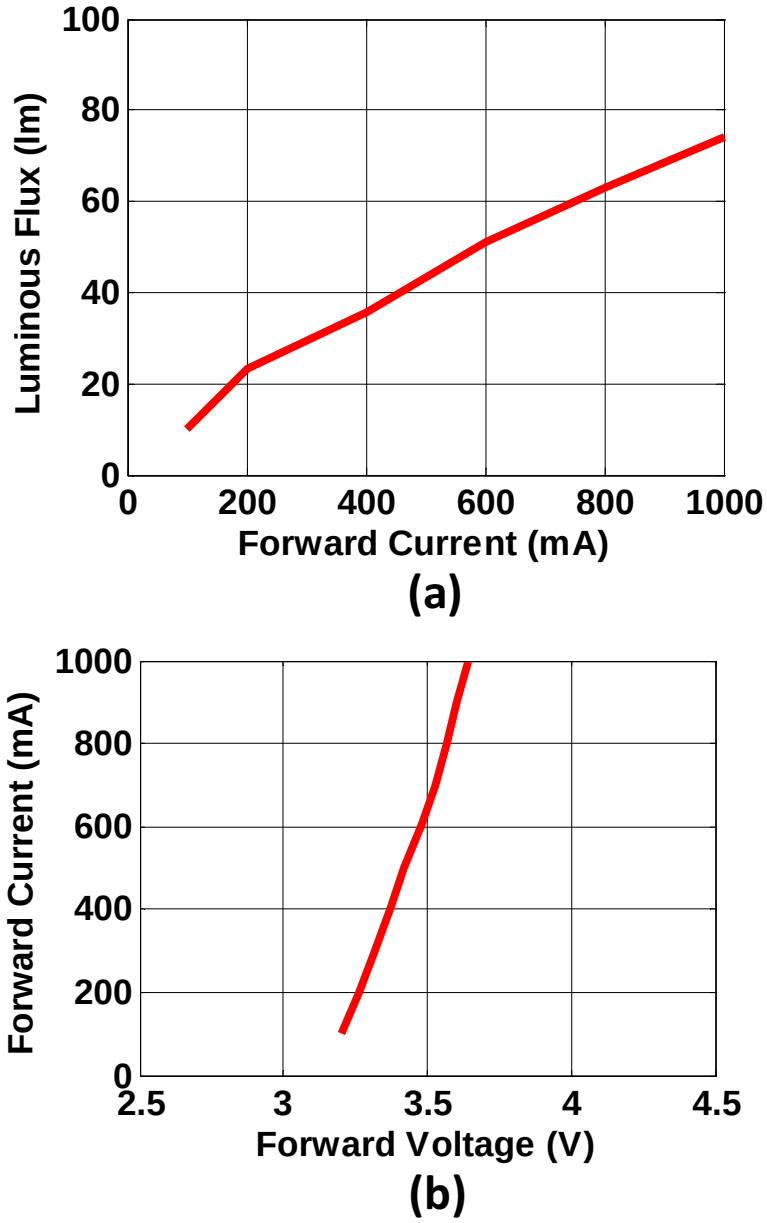

Figure 1.1: Typical Flash LED characteristics: (a) Luminous flux versus forward current. (b) Forward current versus forward voltage.

the light output by forcing a known current through the LED [7]. Simplified block diagrams of two such LED drivers are shown in Fig. 1.2 wherein a current-regulation-element (CRE) is used in series with the LED [1]-[5]. In the architecture

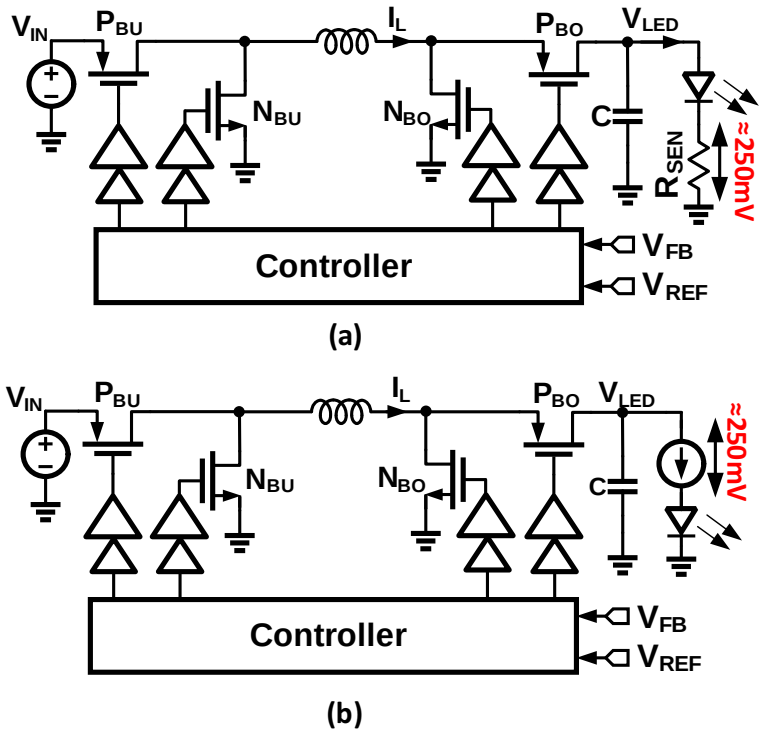

Figure 1.2: Conventional buck-boost LED drivers using: (a) Sense resistor based CRE. (b) Current source based CRE.

depicted in Fig. 1.2(a), the sense resistor, R_{SEN}, acts as the CRE and the average LED current, I_{LED}, is regulated indirectly to the desired value by regulating the voltage across R_{SEN}. To minimize the LED current inaccuracy caused by resistor variation and voltage-sense circuitry offsets, an accurate external sense resistor and large drop out voltage in the order of 250mV is used, respectively. Alternatively in the architecture shown in Fig. 1.2(b), a series current source forces the desired current through the LED. The current source is implemented using a MOSFET and the feedback loop regulates the voltage across the current source to about 250mV and biases it in saturation region.

Though CRE offers a convenient way to regulate the LED current, it incurs

hefty power and area penalty. The voltage drop across the CRE results in a significant power loss. For example, a 1A current through the LED causes a power loss of about 250mW across the CRE and degrades the efficiency by 5%-10%. Furthermore, an on-chip implementation of the current source takes significant silicon area and increases the product cost. On the other hand, a sense resistor based CRE, in addition to causing the efficiency loss as described above, also requires an expensive accurate external sense resistor. Though the power loss in the CRE can be reduced to some extent by minimizing the voltage drop across it, accurately controlling the output current with the reduced voltage across the CRE becomes difficult.

In view of these drawbacks, we seek to completely eliminate the CRE. To this end, a novel on-chip current sensor and a current estimator block are developed to accurately sense I_{LED} without using a CRE. The proposed CRE-less LED driver is both power and cost efficient. We demonstrate the validity of the proposed techniques by employing them in a high current buck-boost Flash LED driver that operates over the entire range of the Li-Ion battery (3V-5.5V).

This thesis is organized as follows. Chapter 2 discusses the proposed architecture and design details of highly accurate current sensors. The control loop, different modes of operation of the converter and the design details of the LED current estimator are discussed in Chapter 3. Chapter 4 deals with the circuit design of important blocks in the LED driver. Chapter 5 discusses the measured results obtained from the prototype chip. Conclusions are drawn in Chapter 6.

CHAPTER 2. PROPOSED ARCHITECTURE

Figure 2.1 depicts simplified block diagram of the proposed LED driver [8]. The CRE is completely eliminated and the converter directly drives the desired current through the LED. At the heart of this architecture are two current sensors, denoted as IP-sensor and IN-sensor, and a LED current estimator block. IP and IN-sensors measure the current through the powerFETs denoted as P_{BU} and N_{BU}, respectively. The sensor outputs, IP and IN, are processed by the current estimator block to accurately sense I_{LED} in the form of voltage $\overline{V_{SENSE}}$. The controller, along with the G_M-C integrator and duty-cycle generator, forms a negative feedback loop which, in steady state, forces $\overline{V_{SENSE}}$ to be equal to the reference voltage, V_{REF}. V_{REF} therefore represents the desired value of I_{LED}. Due to the absence of CRE and lossless current sensing, this architecture minimizes conduction loss and achieves significant improvement in the overall efficiency of the converter. Since this architecture eliminates the need for an explicit on-chip current source and any additional external components, it incurs minimal area and cost penalty.

2.1 Current Sensor Design Issues

The accuracy of the sensed current is paramount as it directly determines the LED current accuracy. Furthermore, to maximize the efficiency improvement offered by the CRE-less LED driver and reduce the system cost, high accuracy current sensing must be performed in a lossless manner without using expensive external components. A number of techniques exist to sense current in DC-DC

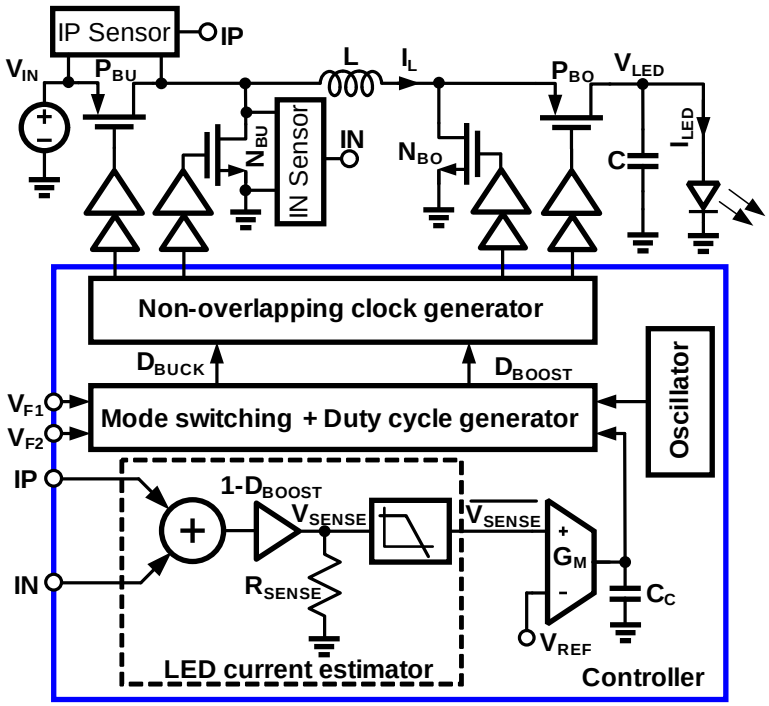

Figure 2.1: Block diagram of the proposed CRE-less LED-driver.

converters [9]-[15]. A brief review of these current sensing techniques reveals that the filter based [9], [10] and senseFET based current sensing [14] techniques are most amenable for fully-integrated implementations [15]. However, as elucidated later, they both suffer from the accuracy versus power loss tradeoff.

The filter based approach relies on the fact that the voltage across the capacitor in a series R-C network is proportional to the current through the inductor in a series L-R network if both the networks have identical time constants [9]. Though this technique is lossless, the sensed current accuracy is highly sensitive to PVT variations of the filter coefficients. Calibration and tuning the filter coefficients can mitigate component variations, but the high-precision analog circuitry complicates the design and incurs power penalty. In practice, the calibration/tuning inaccuracies limit the sensed current accuracy to only about $\pm 8\%$ [10].

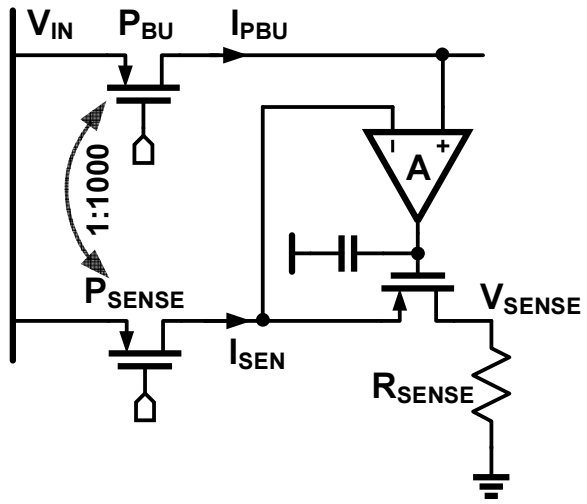

Figure 2.2: Simplified senseFET based current sensing technique.

Contrary to the complicated filter based scheme, the senseFET based approach offers the simplest means to achieve lossless current sensing. Figure 2.2 depicts the simplified senseFET based current sensing technique. The current through the main powerFET, P_{BU}, is sensed using a senseFET, P_{SENSE}. The feedback amplifier forces the terminal voltage across P_{SENSE} to be same as P_{BU}. Thus the current through the senseFET, I_{SEN}, is a fixed fraction of powerFET current, I_{PBU}. Since the powerFET to senseFET ratio is usually very large, in the order of 1000:1, the sensed current is very small and hence the sensing circuitry incurs minimal power loss. Though the simplicity of this technique is appealing, sensed current accuracy across PVT corners is poor and is limited to around 10%-20%.

The two main sources of inaccuracy are the amplifier offset and the mismatch between the powerFET and senseFET. The input referred offset of the amplifier causes the drain-to-source voltage, V_{DS}, across the powerFET and senseFET to be different. Because both these FETs operate in the triode region, V_{DS} mismatch directly appears as error in sensed current. For instance, with a V_{DS} of 100mV,

even a modest input referred offset of 5mV can cause about 5% error in the sensed current. The second source of error is the mismatch between the powerFET and the senseFET. Since the senseFET is much smaller than the powerFET, mismatch between them across PVT corners can be as high as 10-20%, resulting in a sensed current inaccuracy of the same order [10, 16]. Any attempt to improving the matching by using a larger senseFET would also increase the sensed current and degrades the driver efficiency. For example if the senseFET size is increased such that the powerFET to senseFET ratio reduces to 10:1, the efficiency degradation can be as high as 10% since 10% of the powerFET current is not being delivered to the load. Thus, the senseFET based current sensing scheme suffers from a fundamental tradeoff between accuracy and efficiency. In view of this, we propose an error-current averaging technique that decouples this tradeoff. We employ auto-zeroing to mitigate errors due to amplifier offsets.

2.2 Proposed Error-Averaging Architecture

To understand how the accuracy versus power loss tradeoff can be decoupled, we note that the goal is to derive I_{LED} from the sensed powerFET current and regulate it using a negative feedback loop as shown in Fig. 2.3. The powerFETs operate at the switching frequency of the converter that is governed by tolerable switching losses and the inductor size and is typically around 1MHz to 2MHz in portable applications [1]-[3]. However, due to the absence of stringent transient performance requirements in the driver, the bandwidth of the feedback loop that regulates I_{LED} is relatively small and is usually around 10s of kilo-hertz. Consequently, the feedback loop shown in Fig. 2.3 filters out high frequency error in the sensed current and is sensitive only to slow changes in the sensed current.

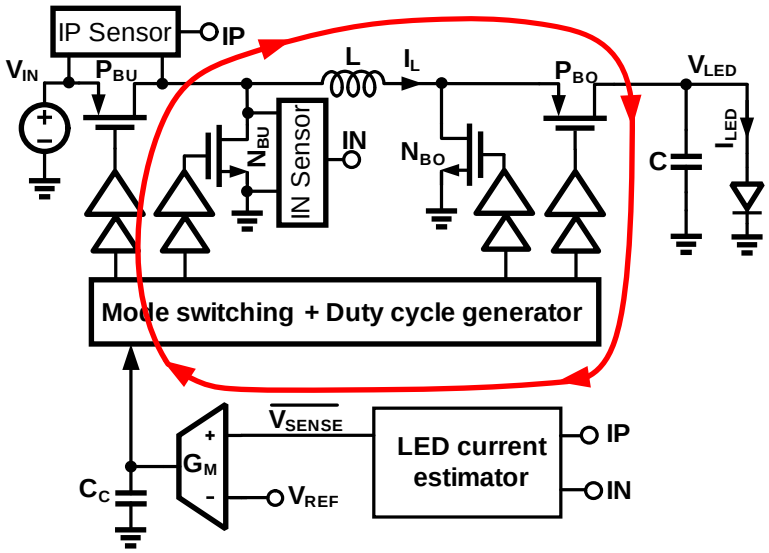

Figure 2.3: Illustration of the regulation loop.

Therefore, the required effective bandwidth of current sensing is much smaller than the switching frequency. This gives an additional degree of freedom in time that can be used to improve the sensed current accuracy without the power penalty.

Figure 2.4 shows the proposed IP-sensor circuit diagram. It consists of two important sections, on the left it has powerFET, P_{BU} and an array of senseFETs, $P_{S1}, P_{S2}, \ldots P_{SN}$ that are used for error-averaging. Offset canceling is performed by IP-stage1 and IP-stage2, shown on the right. Error-averaging is discussed next followed by discussion on offset canceling blocks. SenseFETs $P_{S1}, P_{S2}, \ldots P_{SN}$ are nominally matched to P_{BU}. A one-hot encoded circular shift register selects a different senseFET during each switching cycle and the moving average of the sensed currents over N switching cycles is used as an estimate of P_{BU} current. To quantify the accuracy improvement achieved by averaging, let $I_{S1}, I_{S2} \ldots I_{SN}$, denote the currents sensed by N sense-FETs $P_{S1}, P_{S2} \ldots P_{SN}$, respectively. The

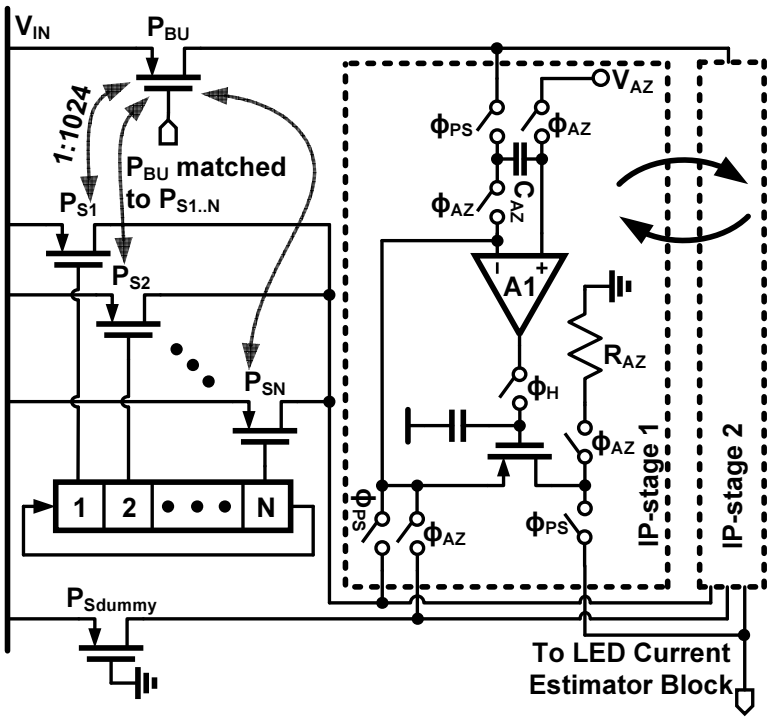

Figure 2.4: Proposed IP-sensor block diagram.

average sensed current, $\overline{\mathrm{I_{SEN}}}$, is given by

$$\overline{\mathrm{I_{SEN}}} = \frac{\mathrm{I_{S1}} + \mathrm{I_{S2}} \cdots + \mathrm{I_{SN}}}{\mathrm{N}}. \tag{2.1}$$

In the presence of random mismatches in the sensed currents, the standard deviation of the average sensed current equals

$$\sigma_{\overline{\mathrm{I_{SEN}}}} = \frac{\sigma_{\mathrm{I_S}}}{\sqrt{\mathrm{N}}} \tag{2.2}$$

where we have assumed that the senseFET mismatches are uncorrelated and have same standard deviation i.e.

$$\sigma_{\mathrm{I_S}} = \sigma_{\mathrm{I_{S1}}} = \sigma_{\mathrm{I_{S2}}} \cdots = \sigma_{\mathrm{I_{SN}}} \tag{2.3}$$

Thus, ideally, error-averaging over N senseFETs improves the sensed current accuracy by $\sqrt{\mathrm{N}}$ times. In practice, however, the improvement in sensed current

accuracy is some what limited by the correlation between the error sources. Nevertheless, the proposed technique is very effective in reducing the effect of random mismatches. Because only one senseFET is enabled at any time, this approach incurs no extra power penalty, thereby breaking the fundamental tradeoff between accuracy and efficiency in a conventional senseFET based approach. In our implementation, a total of 32 senseFETs, each 1024 times smaller than the powerFET, are used.

Though a larger number of senseFETs would reduce the mismatch to a greater extent, we limited the number of senseFET to 32. This choice is mainly governed by two practical considerations. First, increasing the number of senseFETs further would increase the circuit complexity in terms of layout and parasitics. Second, increasing the number of senseFETs would increase the area. Since N=32 can ideally reduce the random mismatch-induced error by more than 5 times, it was chosen as a good compromise between complexity, area, and performance. To minimize the effect of temperature gradients in the large powerFET and to improve matching, the senseFETs are spread out across the powerFET in the layout. Good layout techniques are employed to reduce systematic errors due to routing metal parasitics.

The problem of inaccuracy in the sensed current due to amplifier input referred offset is minimized with auto-zeroing [17]. In general, auto-zeroing stage operates in two phases namely offset-sampling phase, Φ_{AZ}, and offset-canceling phase, Φ_{PS}. During Φ_{AZ} the amplifier is connected in a unity feedback configuration and the offset of the amplifier is sampled on capacitor, C_{AZ}. During Φ_{PS}, C_{AZ} is connected in series such that the stored offset voltage on the capacitor cancels the input referred offset.

Offset cancellation in the IP-sensor can be implemented by sampling the

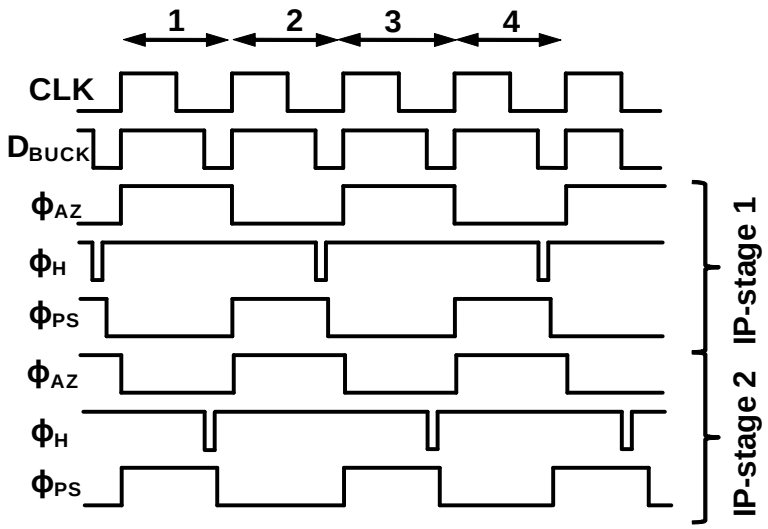

Figure 2.5: Timing diagram of different phases in IP-sensor.

offset during the time when P_{BU} is OFF and N_{BU} is ON. However at high duty-cycle, P_{BU} is OFF only for a very small fraction of the switching cycle. This puts stringent settling requirement on the offset sampling phase. For example, when the duty-cyce is 90%, assuming 2MHz switching frequency, the available time for Φ_{AZ} is only 50ns. In order to relax the speed requirements, two identical stages named IP-stage1 and IP-stage2, operate in a ping-pong fashion to sense the P_{BU} current [18]. Figure 2.5 shows the associated timing diagram for the IP-stage. During every switching cycle, P_{BU} turns ON when D_{BUCK} goes high and the IP-sensor starts sensing the P_{BU} current. During the odd clock period, IP-stage1 is auto-zeroed and IP-stage2 senses the current. During the even switching period, their roles reverse and IP-stage2 is auto-zeroed while IP-stage1 senses the current. An additional phase, Φ_H, which holds the value of sensed current, is asserted during the dead-time. As explained later in chapter 3, Φ_H minimizes the sensing error introduced during the non-overlapping time.

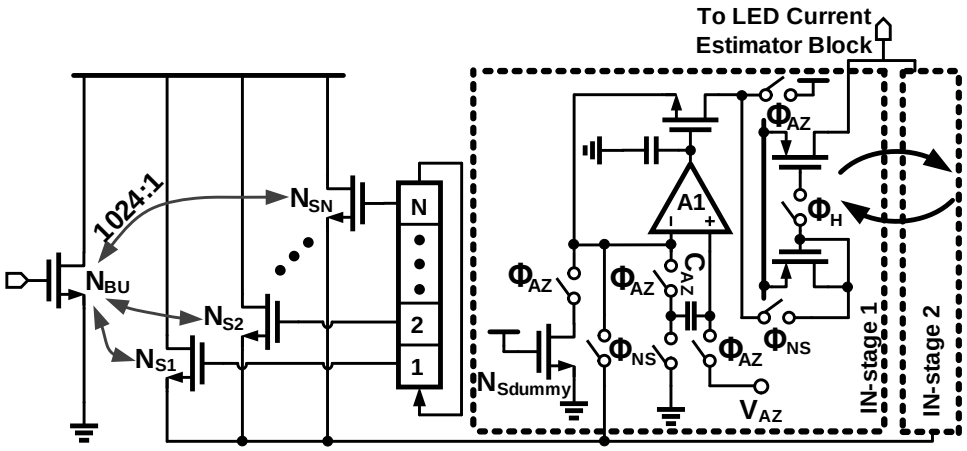

Figure 2.6: Proposed IN-sensor block diagram.

A simplified schematic of IN-sensor to sense the current through N_{BU} is shown in Fig. 2.6. Error-averaging and auto-zeroing techniques, similar to the ones employed in IP-sensor, are used to improve the accuracy of the sensed current. IN-sensor is complimentary to the IP-sensor except that the connection of the senseFETs, $N_{S1}, N_{S2}, \ldots N_{SN}$ is different from that of the $P_{S1}, P_{S2}, \ldots P_{SN}$. In the IP-sensor, all the senseFETs share the source connection with the source of P_{BU} and the amplifier forces the drain voltage of the senseFET to be same as that of the drain of the powerFET. However in the IN-sensor, all the senseFETs share the drain connection with the drain of N_{BU} and the amplifier forces the source voltages of senseFET and powerFET to be identical. This difference arises because when N_{BU} is turned ON the inductor current flows from source to drain, causing N_{BU} drain voltage to go below ground. If the senseFET connections were identical to that of the IP-sensor, the sensing circuitry would have to draw current from the drain of $N_{S1}, N_{S2}, \ldots N_{SN}$. This would need a negative supply voltage, which would complicate the IN-sensor design. The number of senseFETs and the ratio of powerFET to senseFET remains the same as the IP-sensor.

CHAPTER 3. OPERATING MODES AND CURRENT ESTIMATION

3.1 Converter Operating Modes

Depending on the desired I_{LED}, the forward voltage across a flash-LED can range from 3V-3.8V while the input battery voltage may vary from 3 to 5.5V. Since the desired V_{LED} lies within the range of the input battery voltage, a simple buck converter or a boost converter would be impractical as they can only produce an output voltage either lower than or higher than the input voltage, respectively. Therefore in our implementation, for seamless operation over the entire range of V_{IN}, the converter operates in 3 different modes depending on the relative magnitudes of the battery voltage, V_{IN}, and the desired V_{LED} as depicted in Fig. 3.1. This is referred to as tri-mode operation. Compared to a conventional uni-mode buck-boost converter, the tri-mode operation greatly improves the efficiency, mainly by reducing the conduction losses at high current [20], [21].

If V_{IN} is much greater than the desired V_{LED}, the converter operates in the buck mode by configuring the powerFETs as shown in Fig. 3.2(a). In this mode, the boost-side powerFET, P_{BO}, is always ON ($D_{BOOST} = 1$) and the inductor is connected to the output capacitor. The buck-side powerFETs operate with a duty-cycle, D_{BUCK}, generated by the feedback controller. The voltage and current

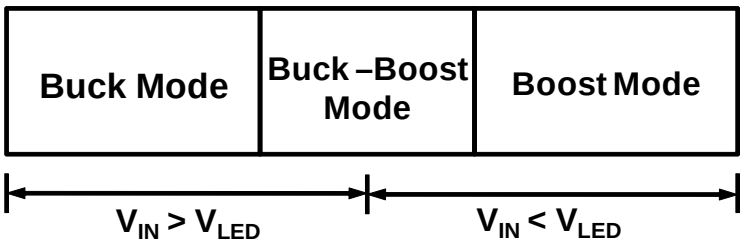

Figure 3.1: Operating modes of a tri-mode buck-boost converter.

equations in this mode are given by,

$$V_{LED} \approx (V_{IN})(D_{BUCK}) \tag{3.1}$$

and

$$I_{LED} = \overline{I_L} \tag{3.2}$$

where $\overline{I_L}$ denotes the average inductor current. Note that Eq. 3.1 represents only an approximate value of V_{LED} as the exact expression depends on parasitic resistances and load current [19]. However, the current relationship given by Eq. 3.2 is exact and is independent of parasitic losses. Intuitively, since the average current flowing through the output capacitor is zero in steady state, all the inductor current must flow through the LED. Therefore, from Eq. 3.2, the LED current can be precisely determined by finding the average value of the inductor current. If V_{IN} is much lower than the desired V_{LED}, the converter operates in the boost mode by configuring the powerFETs as shown in Fig. 3.2(b). In this mode, the buck-side powerFET P_{BU} is always ON ($D_{BUCK} = 1$) and the boost-side powerFETs operate with a duty-cycle D_{BOOST}. The voltage and current equations in this mode are given by,

$$V_{LED} \approx \frac{V_{IN}}{1 - D_{BOOST}} \tag{3.3}$$

and

$$I_{LED} = \overline{I_L}(1 - D_{BOOST}) \tag{3.4}$$

Thus, from Eq. 3.4, the LED current can be accurately determined by multiplying the average inductor current by a factor, $1 - D_{BOOST}$. Similar to the buck mode, the exact expression for V_{LED} depends on parasitic losses, however Eq. 3.4 can be shown to be independent of parasitic losses.

If V_{IN} is close to the desired V_{LED} the converter operates in the buck-boost mode by configuring the powerFETs as shown in Fig. 3.2(c). In this mode, the buck-side and the boost-side powerFETs operate with a duty-cycle, D_{BUCK} and D_{BOOST}, respectively. The voltage and current equations in this mode are given by,

$$V_{LED} \approx \frac{(V_{IN})(D_{BUCK})}{1 - D_{BOOST}} \tag{3.5}$$

and

$$I_{LED} = \overline{I_L}(1 - D_{BOOST}) \tag{3.6}$$

Again, the current equation remains same as that of the boost mode and is independent of parasitic losses.

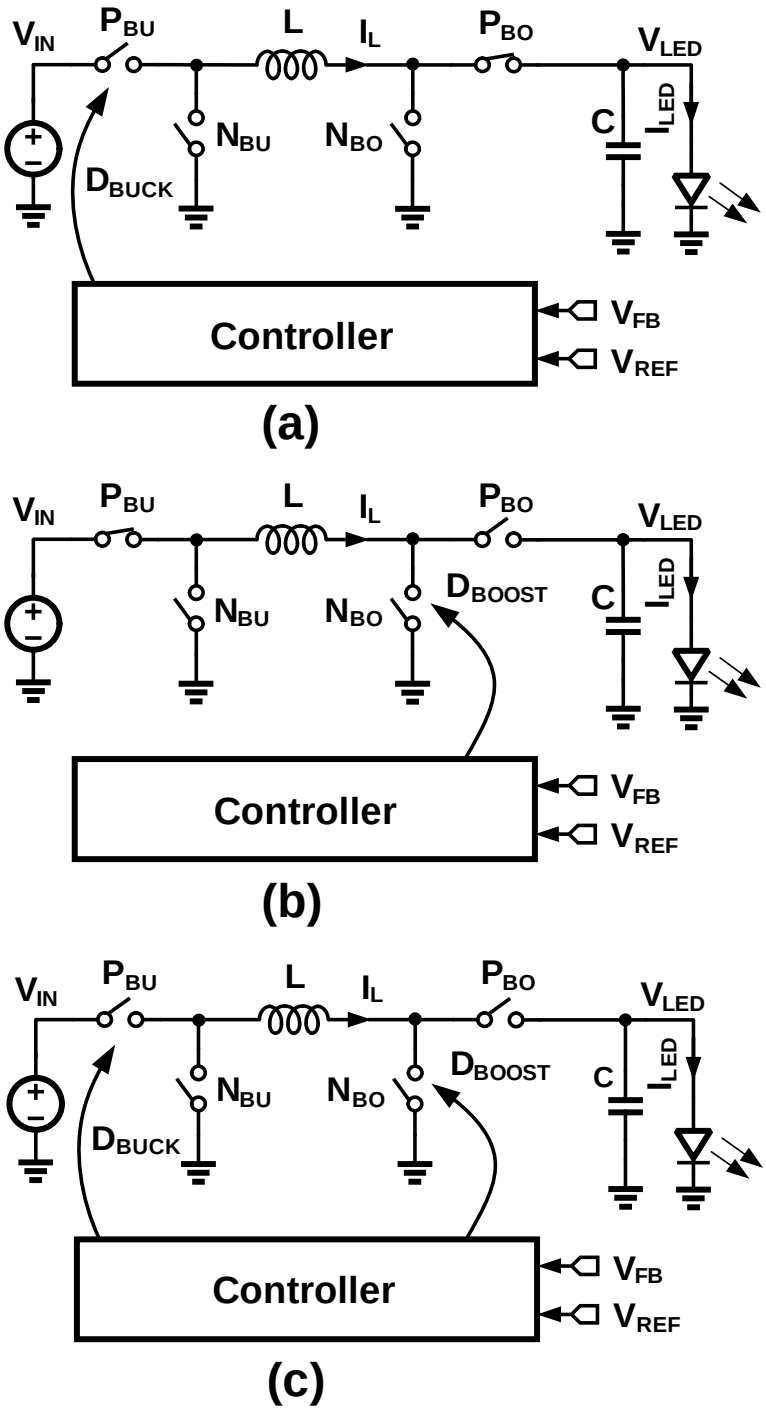

Figure 3.2: PowerFET configuration in different modes: (a) Buck mode. (b) Boost mode. (c) Buck-Boost mode.

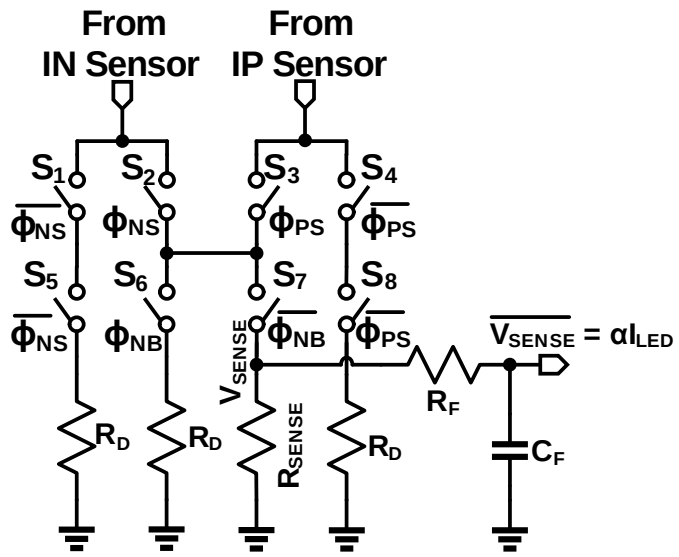

Figure 3.3: Simplified schematic of the LED current estimator.

3.2 Current Estimator Implementation

Figure. 3.3 shows the simplified schematic of the current estimator block. Using switches S_1-S_8, IP- and IN-sensor outputs are selectively routed to the sense resistor, R_{SENSE}, to produce voltage V_{SENSE}. The filter formed by R_F and C_F finds average value of the voltage across R_{SENSE} to produce voltage, $\overline{V_{SENSE}}$, which represents I_{LED}. The operation of the current estimator in different modes is explained next. Figure 3.4(a) depicts the timing diagram in the buck mode. A switching cycle can be divided into 4 distinct regions marked 1, 2, 3 and 4 in Fig. 3.4(a). During the time period marked 1, D_{BUCK} is high, powerFET P_{BU} turns ON and the IP-sensor starts sensing the P_{BU} current. During this phase, Φ_{PS} goes high and switches S_3 and S_7 in the current-estimator turn ON, and route the sensed IP-sensor current to R_{SENSE} to produce voltage, V_{SENSE}. During the time period marked 3, D_{BUCK} is low, powerFET N_{BU} turns ON and the IN-sensor starts sensing

the current. During this phase, switches S_2 and S_7 are enabled to produce V_{SENSE}. Thus, neglecting dead-time, V_{SENSE} represents an exact but scaled version of the inductor current. The scaling factor α depends on the powerFET to senseFET ratio and the value of the sense resistor. Since in our implementation the ratio is 1024:1 and the value of sense resistor is set to 640Ω, α is equal to 640/1024.

During the dead-time, the inductor current flows through the body-diode of N_{BU}. Since both P_{BU} and N_{BU} are OFF, the sensed current is zero and therefore IP/IN-sensor outputs cannot accurately reproduce the inductor current. Furthermore, since sense-stage amplifier slews initially for a few nano-seconds, the sensed current is inaccurate. To improve the overall accuracy of the sensed current, Φ_H phase is introduced into the current sensor. Time periods 3 and 4 in Fig. 3.4(a) correspond to the Φ_H phase. The current sensor holds the value of sensed current during Φ_H and V_{SENSE} remains constant. Since Φ_H is asserted for a very small fraction of the entire switching period, the sensed current error during Φ_H, has negligible impact on the $\overline{V_{SENSE}}$. For example, if Φ_H duration is 20ns for a converter operating at 2MHz, a sensing error of 15% during Φ_H causes an overall error of only $15\% \times (20/500) = 0.6\%$, approximately.

In the boost-mode, as shown in Eq. 3.4, I_L needs to be scaled by a factor $1 - D_{BOOST}$ to estimate I_{LED}. By turning ON switch S_7 only when the boost powerFET N_{BO} is OFF, the sensed current gets scaled exactly by $1 - D_{BOOST}$. Typical I_L and V_{SENSE} waveforms in the boost mode of operation are shown in Fig. 3.4(b). V_{SENSE} now represents the exact but scaled version of the current through the powerFET P_{BO}, the average value of which equals I_{LED}. The operation of the current sensor in the buck-boost mode is a combination of buck-mode and the boost-mode. Consequently, the scaling factor is accounted for in a similar manner to that of the boost mode. The associated timing diagram is depicted in

Fig. 3.4(c).

While only the branch containing R_{SENSE} is used to sense the current, two other auxiliary branches formed by switches S_1-S_5, S_4-S_8 and R_D are used to improve the accuracy of the sensed current. These switches along with R_D are sized such that the auxiliary branches have the same impedance as the branch containing R_{SENSE}. To understand how these branches help improve the accuracy, consider the case when the powerFET N_{BU} is conducting and D_{BUCK} goes from 0 to 1. When N_{BU} turns OFF, the IN-sensor enters the hold mode and the held value is routed to R_{SENSE}. Next, when P_{BU} turns ON, the amplifier in the IP-sensor slews initially. During this time, instead of routing the erroneous slewing current through R_{SENSE}, the dummy branch formed by switches $S_4 - S_8$ is enabled. Once the amplifier settles and starts sensing the current accurately, IN-sensor comes out of the hold phase and IP-sensor current is routed to the sense resistor R_{SENSE}. Thus the auxiliary branches improve accuracy by providing another identical impedance path to the slewing IP-sensor current.

Another source of error in the sensed current is the variation in the sense resistor R_{SENSE}. Highly accurate thin-film resistors with very low variation across process and temperature were used to minimize the error. Alternatively, if accurate resistors are unavailable in the process, accurate external sense resistor can be used.

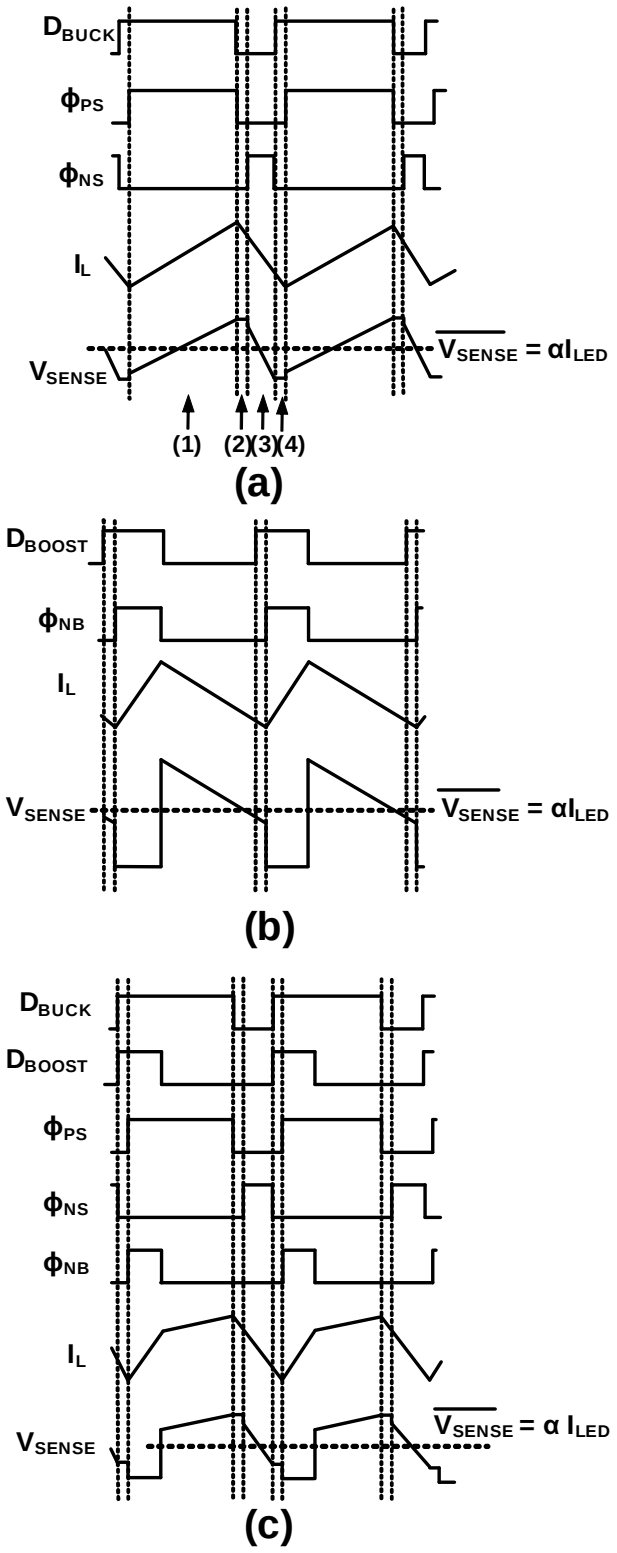

Figure 3.4: Current estimator internal waveforms: (a) Buck mode. (b) Boost mode. (c) Buck-Boost mode.

CHAPTER 4. CIRCUIT DESIGN

4.1 Current Sensor Opamp Design

The sensed current accuracy depends on the opamp parameters such as gain and bandwidth. Inadequate gain causes the drain voltages of the powerFET and senseFET to be different and its effect is similar to the input referred offset of the amplifier. Since auto-zeroing is employed, the effective loop gain is boosted and is much higher than the opamp gain [17]. Therefore, sensed current accuracy is achieved with moderate opamp gain. Since the terminal voltage across the powerFET follows the inductor current profile which ramps up and down at the switching frequency, F_S, the opamp bandwidth needs to be high enough to track it. Since the required bandwidth depends on various factors such as tolerable inaccuracy, V_{IN}, V_{LED} and inductance L, exhaustive simulations remain the best tool to determine the desired bandwidth.

Figure. 4.1 shows the schematic of the amplifier in the IP-sensor. Since the input common mode is close to the supply, NMOS input pair is used. Simulations indicate that a nominal gain and bandwidth of 55dB and 60MHz, respectively, are sufficient to realize accurate current sensing. Extensive simulations performed across corners ensures stability and accuracy of the system. A complimentary structure is used to realize the IN-sensor amplifier.

To determine the required sense stage opamp bandwidth, the amplifier response to the waveform shown on top in Fig. 4.2, which represents the typical

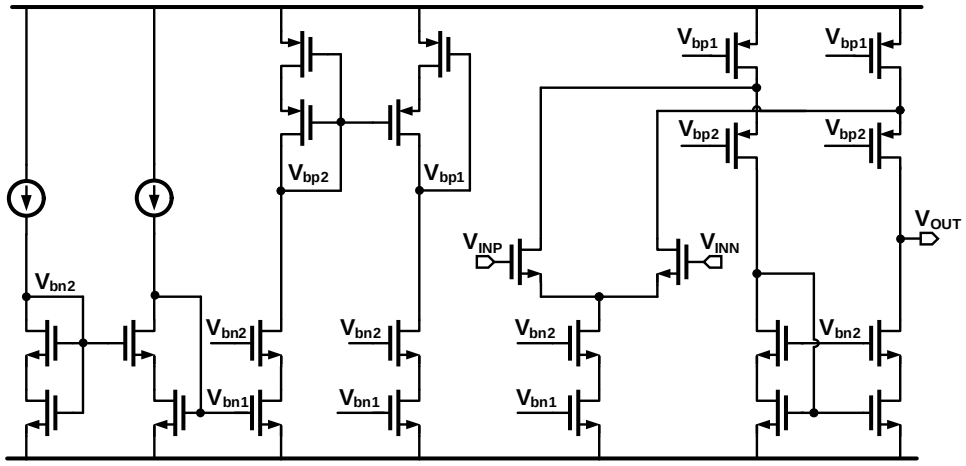

Figure 4.1: IP-sensor opamp schematic.

drain voltage of P_{BU} needs to be analyzed. The drain voltage can be expressed as the sum of two waveforms as shown in the bottom half of Fig. 4.2. Since the IP-sensor begins sensing periodically at the beginning of every time-period, within a time period (marked 1, 2, 3 etc), the two waveforms can be expressed as the sum of a step component, v_u, and a ramp component, v_r. So the drain voltage within a given period can be expressed as,

$$v_{pfet}(t) = v_u(t) + v_r(t) \tag{4.1}$$

The step and the ramp components can be expressed as

$$v_u(t) = -V_{DC}u(t) \tag{4.2}$$

$$v_r(t) \approx -at \approx -(\frac{V_{IN} - V_{LED}}{L}) * (R_{ON})t \tag{4.3}$$

where a corresponds to the slope of the ramp, L is the external inductance and R_{ON} is the ON resistance of the powerFET. For simplicity let us assume that the unity

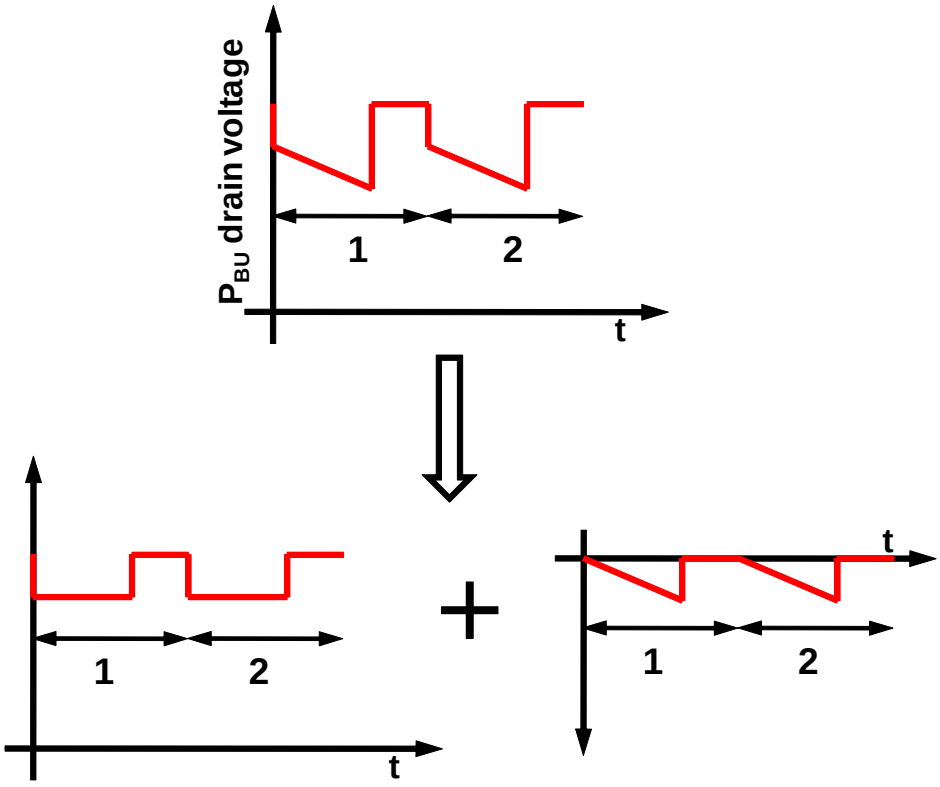

Figure 4.2: Typical drain voltage across P_{BU} expressed as sum of two waveforms

gain feedback loop formed by the amplifier has a single pole closed loop behavior given by,

$$A(s) = \frac{K}{1 + \frac{s}{\omega_{cl}}}. \tag{4.4}$$

The value of K depends on open loop gain and feedback factor. For the unity gain feedback system, $K \approx 1$. ω_{cl} corresponds to the closed loop bandwidth. The response of the system given by Eq. 4.4 to the step stimulus in Eq. 4.1 is given by,

$$v^{u}_{senfet}(t) = -K[V_{DC}(1 - e^{-\omega_{cl}t})]. \tag{4.5}$$

The exponential term in Eq. 4.5 represents the error due to finite bandwidth

and it indicates that a wider bandwidth minimizes the error. Since the steady state error goes to zero, large error is introduced only at the beginning of each time-period. The response of the system given by Eq. 4.4 to the ramp stimulus in Eq. 4.1 is given by,

$$v^{r}_{senfet}(t) = -K[at + \frac{a}{\omega_{cl}}(1 - e^{-\omega_{cl}t})]. \tag{4.6}$$

Unlike Eq. 4.5, Eq. 4.6 shows that the error due to finite bandwidth depends on the ramp-slope in addition to the bandwidth. Furthermore, the steady-state error does not decay to zero but has a finite value given by a/ω_{cl}. This error can therefore be minimized by either increasing the bandwidth or reducing the ramp slope. For a given V_{IN} and V_{LED}, from Eq. 4.6, the ramp slope can be minimized by either increasing the value of L or reducing R_{ON}. However, since the sensed current is inversely related to R_{ON}, the error in sensed current would only depend on the value of V_{IN}, V_{LED} and L.

Since the amplifier is approximated as a first order system and the required bandwidth depends on various factors such as tolerable inaccuracy, input output voltages, value of external inductance mathematically deriving the exact bandwidth requirement is laborious and unnecessary. However, Eqns. 4.5 and 4.6 serve as a good guide to determine how various parameters affect the required bandwidth and accuracy.

4.2 $G_M - C$ stage design

The G_M-C stage integrates the error between the current estimator output, $\overline{V_{SENSE}}$, and the reference voltage. A PMOS input pair folded-cascode amplifier re-

alizes the G_M stage. Large device sizes and good layout techniques are employed to minimize the offset in this stage. An external capacitor, C_C, creates the dominant pole and ensures loop stability.

4.3 Controller and Mode Switching Block

A voltage-mode control is used due to its simplicity compared to a current-mode control [19] and mode switching is performed by a finite-state-machine (FSM). On power up, the converter starts in the buck mode and the FSM performs mode transitions based on the output of the G_M-C stage. For example, the converter transitions from buck mode to buck-boost mode when G_M-C output is high enough to cause D_{BUCK} to be about 90%. Hysteresis is added to the transition points to avoid toggling between the modes during transition. To reduce voltage ripple at the output during mode transitions, D_{BUCK} and D_{BOOST} are instantaneously changed using feedforward voltages, V_{F1} and V_{F2} [21].

4.4 Power Stage Design

The size of the powerFET determines both the conduction loss and switching loss. Though a large powerFET reduces ON resistance and therefore minimizes conduction losses, it results in increased switching losses and area. On the other hand, a small powerFET leads to high conduction loss and degrades the efficiency. As a good compromise between efficiency and area, all the powerFETs were sized to have an ON resistance of around 90mΩ. Good layout techniques were employed to minimize the routing metal parasitic resistance.

CHAPTER 5. MEASURED RESULTS

The die photograph of the proposed LED driver, fabricated in 0.5μm CMOS process, is shown in the Fig. 5.1. The prototype includes all the powerFETs, drivers, current sense circuitry, reference system, control block, oscillator to produce the clock and the ramp signals. An I^2C interface is used to control various test modes. The die size is 2.5mmx3mm and the prototype occupies an active area of about $5mm^2$. The chip was packaged in a 30pin micro-SMD package which offers very low package parasitics.

The test setup is shown in Fig. 5.2 and the corresponding component values are tabulated in Table 5.1. Note that resistor R_S is used only for test purposes to measure I_{LED} and shorted using S_1 during normal operation. Though current estimator uses an internal accurate sense resistor, an option to use an external sense resistor R_{SEN} is also incorporated. Figure 5.3 shows startup profile of the converter. On power up, G_M stage slews to charge the capacitor, C_C. The startup time is around 7ms and is mainly determined by the slew-rate of the G_M-C_C stage. Figure 5.4 shows the measured D_{BUCK} and D_{BOOST} when V_{IN} is changed from 5.2V to 2.7V at 600mA of I_{LED}. At maximum V_{IN}, the converter operates in the buck mode with $D_{BOOST} = 0$. As V_{IN} is reduced, D_{BUCK} increases to regulate I_{LED}, and when D_{BUCK} reaches around 90%, the converter enters buck-boost mode of operation. In this mode D_{BOOST} initially set to around 10% and when it reaches around 30%, the converter enters the boost mode of operation. Figure 5.5 shows the measured V_{LED} when V_{IN} is changed from 2.7V to 5.2V and back to 2.7V. This shows that the converter performs smooth transition across different modes

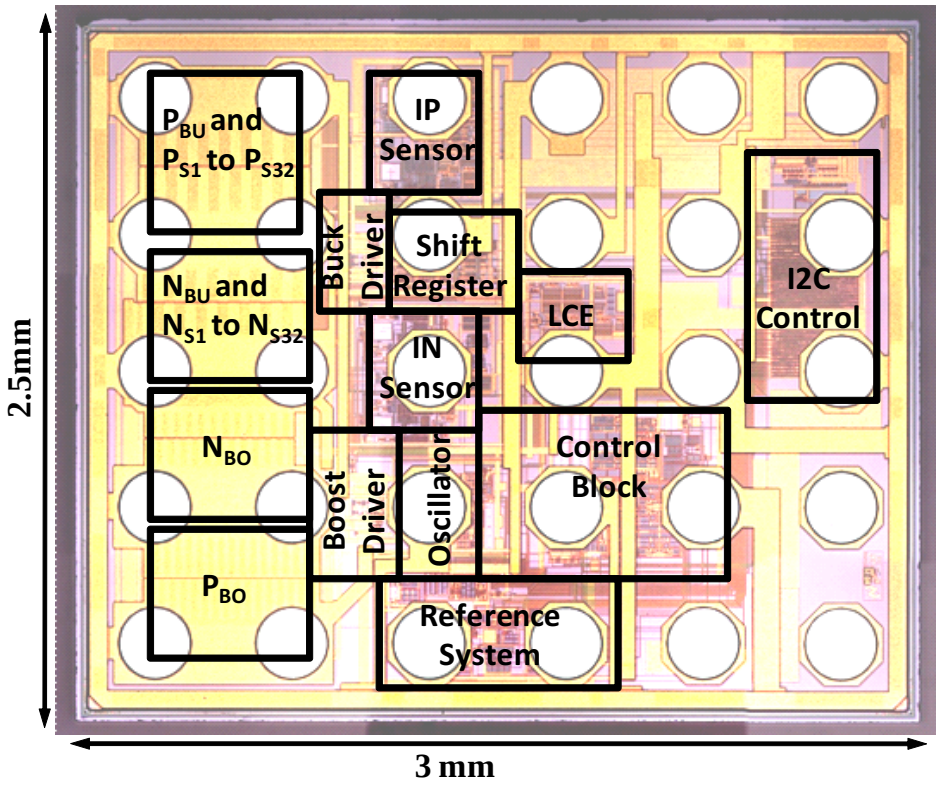

Figure 5.1: Die photograph.

and maintains a steady V_{LED} over the entire range of V_{IN}. When converter is shut down, V_{LED} does not immediately go to 0V, this is due to the absence of an active pull-down transistor at the output of the driver. Figures 5.6(a), 5.6(b) and 5.6(c) depict the sensed voltage and inductor current in the buck, boost and buck-boost modes of operation, respectively. For better illustration, I_L and V_{SENSE} are intentionally offset by 50mA and V_{SENSE} is scaled appropriately to account for the factor α (640/1024) in the sensed current. Note that in all the modes, the sensed voltage differs from cycle-to-cycle depending on the mismatch between the power-FET and the enabled senseFET. However, the measured average LED current, is accurate as proposed. Figure 5.7 shows the measured average I_{LED} across V_{IN} for

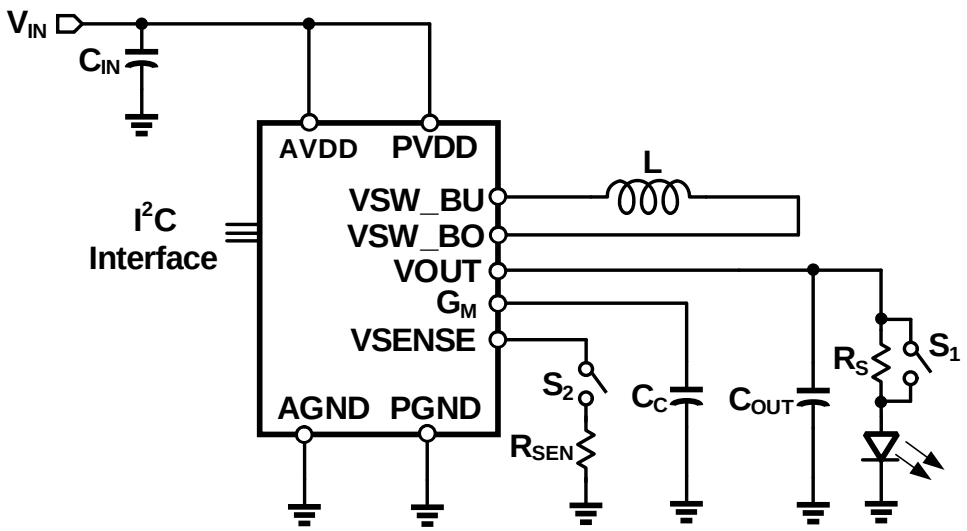

Figure 5.2: Test setup.

Table 5.1: Component values

Component Name	Value
C_{OUT}	10μF
L	2.2μH
C_{IN}	10μF
C_C	100nF
R_s	100mΩ
R_{SEN}	640Ω

7 different devices at 600mA, 900mA and 1.2A. Thanks to the proposed current sensing technique, the variation in I_{LED} is less than $\pm 2.8\%$. Figure 5.8 shows the standard deviation of the measured I_{LED} across 7 devices. To isolate sens-

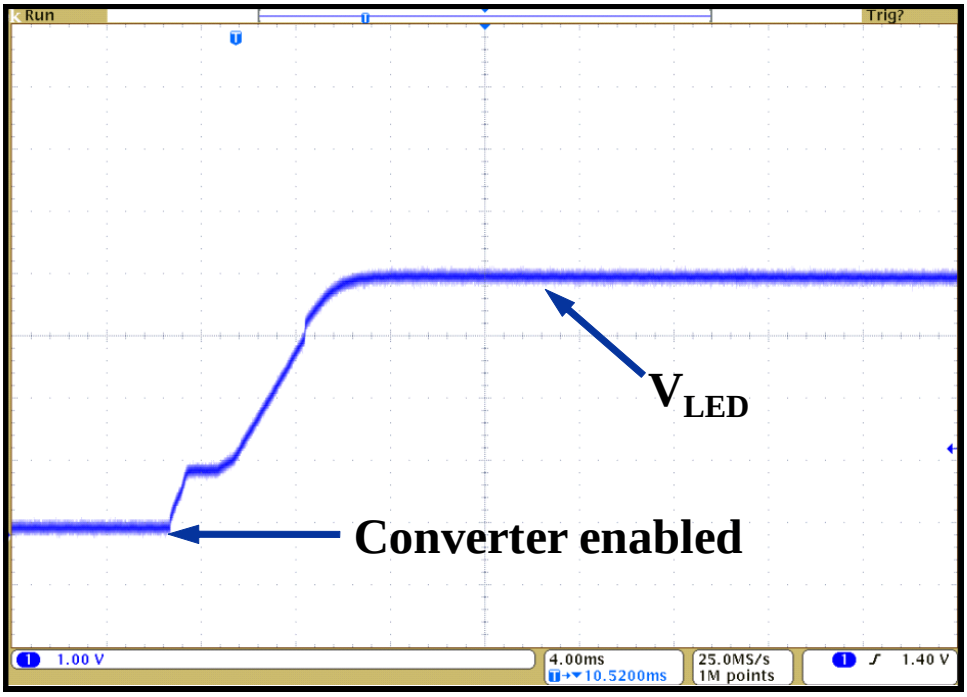

Figure 5.3: Converter startup.

ing accuracy from other error sources, the variation in band-gap reference voltage is corrected and an external sense resistor is used in the LED current estimator block. The standard deviation is less than 1.6% over the entire input range. Using an internal accurate thin film sense resistor increased the standard deviation to 2.2%. This low standard deviation across devices shows that auto-zeroing and error-averaging are effective in achieving very good sense accuracy. Figures 5.9(a) and 5.9(b) show the efficiency improvement of the proposed converter over the conventional LED driver at 1.2A and 600mA current, respectively. The efficiency of the conventional architecture was measured by connecting a resistor, in series with the LED (see Fig. 1.2(a)). The voltage drop across the resistor is set to 250mV. For fair comparison, the power loss due to the sensing circuitry was subtracted from the input power. At 1.2A LED current, the proposed architecture

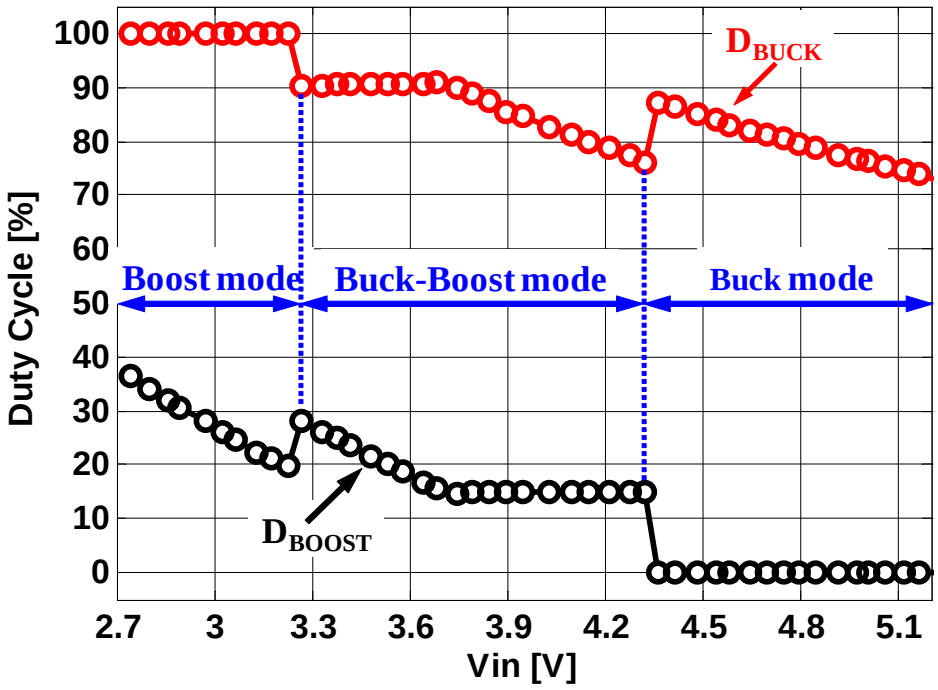

Figure 5.4: Measured D_{BUCK} and D_{BOOST} versus V_{IN}.

achieves an efficiency improvement of 4.5%, 6% and 13% in buck, buck-boost and boost modes of operation, respectively. The efficiency improvement is maximum in the boost mode. This is because, the lower converter output voltage, due to the absence of the CRE, reduces the conduction loss to a greater extent in the boost mode. The efficiency improvement at 600mA current is 6%-8%. Table 5.2 summarizes the performance of the LED driver.

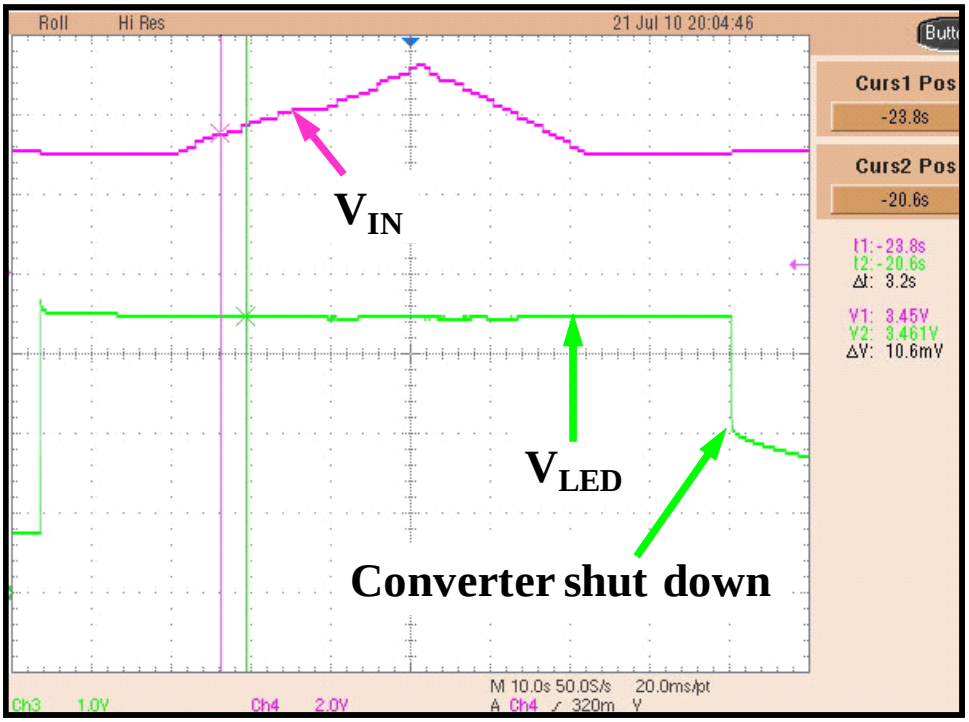

Figure 5.5: Measured V_{LED} versus V_{IN}.

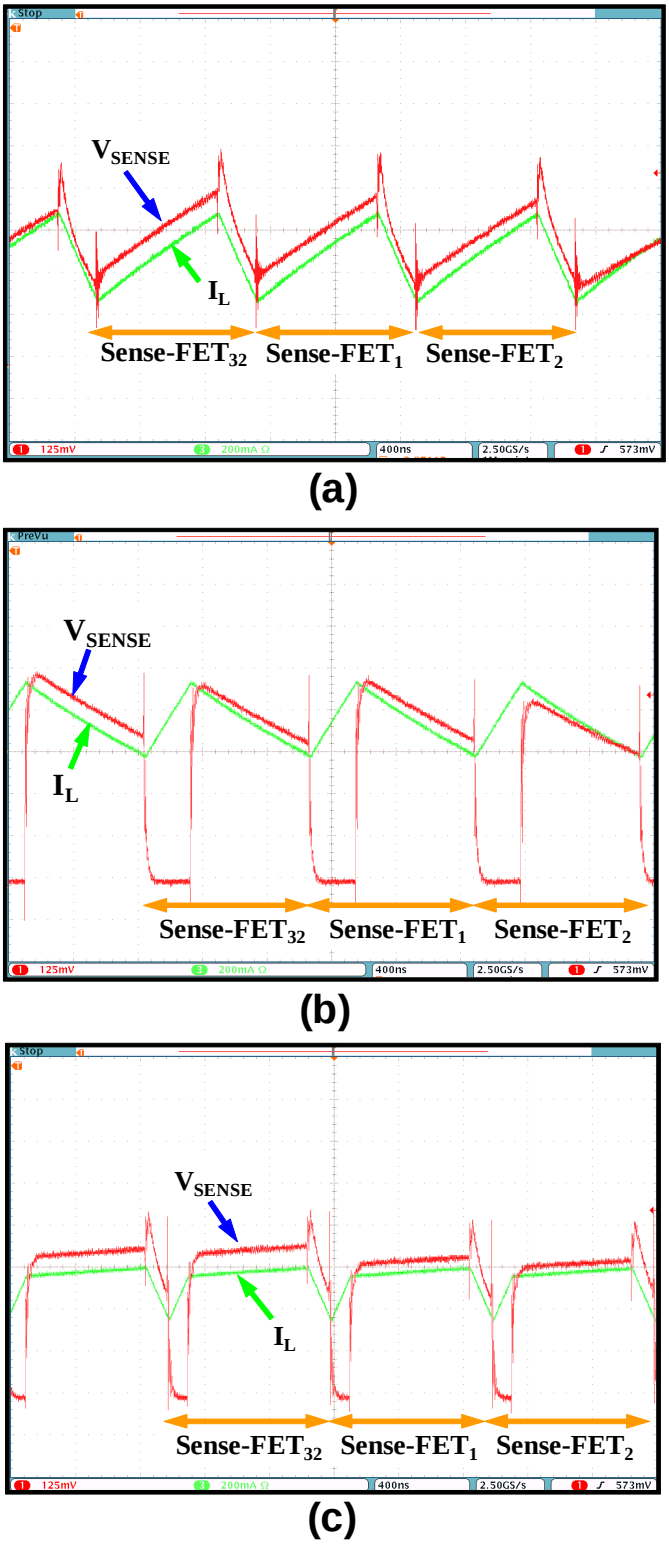

Figure 5.6: Measured inductor current and sensed voltage: (a) Buck mode. (b) Boost mode. (c) Buck-Boost mode.

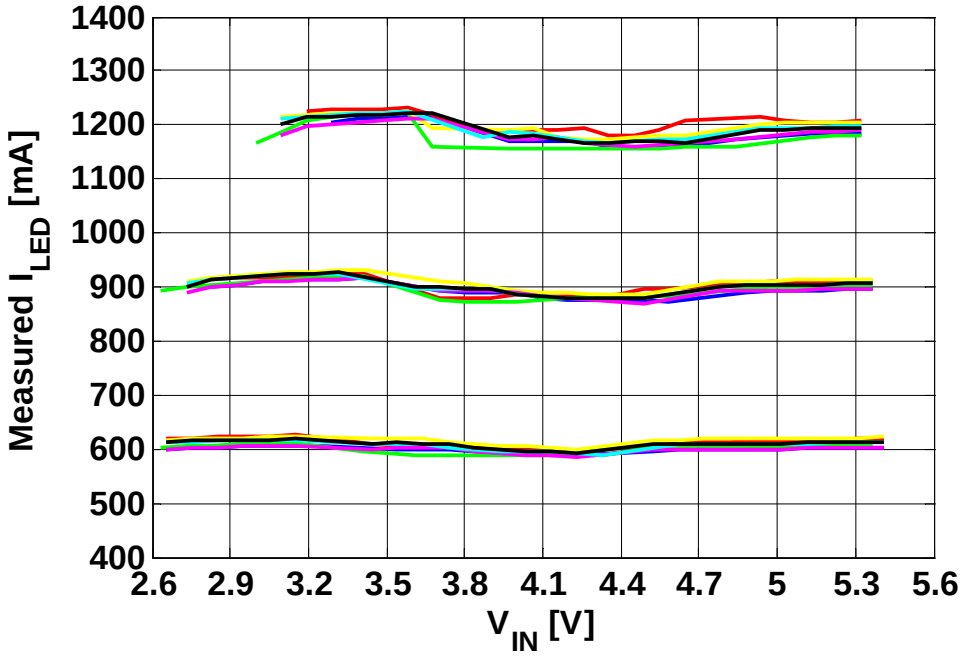

Figure 5.7: Measured I_{LED} versus V_{IN} at 600mA, 900mA, 1200mA for seven different devices.

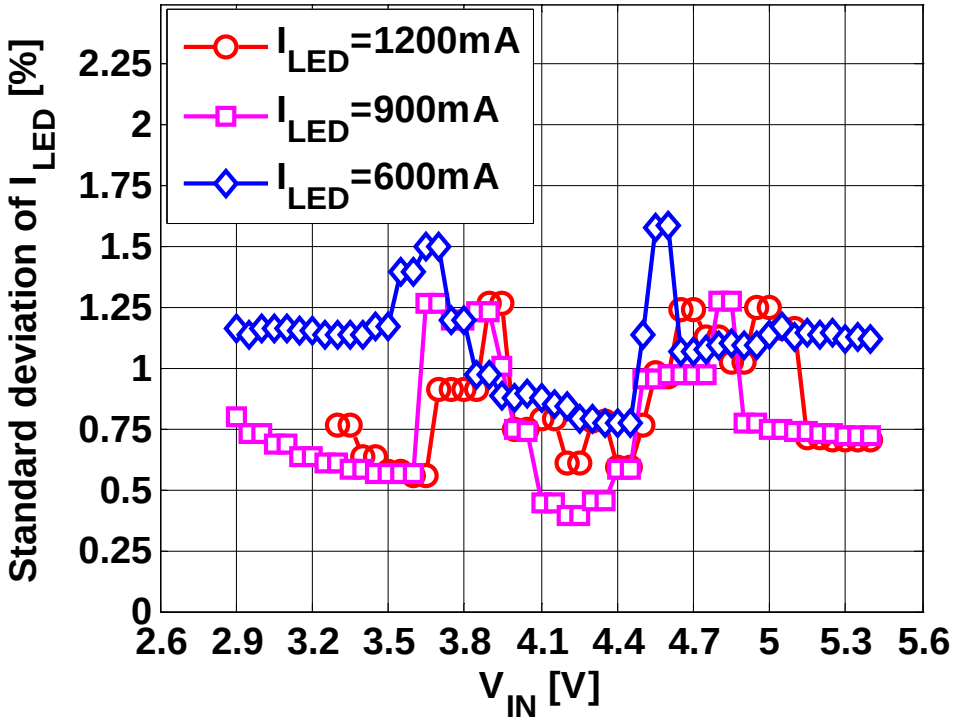

Figure 5.8: Measured standard deviation of I_{LED} at 600mA, 900mA, 1200mA across seven different devices.

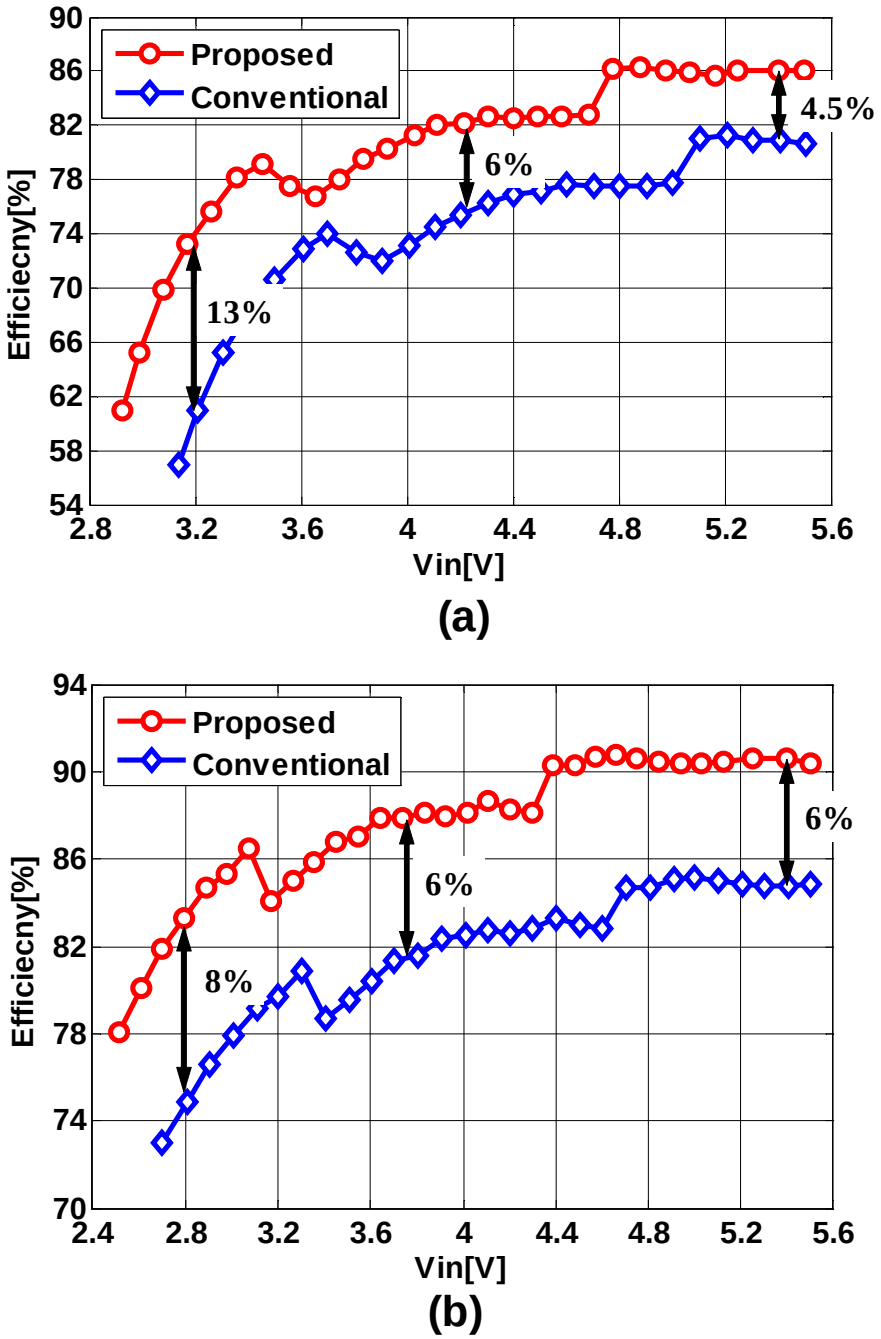

Figure 5.9: Measured efficiency versus V_{IN}: (a) 1.2A LED current. (b) 600mA LED current.

Table 5.2: Performance summary of the converter

Technology	0.5μm CMOS
V_{IN}	3-5.5V
V_{LED}	$\approx$ 3.6V
Switching Frequency	1MHz-2MHz (programmable)
I_{LED} variation with V_{IN}	$\pm$2.8%
Current sense standard deviation	1.6%
Efficiency improvement (at 1.2A)	13 %
Peak Efficiency (at 600mA)	90.7%
Active area	5mm^2
Package	μSMD

CHAPTER 6. CONCLUSION

This thesis presented design techniques to improve the efficiency of LED drivers. A CRE-less buck-boost LED driver was designed using novel, highly accurate, on-chip, lossless senseFET based current sensors. Error-averaging and auto-zeroing techniques were employed to improve the accuracy of the sensed current and decouple the tradeoff between power loss and accuracy present in all conventional current sensing schemes. Measurement results from multiple devices of the prototype showed that the proposed techniques are insensitive to process variations and are capable of sensing LED current accurately. Measured results also validate the claim that I_{LED} can be accurately estimated from sensed powerFET currents in buck, buck-boost and boost modes of operation. Because the proposed scheme eliminates the series current-regulation-element, it greatly improves efficiency and reduces cost. Fabricated in $0.5\mu\mathbf{m}$ CMOS process, the prototype occupies an active area of $5mm^2$. At 1.2A LED current, the driver achieves an efficiency improvement of over 13% compared to current-regulation-element based LED drivers. Measured LED current accuracy is better than 2.8% over the entire range of the battery and its standard deviation measured across 7 devices is less than 1.6%. The peak efficiencies are 90.7% and 86% at 600mA and 1200mA currents, respectively.

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