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Title: Dual Referencing Guidelines to Minimize Power Delivery Noise Coupling.

Abstract approved:

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Dual referencing has been garnering a lot of attention in the power integrity community, specifically in the voltage mode driver application because it shows a lower overall power delivery noise (PDN) compared to other signal referencing types. Additionally, the increasing push to drive down package and board manufacturing costs is another essential factor to consider dual referencing. As bus operating frequency increases, PDN increases, which could lead to more coupling onto signal nets which, in turn, can distort data and degrade signal integrity. It is generally understood that since dual referenced signals are closer to the power rails, they are more prone to coupling of power delivery noise. As system speeds begin to surpass the 5GT/s range, the noise from the power rails can no longer be neglected. This work provides a comprehensive study of PDN coupling onto signal nets in dual referencing and attempts to quantify the magnitude of the coupling and the factors that increase these noise effects. A dual referenced board was manufactured in order to conduct various experiments to which parameters could be manipulated in order to minimize the effects of the noise. Guidelines to mitigate the effects of PDN in dual referenced boards are proposed.

Key Words: Dual Referencing, Crosstalk, Power Delivery Noise, Signal Integrity
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Dual Referencing Guidelines to Minimize Power Delivery Noise coupling.

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Shannon Mark, Author

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TABLE OF CONTENTS

Page

1. Introduction 11

1.1. Typical Signal Integrity Problems..... 11

1.1.1. Reflections..... 2

1.1.2. Crosstalk..... 2

1.1.3. Power Delivery Noise..... 5

1.2. Referencing Types..... 7

1.3. Paths of Noise..... 8

2. Methodology..... 10

2.1. Experimental Setup..... 10

2.2. Simulation and Measurement Tools Overview..... 12

2.2.1. Frequency Domain Tools..... 12

2.2.2. Frequency Domain Setup..... 14

2.2.3. Time Domain Simulation and Measurement Tools..... 18

2.2.4. Time Domain Setup..... 19

2.2.5. Simulation Tool vs. Measurement Tool Correlation..... 25

3. Experiments and Results..... 29

3.1. Noise Coupling Paths..... 29

3.2. Trace vs. Via..... 31

3.3. Length Impact..... 35

3.4. Layer Impact (Via stub Impact)..... 37

3.5. Asymmetric vs. Symmetric Routing..... 42

4. Conclusion and Next Steps 46

LIST OF FIGURES

Figure Page

Figure 1: Crosstalk Representation……14

Figure 2: Microstrip vs. Stripline……15

Figure 3: Single Referencing……18

Figure 4: Dual Referencing…… 18

Figure 5: Paths of noise……19

Figure 6: Set up of experiments on the board. ……21

Figure 7: Example of one experiment. ……21

Figure 8: Side view of experiments. Green (Ground), Red(Power), Blue (Signal) ..21

Figure 9: Picture of the manufactured board……22

Figure 10: Port setup in HFSS. ……25

Figure 11: Power Return loss – Experiment 1 (S11) ……26

Figure 12: Signal Return loss – Experiment 1 (S22) ……27

Figure 13: Power Insertion loss – Experiment 1 (S12) ……27

Figure 14: Signal Insertion loss – Experiment 1 (S34) ……27

Figure 15: Near-end Crosstalk (NEXT) – Experiment 1 (S13 = S24) ……28

Figure 16: Far-end Crosstalk (FEXT) – Experiment 1 (S14 = S23) ……28

Figure 17: TDR measurements of Power plane path for Experiments 1, 3, 5……29

Figure 18: TDR measurements of Power plane path for Experiments 2 and 4……30

Figure 19: TDR measurements of Signal path for Experiments 1, 3, 5……30

Figure 20: TDR Measurements of Signal path for Experiments 2 and 4……31

Figure 21: TDR measurements of Impedance for Power in Experiments 1, 3, 5……32

LIST OF FIGURES

Figure Page

Figure 22: TDR measurements of Impedance for Power in Experiments 2, and 4..32

Figure 23: TDR measurements of Impedance for Signal in Experiments 1, 3, 5. …..33

Figure 24: TDR measurements of Impedance for Signal in Experiments 2, and 4. .33

Figure 25: Noise Profile for Dual referenced board……34

Figure 26: Time Domain Setup……..35

Figure 27: Insertion loss correlation for Experiment 2. ……36

Figure 28: Crosstalk correlation for Experiment 2……36

Figure 29: Insertion loss correlation for Experiment 3……37

Figure 30: Crosstalk correlation for Experiment 3……37

Figure 31: Power Plane to Trace/return path setup……39

Figure 32: Power plane to trace and return path coupling……40

Figure 33: Via to via coupling setup……40

Figure 34: Power via to signal via coupling……41

Figure 35: HFSS model with trace. (Top View) ……..42

Figure 36: HFSS model without trace. (Top View)……42

Figure 37: Side view with the signal trace……42

Figure 38: Side view without signal trace. ……42

Figure 39: NEXT Frequency Response……..43

Figure 40: FEXT Frequency Response……43

Figure 41: NEXT Time Domain……44

LIST OF FIGURES

Figure Page

Figure 42: FEXT Time Domain……44

Figure 43: Length impact setup……45

Figure 44: NEXT with varying lengths in frequency domain……45

Figure 45: FEXT with varying lengths in frequency domain. ……46

Figure 46: NEXT with varying layers in time domain……46

Figure 47: FEXT with varying layers in time domain. ……47

Figure 48: Example of a via stub……48

Figure 49: Side view of experiments used……49

Figure 50: NEXT comparing layers……49

Figure 51: FEXT comparing layers……50

Figure 52: NEXT comparing layers……51

Figure 53: FEXT comparing layers……51

Figure 54: Symmetric vs. Asymmetric Setup……52

Figure 55: NEXT frequency domain of Symmetric vs. Asymmetric……53

Figure 56: FEXT frequency domain of Symmetric vs. Asymmetric……53

Figure 57: NEXT time domain of Symmetric vs. Asymmetric……54

Figure 58: FEXT time domain of Symmetric vs. Asymmetric……54

Dual Referencing Guidelines to Minimize Power Delivery Noise Coupling.

1. Introduction

In high-speed circuit design, signal integrity (SI) becomes a major concern for both high-speed boards, packages and for deep-submicron integrated circuits (ICs). Systems operating in high frequency, where conductors no longer behave as simple wires but as transmission lines are used to transmit or receive electrical signals from components in close proximity. These transmission lines need to be handled appropriately; otherwise the potential of ruining system timing becomes substantial. Therefore, as clock rates increase, designers are forced to investigate new ways to maintain the signal integrity. The main goal of signal integrity is to transmit inter-chip digital data signals successfully.

1.1. Typical Signal Integrity Problems

The three most common SI problems include reflections, crosstalk and power/ground noise. The primary reason that reflections come into play is when there is impedance mismatch along the signal path, other reasons include stubs, vias and various other interconnect discontinuities. Crosstalk noise is due to the electromagnetic coupling that occurs between signal traces and vias. Lastly, power/ground noise is due to the parasitics of the power/ground delivery method during the drivers' simultaneous switching output (SSO) [1]. These three challenges are further discussed in the following sections. Other SI problems include Electromagnetic Compatibility or Electromagnetic

Interference (EMC/EMI) problems that could contribute to the signal waveform distortions. All of these issues can cause voltage fluctuations that disturb the data as well as cause a logic error, dropped data, false switching, and even system failure can be a potential result [1]. This work primarily focuses on the crosstalk that occurs from power delivery noise.

1.1.1. Reflections

As previously mentioned, reflections are principally the result of an impedance discontinuity along the signal transmission path. As a signal moves from one layer to another, and the impedance values are not taken into account, reflection will occur at the discontinuity boundary. When a trace is routed over planes that have perforations at various locations such as degassing and via holes, crossing a gap, having stubs, or passing the proximity of another trace, an impedance discontinuity will occur and a reflection is observed [1]. Lastly, as a signal reaches the receiving end of a transmission line, the load needs to be matched with the transmission line characteristic impedance; otherwise reflections will be encountered again. Some common solutions to minimize reflection noise include controlling the trace characteristic impedance, eliminating stubs, choosing appropriate termination schemes and always using a solid metal plane as the reference plane for return current.

1.1.2. Crosstalk

Crosstalk is caused by electromagnetic coupling between multiple transmission lines running in parallel [2]. When transmission lines or transmission structures are close to each other, their electric field and magnetic fields from the propagating signal will fringe

and interact with the neighboring conductors. In circuit terms, the electric field refers to the mutual capacitance between the two lines while the magnetic field refers to the mutual inductance. This interaction of the fields encourages the coupling of energy from one transmission structure to another when it is driven by a signal and this is what is referred to as crosstalk [2]. There are many transmission lines routed in parallel in packages, connectors, and printed circuit boards, so crosstalk plays an imperative role in determining the performance of the whole system. The main focus of this work is to see the crosstalk that occurs when power delivery noise comes into contact with the signal traces and vias. Power delivery noise will be discussed in more detai, in the following section.

There are two main types of crosstalk. The first is near-end crosstalk (NEXT) and the second is far-end crosstalk (FEXT). NEXT is described as the noise induced between adjacent pairs at the near-end of the transmission line, or the end closest to the point of the signal origin. In order to measure NEXT, a signal is driven onto one of the parallel lines while keeping the other line quiet, and the close-end of the quiet line is measured to see how much of the signal was coupled onto that line[2]. FEXT is defined as noise induced onto an adjacent pair at the far-end of the transmission line. It is measured by transmitting a single into one line at one end and measuring the resulting signal power on an adjacent part at the other end. Figure 1 shows these phenomenon's in a graphical representation. The figure shows coupling between two transmission lines, but it is important to note that coupling can occur between planes and traces, and also between vias.

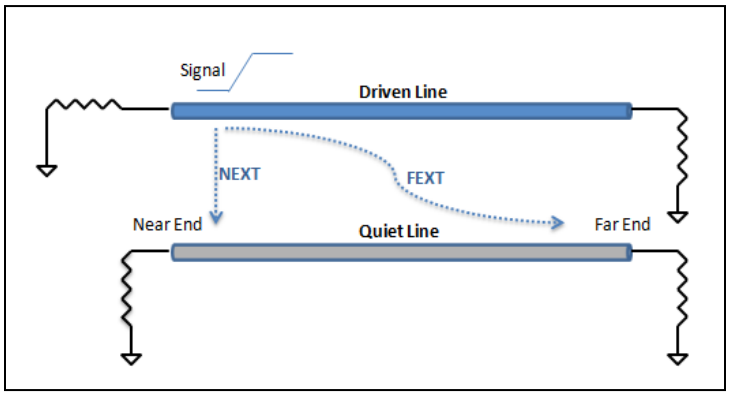

Figure 1: Crosstalk Representation.

Trends are relaying that as systems become smaller and faster, crosstalk levels increase affecting the signal integrity and timing by varying the propagation characteristics of the lines. In addition, crosstalk couples noise onto the driven lines which harms the signal integrity and reduces noise margins.

There have been some guidelines that have been developed to help a designer limit the negative impact of crosstalk. These reduction techniques include [2]:

- Expanding the spacing between the lines as much as routing restrictions will allow reduction of electromagnetic coupling.
- Designing the transmission line so that the conductor is as close to the ground plane as possible so that more coupling will occur between the ground plane and trace rather than adjacent traces.
- Using differential routing techniques to cancel common mode inserted noise.
- Route traces on adjacent PCB signal layers orthogonally to each other.
- Reduce signal edge rates.

- Insert power/ground pins between signal I/O pins in connectors, sockets and packages.
- Routing the signals on a stripline, which is a signal layer that has two reference planes and is between the same dielectric, rather than on a microstrip which has only one reference plane is usually a signal layer sandwiched between air and a dielectric. Refer to Figure 2 to show the difference between a stripline and a microstrip.
- Choosing placement of components to minimize the congestion of traces.

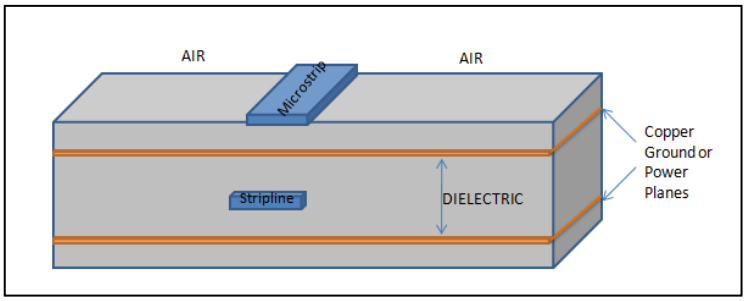

Figure 2: Microstrip vs. Stripline

1.1.3. Power Delivery Noise

Power delivery noise has been known to be one of the most difficult electromagnetic effects to be modeled because of the complexity of the distribution system. The power distribution networks are formed from the power/ground planes and vias located on chip packages and printed circuit boards [4]. The power delivery noise consists of simultaneous switching noise and random noise. Transient currents that are drawn by various number of devices that are switching simultaneously can cause voltage variations between the power and ground planes and this is what is

referred to as simultaneous switching noise. Random noise also comes from high frequency noise currents from the core circuits.

This power delivery noise has several impacts on the signal integrity such as the drop in signal quality, timing issues, jitter, and in extreme cases it has the ability to affect the functionality [6]. The signal quality degrades when power delivery noise increases due to the coupling of that noise onto the signals. The timing gets affected because there is a delay associated with the multiple stages of devices the signal needs to pass through from the core logic and all of these stages are connected to the same power and ground rails. Therefore as the rail voltage fluctuates due to PDN, the delay through each stage increases or decreases. The noise in the power delivery rails has a few ways of increasing jitter on clock and strobe signals. The noise on the voltage controlled oscillator (VCO) will cause phase distortion and frequency shift, and the noise on the input/output (IO) rails will cause simultaneous switching output (SSO) type effects that produce jitter. The slew rate mismatches also produces duty cycle errors. Lastly, in severe cases, PD noise can make IOs non-functional by causing the voltage to fall below the threshold levels.

There are a few ways to minimize the power delivery problems [5]. These include:

- Buffer strength & slew rate selection
- Clock isolation schemes
- Vcc/Vss isolation schemes
- Power/Ground referencing schemes.

- Using a decoupling capacitor.

This work focuses on the last option of choosing the power and ground referencing schemes. The next section will go into more detail of the different referencing types and their relation to power delivery noise.

1.2. Referencing Types

Referencing is used to supply power or a ground path to various signals on the package and the board. The three most common referencing types include single, dual and cross referencing. Single referencing entails the referencing of signals to one reference plane, typically ground (Vss), while dual referencing corresponds to two different reference planes, generally ground and power (Vddq). The third referencing technique, cross referencing, is a combination of both dual and single referencing on the same platform. Examples of single and dual reference configurations in 3D and 2D are shown in Figure 3 and Figure 4 respectively. The 2D shows the side view of the referencing scheme as well as the top view of the vias. The green planes and PTH's correspond to ground, the red plane and PTH's correspond to power and the multicolored PTH's correspond to the different signal traces.

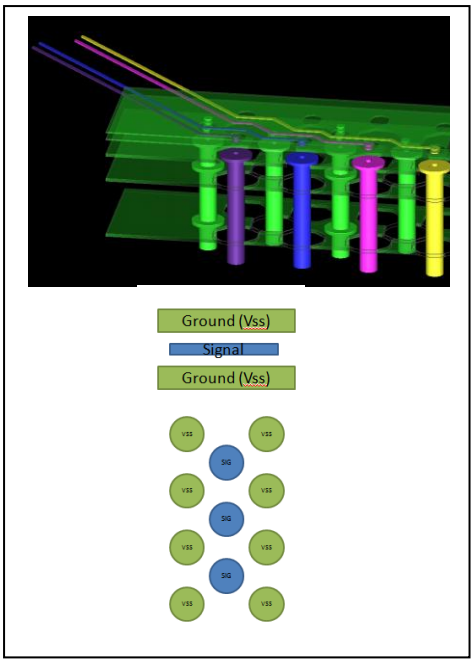

Figure 3: Single Referencing.

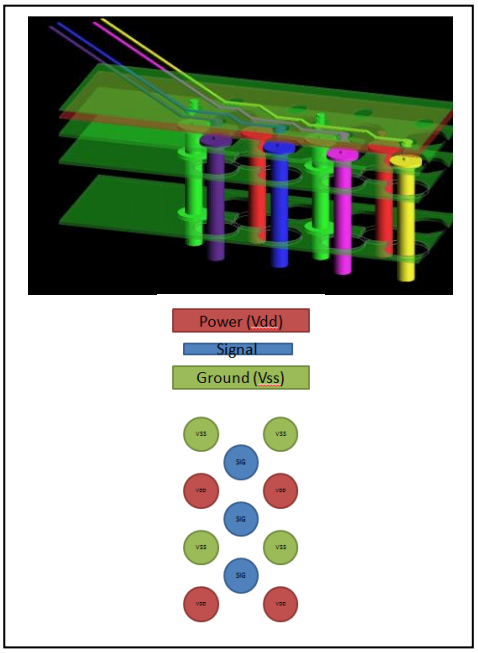

Figure 4: Dual Referencing.

Dual referencing is shown to produce less power delivery noise than any of the other referencing types which is why it has been acquiring a lot of interest [5]. The reduction in power delivery noise helps with the signal performance and speed improvement. Dual referencing can reduce two layers on a package which in turn reduces the loop inductance which reduces the power delivery noise impedance. In addition, as previously mentioned, the manufacturing cost reduction due to the layer count difference is also another motivation.

1.3. Paths of Noise

There are three different paths through which noise from the power rail can get coupled onto the signals. The first path by which power noise can get coupled onto signals is by direct coupling from the Vddq nets to Signal nets. The second path is through the coupling of Vddq noise from traces and vias to neighboring traces and

neighboring vias. The third path is through a shared or common return path. Figure 5 shows the graphical representation of these noise paths. Direct coupling can be due to the power plane to the signals or the power via/PTHs to the signal vias/PTHs. An in-depth study of these noise avenues and their contribution to coupling will be discussed in a subsequent section.

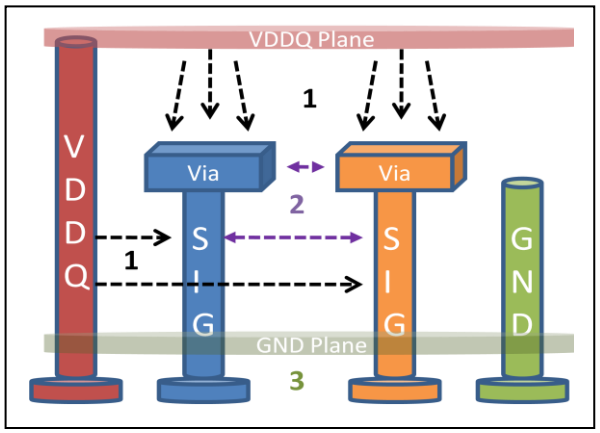

Figure 5: Paths of noise.

Dual Referencing Guidelines To Minimize Power Delivery Noise Coupling.

2. Methodology

2.1. Experimental Setup

In order to understand the power delivery noise coupling onto signal nets for dual referencing, a board was manufactured with five experiments designed on it. The purpose was to understand PDN coupling when signal trace lengths vary and when signals are on different layers of the board. Furthermore, these experiments will help to understand whether the traces or the via stubs are the dominant source of noise and which, if any, can be ignored.

A 14 layer dual referenced board with a 62 mil thickness was manufactured that contained the experimental structures. The first two experiments had signal trace lengths equal to 0.5 inches on layer 3 and on layer 12. Experiments 3 and 4 had signal trace lengths equal to 1 inch located on layer 3 and 12. The last experiment had a 2 inch signal trace routed on layer 3. These setups are shown in Figure 6 and Figure 7 shows an example of what one experiment looks like. This signal trace can be both on layer 3 and Layer 12 and the lengths of the trace are varying. Figure 8 shows a side view representation of the experiments where the green refers to ground, the red to Vddq, and the blue to the signal. A side view of the board Figure 8 and the manufactured board is shown in Figure 9.

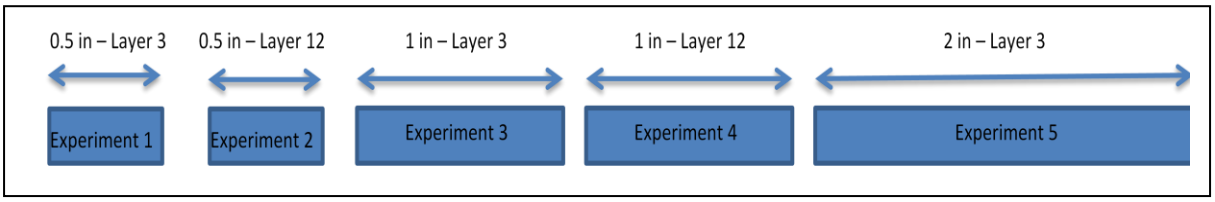

Figure 6: Set up of experiments on the board.

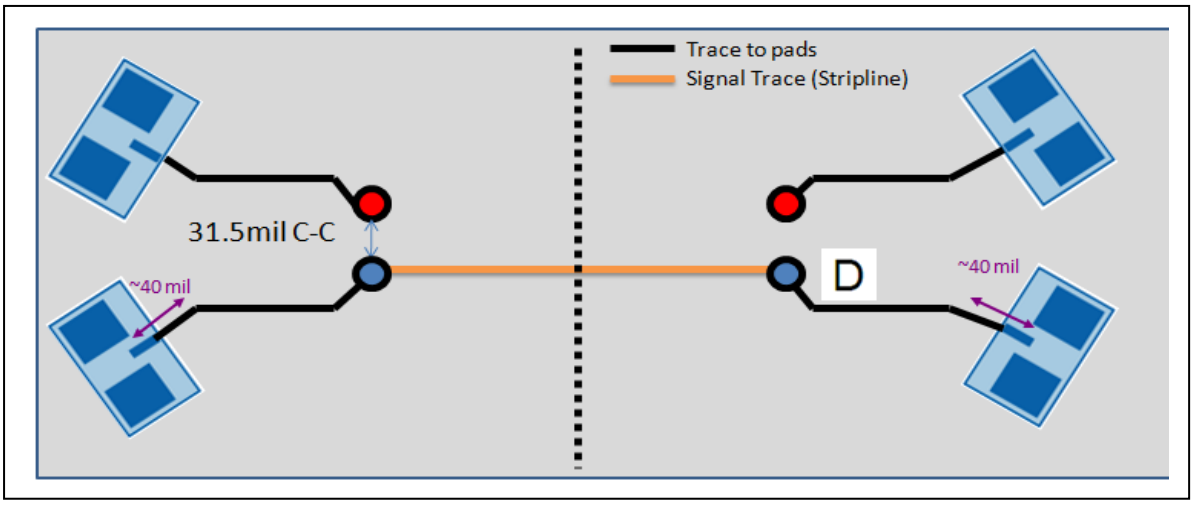

Figure 7: Example of one experiment.

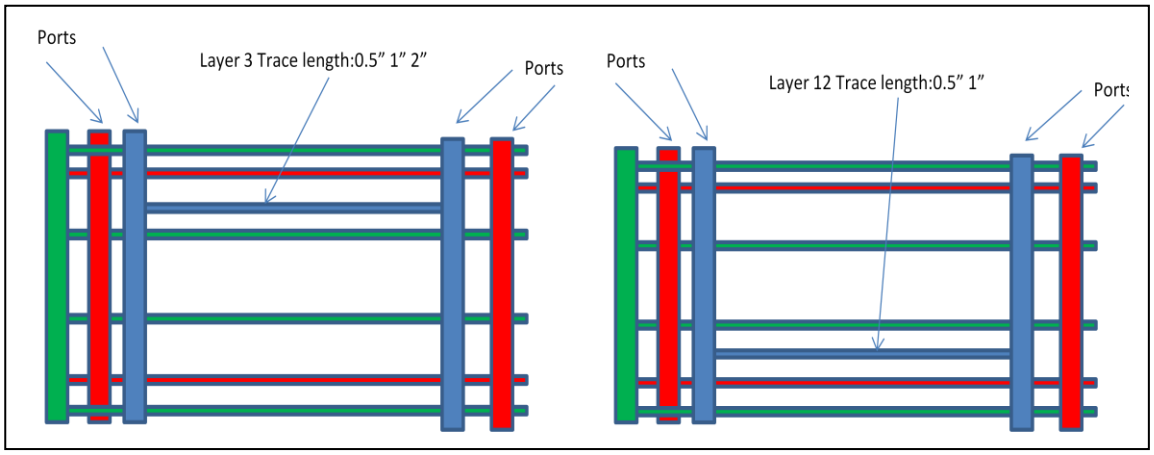

Figure 8: Side view of experiments. Green (Ground), Red(Power), Blue (Signal)

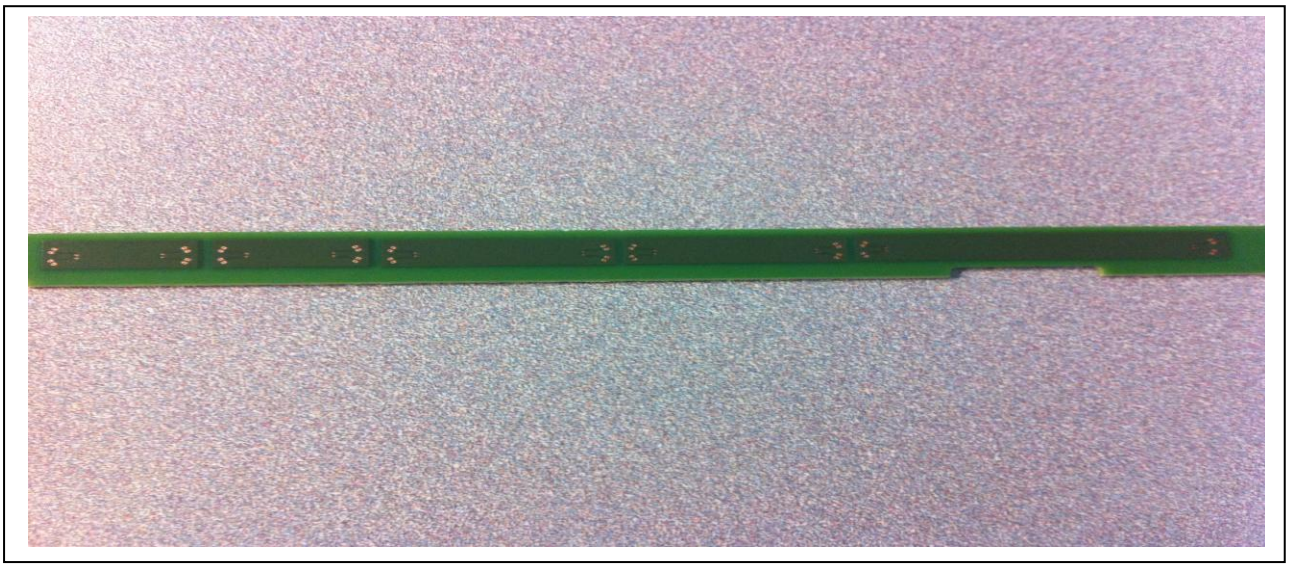

Figure 9: Picture of the manufactured board.

2.2. Simulation and Measurement Tools Overview

The simulation tools that were used to find the frequency domain characteristics include HFSS by Ansoft, a vector network analyzer (VNA) and a time domain reflectometer (TDR). PowerSI is another tool that is used by signal integrity engineers will be briefly discussed in the following section. For the time domain characteristics, HSPICE was utilized as well as Broadband Spice. One of the studies that was analyzed was to see whether HFSS correlates well with the measured results from the VNA. This section will cover a brief summary of the frequency domain tools, the time domain tools, the frequency and time domain setup, and the correlation between HFSS and the VNA.

2.2.1. Frequency Domain Tools

HFSS is a simulation tool for 3D full-wave electromagnetic field simulation. It can extract parasitic parameters, visualize 3D electromagnetic fields (near and far-field) and

generate SPICE models that link to circuit simulations. It is mainly used to evaluate signal quality by looking at the transmission line path losses, reflection loss from impedance mismatches, parasitic coupling and radiation.

PowerSI is another simulation tool that provides a full-wave electrical analysis of integrated circuit packages and printed circuit board. A broad range of studies can be performed to identify issues such as trace to via coupling, power/ground bounce caused by simultaneously switching outputs, and identify design regions that are under or over voltage targets. It can evaluate the electromagnetic coupling between geometries to help enable better component placement. It can also extract parasitic parameters for package and board modeling, and perform what-if studies on a potential design scenario.

The differences between PowerSI and HFSS is that HFSS solves Maxwell's equation using tetrahedral meshing while PowerSI hand solves structures using circuit and electromagnetic analysis and combines them. Below are shown some trends that were found when these tools were compared. The main advantage of using PowerSI is that the time it takes to run a simulation is significantly less than HFSS. A two day simulation in HFSS can take around three hours in PowerSI. In this study, only HFSS was used as the simulation tool.

The last frequency measurement tool that was used is the VNA. The VNA is a measurement tool used to get network parameters of electrical networks. The most common use of a network analyzer is to find the s-parameters. A discussion of s-

parameters will be given in section 2.2.3. The basic architecture of a VNA is a signal generator, a test set, and one or more receivers. The signal generator is used to provide a test signal, the test set takes the output of the signal generator and sends it to the device under test, and lastly the receiver takes the measurements. In this work, the VNA was used on the manufactured board to obtain the S-parameters.

2.2.2. Frequency Domain Setup

In order to do the correlation, the experiments were imported into the 3D field solver, HFSS, and simulated with the board vendor recommended dielectric properties. The dielectric loss tangent was set to 0.025 and there was an airbox around the model which shorted all of the planes except for the power plane with an impedance of 377 ohms. The power planes were cut smaller so that the ground and the power would not be shorted together. The configuration of the ports setup in HFSS is shown in Figure 10. The first port is the input of the power plane, the second is the output of the power plane, then port 3 is the signal input port and concurrently, port 4 is the signal output port. HFSS takes this setup and generates the s-parameters. Similarly, in a VNA measurement, a probe is placed on each of four ports and the S-parameter waves are generated.

Figure 10: Port setup in HFSS.

S-parameters refer to the scattering matrix and are known as a mathematical construct that quantifies how radio-frequency (RF) energy propagates through a multi-port network. It allows the accurate description of properties of complicated networks as simple "black boxes." When an RF signal is inserted into one port, some of the signal bounces back out of that port, some of it goes into other ports and some of it disappears as heat or radiation. The S-matrix allows us to see each of the possible input-output paths. They are complex coefficients because both the magnitude and the phase of the input signal are changed due to the network. Overall, S-parameters describe the response of an N-port network to voltage signals at each port which easily helps the identification of signal integrity characteristics such as crosstalk, reflections, return loss, and insertion loss. They are also relatively easy to measure which makes them a desired matrix when looking at parasitic parameters. The

The other parameters, such as Z,Y, or ABCD parameters are not quite as helpful in indentifying signal integrity characteristics due to the way they are analyzed. They are

usually characterized by opening the circuit or shorting the circuit which may make the devices oscillate or self-destruct and makes them less desirable to work with. These parameters can be obtained by transforming the s-parameters and vice versa.

Examples of power return loss, signal return loss, power insertion loss, signal insertion loss, near-end crosstalk, and far-end crosstalk for Experiment 1, which is a 0.5 inch trace on layer 3, are shown in the following Figures 11-15. The first number in the subscript of the S-parameter refers to the responding port, while the second number refers to the incident port. For example, S_{21} means the response at port 2 is due to a signal on port 1.

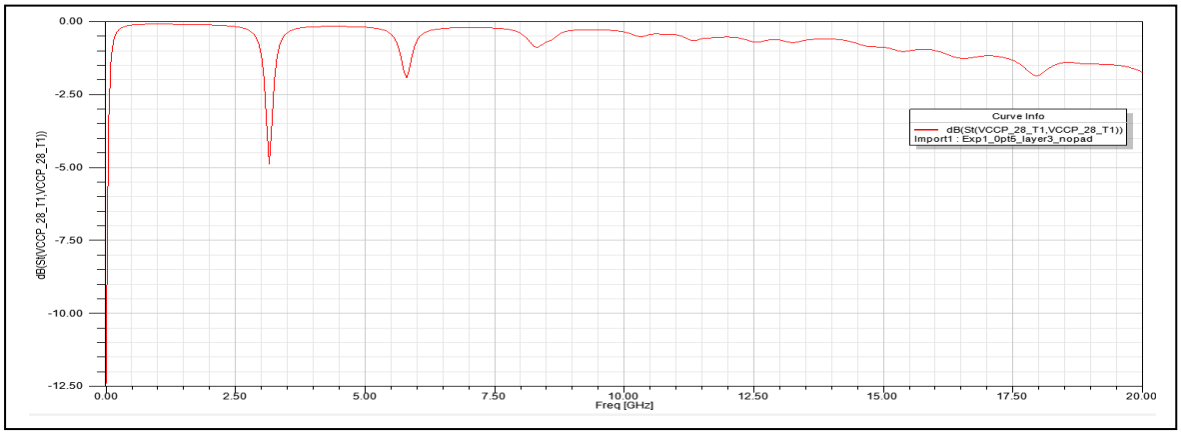

Figure 11: Power Return loss – Experiment 1 (S_{11})

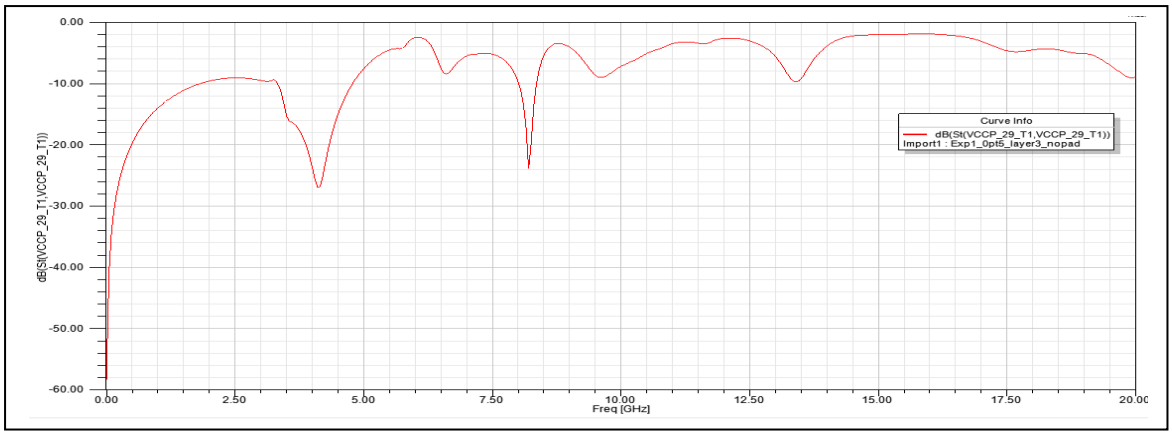

Figure 12: Signal Return loss – Experiment 1 (S_{22})

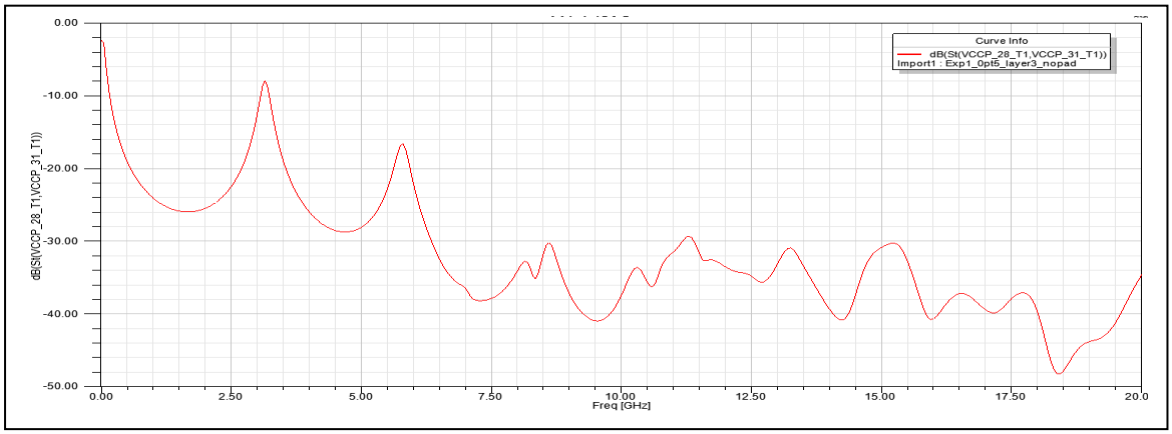

Figure 13: Power Insertion loss – Experiment 1 (S_{12})

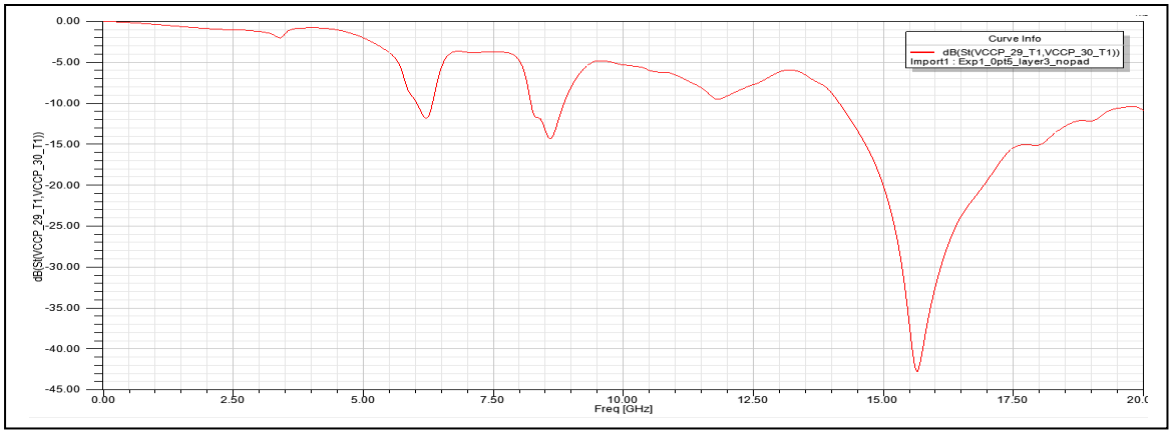

Figure 14: Signal Insertion loss – Experiment 1 (S_{34})

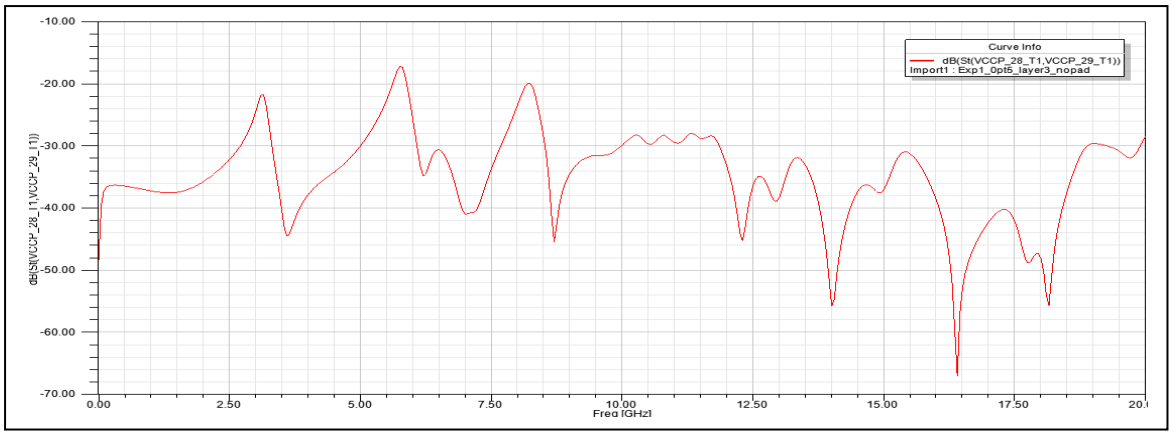

Figure 15: Near-end Crosstalk (NEXT) – Experiment 1 (S_{13} = S_{24})

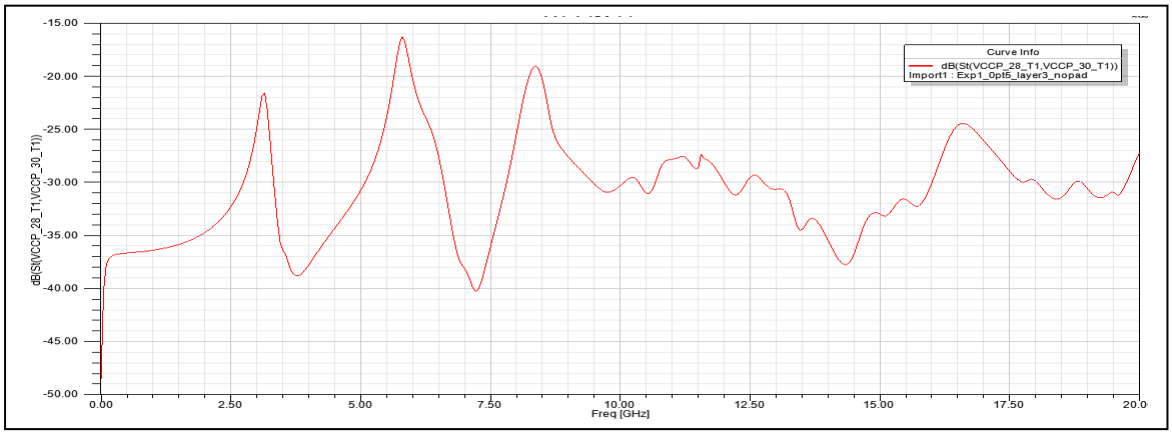

Figure 16: Far-end Crosstalk (FEXT) – Experiment 1 (S_{14} = S_{23})

2.2.3. Time Domain Simulation and Measurement Tools

The three time domain tools that were used were HSPICE, Broadband SPICE and a TDR. SPICE is a common circuit simulator used for a variety of applications. HSPICE can be used specifically for signal integrity purposes by generating the time domain crosstalk characteristics, and the loss. It is used primarily to check the integrity of circuit designs and to predict the circuit behavior. Broadband SPICE has the ability to create SPICE equivalent circuits from network parameters, specifically for this work, S-parameters were converted into circuit models. It is a tool used to bridge frequency and time domains by generating models for DC through broadband frequencies.

A TDR sends a small rise time pulse across the conductor or transmission line in this case, and if the line is terminated correctly, the pulse will be absorbed on the other side of the line. Otherwise, a part of the signal will be reflected toward the TDR due to impedance discontinuities. There are many uses for a TDR, but for this work, it was primarily used to find the impedance of a line in order to correctly terminate it in the time domain analysis.

2.2.4. Time Domain Setup

The first step in setting up the time domain configuration was to find the line impedances using the TDR so that those values can be used to terminate the transmission lines in HSPICE. The measurements of the 5 experiments are shown in Figures 17-20. The power plane refers to the path between Port 1 and Port 2 in Figure 10 while the signal path refers to the path between Port 3 and Port 4.

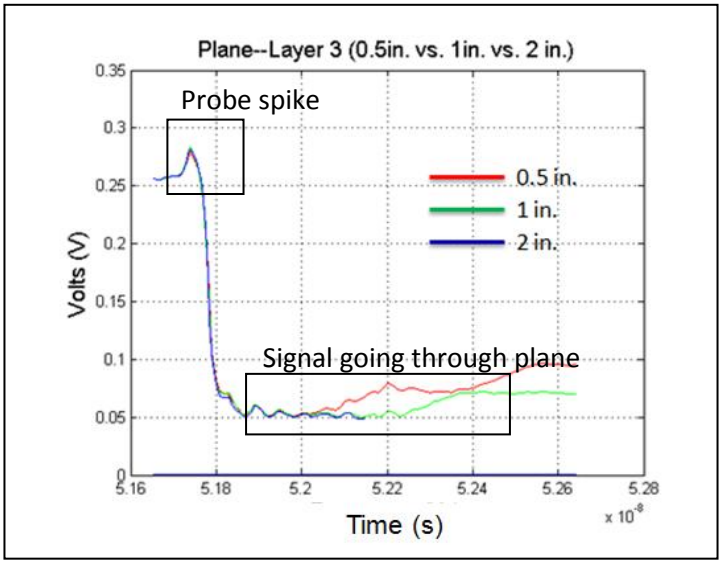

Figure 17: TDR measurements of Power plane path for Experiments 1, 3, 5.

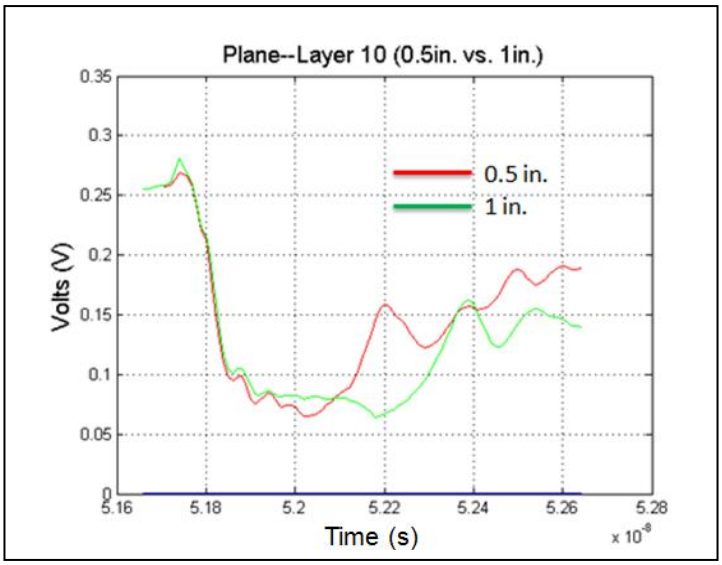

Figure 18: TDR measurements of Power plane path for Experiments 2 and 4.

The first spike shown in these graphs is due to the inductive spike from the probe, then, where it flattens out is where the signal is going through the power plane.

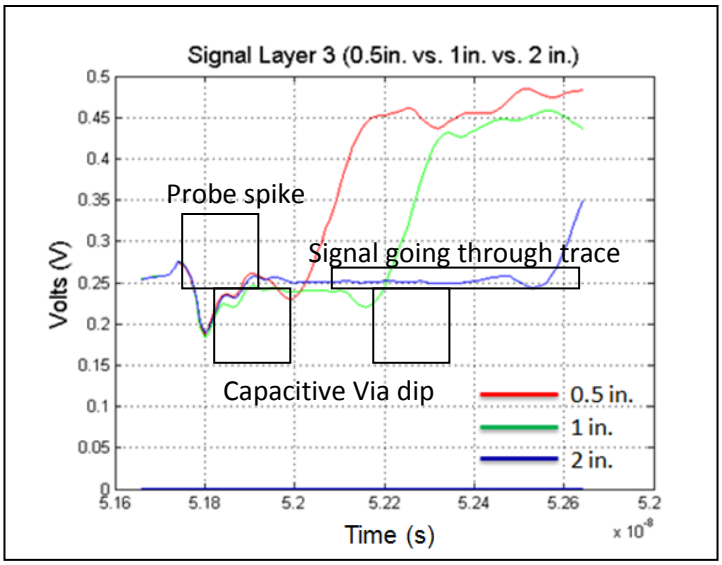

Figure 19: TDR measurements of Signal path for Experiments 1, 3, 5.

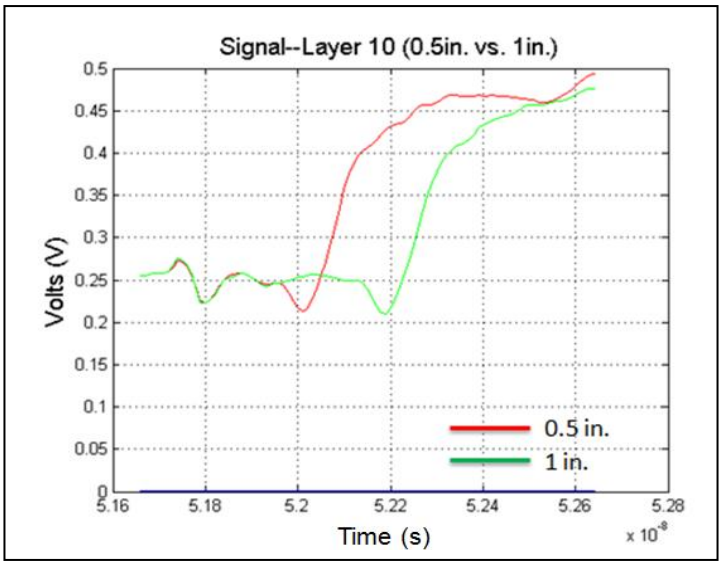

Figure 20: TDR Measurements of Signal path for Experiments 2 and 4.

The signal graphs again have the inductive spikes in the beginning, then a capacitive dip due to the vias. The flattening out occurs when the signal is going through the trace and then there is another capacitive dip when it is encountering another via on the other side and it ends with an open circuit formation. To get the impedance of the transmission line and of the power plane from these graphs, the following equations were used:

$$\rho = \frac{V_{reflected}}{V_{incident}} = \frac{Z_{load} - Z_o}{Z_{load} + Z_o} \qquad \text{Equation 1-1}$$

$$V_{reflected} = V_{measured} - V_{incident} \qquad \text{Equation 1-2}$$

$$Z_{load} = Z_o * \frac{1+\rho}{1-\rho} = Z_o * \frac{V_{measured}}{2V_{incident} - V_{measured}} \qquad \text{Equation 1-3}$$

From these equations we approximated that the matching impedance is 50 ohms for both the signal and the plane, so the following setup has this assumption. In order to

verify, the impedance graphs were also obtained from the TDR. Figures 21 to 24 are the corresponding graphs.

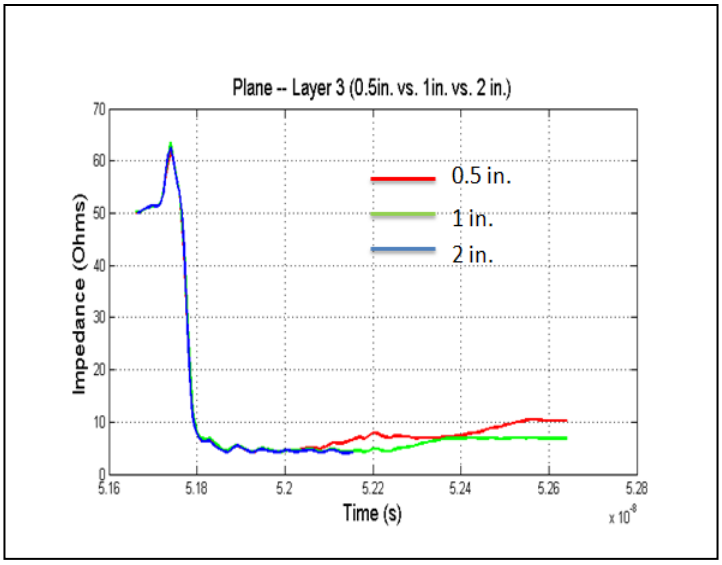

Figure 21: TDR measurements of Impedance for Power Plane in Experiments 1, 3, 5.

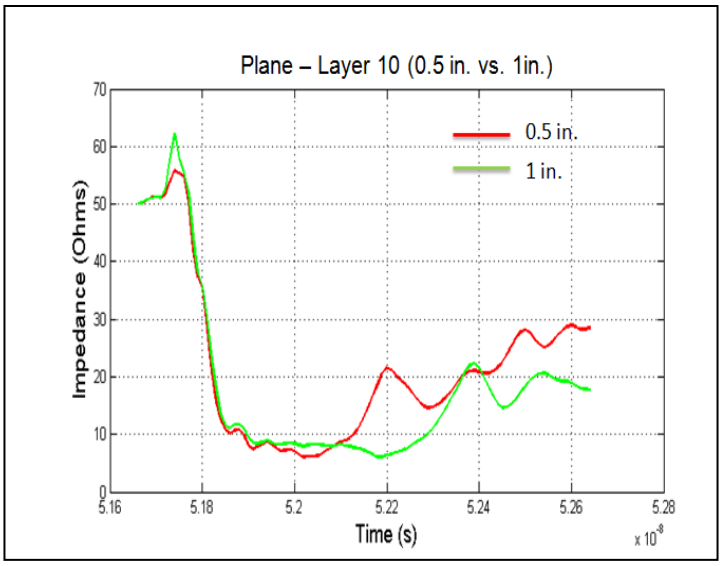

Figure 22: TDR measurements of Impedance for Power Plane in Experiments 2, and 4.

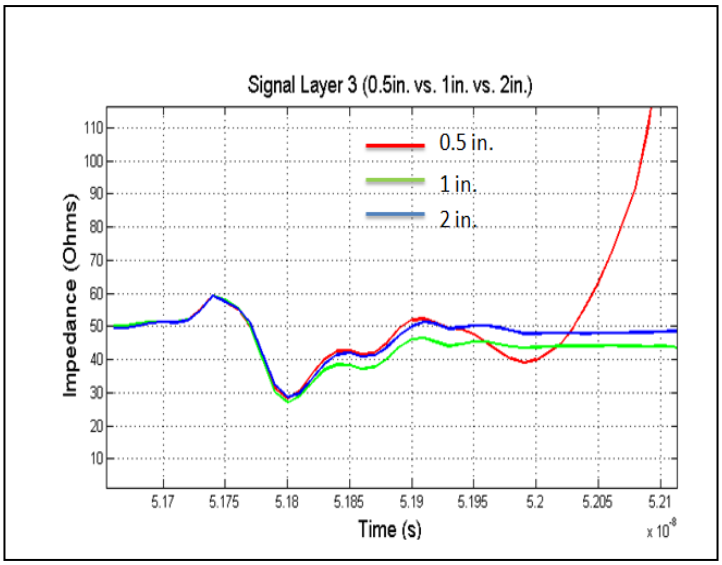

Figure 23: TDR measurements of Impedance for Signal layers in Experiments 1, 3, 5.

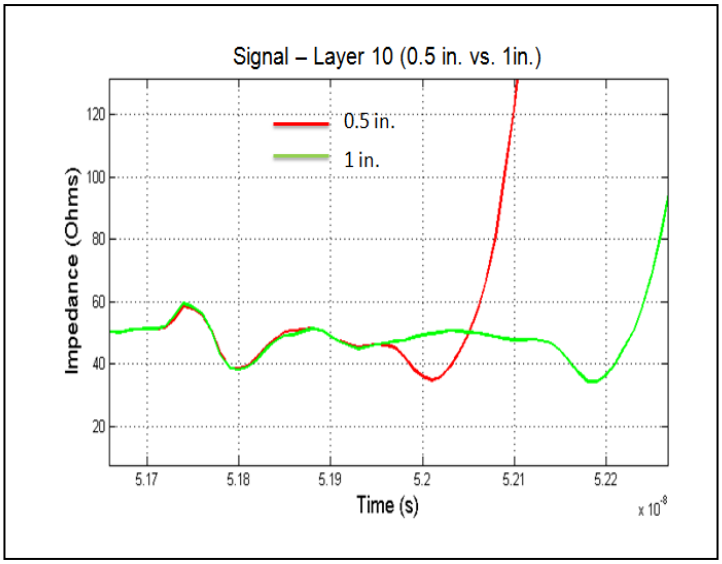

Figure 24: TDR measurements of Impedance for Signal layers in Experiments 2, and 4.

The extractions of time domain graphs, shown in the following sections, were obtained using the generated S-parameter touchstone files from HFSS. Then, Broadband SPICE was used to take the frequency domain characteristics generated by HFSS, and making them into circuit models (.inc files) that can be used in HSPICE. This circuit model is then used in HSPICE to generate the time domain loss and crosstalk. A power delivery

noise profile was inserted into the power plane of the circuit model to see the coupling effects onto the signals. The noise profile is shown in Figure 25 and was given by the power deliver team from their research on dual referenced noise coming from the circuit. The noise profile shows peak to peak values ranging in between 20 to 50mV centered on 1.49V. Fundamental frequency is in the 100MHz range. Figure 29 shows the setup used to obtain the time domain graphs in HSPICE. As mentioned earlier the noise profile is injected into the power plane, with the other ports quiet. The near and far-end nodes shown in Figure 26 are then probed.

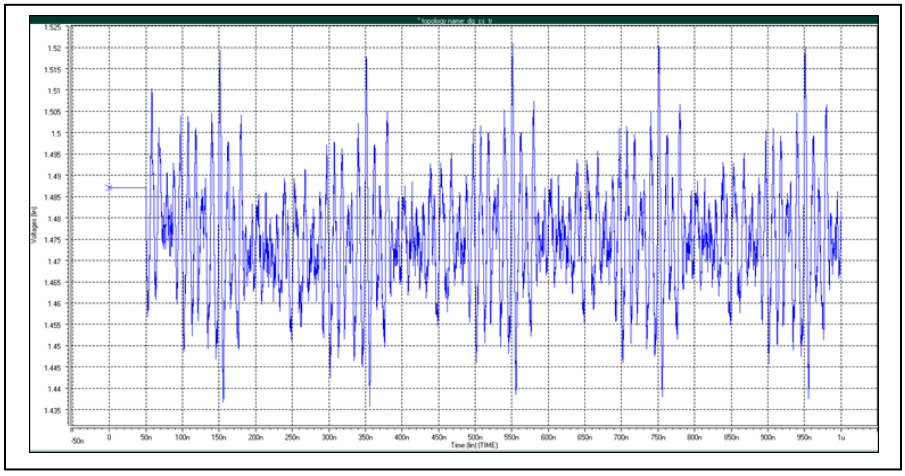

Figure 25: Noise Profile for Dual referenced board.

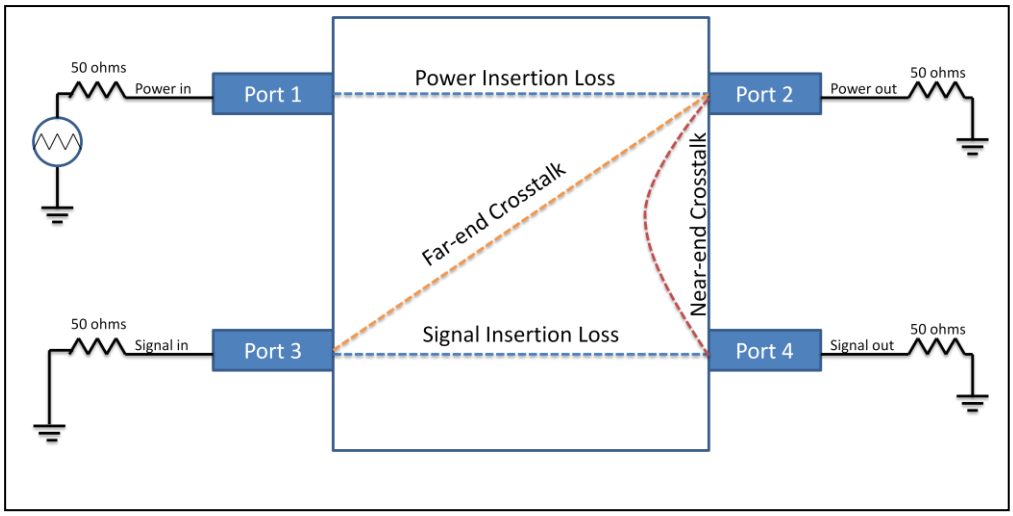

Figure 26: Time Domain Setup.

2.2.5. Simulation Tool vs. Measurement Tool Correlation

The main intention behind the correlation of the frequency domain tools was to see if the VNA measurements are comparable to the measurements from HFSS. The first 4 graphs are the S-parameter characteristics of Experiment 2in. Figures 27 to 30 with a 0.5 inch trace on signal layer 12. The last 4 graphs are the S-parameters characteristics of Experiment 3 of a 1 inch trace on layer 3. The setup of these experiments was shown in section 2.1. These graphs are just to provide the comparison between the three different tools, consequently, the loss graphs will be explained in more detail in the following sections.

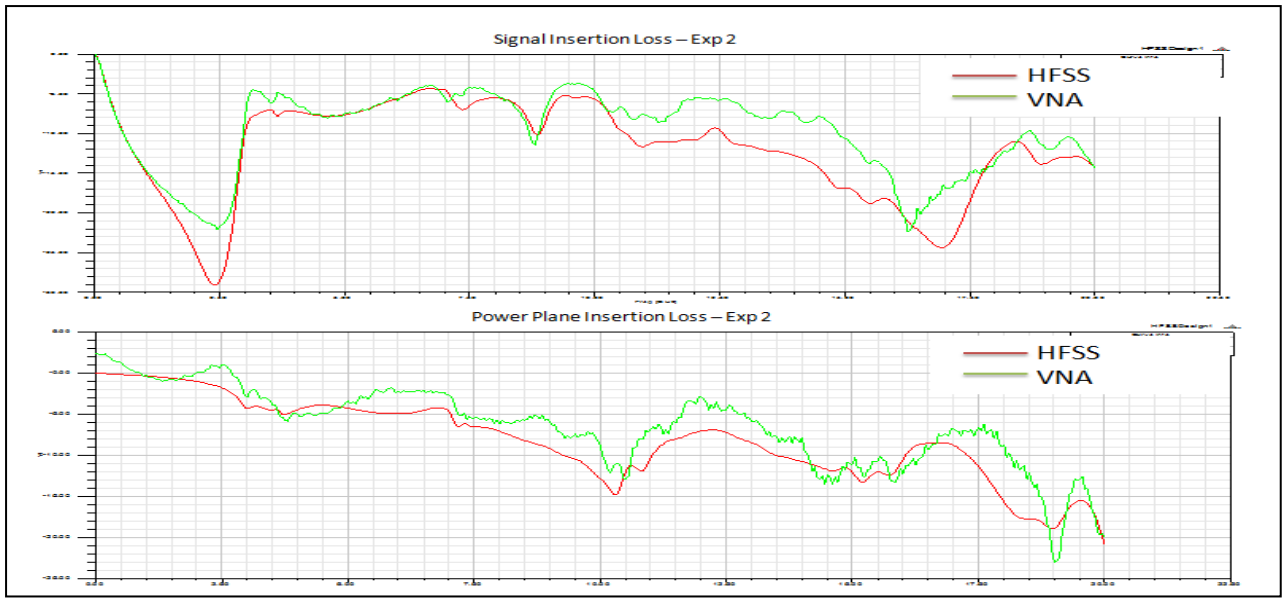

Figure 27: Insertion loss correlation for Experiment 2.

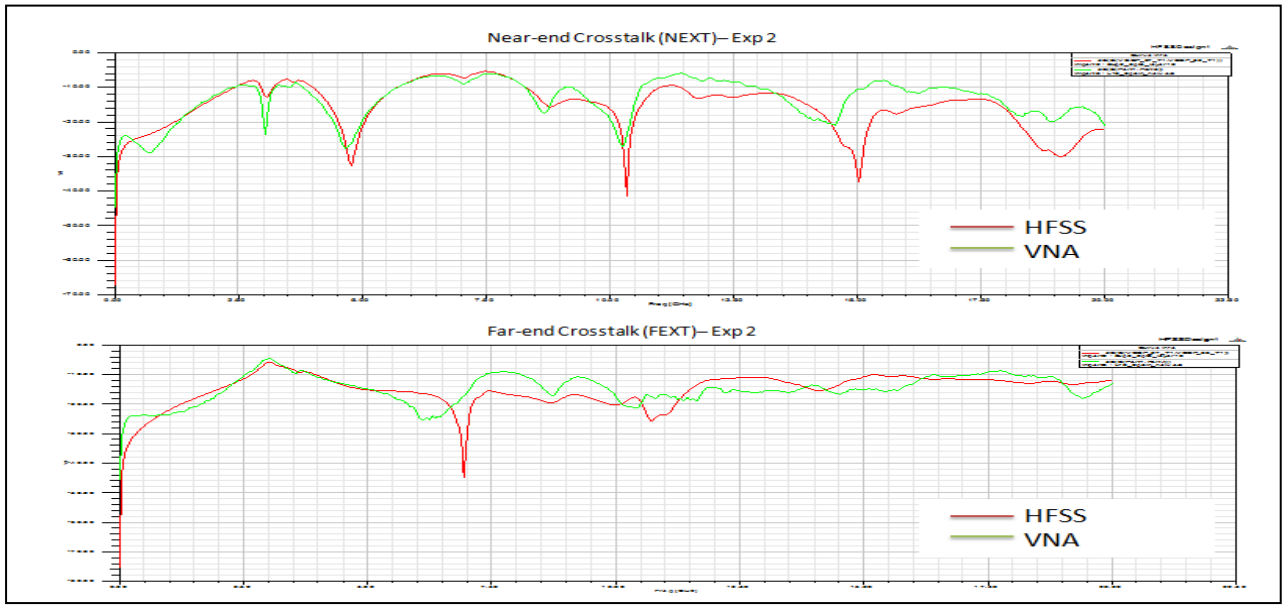

Figure 28: Crosstalk correlation for Experiment 2.

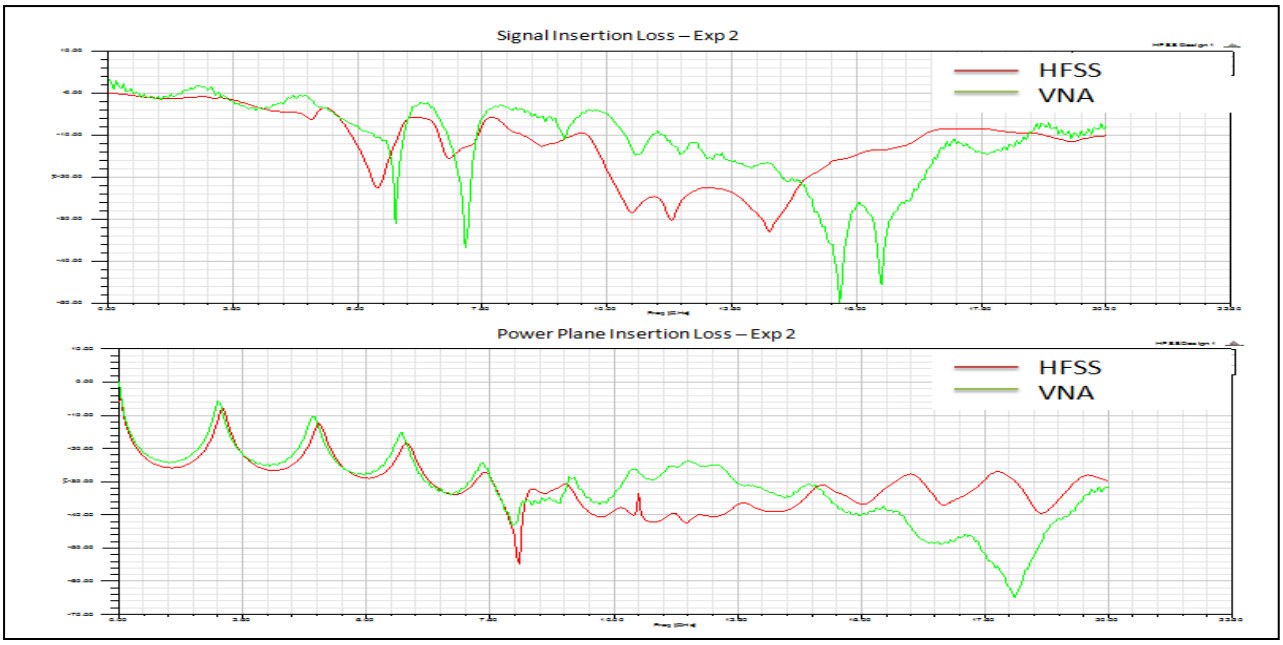

Figure 29: Insertion loss correlation for Experiment 3.

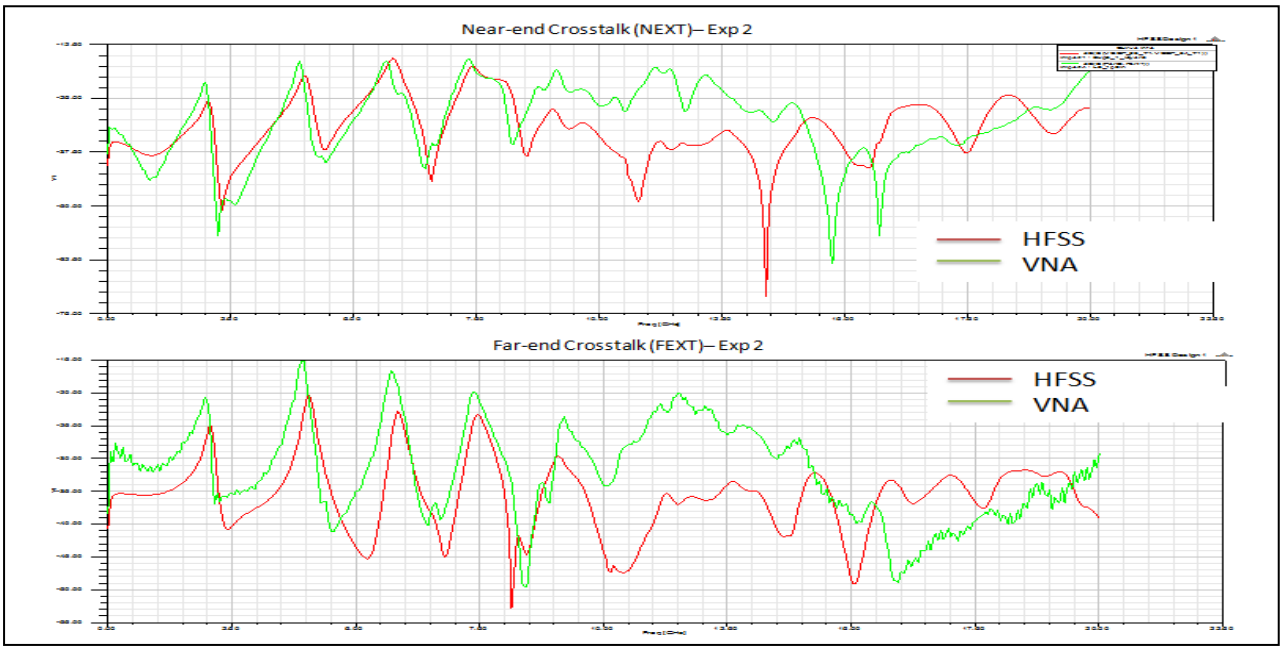

Figure 30: Crosstalk correlation for Experiment 3.

From these graphs, it is shown that for the most part HFSS correlates closely to the VNA measurements. Although the graphs are not exactly on top of each other, it is seen

that for the lower frequencies that HFSS can be used as a reliable simulation tool. The following experiments in subsequent sections contain results exclusively from HFSS.

Dual Referencing guidelines to minimize Power Deliver Noise coupling.

3. Experiments and Results

3.1. Noise Coupling Paths

The experiments in the noise coupling paths section were mainly to quantify the noise that occurs between the power plane and the signal trace and between the power via and signal via. It was also conducted to gain an understanding of the physics associated with noise coupling. In order to do this, the setup in Figure 31 was modeled in HFSS where the power vias simply terminate to the power plane (in red). This isolates coupling between the trace and the power plane as a result of the shortened via and it eliminates the coupling that could occur between the via and the trace. As the time domain results show in Figure 32, there is some coupling onto the trace. The coupling can only come from the plane to the trace because power and signal nets share the same ground return path.

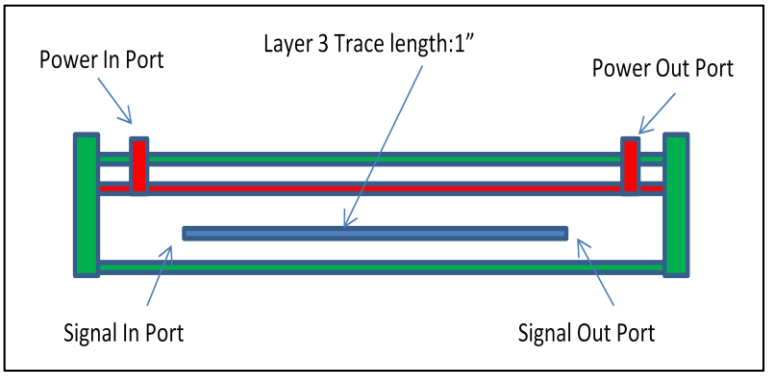

Figure 31: Power Plane to Trace/return path setup.

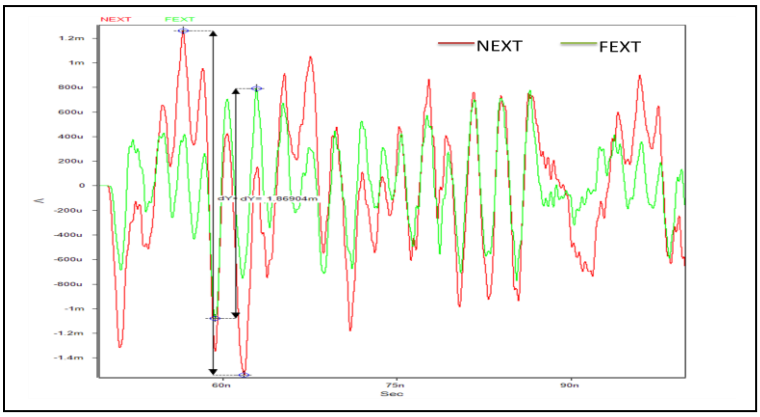

Figure 32: Power plane to trace and return path coupling.

This shows that in this case, near-end crosstalk is slightly larger than the far-end crosstalk and the coupling is in the mille-Volt range for the crosstalk between the power plane and the signal trace. More specifically, the near end crosstalk is approximately 2.2 mV while the far-end crosstalk is 1.9 mV. Another path for noise coupling is from power via to signal via. The structure shown in Figure 34 was modeled without any trace. Injecting the noise profile into the power via showed coupling onto the neighboring signal via and at the signal via that is one inch away. This is shown in Figure 33.

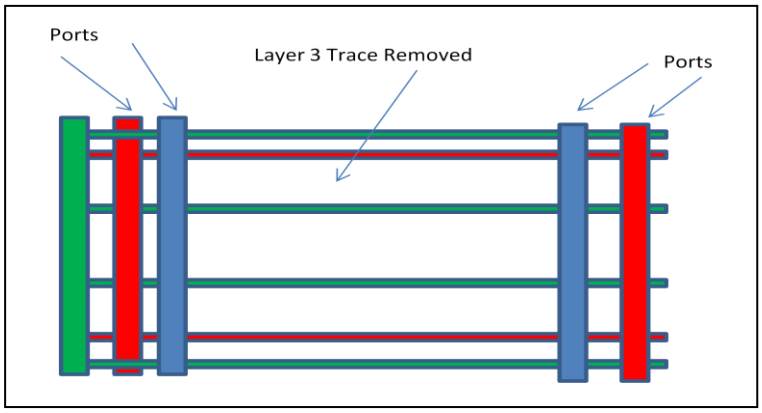

Figure 33: Via to via coupling setup.

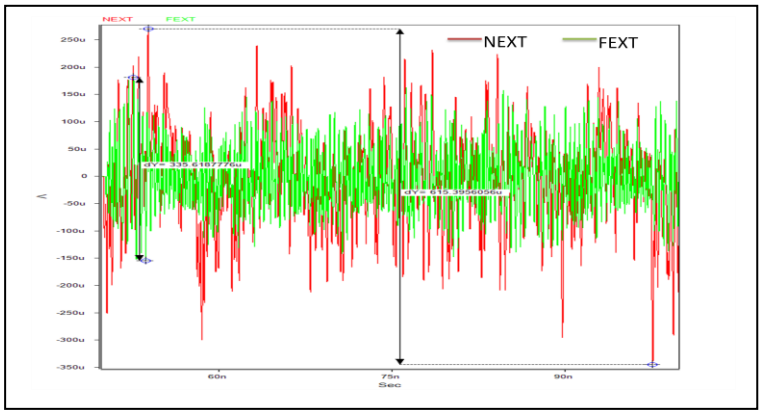

Figure 34: Power via to signal via coupling.

The time domain graphs shows that for this setup, the signal via to power via coupling is in the micro-Volt range. The near-end crosstalk shows about 615uV while the far end crosstalk shows 335uV. These results show that noise can be coupled from planes to traces, through the common return path and through via to via coupling. It would be erroneous to say via to via coupling is always smaller than coupling onto the trace because the magnitude of the coupled noise depends on the frequency content and magnitude of the noise. Frequency domain plots showing impact of noise coupling to signal nets will be shown in subsequent sections.

3.2. Trace vs. Via

In the next experiment, an HFSS model was manipulated to see the amount of coupling that occurs without a trace connecting the vias as shown in Figure 36. If the trace is not present, then obviously, it will not be contributing to the overall noise coupling and the emphasis will be on the contribution of the via. This experiment shows which contributes more to the overall noise coupling, the via or the trace. These two

setups are shown in Figures 35 to 38. Figures 35 and 36 are a top view of the HFSS model with and without a trace while Figures 37 and 38 are side views.

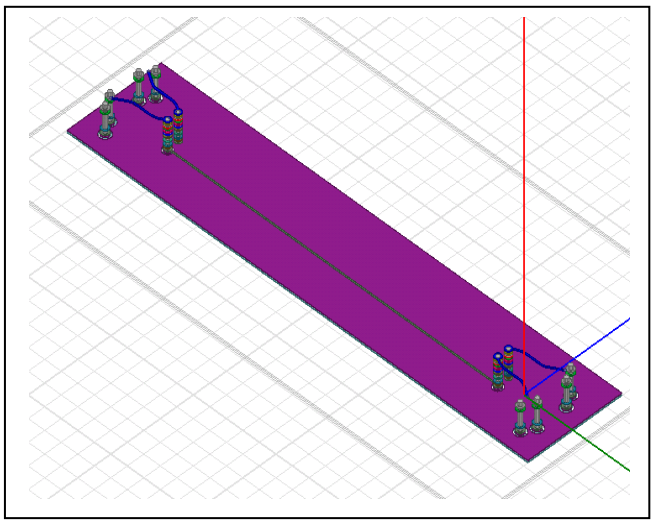

Figure 35: HFSS model with trace. (Top View)
(Top View)

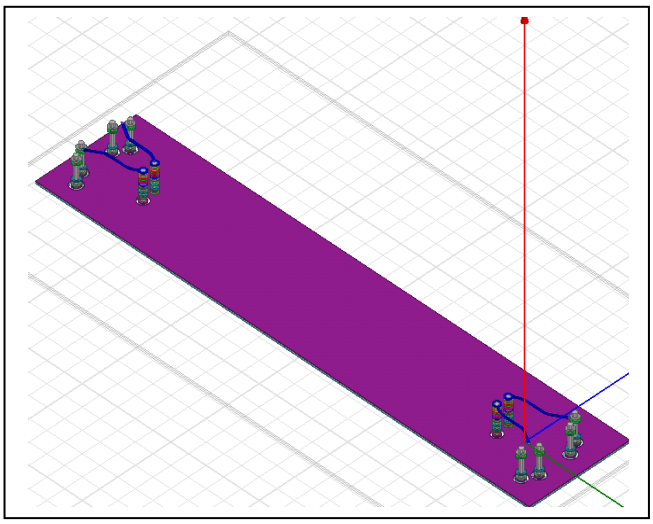

Figure 36: HFSS model without trace.

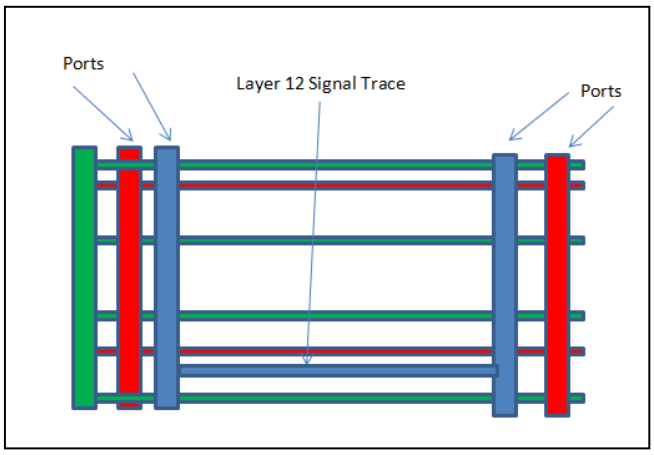

Figure 37: Side view with the signal trace.
trace.

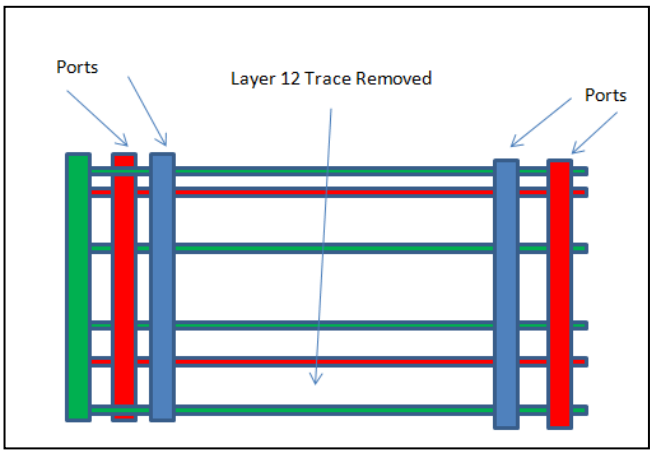

Figure 38: Side view without signal

Figure 39 and 40 show the near-end and far-end crosstalk comparison between the structure which has the trace and without the trace. The results show that the trace dominates crosstalk at low frequency, but as the frequency increases, NEXT for both

structures line up (via dominates). The same interpretation holds true for far-end crosstalk (FEXT).

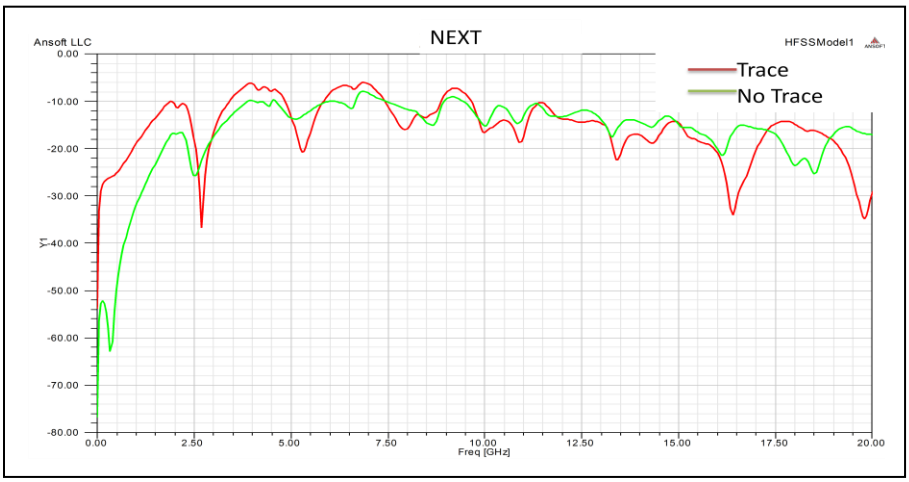

Figure 39: NEXT Frequency Response.

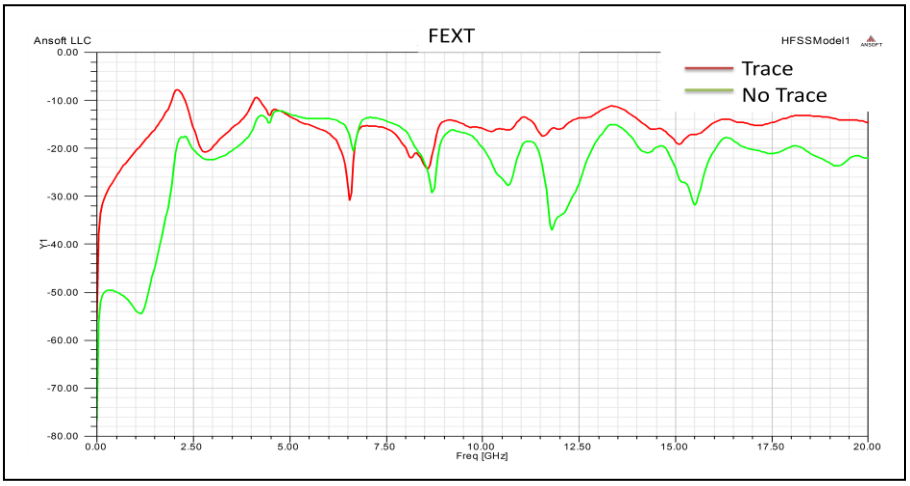

Figure 40: FEXT Frequency Response.

Simulating in the time domain shows that at the frequency of interests, which is in the 100MHz range, the structure with a trace shows much more NEXT and FEXT than the one without. The structure with a trace shows crosstalk in the milli-Volts range, while

the one without (only vias) is in the micro- Volts range. These are shown in Figures 41 and 42.

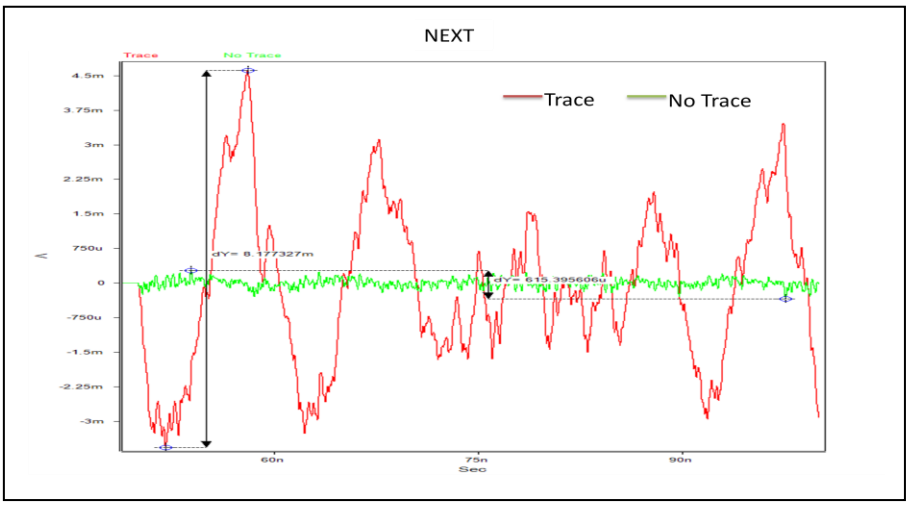

Figure 41: NEXT Time Domain.

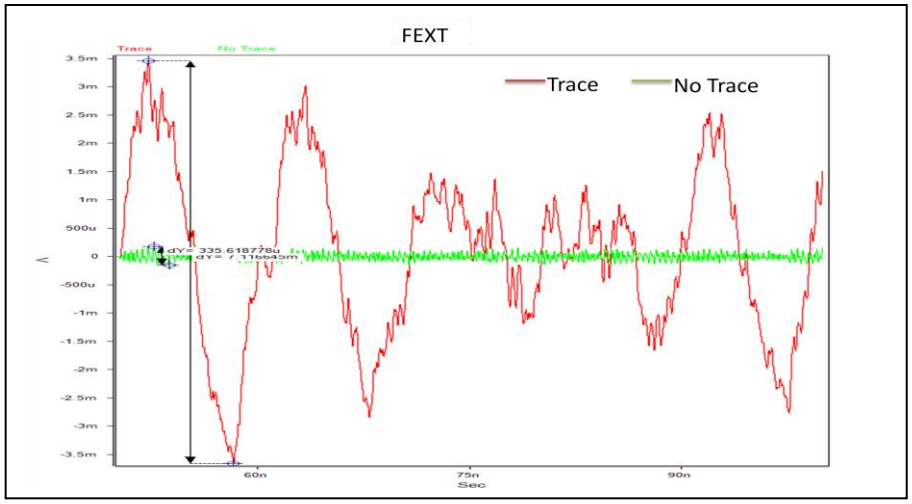

Figure 42: FEXT Time Domain.

The results from this study show that the impact of the trace is significant and it increases the coupling considerably especially in low frequencies. The via impact is small in the lower frequencies but come into play in the higher frequencies and sometimes surpass the trace impact.

3.3. Length Impact

The previous section showed that traces are important in power delivery noise coupling at low frequencies. This section focuses on the impact that trace lengths have on the amount of noise coupled in dual referenced environments. The configuration of the setup is shown in Figure 43 and these correspond to Experiments one, three, and five on the manufactured board discussed in Section 2.1.

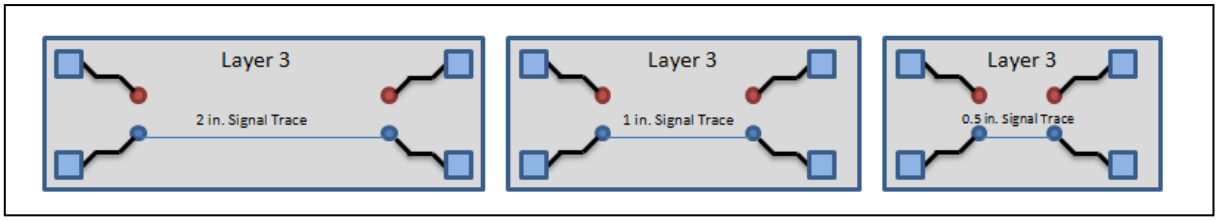

Figure 43: Length impact setup.

The HFSS frequency domain plots comparing the effects of trace length variation are shown in Figure 44 and 45 for NEXT and FEXT respectively for trace lengths of 0.5, 1 and 2 inches.

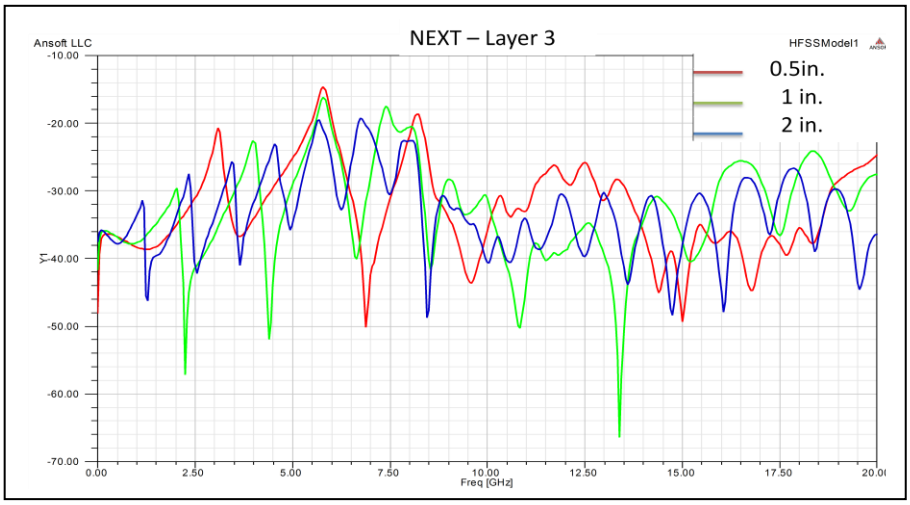

Figure 44: NEXT with varying lengths in frequency domain.

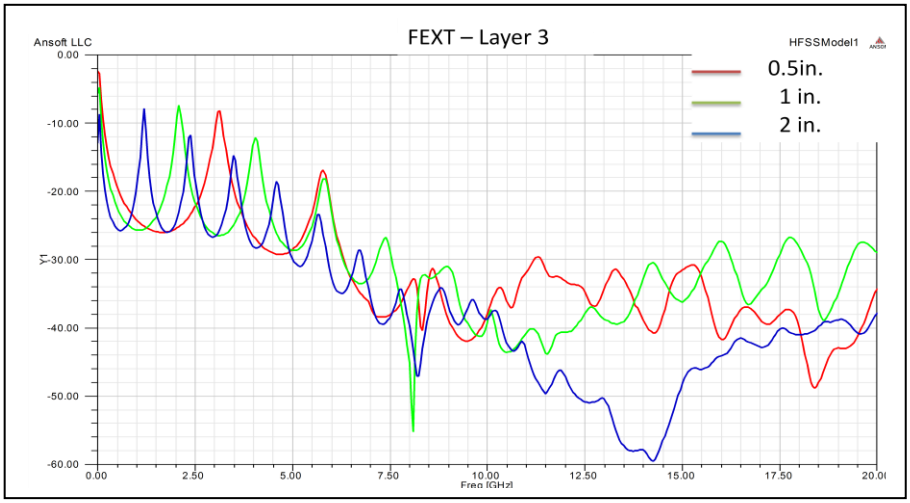

Figure 45: FEXT with varying lengths in frequency domain.

It can be observed from the plots that the resonance of the crosstalk increases as the trace length increases but the magnitude remains relatively the same except for in the high frequency range of the far-end crosstalk graph. The length impact comparison in the time domain is shown in Figure 46 and 47.

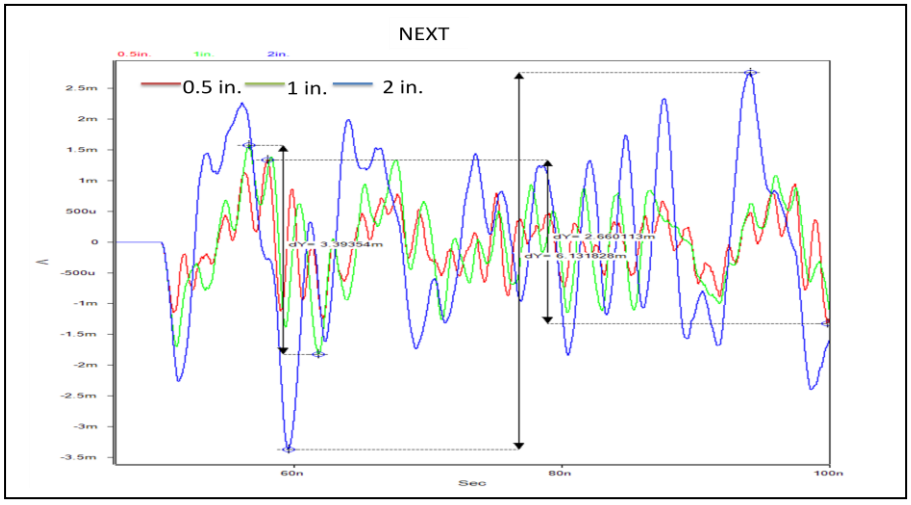

Figure 46: NEXT with varying layers in time domain.

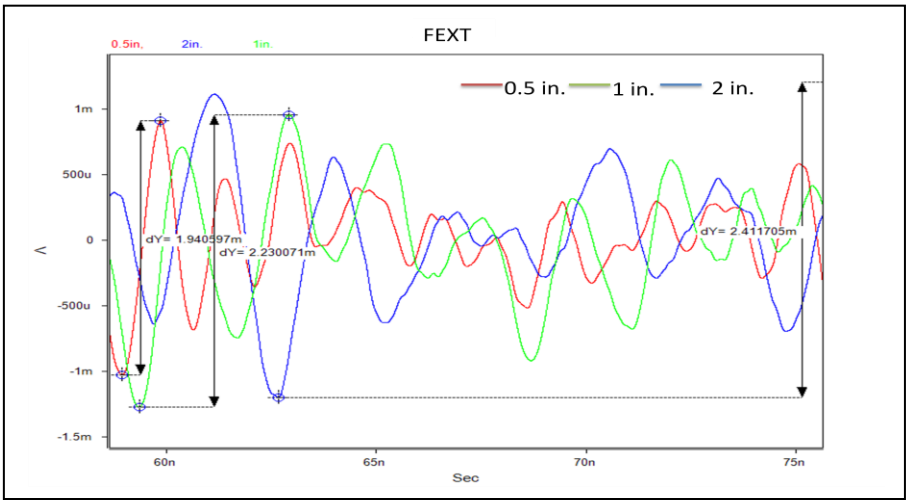

Figure 47: FEXT with varying layers in time domain.

Figure 46 shows that the NEXT increases with increasing trace lengths with the 2 inch trace having the largest peak amplitude. Figure 47 shows that the FEXT magnitude is similar to each other, but follows the same trend as the NEXT plot showing that overall the crosstalk increases with increasing trace lengths. These results agree with the general trends of increased length giving increased crosstalk. However, crosstalk will not increase infinitely with length because loss sets in. To sum up this section, the results show that shorter lengths are preferable when using dual referencing.

3.4. Layer Impact (Via stub Impact)

Via stubs refer to the length of the signal via from the signal trace layer to the last layer. Long via stubs are normally frowned upon in signal integrity because they like to radiate like antennas. A picture of a via stub is demonstrated in Figure 48 where the length of the via is from the bottom of the signal trace to the bottom of the board. At their resonance frequencies, most of their energy flows into the planes if there is no

adequate return path [1]. The worst case stubs in the experiments will be the cases with signal traces on layer 3. Since we know that the board thickness is 62 mils, it is used as the largest length that a stub can be in these experiments. Using [1], it was found that for a 62 mil stub, the resonance frequency is around 12GHz. Thus, at 12GHz, the stub will dump most of its energy into the plane which can be picked up by other vias close by. Since our frequency of interest is around 100MHz, long via stubs can be an advantage.

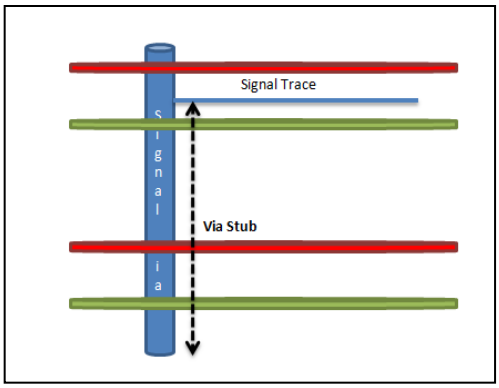

Figure 48: Example of a via stub.

The purpose of this section is to analyze how the via stub lengths effect the magnitude of the coupling. Experiments 3 and 4 from Section 3.1, with the side view shown in Figure 49, compare the coupling of vias transitioning to layer 3 (long stub) to vias transitioning to layer 12 (short stub) These experiments use the same trace length but are on different layers.

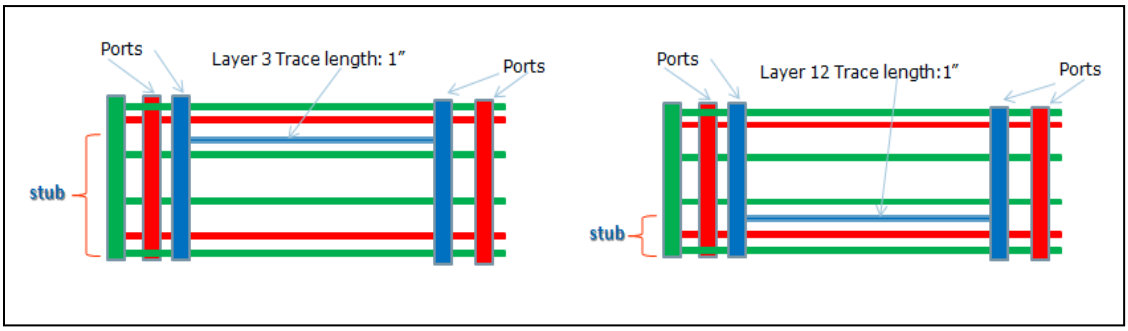

Figure 49: Side view of experiments used.

Figure 50 shows frequency domain NEXT comparison between layer 3 and layer 12. It can be observed that the short stub case shows more coupling; an average of 20dB difference. The same is true for the FEXT comparison in Figure 51.

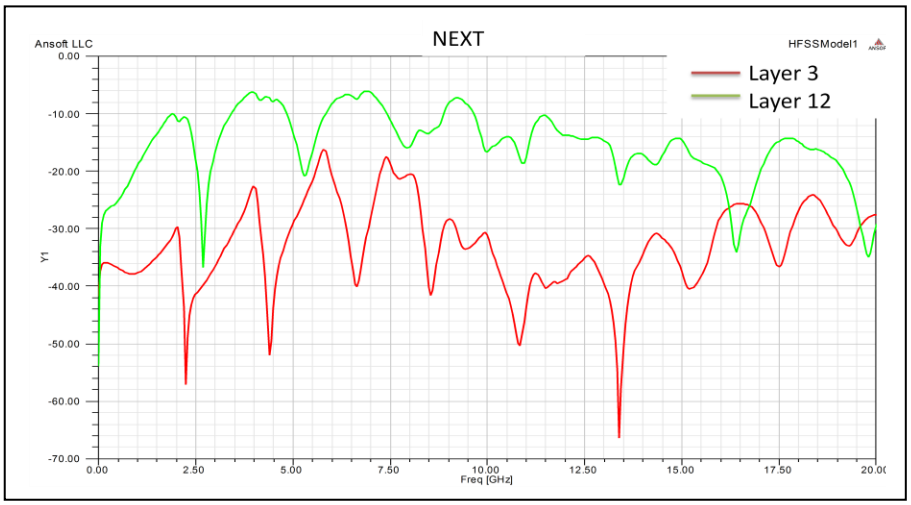

Figure 50: NEXT comparing layers.

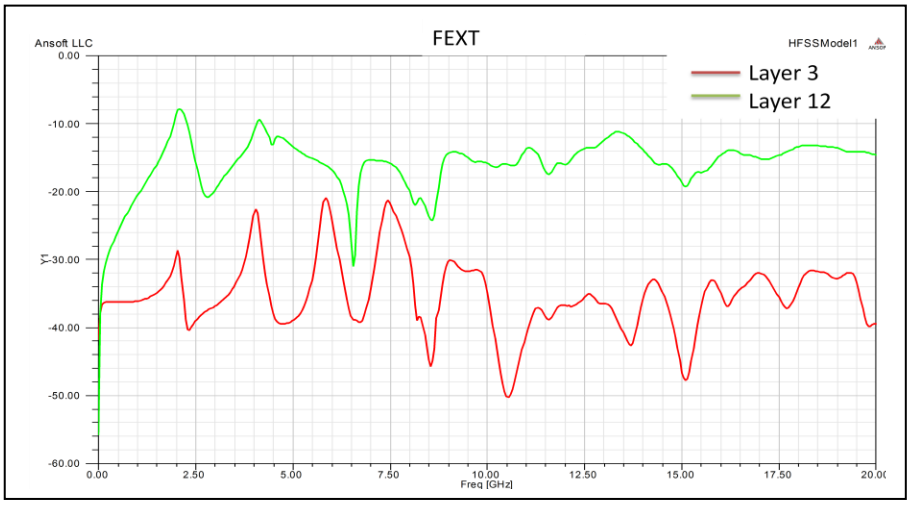

Figure 51: FEXT comparing layers.

In the time domain NEXT and FEXT plots in Figure 52 and 53, respectively, confirm the frequency domain results. The short stub shows more coupling than the long stub scenario. This finding can be explained; as the noise travels down the via, a magnetic field is created around the via which couples to the neighboring signal via. The longer the barrel, the more coupling on to the signal net is observed. In other words, layer 3 experiences smaller crosstalk than layer 12 because of its lower via barrel to barrel coupling.

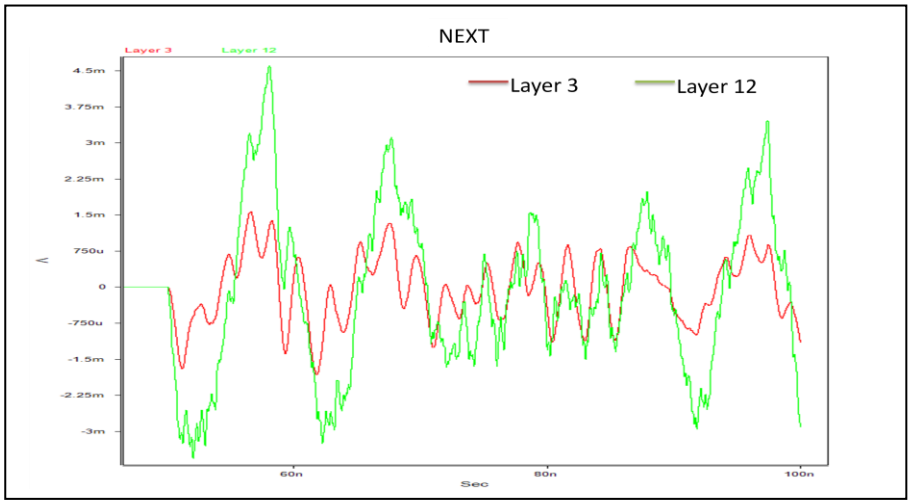

Figure 52: NEXT comparing layers.

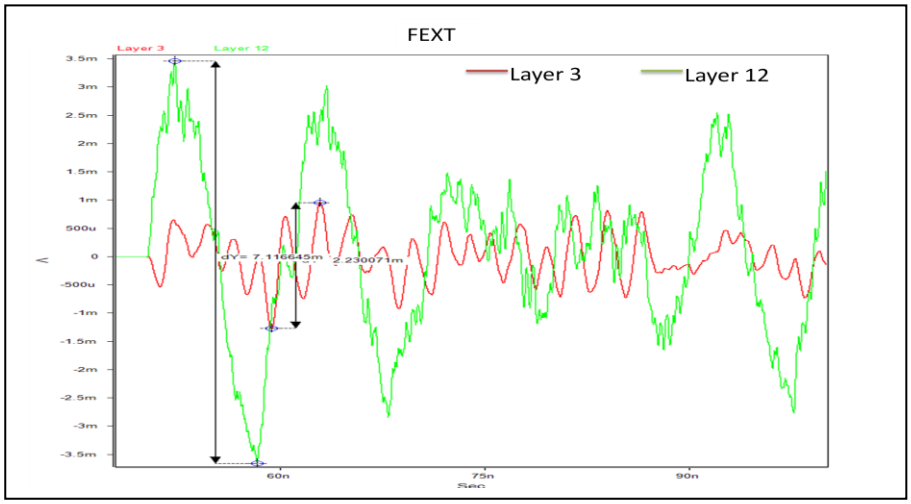

Figure 53: FEXT comparing layers.

This implies that if dual referencing is considered, routing on the top half of the board (layer 3) should be strongly considered, given that the resonant frequency is not close to the frequency of interest. In this frequency range, magnetic coupling from the long barrels (layer 12) dominates the energy dumped into the cavity from the longer stub (layer 3).

3.5. Asymmetric vs. Symmetric Routing

This last section explores the possibility of routing a signal trace closer to the ground plane so that less power noise from the power plane in a dual referenced board can be minimized. The setup of the experiment is shown in Figure 54, where the one on the left is the symmetric case and the one on the right is the asymmetric case.

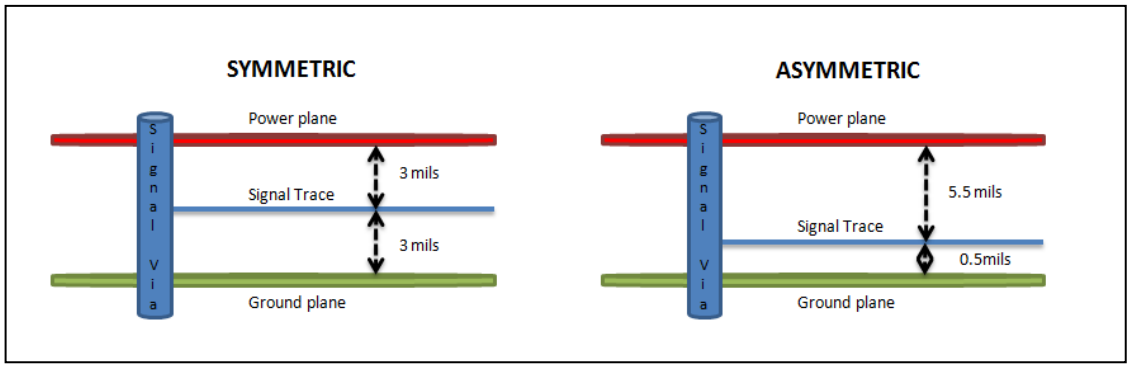

Figure 54: Symmetric vs. Asymmetric Setup.

The NEXT and FEXT of these configurations in frequency domain are shown in Figures 55 and 56. It can be seen that they match up pretty closely in the frequency domain. For the near-end crosstalk in the lower frequencies, the symmetric configuration seems to be slightly smaller but in the higher frequencies, the asymmetric coupling begins to faintly overtake the symmetric.

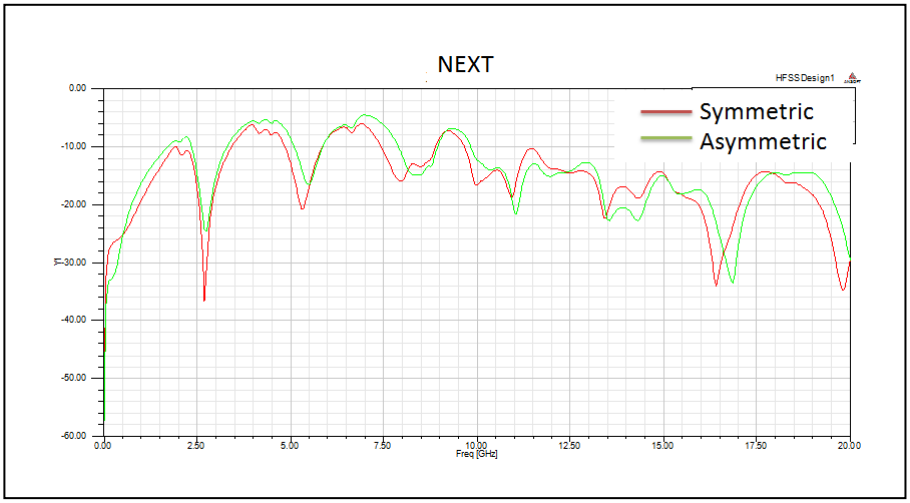

Figure 55: NEXT frequency domain of Symmetric vs. Asymmetric.

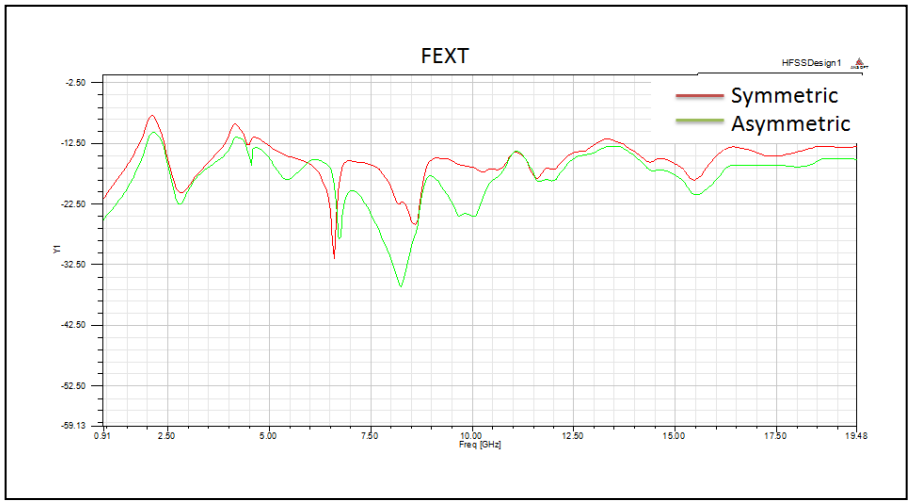

Figure 56: FEXT frequency domain of Symmetric vs. Asymmetric.

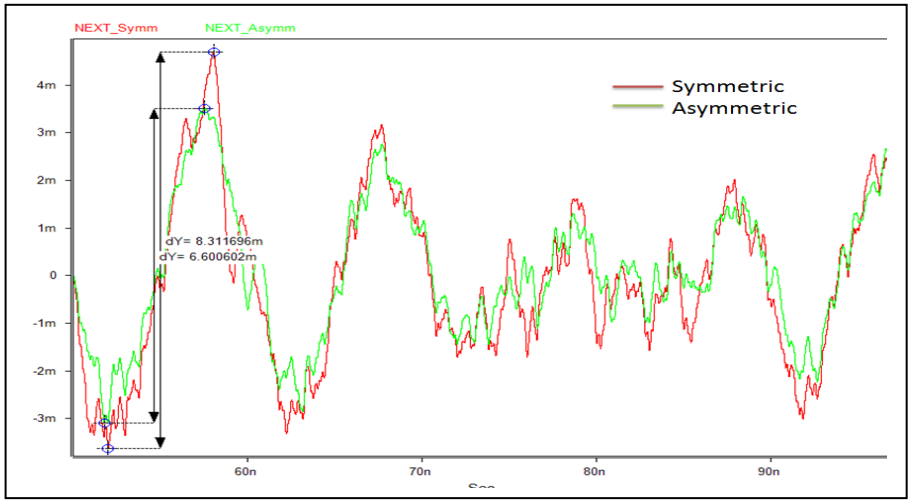

Figure 57: NEXT time domain of Symmetric vs. Asymmetric.

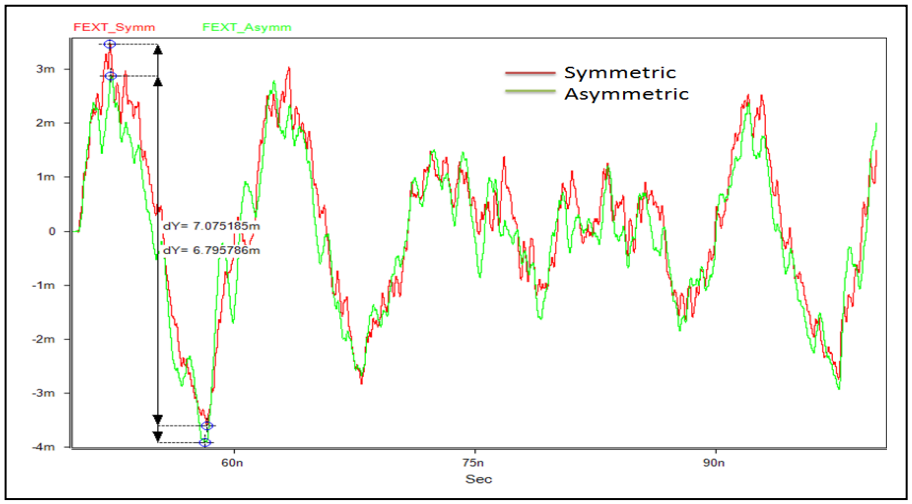

Figure 58: FEXT time domain of Symmetric vs. Asymmetric.

The time domain graphs shown in Figure 57 and 58 correspond with the frequency domain graphs showing that the asymmetric configuration has slightly less coupling but not enough to recommend asymmetric routing. If there is a need to slightly decrease the coupling, then this could be an option but the line impedance changes when the signal trace is moved closer to the ground plane. The equation for impedance is given by the following:

$$Z_o = \sqrt{\frac{L}{C}}$$ Equation 1-4 [1]

As the signal trace is moved closer to the ground plane, the capacitance increases and the impedance decreases. Due to this fact, the matching impedance for the line needs to change so that reflections don't become an added problem. When the matched impedance is forced to decrease to compensate for the decreased line impedance, more power will be burned through the matched resistance which creates another area of concern. Due to these consequences, routing a signal trace asymmetrically is not advised.

4. Conclusion and Next Steps

A comprehensive study of power delivery noise coupling onto signal nets when dual referencing is utilized has been presented. The avenues for noise coupling include via to via, plane to trace and common return path coupling. One important conclusion that was drawn from deriving where most of the coupling takes place is that trace coupling dominates in lower frequencies and via coupling catches up and sometimes overtakes trace coupling in higher frequencies. To mitigate the amount of noise impact a few guidelines can be followed. To reduce via crosstalk, routing on the top half of the board is recommended. Shorter routing lengths are also preferred as they reduce the amount of noise coupling. Routing asymmetrically can give you a little bit of margin when looking at crosstalk but not enough to significantly impact the overall coupling. Shown below is a table summarizing the results found from the experiments conducted.

Table 1-1 : Experimental Results

Question	Experiment	Result
How is the noise quantified in the different noise avenues?	Noise Coupling Paths (Sec. 3.1)	Plane to via coupling in milli-Volt range. Via to via coupling in micro-Volt range.
Does the trace or the via dominate in coupling?	Trace vs. Via (Sec. 3.2)	The trace dominates in the lower frequencies and the via coupling catches up in higher frequencies.
Does the length of the trace effect the coupling?	Length Variation (Sec 3.3)	As the length of the trace increases, so does the coupling.
Does routing on different layers effect the coupling?	Layer Variation (Section 3.4)	The higher signal layers have less coupling than the lower.
Does an asymmetric stack-up have less coupling?	Asymmetric vs. Symmetric (Sec. 3.5)	Only by a little bit, but it has other implications.

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