AN ABSTRACT OF THE THESIS OF

Srinivas V. Pattamatta for the degree of Master of Science in Electrical and Computer Engineering presented on June 7, 1994.

Title: Switched-Current Circuits for a Bandpass Delta-Sigma Modulator.

Abstract approved: Redacted for Privacy

Richard Schreier

Delta-sigma data converters have gained popularity in analog-to-digital converters due to their simplicity, high linearity and tolerance to circuit imperfections. In addition, the anti-alias filter is simplified by the use of oversampling. Bandpass conversion in delta-sigma is well suited for high frequency narrow-band signals in systems such as radio receivers, cellular communication and spectrum analyzers. Switched-Current (SI) circuits are faster than conventional Switched-Capacitor (SC) circuits. Furthermore, SI circuits are compatible with standard digital processes whereas SC circuits require special processes incorporating linear capacitors.

The basis of this thesis is the first implementation of the primary building blocks for a switched-current bandpass modulator. The advantage of the regulated cascode current copier over other current memory cells is demonstrated clearly in the process. The other necessary parts of the modulator are designed and simulated. All the blocks needed for the modulator are implemented in a 1.2μm CMOS N-Well technology. The test results of the fabricated individual devices indicate that the construction of an SI bandpass modulator is feasible, provided charge-injection is adequately addressed.

Switched-Current Circuits for a Bandpass Delta-Sigma Modulator

by

Srinivas V. Pattamatta

A THESIS
submitted to
Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Completed June 7, 1994
Commencement June 1995

APPROVED:

Redacted for Privacy

Professor of Electrical & Computer Engineering in charge of major

Redacted for Privacy

Head of Department of Electrical & Computer Engineering

Redacted for Privacy

Dean of Graduate School

Date thesis is presented June 7, 1994

Typed by Srinivas V. Pattamatta

ACKNOWLEDGEMENTS

Thanks to my parents and brother for their love and support.

I am grateful to my advisor Dr. Richard Schreier for the interest he created in me for the subject. This work is the result of his tireless efforts, helpful advice and guidance. His constant encouragement has helped me in the completion of my work.

I would like to thank Dr. John Kenney, Dr. Shih-Lien Lu and Dr. John Chen for taking time out of their busy schedules to serve on my graduate committee.

Special thanks to Praveen Manapragada for helping with the design of the DACs and Charlie Chairatanatrai for putting up the padframe.

Thanks to the others in BPDS group: Brian Misek, Colin Kuskie, Sanjeev Joshi, Bo Zhang, Sridhar Jasti, Shivani Gupta and George Corrigan for their positive comments.

Others who made my stay enjoyable and kept me (in)sane: Ravi Ramachandran, Sridhar Kotikalapoodi, Manoj Kumar, Shankar Pennathur, Satish Kulkarni and Ashutosh Kale.

TABLE OF CONTENTS

Chapter 1. INTRODUCTION

1.1 Motivation 1

1.2 Outline of the Thesis 2

Chapter 2. BACKGROUND

2.1 A Word About Delta-Sigma 3

2.2 Bandpass Delta-Sigma Data Converters 6

2.3 Why Switched-Current? 8

2.4 The Modulator 11

2.5 Resonator 14

2.6 Previous Work 16

2.7 Summary 16

Chapter 3. DESIGN AND LAYOUT

3.1 SI8: The Eighth-Order Bandpass Delta-Sigma Modulator. 18

3.2 Regulated Cascode Current Copier - RC^3 19

3.3 Voltage Comparator 36

3.4 The Digital-to-Analog Converter (DAC) 37

3.5 Clock Circuit 42

3.6 SI2: The Second Order Modulator. 45

Chapter 4. TESTING

4.1 Current Source 48

4.2 Digital-to-Analog Converter 49

4.3 Comparator 51

4.4 Clock Circuit 51

4.5 The Current Memory Cell: RC^3 53

4.6 Reson 55

Chapter 5. CONCLUSIONS

5.1 Summary 59

5.2 Future Work 60

BIBILIOGRAPHY 61

APPENDIX 63

LIST OF FIGURES

Figure 2.1: A first-order delta-sigma analog to digital converter. 3

Figure 2.2: A general delta-sigma modulator. Note that there is a unit delay in the feedback since is required to be strictly causal. 5

Figure 2.3: A bandpass modulator based A/D converter. 6

Figure 2.4: Comparison of radio receivers using bandpass $\Delta\Sigma$ and a zero IF with lowpass $\Delta\Sigma$ 7

Figure 2.5: A conceptual bandpass noise shaping feedback loop 8

Figure 2.6: MOS current memory cells. 9

Figure 2.7: The regulated cascode current copier. 10

Figure 2.8: The block diagram of the eighth-order bandpass modulator 12

Figure 2.9: An FFT of the output of the modulator. 12

Figure 2.10: The SNR curve for the modulator of Figure 2.8, when operated with an over-sampling ratio of 64. 13

Figure 2.11: The single-ended resonator block, RESON, and its clock signals 15

Figure 3.1: Block diagram of the scaled SI8 18

Figure 3.2: Regulated cascode current copier. 20

Figure 3.3: Small signal model of RC^3 for the calculation of settling time. 21

Figure 3.4: Settling behavior using HSPICE and MATLAB. 23

Figure 3.5: Configuration for measuring the input impedance. 24

Figure 3.6: Circuit for measuring output impedance. 25

Figure 3.7: Modified regulated cascode current copier. 26

Figure 3.8: Layout of RCTH 28

Figure 3.9: Transistor schematic and block diagram of the Ib1=1.5mA current source, with the biasing arrangement. 29

Figure 3.10: Layout of the 1.5mA current source 30

Figure 3.11: RC^3 for producing coefficients. 32

Figure 3.12: Output of the resonator at input of 25MHz and clocked at 100MHz. 33

Figure 3.13: Layout of RC^3. 34

Figure 3.14: Layout of the resonator 35

Figure 3.15: The voltage comparator. 36

Figure 3.16: Comparator output for a 100MHz clock. 37

Figure 3.17: The basic architecture of the DAC. 38
Figure 3.18: Transistor schematic biasing of the current source I for the DACs. 39
Figure 3.19: Transistor schematic of current sink 2I and its bias circuit. 40
Figure 3.20: Output waveforms of the DACs. 41
Figure 3.21: Logic for the three phase clock generation. 42
Figure 3.22: Logic for generation of track and output phases. 43
Figure 3.23: Waveforms of the clock circuit. 44
Figure 3.24: The merged resonator-comparator and feedback circuitry for a second-order bandpass modulator. 46
Figure 3.25: Simulation of SI2 using mixed ideal/real components 47
Figure 4.1: Test setup for 1.5mA current source. 48
Figure 4.2: Graph for measuring the output impedance of the current source 49
Figure 4.3: Test setup for the 516mA DAC 50
Figure 4.4: Graph for measuring output impedance of 516mA DAC. 50
Figure 4.5: Output of the DAC under test at a speed of 1MHz. 51
Figure 4.6: Output of the comparator under test. 52
Figure 4.7: Output impedance of RC^3. 53
Figure 4.8: Output of RC3 for a 0.125MHz sine wave clocked at 4MHz. 54
Figure 4.9: Test setup for measuring charge injection in RC^3 54
Figure 4.10: Signal-dependant charge injection for the current copier. 55
Figure 4.11: Adding a resistor to the input of the resonator. 56
Figure 4.12: Output waveform of the resonator under test 57
Figure 4.13: Decrease in output impedance due to the erroneous scaling method. 58

LIST OF TABLES

Table 3.1: Specifications for RC^3 19
Table 3.2: Value of the Capacitances 22
Table 3.3: Transistor sizes for Ib1. 29
Table 3.4: Transistor sizes for current source I of the DACs. 38
Table 3.5: Transistor sizes for current sink 2I of the DACs. 40
Table 4.1: Performance of the current source under test. 49

Switched Current Circuits for a Bandpass Delta-Sigma Modulator

Chapter 1. Introduction

1.1 Motivation

Analog-to-digital converters (ADCs) are used to transform continuous-time analog signals into digital signals which contain all the information present in the original analog signal. This conversion allows real world signals, which are analog, to be processed with digital circuitry. Digital signal processing is generally chosen over analog signal processing whenever possible since digital circuits are more robust, are easier to design and can be made programmable.

Delta-sigma ADCs exhibit high linearity, high tolerance to circuit imperfections and require less complex anti-aliasing filters than ordinary Nyquist-rate converters [1]. Delta-sigma converters achieve these desirable features by *oversampling* (sampling faster than the Nyquist rate) and exploiting the extra bandwidth through noise-shaping. Since the *oversampling ratio*[1] is typically 64 or more and the sampling rate is limited to a few tens of MHz, regular (lowpass) delta-sigma ADCs are only useful for frequencies up to a few hundred kHz.

In contrast, bandpass delta-sigma ADCs provide the means to perform high-resolution conversion of narrow-band signals at frequencies in the MHz range. Bandpass modulation is more attractive than mixing followed by lowpass modulation since bandpass modulation results in simpler circuits and is not subject to such nonidealities as $1/f$ noise and errors in the mixing process.

---

1. Defined as the ratio of sampling frequency to twice the signal bandwidth.

Switched-capacitor implementations of bandpass modulators have been reported to operate with sampling rates as high as 44MHz [2], but switched-current implementations have the potential for much higher speeds [4]. An additional advantage of switched-current circuits is that, in contrast to switched-capacitor circuits, they do not need linear capacitors and hence are compatible with standard digital processes.

This thesis builds on the work of [5] which originally proposed the use of switched-current circuits for bandpass delta-sigma and performed some early simulations.

1.2 Outline of the thesis

The fundamentals of bandpass delta-sigma and switched-current topologies are presented to the reader in Chapter 2. Chapter 3 describes the design and layout considerations of the various blocks in the modulator. Test results of the chip are discussed in Chapter 4. Chapter 5 concludes the thesis and gives directions for future work.

Chapter 2. Background

This chapter reviews the state-of-the-art for bandpass delta-sigma converters and switched-current circuits. As this thesis builds upon the work of [5], the relevant portions of that work are also summarized.

2.1 A word about delta-sigma

Delta-sigma modulation relies on *oversampling* and *noise-shaping*. Oversampling is the act of sampling a signal at a rate above the Nyquist rate.The oversampling ratio, R, is given by $f_s/(2f_B)$, where f_s is the sampling frequency and f_B is the signal bandwidth. Noise-shaping is the process of shaping the spectrum of the quantization noise. Noise-shaping is achieved by embedding the quantizer in a feedback loop and thus can be used to spectrally separate the noise from the input signal. Subsequent filtering can then remove the out-of-band quantization noise and thus leave only the desired signal behind.

A first-order delta-sigma modulator consisting of an analog integrator, a single-bit ADC, a single-bit DAC and a digital filter is shown in Figure 2.1. The output of the modulator is given by [1]

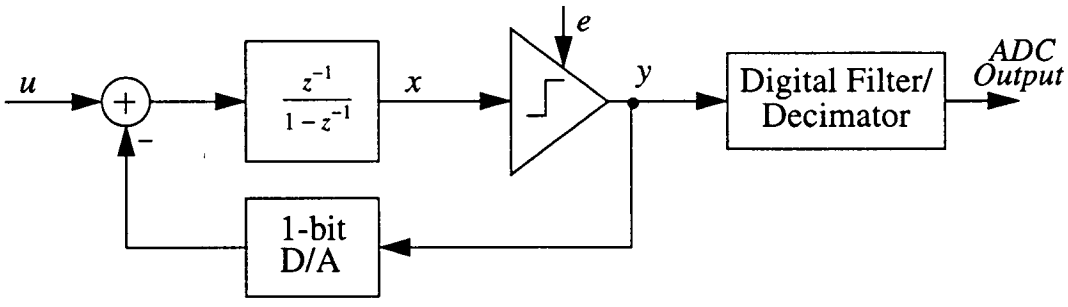


Figure 2.1: A first-order delta-sigma analog to digital converter.

$$Y(z) = z^{-1}U(z) + (1 - z^{-1})E(z). \tag{2.1}$$

In the above relation Y is the output, U is the input and E is the quantization error. It is apparent from the above equation that the quantization noise is frequency shaped by the high-pass transfer function $(1 - z^{-1})$. Although the total quantization noise is increased, the low frequency energy of the quantization noise is reduced. The digital lowpass filter removes the out of band noise and produces a high-resolution digital representation of the input. The in-band noise power for this modulator is given by [1]

$$N_0^2 = \frac{\pi^2 \sigma_e^2}{3} R^{-3}. \tag{2.2}$$

This shows that an octave increase in R reduces the in-band noise by 9 dB, which corresponds to a 1.5 bit increase in the resolution of the converter. In principle, the in-band noise can be made as small as desired, provided R is large enough. The resolution of a delta-sigma converter is thus improved by clocking faster (which is easy) and not by making larger, more sensitive analog circuitry (which is hard).

An important property of single-bit modulators is what is commonly referred to as "inherent linearity." This property refers to the fact that any static two-level DAC can be modelled with a linear gain and an offset. The offset translates into an offset of the input, and the gain merely scales the input. As a result, gain and offset errors do not cause distortion and the conversion is "linear."

The first order modulator only uses first order noise-shaping and hence requires large oversampling ratios in order to achieve high resolution. Higher order modulators overcome this disadvantage by using a high-order noise transfer function. Eq. (2.3) shows

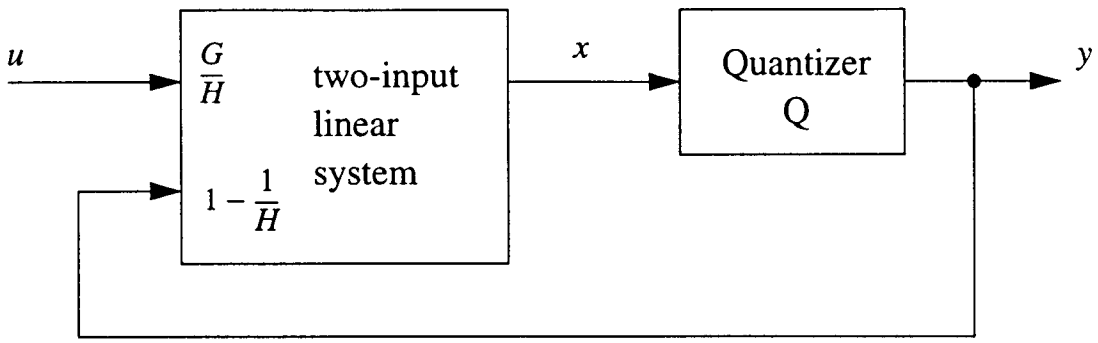


Figure 2.2: A general delta-sigma modulator. Note that there is a unit delay in the feedback since $1 - 1/H$ is required to be strictly causal.

how the output of a general single-quantizer modulator consists of noise and signal components and Figure 2.2 shows the general structure.

$$Y(z) = G(z)U(z) + H(z)E(z) \tag{2.3}$$

In this equation $G(z)$ is the signal transfer function (STF) and $H(z)$ is the noise transfer function (NTF). Typically, for an order-n modulator, $H(z)$ is given by

$$H(z) = \frac{(z-1)^n}{z^n + a_{n-1}z^{n-1} + \ldots + a_0}. \tag{2.4}$$

The denominator coefficients $a_{n-1}, \ldots a_0$ must be chosen such that the modulator is stable. Although this is an unresolved problem, rules of thumb such as $||H||_\infty < 1.6$ (Lee's rule [7]) work well in practice. The in-band noise power for the general case is given by

$$N_0^2 = \frac{\pi^2 \sigma_e^2}{(2n+1)R^{2n+1}} \cdot \frac{1}{(a_{n-1} + a_{n-2} \ldots + a_0)^2}. \tag{2.5}$$

Eq. (2.5) shows that an octave increase in R increases the resolution by n + 0.5 bits, resulting in a higher resolution at a given value of R than the first order modulator.

Notwithstanding the performance advantages offered by high-order modulation, an oversampling ratio on the order of 32 is still needed to achieve 16-bit resolution [8]. Thus, the clock frequency must still be significantly higher than the upper frequency of interest. For high-frequency signals, this means that the modulator will be operated at the limit imposed by the technology. As the next section shows, bandpass modulators can overcome this limitation to some degree.

2.2 Bandpass Delta-Sigma Data Converters

The previous section showed that quantization noise can be nulled at low frequencies by enclosing the quantizer in a feedback loop. The same principle can also be applied to higher-frequency low-bandwidth signals, simply by placing nulls in the quantization noise spectrum across the band of interest [6]. The band-reject noise-shaping of bandpass delta-sigma converters results in high signal-to-noise ratios for narrow-band signals not centered at DC. An ADC based on this principle is shown in Figure 2.3. Since bandpass delta-sigma modulators operate in much the same manner as conventional (lowpass) modulators they retain many of their advantages over Nyquist-rate converters.

The primary motivation for the development of bandpass converters is the simplicity they impart to systems dealing with narrowband signals. Examples of such systems include RF communication systems, spectrum analyzers and special-purpose

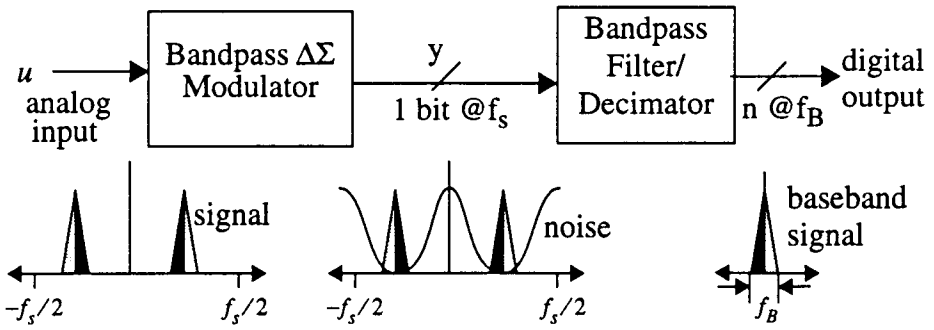


Figure 2.3: A bandpass ΔΣ modulator based A/D converter.

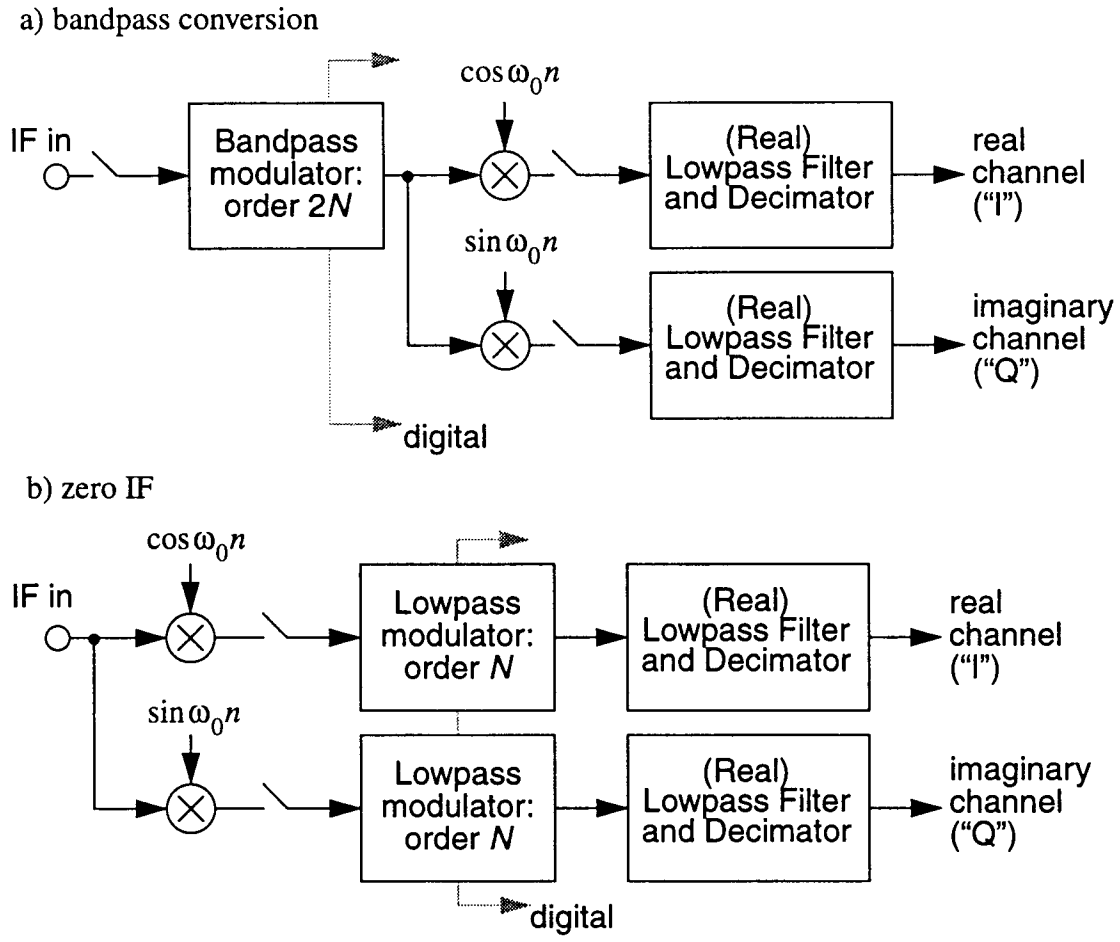


Figure 2.4: Comparison of radio receivers using bandpass ΔΣ and a zero IF with lowpass ΔΣ [10].

instrumentation for narrowband sources. In the context of a communication system, early conversion to digital at either the IF or RF stage results in a more robust system and provides opportunities for dealing with multiple broadcast formats. As shown in Figure 2.4, the competing "zero-IF" receiver architecture does quadrature mixing with analog components while the bandpass modulator does mixing digitally.

In a manner analogous to a lowpass modulator, a bandpass delta-sigma can be constructed by connecting a filter and quantizer in a loop as shown in Figure 2.5. The resonator may be implemented as a discrete-time filter using, for example, switched-

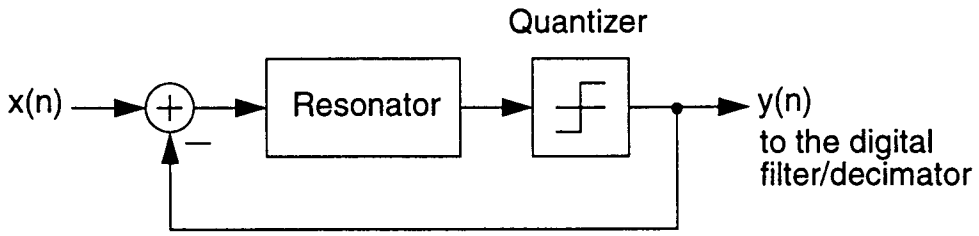


Figure 2.5: A conceptual bandpass noise shaping feedback loop.

capacitor or switched-current technology, or it may be implemented as a continuous-time filter. The quantizer may be multi-bit or single-bit, and the loop may use multiple quantizers. In this work, we use a single-bit quantizer and implement resonators in switched-current technology. The in-band noise power for a bandpass modulator of order $2n$ is given by

$$N_0^2 = \frac{\pi^2 \sigma_e^2}{(2n+1) R^{2n+1}} \cdot \left(\frac{2 \sin \omega_0}{D(1)}\right)^n \tag{2.6}$$

where ω_0 is the normalized radian center frequency. From Eq. (2.6) it is evident that for every octave increase in R the resolution increases by $n + 0.5$ bits.

2.3 Why Switched-Current?

The conventional technique used to implement delta-sigma modulators is switched-capacitor technology. Since the linear capacitors used in SC circuits require special process steps, a standard digital process is not suitable for switched-capacitor circuits. In a mixed-signal chip where typically less than 20% of the area is occupied by the analog circuitry, using a special process is not cost effective. On the other hand, switched-current circuits do not need linear capacitors and so can be implemented in a standard digital process [11]. The other advantage of switched-current circuits is that they are reputed to be faster than conventional switched-capacitor circuits.

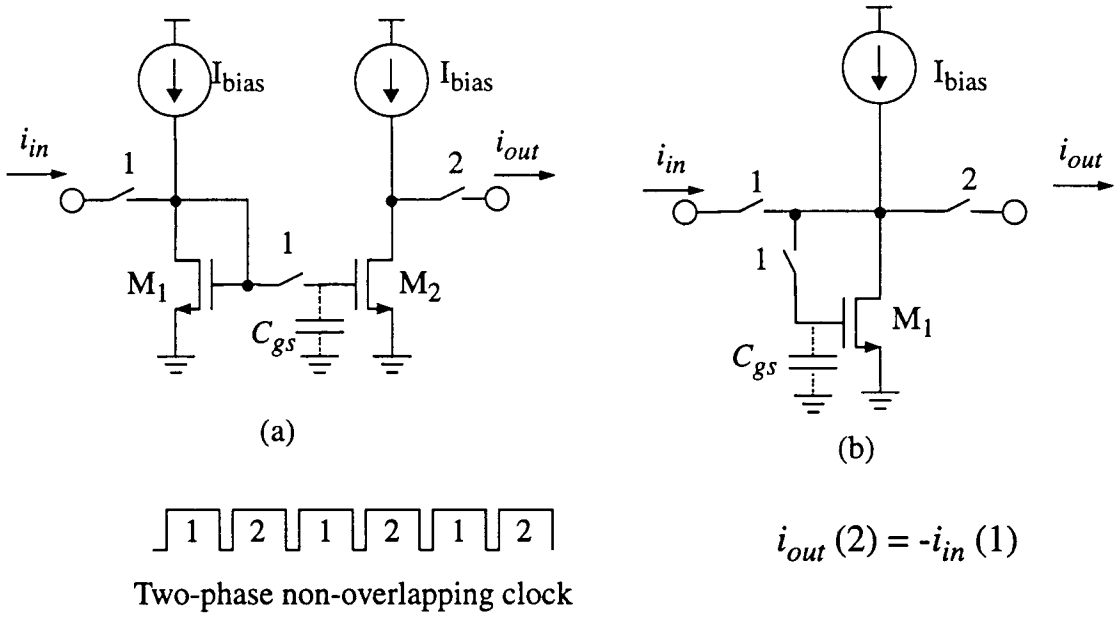


Figure 2.6: MOS current memory cells.

The basic building block of switched-current circuits is a current copier or a current mirror. Shown in Figure 2.6(a) is a current copier built with a current mirror. In the initial *track* phase (phase 1), the mirrored input current is stored as a voltage on the C_{gs} of M_2. In the complementary *hold* phase (phase 2) the transistor M_2 tries to hold at its output the same amount of current as it memorized in the *track* phase. Current scaling can be done easily in this kind of circuit but mismatch between the transistors is a significant source of error. The dynamic current copier shown in Figure 2.6(b) overcomes the mismatch problem by using only a single transistor. In the *track* phase transistor M_1 is diode connected and the voltage corresponding to the input current is stored on the C_{gs}. The same current is held at the output in the *hold* phase by the voltage on C_{gs}. Since the dynamic current copier uses only one transistor, transistor matching is not an issue, but scaling cannot be performed very easily. Addition of current is done by routing currents into a common node. Thus, all the arithmetic functions such as summation, inversion, delay and scaling which are necessary for signal processing can be performed by switched-current circuits.

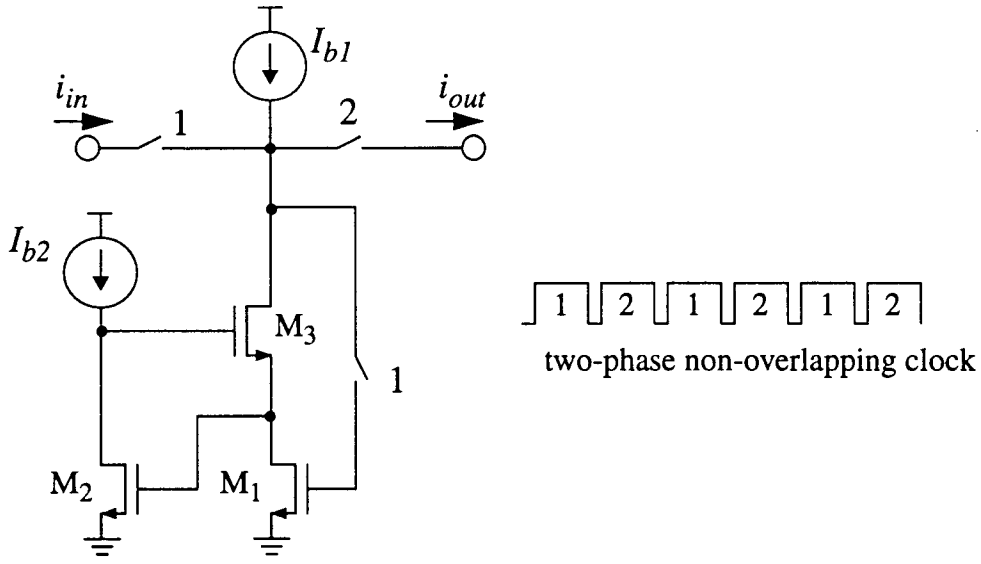


Figure 2.7: The regulated cascode current copier.

Unfortunately, circuits built with the simple current copier are not as accurate as switched-capacitor circuits. For example, if the V_{ds} of M_1 changes (due to the load) in phase 2, there will be an error in the output current due to channel length modulation. Since the output impedance of a single MOS transistor cannot be made very high relative to the load without using extremely long devices, this circuit is not suitable for high-speed high-accuracy applications. In order to overcome this problem an improved structure was considered.

The regulated cascode current copier (RC^3) shown in Figure 2.7 is an enhancement of the basic dynamic current copier [12]. Although the operation of the structure is similar to that of the dynamic current copier, it has improved voltage swing and output impedance. The operating principle of the regulated cascode circuit is as follows. Transistor M_1 converts the input voltage corresponding to the input current into a drain current i_{out} that flows through the drain-source path of M_3 to the output terminal in phase 2. To obtain a high output resistance, i.e. to suppress channel-length modulation in M_1, the drain-to-

source voltage of M_1 is regulated. This is accomplished by a feedback loop consisting of an amplifier (M_2 and I_{b2}) with M_3 acting as a follower. Since M_2 carries a constant current, any change in V_{ds1} is detected, amplified and fed back in the loop formed by M_2 and M_3. In this way the drain-source voltage of M_1 is regulated to a fixed value. It should be noted that the feedback mechanism upon which the stabilization is based works even if M_3 is driven into the ohmic operation region. This feature extends the usable range for the output signal [15]. The V_{ds1} voltage variations are reduced by approximately a factor of $(g_m r_{ds})^2$ which can be as high as 1000. Thus in the track mode the input resistance is $1/g_m$, which is in the kΩ range, while the output impedance in hold mode is approximately $g_m^2 r_{ds}^3$, which is in the MΩ range. This allows interconnection of cells with high current transfer efficiency.

Compared to a simple cascode, the minimum output voltage of the regulated version is lower by 30-60% while the output conductance and feedback capacitances are lower by 100 times [15]. So for increased dynamic range, increased output impedance and faster settling time, the regulated version is better than the simple cascode. For VLSI and high-frequency circuits, transistors with minimum feature size are often used. Such transistors exhibit pronounced channel-length modulation and carrier multiplication, even at relatively low voltages, as well as a moderate transconductance. In such cases to minimize the effect of channel-length modulation RC^3 can be used. A more detailed analysis of this circuit is postponed to Chapter 3.

2.4 The Modulator

The eighth-order bandpass modulator in Figure 2.8 was designed by applying a pseudo *N*-path transformation, $z \rightarrow -z^2$ to a lowpass fourth order modulator [5]. The zeros of $H(z)$ are thus mapped from DC to $\pm\pi/2$ and the integrator transfer function becomes $1/(1+z^{-2})$. This transformation places the center frequency at $\omega_0 = \pi/2$, and thus for

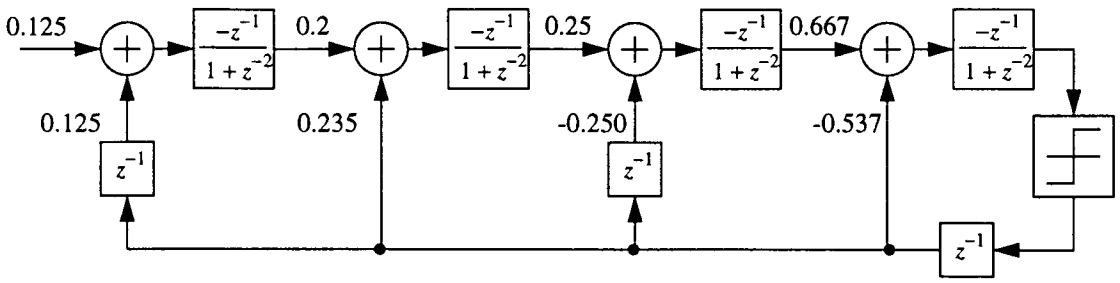


Figure 2.8: The block diagram of the eighth-order bandpass modulator, [5].

a fixed center frequency the sampling frequency is dictated by the relation $f_s = 4f_0$. The advantage of $z \rightarrow -z^2$ transformation is that it does not affect the dynamics of the prototype [10]. Specifically, the modulator behaves as a pair of multiplexed lowpass modulators with alternate samples of each modulator negated. As a result, the bandpass modulator is stable if and only if the lowpass modulator is and the SNR curves of the

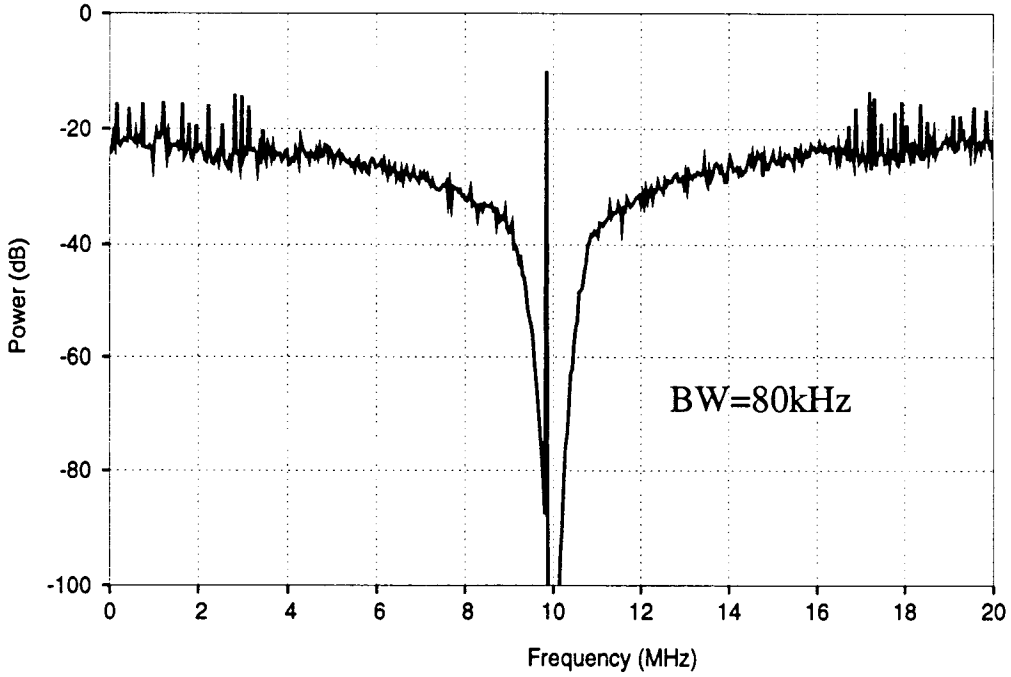


Figure 2.9: An FFT of the output of the modulator.

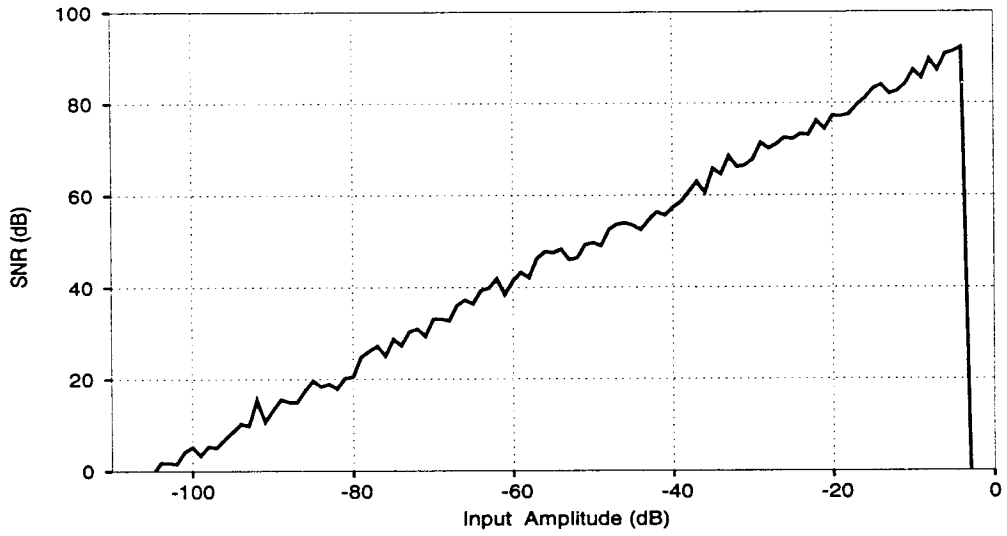


Figure 2.10:The SNR curve for the modulator of Figure 2.8, when operated with an oversampling ratio of 64.

modulators are identical. A modified version of this modulator which will be shown in Chapter 3 is used as a design target for this thesis.

For an application of conversion of 10 MHz±150 KHz signals with 15-bit accuracy (SNR 90 dB) a choice of $\omega_0 = \pi/2$ gives an oversampling ratio of 66.67 for the eighth-order modulator. To give a slightly wider passband than required, an oversampling ratio of 64 (nearest integral power of 2) is chosen. Figure 2.9 shows a sample spectrum of the output of the modulator which clearly shows the spectral null in the noise at $f_s/4$. The input is a -10 dB sine wave with frequency of 40MHz. Figure 2.10 shows the SNR curve for the modulator as determined by simulation of the block diagram. As this figure shows, the modulator achieves 92 dB SNR at an input power of -4 dB when the oversampling ratio is 64. For other oversampling ratios, the peak SNR increases by 27 dB (the resolution by 4.5 bits) with each doubling of the oversampling ratio, as would be the case with a fourth-order lowpass modulator.

The output $Y(z)$ of the modulator is given by (assuming that the input has a unit delay which is not shown in the block diagram)

$$Y(z) = \frac{-0.004Uz^4}{D(z)} + \frac{(1+z^2)^4 E}{D(z)} \tag{2.7}$$

where $D(z)$ is given by

$$D(z) = z^8 + 3.484z^6 + 4.6496z^4 + 2.8056z^2 + 0.644. \tag{2.8}$$

While the noise transfer function $H(z)$ is given by

$$H(z) = \frac{(1+z^2)^4}{D(z)}. \tag{2.9}$$

Using Lee's rule of thumb, $||H||_\infty = 1.55 < 1.6$ indicates that the modulator should be stable.

2.5 Resonator

The most critical block in the modulator is the resonator block RESON, whose transfer function is given by

$$RESON(z) = \frac{-z^{-1}}{1+z^{-2}} \tag{2.10}$$

and whose time domain behavior can be described by

$$i_{OUT}(n+1) = -i_{IN}(n) - i_{OUT}(n-1). \tag{2.11}$$

Since the above equation requires the use of a current memory, use is made of the regulated cascode current copier (RC^3). Figure 2.11 shows a realization of the resonator which uses three RC^3 cells. With the control signals shown, the output current is supplied by each cell in a cyclical manner. The output current of an RC^3 cell is simply the negative of the current memorized by that cell during the previous clock cycle. Since the *I* switch of the cell which last produced the output current is on at the same time as the *I* switch of the

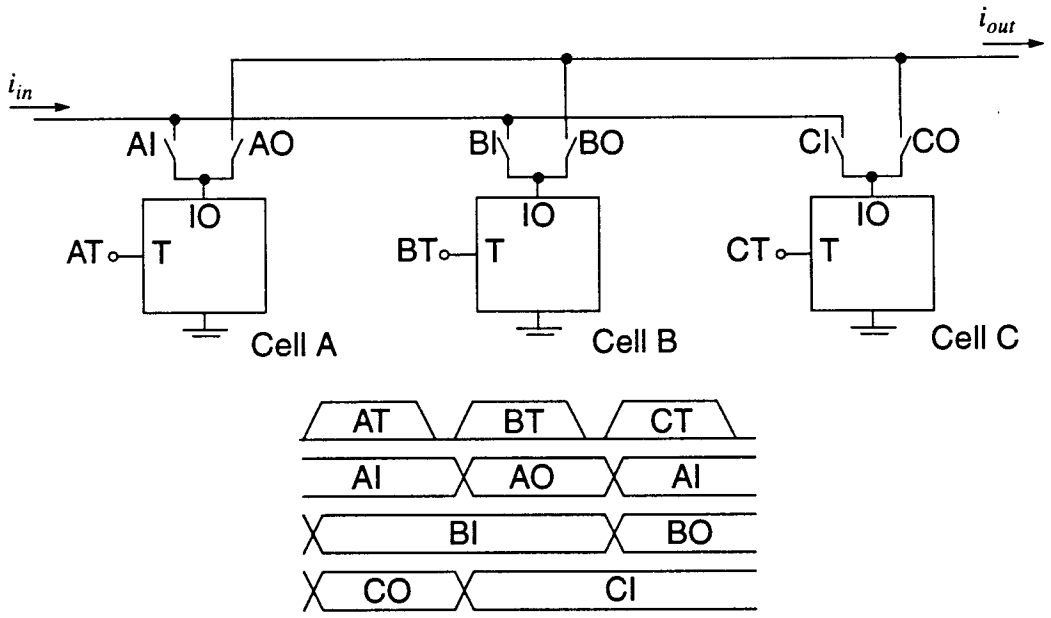


Figure 2.11:The single-ended resonator block, RESON, and its clock signals

cell in the track mode is, and since the *IN* terminals of these two cells are connected, the current memorized is the sum of the input current and the output current from one cycle earlier. Thus the input-output relationship for this circuit is

$$i_{OUT}(n+1) = -(i_{IN}(n) + i_{OUT}(n-1)), \tag{2.12}$$

which is identical to (2.11). The clocking required to achieve this is also shown in Figure 2.11 while the generation of it will be explained in the next chapter.

The use of current-copiers to shuffle currents back and forth makes the negation of the state required by (2.11) come at no cost. This contrasts with switched-capacitor implementations of this block, which can only accomplish this inversion by adding switches and making the circuit differential [13]. Several other features of this design are also worthy of note. Firstly, mismatch among the current copiers is modulated to $f_s/3$ by the period-3 clock and thus DC errors (such as signal-independent charge injection) do not

appear in the passband. Secondly, the tracking cell has a full clock period to settle. This contrasts with typical switched-capacitor circuits which have only half a clock period in which to settle. This, coupled with the inherent speed advantage of SI, allows the circuit to function at high clock rates. Lastly, the output current is available for a full clock period.

2.6 Previous Work

The target for this thesis is derived from the work done by Vineet Dalal as a part of his Masters thesis [5]. That work demonstrated that switched-current circuits are viable for the implementation of a bandpass modulator. In particular, the design of the bandpass modulator from its lowpass prototype was briefly discussed; a block level design approach was adopted and a new SI architecture for the pseudo 2-path resonator was developed; the transistor level implementation of the differential resonator and preliminary simulations were performed. The resonator was shown to operate at a clock rate of 10MHz. The design of the other less critical blocks and the circuit implementation of the modulator was left for future work.

2.7 Summary

Delta-sigma converters have been shown to have a high linearity, high tolerance to circuit imperfections and reduced anti-alias filter design over Nyquist-rate converters. The speed limitation for lowpass modulators makes them unattractive for high frequency conversion. On the other hand, bandpass delta-sigma modulators can perform high-resolution conversion of narrow-band signals even at high frequencies. For narrow-band high-frequency signals, bandpass modulation results in simpler circuits and is not subject to such nonidealities as $1/f$ noise.

Switched-current circuits were shown to have certain advantages over conventional switched-capacitor circuits. The compatibility of SI circuits with a standard digital process

and the inherent advantage of speed over SC circuits has led to the continued development of SI circuits.

The implementation of the eighth-order bandpass delta-sigma modulator in switched-current technology is the first of its kind combining the advantages of both higher order bandpass delta-sigma and switched-currents. The modulator and the resonator, an important block level component, were presented to the reader. The current copier, which is the basic cell needed for the implementation of the resonator was discussed. Although block level simulations of the modulator verified its functionality, implementation at the transistor level followed by fabrication in silicon and then testing are needed to prove the viability of the technique.

Chapter 3. Design and Layout

In this chapter the design of the various blocks of the modulator is discussed. The regulated cascode current copier is designed to meet the required specifications. The transistor-level circuits of other less critical blocks such as the comparator and DAC are then shown. The trade-offs involved in the design of the clock circuit are explained. The modified SI2, a critical block of the modulator, is presented to the reader. Simulations are shown to verify the designs and practical layout issues are also considered.

3.1 SI8: The eighth-order bandpass delta-sigma modulator.

The eighth-order modulator shown in Figure 2.8 on page 12 was modified to suit the implementation of this thesis. The target modulator of this thesis is shown in Figure 3.1. When compared to its original version the feedforward and the feedback coefficients were modified to facilitate easy scaling of currents. Scaling was done in the resonator itself to achieve the feedforward coefficients and will be discussed later. The block diagram was altered to give all resonators in the modulator identical transfer functions, with the sole exception of the last resonator. For reasons which will be described later, this resonator is

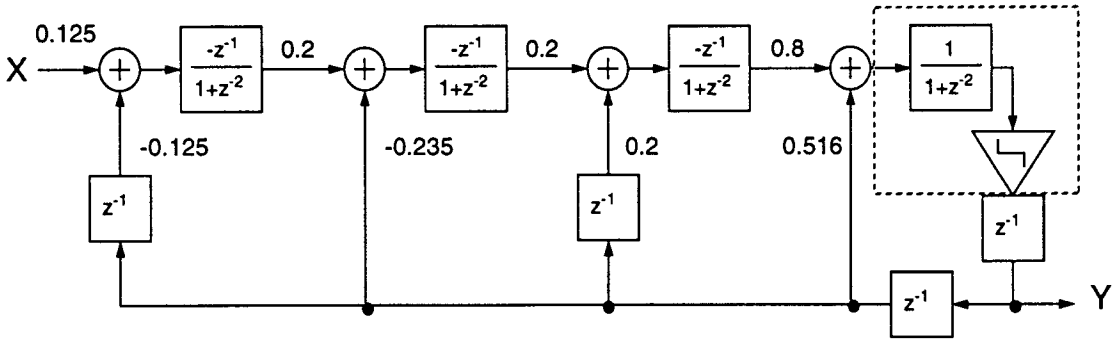


Figure 3.1: Block diagram of the scaled SI8.

merged with the comparator and the delay and inversion are absent. Nevertheless, all the resonators are identical in terms of their layouts, which greatly simplifies the design. Since Figure 3.1 is merely a scaled version of Figure 2.8, the conversion parameters remain the same.

3.2 Regulated Cascode Current Copier - RC^3

3.2.1 Specifications

In order to design the current copier, its specifications need to be defined. Form the earlier chapter it was observed that the resonator required interconnection of three current copiers for its implementation. This dictates that the output impedance of each copier must be high and the input impedance must be low in order to achieve high current transfer efficiency. For an input impedance in the kΩ range (say 1kΩ), the output impedance must be in the MΩ range (say 1MΩ). This gives an r_{out}/r_{in} of 1000, which in turn makes the resonator gain 1000. The clock rate of 100MHz indicates that a settling time of less than 10ns is required for the current copier. A signal current of 1mA was chosen to achieve the required speed and also to withstand the noise level. A value of 1mA which is equal to the signal current was chosen for the bias current I_{b1}. The value of the other bias current I_{b2} was fixed at 100μA (10% of I_{b1}) since its purpose is to bias M_2. These current values were

Table 3.1:Specifications for RC^3

Parameter	Value
t_s	≤10ns
r_{out}	≥1MΩ
r_{in}	≤1kΩ
I_{b1}	≥1mA
I_{b2}	100μA

chosen to give a first cut specification to the design but could also be subject to adjustment for greater design flexibility. The specifications are summarized in Table 3.1.

3.2.2 Analysis

The regulated cascode current copier was presented in the previous chapter, and is shown once again in Figure 3.2. The output impedance (in the hold phase) of the regulated cascode is $g_{m3}r_{ds3}g_{m2}r_{ds2}r_{ds1}$. During the track phase, M_1 is diode connected and the input impedance is equal to $1/g_{m1}$. It is observed from the above results that r_{out}/r_{in} is easily made larger than 1000, which results in good current transfer efficiency (99.9%) and consequently a gain of 1000 in the RESON block which is sufficient. This performance is approximately equivalent to an opamp-based circuit employing an opamp with a gain of 60dB.

For high-speed operation, a short settling time is very important. We initially chose 100 MHz as the desired clock rate, and thus required a settling time of less than 10ns.

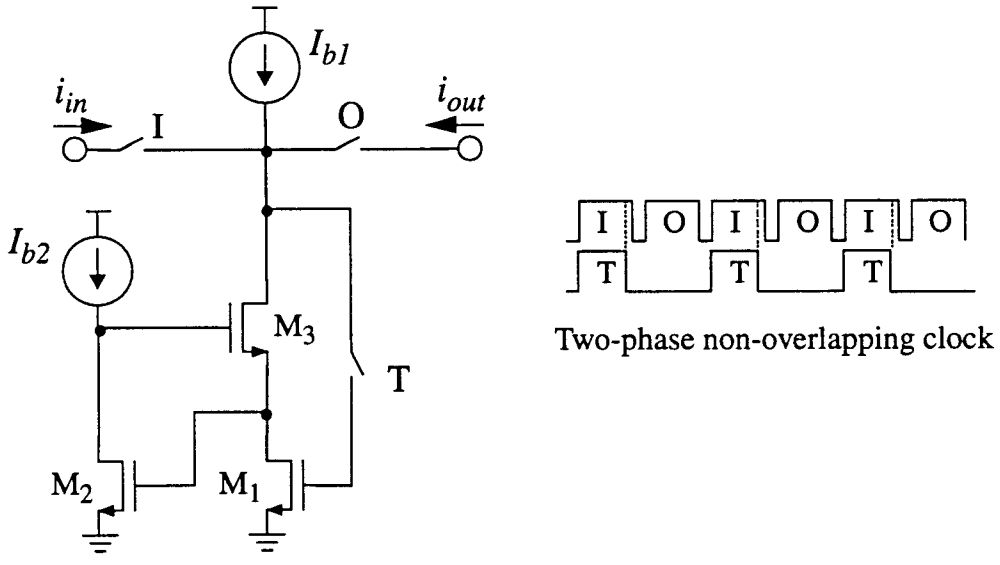


Figure 3.2: Regulated cascode current copier.

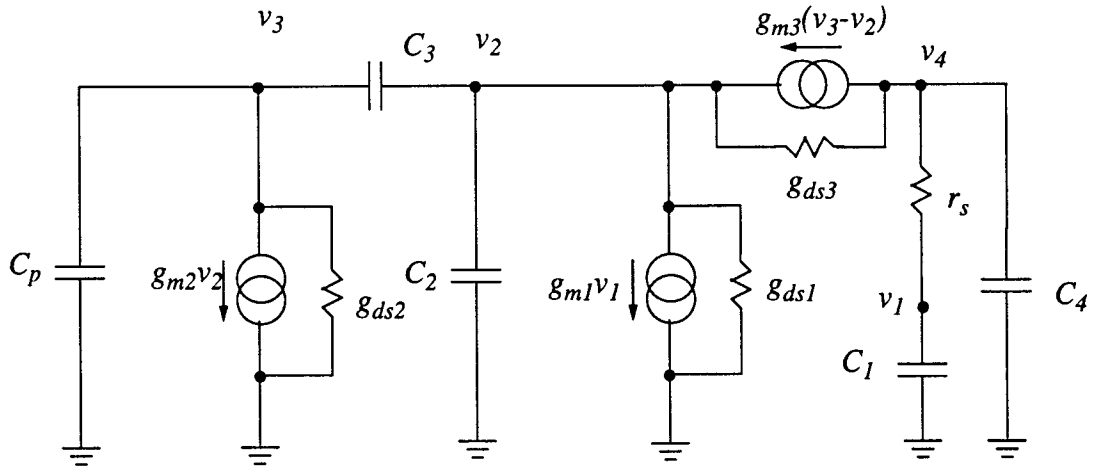


Figure 3.3: Small signal model of RC^3 for the calculation of settling time.

Shown in Figure 3.3 is the small signal equivalent model used for settling behavior. Neglecting the smaller parasitic capacitances and including the conductances which contribute to r_{out}/r_{in} the matrix shown in Eq. (3.6) is obtained. From the eigenvalues of the matrix, the settling time can be estimated using MATLAB. For if it is assumed that this system has a dominant pole with associated time constant τ, the time required for 0.1% settling will be

$$t_s = 7\tau \tag{3.1}$$

Using the values of:

$$C_1 = C_{gs1}\ ;\ C_2 = C_{ds1} + C_{gs2}\ ;\ C_3 = C_{gs3} + C_{gd3}\ ;\ C_4 = C_{ds3}\ ;\ C_p = C_{ds2}$$

and

$$K = C_2C_3 + C_2C_p + C_3C_p \tag{3.2}$$

$$G = g_{m3} + g_{ds1} + g_{ds3} \tag{3.3}$$

$$C_{p3} = C_p + C_3 \tag{3.4}$$

$$C_{23} = C_2 + C_3 \tag{3.5}$$

the following matrix is obtained

$$s\begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} \frac{-g_s}{C_1} & 0 & 0 & \frac{-g_s}{C_1} \\ \frac{-g_{m1}C_{p3}}{K} & -\frac{g_{m2}C_{23}+GC_{p3}}{K} & \frac{g_{m3}C_{p3}-g_{ds2}C_3}{K} & \frac{g_{ds3}C_{p3}}{K} \\ \frac{-g_{m1}}{K} & -\frac{g_{m2}C_{23}+GC_3}{K} & \frac{g_{ds2}C_{23}+g_{m3}C_3}{K} & \frac{g_{ds3}C_3}{K} \\ \frac{g_s}{C_4} & \frac{g_{m3}+g_{ds3}}{C_4} & -\frac{g_{m3}}{C_4} & -\frac{g_s+g_{ds3}}{C_4} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} \quad (3.6)$$

The values of the capacitances used for the simulations are shown in Table 3.2. From the HSPICE simulations it was observed that the settling time was 7.86ns, whereas the above approximation yielded 9.7ns using MATLAB. The settling behavior of the voltage v_1 for both the above methods is shown in Figure 3.4. The waveforms indicate that the two methods are in fairly good agreement considering the fact that many approximations were made.

In order to achieve the shortest possible settling time, the dominant capacitances had to be identified. In order to find out this, the values of the capacitors were altered to

Table 3.2:Value of the Capacitances

Capacitance	Value (pF)
C_1	0.0731
C_2	0.0713
C_3	0.1594
C_4	0.0684
C_p	0.0269

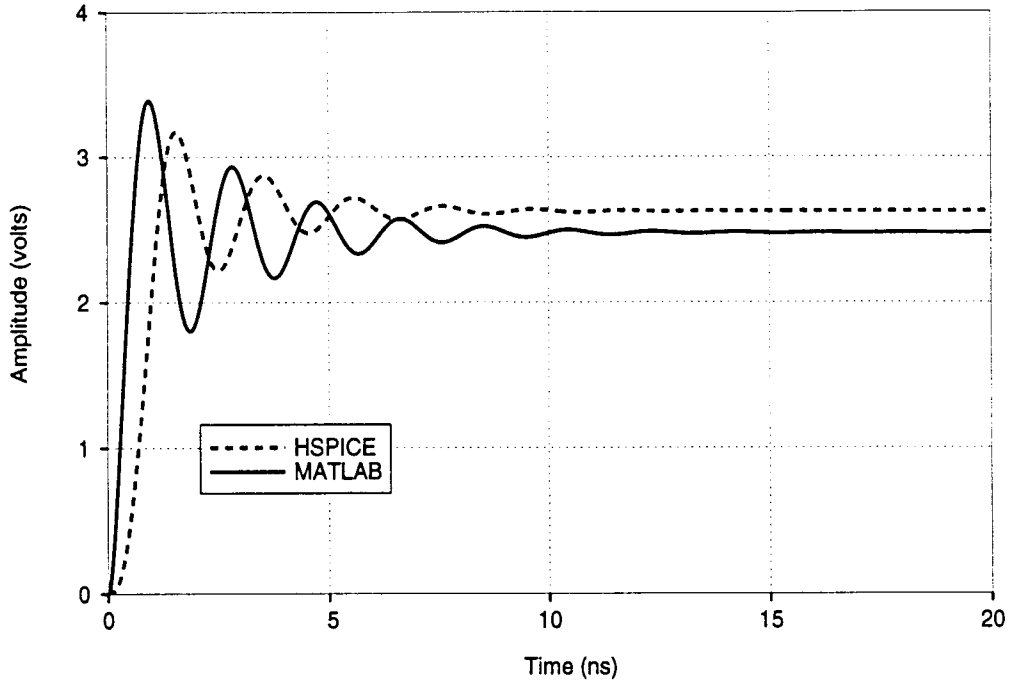


Figure 3.4: Settling behavior using HSPICE and MATLAB.

notice their effect on the settling time. In this process it was found that C_2 and C_p had a strong effect on the settling behavior. The reason both of them were considered was the fact that they both were affected by the size of M_2 and it was not practical to alter only one of them. So in order to decrease the settling time the W and L of M_2 had to be reduced. However since the output impedance was affected by the ratio $\frac{W}{L}$ of M_2 there was a trade-off involved between the output impedance and the settling time. This indicated a limit on the size of the transistor. This issue is to be remembered when the sizes of the transistors are determined later.

3.2.3 Design Methodology

An optimal design of the three transistors which perform the track and hold operation is a key part of this thesis. In order to meet all the required specifications the

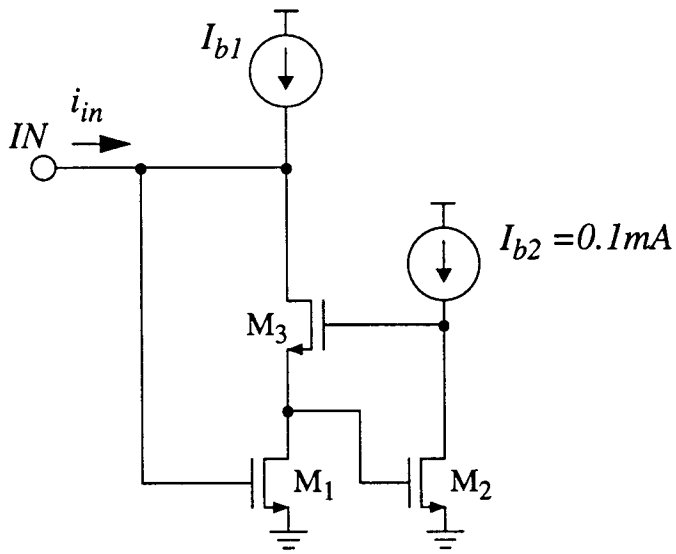


Figure 3.5: Configuration for measuring the input impedance.

method of characterizing the cell was automated. The specifications from Table 3.1 are used as a starting point for the design of the cell.

Before the design automation is started it should be remembered that the purpose of I_{b2} is to bias the transistor M_2 only. As a result, the specifications of output impedance and output voltage swing are not critical for I_{b2}. So its value was fixed at 100μA (from Table 3.1). On the other hand the value of the bias current I_{b1} was critical for the performance of the cell since it would determine the speed and the dynamic range of the cell. In the process of fixing its value it was noticed that for a value of I_{b1} less than 1.3mA transistor M_3 was out of saturation. A value of 1.5mA was chosen for I_{b1} to provide some margin for error.

In order to measure the input impedance r_{in}, the circuit shown in Figure 3.5 is set in the *track* mode. For both positive and negative input currents the input voltage is measured and the worst case r_{in} (which turned out to be for the positive input current) was

considered. Also measured were the gate voltages of M_1, V_{g1max} and V_{g1min} for positive and negative input currents respectively. Allowing for a switch drop of 0.2 V, the required output voltage range is then $V_{min}= V_{g1min}- 0.2$ to $V_{max}=V_{g1max}+ 0.2$.

The measurement of output impedance was done by the circuit shown in Figure 3.6. In order to measure the output impedance, the current copier needs to be in the *hold* mode. However in the *hold* mode, the gate voltage of M_1 must be set correctly. In order to accomplish this the gate voltage of M_1 was set by the gate voltage of a second copier which was in the track mode and which was sinking the desired output current. For positive and negative output currents the output impedance for an output voltage at either end of the range (V_{max} and V_{min}) was measured. The worst case (which turned out to be for a negative output and $V_{out} =V_{max}$) was then chosen from the four measurements. With $r_{out,min}$ and $r_{in,max}$ in hand, the worst case value of the r_{out}/r_{in} figure of merit could be compared against the design requirement of 1000.

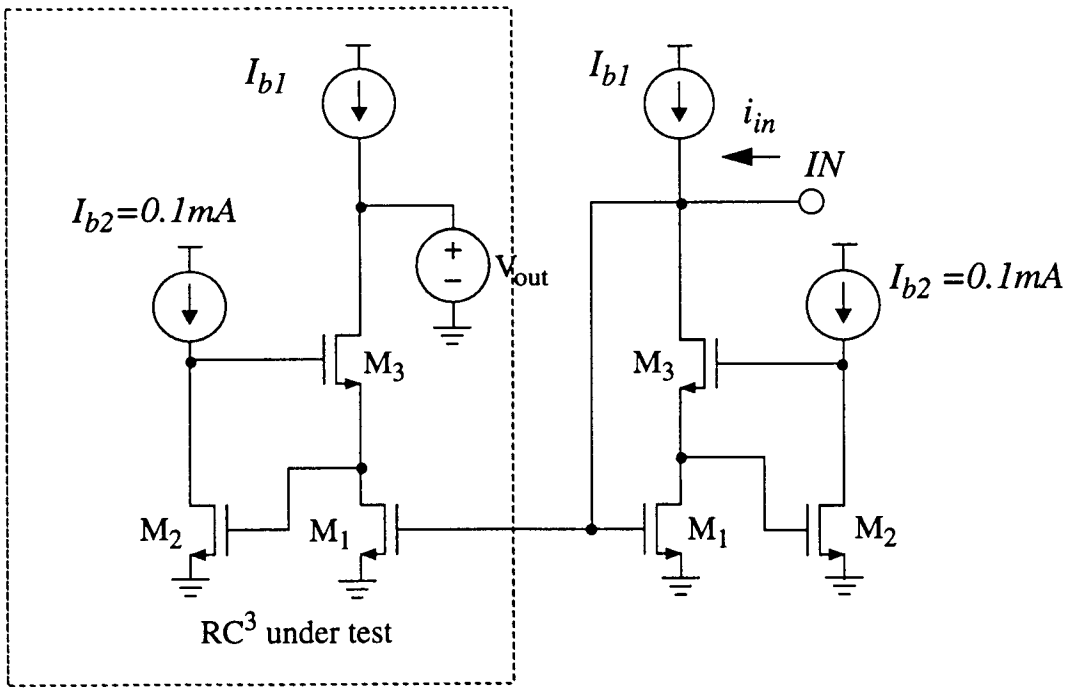
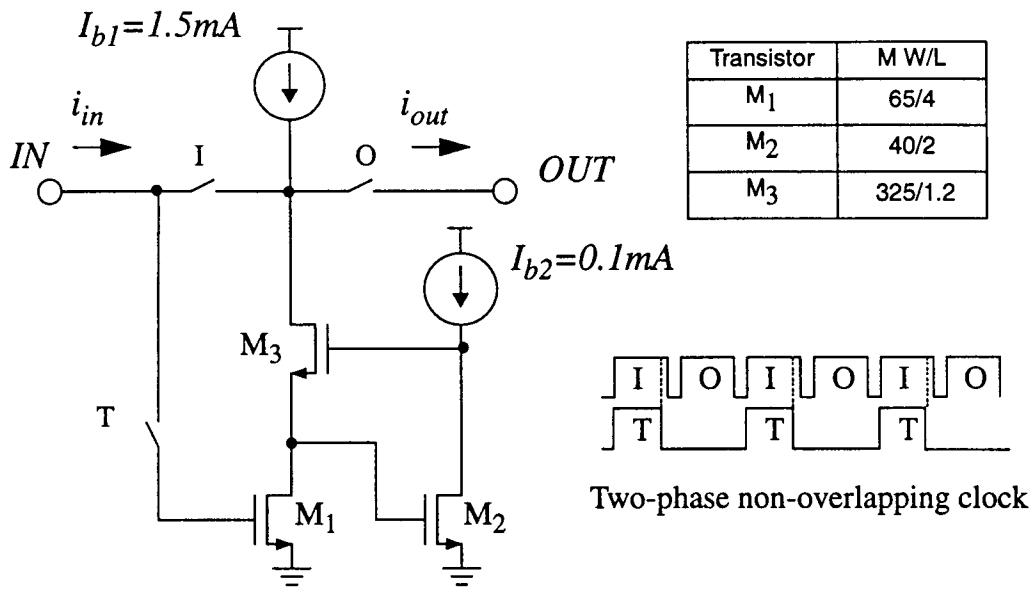


Figure 3.6: Circuit for measuring output impedance.



Transistor	M W/L
M_1	65/4
M_2	40/2
M_3	325/1.2

Figure 3.7: Modified regulated cascode current copier.

In order to measure the settling time the same configuration of Figure 3.5 was used except that a resistance of 500Ω was used to model the r_{on} of the track switch. Since the value of V_{g1}(in the track mode) determines the accuracy of the settling, the time taken for V_{g1} to settle within 1mV for current steps between ±1mA (signal current) was calculated. The worst case (for a falling step from +1mA to -1mA) was used to bound the settling time.

Using the above tests the method of determining the transistor sizes was automated very easily. For different values of transistor sizes and bias current the results were considered. Using these results the first 'cut' of transistor sizes was determined to meet the specifications. Finally the value of W_3 was slightly adjusted to be a multiple of W_1 for easy layout. The resultant sizes and the circuit are shown in Figure 3.7. The clocking is such that the track switch opens slightly ahead of the input switch so that erroneous voltages will not be memorized by the memory transistor. It should be observed that the track switch is now connected directly to the *IN* terminal to bypass the voltage drop across the input switch and so increases the dynamic range of the cell. Later we shall see that this innovation was not

without its drawbacks. The automated process used to determine the cell specification is given in the Appendix.

The layout corresponding to the circuit is shown in Figure 3.8. It consists of only the three transistors which perform the regulated cascode track and hold (RCTH). The transistors are broken into five identical units and layed out in such a manner that it would be easy to scale the output by multiples of 0.2. It should be observed that the drains of unit transistors of M_3 are not connected together to facilitate scaling. In order to match the layout of the current source and the switches (which will be shown later), the layout of RCTH has been adjusted accordingly. The gates of all transistors have been 'snaked' so that the transistor layout will not be unduly wide. The layout was done for ORBIT's 1.2 CMOS N-well process. The next step in the design is transistor level implementation of the current sources I_{b1} and I_{b2}.

3.2.4 Current Sources

Thus far, the current sources have been assumed to be ideal. Since the output of the I_{b1}=1.5ma current source has to withstand a voltage swing of 1.7V to 3.8V while maintaining an output impedance of 1MΩ, the design of this was more difficult than anticipated. Shown in Figure 3.9, it was implemented with a regulated p-channel cascode, where the regulation is done by a two stage opamp. A two stage opamp was preferred since it has a large voltage swing and gain compared to a single stage. Transistors M_1 and M_3 are the two cascoded transistors while the opamp consists of the remaining transistors. Large sizes for both these transistors were chosen so that the output impedance would be high and they could conduct a current of 1.5mA. Table 3.3 shows the sizes of the transistors.

Biasing of the current source was done by another current source which was diode connected and sinking the desired amount of current. Simulations showed that the current

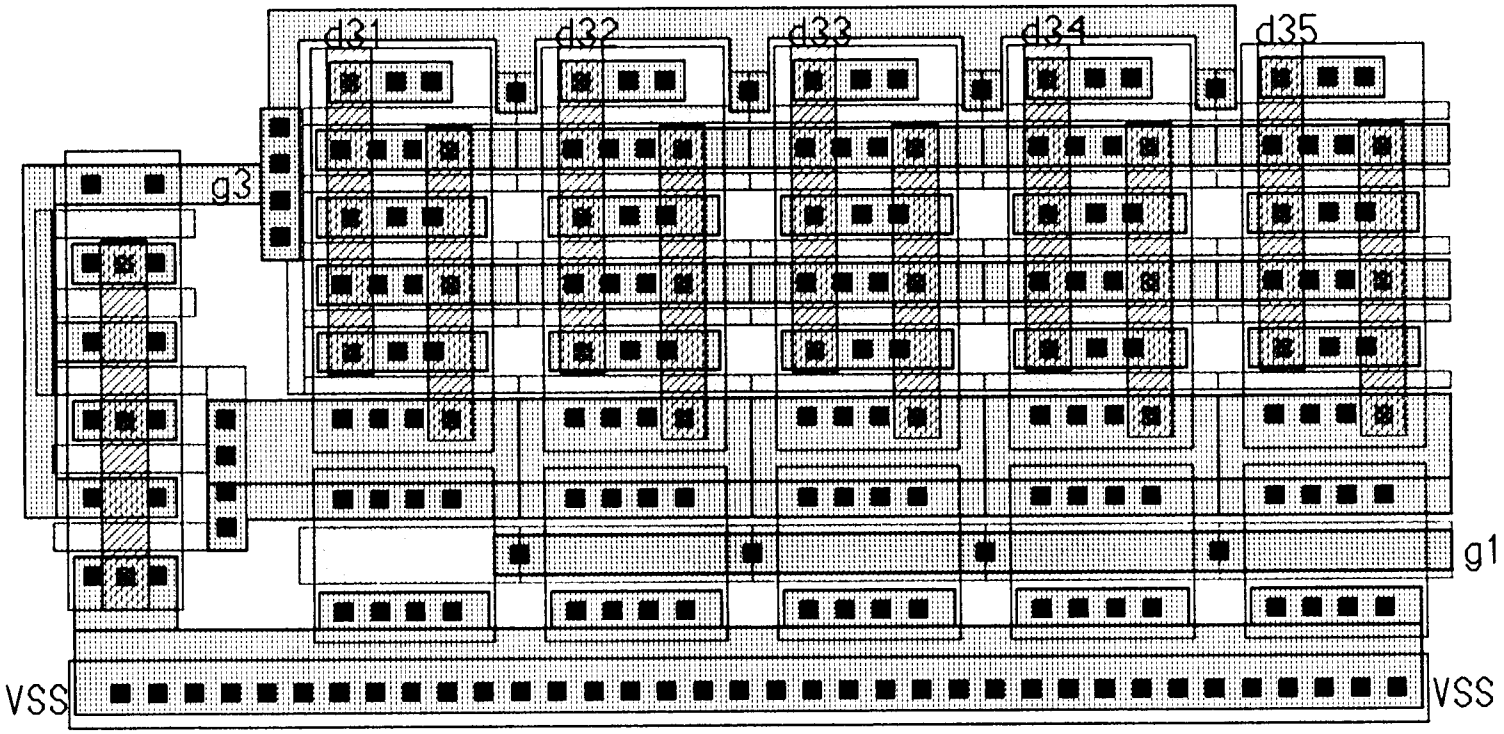


Figure 3.8: Layout of RCTH.

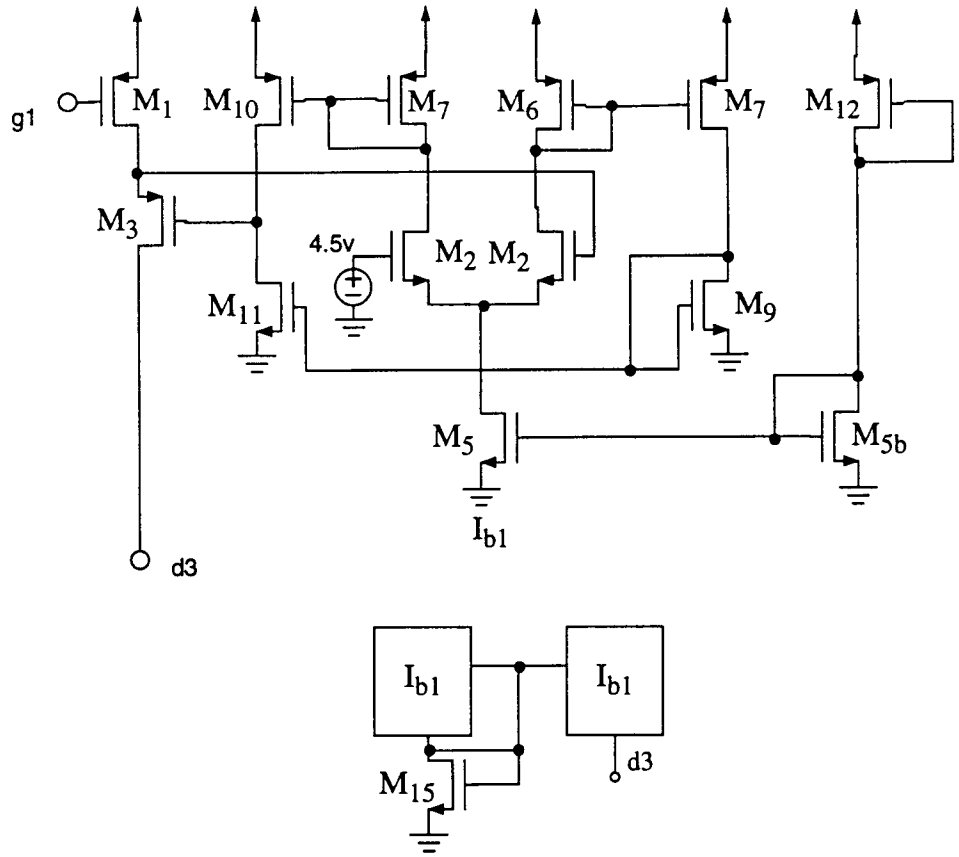


Figure 3.9: Transistor schematic and block diagram of the I_{b1}=1.5mA current source, with the biasing arrangement.

source had a constant current of 1.56mA for an output voltage range from 0 - 4.23V. The output impedance was 1.24MΩ which is on the same order as the r_{out} of RC[3].

Table 3.3: Transistor sizes for I_{b1}.

Transistor	W/L
M1	400/1.4
M3	400/1.2
M2,M4	80/1.6
M5,M5b	25/.2.0
M6,M7,M8 M9,M10,M11	10/2.0
M12	4/2.0
M15	20/1.8

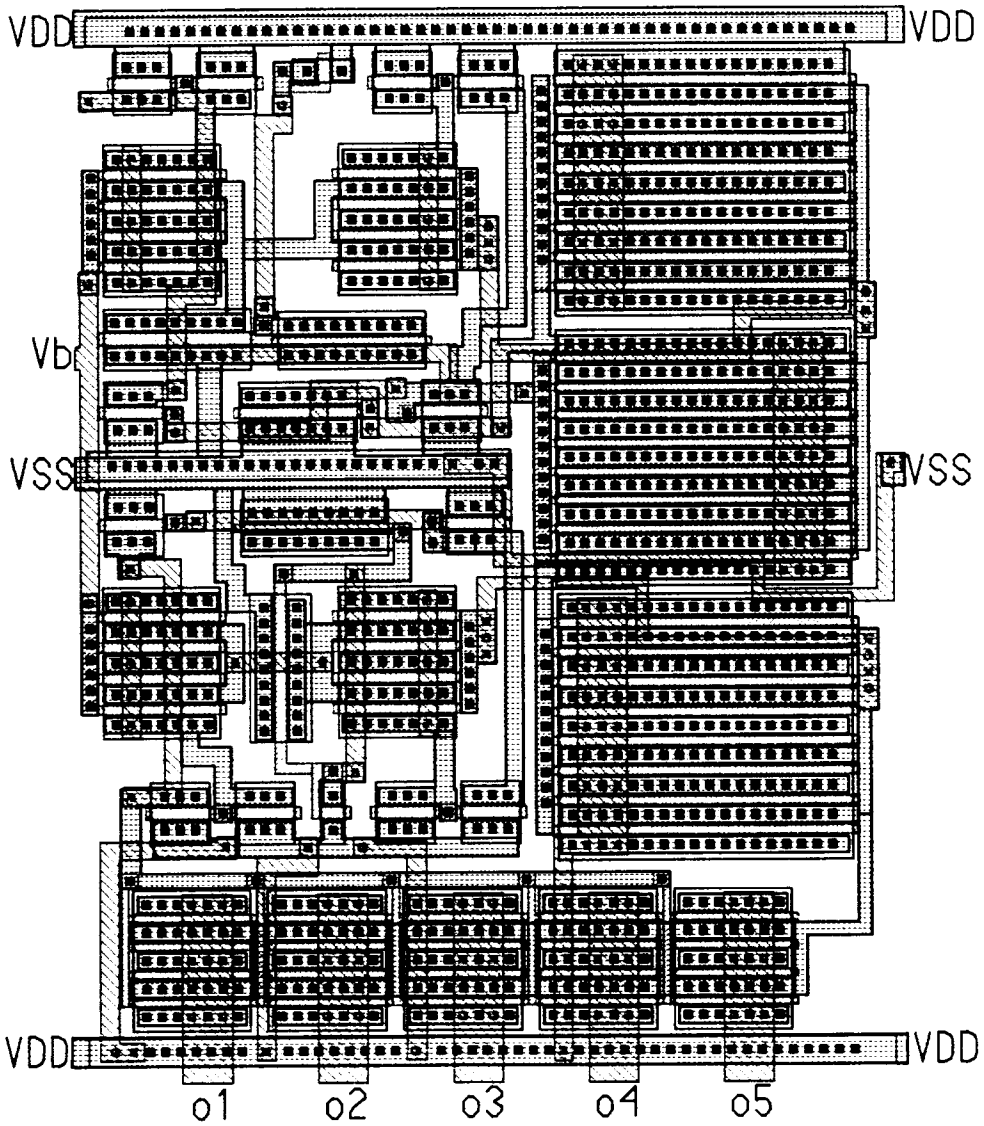


Figure 3.10:Layout of the 1.5mA current source.

For the I_{b2} current source, a simple minimum size p-channel transistor with appropriate bias sufficed. Due to its simplicity the circuit is not shown here.

The layout of the 1.5mA current source is shown in Figure 3.10. The layout was done such that it would be compatible with the other blocks which make up the current copier. The huge transistors shown in the right portion of the layout and the bottom, are the main cascoded transistors M_1 and M_3. A note should be made that the layout shown corresponds to two regulated cascodes, one biasing the other. This accounts for the four large transistors and the overall size of the circuit.

3.2.5 Scaling

In order to obtain the coefficients in the modulator the current copier had to be modified to produce the scale factors. The circuit corresponding to the layout is shown in Figure 3.11. This circuit is based on the principle that when the input current is memorized all the 5 parts memorize it, while only some of the 5 parts try to hold the output current depending on the coefficient factor. This allows coefficients in multiples of 0.2. Since in the *track* mode all the five parts memorize the input current only one track switch is sufficient. It is not so with the case of input and output switches. Since the I/O node of each part has to be isolated from the other in the *hold* phase, five I/O switches are required. A flaw was observed during testing which will be illustrated in the next chapter. In hindsight the author feels that this method of scaling the coefficients using the memory cell is not a good one since it relies on the matching of the transistors, which was what we were trying to overcome by using the RC^3. A better way would be to do the factoring outside the memory cell before the current is fed to the next cell (which is still not a trivial task).

In the layout the input and the output switches are transmission gates with $\frac{W}{L}$ ratios of $\frac{40}{1.2}$ microns for both the p and n transistors. Large sizes were needed so that 1mA

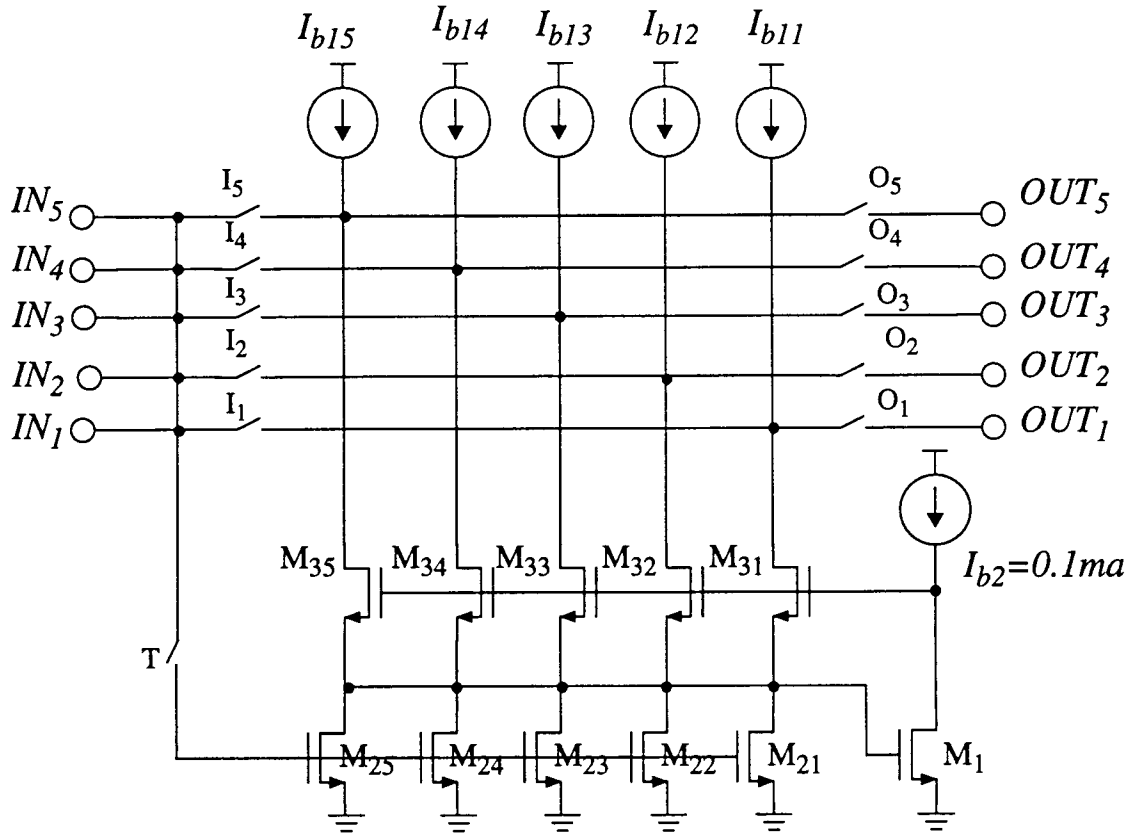


Figure 3.11:RC^3 for producing coefficients.

currents could be carried with less than 0.2V drop across the switch. The track was chosen to have a $\frac{W}{L}$ ratio of $\frac{30}{1.2}$ microns for the p-channel and $\frac{15}{1.2}$ microns for the n-channel. These sizes were chosen to give the least charge injection while maintaining high speed. In order to reduce the charge injection due to the large sizes the speed may have to be cut down in future versions.

The layout corresponding to the circuit in Figure 3.11 is shown in Figure 3.13. It should be observed how all the blocks fit together to form the whole layout. The IN and OUT lines have been provided so that the corresponding nodes could be joined to them. Care should be taken to observe that the output node of the O switches is not connected to

the OUT line since that would be done depending on the coefficient. The substrate contacts of the switches have been connected to 'Analog' power rails (AVDD and AVSS) so that the high frequency switching of the digital cells will not be coupled to the analog cells. A power bus for VDD2 has been provided which corresponds to the supply Vdd/2. This is needed to connect the unused outputs of the copier so that the current source does not saturate. The rail VB corresponds to 4.5v which is used to set the input of the opamp of the current source.

The circuit shown in Figure 2.11 on page 15 is the resonator which is simply three regulated-cascode-current-copiers with their inputs and outputs connected separately to two nodes. Since the layout of RC^3 had been done with consideration for the fact that three of these would be used to make the resonator, the layout of RESON shown in Figure 3.14 is simply three RC^3 cells connected side-by-side. The simulation of the macro model for the resonator indicated a gain of 1000 at signal frequency $f_s/4$. Shown in Figure 3.12 is the output for an input of 10μA and frequency of 25MHz while the resonator is clocked at

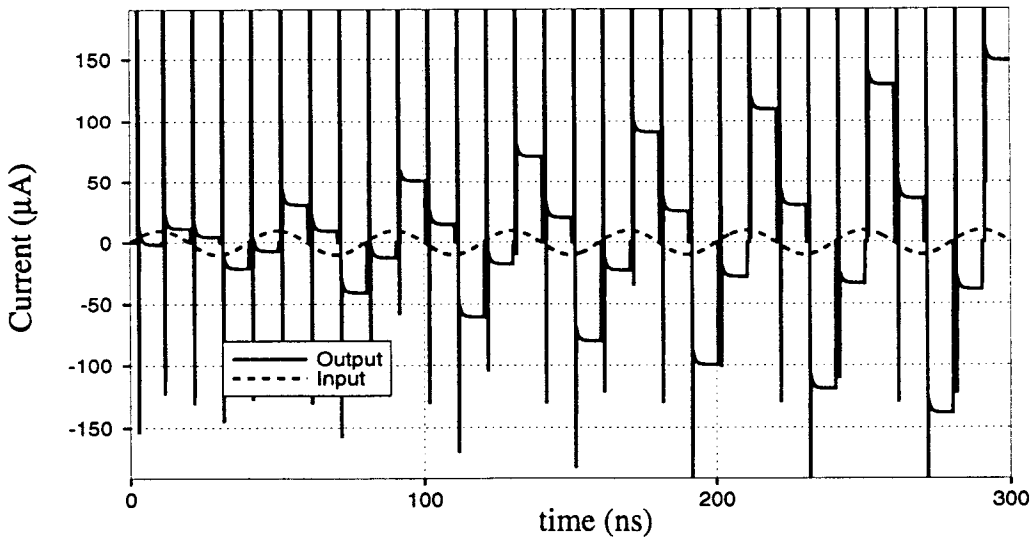


Figure 3.12:Output of the resonator at input of 25MHz and clocked at 100MHz.

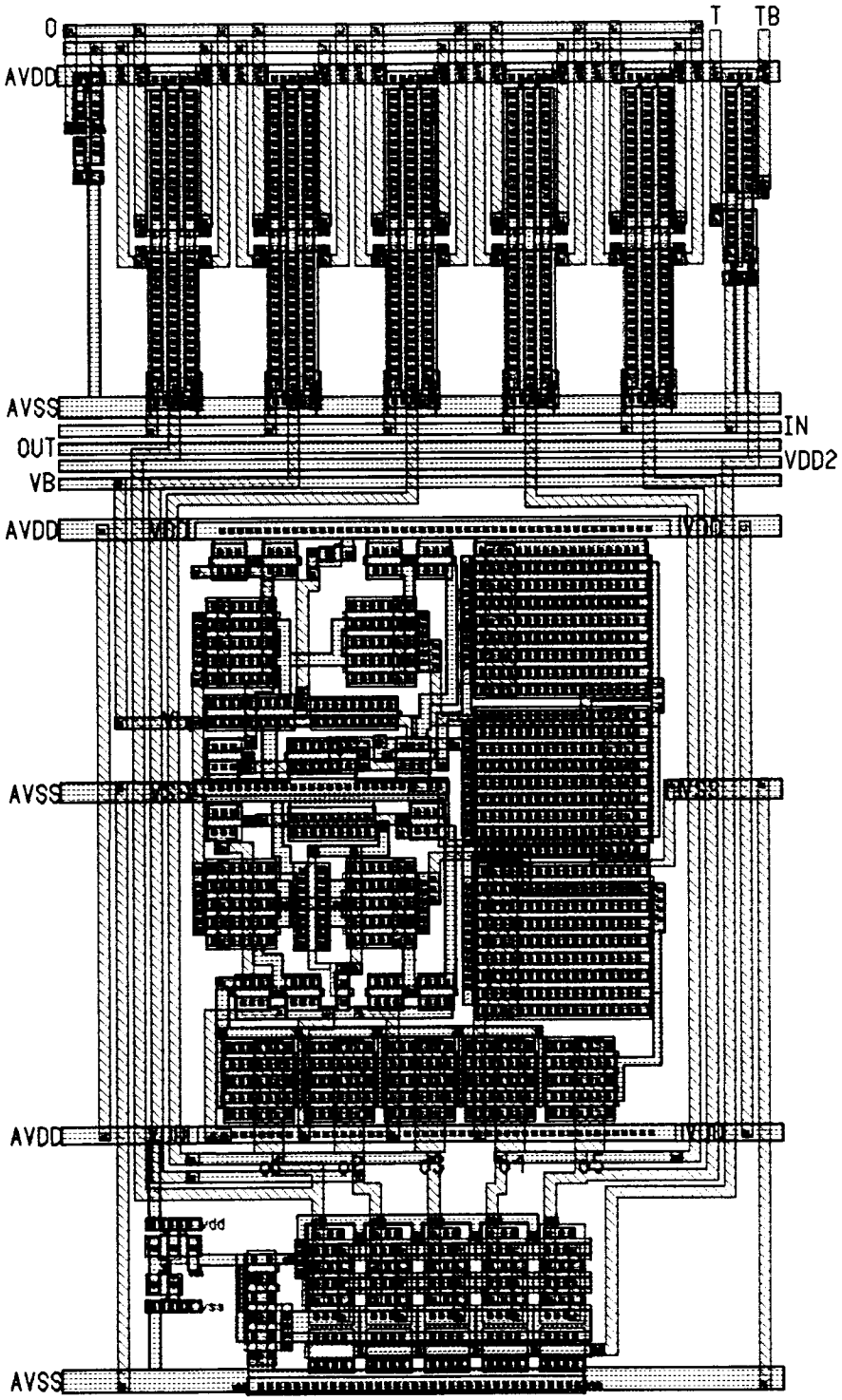


Figure 3.13:Layout of RC^3.

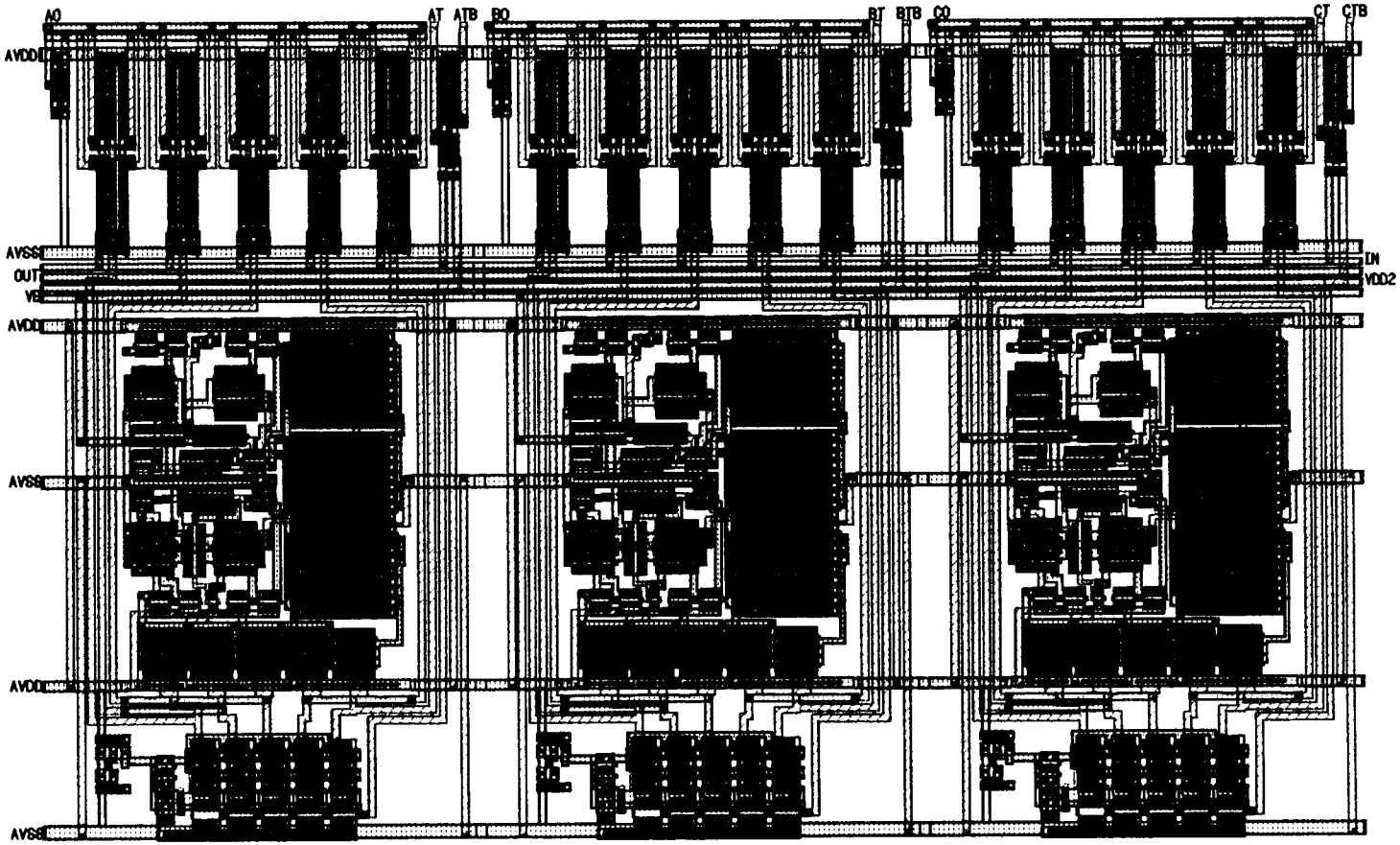


Figure 3.14:Layout of the resonator.

100MHz. As this figure shows, the output grows linearly, but does not reach steady-state within the time span of this simulation run.

3.3 Voltage Comparator

The basic analog to digital conversion is done at the comparator. Since the modulator's internal signals are currents, the comparator needs to be a current comparator. For high-speed operation, a current-comparator needs to have a low input resistance. However, high-speed comparators are most conveniently implemented with cross-coupled inverters, which have a high input resistance. By noting that during the track phase the RC^3 cell produces a voltage at the *IN* terminal which is monotonically related to the input current, we see that a voltage comparator connected to this terminal could be used to detect whether i_{IN} is positive or negative.

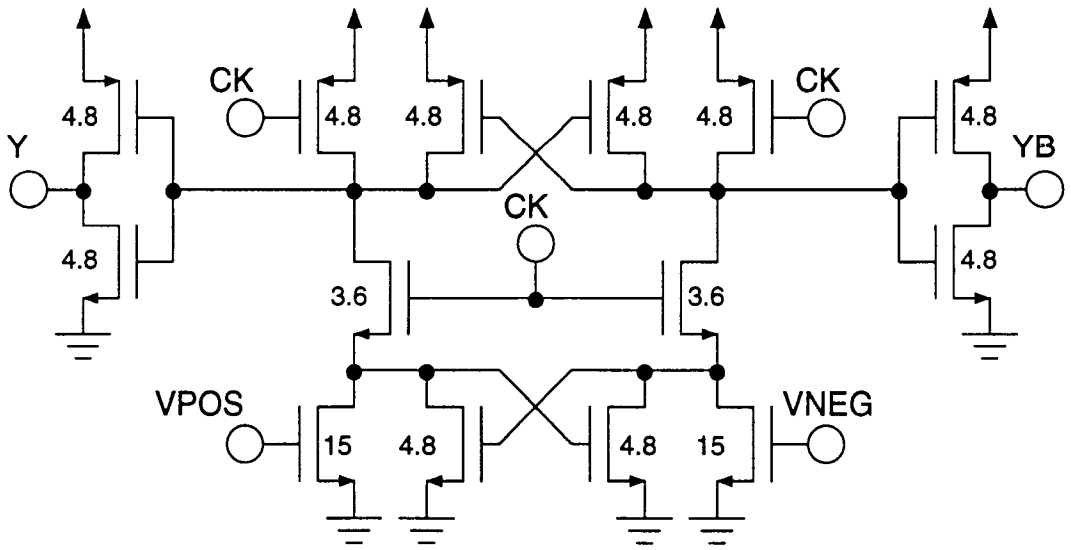


Figure 3.15:The voltage comparator.

Shown in Figure 3.15 is the schematic for the voltage comparator [16]. The comparator needs to compare at a speed of 100MHz. As pointed out above this was one of the reasons the voltage comparator was chosen. It should be noted that all the transistors are of minimum length. The performance of the modulator is relatively insensitive to comparator offset and hysteresis since the effects of these impairments are attenuated by the same shaping that attenuates the quantization noise. As shown in Figure 3.15 the latch has cross-coupled devices that are strobed at their drains rather than sources, to eliminate backgating effects and promote faster regeneration [16]. The latch is reset during each clock cycle and the result of each comparison stored in a flip-flop (not shown). The comparator output for a varying input is shown Figure 3.16. Simulations indicate that it is possible to clock the comparator at 100MHz.

3.4 The Digital-to-Analog Converter (DAC)

The feedback coefficients shown in the block diagram in Figure 2.8 are achieved by digital to analog converters which are not shown in the block diagram explicitly. The

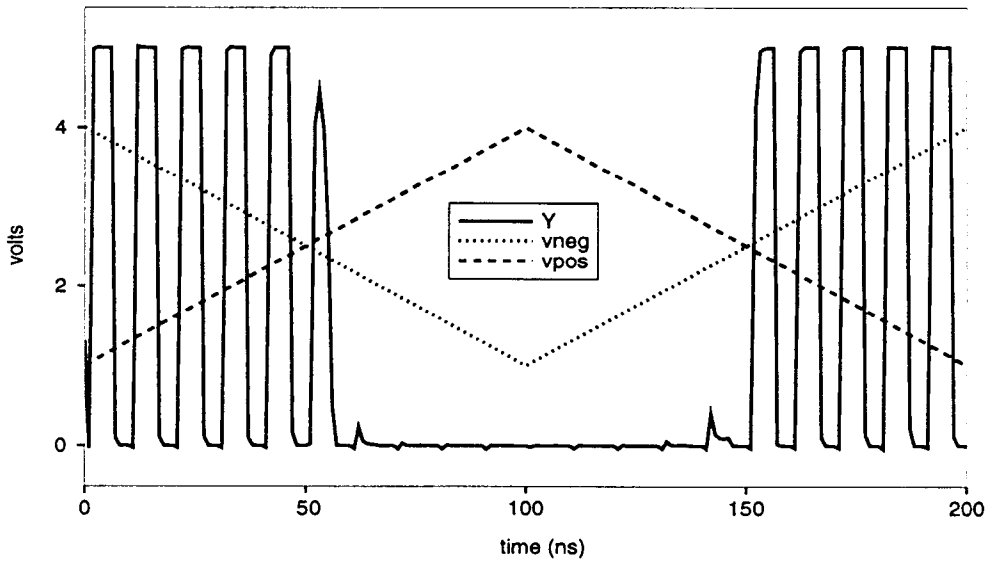


Figure 3.16:Comparator output for a 100MHz clock.

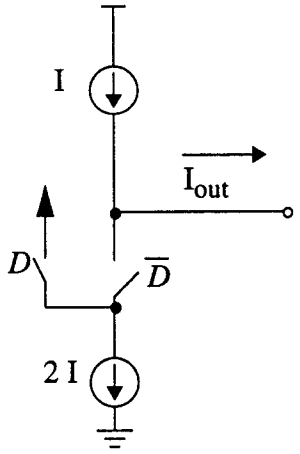


Figure 3.17:The basic architecture of the DAC.

architecture of the DAC is shown in Figure 3.17. When the switch $\overline{D}$ is open a current I flows in the direction of I_{out}. An equal amount of current flows in the opposite direction when switch $\overline{D}$ is closed. The digital input is given to the switch $\overline{D}$ and the corresponding analog output current is I_{out}. Since the modulator requires DAC currents of 516μA, 200μA, 235μA and 125μA the transistor dimensions are scaled even though the same architecture is used for all. The output impedance and voltage swing is the same as that of the bias current of the regulated cascode current copier since the DACs feed into the same node as the bias current. Thus care needs to be taken to ensure that the DACs have an output impedance of 1MΩ and a voltage range of 1.7V-3.8V. The same architecture as the bias current source of RC^3 is used for the top current source of all DACs. The transistor schematic and block diagram used for the current source I are shown in Figure 3.18.

Table 3.4:Transistor sizes for current source I of the DACs.

I (μA)	M_1 W/L	M_2 W/L	M_3 W/L
125	100/1.6	100/1.2	15/5
200	200/1.6	200/1.2	50/10
235	200/1.6	200/1.2	60/10
516	300/1.6	300/1.2	130/10

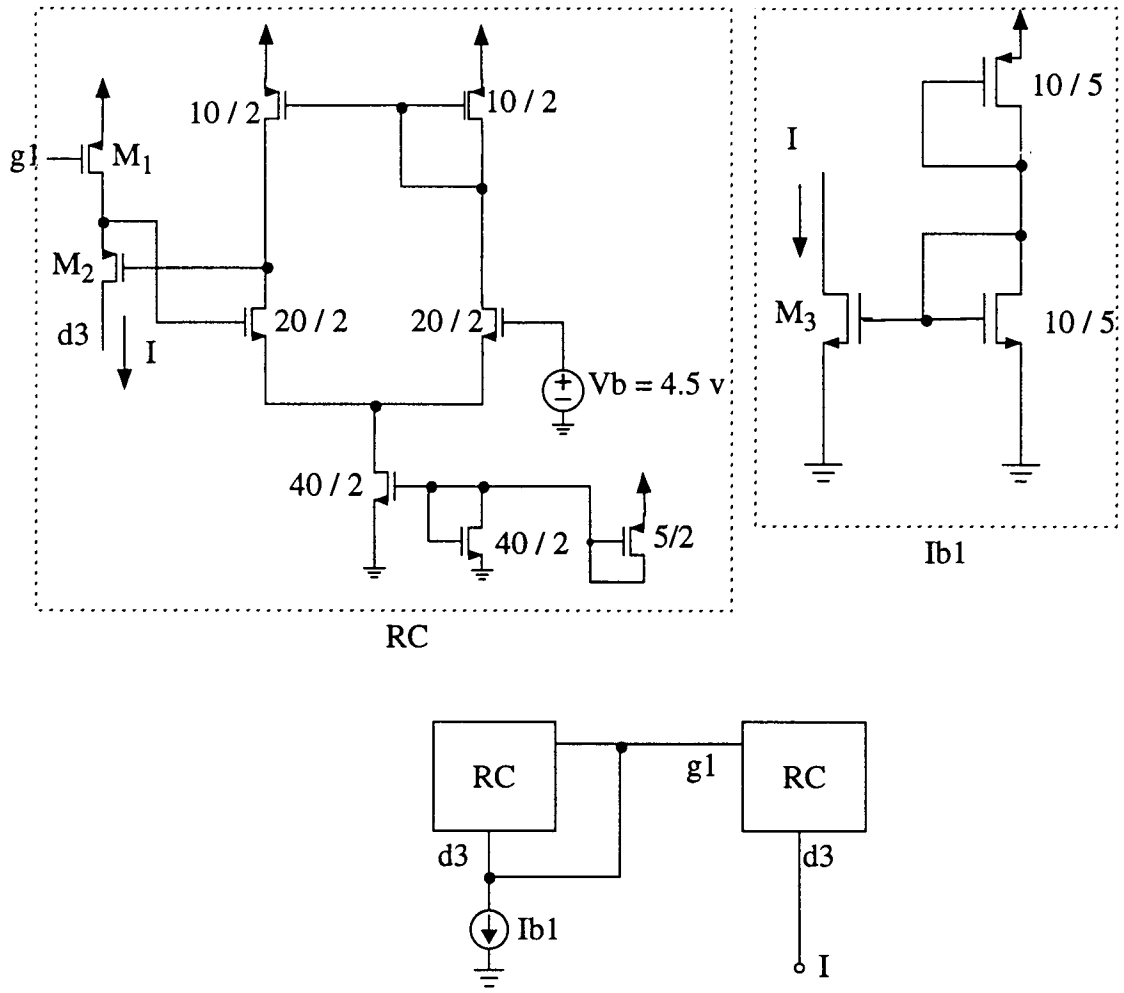


Figure 3.18:Transistor schematic biasing of the current source I for the DACs.

Simulations show an output impedance of 1.2MΩ and an output voltage range from 0 - 4v.The transistor sizes for current source I for various DACs are shown in Table 3.4. The sizes of the cascoded transistors are smaller than those used in the 1.5mA current source since the current levels are lower. The opamp serves the same purpose, namely it increases the output impedance.

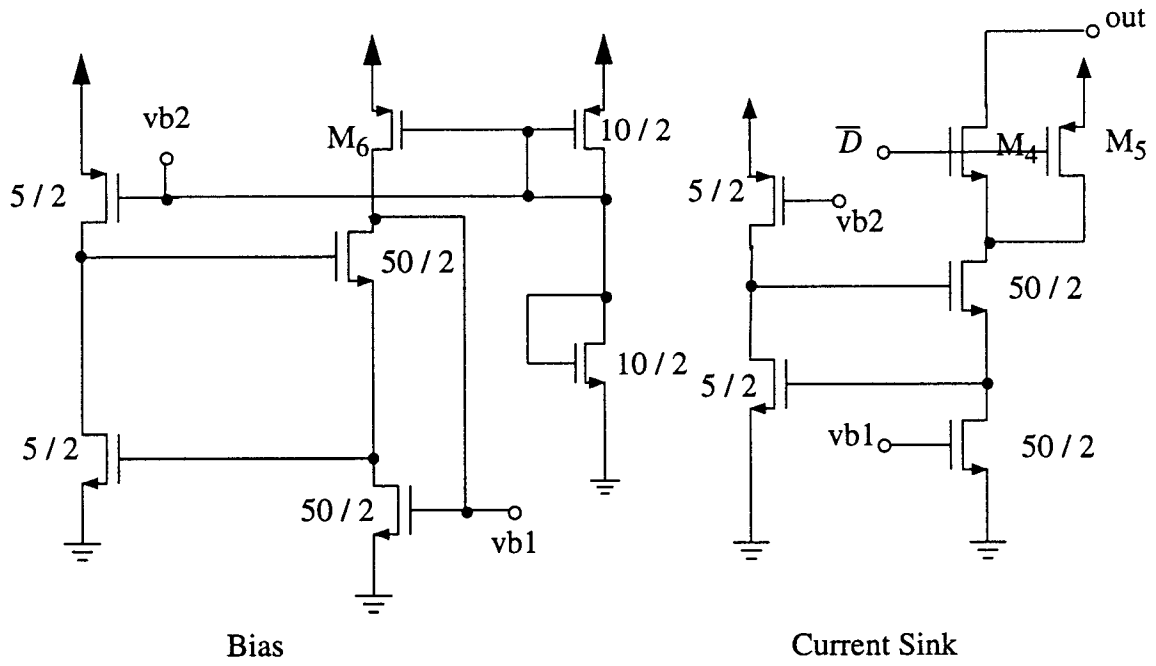


Figure 3.19:Transistor schematic of current sink 2I and its bias circuit.

The current sink 2I can be constructed easily since it consists of n-channel transistors. The transistor M_4 acts as a switch for the DAC. The saturation of the current sink 2I, when it is not being used is prevented by the transistor M_5. The current sink is essentially a regulated cascode current copier with an output switch and a fixed control voltage, v_{b1}. This ensures a high output impedance and large output voltage swing. The bias circuit is the same as the current sink where the current in it is set by a p-channel, n-channel diode connected transistor pair. The bias voltages are generated by diode

Table 3.5:Transistor sizes for current sink 2I of the DACs.

I (μA)	M_4 & M_5 W/L	M_6 W/L
125	15/5	13/2
200	50/10	20/2
235	60/10	23/2
516	130/10	50/2

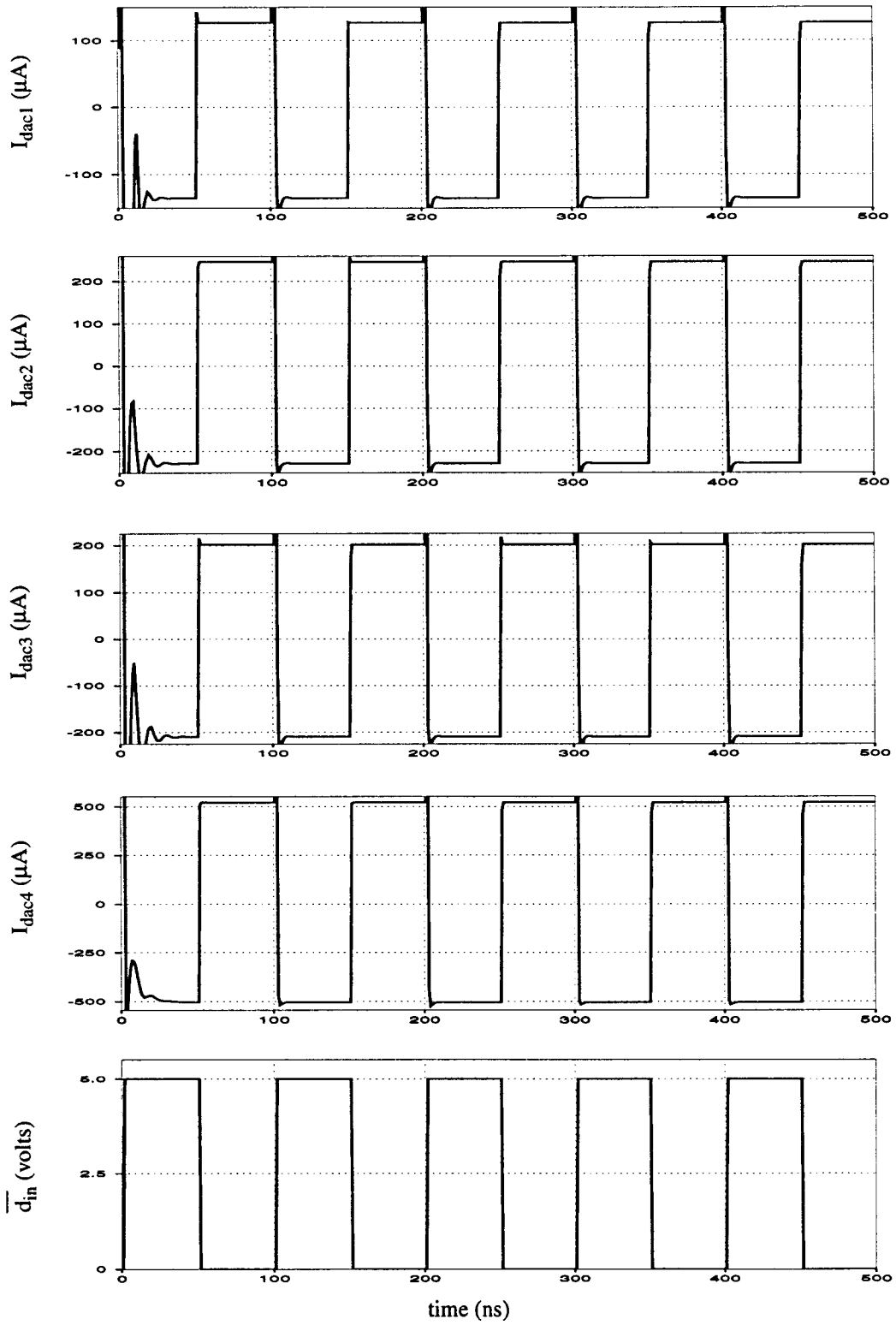


Figure 3.20:Output waveforms of the DACs.

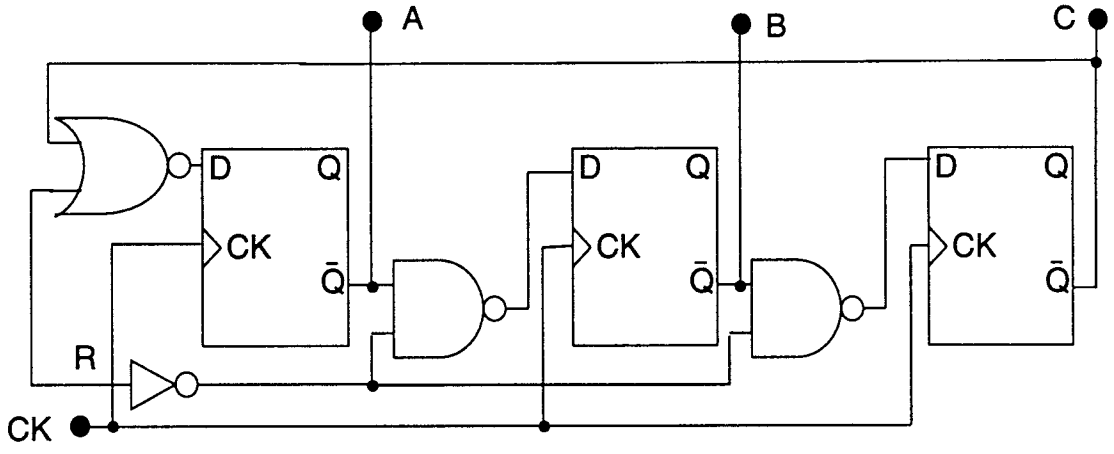


Figure 3.21:Logic for the three phase clock generation.

connecting the respective transistors which correspond to the current sink. The impedance and voltage swing remain the same for the current sink too. Simulations indicated an output impedance of 1.3MΩ and an output voltage swing range of 0 - 4.1V. The transistor sizes of the current sink 2I are shown in Table 3.5. The output currents for the various DACs are shown in Figure 3.20. Non-minimum lengths transistors have been used in top and bottom current sources so that a high output impedance can be achieved.

3.5 Clock Circuit

The previous chapter showed that a three phase clock is needed by the modulator. There are some subtleties in the clocking which result from the use of switched-currents and these warrant further explanation. The guiding consideration behind all timing requirements is that no topology-determining switch or inactive track switch can be allowed to change state until after the active track switch has been opened. This ensures that the gate of the memory transistor is isolated before the cell configuration is changed.

In terms of the signals illustrated in Figure 2.11, this requirement dictates that the AT, BT and CT track signals must go low before any of the topology-determining switches (those controlled by AI, AO, BI, BO, CI or CO) change state. Note that in contrast to switched-capacitor circuits, the topology-determining switches can be opened or closed in any order; there is no need for non-overlap in these signals. In order to generate the three basic phases from the main clock the circuit shown in Figure 3.21 was used. This is a simple shift register which is reset to a state where only one of the phases is high and is then shifted with the main clock. While testing it was found out that a simple reset pulse (such as from a push button) often put the register into an incorrect state since such a reset pulse contained numerous glitches. To simplify testing, future designs should ensure that all flip-flop states lead to the desired period-3 behavior. From the three basic phases, the track and the output phases can be generated using the circuit shown in Figure 3.22. This circuit uses

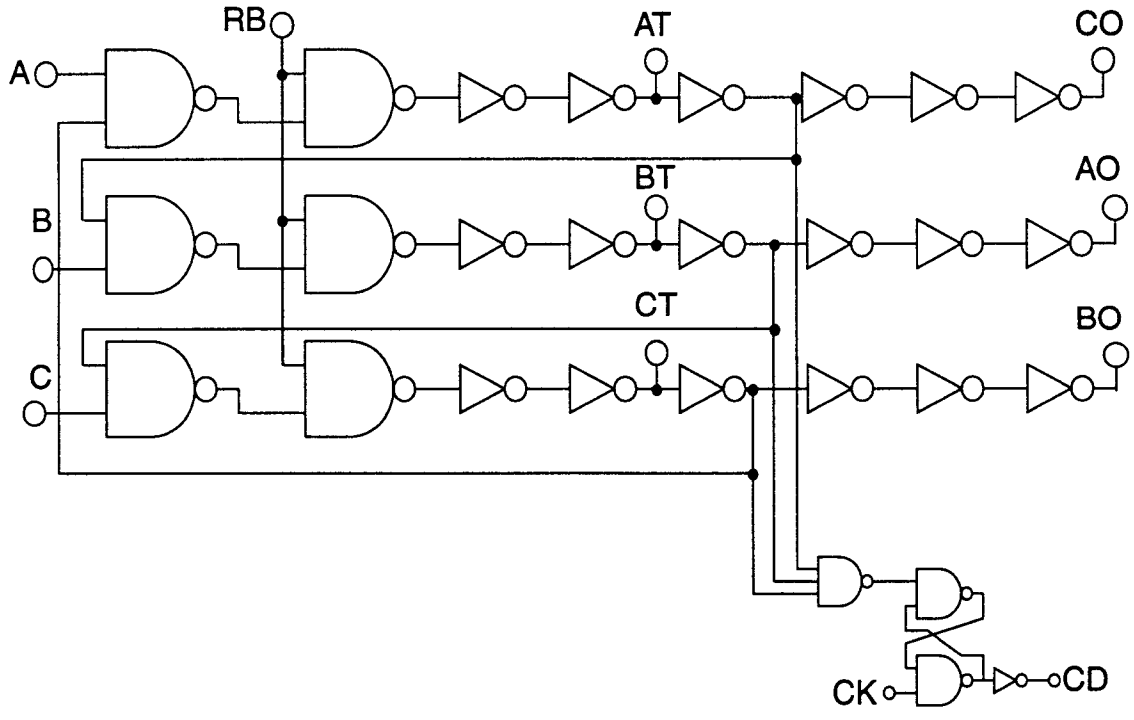


Figure 3.22:Logic for generation of track and output phases. Each input phase is the inverse of the corresponding output phase.

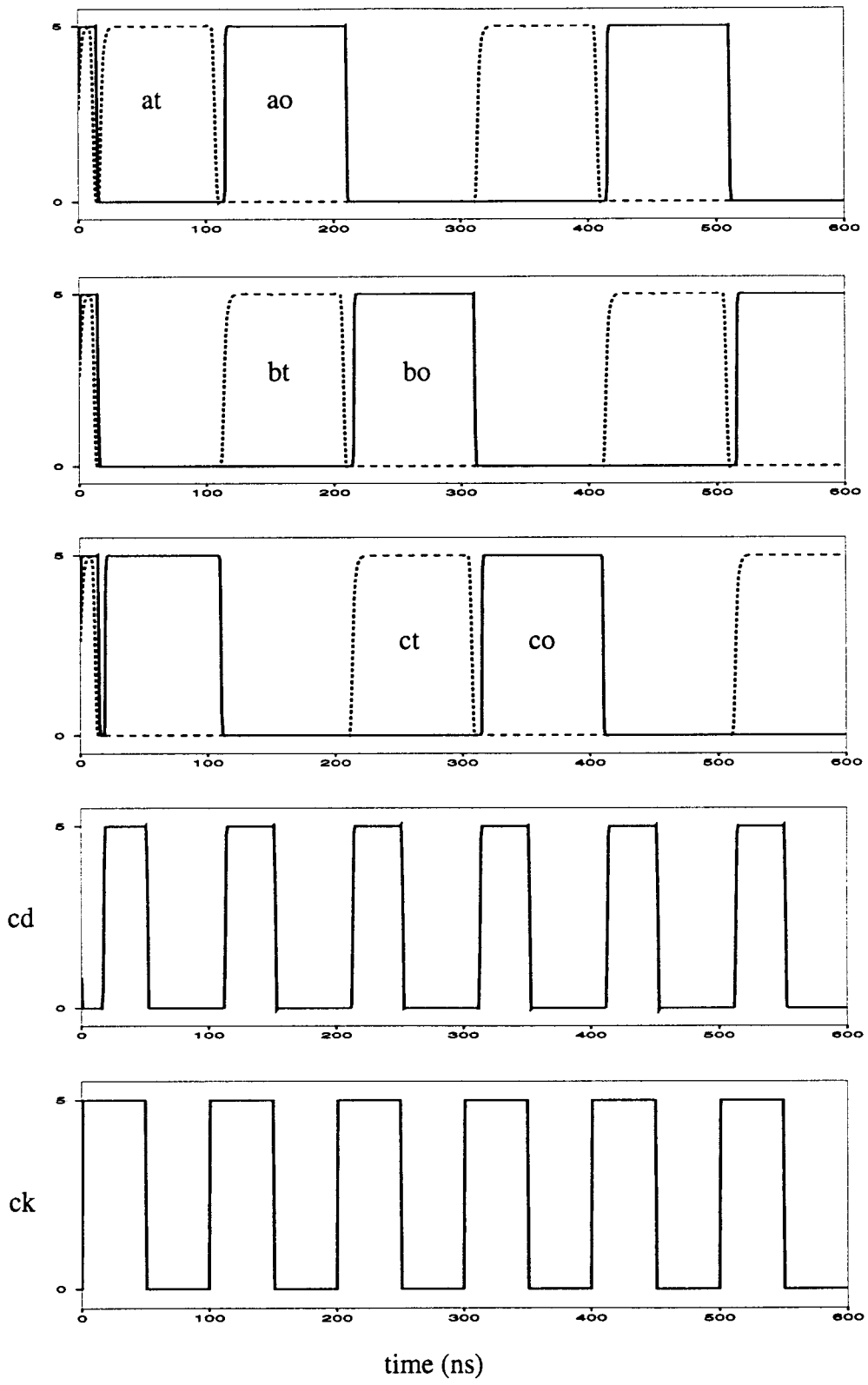


Figure 3.23:Waveforms of the clock circuit.

three cross coupled NAND gates to generate the three non-overlapping track phase signals and the output signals which follow them.

The clock circuit generated only the output phases which are inverted to produce the input clocking phases. This made the design of the clock circuit and its wiring to the analog part much easier. The need of clock phase CD will be evident in the next section. The waveforms of the clock circuit are shown in Figure 3.23.

3.6 SI2: The second order modulator.

Since it was observed in section 3.3 that it was easier to design a high speed voltage comparator than a high speed current comparator the last section of the modulator had to be modified. The new connection converts the last block into a $\frac{1}{1+z^{-2}}$ block instead of $\frac{z^{-1}}{1+z^{-2}}$ block since the input voltage is compared to detect whether the current is positive or negative one cycle early. Figure 3.24 illustrates the modified system. The comparator is connected to the input of the resonator and uses the input voltage of an RC^3 cell which is permanently in the track mode as its reference. The output of the comparator is high if the current being memorized by the resonator is positive. The output of the RESON block is not strictly needed, but provides a convenient test point. To prevent the internal current copier which drives the output terminal from saturating, the output terminal is connected to $V_{DD}/2$.

Figure 3.24 also shows the feedback circuitry and the associated control signals which make the merged resonator-comparator function as a second-order bandpass modulator. The comparator is tripped near the end of the track phase by rising CK and produces a stable output by the time CK falls. Thus the comparator provides the small amount of delay needed to shift a signal from time slot n to time slot $n+1$. The first D-flip flop is clocked by falling CK so as to latch the comparator output and so produces

approximately another one half-period of delay. The second D-flip flop is clocked so as to hold the input to the current DAC constant until all track signals are low; it produces slightly more than one half-period of delay. This requires that CD rises when all the track phases are low while the clock is high and falls when the clock goes low. This is accomplished by the circuit in the lower right corner of Figure 3.22.

SI2 was simulated using ideal 100 MHz clocks and mix of macro-model and transistor blocks to verify its operation as well as the timing and the polarity of all signals. The results of these simulations are shown in Figure 3.25. At time zero, SI2 leaves the reset condition, $Y = 0$ and RESON produces an output of 0 mA. The RESON output current in the second period is 0.3 mA, which is the negative of the sum of the -0.5mA feedback current and the 0.2 mA input current of the first time period. By continuing these

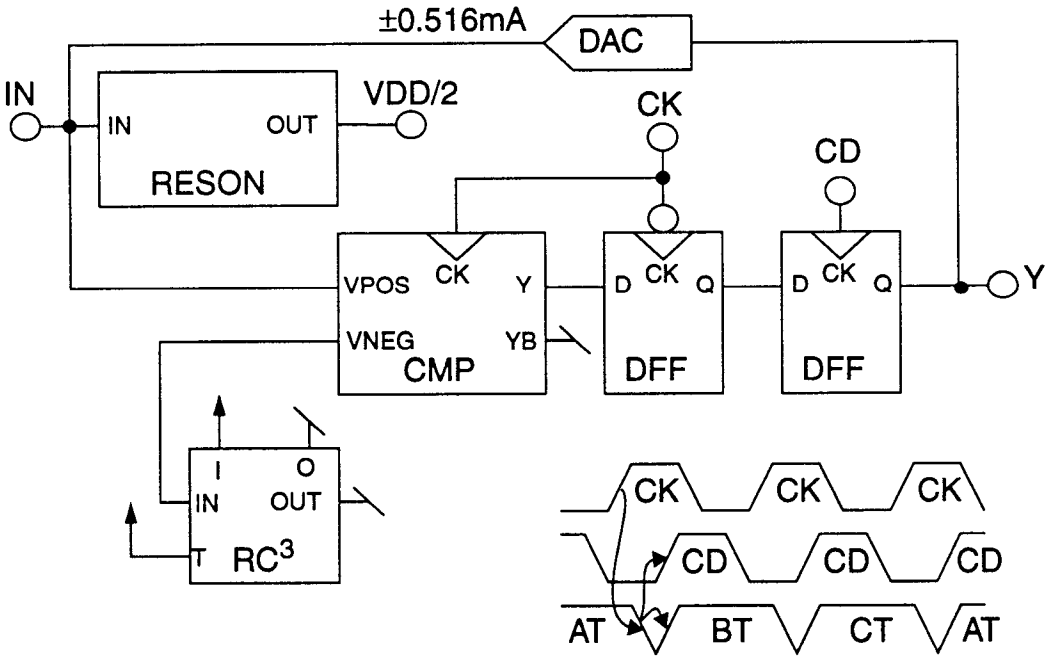


Figure 3.24:The merged resonator-comparator and feedback circuitry for a second-order bandpass modulator.

calculations, the simulation can be shown to be consistent with the desired operation of the modulator.

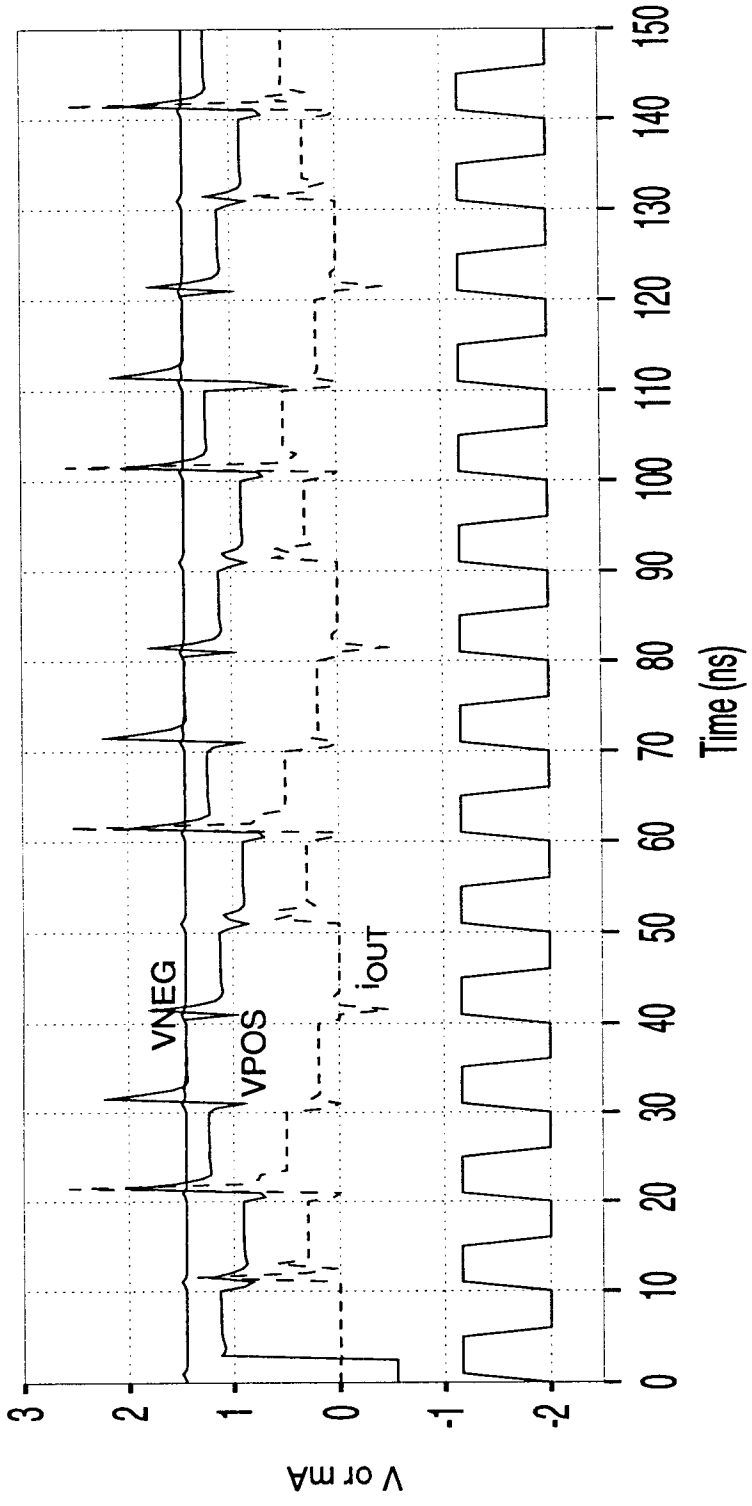


Figure 3.25:Simulation of SI2 using mixed ideal/real components. The input is a 0.2 mA current pulse during the first clock period and zero thereafter and the reference current is 0.5 mA. The output current is a periodic waveform: (0, 0.3, 0.5,0.2) mA, which is consistent with the desired operation

Chapter 4. Testing

This chapter discusses the test results from the individual parts of the modulator. Based on the results, performance levels are evaluated and design rectifications are suggested.

4.1 Current source

The simplest of all the test devices is I_{b1}, the 1.5mA bias current source for RC^3. The test setup is shown in Figure 4.1. The test setup is used to measure the current of the source at various output voltages. A voltage source is used to control the output voltage of the current source. A constant current of 1.54mA was observed for the voltage range from 0 to 4.1V. Since the required maximum output voltage was 3.8V, the results showed that the current source could operate for the desired output range. The output impedance was found from the slope in the region of operation of the graph shown in the inset of Figure 4.2. The output current varied by 4μA over the 4V operating range and thus the current source had an output resistance of ≈1.1MΩ which is quite near to what had been observed from the simulations. The comparison of the test results with the simulated results are shown in Table 4.1. These results indicate that the current source (including the embedded op-amp) performed as desired.

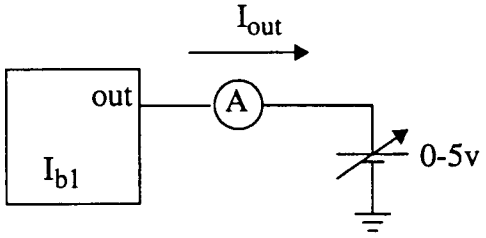


Figure 4.1: Test setup for 1.5mA current source.

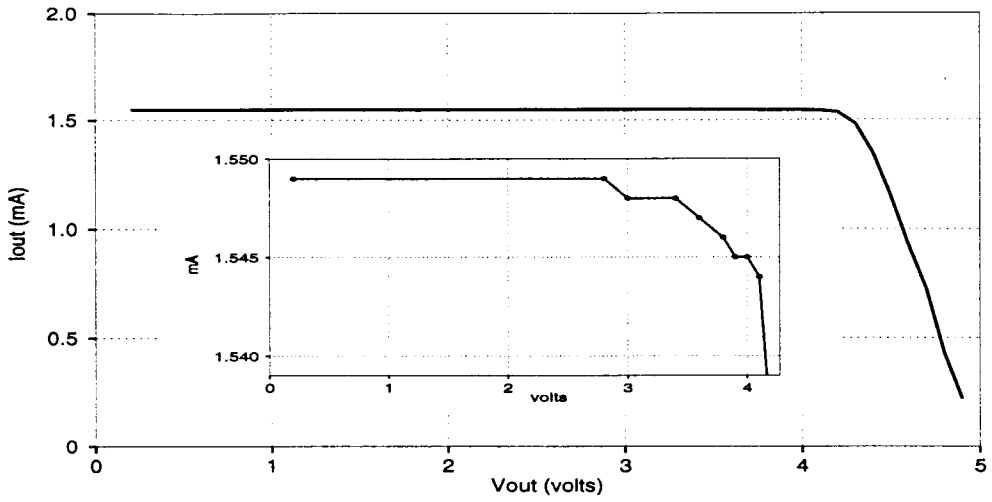


Figure 4.2: Graph for measuring the output impedance of the current source

Table 4.1:Performance of the current source under test.

Parameter	Simulated	Test	difference
I	1.56	1.54	1%
r_{out}	1.24	1.12	10%
$V_{o,max}$	4.23	4.10	3%

4.2 Digital-to-Analog Converter

The second block to be tested was the 516μA DAC. Since this requires the same kind of output impedance and voltage range as the 1.5mA current source, the test setup was very similar. As shown in Figure 4.3 the test structure is given a digital input and its output current is tested. For a digital input 'high', the output current was observed to be -512μA and for a digital input 'low', the output current was observed to +514μA. For measuring the maximum output voltage, the digital input was set 'low' and the output voltage was increased from 0V. It was observed that the output current was almost constant in the

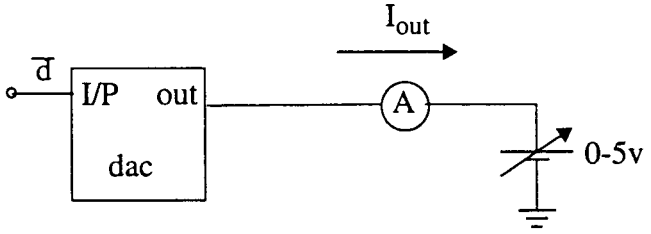


Figure 4.3: Test setup for the 516µA DAC.

region from 0 to 4V of the output voltage. The output voltage versus the current is plotted graphically in Figure 4.4. From the inset of Figure 4.4, the output impedance was measured to be 1.2MΩ from the slope of the graph in the region of operation. These results are similar to those observed from the simulations. The output voltage range for a 'high' digital input is not illustrated since it was observed to be similar to the 'low' digital input.

The DAC was given an input of 0 - 5v at a speed of 1MHz and the resulting output was observed on an oscilloscope. The output is as shown in Figure 4.5.

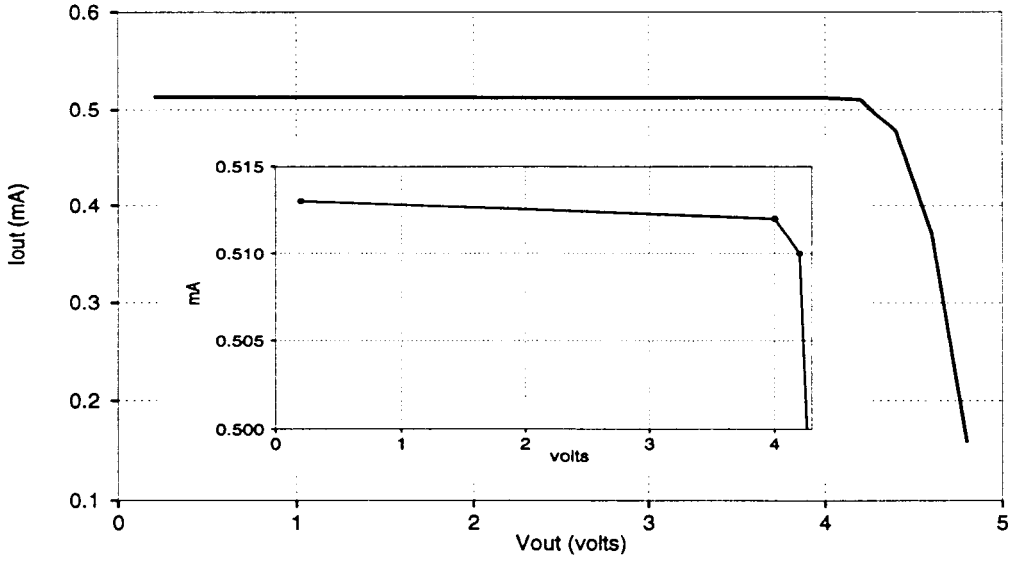


Figure 4.4: Graph for measuring output impedance of 516µA DAC.

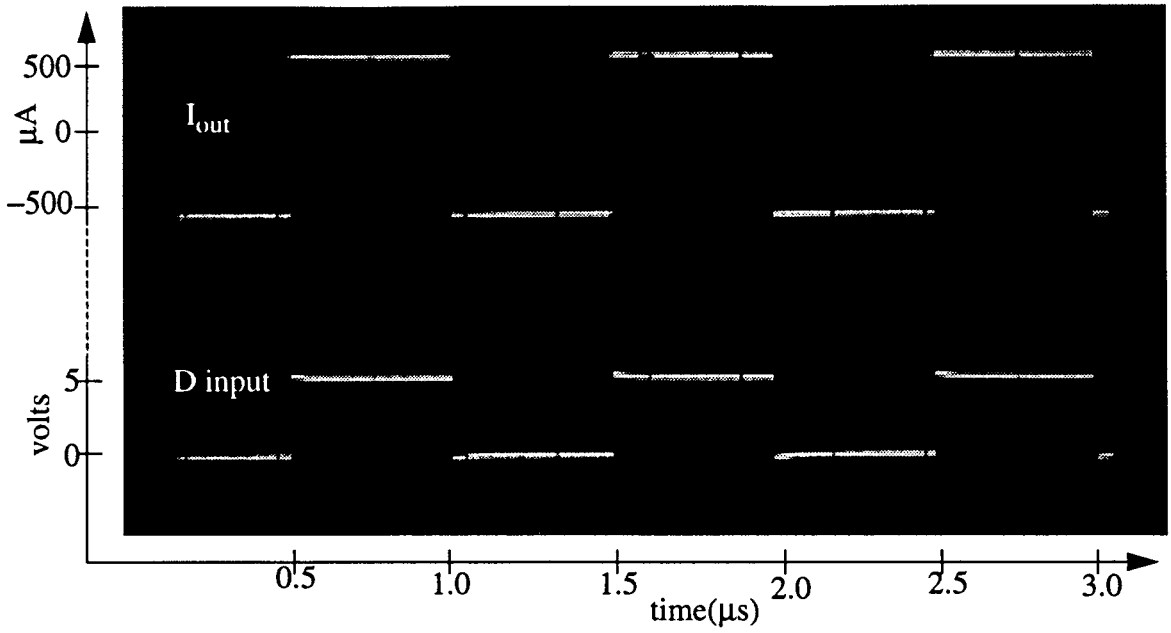


Figure 4.5: Output of the DAC under test at a speed of 1MHz.

4.3 Comparator

The device tested next was the high speed voltage comparator. In order to test the comparator a constant input of 2.5V was given to the negative input while the voltage at the positive input was changed between 1V and 4V and the clock input received a 1MHz signal. The resultant comparator output is shown in Figure 4.6. The results were similar to those from simulations. The test setup was not sufficient to clock the comparator at higher speeds.

4.4 Clock Circuit

The initial test results showed that the clock circuit was not functioning as expected. It was later observed that this was due to the way the circuit was being reset. Since the reset used initially had glitches in it, the flip-flops in the circuit were often put in an incorrect state. A sharper and glitch free reset was used to correct the problem. The resultant waveforms were then observed to be logically correct. The non-overlap between the

closing of the track switch and the output switches could not be determined easily because the non-overlap is both of short duration and only guaranteed internally (only buffered waveforms are available at the pins of the chip).

The present clock circuit puts the modulator in a 'near zero' initial state. This is due to the fact that during reset all the output switches are closed and the input switches are open. In order to achieve a 'zero' initial state both the output and input switches have to be open and the track switch connected to the drain of M_3. The present design and clocking do not achieve this. In order to open both the output and input switches, it should be observed that none of the output and input clock phases can be derived as a complement of the other. Otherwise both the input and output switches will not be open during rest. So future designs should see to it that the clocking during reset puts the modulator in a 'zero' initial state.

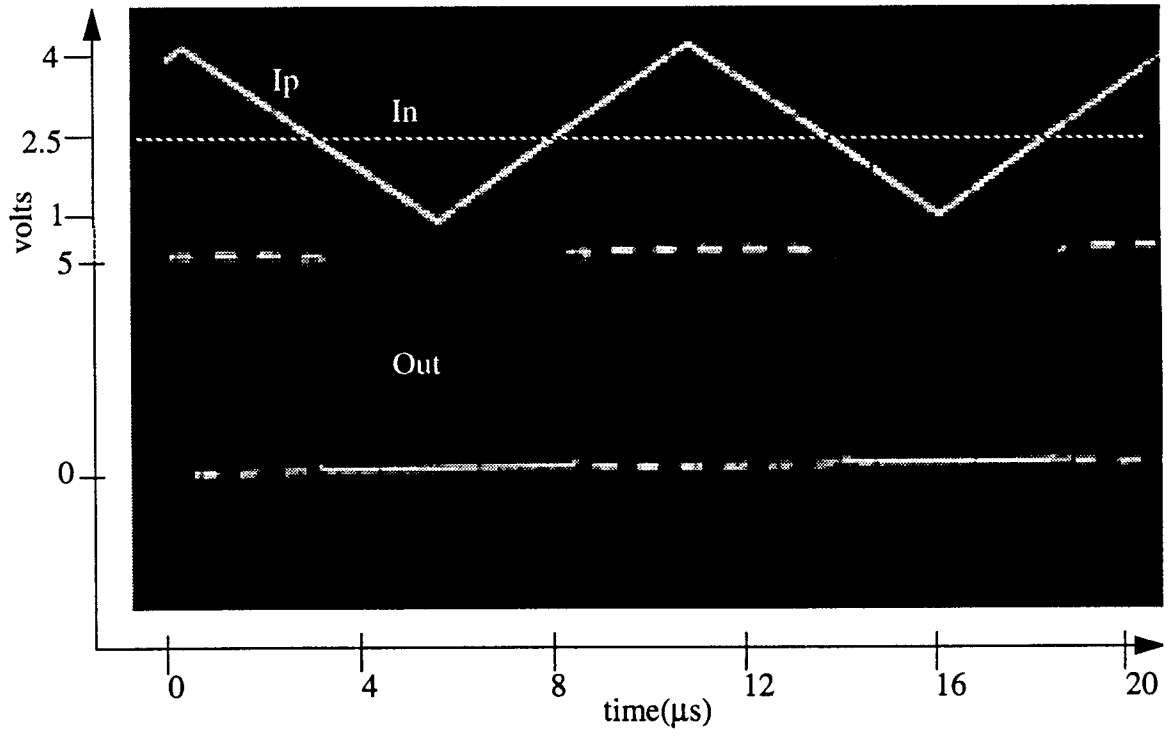


Figure 4.6: Output of the comparator under test.

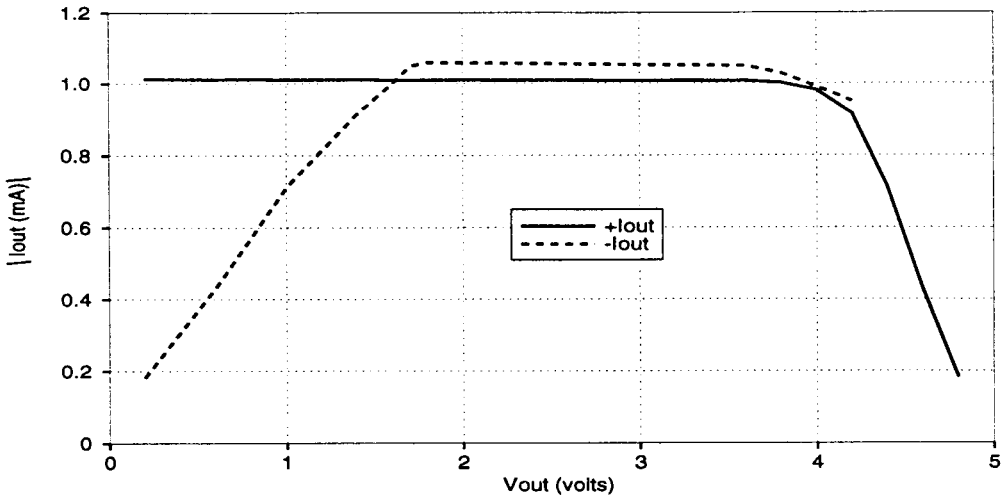


Figure 4.7: Output impedance of RC^3.

4.5 The current memory cell: RC^3

The most important of the blocks to be tested was the current copier. In order to measure the output impedance the track switch and the output switch were closed and the input switch was open. This put the circuit in the *hold* mode. For a particular input current the output current for various output voltages was measured. The graph in Figure 4.7 shows the measurements for an input current of ± 1mA. The output impedance was approximately 0.9MΩ for an output voltage swing from 1.8 - 3.84V.

Since it was established that the output voltage swing and impedance were as expected, the functionality of the block remained to be verified. A sine wave was given to the input and the output was observed for a fixed clock frequency. It was noted that the output indeed was a sampled sine wave and was delayed by one phase of the clock. This demonstrated the memory cell functioned as desired. The current copier could take in currents in the range of ± 1mA without any saturation. Shown in Figure 4.8 is the output of the current memory cell for a 0.125MHz input when clocked at 4MHz.

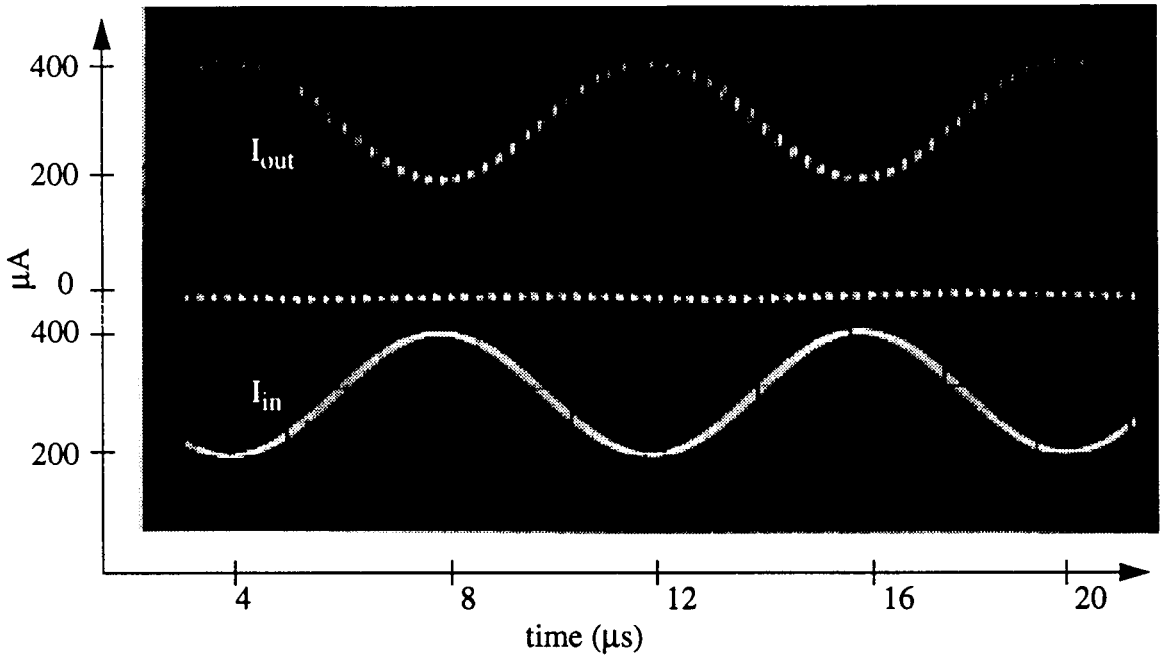


Figure 4.8: Output of RC^3 for a 0.125MHz sine wave clocked at 4MHz.

Since charge injection is one of the important aspects for the memory cell, its magnitude had to be computed. The signal-dependence of the charge injection is especially important since this can affect the resonator's transfer function. Shown in Figure 4.9 is the setup for measuring the signal-dependent charge injection. The input and output nodes of the cell under test are connected to the signal current and the current copier is clocked. In the *track* phase the cell memorizes the input current I, while in the *hold* phase the same

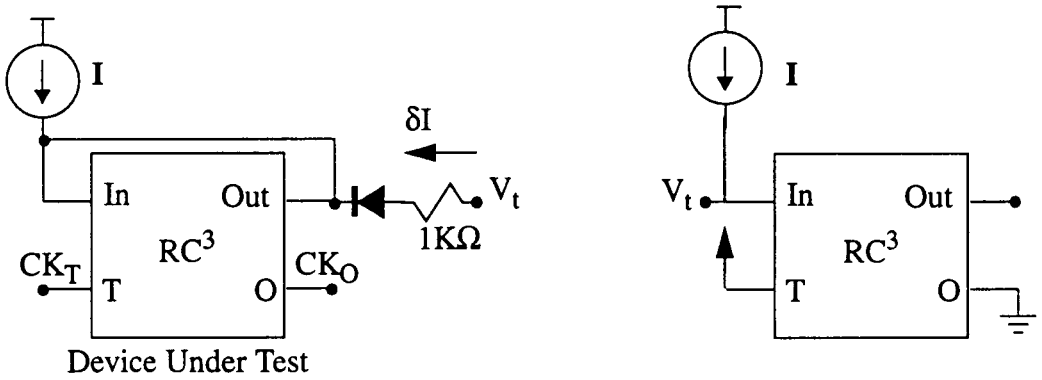


Figure 4.9: Test setup for measuring charge injection in RC^3.

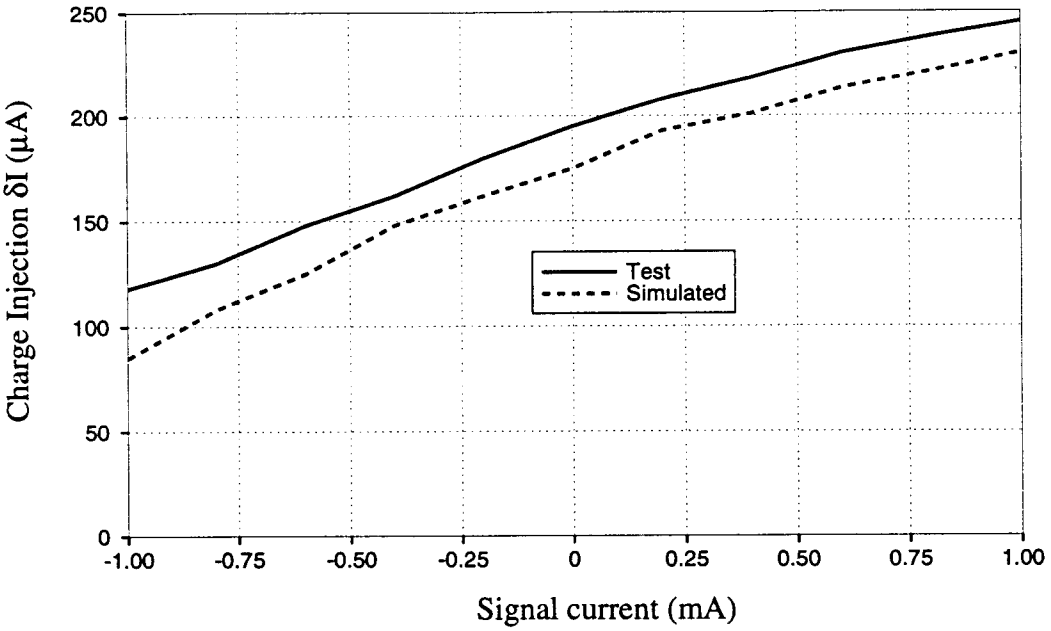


Figure 4.10:Signal-dependant charge injection for the current copier.

current flows into the output node. Due to charge injection any difference between the input and the output current δI would flow through the resistor R and diode D which are connected to a voltage V_t. The voltage V_t is generated by another memory cell sinking the same amount of current and permanently in the track mode. This voltage prevents any current flow into the resistance R during the track phase. Charge injection was measured for an input current range from -1mA to +1mA. From the test results it was observed that the charge injection increased when the signal current increased as shown in Figure 4.10. This indicates that the performance of the resonator would be affected.

4.6 Reson

Since the current memory cell was shown to be functional, the next block to be tested was the resonator. The output voltage range and impedance had been established earlier for the memory cell, and did not need to be repeated.

The positive slope of the curve in Figure 4.10 indicates that the current memory cell would have a current gain greater than 1 and consequently the resonator would be unstable. Measurements showed that this was indeed the case. However, by loading the input of the resonator with a resistor as shown in Figure 4.11, this effect could be partially corrected. The resistor needs to be adjusted so that it absorbs the extra signal current caused by charge injection. If the resistor is too large, the circuit stays unstable; if the resistor is too small, the gain of the circuit at resonance is degraded.

After careful adjustment of R_{comp}, to ~25kΩ, it was verified that for a sine wave input the output was a sampled sine wave. Theoretically the resonator was supposed to have a gain of 1000 at the signal frequency of $f_s/4$. From the waveforms in Figure 4.12 it is clear that only a gain of little more than 100 could be achieved. Attempts to adjust R_{comp} so that higher gains could be observed resulted in chaotic behavior.

In the previous section it was observed that there was some amount of signal-dependent charge injection in the current copier. This charge can be characterized as

$$\delta I = I_0 + kI_{in} \tag{4.1}$$

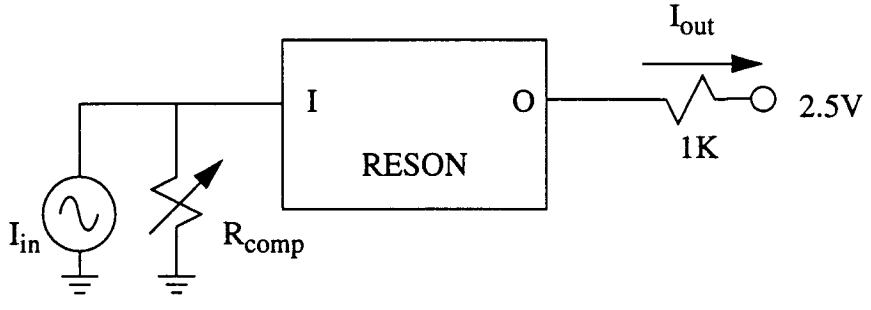


Figure 4.11:Adding a resistor to the input of the resonator.

where I_0 is a constant current. This is reflected in the resonator time domain equation as

$$I_{out} = -((k+1)I_{out}(n-2) + I_0(n-1) + (k+1)I_{in}(n-1)). \quad (4.2)$$

So that the transfer function of the resonator is

$$I_{out}(z) = \frac{-z^{-1}}{1 + (k+1)z^{-2}} (I_0(z) + (k+1) I_{in}(z)). \quad (4.3)$$

This indicates that for values of $k > 0$ the poles of the resonator are outside the unit circle and the resonator saturates very quickly. Test results were in agreement with this, since the resonator was observed to saturate in about 15 clock cycles.

Since scaling for the coefficients of the modulator was done in the resonator itself, it was important that this be tested. It was initially observed that the scaling between two

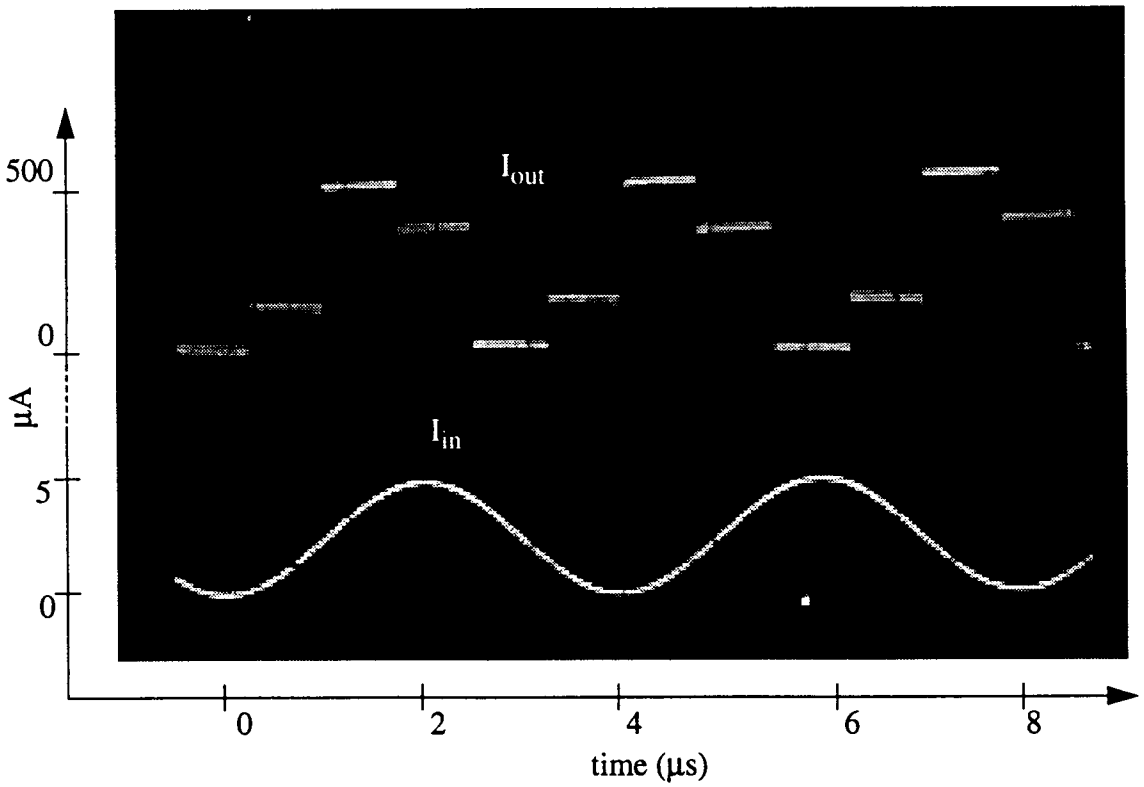


Figure 4.12:Output waveform of the resonator under test. The input signal frequency is 0.25MHz and the resonator is clocked at 1MHz.

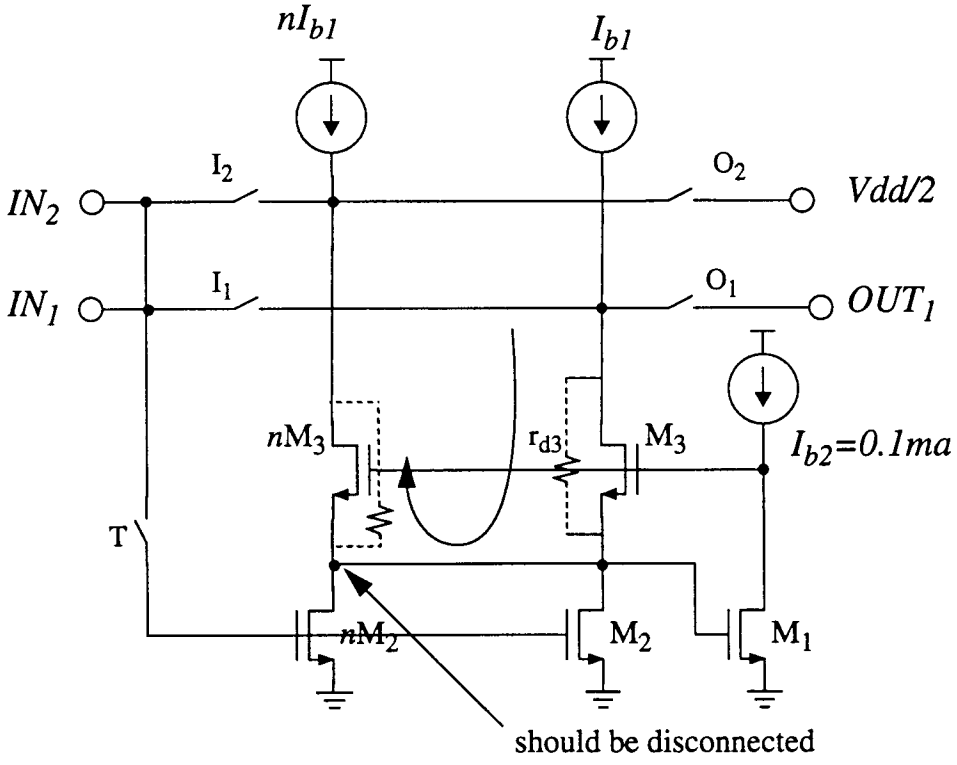


Figure 4.13:Decrease in output impedance due to the erroneous scaling method.

parts of the resonator was not as predicted from the simulations. Later when the unconnected output was fed to a voltage source, scaling between the parts was evident. This brought out a design flaw, that during scaling the output impedance of the resonator was not sufficiently high. The reason for this is that the drain of the unconnected part of transistor M_2 is in the regulatory loop and thus current flows along the path shown in Figure 4.13. As a result of this unforeseen effect, the output impedance is only $r_{d3}(1+1/n)$. Thus, the gain of the next resonator in the chain is severely degraded. This is easily rectified by disconnecting the unused portion of M_2 as indicated in Figure 4.13. A preferred solution is to perform scaling at the output of the resonator, since this circumvents problems caused by scaling mismatch among the three current memory cells of the resonator.

Chapter 5. Conclusions

5.1 Summary

A brief tutorial on delta-sigma modulation was presented to the reader in Chapter 2. Bandpass modulation was offered as a means for converting low-bandwidth high-frequency signals. Chapter 2 also discussed the merits of switched-currents and introduced an architecture for an eighth-order bandpass modulator, SI8. Implementation of this modulator with 100MHz clock frequency was the original goal of this thesis.

The design of the sub-blocks needed by SI8 was detailed in Chapter 3. The regulated-cascode current copier, RC^3, which is the critical building block of the modulator, was discussed in detail. Simulations showed a settling time of 9.6ns and a current transfer efficiency of 99.9%. One surprise was the level of difficulty in the design of the 1.5mA current source. This block required an internal opamp to achieve sufficiently high r_{out} and consumed a little more than half the area of the RC^3 cell. The layout of each part of the resonator and of the resonator as a whole were done in a manner such that the blocks would connect together easily. The design of voltage comparator was also given. The design of the four DACs was simplified by making use of the earlier current sources. The trade-offs involved in the number of clock phases and their generation was explained. Simulations of the last part of the block diagram SI2, indicated that it was expected to clock at 40MHz.

The testing of the chip showed that most of the individual blocks performed as expected, although the modulator as a whole was not functional. The current source and the DACs showed that they indeed had a high output impedance of 1MΩ and the required voltage swing. The clock circuit had initial problems with reset which were later overcome. The logical correctness of the clocks was verified and the circuit performed up to 1MHz.

Beyond this speed the test setup was not adequate. RC^3 demonstrated a high output impedance and adequate voltage swing. The basic functionality was verified for a sine wave input. After considerable tinkering the resonator showed a gain of only 100 at its resonant frequency whereas a gain of 1000 was expected. This degradation was determined to be signal-dependent clock injection. Test results also uncovered a flaw in the scaling of the output current which needs to be corrected in future revisions.

5.2 Future Work

As a result of this work, numerous insights were gained into the design of SI8. Firstly, scaling should be done independent of the current copier. Design alternatives for RC^3 need to be explored since the current source was found to be unduly complex. Speed may have to be sacrificed in order to reduce clock injection. The reset of the whole modulator should be done properly. Not only should the resonators be reset, even the comparator and also the DACs need to be put in a proper reset during start-up or at overload. Lastly, a differential version of the modulator should be attempted.

Bibiliography

[1] J. C. Candy and G. C. Temes, "Oversampling methods for A/D and D/A conversion," in *Oversampling Delta-Sigma Data Converters*, J. C. Candy and G. C. Temes, Eds. New York: IEEE Press, 1991.

[2] Frank W. Singor and Martin Snelgrove,"10.7 MHz Bandpass Delta-Sigma A/D Modulators," IEEE Proc. CICC'94, May 1994.

[3] S. Pattamatta, P. .Manapragada, V. Dalal, R. Schreier,"A Switched-Current Bandpass Delta-Sigma Modulator, *Proceedings of the 1994 IEEE International Symposium on Circuits and Systems*, May 1994.

[4] J. B. Hughes and K. W. Moulding, "Switched-Current Signal Processing For Video Frequencies And Beyond," *IEEE Journal of Solid-State Circuits*, vol. SC-28, no. 3, pp. 314-322, March 1993

[5] Vineet Dalal, "A Switched-Current Bandpass Delta-Sigma Modulator," *Master's Thesis, Oregon State University*

[6] R. Schreier and W. M. Snelgrove, "Bandpass sigma-delta modulation," *Electronics Letters*, vol. 25, no. 23, pp. 1560-1561, 9th Nov. 1989.

[7] K. C. H. Chao, S. Nadeem, W. L. Lee, and C. G. Sodini, "A higher order topology for interpolative modulators for oversampling A/D conversion," *IEEE Transactions on Circuits and Systems*, vol. 37, pp. 309-318, March 1990.

[8] R. Schreier, "An empirical study of high-order single-bit delta-sigma modulators," *IEEE Transactions on Circuits and Systems II*, vol. 40, no. 8, pp. 461-466, August 1993.

[9] R. Schreier, "Oversampled A/D Conversion," *ECE 619: Oversampling Delta-Sigma Data Converters*, Department of Electrical and Computer Engineering, Oregon State University, Fall Term 1993.

[10] S. Jantzi, R. Schreier and M. Snelgrove, "The Design Of Bandpass Delta-Sigma ADCs," *Delta Sigma Data Converters, Norsworthy, Schreier and Temes, Eds., IEEE Press, Piscataway, NJ,* ch. 9.

[11] J. B. Hughes, N. C. Bird and I. C. Macbeth, "Switched Currents -A New Technique For Analogue Sampled-Data Signal Processing," *Proceedings of the 1989 IEEE International Symposium on Circuits and Systems*, pp. 1584-1587, May 1989.

[12] C. Toumazou, J. B. Hughes and D. M. Pattullo, "A Regulated Cascode Switched-Current Memory Cell," *Electronics Letters,* vol. 26, no. 5, pp. 303-305, March 1990.

[13] R. Schreier, G. C. Temes, A. G. Yesilyurt, Z. X. Zhang, Z. Czarnul and A. Hairapetian, "Multibit bandpass delta-sigma modulators using *N*-path structures," *Proceedings, IEEE International Symposium on Circuits and Systems*, pp. 593-596, May 10-13 1992.

[14] G. Palmisano and F. Montecchi, "Simplified pseudo-*N*-path cells for z to -z^N transformed SC active filters," *IEEE Transactions on Circuits and Systems*, Vol. 35, No. 4, pp. 409-415, April 1988.

[15] E. Säckinger and W. Guggenbühl, "A High-Swing, High-Impedance MOS Cascode Circuit," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 1, pp. 289-298, Feb. 1993.

[16] B. Brandt, D. Wingard, and B. Wooley, "Second-order sigma-delta modulation for digital-audio signal acquisition," *IEEE Journal of Solid State Circuits*, vol. 26, pp. 618-627, April 1991.

[17] P. Wrighton, G. Taylor, I. Bell and C. Toumazou, "Test for Switched-Current Circuits," *Switched-Currents an analogue technique for digital technology,* C. Toumazou, J.B. Hughes and N.C. Battersby, Eds. IEE, 1993.

APPENDIX

MAKEFILE:

```
rc:     rc.set rc.rout
        @min rc.rout > rc.temp
        @max rc.rin >> rc.temp
        @awk 'NR==1{rout=$$1} NR==2{rin=$$1}END{print rout/rin , rout
,rin}' rc.temp >rc
        @rm rc.temp
        @max rc.set >> rc
        @cat Vminmax >>rc
        @cat rc
        @awk 'NR==2{W1=$$2} NR==2{L1=$$3}NR==3{W2=$$2}NR==3{L2=$$3}N-
R==4{W3=$$2}NR==4{L3=$$3}NR==5{I1=$$2}NR==6{I2=$$2} END{print W1,L1,"
", W2,L2,"  ", W3,L3,"   ",I1,I2}' rc.inc >>rc.all
       @awk 'NR==1{z=$$1} NR==1{ro=$$2} NR==1{ri=$$3} NR==2{ts=$$1}END{-
print "Rout/Rin =" ,z," Rout =" ,ro, " Rin =", ri," Ts =",ts,"\n"}' rc
>>rc.all

rc.set: rc.inc set.sp rc.rin opt.inc
        hspice set.sp > set.lis
        @awk 'NR==4{if ($$1>$$2) print $$1*1e9; else print $$2*1e9}'
set.mt0 > rc.set
        @awk 'NR==4{if ($$1>$$2) print $$1*1e9; else print $$2*1e9}'
set.mt1 >> rc.set
        @rm -f set.*[012]

rc.rout: rc.inc rout.sp rc.rin opt.inc
        hspice rout.sp > rout.lis
        @awk '/output resistance/{print $$6}' rout.lis | tee rc.rout
        @rm -f rout.pa* rout.st*

rc.rin: rc.inc rin.sp opt.inc
        hspice rin.sp > rin.lis
        @awk '/input resistance/{print $$6}' rin.lis | tee  rc.rin
        @GetVminmax
        @rm -f rin.pa[01]

clean:
        @rm -f *.bak  *.st* *.tr*  *.gr* set.cfg
```

RC.INC:

```
*Subckt for rcth :Uses ideal currents
.param  W1=65u L1=4u
+       W2=40u L2=2u
+       W3=325u L3=1.2u
+       I1=1.2m
+       I2=100u

.subckt rc g1 d3
m1 g2 g1 0 0 N w=W1 l=L1
m2 g3 g2 0 0 N w=W2 l=L2
m3 d3 g3 g2 0 N w=W3 l=L3

Ib1 0 d3 I1
```

```
Ib2 0 g3 I2
.ends
```

RIN.SP:

```
*To measure Rin
.include opt.inc

xrc g1 io rc
r1 io g1 1k

Iin 0 io 1ma

.tf V(g1) Iin
.alter
Iin 0 io -1ma
.end
```

ROUT.SP:

```
*To measure Rout
.include 'Vminmax'
.include opt.inc
.param IIN=1mA VOUT=Vmin

Xrc1 g1 io   rc
Xrc2 g1 io2 rc
R2   g1 io2 1M
Iin 0 io2 IIN
Vout io 0 VOUT

.tf  I(vout) Vout

.alter
.param VOUT=Vmax
.alter
.param IIN=-1mA VOUT=Vmin
.alter
.param VOUT=Vmax
.end
```

SET.SP:

```
*To measure settling time
.include 'opt.inc'
.include 'Vminmax'

xrc1 g1 io rc
r1 g1 io 500

Iin 0 io pwl(0 -1ma 1n 1ma )

d1 1 io diode
d2 io 4 diode

v1 1 0 1v
```

```
v2 4 0 4v

.MODEL diode D LEVEL=1
.measure tran 'ts1' trig I(Iin) VAL=0ma cross=1 targ v(g1) VAL= 'Vf + Vs'
fall=LAST
.measure tran 'ts2' trig I(Iin) VAL=0ma cross=1 targ v(g1) VAL= 'Vf - Vs'
rise=LAST
.tran 0.1n 100n
.param Vf=Vg1max Vs=1mv
.alter
Iin 0 io pwl(0 1ma 1n -1ma )
.param Vf=Vg1min
.end
```

GetVminmax:

```
awk 'BEGIN{first=1} /0:g1/{if(first) {line =".param Vg1max=" $3 " Vmax="
$3+0.2; first=0} else line = line " Vg1min="  $3 " Vmin=" $3-.2} END
{print line}' rin.lis > Vminmax
```