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Title: Semi-digital PLL Architecture for Ultra Low Bandwidth Applications

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Phase Locked Loops (PLLs) are an integral part of almost every electronic system. Systems involving low frequency clocks often require PLLs with low bandwidth. The area occupied by the large loop filter capacitor and resistor in a low bandwidth PLL design makes the realization of traditional charge-pump PLL architecture impractical on a single die, mandating external components on the board. In order to maintain low loop bandwidth the designer is often forced to choose very low values of charge pump current which can lead to reliability issues.

In this work, a semi-digital architecture for very low bandwidth monolithic PLLs is proposed. This architecture eliminates large components in traditional charge-pump PLL, thus allowing the realization of on-chip low bandwidth PLLs. A 2x2mm PLL is realized in 180nm CMOS with 75mHz bandwidth consuming 400µW power from 1.8V supply. The prototype PLL locks to an input clock of 1Hz and generates 20kHz output clock with a measured peak-to-peak jitter of 100ns.
Semi-digital PLL Architecture for Ultra Low Bandwidth Applications

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Edmond George, Author
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Chapter 1: Introduction

1.1 Area of focus

Phase Locked Loops (PLLs) are used in a wide range of applications such as frequency synthesis, clock and data recovery, frequency translation, modulation and demodulation. Bandwidth of the PLL used in a system is selected to minimize the phase noise at the output of the PLL while maintaining stability of the system. High loop bandwidth is preferred when the reference clock input has relatively low noise contribution at the output compared to other noise sources in the system. Clocks traveling through backplanes, clocks generated by low performance PLLs, or clocks recovered from Serializer/Deserializer (SERDES) or Field-Programmable Gate Arrays (FPGAs) are typically noisy and require low bandwidth PLL to filter out the excessive noise on them [1].

In addition to jitter cleaning applications, low bandwidth PLLs are also used in synchronizing local clocks to a low frequency input signal. GPS receivers typically provide one pulse per second (1PPS) timing pulse, the rising edge of which is aligned to the Coordinated Universal Time (UTC) second rollover and can be used to discipline local clocks to maintain synchronization between locations separated by hundreds of kilometers [2]. The K2K long-baseline neutrino oscillations experiment used 1PPS signal from GPS to maintain synchronization between 50MHz clocks at near and far detector sites separated by 250km [3]. Implementation of such synchronization circuits require Printed Circuit Boards (PCBs) with multiple components [4] or DPLLs implemented in FPGAs [5]. Figure 1.1 shows a simplified block diagram of a system using 1PPS signal...
from GPS receiver to synchronize the local clock using microcontroller and software to perform calibration for variation due to aging, temperature variation and other environmental factors. In addition to having external components for filtering, the circuits using Direct Digital Synthesizer (DDS) can have spurious components due to truncation errors in the Numerically Controlled Oscillator (NCO) and aliasing from higher order harmonics [6].

![Figure 1.1: GPS disciplining of local clocks by 1PPS signal](image)

In today’s world everything goes to portable solution necessitating as much integration on chip as possible. Applications involving low frequency clocks similar to 1PPS pulse need PLLs with very low bandwidth to maintain stability. Low bandwidth PLL design is difficult on single chip due to large chip area required by loop filter capacitor and resistor. Charge-pump current used may also be low to maintain low bandwidth. This can lead to circuit reliability problems. In this work a semi-digital PLL with 75mHz bandwidth consuming 400μW power from 1.8V supply was realized in 180nm CMOS process on a chip of 2x2mm size. The prototype PLL can lock to a reference clock of 1Hz generating an output of 20kHz. The semi-digital architecture eliminates the need of bulky external components such as capacitors and resistors.
1.2 Primary contributions

This thesis examines the design of monolithic semi-digital PLL with bandwidth as low as 75mHz. The proposed PLL extends the semi-digital PLL architecture [7] to very low bandwidths thus avoiding the need for large external components on PCBs. Semi-digital cells are used in the integral path to replace the large loop filter capacitor in traditional charge-pump PLL. The loop filter resistor in the proportional path is replaced with active damping further reducing the die area. The PLL is compensated for variations in process, voltage and temperature(PVT) by adjusting reference currents based on the current consumed by VCO. The PLL also uses a Frequency Locked Loop(FLL) on power up to speed up the locking process by increasing the reference current thereby increasing the integral path charging current until the VCO reaches close to the target frequency. Peaking in the PLL frequency response is reduced by sampling down the integral path charging current using a low duty cycle clock to reduce the average value of integral current.

1.3 Thesis organization

This thesis is divided into 6 chapters. Chapter 2 gives background on PLLs and discusses the challenges in designing on-chip low bandwidth PLLs. Chapter 3 introduces the semi-digital PLL architecture and presents the methods to reduce the area of loop filter components. Z-domain model for the complete PLL is derived with the new proportional and integral path circuits, and various circuit parameters for the PLL are chosen with the aid of MATLAB. In chapter 4, the circuit design of blocks within the PLL is discussed along with the layout and post-layout transient simulation. Chapter
5 presents the silicon measurement results of the proposed PLL with a 1Hz input clock and analyzes the results. The thesis is concluded in chapter 6 along with a discussion on future work.
Chapter 2: Background on Phase Locked Loops

2.1 Introduction to PLL

A PLL is a feedback system consisting of a Voltage Controlled Oscillator (VCO) and a Phase Detector (PD) connected such that the VCO output maintains a constant phase angle relative to the reference clock input to the PD. The negative feedback acts to reduce the error signal $e(s)$ at the output of PD by changing phase angle of the VCO output. PLLs find numerous applications including demodulation and modulation, signal conditioning, frequency synthesis, clock and data recovery and frequency translation [8].

![PLL block diagram](image)

Figure 2.1: PLL block diagram

Figure 2.1 shows the basic block diagram of a system for using a PLL to generate higher frequencies from the input clock. The VCO oscillates at an angular frequency of $\omega_{out}$. The VCO output signal with a phase angle $\phi_{out}$ is feedback to the PD input after dividing the frequency (phase) by a factor $N$. The other input of the PD is driven by the
reference input clock with a phase angle of $\phi_R$. The PD operates as an error detector and compares the phase difference between the signals at its inputs. When the phase angles of both inputs to the PD are equal, the error detector output remains constant and the PLL locks with $F_{out} = N.F_R$. If $F_{out} \neq N.F_R$, the error detector outputs source or sink current pulses to the low-pass loop filter proportional to the phase difference between the reference and feedback signals. The loop filter smooths the current pulses and generates a voltage which changes the VCO frequency such that the PLL moves towards lock condition. The VCO frequency thus increases or decreases as necessary, by $K_{VCO}.\Delta V_c$, where $K_{VCO}$ is the VCO sensitivity in Hz/Volt and $\Delta V_c$ is the change in VCO control voltage provided by the loop filter. The feedback action continues until the loop reaches steady state with $E(s) = 0$.

2.2 Overview of charge-pump PLL

The most commonly used charge-pump PLL is a Proportional Integral (PI) controller similar to Figure 2.2. The proportional control provides a signal proportional to the current value of error and the output change occurs with the error without any delays.

![Figure 2.2: PI controller block diagram](image)
Proportional control can be represented by equation 2.1, where \( P(t) \) is the proportional control, \( K_P \) is the proportional gain and \( e(t) \) is the error at time \( t \).

\[
P(t) = K_P e(t) \quad (2.1)
\]

Proportional only controllers suffer from steady state offset due to their one-to-one relation between the error and the output [9].

The integral action responds to the error based on the integral of error, thus considering its magnitude and duration as represented by equation 2.2, where \( I(t) \) is the integral control at time \( t \) and \( K_I \) is the integral gain.

\[
I(t) = K_I \int_0^t e(\tau) d\tau \quad (2.2)
\]

The integral action continues until the error is zero and can achieve any output values thus eliminating the offset present in proportional only control. The combined effect of proportional and integral control can be represented as in equation 2.3.

\[
m(t) = K_P e(t) + K_I \int_0^t e(\tau) d\tau \quad (2.3)
\]

Equation 2.3 can be represented in s-domain as shown in equation 2.4.

\[
\frac{M(s)}{E(s)} = K_P + \frac{K_I}{s} = \frac{sK_P + K_I}{s} \quad (2.4)
\]

As shown by equation 2.4, addition of integral control introduces a pole at origin and a zero at \( \frac{K_I}{K_P} \) in the s-plane. Adding the integral control thus improves the steady state performance at the cost of system’s relative stability.
The typical implementation of a charge-pump PLL (CPLL) consists of a Phase Frequency Detector (PFD), a Charge-pump (CP), a passive Loop Filter (LF) and a VCO as shown in Figure 2.3. To generate an output signal with a frequency multiplication, a frequency divider can be employed in the feedback path.

![Figure 2.3: Type 2 charge-pump PLL](image)

Commonly used PFD operates at the rising edges of its input clocks and generates a pair of digital pulses corresponding to the phase error between the reference clock and the VCO output clock. The CP then converts the digital pulses into an analog current that is lowpass filtered to generate a DC control voltage via the passive loop filter network. Resistor R in the loop filter provides the proportional control as the voltage drop across it, \( R.I_{cp} \) is proportional to the phase error. Capacitor \( C_1 \) integrates the error information...
and thus provides the integral control for the loop. The sum of voltages across the series components $R$ and $C_1$ is filtered by the ripple bypass capacitor $C_2$ and provides the control voltage to drive the VCO towards a steady state condition with zero phase error. Like any other feedback system, a CPLL has to be designed with a proper consideration for stability [10].

The charge-pump PLL in Figure 2.3 can be represented by a linearized s-domain model as shown in Figure 2.4 using phase as the variable. The analysis and design of PLL can then be carried out by choosing the values of $I_{cp}$, $R$, $C_1$, $C_2$, $K_{VCO}$ and $N$ to ensure stability of the system considering various trade-offs.

Figure 2.4: S-domain model of type 2 charge-pump PLL

From the s-domain model, the loop gain can be written as shown in equation 2.5 below.

$$LG(s) = \frac{K_{VCO}I_{cp}}{2\pi N} \cdot \frac{s + \frac{1}{RC_1}}{s^2RC_1C_2 + s(C_1 + C_2)}$$

The loop gain has a zero at $\omega_z = -\frac{1}{RC_1}$, two poles at $\omega_{p1,p2} = 0$ and a third pole at $\omega_{p3} = -\frac{(C_1 + C_2)}{RC_1C_2}$. As the PFD operates on the positive edge of the clock input, the feedback information is updated only once every reference clock cycle. The delay in feedback loop due to this sampling operation degrades the phase margin by introducing
a pole. To avoid the stability degradation due to sampling, the PLL bandwidth needs to be chosen much less than the update rate. The component values can be chosen to place the third pole and zero locations such that the loop has sufficient phase margin.

Equation 2.6 shows the closed loop transfer function of a charge-pump PLL. For values of \( LG(s) \gg 1 \), \( \Phi_{out} = N \Phi_R \), multiplying the input phase by the feedback divider \( N \).

\[
\frac{\Phi_{out}}{\Phi_R} = \frac{N \cdot LG(s)}{1 + LG(s)}
\]  \hspace{1cm} (2.6)

2.3 Low bandwidth charge-pump PLL design challenges

The loop gain equation 2.5 of type 2 charge-pump PLL can be used to calculate the component values required to design a low bandwidth PLL using conventional charge-pump architecture. As an example, a PLL with 1Hz clock input and 20kHz clock output is considered. To design a stable PLL operating at this low frequency, theoretical upper limit for the PLL bandwidth is 100mHz [11].

To design a stable loop with low bandwidth, the loop gain will have to be restricted to low values. From the loop gain equation 2.5, it can be seen that the loop gain at low frequencies depend on the VCO sensitivity\( (K_{VCO}) \), charge-pump current\( (I_{cp}) \) and \( C_2 \). To keep the loop bandwidth low, both \( K_{VCO} \) and \( I_{cp} \) need to be selected as low values. The value of \( C_2 \) needs to be maximized to decrease the loop gain, but this will result in an increase in the area.

Reducing the charge-pump current to a very low value can pose reliability concerns as the leakage and noise currents could cause malfunctioning of the circuit. In addition, at low current values the transistors begin to operate in subthreshold region with normal \( W/L \) ratios. Due to this reason the nominal value of charge-pump current was fixed at
a value of 1nA. Even though a very low value of VCO gain is desirable to provide a low loop gain, with a supply voltage of 1.8V this can result in a significant reduction in VCO frequency tuning range limiting the operation in Process, Voltage and Temperature (PVT) corners. As a compromise between the loop gain and functioning at PVT corners, the nominal value of VCO gain was selected as 1200Hz/V.

<table>
<thead>
<tr>
<th>Example</th>
<th>R</th>
<th>C1</th>
<th>C2</th>
<th>Icp</th>
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<tr>
<td>1</td>
<td>100kΩ</td>
<td>59µF</td>
<td>4.6µF</td>
<td>5.6nA</td>
</tr>
<tr>
<td>2</td>
<td>1MΩ</td>
<td>5.9µF</td>
<td>460nF</td>
<td>0.56nA</td>
</tr>
<tr>
<td>3</td>
<td>1GΩ</td>
<td>5.9nF</td>
<td>0.46nF</td>
<td>0.56pA</td>
</tr>
</tbody>
</table>

Table 2.1: Calculation of CPLL parameters

With the above constraints, the remaining parameters R, C1 and C2 required to design a PLL with a loop bandwidth of 100mHz and a loop gain phase margin of 60° can be calculated. The values of resistor and capacitors turn out to be too large to practically implement the circuit on a chip without using any external components. Resistor value can be as large as hundreds of MΩ and capacitors values can be hundreds of nF or even a few µF. The large area consumed by these passive components makes it impractical to implement such a PLL as a stand alone circuit block.

Table 2.1 shows the charge-pump PLL parameter calculation for various trade offs. Low bandwidth PLLs require large capacitors, resistors and/or extremely low current levels making it difficult to realize them on-chip. In chapter 3, we discuss the semi-digital PLL architecture to realize on-chip PLLs with such low bandwidths.
Chapter 3: Semi-digital PLL architecture

3.1 Overview of semi-digital PLL

Semi-digital PLL is proposed as an alternative to conventional charge-pump PLL to realize single chip solutions for very low bandwidth applications. The proposed semi-digital PLL architecture addresses the large proportional damping resistor and loop...
filter capacitor required by the conventional charge-pump PLL architecture for a low bandwidth design. The need for damping resistor \( R \) in the proportional path is avoided by introducing active damping technique using transistors [7]. The large integral path capacitor is replaced with semi-digital cells [12]. The proposed PLL is compensated for PVT variations and hence provides a relatively constant bandwidth across operating conditions.

3.2 Proportional control

Active damping is introduced at the output of charge-pump to avoid the need of loop filter resistor for proportional control. The thermal noise from the loop filter resistor gets amplified by the VCO gain in conventional charge-pump PLL. Eliminating the resistor from the loop filter reduces the area and also decreases the noise contribution at the output. A simplified diagram illustrating the active damping principle is shown in Figure 3.2.

Two resistors of equal value \( R \) connect the charge-pump output node to VDD and GND through switches controlled by DAMP signal. The resistors are implemented by appropriately sized PMOS and NMOS transistors such that when DAMP signal is asserted, the voltage across capacitor \( C \) is actively pulled to \( \frac{V_{DD}}{2} \). When DAMP signal is inactive, the resistive branches are disconnected from VDD and GND nodes and do not affect the output node voltage. The DAMP signal remains inactive during the entire reference period allowing the charge-pump current \( I_{cp} \) to linearly charge or discharge the capacitor \( C \), for a duration equal to the phase difference between the reference and feedback clocks. At the end of every reference clock period DAMP signal is asserted high for a short duration, which restores the voltage across the capacitor to \( \frac{V_{DD}}{2} \).
Waveforms illustrating active damping is shown in Figures 3.3 and 3.4 for a reference clock period of 1s and VDD of 1.8V. UP and DN signals are generated by PFD based on the phase difference between the reference and feedback clocks, allowing the charge-pump current to charge or discharge the capacitor from the steady state value of 0.9V.
For a phase difference of $\Phi_e$, the UP/DN current flows for a time of $\frac{\Phi_e T_R}{2\pi}$, generating a voltage difference of $\pm \frac{\Phi_e T_R I_{cp}}{2\pi}$. Thus the capacitor voltage remains at $\frac{VDD}{2} \pm \frac{\Phi_e T_R I_{cp}}{2\pi}$ for the rest of the reference period, until it is pulled back to the nominal value of $\frac{VDD}{2}$ at the end of reference period. For small values of phase difference $\Phi_e$, the change in voltage at the output node is proportional to $\Phi_e$. Assuming the VCO frequency changes by $K_P$ Hz/V through the proportional control, the proportional gain for the semi-digital
PLL can be written as in equation 3.1.

\[
K_{prop} = \frac{\Phi_{err} T_R I_{cp}}{2\pi C K_P}
\]  

(3.1)

Figure 3.4: Active damping with DN pulse

As the circuit provides a change in the VCO control voltage proportional to the instantaneous phase difference between reference and feedback clocks every cycle, it can
be used for providing the proportional control in the loop without the need of large resistor R as in the case of traditional charge-pump PLL.

3.3 Integral control

The major bottleneck in the implementation of on-chip low bandwidth analog PLL is the area occupied by the loop filter capacitor. Digital PLLs, on the other hand, can be implemented on-chip but their granularity of tuning is limited by the quantization step size. The proposed semi-digital PLL combines the merits of both analog and digital PLL thus providing an on-chip solution with fine granularity as an analog PLL.

Figure 3.5: Integral control circuit for VCO

Integral control for the semi-digital PLL as shown in Figure 3.5 consists of n+1
current sources $I_{d0} - I_{dn}$ of equal value $I_{\text{step}}$, supplying operating current to the VCO. The two current sources $I_{a0}$ and $I_{a1}$ provide fine granular control for VCO frequency. The current sources $I_{d0} - I_{dn}$ can be individually turned ON or OFF through switches $S_{d0} - S_{dn}$ which are controlled by digital bits while the current sources $I_{a0}$ and $I_{a1}$ can be tuned individually to supply a current varying from 0 to $I_{\text{step}}$ by controlling the voltage across switches $S_{a0}$ and $S_{a1}$ respectively. The total current supplied by turning ON all the current sources is designed such that the VCO will be able to oscillate above the target frequency even in weak PVT conditions.

On power up, all digital bits controlling the switches $S_{d0} - S_{dn}$ are initialized to 0, turning OFF all the n+1 current sources. At this point, the VCO draws minimum current and oscillates at its minimum frequency. As the VCO frequency is below the reference frequency, the PFD generates continuous UP pulse charging a capacitor $C_{a0}$ through an auxiliary charge-pump $CP_0$. The voltage across $C_{a0}$ controls the switch $S_{a0}$, thus increasing the current supplied by $I_{a0}$ and hence the VCO frequency. As the current supplied by $I_{a0}$ crosses $I_{\text{step}}/2$, a second capacitor $C_{a1}$ starts charging through a second auxiliary charge-pump $CP_1$, the voltage across which controls the switch $S_{a1}$. Each time $I_{a0}$ or $I_{a1}$ reaches $I_{\text{step}}$, the voltage across the corresponding capacitor is reset to 0 and a digital bit is set high turning ON one additional current source from $I_{d0} - I_{dn}$. The coarse integral control is thus transferred to digital domain, retaining the fine analog control through current sources $I_{a0}$ and $I_{a1}$. The charging of capacitors $C_{a0}$ and $C_{a1}$ are staggered in time so that one of the capacitors will remain in the middle of the tuning region while the other is pulled back to minimum voltage.

If the VCO oscillates above the target frequency, the PFD generates continuous DN pulse, which discharges the capacitors $C_{a0}$ and $C_{a1}$. Similar to the charging operation, once the voltage across the capacitor reaches its minimum value, it is actively pulled to
the maximum value and a digital bit is reset to 0 thus turning OFF a coarse current
source.

In locked state, depending on the PVT corner, the VCO current will be supplied by
‘m’ coarse current sources and the fine current sources $I_{a_0}$ and $I_{a_1}$. The ‘m’ coarse current
sources bias the VCO close to the target frequency and the fine current sources help the
PLL to lock to the right frequency by supplying the required amount of current. A device
in strong PVT conditions thus require less number of coarse current sources(smaller ‘m’)
turned ON compared to a device in weak PVT conditions(larger ‘m’).

The modified integral control for semi-digital PLL can be modeled in z-domain. Assume each current source is designed to change the VCO frequency by $K_S$ Hz and
each of the capacitors $C_{a_0}$ and $C_{a_1}$ takes $T_d$ seconds to charge completely through
their auxiliary charge-pumps. In time domain, a phase difference $\Phi_e$ corresponds to
$\frac{\Phi_e}{2\pi} T_R$ seconds and during this time each capacitor can be charged or discharged $\frac{\Phi_e}{2\pi} \frac{T_R}{T_d}$
number of times. As this number gets added up every cycle, representing the operation
as integration in z-domain, we can write the overall integral control as in equation 3.2.

$$K_I = \frac{\Phi_e}{2\pi} \frac{T_R}{T_d} K_S, \frac{1}{1 - z^{-1}} \quad (3.2)$$

The semi-digital PLL uses $n+1$ current sources controlled by digital bits and two
current sources directly controlled by capacitors to store the integral information as
opposed to the traditional PLL in which the integral current is solely supplied by a
single current source controlled by a large capacitor. This architecture thus results in
a reduction in capacitor size by a factor of $\sim \frac{n+1}{2}$. Thus the savings in capacitor area
increases with $n$. However the current supplied by each current source decreases, thus
pushing the transistors towards sub-threshold region of operation. For reliable operation
of the circuit, \( n \) has to be selected such that the current levels are much higher than the leakage and noise currents.

### 3.4 Z-domain model of semi-digital PLL

The z-domain model for the complete PLL can be derived using proportional and integral control equations 3.1 and 3.2. The update delay of one reference clock cycle in the loop is represented as \( z^{-1} \) in the PFD block. The proportional and integral controls are added inside the VCO block and converted to phase (radians) by dividing with the target frequency. The time domain integration is represented by the integrator block \( \left( \frac{1}{1-z^{-1}} \right) \) in VCO and the divider is modeled as \( \frac{1}{N} \) in the feedback path. Figure 3.6 shows the z-domain model of proposed semi-digital PLL architecture. Using the model, loop gain can be written as in equation 3.3.

\[
LG(z) = z^{-1} \left[ \frac{I_{cp}}{C} K_P + \frac{T_R}{T_d} \frac{1}{1 - z^{-1}} K_S \right] \cdot \frac{1}{1} \cdot \frac{1}{N} \cdot \frac{1}{F_{OUT}}
\]  

\( (3.3) \)
The transfer function for the PLL is shown in equation 3.4.

\[
\frac{\Phi_{\text{out}}}{\Phi_R} = \frac{N \cdot \text{LG}(z)}{1 + \text{LG}(z)}
\]  

(3.4)

Figure 3.7: Transfer function plot of semi-digital PLL

Equations 3.3 and 3.4 can be used to choose the parameter values for the semi-digital PLL. Values for \(F_{\text{ref}}\) and divider are fixed based on the input and output clock frequencies. A low value of \(I_{\text{cp}}\) has to be chosen to support low bandwidth, but still operating reliably in presence of leakage and noise. From previous experience on the technology, a low value of 1nA was chosen for \(I_{\text{cp}}\). The number of digital cells is chosen as 480 to reduce the capacitor size by a factor of approximately 240. In addition to this, the gain from integral control(10Hz/Cell) is selected much lower than the gain from proportional control(1200Hz/V). This reduces the capacitor size by another factor of
Figure 3.8: Step response plot of semi-digital PLL

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Units</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$F_{\text{ref}}$</td>
<td>Hz</td>
<td>1</td>
</tr>
<tr>
<td>Divider</td>
<td>-</td>
<td>20000</td>
</tr>
<tr>
<td>$K_P$</td>
<td>Hz/V</td>
<td>1200</td>
</tr>
<tr>
<td>$K_S$</td>
<td>Hz/cell</td>
<td>10</td>
</tr>
<tr>
<td>$T_d$</td>
<td>ms</td>
<td>2000</td>
</tr>
<tr>
<td>$C_{a_{0,1}}$</td>
<td>pF</td>
<td>500</td>
</tr>
<tr>
<td>$C$</td>
<td>pF</td>
<td>600</td>
</tr>
<tr>
<td>$I_{cp}$</td>
<td>nA</td>
<td>1</td>
</tr>
<tr>
<td>Storage cells</td>
<td>-</td>
<td>480</td>
</tr>
</tbody>
</table>

Table 3.1: Low bandwidth PLL parameters

approximately 120 compared to using the same gains for proportional and integral path.

The capacitor sizes are then chosen with a constraint of 2x2mm area for the whole PLL.
The values of $K_P$, $K_S$ and $T_d$ are selected to achieve a bandwidth close to 75mHz with reduced peaking.

The values chosen for a PLL for 75mHz bandwidth is shown in table 3.1. The transfer function of the proposed PLL plotted using the values in table 3.1 is shown in Figure 3.7. With these selection of parameters, the 3dB bandwidth of the PLL is 73.75mHz at nominal PVT conditions. As marked in the transfer function plot, the peaking of the frequency response is also below 0.1dB resulting in a time domain response as shown in Figure 3.8 without oscillations.
Chapter 4: Circuit design of low bandwidth semi-digital PLL

4.1 Loop components

In this section, we discuss the transistor level implementation of various loop components of the semi-digital PLL including PFD, charge-pump, VCO, semi-digital cells and divider. The parameters values derived in chapter 3 are used to achieve a nominal bandwidth of 75mHz.

4.1.1 Phase Frequency Detector

PFD is used as the error detector in the PLL loop. The PFD circuit consisting of two positive edge triggered D flip-flops as shown in Figure 4.1 is used in the proposed PLL. This circuit generates the outputs UP and DN, the widths of which depend on the time difference between the positive edge transitions on the reference clock $T_{REF}$ and the feedback clock $T_{DIV}$. With $T_{REF}$ leading $T_{DIV}$ in phase, we get an UP pulse of wider duration than the DN pulse. On the other hand if $T_{DIV}$ leads $T_{REF}$, the PFD provides a DN pulse which is wider than the UP pulse. When $T_{REF}$ and $T_{DIV}$ are phase aligned, the UP and DN pulses will have equal width.

A positive edge transition on the clock signal $T_{REF}$ sets the Q output of the D flip-flop FF1, producing a logic high level on UP signal. Similarly, a positive edge transition the clock signal $T_{DIV}$ sets the Q output of D flip-flop FF2. This produces a logic high level on the DN signal. When outputs of both the flip-flops are logic high, the output
of the NAND gate resets both the flip-flops. UP and DN pulses control the switches in the charge-pump which turn on the current source and current sink respectively, to generate the control voltage for VCO. A wider UP pulse turns on the current source for longer duration thereby increasing the control voltage. This provides more bias current to the VCO thereby increasing the frequency of $T_{DIV}$. A wider DN pulse sinks current for a longer duration thereby decreasing the control voltage and hence the oscillation frequency. In locked state, the rising edges on $T_{REF}$ and $T_{DIV}$ occur at the same instant and UP and DN pulses of equal duration are generated. The width of the pulses in this state is equal to the delay of NAND gate and the R to Q delay of the flip-flops.

4.1.2 Charge-pump

The charge-pump generates charging and discharging current pulses based on the UP and DN signals provided by the PFD, thereby producing a control voltage dependent
on the phase difference between reference and VCO clocks. The circuit shown in figure 4.2 is used as the charge-pump with an integrated active damping circuit replacing the loop filter resistor. In addition, this charge pump also implements self compensation for PVT variations.

The PMOS transistor P8 is biased to a fixed voltage to generate a reference current on N5 which is mirrored to the differential pair branches through N6 and N7. An active high UP signal turns on N1 and turns off N2. The current through N6 is thus mirrored to P4 through P1, which flows to the output if the DN signal is logic low. An active high DN pulse turns off N3 and turns on N4. In this state, all of the N7 current is driven out of N4. If the UP signal is low, P4 will supply no current and all of the current through N4 will discharge the output capacitor. If the UP signal is high, the current mirrored to P4 from the first differential pair supplies the N4 current and no current flows to the output.

Figure 4.2: Charge-pump
The transistor P7 added to the reference branch provides PVT compensation for the charge-pump reference current. This branch provides a compensating current to the reference branch by adding a small current proportional to the VCO operating current. At weak PVT corners the VCO consumes more current to operate at the target frequency compared to strong PVT corners. Thus the current added by the compensation branch is more in weak PVT corners than in strong corners and provides a compensated reference current for the charge-pump.

The active damping circuit added at the output of the charge-pump circuit helps to avoid the large loop filter resistor. In normal operation of the charge-pump, DAMP signal is low turning OFF transistors N8 and P5 and the active damping circuit does not affect the charge-pump operation. This allows the node voltage at ICH to be controlled by the charging and discharging currents of the charge-pump. At the end of every update cycle, the DAMP signal is made high for a short duration, turning ON the transistors N8 and P5. This pulls the node voltage at ICH to a fixed voltage through the diode tied transistors P6 and N9. Aspect ratios of P6 and N9 are chosen such that when the DAMP signal is asserted, the voltage generated at ICH node is \( \frac{V_{DD}}{2} \).

As the PLL bandwidth is proportional to the charge-pump current \( I_{cp} \), a very low value of \( I_{cp} \) is required to achieve a bandwidth of 100mHz. In this design a charge-pump current of 1nA was selected. At this low current levels, special care has to be taken to ensure that the circuit is tolerant to leakage currents of OFF transistors. With a reference clock period of 1s, even a small leakage current can change the VCO control voltage by a considerable amount. This causes the VCO frequency to drift away from the lock point during the update period and results in a failure to lock. To address this issue all switches are implemented with high \( V_t \) transistors. Transistors N1 - N4, N8 and P5 are thus selected from 3.3V transistor library such that their leakage current are
negligible($< 10^{-24}$A) and do not affect the normal operation.

4.1.3 Semi-digital cells

Semi-digital cells provide integral control for the VCO and helps to reduce the size of the loop filter capacitor required for very low bandwidths. The circuit level implementation of a semi-digital cell used is shown in Figure 4.3. The cell can be connected or disconnected to the loop filter capacitor at node CC through the pass transistor switches. During power on reset, INIT signal is pulsed high to discharge the output node to GND potential by turning ON transistor N6. Each cell can operate in two modes; analog tuning mode and digital mode.

![Figure 4.3: Semi-digital cell used for integral control](image)

In analog mode, the capacitor is connected to the storage cell output by turning ON
both the pass transistor switches. In this state, transistors N2 and P1 remain in OFF state while transistors N1 and P2 are ON. Transistors P3 and N3 operate as charge-pump by mirroring a reference current to charge or discharge the loop filter capacitor. The signals FAST and SLOW are generated from the PFD outputs UP and DN similar to the main charge-pump. The voltage across the integrating capacitor controls the current through the transistor N7 which supplies a fraction of VCO operating current. Thus in analog mode, the current supplied by the storage cell to the VCO depends on the phase difference information provided by the PFD.

In digital mode, the semi-digital cell either supplies a fixed amount of current or provides no current to the VCO. If signal $\text{LEFT}_1$ is high the gate of N7 is pulled low, turning OFF the current source and no current is supplied to the VCO. If $\text{LEFT}_1$ and $\text{RIGHT}_1$ are low, the gate of N7 is pulled high and the cell supplies maximum current to the VCO. The semi-digital cells are cascaded in such a way that at a given instant, only two cells remain in analog mode, while all other cells are in digital mode. The cells in the chain appearing before the analog mode cells are completely turned ON and provide maximum current to the VCO. The storage cells appearing after the analog modes cells are completely turned OFF and supply no current to the VCO. The signals $\text{LEFT}_1$ and $\text{LEFT}_2$ of $N^{th}$ storage cell on the chain will be controlled by $N - 1^{st}$ and $N - 2^{nd}$ cells in the chain respectively. Similarly $\text{RIGHT}_1$ and $\text{RIGHT}_2$ signals of $N^{th}$ storage cell will be controlled by the output from $N + 1^{st}$ and $N + 2^{nd}$ cells in the chain respectively.

An additional branch with transistors N8 and N9 are added to each cell to provide PVT compensation for the proportional gain. The number of cells turned ON to oscillate the VCO at a particular frequency depends on the PVT corner of the device. As more and more cells are turned ON, the proportional current supplied to the VCO is also increased by the same factor. This provides more proportional current in weaker devices,
as it takes more cells to oscillate at a particular frequency compared to a strong device, and provides compensation for proportional gain.

4.1.4 VCO

A five-stage ring oscillator based VCO as shown in Figure 4.4 is used in the proposed PLL to generate the output frequency of 20kHz. Transistors P1 - P5 and N1 - N5 constitute the ring oscillator. The frequency of oscillation is controlled by the current supplied at the VSUP node by transistors N7 and N8. In addition, VSUP node is connected to the output of every semi-digital cell which provides integral current to control the frequency.

Figure 4.4: Ring oscillator based VCO

Transistor N8 provides a fixed bias current to the VCO, such that at strong PVT corners the VCO free-running frequency is below the target frequency of 20kHz. Tran-
sistor N7 is driven by the output of the charge-pump, providing proportional control and the semi-digital cells provide the integral current required for the operation of the PLL loop. The ring oscillator output is passed through an inverter and a buffer stage to generate differential outputs CLK_N and CLK_P respectively.

An additional inverter branch consisting of transistors P6 and N6 is added for PVT compensation of the charge-pump reference current. These transistors are sized in the same ratio as transistors in the VCO inverter stages such that the current through this branch changes in proportion to the current drawn by the VCO. The voltage at node COMP is used to generate a compensation current in the charge-pump. For weak devices the VCO draws more current to oscillate at the target frequency, while the current through the compensation branch also increases by the same proportion thus providing more compensation current to the charge-pump. This helps in increasing the charge-pump current for weaker devices thus providing self compensation for PVT variation.

4.1.5 Buffer

The buffer stage shown in figure 4.5 is used to convert the VCO output to full swing signal. A differential amplifier stage consisting of transistors N1, N2, P1 and P2 amplify the VCO output and generates a single ended clock signal. This signal is passed through two inverter stages to produce a full swing clock signal with sharp rising and falling edges before providing the clock signal to the divider and the output port.
4.1.6 Divider

A divider is used in the feedback path to multiply the input clock frequency to generate a higher frequency at the output. To generate a 20kHz clock from 1Hz input, a modulo-20000 asynchronous up counter is implemented using D flip-flops. The counter operates at every positive edge of VCO clock, until it reaches the maximum count and generates a pulse on SYSCLK which if used as the feedback clock to the PFD. The 20kHz clock from the VCO is also divided by 4 to generate a 5kHz output clock.

The divider is also used to generate the DAMP signal required for the active damping of proportional control. The DAMP signal is asserted high for 32 clock cycles before the counter reaches its maximum value. 32 cycles is selected based on the time the DAMP signal needs to pull the control voltage to $\frac{V_{DD}}{2}$. This signal resets the voltage at the main charge-pump output to $\frac{V_{DD}}{2}$ providing the proportional control.

![Figure 4.5: Buffer for VCO output](image-url)
4.2 Frequency Locked Loop (FLL) mode

As the PLL has very low integral path gain, it takes very long time to acquire lock, especially in weak PVT conditions. To speed up the lock acquisition of the PLL, a faster frequency lock mode is implemented in the integral path. On power up, the loop turns on in FLL mode by default. In this mode, the integral path current is boosted up such that the capacitors in integral path are charged at a much higher rate than in the normal PLL operation. As the VCO frequency approaches the target frequency, the FLL mode signal is made low reducing the loop bandwidth to continue locking in PLL mode.

![Bias current for semi-digital cells](image)

The FLL\_MODE signal is generated from the feedback divider count value. Every reference clock edge, the divider is reset to 0 and starts counting VCO clocks until the next reference edge. If the count value at the end of reference cycle is above a certain threshold the circuit exits FLL mode. Thus the digitally controlled current sources in the integral path are turned ON at a much faster rate until the VCO reaches close to
the target frequency thereafter reducing the rate to continue normal PLL operation.

When FLL_MODE signal is high, transistor N1 is OFF and the current through N2 is mirrored to N3 providing additional current for the reference branch for charging the capacitors. As the FLL_MODE signal goes low, the transistor N1 turns ON and pulls the gate of N3 to GND potential and turns OFF the additional current available for charging. In this mode, the charging and discharging currents for the integral path capacitors will be generated by mirroring currents through P2 and N6 inside the semi-digital cells.

4.3 Peaking reduction

Figure 4.7: Sampling down the integral path current
The peaking in frequency response of the loop can be reduced by lowering the integral path gain. This can be achieved by increasing the capacitors on the integral path or reducing the charging current. Increasing the capacitor size significantly increases the die area. As the transistors in the semi-digital cells already operate at very low current levels, this can pose reliability concerns as well. Sampling on the integral path was used to overcome this limitations and achieve lower gain through the integral path.

The output current from the storage cells is passed through switches before connecting to the VCO input. A very high frequency clock signal (1GHz at nominal operating conditions) was generated from a ring oscillator to control the sampling switches. The oscillator was designed such that the duty cycle of the clock is close to 25% thus turning on the switches only 25% of the duration and reducing the charge transferred to the capacitors by a factor of 4. As the signal is sampled by a relatively high frequency clock, on an average the integral path gain is reduced by a factor of 4. As shown in figure 4.7, when the sampling is disabled, the voltage across the capacitor increases at a higher rate than when it is enabled. This helped in reducing the peaking to a level lower than 0.1dB.

4.4 Process compensation

Change in process, voltage and operating temperature can cause large variations in loop parameters designed for nominal values, thus affecting the performance of the PLL. To minimize the effects of PVT variation, compensation is introduced at various places in the PLL.
One of the parameters affecting the loop bandwidth is the charge-pump current and hence a constant charge-pump current is required for constant bandwidth. Variation in charge-pump current is compensated by adding a correction current based on the PVT conditions. The current consumed by the VCO is used as an indication of the PVT condition and a fraction of VCO current is added to the charge-pump current for compensation. In weak corners the charge-pump current has lower values, but more correction current is added to it as the VCO consumes more current in weak conditions to generate the target frequency. The time taken for charging the capacitors in the integral path depends on the reference current used for auxiliary charge-pumps. This current can
vary with PVT similar to the main charge-pump current. The auxiliary charge-pumps are compensated similar to the main charge-pump by adding compensation current from the VCO.

Another parameter affecting the loop dynamics is the proportional gain of the VCO, $K_P$. The value of $K_P$ can vary by more than a factor of 4 across process corners, thus changing the PLL bandwidth. Compensation for $K_P$ is added to provide fairly constant value of proportional gain across PVT conditions. As discussed in chapter 3, the integral path uses semi-digital cells to provide the VCO current. The number of cells turned ON to reach the target frequency is used as PVT indication. For each cell that is turned ON, an additional current source is added to the proportional path, thus increasing the proportional current supplied to the VCO. As the weak devices need more semi-digital cells to be turned ON for locking, more proportional current is added for them thus compensating the proportional gain.

Figure 4.8 shows the transfer function plot for the PLL with PVT compensation. The parameters $I_{cp}$, $K_P$ and $T_d$ are measured across corners and used for plotting the transfer function. As seen in the figure, the bandwidth remains fairly constant across the corners.

4.5 Layout

Layout for the prototype of proposed semi-digital PLL is shown in Figure 4.9. The complete PLL layout was done using an area of 2x2mm. Three metal layers were used for signal routing and fourth metal layer was used for supply. Two IO pads were assigned for each of the power pins AVDD and GND. Three input pads were used to supply the reference clock, power-on-reset and a control signal to enable or disable the sampling
logic on the integral path current. Two dedicated output ports were assigned to observe the 20kHz output from the VCO and a divided clock of 5kHz.

Figure 4.9: Layout of low bandwidth PLL

4.6 Post-layout transient simulation

Transient simulation for the proposed PLL using layout extracted netlist is shown in Figure 4.10. Waveforms for the reference clock REFCLK, feedback clock SYSCLK are shown along with the frequency plot of 20kHz and 5kHz outputs. Due to the low bandwidth, the PLL take many cycles to lock, only first few cycles are shown in figure.
Figure 4.10: Transient simulation of PLL with layout extracted netlist
Chapter 5: Measurement results

The semi-digital PLL designed was fabricated in 180nm CMOS process. A 1Hz input clock was supplied to the CLKIN and the signal at 20kHz output was observed. The PLL takes about 100 reference clock cycles to acquire lock. The output clock period measured for a duration of 1s after the PLL locks is shown in Figure 5.1. The average frequency measured for this duration is 20.008kHz with a minimum and maximum values measured for a duration of 1s after the PLL locks is shown in Figure 5.1. The average frequency measured for this duration is 20.008kHz with a minimum and maximum values
of 19.992kHz and 20.032kHz respectively corresponding to a total peak-to-peak jitter of 99.88ns (0.2% of the period).

Figure 5.2: Measurement noise due to 50Hz supply

The higher frequency jumps seen in the period measurement in Figure 5.1 is caused by the coupling from 50Hz supply. In Figure 5.2, the measurement is zoomed in to show the 50Hz interference from the supply line.

The period measurement in Figure 5.1 also exhibits periodic variations in frequency at the reference rate causing deterministic jitter at the output. This is caused by the coupling of reference clock transitions to the semi-digital cells. As the reference clock is
routed above the semi‐digital cells supplying the integral path current, each transition on the reference clock is coupled to the cells causing variation in the output frequency.
Chapter 6: Conclusion and future work

In this thesis, a semi-digital architecture for very low bandwidth PLL was discussed. The proposed architecture enables the realization of very low bandwidth PLLs on a single chip solution eliminating the need for bulky on-board components. The measurement results for a prototype PLL fabricated in 180nm CMOS was presented. The 75mHz bandwidth PLL consuming 400µW power from a 1.8V supply was able to lock to the input clock at 1Hz and generate 20kHz output without any external components on board. The PLL is able to retain the voltages on proportional and integral control paths for a long update period of 1s without being affected by leakage.

The proposed PLL, unlike DPLLs, do not suffer from quantization error. Due to very low VCO gain the noise amplification from charge-pump is low. The loop filter resistor from the conventional charge-pump architecture is replaced by active damping, thus eliminating the thermal noise from the resistor. The architecture thus provides the benefit of charge-pump PLLs with no external components on the board.

Due to the low bandwidth of the PLL, the lock acquisition time is significant even with the FLL introduced at power-up. In the current scheme, additional constant current sources are turned ON while charging the capacitors on the integral path to speed up the locking process. As the update happens only in 1s even in FLL mode, in weak and strong process corners the PLL can take more time to lock compared to nominal corner. The semi-digital nature of the PLL can be used to turn ON/OFF the current sources using VCO clock thereby reducing the lock time in all PVT conditions.

The prototype PLL also exhibited deterministic jitter due to coupling from reference
clock to the semi-digital cells. The effect of coupling this can be reduced by careful layout of the reference clock, especially across the sensitive blocks including charge-pump and semi-digital cells thus significantly improving the jitter number.
Bibliography


