AN ABSTRACT OF THE THESIS OF

Tian-chen Liu for the degree of Master of Science in Electrical and Computer Engineering presented on April 5, 1988. Title: CMOS Analog Design Using A Digital Gate Array

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The core area of a conventional CMOS digital gate array consists of only one size of NMOS device and one size of PMOS device. Both primitives have fixed minimum channel lengths, and this has significantly impeded analog applications. This work has shown that by forming series and parallel interconnections between device primitives, the composite structure approximates a MOSFET of larger channel length and width. Thus, this simple configuration removes the constraints caused by the fixed channel length and width. Using this technique, designs for all of the basic analog building blocks such as inverters, current mirrors, source followers, and various other amplifiers have shown excellent performance. As an example, using a 3-μm CMOS technology, a folded-cascode amplifier and its associated DC biasing circuitry were designed using the digital gate array.

CMOS Analog Design Using A Digital Gate Array

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Tian-chen Liu

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Associate Professor of Electrical and Computer Engineering
in charge of major

Redacted for Privacy

Head of department of Electrical and Computer Engineering

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Dean of Graduate School

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Typed by Tian-chen Liu for Tian-chen Liu

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I. INTRODUCTION

The driving force behind the development of analog MOS integrated circuits was the need for the integration of both analog and digital functions on the same IC chip to reduce the number of components in a system. Many significant developments impact this need in certain obvious trends such as programmable systems, self-correcting systems, oversampling techniques, continuous-time techniques, and integrated sensors [1]. Among them, the programmable systems are especially important in recent VLSI applications. CMOS gate arrays are inexpensive programmable systems that are extensively used. Accordingly, the needs for the realization of analog circuits on gate arrays have increased.

In a conventional CMOS gate array, only one size of PMOS device and one size of NMOS device are available. Each primitive has a fixed width and a minimum channel length determined by standardized fabrication processes. The size of the primitive is determined only by digital applications, and this has impeded implementation of analog functions.

The earliest effort for incorporating analog circuits into a CMOS gate array was by Kash in 1981 [2]. He solved the fixed width problem using parallel interconnections between device primitives. The major drawback was the fixed minimum channel length that limited both design flexibility and circuit performance. This limitation was evident even in the recent paper of Hagelauer and Ronge [3]. For all their work in realizing resistor and capacitor elements by interconnecting CMOS source/drain regions, their circuits were still subject to the minimum channel length constraint. Because of this problem, many researchers facilitated standard cell analog CMOS building blocks for use in custom and semicustom VLSI designs [4]. This alternative increased fabrication complexity which inevitably raised the cost. Some other resolutions were sought using bipolar gate arrays for mixed analog/digital applications [5]-[6]. Despite their outstanding performance, they inherited the major disadvantages of bipolar technology compared to CMOS technology such as larger power consumption, less circuit density and more expensive fabrication cost. This thesis presents solutions to these problems using series/parallel interconnections of CMOS primitives to approximate a longer equivalent channel device. Designs for different analog building blocks and a folded-cascode amplifier including bias circuitry were simulated using the SPICE

program [7]. The main idea is to design analog circuits by using only their equivalent devices, and then transform these devices into the corresponding CMOS gate array primitives. Only small discrepancies were observed between these two structures for both DC and AC analysis. Encouraged by the promising results, designs were laid out using 3-μm CMOS technology and will be fabricated by MOSIS [1]. Details of the approach and results are presented in later sections of this paper. Using this technique, it appears that most analog circuits can now be realized on conventional low-cost CMOS digital gate arrays.

1. MOSIS is MOS Implementation Service which is an organization that provides university communities with IC fabrication services.

II. REALIZATION OF ANALOG CIRCUITS

2.1 Basic Concepts

For the realization of analog circuits using digital gate arrays, it is necessary to gain some familiarity with gate array structures. The basis of the design concept using gate arrays is to remove the constraint of fixed device size so that most analog circuits can be realized. The following subsections give an approach serving this demand.

2.1.1 Introduction to gate arrays

Gate arrays are really semicustom digital integrated circuits, also called uncommitted logic arrays (ULAs), configurable gate arrays (CGAs), master slices, and logic arrays. The term "semicustom" means that the IC can be made into many different application-specific designs. The structures of the active and the passive elements are fixed, and design is achieved by routing metal interconnections among the potential circuit elements. Unlike many other ICs, gate arrays can be pre-fabricated up to the point where the final metalization is performed. An exemplary CMOS gate array shown in Fig. 1 consists of thousands of cells, with each cell consisting of active device primitives and polisilicon underpasses [8]. Because the cells are closely placed to one other and the

structure is repetitive, the gate arrays are especially suitable for programmable systems in VLSI design. In programmable systems, the system can be arranged either by making certain final connections between primitives or by destroying the already existing connections. Normally, the former one is called mask-programmable, and the latter one field-programmable. Present gate array applications are mainly in replacing many standard digital ICs of a system by an application-specific design. Further overviews of the gate array technology were presented by Wiegand [9], and Posa [10].

2.1.2 Modeling Of composite primitives

A typical cell structure along with its layout in a CMOS digital gate array are shown in Fig. 2 [8]. Note that each primitive structure of the cell is fixed in both channel width and channel length. For analog design needs, this restriction has curbed the realization of most analog circuits. Most high performance CMOS analog circuits have different channel width and channel length for each device. Therefore, in order to realize them on a CMOS gate array, a composite structure for approximating a larger device was developed. Our studies have shown that primitives appropriately connected in series/parallel combinations behave very much like a single device operating in the saturation region. This feature is

somewhat surprising in that the drain row of composite primitives operates in saturation region, while the other row(s) operates in non-saturation. This interesting behavior implies that the drain-to-be row acts like a single MOS transistor of minimum channel length, while the other row(s) behave like a resistor in series with this MOS transistor. An example of this composite structure along with its approximate device are shown in Fig. 3. For a clear interpretation, Fig. 4 shows in (a) a composite-configured inverter, in (b) its equivalent circuit model with series feedback resistor, and in (c) its effective equivalent circuitry. Note that V_{dd} is 5 volts and V_{ss} is -5 volts for <u>all</u> of the circuits in this thesis. The ratio of the effective channel length to the primitive channel length is,

$$(L_{eff} / L) = .5 * [Y + Y^2 - 4 * G^2]; \quad (1)$$

where $Y = [(K + G)^2 - 2 * G]^{\frac{1}{2}}$, (2)

and $G = G_{ds} / G_{load}$, (3)

$K = 1 + (G_m / Gs)$. (4)

Details of the derivation can be found in APPENDICES VIII of this thesis. Note that the equivalent channel length depends on the upper load conductance G_{load}, which is different from place to place in the general analog circuit. This results in design complexity. For a more

complicated circuit, design is almost impossible. Thus, a simple overlapping technique is used instead. This technique is a close approximation for the equivalent device of the composite structure. It does result in some minor discrepancies in the design results, but it is a fairly accurate method of analog design using a CMOS gate array.

2.1.3 Overlapping technique

The most straightforward way to determine an equivalent device for a composite structure is to closely match the DC transfer curves of inverters. The matching approach proceeds by overlapping the zero output point of a composite structure with the one for a single larger device. Since a perfect match is hard to find at first, the overlapping technique is actually performed by interpolating the zero output point in the transfer curves of different single devices. By doing so, the equivalent channel width and channel length can be found. A suggested approach for approximating a composite structure of M primitives in series and N primitives in parallel is as follows:

(1) Since the aspect ratio of each primitive is W/L, for a composite structure of M primitives in parallel and N primitives in series, the ideal equivalent device width should be M times greater than that of the primitive, and

its ideal equivalent device length should be N times greater than that of the primitive. Thus, a first guess for an equivalent devices aspect ratio should be (M*W)/(N*L).

(2) Due to the lateral diffusion in both width and length directions in the gate channel, the effective channel size is reduced. This becomes more prominent as the primitive channel length decreases. Accounting for this effect, the actual aspect ratio of the primitive is $(W-2W_D)/(L-2L_D)$. Thus, a better approximation to the composite device should be $(M*(W-2W_D))/(N*(L-2L_D))$. Fig. 5 shows an equivalent aspect ratio as determined by interpolating the zero output points between these two points so as to overlap the one of a composite. Once the equivalent device size is determined, most analog circuits can be designed using the equivalent device. Consequently, this configuration greatly increases the flexibility of the analog design on a gate array.

2.2 Basic Analog Building Blocks

The basic MOS characteristics have been known for years as presented by Sah [11]. MOS devices are normally designed to operate in the saturation region for analog applications. A major objective of MOS analog design is to design an operational amplifier. A tutorial overview

was done by Gray and Meyer [12]. In order to design a useful operational amplifier, most basic analog building blocks must be understood beforehand. Hence, analog design using a CMOS digital gate array must start from the basic building blocks such as inverters, current sources, source followers, differential-pair amplifiers and cascode amplifiers.

2.2.1 Inverters

A typical NMOS inverter structure as shown in Fig. 6 (a) consists of a load conductance, and an input transistor. For a PMOS one, the elements in the structure are swapped in position. Because the inverter result is the criterion for adapting the overlapping technique, it has already been described in the previous section. Still, a further analysis is necessary.

As an example, if there are two transistors in series instead of just one as in Fig. 6 (b), its transfer curve and the one for a single transistor, shown in Fig. 7, look similar but with a different aspect ratio. Why these two transistors in series behave like an inverter is not easily understood. If they are presumed to be digital inputs, the inverting effect is quite obvious because they are actually an AND logic function with the same input. If the input is high, the output is

low. If the input is low, the output is high. This phenomenon results in an inverter-like DC transfer curve.

A study of the operation of these two series-connected transistors during transition shows an interesting result. Only the upper (drain-side) one actually experiences transition from the cutoff to the saturation to the nonsaturation region, while the lower (source-to-be) one bypasses the saturation region and stays in nonsaturation after leaving the cutoff region. This unusual behavior tells us that the lower one works like a resistor and affects the small-signal transconductance of the upper one by series feedback. This interesting behavior is demonstrated for the circuit of Fig. 6 (b) as shown in Fig. 8.

Note that the actual transfer curve for the series configuration is not exactly the same as for a regular inverter structure. Compared to its equivalent inverter using a single device, the very small discrepancy shown in Fig. 9 exists. The difference results partly from the imperfect matching using the overlapping technique, and partly from different second-order effects in the two configurations. For inverters with more transistors in series, they all behave alike. For PMOS inverters, their second-order effects are much stronger than for the NMOS ones because of the unavoidable body-effect associated

with this p-well CMOS technology. This increases the discrepancy from the ideal behavior.

2.2.2 Current sources

The best way to study a current source is to build current mirror circuits. By evaluating the current mirror effect, key features can be characterized. This section will discuss the composite structure in four widely used current sources-- simple current source, Wilson current source, balanced Wilson current source and cascode current source. All of the following circuitry consists of the original approximated devices, the composite devices and its equivalent devices. For example, the initial approximated device is (40/6) for its size; the composite one consists of primitives of two in series by two in parallel, with (20/3) for each NMOS primitive size, and is expressed as N2*2; the equivalent device determined by the overlapping technique is (40/4.73) for its size.

(A) Simple current source

A typical circuit shown in Fig. 10 (a) is studied for its current transfer characteristics at different voltages across the specific current mirror device. The results of Fig. 10 (b) show that the equivalent current mirror structure almost exactly reproduces the current transfer curve for the composite one. Note that these two structures deviate from the original approximated current

mirror owing to their shorter effective channel length, which strengthens the second-order effect.

(B) Wilson current source

A similar study for a circuit depicted in Fig. 11 (a) reflects an analogous result to the simple current source. The result is given in Fig. 11 (b). A smaller discrepancy for these three current mirror structures is expected because the presence of another device reduces the second-order effect in the mirror branch for each structure.

(C) Balanced Wilson current source

A balanced Wilson current source exhibits better performance than the previous two types. It does not have a DC offset voltage like a Wilson current source nor a strong second-order effect like a simple current source. Examination of the circuit in Fig. 12 (a) reveals the same facts. Its mirror effect, represented in Fig. 12 (b), is further improved.

(D) Cascode current source

The analysis of the circuit shown in Fig. 13 (a) gives a nearly identical result to the balanced Wilson current source (Fig. 13 (b)). Because these two current sources are similarly configured, they improve the mirror effect at the expense of output voltage swing capability and power consumption. Normally they are not used in

designing a medium performance amplifier that is suitable for VLSI needs.

To realize these four current sources using the composite primitives, the number of primitives in series must be the same for both the mirror device and the mirrored one. To ensure an equivalent length at both sides. This is very critical in the design as failure to accommodate this will result in bad matching performance for the current source.

2.2.3 Source followers

The role of source followers in analog design often is to serve for level shifting in designing DC bias circuitry because good bias circuitry will balance the amplifier to secure the optimal performance. Accordingly, it is necessary to analyze how well source followers are designed using the composite primitives. From Fig. 14 (a), circuits using a constant current source, consisting of the approximated device, the composite one, and the equivalent one are tested. Only a minor discrepancy is observed in Fig. 14 (b). If a PMOS source follower is implemented, the discrepancy is increased owing to a stronger second-order body effect. Despite this tolerable deviation, all the results imply that the composite primitives may be designed for DC bias circuitry.

2.2.4 Differential-pair amplifiers

The differential pair, formed by a common-source transistor structure, is widely used in both digital and analog applications. For digital applications, it serves as a current switch to do a logical OR operation. But for an analog implementation, it is normally used as a differential amplifier in the input stage. Its swing capability and frequency response will critically affect the circuit performance. Fig. 15 (a) shows a circuit consisting of the three different types of circuits as discussed before. Their frequency responses in Fig. 15 (b) show a discrepancy occuring only at very high frequencies. Fig. 16 shows that the swing capability of the composite one is worst among the three which is conceptually reasonable. It has non-saturated transistor(s) in series with the saturated one; accordingly, its swing range is reduced. Notwithstanding, its transfer characteristic is closely matched with the other two.

2.2.5 Cascode amplifiers

A cascode structure is normally used to ensure a higher small-signal gain for the amplifier. Typical implementation using the equivalent devices as well as the composite ones are shown in Fig. 17 (a). Note that there are DC voltage bias inputs for each device to secure the

optimal performance of the amplifier. In comparison to the same cascode amplifier formed by composite primitives, the equivalent one has a small difference in the input offset voltage if the same bias is used. Still, if their output are biased near zero, their AC analysis should be approximately the same except at a higher frequency. Fig. 17 (b) demonstrates the frequency response of the circuits in Fig. 17 (a). The increasing discrepancy as the frequency goes higher indicates that the overlapping technique may need a further improvement for modelling the composite structure at high frequency. However, if there are no more than four series connections in the composite structure, this discrepancy will not be significant.

2.3 Folded-cascode Amplifier with Bias Circuitry

To implement an analog design which consists of most of the basic building blocks, a folded-cascode amplifier including its DC bias circuitry shown in Fig. 18 (a), was designed to demonstrate the overall performance of analog design on a digital gate array. The design approach is described in the following subsections.

2.3.1 The folded-cascode amplifier

The folded-cascode amplifier was designed using the equivalent devices to optimize circuit performance. The design was actually done by the conventional approach.

This means that specifications are met by adjusting the reference current, device size, and device saturation voltage in the sense of higher gain, wider operation domain, lower power consumption and less silicon area. After the best performance had been attained, the equivalent devices were all replaced by their composite structures. Then the whole composite circuit was simulated again to check its discrepancy from its equivalent creation. Normally, there is not much deviation between them. However, if any contingent requirement is not fulfilled, the design should be repeated for another trial.

2.3.2 The bias circuitry

For the high-level integration of a gate array, the on-chip structure must include the necessary reference voltages and the bias voltages. Therefore the bias circuitry should be incorporated into the design. So far there is not much deviation for AC analysis among most designs. However, DC bias circuitry encounters a similar problem as the differential pair does. Resulting from the serial connections, the DC reference voltage designed by the equivalent bias circuit is not exactly the same as the one formed by the composite circuit. Normally, the deviation is small. The more serial connections in the composite device, the larger the discrepancy that

resulted. Fortunately, there are no more than four or five primitives in series for a typical design using the 3 μm technology. Still, for a typical gate array using less than 1.25 μm technology, the design of the DC bias circuitry must consider a larger tolerance for the bias voltage.

2.3.3 The performance analysis

The frequency response of the design is shown in Fig. 18 (b). The result indicates a good performance even for the operation in mega-hertz range. This specific design is compared to the performance of a general purpose operational amplifier in Table 2. Apparently, the common mode range is smaller and the silicon area is larger than the versatile custom design. Considering the lower fabrication cost and off-the-shelf capability, the composite semi-custom design is very attractive. And most of all, it can build analog circuits on the digital structure with little additional effort.

III. LAYOUT GUIDELINES

To assure the best design performance, circuits must be properly laid out before fabrication. Since circuit simulations were all done by using the device parameters of the MOSIS 3-um CMOS technology as listed in Table 2, they must be laid out using MOSIS design rules as well. The following sections will introduce the basic concept of design rules and the layout approach for the preceding folded-cascode amplifier circuitry.

3.1 Design Rules

Design rules are a set of regulations which define the acceptable geometrical dimensions and electrical characteristics achievable in a fabrication process. These regulations are essential in defining the worst case design parameters such as transistor aspect ratios, capacitance values, electrical interferences, and so on. In order to realize the conceptually designed circuit, these rules must be faithfully carried out. The circuit will thereby have a high probability of correct operation and independence of processing variations.

In the MOSIS p-well 3-μm CMOS process, most layout guidelines are made just to assure the possible process tolerance such as mask alignment error and etching deformation. The rest of the guidelines are made to secure the immunity for electrical performance. A

simplified summary for MOSIS design rules is shown in Fig. 19, where all geometrical distances are in units of microns.

3.2 Layout Approach

The designed analog circuits must be laid out with a digital gate array structure. That means its internal structure is fixed and repetitive. The only accessible processing steps are contact holes and metal interconnections. Accordingly, the layout environment is fully identical to a typical digital gate array.

The layout for the designed cell library is shown in Fig. 20. Compared to most digital gate array layouts, there is a little difference. Conventionally, power lines are connected into the active region. This is acceptable for digital applications. For analog design, power lines should be separated from the active region as much as they can. Wherever the overlapping occurs, the cross-talk phenomenon may distort the analog signal and introduce noise, inevitably degrading the circuit performance. Therefore, the power lines of V_{dd} and V_{ss} are placed alongside the active region. However, the fixed metal channels which serve distant interconnections inevitably have cross-talk with the polysilicon underpasses. Indeed, they will deteriorate the circuit performance. Because these metal channels are built within a gate array

library, there is no alternative for overcoming this disadvantage. This is one of the tradeoffs for analog design using a digital gate array.

Fig. 21 shows the previous design of a folded-cascode amplifier with biasing circuitry using the designed cell library. Note that the central regions are NMOS in a p-well, while the rest are PMOS. The metal channels are used for ground and the test points for the bias voltage. The polysilicon underpasses are used as jumpers for interconnections of PMOS and NMOS devices. From this layout scheme, 59 transistors are required out of a total of 96 available in the library core. The die area is about 50 percent greater than that required for a custom layout of the same amplifier.

IV. EXPERIMENT RESULTS

Because the designed circuits have not been fabricated, the most straightforward way to demonstrate the core design concept is to check the current-voltage (I-V) characteristics curve for the series connected devices. A CD4007UB CMOS chip contains three identical NMOS and three identical PMOS devices. The backgates are connected to most positive voltage for PMOS and most negative for NMOS, respectively. The results of both PMOS and NMOS as a single device, two-in-series structure, and three-in-series structure are shown in Figs. 22 and 23. From these figures, the qualitative analysis can be made as follows:

(A) The current of each corresponding gate voltage step among different configurations is almost in exact inverse proportion to the number of device in series. Since the current is proportional to the (W/L_{eff}) ratio, this leads to the fact that the equivalent channel length L_{eff} increases with more devices in series.

(B) The slope and the step spacing of the corresponding curves in the saturation region gives the necessary information for the Early voltage and the transconductance (G_m). Since the Early voltage is actually proportional to L_{eff} and G_m is inversely proportional to L_{eff}, a larger

Early voltage and a smaller G_m (i.e. a smaller spacing between steps) for more devices in series are as expected.

(C) Similar to the analysis in the previous part, the slope of the corresponding step in nonsaturation region indicates the drain conductance (G_{ds}). A less steep slope indicates a smaller G_{ds} which also relates to a larger L_{eff}.

(D) These I-V characteristics curves reveal that series-connected devices are suitable for forming basic analog circuits owing to their longer effective channel length and hence less second-order effect.

V. FUTURE ASPECTS

To design high performance analog circuitry on digital CMOS chips, some passive elements such as resistors or capacitors are often required to obtain the best quality. Although this important part of design is not involved here, it had already been presented by Vittoz [13]. His work mainly focused on geometry and noise control of the circuitry in different analog building blocks. Because our work does not include a detailed analysis for noise, this is an important topic for future applications. Vittoz also presented optimal matching rules for designing analog circuits on digital chips. These rules, although not directly related to our overlapping technique, are very useful for further applications in our work.

From the simulation results, the overlapping technique is working quite well for the design. Still, most of the discrepancies appear at high frequencies. This result shows that the overlapping technique may need a minor modification to give a better prediction for the equivalent device at high frequencies.

VI. CONCLUSION

Our work shows an easy way to design analog circuits on a digital gate array. This study increases the versatility of the CMOS technology in mixed analog and digital design. The matching approach using the overlapping technique is the core of the design. An equivalent device using this strategy can be obtained for any composite structure. However, mismatch of an equivalent device and its composite structure represents a limitation to the accuracy of analog circuits. Therefore, precaution must be taken to get an accurate equivalent device.

The degradation of circuit performance caused by the cross-talk of fixed channels and underpasses in the gate-array layout is an inherited disadvantage. This shortcoming may be greatly reduced if a cell library is specifically designed for possible analog blocks. Another inherited disadvantage is a lower output voltage swing capability resulting from the series-connected structure.

The design of analog circuits on a digital CMOS gate array requires much more knowledge about process variations, parasitic effects, and reliability of simulation than does a purely digital one. Indeed, the circuit of composite devices restricted to the fixed structure has a lower performance than the custom

counterpart. However, the advantage of mixing analog and digital functions on the same chip are remarkably attractive. Most of all, it increases the design flexibility without raising the fabrication cost for a digital gate array.

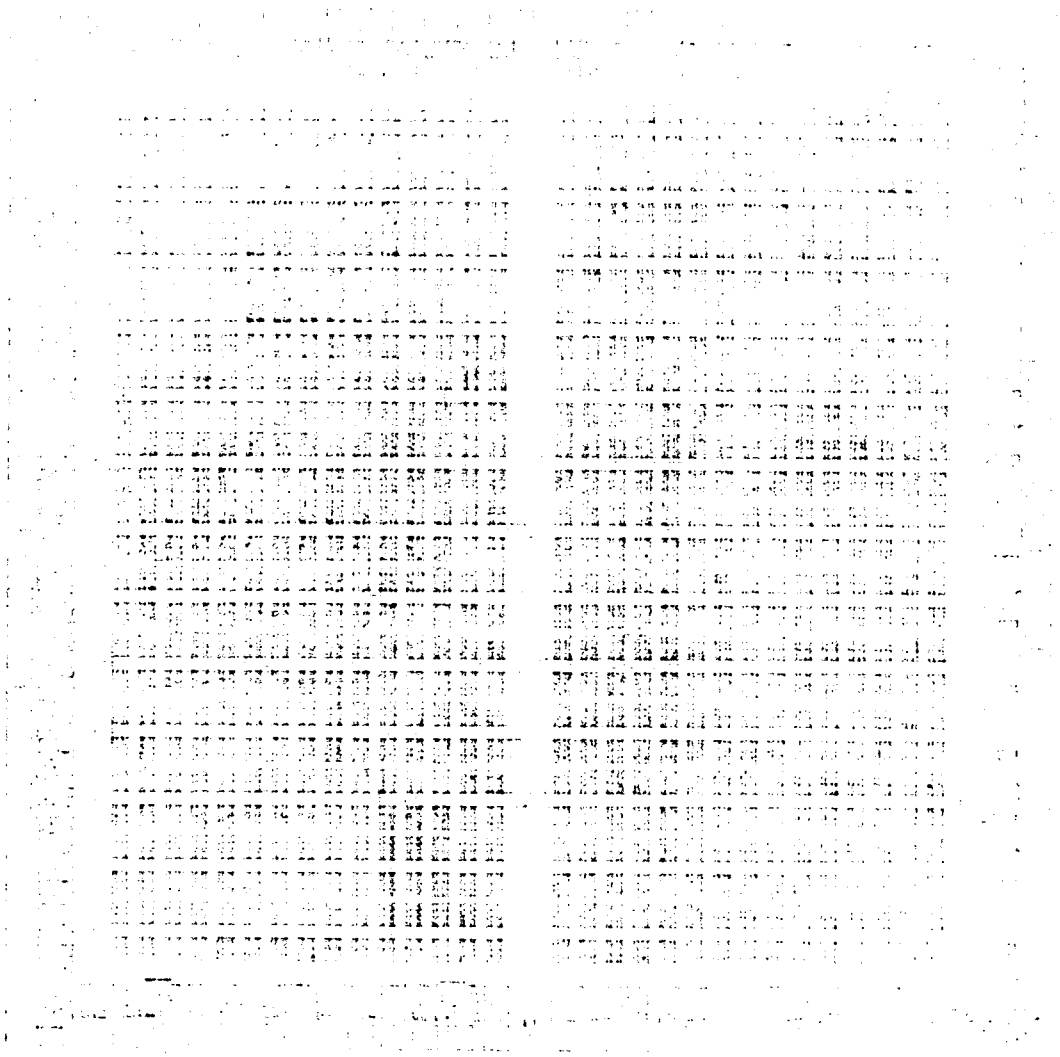


Fig. 1: A commercial masterslice uncommitted gate array. (Photo courtesy of Harris Corp., Melboure, Florida [8].)

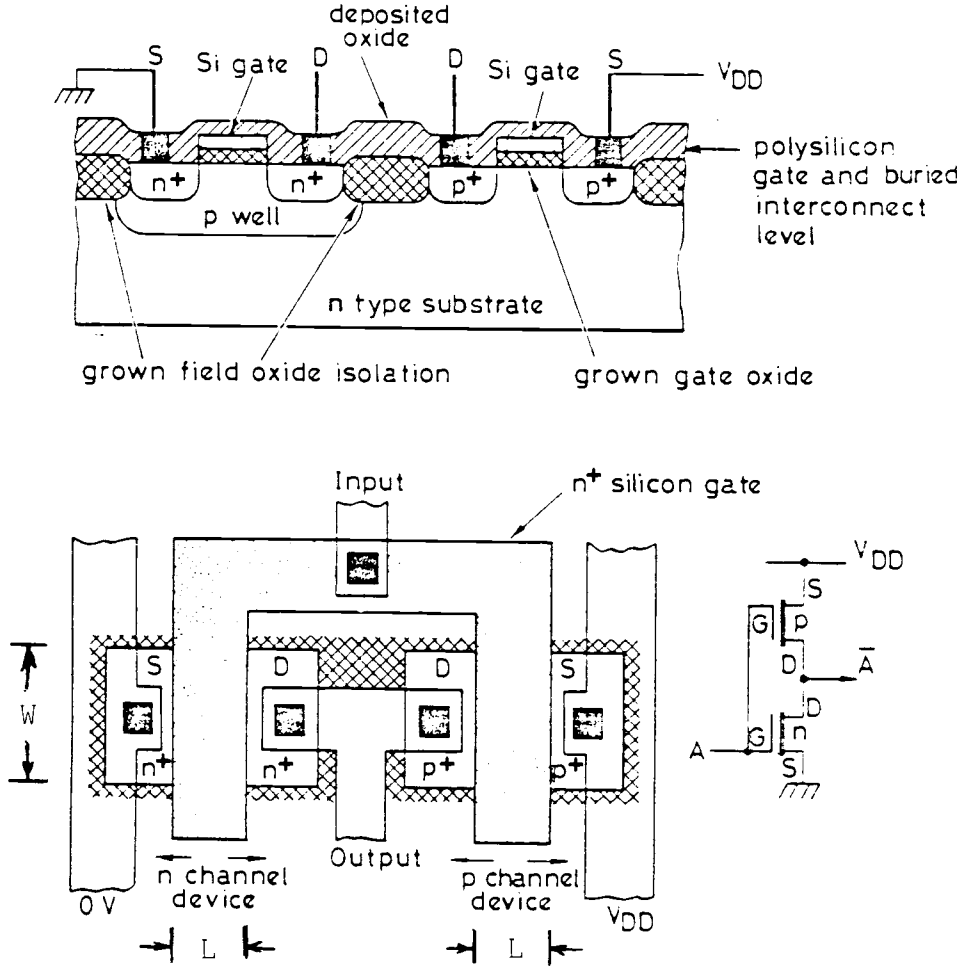
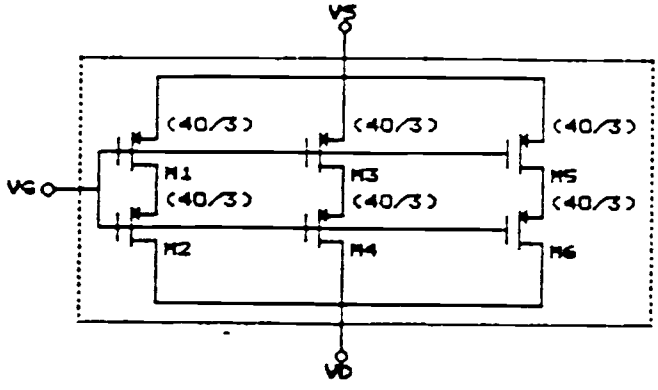
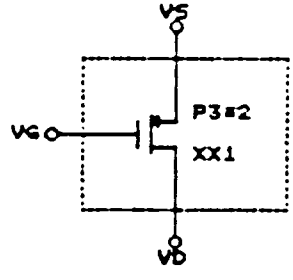


Fig. 2: A typical oxide-isolated separated p-well CMOS structure [8].



(a)



(b)

Fig. 3: (a) A composite PMOS device consisting of three primitives in parallel and two in series. This is approximately equivalent to (b) a single PMOS with 3X width and 2X length of primitive.

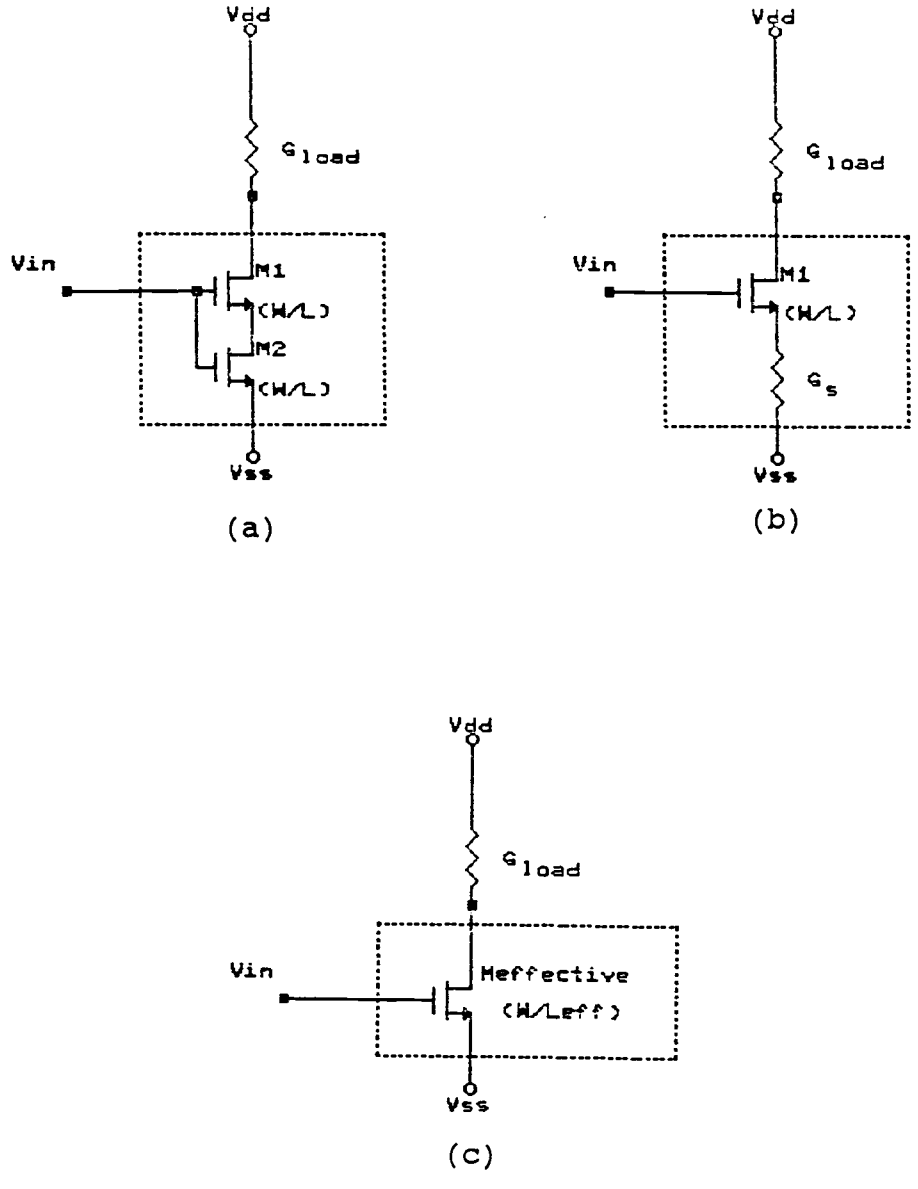


Fig. 4: (a) A composite-configured inverter is analogous to (b) an equivalent circuit model with series feedback resistor, or it can also be redefined as (c) an inverter with an effective device.

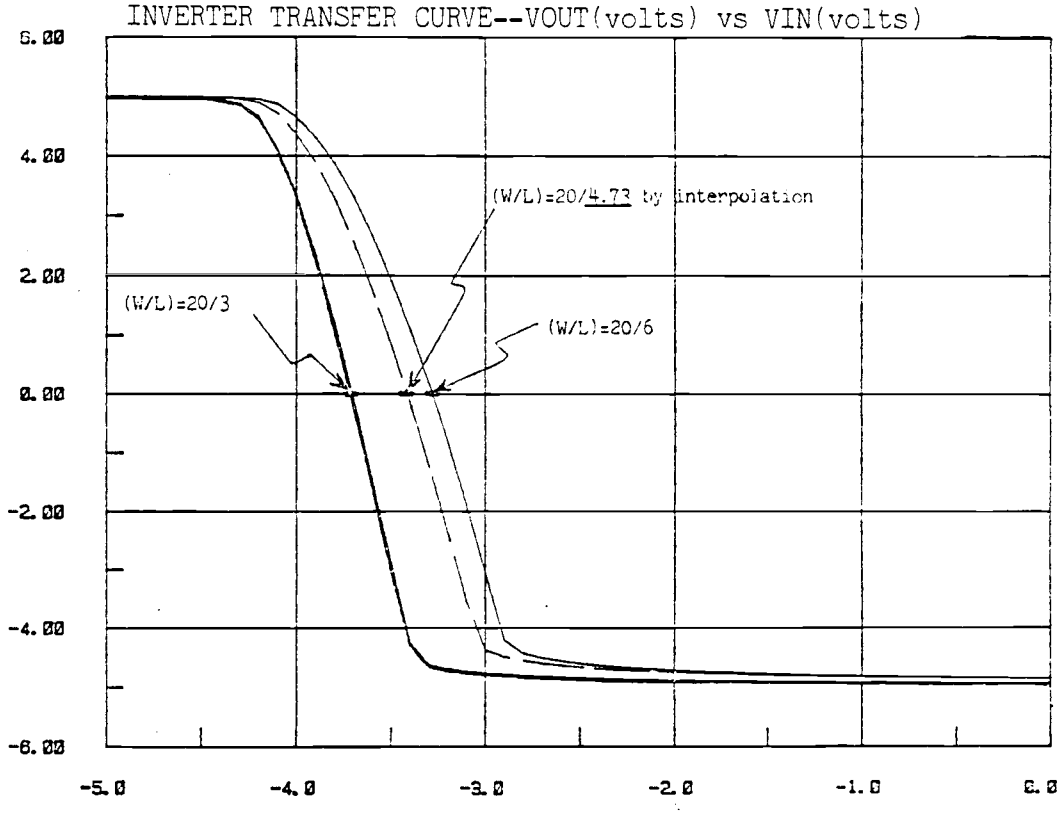
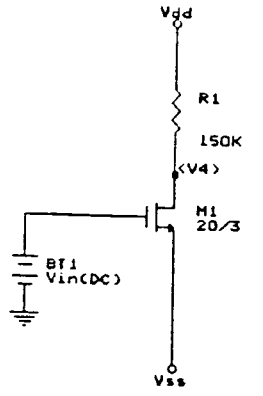
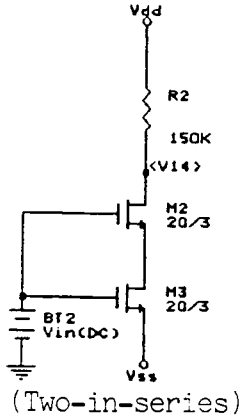


Fig. 5: An equivalent aspect ratio of a composite structure can be determined by interpolating the zero output point between those points of normal inverters with different aspect ratio and a same load resitance of 150K Ohm.



(Single device)

(a)



(Two-in-series)

(b)

Fig. 6: (a) A typical inverter which consists of a single active device and a resistor is compared to (b) a composite-configured inverter of two active devices in series.

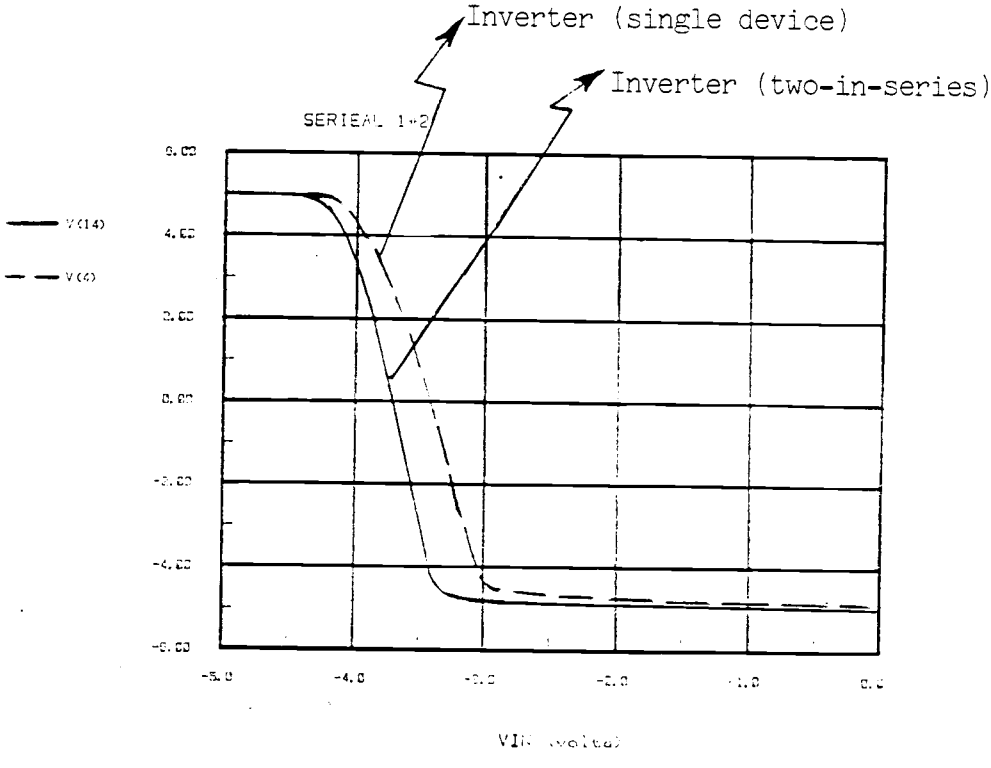


Fig. 7: (a) The inverter transfer curve of Fig. 6 (a) is compared to (b) the inverter transfer curve of Fig. 6 (b).

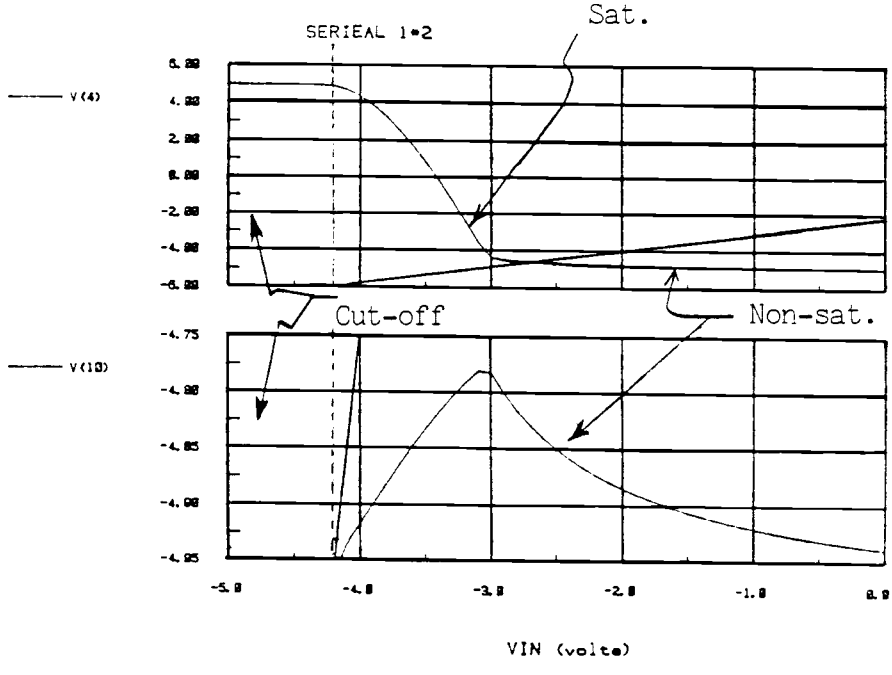
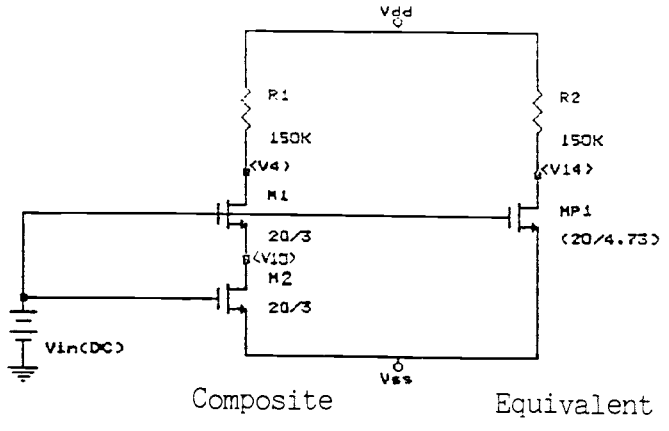
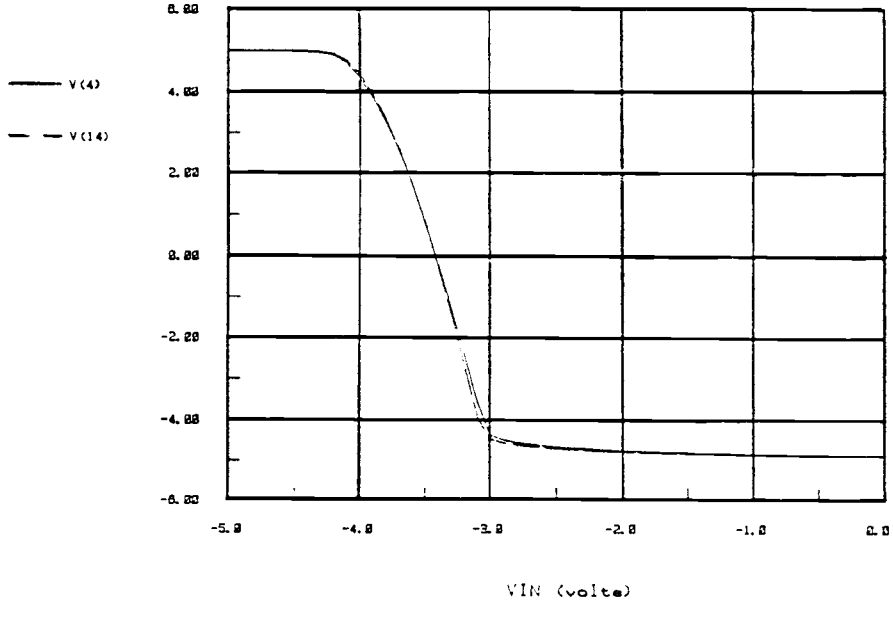


Fig. 8: Node analysis of two series-connected transistors in the inverter of Fig. 6 (b) reveal the drain-side transistor experiences transition from cutoff, saturation to nonsaturation, whereas, the other never experience saturation.

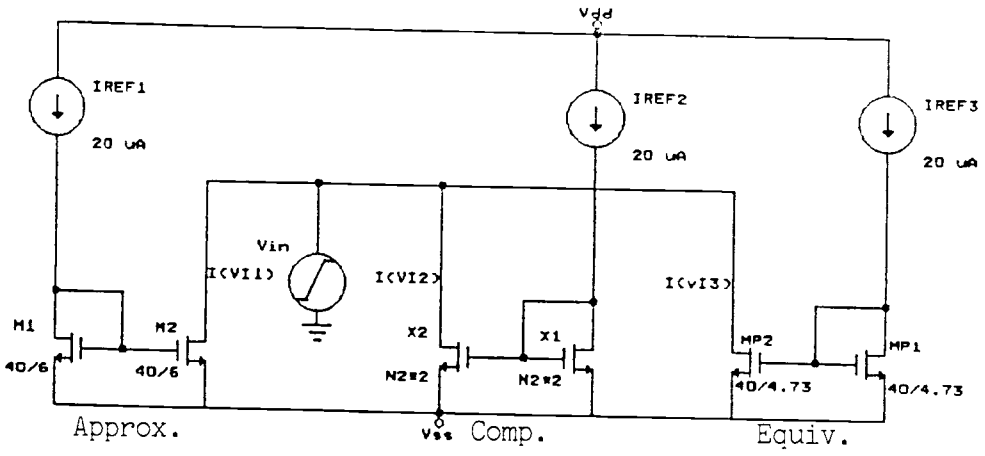


(a)

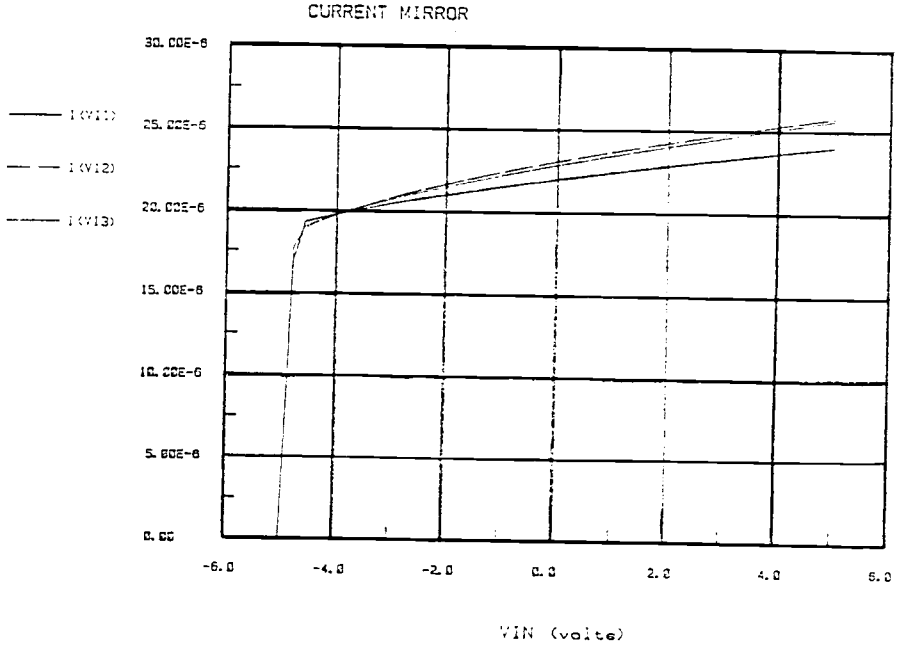


(b)

Fig. 9: (a) A circuit consisting of a composite-configured inverter and its equivalent inverter using a single device. Their inverter transfer curves are shown in (b).

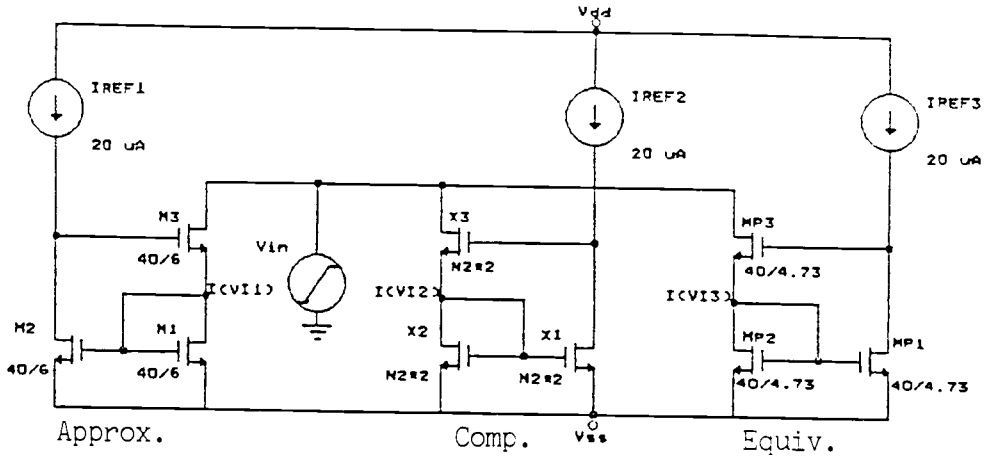


(a)

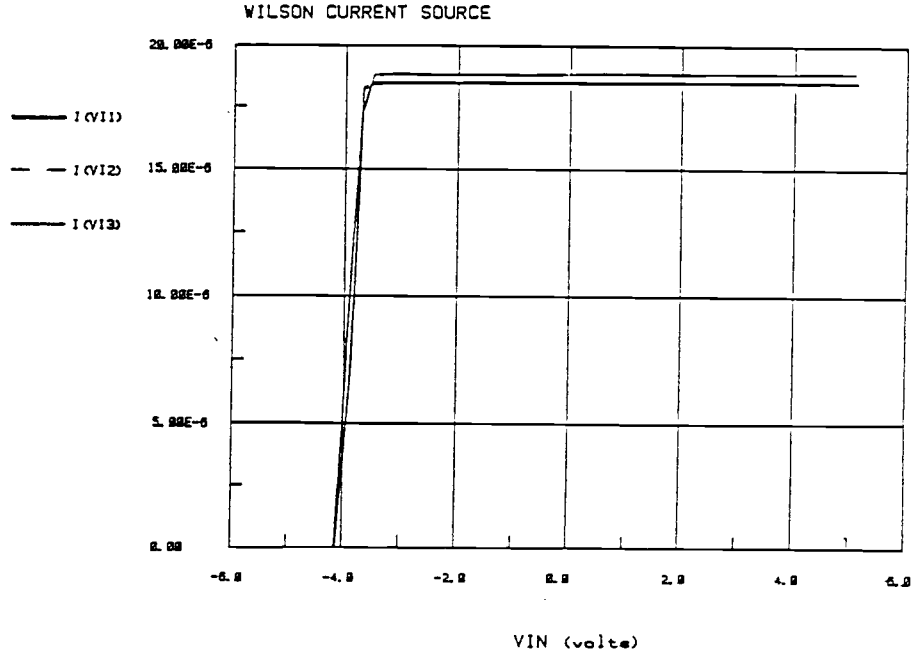


(b)

Fig. 10: (a) A circuit for comparing the performance of simple current source consists of a composite-configured structure, its approximated structure, and its equivalent structure. The performance of each individual structure is shown in (b).

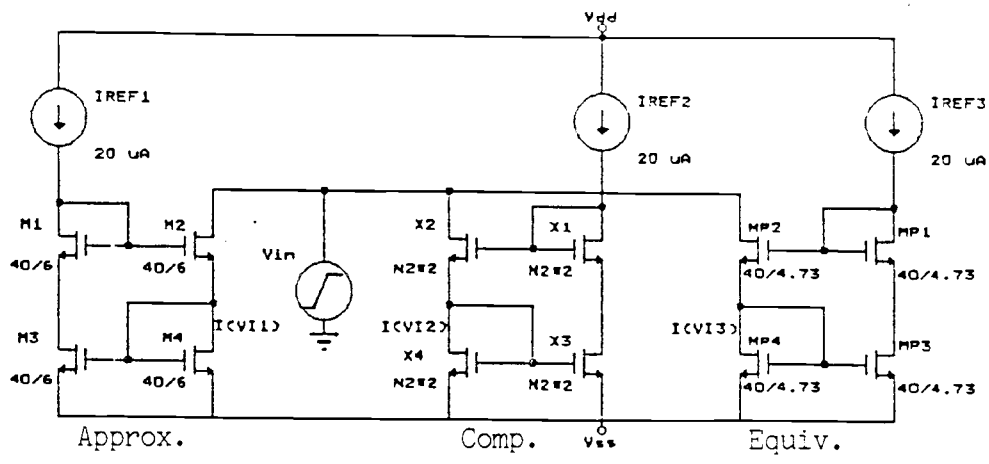


(a)

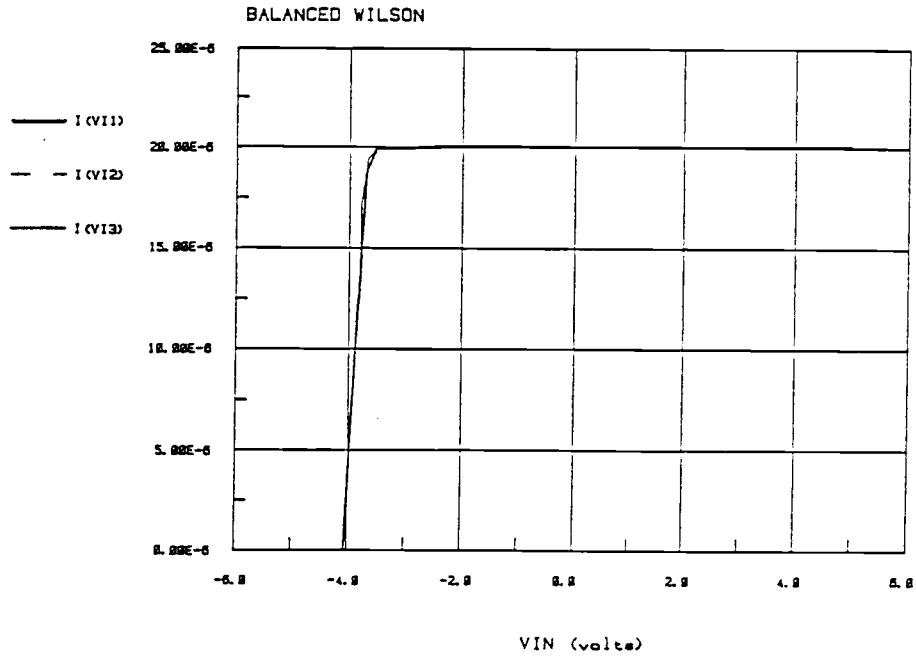


(b)

Fig. 11: (a) A circuit for comparing the performance of Wilson current source consists of a composite-configured structure, its approximated structure, and its equivalent structure. The performance of each individual structure is shown in (b).

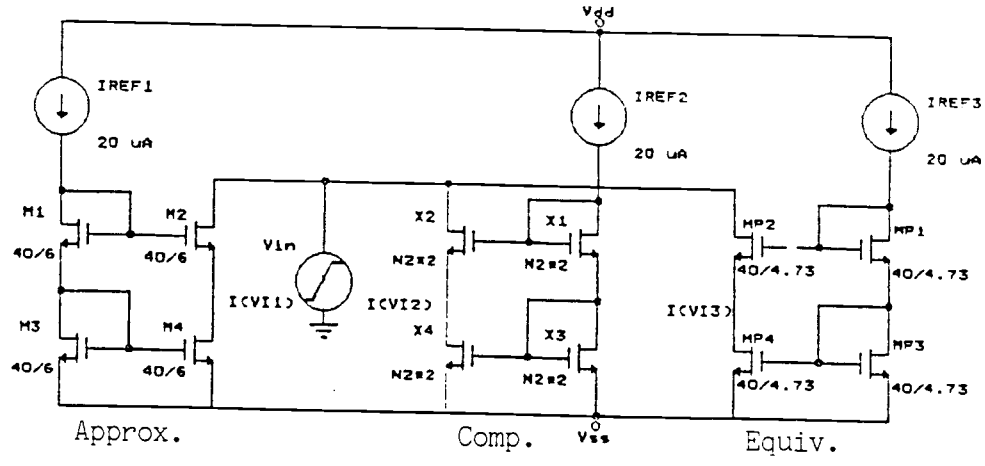


(a)

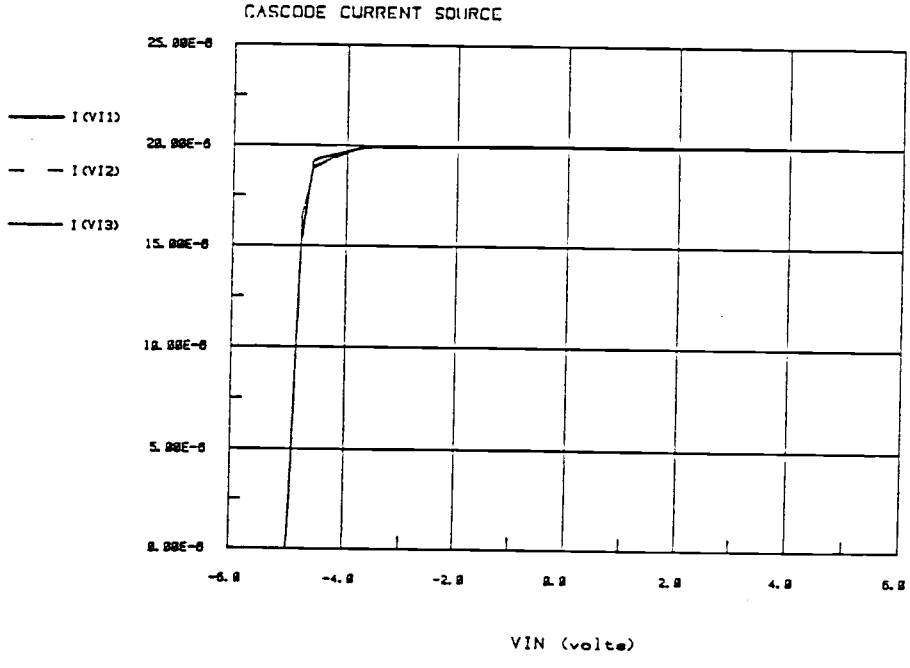


(b)

Fig. 12: (a) A circuit for comparing the performance of balanced Wilson current source consists of a composite-configured structure, its approximated structure, and its equivalent structure. The performance of each individual structure is shown in (b).

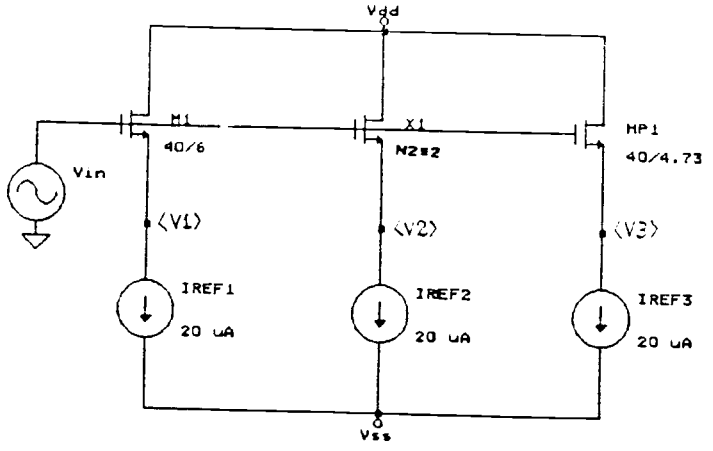


(a)

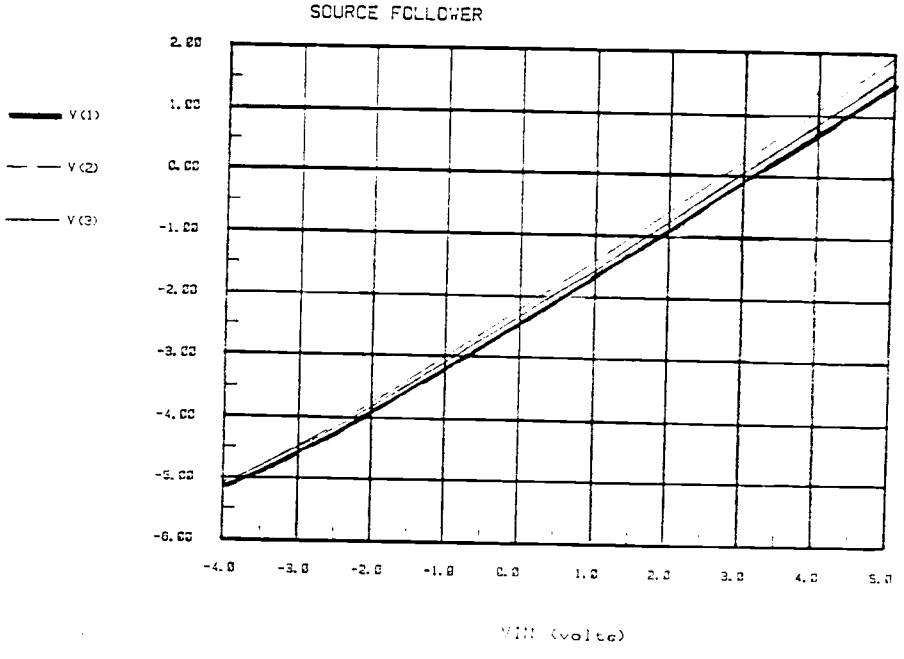


(b)

Fig. 13: (a) A circuit for comparing the performance of cascode current source consists of a composite-configured structure, its approximated structure, and its equivalent structure. The performance of each individual structure is shown in (b).

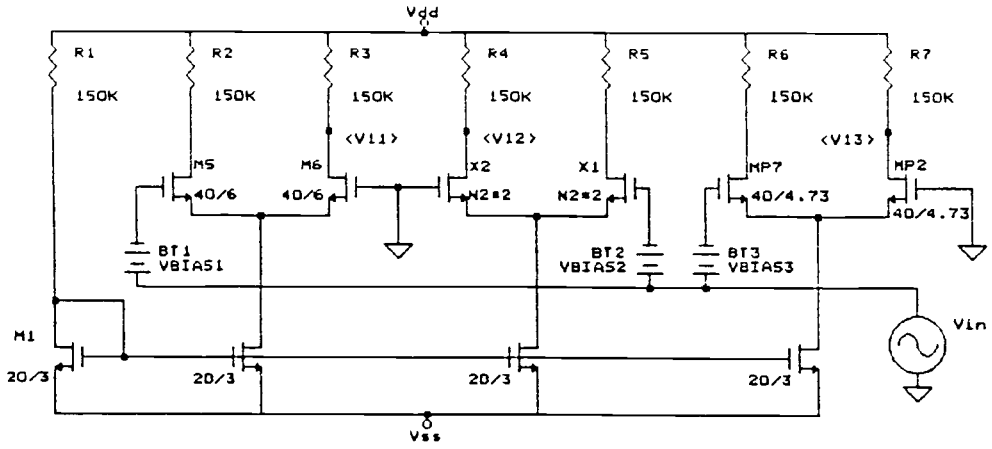


(a)



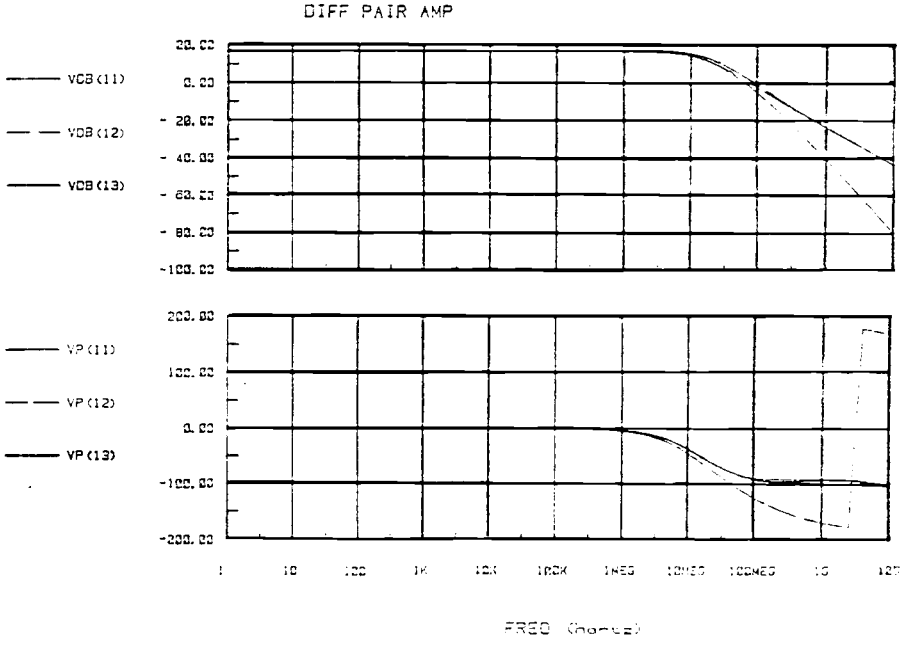
(b)

Fig. 14: (a) A circuit for comparing the performance of source follower consists of a composite-configured structure, its approximated structure, and its equivalent structure. The performance of each individual structure is shown in (b).



Approx. Comp. Equiv.

(a)



(b)

Fig. 15: (a) A circuit for comparing the performance of differntial-pair amplifier consists of a composite-configured structure, its approximated structure, and its equivalent structure. The performance of each individual structure is shown in (b).

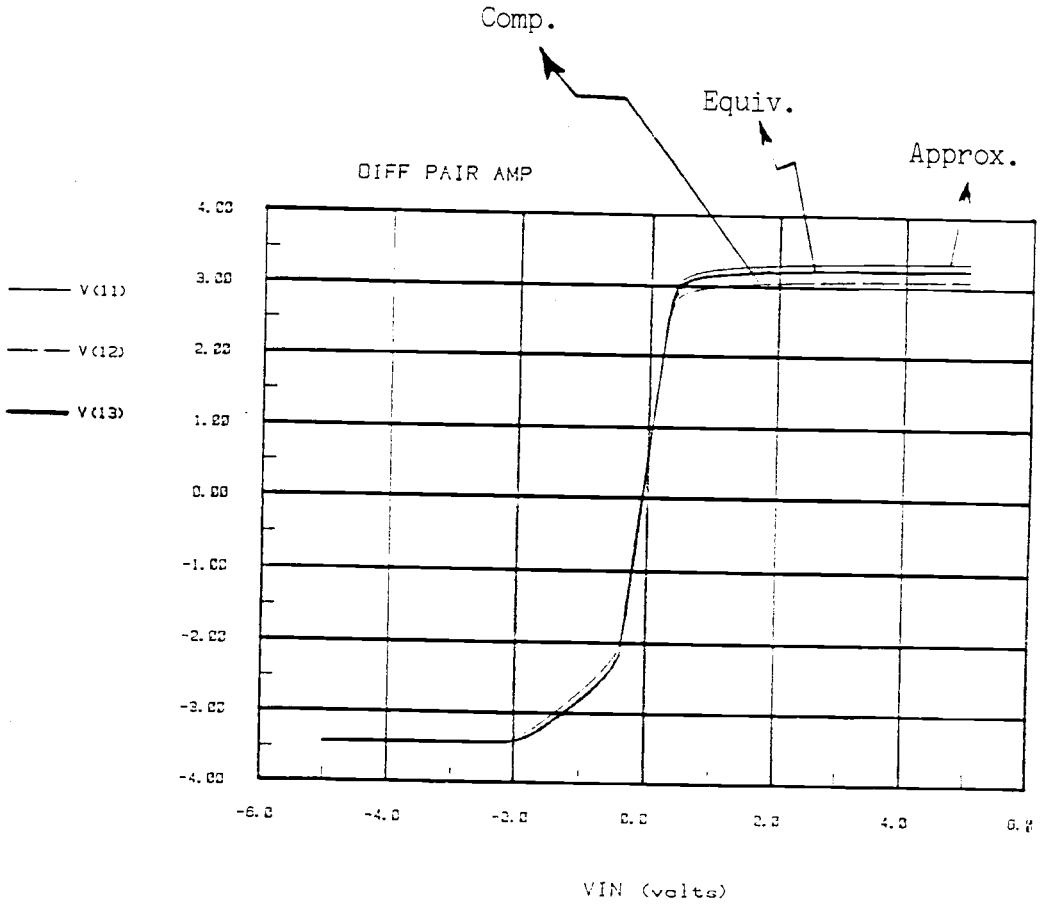
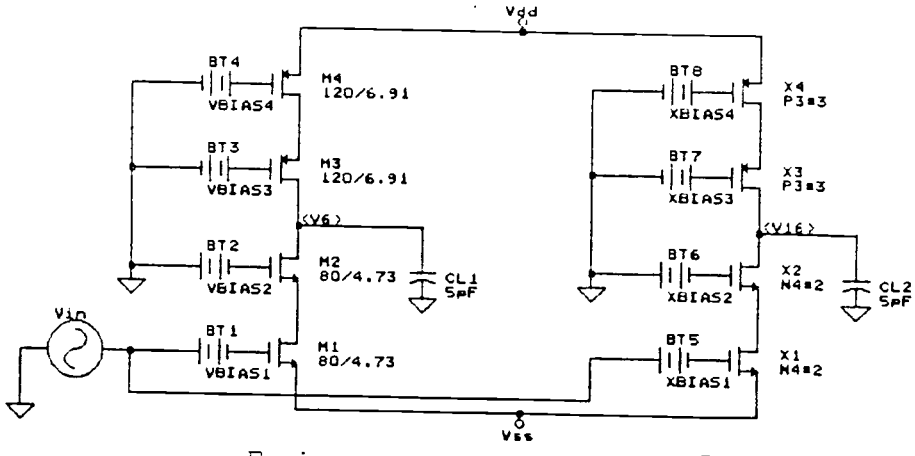
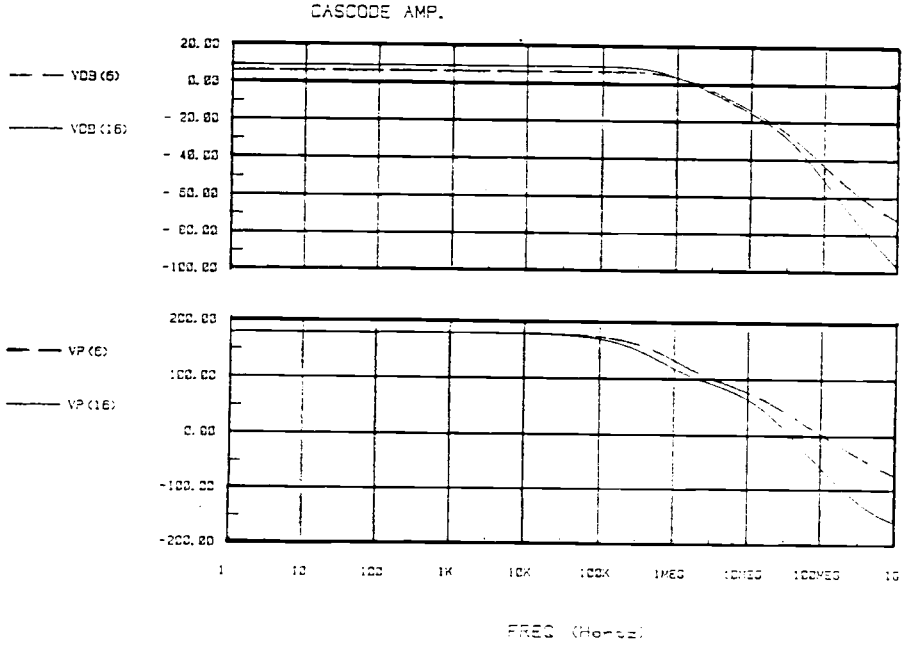


Fig. 16: The swing capability of different structures of the differential-pair amplifier of Fig. 15 (a).

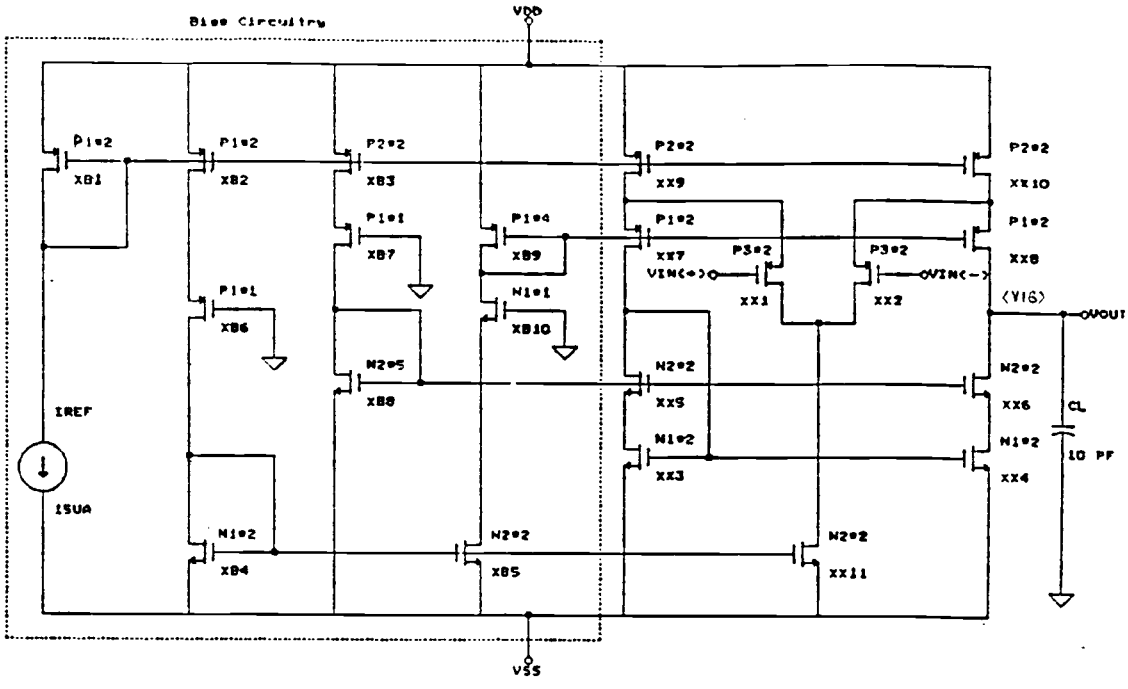


(a)

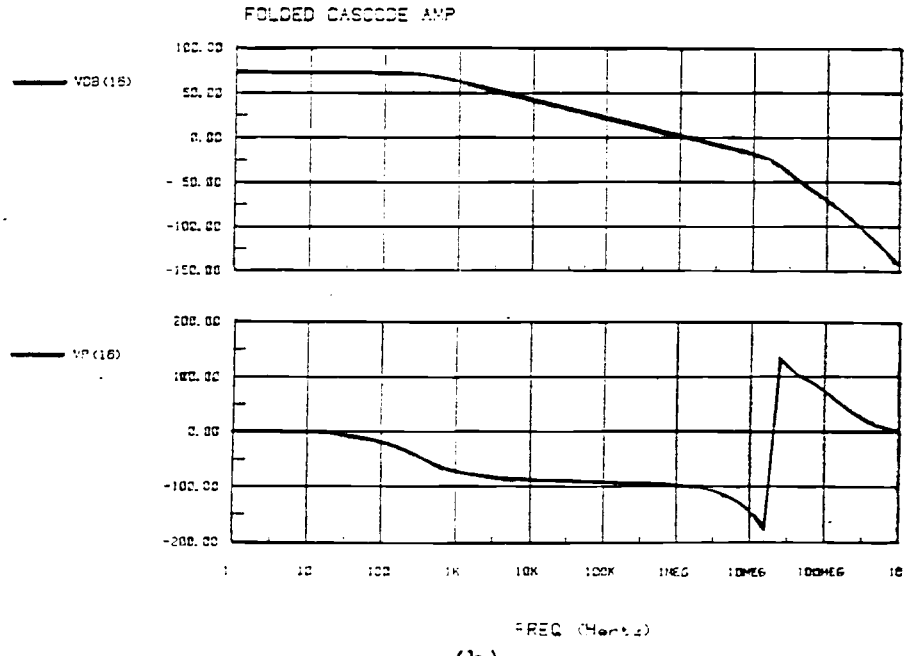


(b)

Fig. 17: (a) A circuit for comparing the performance of cascode amplifier consists of a composite-configured structure and its equivalent structure. The frequency responses of these two structure are shown in (b).



(a)



(b)

Fig. 18: (a) A folded-cascode amplifier with bias circuitry using the composite structure, and (b) its simulated SPICE result.

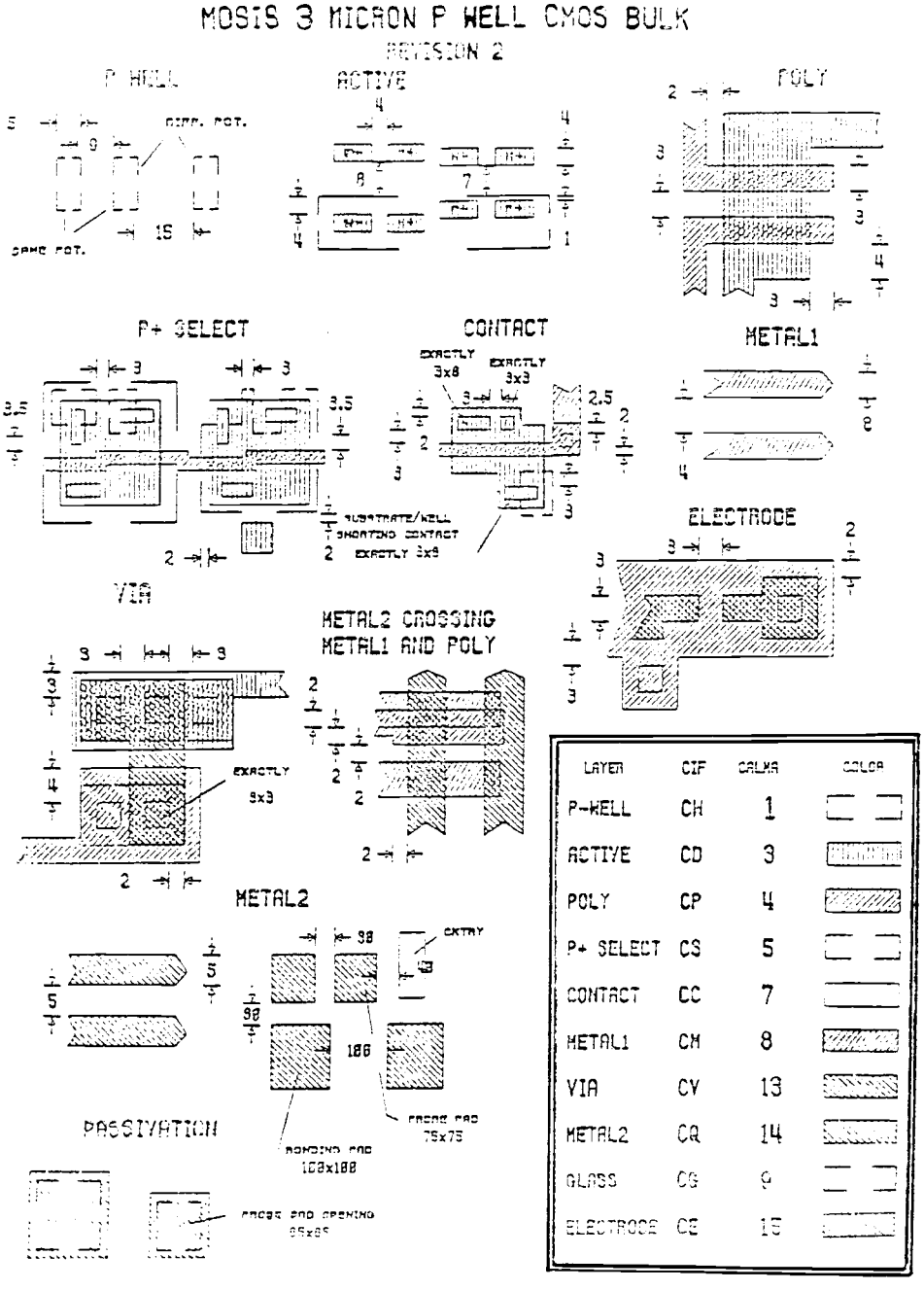


Fig. 19: Summarized design rules for MOSIS 3 µm p-well CMOS process.

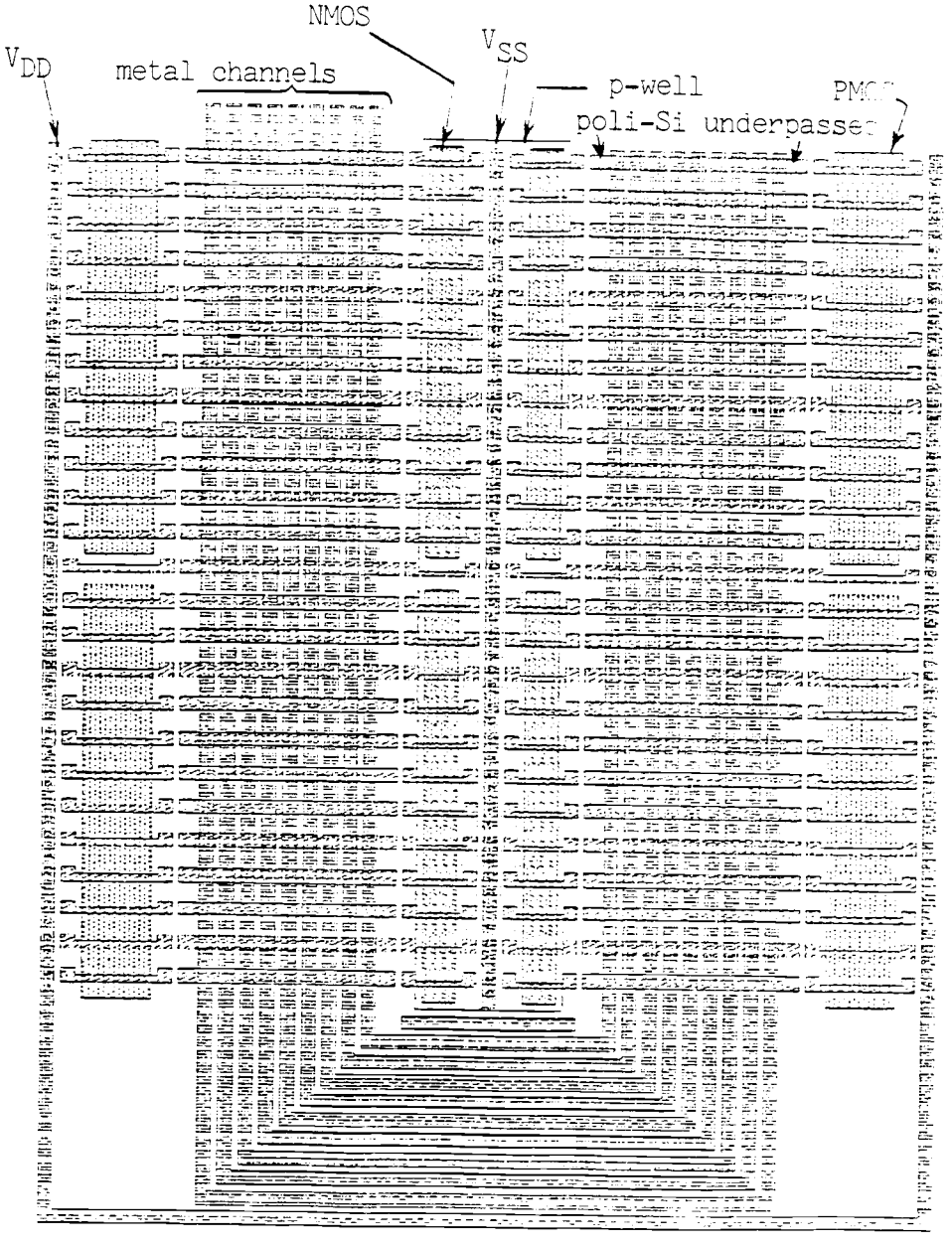


Fig. 20: The layout for a designed unprogrammble cell library.

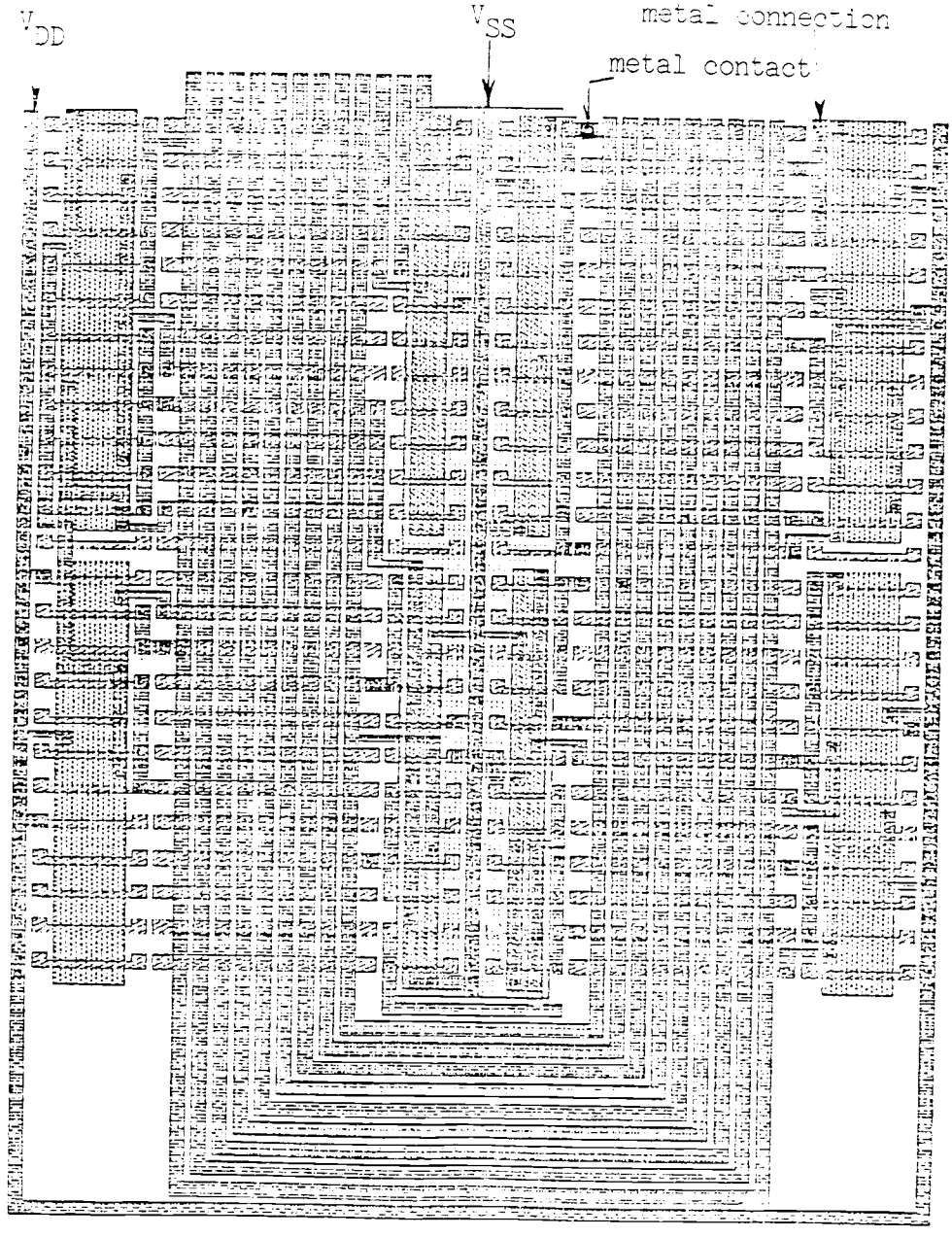


Fig. 21: The layout for a composite-configured folded-cascode amplifier with bias circuitry using the designed cell library.

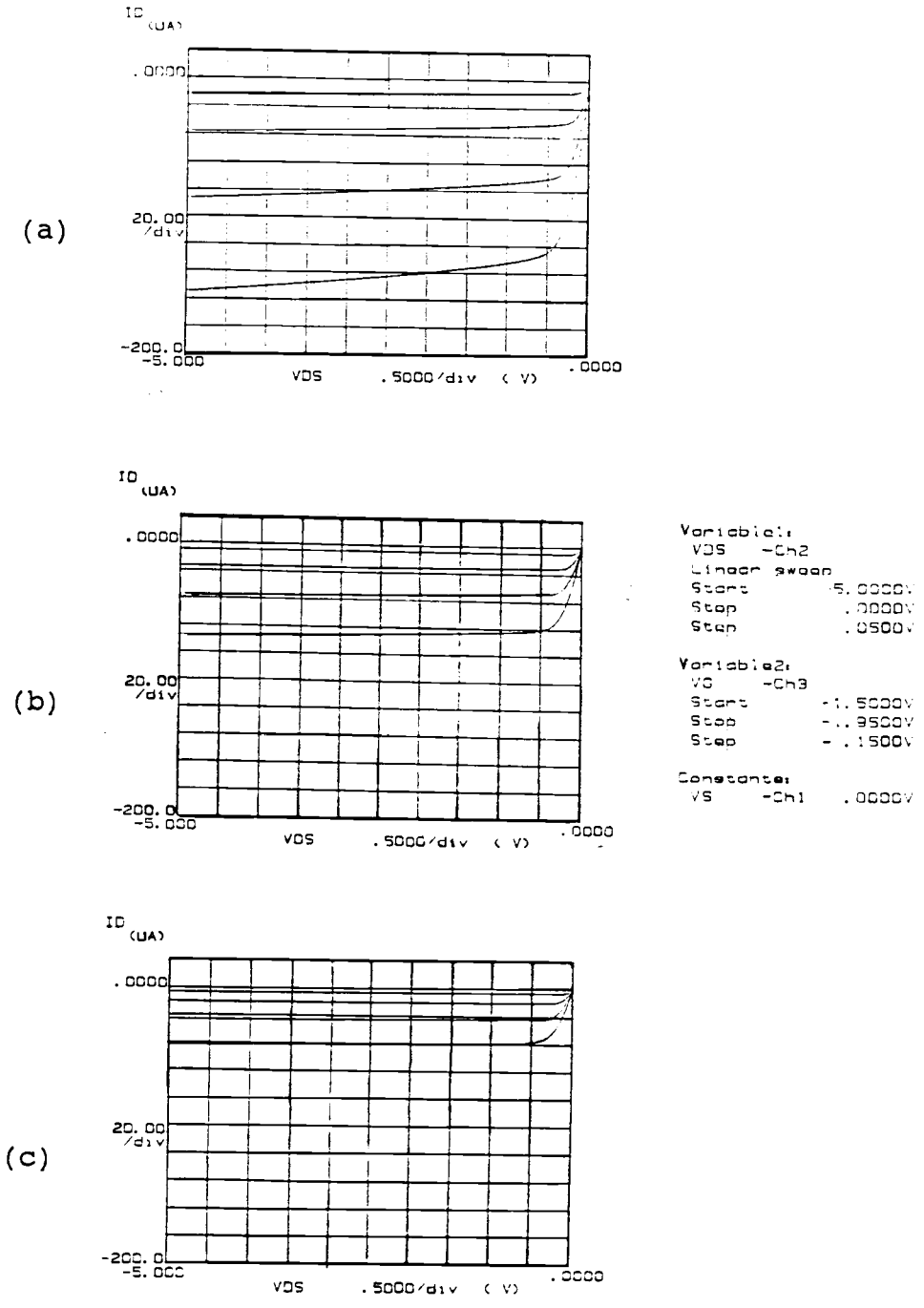


Fig. 22: PMOS device characteristics curves for (a) a single device, (b) a two-in-series structure, and (c) a three-in-series structure. The horizontal scale is 0.5 volts/division, the vertical is 20 μA/division, and the gate voltage step size is -0.15 volt.

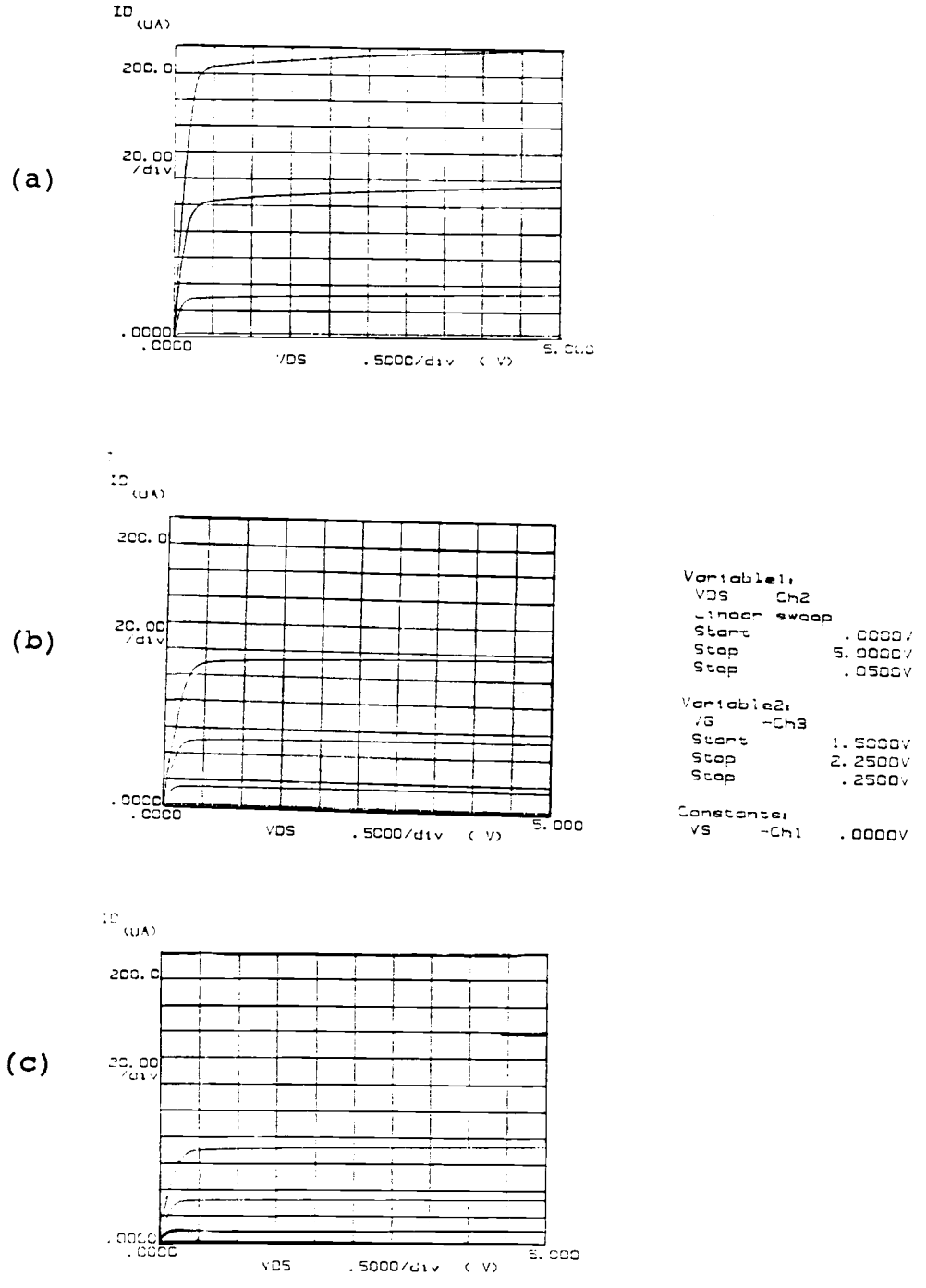


Fig. 23: NMOS device characteristics curves for (a) a single device, (b) a two-in-series structure, and (c) a three-in-series structure. The horizontal scale is 0.5 volts/division, the vertical is 20 μA/division, and the gate voltage step size is 0.25 volt.

TABLE 1: MOSIS 3 micron p-well CMOS process parameters.

	NMOS	PMOS
LEVEL	2	2
LD	2.8E-07	2.8E-7
TOX	5.0E-08	5.0E-08
SUB	1.0E+16	1.121088E+14
VTO	0.827125	-0.894654
KP	3.286649E-05	1.526452E-05
GAMMA	1.3596	0.87903
PHI	0.6	0.6
UO	200	100
UEXP	1.001E-03	0.153441
UCRIT	9.99E+05	1.63765E+04
DELTA	1.2405	1.93831
VMAX	1.0E+05	1.0E+05
XJ	4.0E-07	4.0E-07
LAMBDA	1.604983E-02	4.708659E-02
NFS	1.234795E+12	8.788617E+11
NEFF	1.001E-02	1.001E-02
TPG	1.0	-1.0
RSH	25	95
CGSO	5.2E-10	4.0E-10
CGDO	5.2E-10	5.2E-10
CJ	3.2E-04	2.0E-04
MJ	0.5	0.5
CJSW	9.0E-10	4.5E-10
MJSW	0.33	0.33
AF	1.25	1.25
KF	1.0E-27	1.0E-27

TABLE 2: Performance comparison for the general purpose amplifier and the composite-configured folded-cascode amplifier.

	General	Composite
AC gain (dB)	80	73
Unit-gain bandwidth (Meg Hz)	2	1.7
Phase margin (degree)	> 60	80
Gain margin (dB)	> 12	22
Slew-rate (volt/us)	2.0 - 4.0	2.3
Common-mode rejection ratio, CMRR (dB)	> 80	100
Common-mode range, CMR (volt)	-5.0 - 3.0	-5.0 - 3.5
Power consumption (m Watt)	1.0 - 2.0	1.34

VII. BIBLIOGRAPHY

[1] Y.P. Tsividis, "Analog MOS Integrated Circuits--Certain New Ideas, Trends, and Obstacles," IEEE J. Solid-State Circuits, vol. SC-22, no. 3, pp. 317-321, June 1986.

[2] R. Kash, "Building Quality Analog Circuits with C-MOS Logic Arrays," Electronics, pp. 109-112, August 11, 1981.

[3] R. Hagelauer and K. Ronge, "Analog Functions Implemented on Digital CMOS Gate Arrays--Merits and Problems," IEEE Trans. Industrial Electronics, vol. IE-33, no. 4, pp. 371-376, November 1986.

[4] D.C. Stone, J.E. Schroeder, R.H. Kaplan, and A.R. Smith, "Analog CMOS Building Blocks for Custom and Semicustom Applications," IEEE J. Solid-State Circuits, vol. SC-19, no. 1, pp. 55-61, February 1984.

[5] G. Giannella, "Array IC Presents New Ways To Customize Analog Circuits Without Wasting Silicon," Electronic Design, pp. 171-178, May 1, 1986.

[6] G.L. Heyes and J.S. Shier, "Analog Arrays Speed Design and Lower Cost of UHF Chips," Electronic Design, pp. 119-123, December 11, 1986.

[7] A. Vladimirescu, K. Zhang, A.R. Newton, D.O. Pederson, and A. Sangiovanni-Vincentelli, "SPICE Version 2G.5 User's Guide," Dept. Elec. Eng. and Computer Sci., Univ. of California, Berkeley, California, 1981.

[8] S.L. Hurst, "Custom-specific Integrated Circuits--Design and Fabrication," Marcell Dekker, New York, First Edition, 1985.

[9] J. Wiegand, "Gate Array Trend--An Introduction," Electronic Design News, pp. 135-140, June 25, 1987.

[10] J.G. Posa, "Gate Arrays--A Special Report," Electronics, pp. 145-158, September 25, 1980.

[11] C.T. Sah, "Characteristics of the Metal-Oxide-Semiconductor Transistors," IEEE Trans. Electron Devices, vol. ED-11, no. 7, pp. 324-330, July 1964.

[12] P.R. Gray and R.G. Meyer, "MOS Operational Amplifier Design--A Tutorial Overview," IEEE J. Solid-State Circuits, vol. SC-17, no. 6, pp. 969-982, December 1982.

[13] E.A. Vittoz, "The Design of High-Performance Analog Circuits on Digital CMOS Chips," IEEE J. Solid-State Circuits, vol. SC-20, no. 3, pp. 657-665, June 1985.

VIII. APPENDICES

VIII. APPENDICES

8.1 Derivation for The Equivalent Model

(A) Small signal gain for Fig. 4 (b)

$$A_{v[A]} = \frac{G_m}{G_{load} + G_{ds}} ;$$

where

$$G_{ds} = \frac{G_s\, G_{ds1}}{G_s + (G_{m1} + G_{mbs1} + G_{ds1})} ,$$

$$G_m = \frac{G_s\, G_{m1}}{G_s + (G_{m1} + G_{mbs1} + G_{ds1})} ,$$

and $G_{m1} \approx (2\, K\, (W/L)\, I)^{\frac{1}{2}}$, $G_{ds1} \approx \lambda\, I$,

$G_{mbs1} \approx \eta\, G_{m1}$,

$\eta = 0.01 - 0.1$, depends on voltage between bulk substrate and source.

(B) Small signal gain for Fig. 4 (c)

Similarly,

$$A_{v[B]} = \frac{G_{m[eff]}}{G_{load} + G_{ds[eff]}} ;$$

where $G_{m[eff]} \approx (2\, K\, (W / L_{eff})\, I)^{\frac{1}{2}}$,

$G_{ds[eff]} \approx \lambda'\, I = (L / L_{eff})\, \lambda\, I$

$= (L / L_{eff}) * G_{ds1}$

At output node, let $A_{v[A]} = A_{v[B]}$, and normally G_{mbs1}, $G_{ds1} << G_{m1}$. Hence Eqn. (1) - (5) can be attained.

8.2 SPICE Program for A Folded-cascode Amplifier

```
FOLDED-CASCODE AMPLIFIER SIMULATION PROGRAM

*********************************************************
***     THIS IS A SPICE PROGRAM, THE CIRCUITRY IS     ***
***     CONSTRUCTED ACCORDING TO THE COMPOSITE        ***
***     CONFIGURATION TECHNIQUE.                      ***
*********************************************************

********* POWER SUPPLY ************************
VDD 7 0 DC 5
VSS 9 0 DC -5

********* DIFFERENTIAL MODE INPUT  ***********
*** ===>  INPUT OFFSET VOLTAGE = 8.02231E-4
VIN 11 0 DC 8.02231E-4 AC 1
X2 18 0 19 9 23 24 25 GA3*2

********* COMMON     MODE   INPUT  ***********
*VOS 11 500 DC 8.02231E-4
*VIN 500 0 AC 1
*X2 18 500 19 9 23 24 25 GA3*2

*********   OUTPUT     CAPACITANCE ***********
CLOAD 16 0 10P

*********    BIAS      CIRCUITRY     ********************
IREF  4    9   14U
XB1   4    4     7    7   110          GB1*2
XB2  101   4     7    7   111          GB1*2
XB3  102   4     7    7   112 113      GB2*2
XB4   1    1     9    9   114          GA1*2
XB5  103   1     9    9   115 116      GA2*2
MB6   1    0   101    7   P03 W=40U L=3U AD=3.6E-10
+                             AS=3.6E-10 PD=58U PS=58U
MB7   2    0   102    7   P03 W=40U L=3U AD=3.6E-10
+                             AS=3.6E-10 PD=58U PS=58U
XB8   2    2     9    9   117 118 119 120 121 122 123 124
+                                GA2*5
XB9   3    3     7    7   125 126 127 GB1*4
MB10  3    0   103    9   N03 W=20U L=3U AD=1.8E-10
+                             AS=1.8E-10 PD=38U PS=38U
*********************************************************

******<<<< COMPOSITE CONFIGURATED STRUCTURE >>>>*****
******[1] NMOS PRIMITIVES TWO-IN-SERIES
.SUBCKT GA1*2 1 2 3 4 5
M1 1 2 5 4 N03 W=20U L=3U AD=1.8E-10 AS=1.8E-10 PD=38U
+              PS=38U
M2 5 2 3 4 N03 W=20U L=3U AD=1.8E-10 AS=1.8E-10 PD=38U
```

```
+                PS=38U
.ENDS GA1*2

******[2] NMOS PRIMITIVES TWO-IN-SERIES & TWO-IN-PARALLEL
.SUBCKT GA2*2 1 2 3 4 5 6
X1 1 2 3 4 5 GA1*2
X2 1 2 3 4 6 GA1*2
.ENDS GA2*2

******[3] NMOS PRIMITIVES TWO-IN-SERIES & THREE-IN-
******    PARALLEL
.SUBCKT GA3*2 1 2 3 4 5 6 7
X1 1 2 3 4 5 GA1*2
X2 1 2 3 4 6 GA1*2
X3 1 2 3 4 7 GA1*2
.ENDS GA3*2

******[4] NMOS PRIMITIVES FIVE-IN-SERIES
.SUBCKT GA1*5 1 2 3 4 5 6 7 8
M1 1 2 5 4 N03 W=20U L=3U AD=1.8E-10 AS=1.8E-10 PD=38U
+               PS=38U
M2 5 2 6 4 N03 W=20U L=3U AD=1.8E-10 AS=1.8E-10 PD=38U
+               PS=38U
M3 6 2 7 4 N03 W=20U L=3U AD=1.8E-10 AS=1.8E-10 PD=38U
+               PS=38U
M4 7 2 8 4 N03 W=20U L=3U AD=1.8E-10 AS=1.8E-10 PD=38U
+               PS=38U
M5 8 2 3 4 N03 W=20U L=3U AD=1.8E-10 AS=1.8E-10 PD=38U
+               PS=38U
.ENDS GA1*5

******[5] NMOS PRIMITIVES FIVE-IN-SERIES & TWO-IN-PARALLEL
.SUBCKT GA2*5 1 2 3 4 5 6 7 8 9 10 11 12
X1 1 2 3 4 5 6 7 8 GA1*5
X2 1 2 3 4 9 10 11 12 GA1*5
.ENDS GA2*5

******[6] PMOS PRIMITIVES TWO-IN-SERIES
.SUBCKT GB1*2 1 2 3 4 5
M1 1 2 5 4 P03 W=40U L=3U AD=3.6E-10 AS=3.6E-10 PD=58U
+               PS=58U
M2 5 2 3 4 P03 W=40U L=3U AD=3.6E-10 AS=3.6E-10 PD=58U
+               PS=58U
.ENDS GB1*2

******[7] PMOS PRIMITIVES TWO-IN-SERIES
.SUBCKT GB2*2 1 2 3 4 5 6
X1 1 2 3 4 5 GB1*2
X2 1 2 3 4 6 GB1*2
.ENDS GB2*2
```

```
******[8] PMOS PRIMITIVES THREE-IN-SERIES
.SUBCKT GB1*3 1 2 3 4 5 6
M1 1 2 5 4 P03 W=20U L=3U AD=1.8E-10 AS=1.8E-10 PD=38U
+              PS=38U
M2 5 2 6 4 P03 W=20U L=3U AD=1.8E-10 AS=1.8E-10 PD=38U
+              PS=38U
M3 6 2 3 4 P03 W=20U L=3U AD=1.8E-10 AS=1.8E-10 PD=38U
+              PS=38U
.ENDS GB1*3

******[9] PMOS PRIMITIVES FOUR-IN-SERIES
.SUBCKT GB1*4 1 2 3 4 5 6 7
M1 1 2 5 4 P03 W=20U L=3U AD=1.8E-10 AS=1.8E-10 PD=38U
+              PS=38U
M2 5 2 6 4 P03 W=20U L=3U AD=1.8E-10 AS=1.8E-10 PD=38U
+              PS=38U
M3 6 2 7 4 P03 W=20U L=3U AD=1.8E-10 AS=1.8E-10 PD=38U
+              PS=38U
M4 7 2 3 4 P03 W=20U L=3U AD=1.8E-10 AS=1.8E-10 PD=38U
+              PS=38U
.ENDS GB1*4
*****************************************************

*********  FOLDED-CASCODE MAIN FRAME  **************
X1    8 11 19  9 20 21 22 GA3*2
X3    5  6  9  9 26       GA1*2
X4   15  6  9  9 27       GA1*2
X5    6  2  5  9 28 29    GA2*2
X6   16  2 15  9 30 31    GA2*2
X7    6  3  8  7 32       GB1*2
X8   16  3 18  7 33       GB1*2
X9    8  4  7  7 34 35    GB2*2
X10 18  4  7  7 36 37     GB2*2
X11 19  1  9  9 38 39     GA2*2
*****************************************************

********* MODEL CARDS FOR DIFFERENT DEVICES  ********
****       NOMINAL N-CHANNEL MODEL ( L=3 MICRONS )

.MODEL    N03  NMOS  LEVEL=2  LD=0.28U  TOX=500E-10
+         NSUB=1.0E+16  VTO=0.827125  KP=3.286649E-05
+         GAMMA=1.3596  PHI=0.6  UO=200  UEXP=1.001E-03
+         UCRIT=999000  DELTA=1.2405  VMAX=100000  XJ=0.4U
+         LAMBDA=1.604983E-02  NFS=1.234795E+12
+         NEFF=1.001E-02  TPG=1.0  RSH=25  CGSO=5.2E-10
+         CGDO=5.2E-10  CJ=3.2E-04  MJ=0.5  CJSW=9.0E-10
+         MJSW=0.33  AF=1.25  KF=1.0E-27

*         NOMINAL P-CHANNEL MODEL ( L=3 MICRONS )

.MODEL    P03  PMOS  LEVEL=2  LD=0.28U  TOX=500E-10
+         NSUB=1.121088E+16 VTO=-0.894654 KP=1.526452E-05
```

```
+         GAMMA=0.879003  PHI=0.6  UO=100  UEXP=0.153441
+         UCRIT=16376.5  DELTA=1.93831 VMAX=100000 XJ=0.4U
+         LAMBDA=4.708659E-02  NFS=8.788617E+11
+         NEFF=1.001E-02  TPG=-1.0  RSH=95  CGSO=4E-10
+         CGDO=5.2E-10  CJ=2E-04  MJ=0.5  CJSW=4.5E-10
+         MJSW=0.33 AF=1.25  KF=1.5E-27
**************************************************

********* SET NODE VOLTAGE TO ENSURE CONVERGENCE  *******
.NODESET V(6)=0 V(8)=4.5078 V(18)=4.5078 V(16)=0
+         V(19)=-4.535  V(15)=-4.535  V(5)=-4.535
+         V(1)=-3.664  V(2)=-3.31  V(3)=2.286   V(4)=3.577
+         V(101)=1.878 V(102)=2.033 V(103)=-2.284
**********************************************************

******** OPTIONS CARD FOR PAGE SUPRESSION AND MORE
******** TOLERANCE
.OPTIONS GMIN=1E-10 NOMOD NOPAGE ITL1=200 ITL2=100 ITL4=20
+         ITL5=1E4   NUMDGT=6

******  DC TRANSFER CURVE ***********
*.DC VIN .80M .81M 1U
*.PRINT DC V(16)
**************************************

******  AC ANALYSIS *****************
.AC DEC 5 1 1G
.TF V(16) VIN
.GR AC VDB(16) VP(16)
.PLOT AC VDB(16) VP(16)
.PR AC VDB(16) VP(16)

******  INPUT NOISE ANALYSIS ********
.NOISE V(16) VIN 10
.GR NOISE INOISE
.PLOT NOISE INOISE
.PR NOISE INOISE
**************************************

.END
```