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John F. Wager

The primary focus of this thesis is modifying the comprehensive depletion-mode model and extending its applicability to p-channel thin-film transistor (TFT) behavior and subthreshold (subpinchoff) operation. The comprehensive depletion-mode model accurately describes depletion-mode TFT behavior and establishes a set of equations, different from those obtained from square-law theory, which can be used for carrier mobility extraction.

In the modified comprehensive depletion-mode model, interface mobility ($\mu_{INTERFACE}$) and bulk mobility (μ_{BULK}) are distinguished. Simulation results reveal that when square-law theory mobility extraction equations are used to assess depletion-mode TFTs, the estimated interface mobility is often overestimated. In addition, the carrier concentration of a thin channel layer can be estimated from an accurate fitting of measured depletion-mode TFT current-voltage characteristics curves using the comprehensive depletion-mode model.

Comprehensive Depletion-Mode Modeling of Oxide Thin-Film Transistors

by
Fan Zhou

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APPROVED:

Major Professor, representing Electrical and Computer Engineering

Head of the School of Electrical Engineering and Computer Science

Dean of the Graduate School

I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Fan Zhou, Author

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COMPREHENSIVE DEPLETION-MODE MODELING OF OXIDE THIN-FILM TRANSISTORS

1. INTRODUCTION

Since oxide thin-film transistors (TFTs) were reported in 2003, a transparent electronics revolution was initiated because of the multiplicity of applications.[1-3] Possible application includes various types of displays and transparent circuits.[4] Oxide TFT technology is moving towards commercialization.[5-9]

Most oxide TFTs are n-channel. Indium Gallium Zinc Oxide (IGZO) TFT are notable examples which are now beginning to replace amorphous-silicon TFTs (a-Si TFTs), in flat-panel display application. N-channel oxide TFT technology is analogous to n-channel metal-oxide-semiconductor (NMOS) silicon technology. Before oxide TFTs can move to a higher performance, complementary metal-oxide semiconductor (CMOS)-like technology -- which combines n- and p-type semiconductors.[5] -- p-channel oxide TFTs must be developed. However, realizing high-performance p-channel oxide TFT is much more difficult mainly due to the fact that p-type oxides invariably have low hole mobilities. Thus, the development of high performance p-channel oxide TFTs is an active field of oxide TFTs.

The primary objective of the work reporting herein is to explain why the channel mobility of an oxide TFT is typically overestimated when a depletion-mode TFT is assessed. This issue is addressed via simulation using the comprehensive

depletion-mode model [18]. Since p-channel oxide TFT development is of much current interest, the simulation included herein focus exclusively on p-channel oxide TFTs. This required extension the comprehensive depletion-mode model from n-channel to p-channel as order. Even through the focus herein is on p-channel TFTs, the conclusion regards as mobility overestimation due to depletion-mode operation are equally applicable to n-channel TFTs.

The structure of this dissertation is as follows. Chapter 2 reviews pertinent literature, including TFT background, general information on p-type oxides, and prior work relevant to p-channel oxide TFTs. Chapter 3 provides a framework for oxide TFT simulation using the comprehensive depletion-mode model. Chapter 4 presents results of applying the comprehensive depletion-mode model to both p-channel and n-channel depletion-mode TFTs. Finally, Chapter 5 contains conclusions and recommendations for future work.

2 LITERATURE REVIEW

This chapter first provides an overview of thin-film transistor. Then the properties of p-type oxide semiconductors are discussed. Finally, the electrical properties of several p-type oxide TFTs are reviewed.

2.1 Thin-Film Transistors

Thin-film transistors (TFTs) are a class of field-effect transistors (FETs), which are recognized as a key element of a flat panel display (FPD). TFTs were firstly invented in 1934 by J. E. Lilienfeld [12], and were initially developed by P. K. Weimer for the early 1960s [13]. In Weimer's work, a thin film of polycrystalline cadmium sulfide (CdS) was used as the semiconductor, together with an insulator of silicon monoxide (SiO), in what would now be called a staggered, top-gate structure [14], as shown in Fig. 2.1(a).

2.1.1 TFT Device Structures

A TFT is a three-terminal device, composed of a source, drain, and gate electrode, a dielectric (insulator) layer, and a semiconductor (active channel) layer. There are four basic types of TFT structures, as shown in Figure 2.1; staggered, top-gate; staggered, bottom-gate; co-planar, top-gate; and co-planar, bottom-gate.

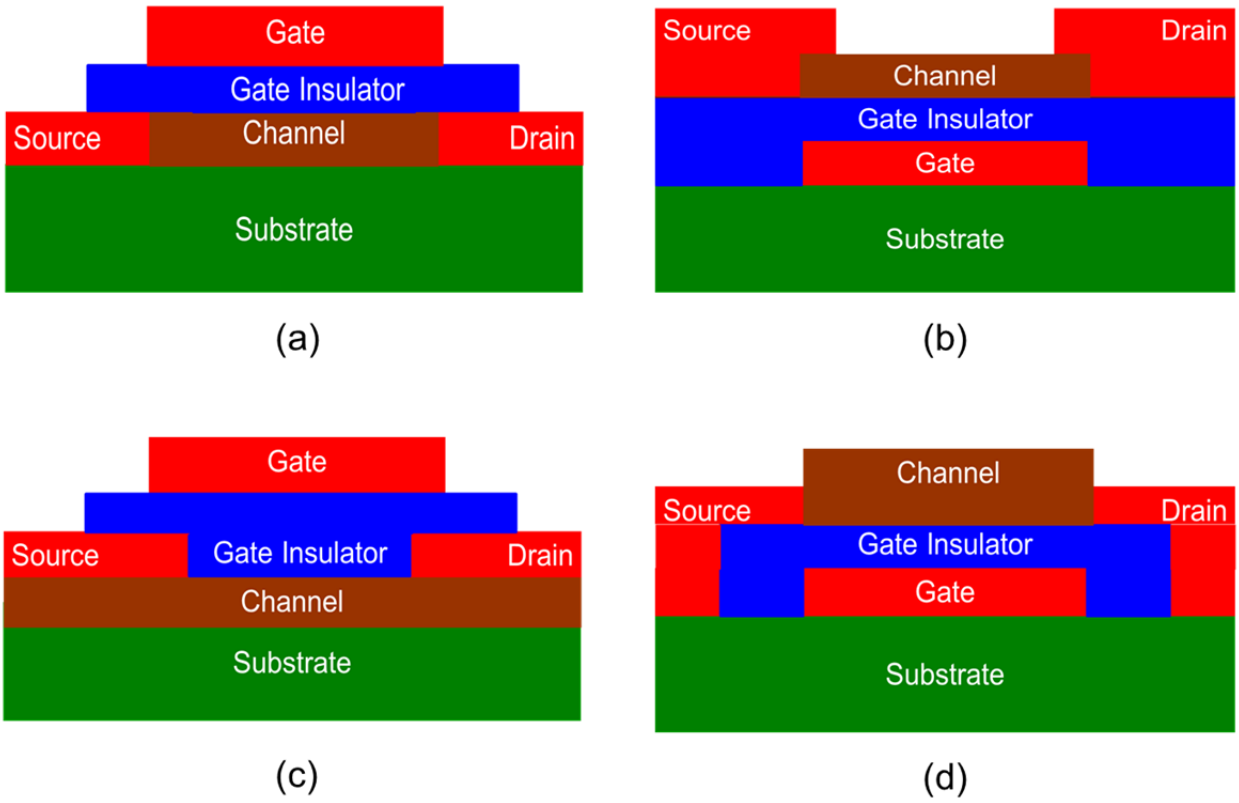


Figure 2.1: Four basic thin-film transistor structures: (a) staggered, top-gate; (b) staggered, bottom-gate; (c) co-planar, top-gate; and (d) co-planar, bottom-gate.

The four basic TFTs structures are defined by the relative positions among source/drain contacts, gate contact, and channel layer. First, the difference between a staggered and a co-planar configuration is whether or not the source/drain contacts and gate contacts are located on the same side of channel layer. If the source/drain and gate contacts are on the opposite side of the channel layer, the device is in a staggered configuration. In contrast, when the source/drain and gate contacts are on the same side of the channel layer, the device is in a co-planar configuration. Second, the difference between top-gate and bottom-gate configuration is the relative location between gate contact and the channel layer. If the gate is on the top of the channel

layer, it is called top-gate configuration; if the gate is on the bottom of the channel layer, it is called a bottom-gate configuration.

2.1.2 TFT Device Operation

Figure 2.2 shows the biasing polarities for a p-channel TFT. Holes are injected from the source, transported through the channel, and extracted at the drain. For a p-channel TFT, a negative gate voltage (V_G) induces positive charge near the channel layer/gate insulator interface by forming a hole accumulation layer. A negative drain voltage (V_D) is applied to transport holes through the accumulation layer from source to drain, assuming that the source is grounded. For the operation of an ideal, long-channel TFT, four operating regimes can be identified: (1) Cut-off, in which no accumulation layer exists to conduct carriers; (2) Linear, pre-pinch-off. When V_D is small enough, $V_D << V_G - V_{ON}$, I_D is linearly proportional to V_D; (3) Non-linear, pre-pinch-off. As V_D increases, I_D is no longer linearly proportional to V_D due to negative feedback, in which the applied drain voltage begins to turn off the channel near the edge of the drain; (4) Post-pinch-off, saturation. When $V_D = V_G - V_{ON}$, I_D is saturated, i.e., I_D is constant due to accumulation layer depletion near the drain. Details of TFT operation and corresponding current – voltage (I -V) models are presented in Chapter 3.

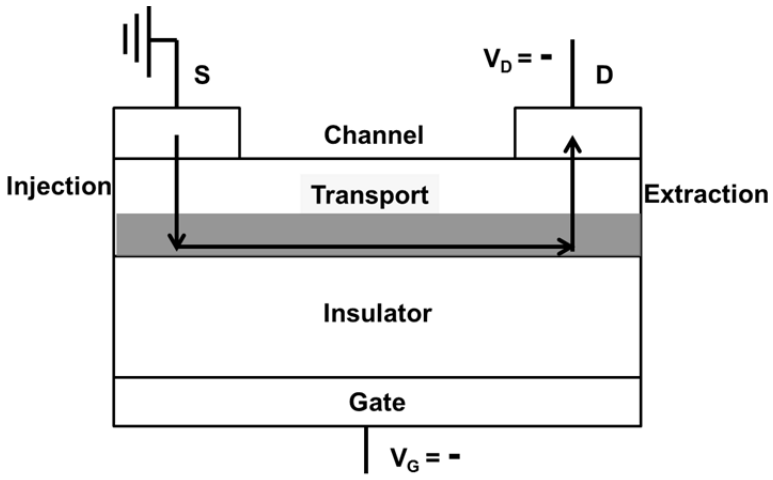


Figure 2.2: Biasing polarity and the hole processes – injection, transport and extraction – giving rise to the drain current flow for an enhancement-mode, p-channel TFT.

Depending on the gate polarity, an applied voltage can either enhance or deplete the concentration of carriers in the channel. Thus, a TFT can be operated either in enhancement-mode or depletion-mode. Figure 2.3 shows transfer curves for an enhancement- and a depletion-mode, p-channel TFT. As shown in Figure 2.3(a), an enhancement-mode TFT is normally off at zero gate bias, such that negligible drain current flows in the channel. In contrast, a depletion-mode TFT is normally on at zero gate bias, as shown in Figure 2.3(b). This means that mobile holes are present in the channel even when no gate voltage is applied. A positive gate voltage must be applied in order to turn off a p-channel depletion-mode TFT. Hence, a depletion-mode TFT consumes more power than an enhancement-mode TFT.

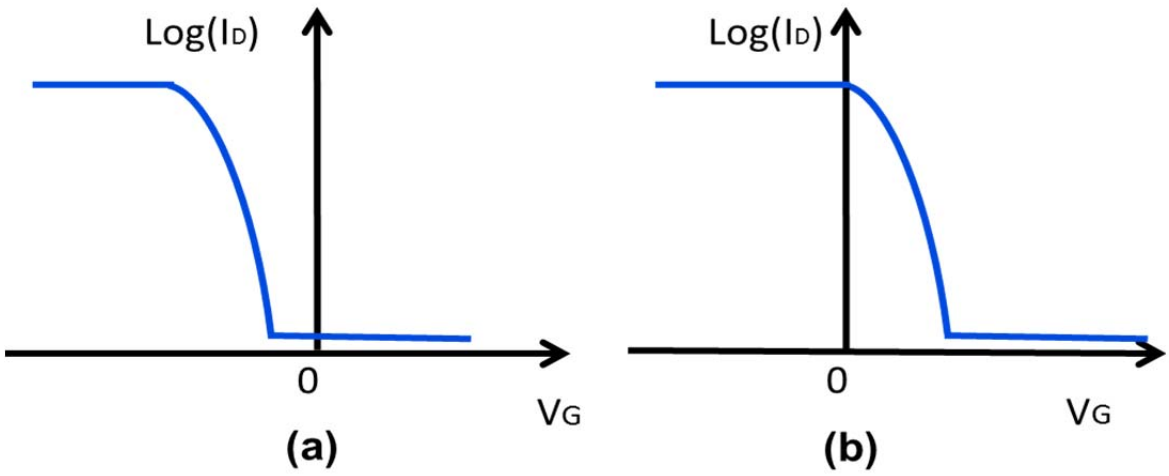
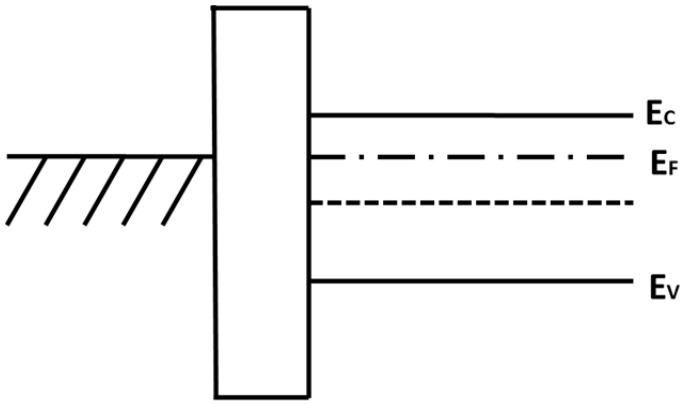


Figure 2.3: Drain current versus gate voltage curve for (a) an enhancement-mode or (b) a depletion-mode, p-channel TFT.

Figure 2.4 illustrates energy band diagrams for a n-channel TFT under various gate bias conditions. Figure 2.4(a) shows an n-channel, depletion-mode TFT with zero gate voltage. Figure 2.4(b) shows an n-channel TFT in depletion. By applying a negative voltage to the gate, mobile electrons in the channel are repelled from the channel, leaving a depletion region near the channel/insulator interface, resulting in an upward band bending of the conduction and valence bands. Figure 2.4(c) shows an n-channel TFT in accumulation. A positive gate voltage is applied so that mobile electrons are attracted to the channel/insulator interface, and an electron accumulation layer is formed. Formation of this electron accumulation layer is consistent with a downward bending of the conduction and valence bands.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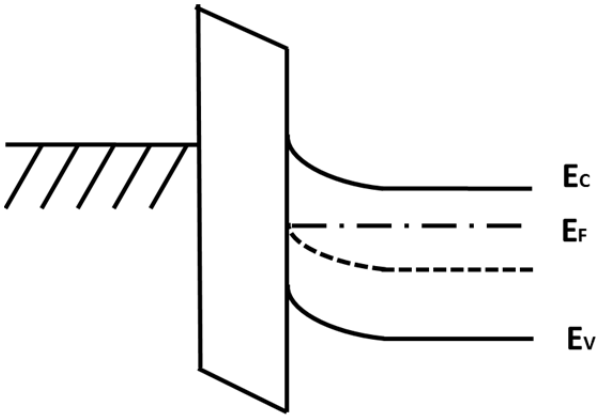
(a)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(b)

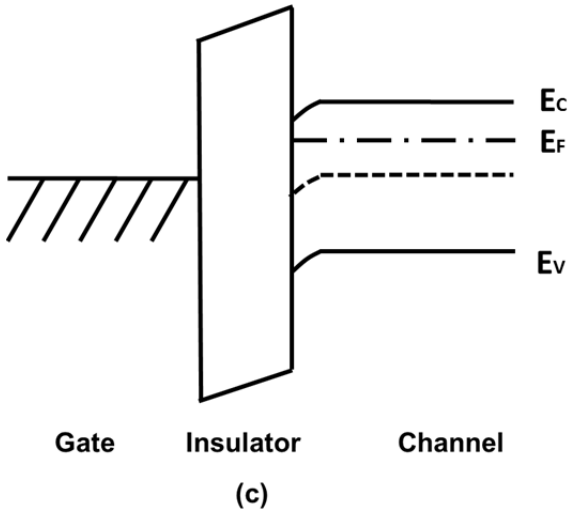

Figure 2.4: Energy band diagrams for an n-channel TFT. (a) Zero gate voltage. (b) A negative gate voltage is applied, so that electrons are depleted from the interface, resulting in upward band bending. (c) A positive gate voltage is applied, so that electrons are accumulated near the interface, resulting in downward band bending.

2.1.3 TFT Device Performance

Four basic figures-of-merit are used to evaluate the performance of a TFT: turn-on voltage (V_{ON}), mobility (μ), drain-current on-to-off ratio (I_D^{ON-OFF}), and subthreshold swing (S). The most basic measurements for extracting these parameters are the low-drain-source-voltage transfer curve and high-drain-source-voltage transfer curve.[19] In the low-drain-source-voltage transfer curve, a very small V_D is applied in order to ensure that the TFT operates in the linear region. From this curve (typically plotted as $\log(I_D)$ - V_G), μ, V_{ON}, and S can be estimated, as shown in Figure 2.5. In the high-drain-source-voltage transfer curve, the condition $V_D/ t_{OX} > \sim 2$ MV/cm, where t_{OX} is the thickness of gate insulator, is maintained in the order to ensure that the TFT operates in the saturation region. I_D^{ON-OFF} is obtained from this measurement.

The turn-on voltage is the voltage at which drain current begins to increase above the gate leakage or noise floor, as shown in Figure 2.5. If a p-channel TFT has a positive V_{ON}, it is identified as a depletion-mode device and requires a positive gate voltage to be applied to turn it off.

From a physical perspective, the magnitude of V_{ON} is determined by the mobile carrier concentration and trap density, which according to the discrete trap model,[5] for a p-channel TFT, is equal to

$$V_{ON} = \frac{q}{C_G}(p_{vo} + p_{to} - n_{to}), \tag{2.1}$$

where q is the elemental electron charge, C_G is the gate capacitance density (F/cm^2), p_{vo} is the equilibrium hole density in valence band (cm^{-2}), p_{to} is the equilibrium donor-like trap density (cm^{-2}), n_{to} is the equilibrium acceptor-like trap density (cm^{-2}). Traps can arise from defects in the channel and/or in the interface.

Mobility (μ) is an important parameter for evaluating the performance of a TFT. A larger mobility value means that the TFT can conduct more current. For an n-channel TFT, the drain current characteristics for a device operation in pre-saturation ($V_D < V_G - V_{ON}$), is equal to [16]

$$I_{D,PRESAT} = \frac{W}{L} C_G \mu \left[(V_G - V_{ON}) V_D - \frac{V_D^2}{2} \right]. \tag{2.2}$$

For a TFT, operating in the linear region ($V_D << V_G - V_{ON}$), Eq. 2.2 can be written as:

$$I_{D,PRESAT} \approx \frac{W}{L} C_G \mu \left(V_G - V_{ON}\right) V_D \,. \tag{2.3}$$

The mobility in linear region ($V_D << V_G - V_{ON}$, or $V_D \to 0$) can be estimated from this expression using the conductance in the linear regime

$$G_D = \left.\frac{dI_D}{dV_D}\right|_{V_D \to 0} = \frac{W}{L} C_G \mu_{LIN} \left(V_G - V_{ON}\right) \,. \tag{2.4}$$

leading to

$$\mu_{LIN} = \frac{G_D}{\frac{W}{L} C_G \left(V_G - V_{ON}\right)}, \tag{2.5}$$

The mobility in saturation regime can be estimated from the saturation region ($V_D > V_G - V_{ON}$) of a TFT characteristics [20]

$$I_{D,SAT} = \frac{W}{2L} C_G \mu_{SAT} \left(V_G - V_{ON}\right)^2 \,, \tag{2.6}$$

leading to

$$\mu_{SAT} = \frac{2}{\frac{W}{L} C_G} \left(\frac{\partial \sqrt{I_{DSAT}}}{\partial V_G} \right)^2 \tag{2.7}$$

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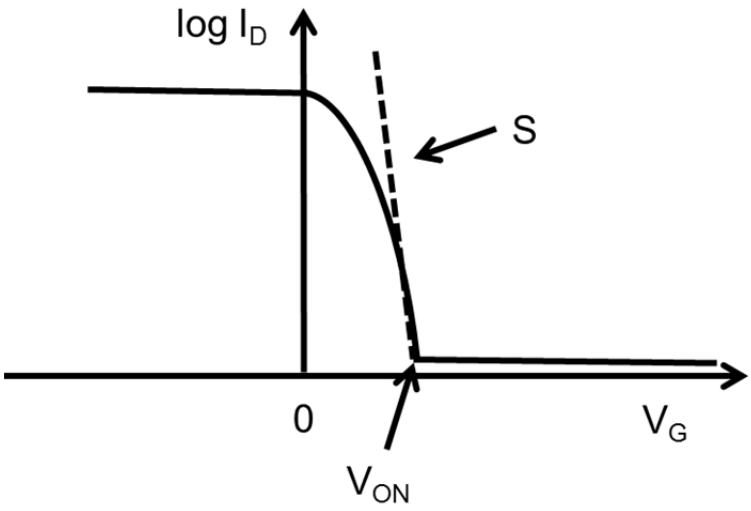


Figure 2.5: The logarithm of the drain current as a function of the gate voltage, log(I_D) - V_G transfer curve of a p-channel depletion-mode TFT.

The drain-current on-to-off ratio (I_D^{ON-OFF}) is an indicator of how well a TFT works as a switch. For achieving a large I_D^{ON-OFF}, a larger on-state drain current (I_D^{ON}) and a smaller off-state drain current (I_D^{OFF}) are required. I_D^{ON-OFF} is affected by many factors. The width-to-length ratio (W/L), drift mobility, interface states, and ohmic contacts are dominant factors for the on-current. The bandgap of channel material and interface states are important for establishing the off-current. These considerations are summarized in Table 2.1.

Subthreshold swing (S) is indicated as a dotted line in Figure 2.5. S is defined to be the amount of change in V_G required to produce a 10× change in I_D, and it is expressed in units of mV per decade.[16] A smaller subthreshold swing is desired, because it is correlated to the interface trap density,

$$S = \ln 10 \bullet \frac{k_B T}{q}\left(1 + \frac{q^2 D_{it}}{C_{OX}}\right) \tag{2.8}$$

where k_B is Boltzmann's constant (J/K), q is the elemental electron charge (C), C_{OX} is the gate oxide capacitance density (F/cm), and D_{it} is the interface trap density, ($cm^{-2}eV^{-1}$). The abruptness of the subthreshold slope depends mainly on the interface trap density. A TFT characterized by a steep subthreshold slope exhibits a more abrupt transition between off- and on-current.

Table 2.1 Main factors influencing the performance of an oxide TFT.

TFT performance parameter	Dominant factor	
Turn-on voltage	Trap concentration Carrier concentration	
Mobility	Interface states Defect states	
Drain-current on-to-off ratio	On-current	W/L Mobility Ohmic contact Interface states
	Off-current	W/L Band gap Interface states
Subthreshold swing	Defect states Interface states	

2.2 p-type Oxide Semiconductors

Although oxide semiconductors, such as IGZO, have made tremendous progress towards commercialization, most reported oxide semiconductors are n-type.[22-25] For p-type oxides, the valence band is mainly formed from oxygen 2p orbitals. This severely limits the hole mobility. Thus, p-type oxides have very low mobility compared to their n-type counterparts.[26] For the realization of a complementary metal oxide semiconductor (CMOS) oxide electronics technology, both n-type and p-type oxides transistors are needed. Thus, the development of p-type oxides and their application has aroused great interest.

It has proven to be difficult to achieve p-type conductivity in a binary oxide such as zinc oxide (ZnO) due to self-compensation. [27] Delafossite $CuMO_2$ thin films (M is a trivalent cation, such as Al, Ga, In, Cr, Y, Sc, La, etc.) have been investigated as channel layers due to their promising p-type conductivity.[28-31] One of the few non-delafossite p-type oxides, $SrCu_2O_2$ thin films were deposited by pulsed laser deposition (PLD) technique.[29] More recently, cuprous oxide (Cu_2O) and tin monoxide (SnO) have been explored as p-type channel layers due to the nature of their band structure.[32] This review of prior work on p-channel oxide TFTs mainly focuses on the use of Cu_2O or SnO as channel layers.

2.3 Prior work on Cu_2O and SnO Thin-film Transistors

2.3.1 Cu_2O TFTs

Cu_2O is a well-known p-type oxide with a direct band gap of 2.0-2.6 eV.[33] It exhibits a high hole Hall mobility exceeding 100 $cm^2V^{-1}s^{-1}$.[34] The p-type nature of

Cu_2O has been mainly attributed to negatively charged Cu vacancies, which introduce an acceptor level above the valence band.[35] Since 2008, several Cu_2O TFTs have been reported. [36-43]

Matsuzaki *et al.* demonstrated top-gate, p-channel TFTs using the Cu_2O epitaxial films as the channel layers.[36] Although the field-effect mobility and drain current on-to-off ratio were small (~0.26 $cm^2V^{-1}s^{-1}$ and ~6, respectively), Cu_2O epitaxial films exhibited high hole Hall mobilities up to 90 $cm^2V^{-1}s^{-1}$ at room temperature (RT) with a reported hole concentration of 10^{14} cm^{-3}. Before 2008, the highest hole Hall mobility reported was ~30 $cm^2V^{-1}s^{-1}$ for an epitaxial film. In this report, they used a (110) MgO substrate and optimized their growth to produce epitaxial films with high hole Hall mobilities. The Cu_2O channel layer and Al_2O_3 gate insulator were deposited by PLD at room temperature. These Cu_2O TFTs operated in depletion-mode as evidence from the fact that V_{ON} is positive, as determined from their reported transfer curves.

Sung *et al.* investigated bottom-gate CuO TFTs by rf magnetron sputtering. Their devices exhibited a field-effect mobility of 0.4 $cm^2V^{-1}s^{-1}$ and I_D^{ON-OFF} of ~10^4, the maximum I_D^{ON-OFF} reported up to the time of their publication.[37] CuO channel layers were fabricated by annealing Cu_2O thin films deposited by rf magnetron sputtering above 200 °C in air. Annealing transformed the as-deposited Cu_2O phase to a CuO phase. Their TFT did not exhibit clear pinch-off behavior, although it had a high I_D^{ON-OFF}. It is asserted that their CuO TFT operated as a p-channel, enhancement-mode TFT. However, since $V_{ON} > 10$ V, their CuO TFT was clearly a depletion-mode TFT.

In 2010, Zou *et al.* reported a polycrystalline Cu_2O TFT with the highest saturation mobility reported to date of ~4.3 $cm^2V^{-1}s^{-1}$.[38] The Cu_2O channel layer films were deposited by PLD at a substrate temperature of 500 °C. Top-gate TFTs were fabricated by using a HfON (high-k gate dielectric, permittivity of ~24) as the gate insulator. Pt was used as the source/drain contact. These p-channel Cu_2O TFTs had a low threshold voltage of -0.8 V, a high I_D^{ON-OFF} of 3×10^6, a large saturation mobility of 4.3 $cm^2V^{-1}s^{-1}$, and a small subthreshold swing of 0.18 V/decade. A Hall mobility of ~10^7 $cm^2V^{-1}s^{-1}$ was reported for a 400-nm-thick polycrystalline Cu_2O film deposited at 400 °C. However, their channel layers were deposited at 500, 600, 700 °C, and their saturation mobilities were extracted to be 4.3, 2.1, 0.7 $cm^2V^{-1}s^{-1}$, respectively. They attributed their saturation mobility as being lower than their Hall mobility as due to traps, but they do not provide the Hall mobility of the thick film deposited at 500 °C in their report.

Also in 2010, Fortunato *et al.* demonstrated p-channel Cu_2O TFTs by rf magnetron sputtering at room temperature, resulting a field-effect mobility of 3.9 $cm^2V^{-1}s^{-1}$.[39] However, this required post-deposition annealing at 200 °C for 10 hours. The threshold voltage V_T = -12.0 V, and V_{ON} > 6 V, so that their device operated as a depletion-mode TFT.

The improvement of p-channel TFT performance was rapid. One year later, in 2011, Zou *et al.* improved the subthreshold swing to 137 mV/decade by fabricating Cu_2O TFTs with a HfO_2/SiO_2 stacked gate dielectric.[40] They were the first to report on the bias stress stability of Cu_2O TFTs. The threshold voltage shifts 1.4 V after a gate-bias stress at 10 V for 3600 sec. The saturation mobility and I_D^{ON-OFF} were 2.7

$cm^2V^{-1}s^{-1}$ and 1.5×10^6, respectively. They asserted that the stacked dielectric had significantly improved the interface properties as evidenced by a lower S, and ascribed this to a lower interface trap state density. However, a higher gate capacitance can reduce S as evident from $S=\ln10\times K_BT/q\times(1+C_{IT}/C_G)$. Their Cu_2O TFT exhibited a high gate leakage current.

In 2012, Yao *et al.* reported a nanocrystalline Cu_2O TFT on a flexible substrate.[41] Their devices exhibited a field-effect mobility of 2.4 $cm^2V^{-1}s^{-1}$, and I_D^{ON-OFF} of 3.96×10^4. Due to the requirement of high processing temperature (200-700°C) in previous work [36-40], Cu_2O TFTs fabricated on plastic substrates at room temperature had not been realized. The Cu_2O channel layer was deposited by rf magnetron sputtering at room temperature, without post-deposition annealing. They claimed their p-channel TFTs were enhancement-mode However, these Cu_2O TFTs operated in depletion-mode as evidence from the fact that $V_{ON} = 4$ V, as determined from the reported transfer curves.

Also in 2012, Nam *et al.* investigated the effect of channel layer thickness on the structural, optical, and electrical characteristics of Cu_2O TFTs.[42] Cu_2O channel layers of 15, 45, 65, 85, and 155 nm thickness were deposited by rf magnetron sputtering using Cu target. The root mean square (RMS) roughness was analyzed by atomic force microscopy (AFM), to be 2.94, 4.74 5.23, 6.09 and 10.9 nm, respectively. The Cu_2O TFTs with a 15 nm-thick channel layer exhibited very small on-currents. They ascribed this to the non-continuous/inhomogeneous nature of their Cu_2O thin film. Their Cu_2O TFT with a 45 nm-thick channel layer exhibited a low

field-effect mobility of 0.06 $cm^2V^{-1}s^{-1}$. The turn-on voltage $V_{ON} > 4$ V, indicates that their device operated as a depletion-mode TFT.

In 2013, Kim *et al.* demonstrated a solution-processed Cu_2O film as the channel layer of p-channel TFT.[43] Their device exhibited a field-effect mobility of 0.16 $cm^2V^{-1}s^{-1}$ and I_D^{ON-OFF} of 1×10^2. They reported a Hall mobility for a 100 nm-thick Cu_2O thin film to be 18.9 $cm^2V^{-1}s^{-1}$. The turn-on voltage was more than 40 V, indicating that their device operated as a depletion-mode TFT.

2.3.2 SnO TFTs

SnO has indirect band gap with contributions from Sn 5s and O 2p orbitals near the valence band maximum (VBM) and Sn 5p orbitals near the conduction band minimum (CBM).[44] The origin of p-type conductivity of SnO is usually attributed to a Sn vacancy and an O interstitial.[45] Since 2008, several SnO TFTs have been reported.[44, 46-54]

In 2008, Ogo *et al.* demonstrated top-gate, p-channel TFTs using the SnO epitaxial films as the channel layer.[44] SnO TFTs exhibited field-effect mobility, I_D^{ON-OFF} and threshold voltage, of 1.3 $cm^2V^{-1}s^{-1}$, 1×10^2, and 4.8 V, respectively. This was the first time to demonstration of a SnO p-channel oxide TFT with reasonable performance. However, the high-quality epitaxial SnO films were grown at a high-temperature of 575°C. Since $V_{ON} > 15$ V in reported transfer curves, their SnO TFTs operate as p-channel, depletion-mode devices.

Also in 2008, Ou *et al.* reported an amorphous SnO_2 TFT fabricated by reactive evaporation.[46] Undoped SnO_2 is n-type in nature with a wide optical band gap of

3.6 eV.[47] The existence of p-type SnO_2 was reported in 2004, although this report is controversial.[48] The origin of p-type conductivity was ascribed to the use of reactive evaporation and prolonged annealing 1 hour at 100°C in an oxygen-rich environment. Their p-type SnO_2 TFT exhibited a low field-effect mobility of 0.011 $cm^2V^{-1}s^{-1}$, much smaller than that reported for SnO TFTs, an $I_D^{ON-OFF} = 10^3$, and a turn-on voltage of 80 V, indication of strongly depletion-mode behavior, when the transfer curve is measured at V_D = -80 V.

In 2009, Ogo *et al*. reported on the electrical properties and electronic structures of SnO films, top-gate, p-channel SnO TFTs, and TFT simulations.[49] Their device exhibited similar performance to that reported in 2008.[44] They calculated from simulation by taking tail-like trap states into consideration indicated that the subgap hole trap density in the SnO channel is greater than 10^{19} cm^{-3}, which limits the mobility and subthreshold swing of their TFTs.

In 2010, Lee *et al.* demonstrated p-channel SnO TFTs fabricated by thermal evaporation using SnO powder.[50] They reported a Hall mobility for a 100 nm-thick SnO thin film to be 2.83 $cm^2V^{-1}s^{-1}$, and a hole concentration of 10^{17} cm^{-3}. Their device exhibited a low field-effect mobility of 4×10^{-5} $cm^2V^{-1}s^{-1}$, I_D^{ON-OFF} of 1×10^2, and V_{ON} = -5 V, indicating that their SnO TFTs operate as p-channel, enhancement-mode devices.

Also in 2010, Yabuta *et al.* reported p-channel TFTs in which SnO-SnO_2 channel layers were deposited on glass by rf sputtering and subsequent annealing at 300 °C.[51] It is asserted that precise control of the oxygen content is required

because tin oxide can change from p-type (Sn^{2+} in SnO) to n-type (Sn^{4+} in SnO_2) with excess oxygen. They fabricated n-type SnO_2 channel layer by oxidation of a SnO film, resulting in a complementary circuit. Their p-channel TFTs exhibited a field-effect mobility of 0.24 $cm^2V^{-1}s^{-1}$, $I_D^{ON-OFF} = 10^2$, and a turn-on voltage of 60 V, indication of strongly depletion-mode behavior.

In 2010, Liang *et al.* investigated a p-channel SnO TFT fabricated by electron beam evaporation using rapid thermal annealing at 400 °C.[52] Their devices exhibited a field-effect mobility, I_D^{ON-OFF}, and subthreshold swing of 0.87 $cm^2V^{-1}s^{-1}$, ~200, and 11 V/decade, respectively. They asserted that a high annealing temperature improves SnO crystallinity, reduces the trap densities, and improves the hole mobility. However, the large S of 11 V/decade indicates a large density of interface trap states, which contradicting their assertion. They claimed their p-channel TFTs were enhancement-mode, although $V_{ON} = 1$ V.

In 2010, Fortunato *et al.* demonstrated p-channel SnO_X TFTs by reactive rf magnetron sputtering at room temperature, resulting a field-effect mobility of 1.2 $cm^2V^{-1}s^{-1}$ and I_D^{ON-OFF} of 10^3.[53] They asserted that their as-deposited SnO films exhibited n-type conductivity, but then exhibited p-type characteristics after annealing at 200 °C at an oxygen partial pressure (O_{PP}) of 5% ~ 15%. Since $V_{ON} > 30$ V, their SnO_X TFT was clearly a depletion-mode TFT.

In 2011, Nomura *et al.* [54] reported an ambipolar SnO TFT. They found that their ambipolar device with a 15.4 nm-thick channel layer operated both in p-accumulation and in inversion with p- and n-type saturation mobilities of 0.81 cm^2V^{-}

$^{1}s^{-1}$ and 4×10^{-4} $cm^2V^{-1}s^{-1}$, respectively. This was the first demonstration of an oxide TFT-based complementary-like inverter using a single channel material. However, they also concluded that inversion originated from the formation of a thin SnO_2 layer by the oxidation of SnO.

In 2012, Liang *et al.* demonstrated p-channel yttrium-doped SnO TFTs.[55] It is reported that the turn-on voltage shifts towards in a positive direction as more yttrium is introduced. Their 0.8 at% Y-doped SnO TFTs exhibited a small saturation mobility of 3.6×10^{-3} $cm^2V^{-1}s^{-1}$, an $I_D^{ON-OFF} = 400$. Since $V_{ON} = 14$ V, their SnO TFTs operate as p-channel, depletion-mode devices.

In 2013, Caraveo-Frescas *et al.* reported a SnO TFT with the highest field-effect mobility reported to date of ~6.75 $cm^2V^{-1}s^{-1}$.[56] They asserted that a SnO thin film with a hole Hall mobility of 18.71 $cm^2V^{-1}s^{-1}$ and a SnO TFT with a field-effect mobility of 6.75 $cm^2V^{-1}s^{-1}$ were obtained by carefully controlling the processing conditions. Their device exhibited I_D^{ON-OFF} of 6×10^3, and a turn-on voltage of 20 V, indicative of strongly depletion-mode behavior.

In conclusion, most of reported p-channel oxide TFTs operate as depletion-mode TFTs, as summarized in Tables 2.2 and 2.3.

Table 2.2. Summary of parameters reported to the performance Cu_2O TFTs.

Channel material	Mobility (cm^2/Vs)	Mode	Channel thickness (nm)	Gate insulator and thickness	Carrier density (cm^{-3})	Year	Reference
Cu_2O	μ_{FE}= 0.26	Depletion	100	Al_2O_X (150 nm)	--	2008	36
CuO	μ_{FE}= 0.4	Depletion	75	SiO_2 (100 nm)	--	2010	37
Cu_2O	μ_{sat}= 4.3	Depletion	120	SiO_2-HfON (20 nm)	--	2010	38
Cu_2O	μ_{FE}= 3.9	Depletion	40	ATO (220 nm)	3.7×10^{15}	2010	39
Cu_2O	μ_{sat}= 2.7	Depletion	40	SiO_2 (100 nm)/ HfO_2 (10 nm)	--	2011	40
Cu_2O	μ_{sat}= 0.43	Depletion	40	SiO_2 (110 nm)	--	2011	40
Cu_2O	μ_{FE}= 2.4	Depletion	--	AIN (100 nm)	--	2012	41
Cu_2O	μ_{FE}= 0.06	Depletion	45	SiO_2 (100 nm)	10^{16}	2012	42
Cu_XO	μ_{FE}= 0.16	Depletion	--	SiO_2	--	2013	43

Table 2.3. Summary of parameters reported to the performance SnO TFTs.

Channel material	Mobility (cm^2/Vs)	Mode	Channel thickness (nm)	Gate insulator and thickness	Carrier density (cm^{-3})	Year	Reference
SnO	$\mu_{FE} = 1.3$ $\mu_{sat} = 0.7$	Depletion	20	Al_2O_X (210 nm)	$>10^{17}$	2008	44
SnO_X	$\mu_{FE} = 1.1\times10^{-2}$	Depletion	7.5	SiO_2 (100 nm)	--	2008	46
SnO	$\mu_{FE} = 4\times10^{-5}$	Enhancement	100	SiO_2 (2 μm)	$>10^{17}$	2010	50
SnO	$\mu_{FE}= 0.24$	Depletion	50	SiN_X (500 nm)	10^{16}~10^{18}	2010	51
SnO	$\mu_{lin}= 0.87$ $\mu_{sat}= 0.46$	Enhancement	100	SiO_2 (190 nm)	--	2010	52
SnO	$\mu_{FE} = 1.1$~1.2	Depletion	30	ATO (220 nm)	5~8×10^{17} (N_H)	2010	53
SnO	$\mu_{lin}= 0.48$ $\mu_{sat}= 0.78$	Enhancement	15.4	SiO_2 /Y_2O_3 (15 nm)	--	2011	54
SnO	$\mu_{sat}= 4.6$	--	--	ATO	--	2011	57
SnO	$\mu_{FE}= 1.24$	Depletion	40	Cellulose	--	2012	58
SnO (Y doped)	$\mu_{sat}=3.6\times10^{-3}$ (Y=0.8)	Depletion	50	SiO_2 (190 nm)	4.7×10^{16} (N_H)	2012	55
SnO	$\mu_{FE}= 6.75$	Depletion	15	HfO_2 (220 nm)	2.18×10^{17}	2013	56

3 THIN-FILM TRANSISTOR MDDELING

In this chapter, the square-law model and the comprehensive depletion-mode model are derived. These models are used to simulate the current-voltage characteristics of thin-film transistors. Moreover, mobilities may be extracted from these models.

3.1 Square-law model

The bottom-gate, n-channel thin-film transistor under consideration is assumed to be a long-channel device, as shown in Fig.3.1. From Fig.3.1, the source is grounded, V_D is applied to the drain, and V_G is applied to the gate. The potential in the channel varies from 0 V at the source to V_D at the drain.

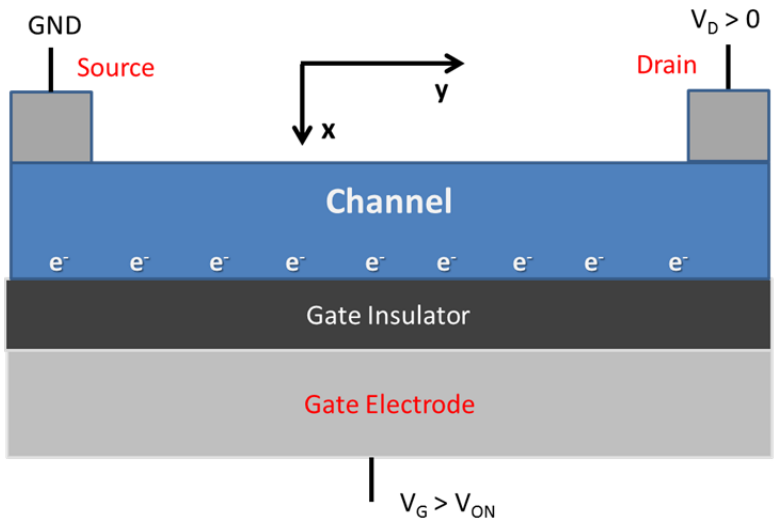


Figure 3.1 Simplified cross section of a thin-film transistor.

A quantitative analysis of the device physics of TFT behavior begins with the continuity equation,

$$\frac{\partial n}{\partial t} = G - R + \frac{1}{q}\vec{\nabla} \bullet \vec{J}_n \ , \qquad (3.1)$$

where n, G, R, q, and J_n refer to the electron concentration, generation rate, recombination rate, elementary charge, and current density of electrons in the channel accumulation layer, respectively. If the assumptions of steady-state and no generation-recombination are applied and if channel layer conduction can be reduced to two-dimensions, the continuity equation simplifies to

$$\frac{\partial J_n(x,y)}{\partial x \partial y} = 0 \ . \qquad (3.2)$$

This means that $J_n(x,y)$ is constant. Moreover, the drain current, $I_D(x,y)$, is constant across the channel. Although $J_n(x,y)$ typically involves components of drift and diffusion current, the diffusion component is initially neglected, so that $J_n(x,y)$ can be expressed as

$$J_n(x,y) = qn(x,y)v(x,y) \ , \qquad (3.3)$$

where $n(x,y)$ is the electron concentration in the channel and $v(x,y)$ is the electron velocity in the channel. One-dimensionalized, Eq. (3-3) becomes

$$J_D(y) = qn(y)v(y) \, , \qquad (3.4)$$

where $J_D(y)$ is the drain current density which can be expressed as the drain current divided by the channel cross-sectional area,

$$J_D(y) = \frac{I_D(y)}{Zh} \ , \tag{3.5}$$

where Z is the channel width and h is the channel thickness. Recognizing that $qhn(y)$ is equal to the electron charge density along the channel, $Q_n(y)$,

$$n(y) = \frac{Q_n(y)}{qh} \ . \tag{3.6}$$

Substituting Eqs. (3-5) and (3-6) into Eq. (3-4) and rearranging leads to

$$I_D(y) = ZQ_n(y)v(y) \ , \tag{3.7}$$

Since the drain current is constant across the channel, Eq. (3-7) can be integrated across the length of the channel (L), finally obtaining,

$$I_D = \frac{Z}{L}\int_0^L Q_n(y)v(y)dy \ . \tag{3.8}$$

This is a general equation used to derive drift-based current-voltage characteristics for field-effect transistors (FETs), and is applicable to all classes of FETs. According to Eq. (3-8), the charge density $Q_n(y)$ and the electron velocity $v(x, y)$ in channel must be specified in order to perform the specific integration.

The gradual channel approximation (GCA) may now be introduced.[59] In a two-dimensional channel, there are two electric field components involving the longitudinal (along the channel direction in the y direction) and transverse (perpendicular to the channel, in the x direction) electric field. The gradual channel

approximation asserts that the rate of change of the longitudinal electric field is much less than the rate of change of the transverse electric field. This approximation allows the two-dimensional electric field problem to be simplified into the one-dimensional electric field problems, involving the gate-induced transverse electric field and the drain-induced longitudinal electric field. The gradual channel approximation is only valid for long-channel devices operating in the pre-pinch-off regime.

Applying the gradual channel approximation and assuming that the applied electric field is small enough that linear transport holds, the velocity is proportional to the electric field $\xi(y)$,

$$v(y) = \mu(y) \bullet \xi(y), \tag{3.9}$$

where $\mu(y)$ is the proportional constant relating the velocity to the electric field, and is defined as the mobility. Recognizing the electric field $\xi(y)$ can be expressed as,

$$\xi(y) = -\frac{d\Delta\psi(y)}{dy}, \tag{3.10}$$

where $\Delta\psi(y)$ is the channel potential along the channel due to the applied drain voltage, V_D. For obtaining the charge density $Q_n(y)$, Gauss' law is used in the channel layer,

$$Q_n(y) = -\varepsilon_S \xi_S(y), \tag{3.11}$$

where ε_S is the channel layer dielectric constant and $\xi_S(y)$ is the electric field along the channel. Because charge due to channel/gate insulator interface states is neglected, the electrostatics boundary condition at the interface can be expressed as

$$\varepsilon_{OX}\xi_{OX}(y)-\varepsilon_S\xi_S(y)=0, \tag{3.12}$$

where ε_{OX} is the gate insulator dielectric constant and $\xi_{OX}(y)$ is the gate insulator electric field along the channel. Additionally, according to the Kirchhoff's Voltage Law (KVL), the voltage applied to the gate and drain are dropped across either the gate insulator or the channel layer,

$$V_G-V_{FB}=V_{OX}(y)-\Delta\psi(y), \tag{3.13}$$

where V_G, V_{FB}, and $V_{OX}(y)$ refer to gate voltage, flatband voltage, and the voltage across the gate insulator along the channel. For an accumulation-mode TFT, V_{FB} is equal to the turn-on voltage, V_{ON}. Moreover, since $\varepsilon_{OX}\xi_{OX}(y)=C_{OX}V_{OX}(y)$, where C_{OX} is gate insulator capacitance density, then, substituting Eq. (3-12) and (3-13) can be substituted into Eq. (3-11), leading to

$$Q_n(y)=-\left[V_G-V_{ON}-\Delta\psi(y)\right]C_{OX}. \tag{3.14}$$

Then, substituting Eq. (3-9) and (3-14) into Eq. (3-8), lead to

$$I_D=\frac{Z}{L}\mu C_{OX}\int_0^{V_D}\left[V_G-V_{ON}-\Delta\psi(y)\right]d\Delta\psi. \tag{3.15}$$

Finally, performing the integration, rearranging Eq. (3-15), and assuming that the mobility is constant across the channel,

$$I_D = \frac{ZC_G\mu}{L}[(V_G - V_{ON})V_D - \frac{V_D^2}{2}] \qquad (3.16)$$

Because the gradual channel approximation is only valid for device operation in the pre-pinch-off regime ($V_G > V_{ON}$, $V_D < V_G - V_{ON}$), Eq. (3.16) is only valid for pre-pinch-off regime. For saturation, when the channel is pinched off on the drain side, $V_D = V_{D,SAT} = V_G - V_{ON}$. Thus, the saturation drain current is given by,

$$I_D = \frac{ZC_G\mu}{2L}(V_G - V_{ON})^2 \qquad (3.17)$$

Equations (3.16) and (3.17) constitute the square-law model, as summarized in Table 3.1.

Table 3.1. A summary of n-channel TFT drain current equations and voltage constraint equations for the square-law model.

Regime of operation	**Drain Current Equation**	**Voltage Constraint Equation**
Cut-off	$I_{OFF} = 0$	$V_G < V_{ON}$
Pre-saturation	$I_{D,PRESAT} = \frac{W}{L}\mu C_G\left[(V_G - V_{ON})V_D - \frac{V_D^2}{2}\right]$	$V_G \geq V_{ON}; V_D < V_{DSAT}$
Saturation	$I_{D,SAT} = \frac{W}{2L}\mu C_G(V_G - V_{ON})^2$	$V_G \geq V_{ON}; V_D \geq V_{DSAT}$

3.2 Comparison of enhancement- and depletion-mode TFTs

In this section, a complete description of depletion-mode TFTs are present by comparing enhancement- and depletion-mode TFTs via transfer curves and energy band diagrams.

As typically defined, the gate turn-on (V_{ON}) and threshold voltage (V_T) of a depletion-mode TFT are negative (positive) for an n-channel (p-channel) TFT. This means that mobile carriers (electrons or holes) are present in the channel even when no gate voltage is applied. Depending on the polarity, an applied voltage can either enhance or deplete the concentration of carriers in the channel of a depletion-mode TFT. When the carrier concentration is enhanced by the applied gate voltage, these additional carriers are induced into an accumulation layer existing in close physical proximity to the gate insulator.

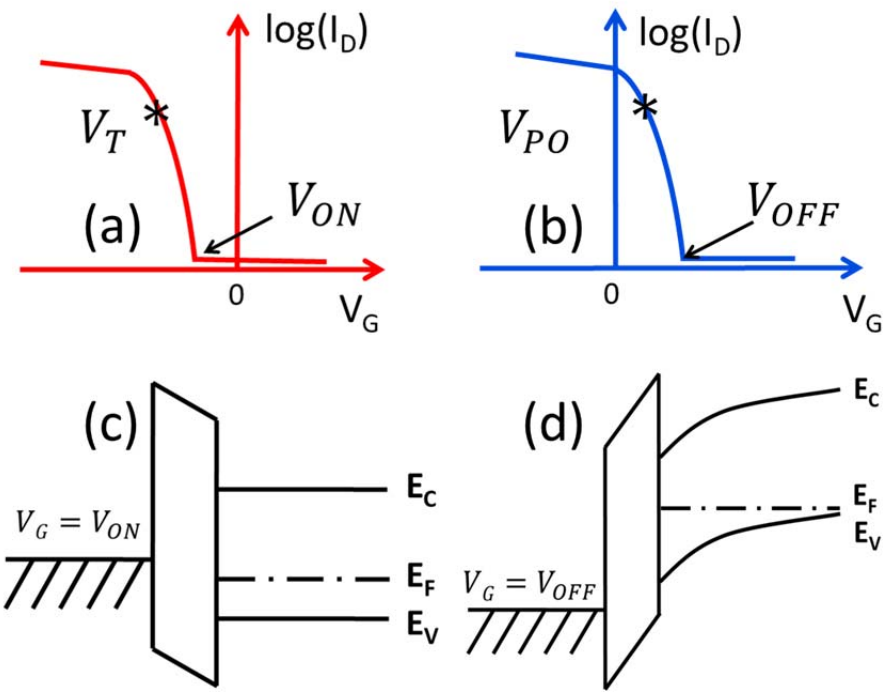


Fig. 3.2 Transfer characteristics for a p-channel (a) enhancement-mode, and (b) depletion-mode TFT, and corresponding energy band diagrams illustrating that (c) V_{ON} corresponds to the flat band voltage for an enhancement-mode TFT, while (d) V_{OFF} corresponds to the applied gate voltage required to fully deplete the channel of a depletion-mode TFT.

Transfer curves and corresponding energy band diagrams distinguishing between enhancement- and depletion-mode TFT behaviors are illustrated in Fig. 3.2. The enhancement-mode case (Fig. 3.2(a) and 3.2(c)) is the familiar one in which the turn-on voltage (V_{ON}) corresponds to the onset of current as measured on a log (I_D) - V_G transfer curve while the threshold voltage (V_T) is indicative of the flow of appreciable TFT current as measured in the context of an $I_D - V_D$ output curve, an $I_D - V_G$ (linear scale) transfer curve, and an $\sqrt{I_D} - V_G$ (in saturation regime) transfer curve. As noted in Fig. 3.2(c), V_{ON} is the applied gate voltage corresponding to flat band in the channel layer. Additionally, in an enhancement-mode TFT, subthreshold current flow occurs when the channel is weakly accumulated and interface trapping of

carriers is at its maximum effectiveness. Enhancement-mode TFT operation is usually well described using the square-law model. The square-law model in section 3.1 can be modified for a p-channel, enhancement-mode TFT, as summarized in Table 3.2.

Depletion-mode TFT operation is distinctly different than that of enhancement-mode TFT operation. For example, Fig. 3.2 (d) reveals that the log (I_D) - V_G onset voltage corresponds to full depletion of the channel, rather than flat band (Fig. 3.2 (c)) as is the case for enhancement-mode operation. Thus, we propose to denote this depletion-mode TFT log (I_D) - V_G onset voltage as a turn-off voltage (V_{OFF}) in order to distinguish it from V_{ON}. Additionally, the onset of current flow in an $I_D - V_D$ output curve is most accurately described as a pinch-off voltage (V_{PO}) for a depletion-mode TFT. (V_{PO} can be measured in an $I_D - V_G$ transfer curve of linear regime, and an $\sqrt{I_D} - V_G$ transfer curve of saturation regime. V_{PO} in a depletion-mode TFT is the counterpart of V_T in an enhancement-mode TFT.). Drain current flowing between an applied gate voltage of V_{OFF} and V_{PO} corresponds to subpinchoff associated with a situation in which the channel is weakly depleted.

As shown in Fig. 3.2(a) and Table 3.2, V_T in an enhancement-mode TFT is adopted in modified square-law model by considering the inevitable subthrehold region in measured log (I_D) - V_G transfer curve. When the log (I_D) - V_G transfer curve has perpendicular subthrehold slope, V_T is equal to V_{ON} in such an ideal case. Similarly available in a depletion-mode TFT, it is necessary to elaborate the subpinchoff region between V_{OFF} and V_{PO} in log (I_D) - V_G transfer curve, as derived in Section 3.4.

Table 3.2 A summary of p-channel, enhancement-mode TFT drain current equations and voltage constraint equations for the modified square-law model. The differences between the square-law model in Section3.1 and the modified square law model in Section 3.3 are marked in green.

Regime of operation	**Drain Current Equation**	**Voltage Constraint Equation**
Cut-off	$I_{OFF} = 0$	$V_G < V_T$
Pre-saturation	$I_{D,PRESAT} = \frac{W}{L}\mu C_G\left[-(V_G - V_T)V_D + \frac{V_D^2}{2}\right]$	$V_G \le V_T < 0$ $V_D < V_{DSAT}$
Saturation	$I_{D,SAT} = -\frac{W}{2L}\mu C_G (V_G - V_T)^2$	$V_G \le V_T < 0$ $V_D \ge V_{DSAT}$

Model parameters	Equation
Threshold voltage	$V_T = \frac{qp_{to}h}{2C_S} + \frac{qp_{to}h}{C_G}$ p_{to} (empty trap density at zero bias)
Saturation voltage	$V_{DSAT} = V_G - V_T$

3.3 Comprehensive depletion-mode model

The square-law model works quite well for the modeling of an enhancement-mode TFT. However, the square-law model is not appropriate for depletion-mode TFT assessment. Rather, the comprehensive depletion-mode model [18] is a more appropriate analytic model for describing depletion-mode TFT I-V characteristics. A modified comprehensive depletion-mode model is developed in this section.

3.3.1 Development of a modified comprehensive depletion-mode model

A summary of n-channel TFT drain current and voltage constraint equations for the comprehensive depletion-mode model as originally proposed by D. Hong [18, 63] is given in Table 3.3. Then a modified comprehensive depletion-mode model is shown in Table 3.4.

Table 3.3 A summary of n-channel TFT drain current equations and voltage constraint equations for the comprehensive depletion-mode TFT model as originally proposed by D. Hong [18,63].

Regime of operation	**Drain Current Equation**	**Voltage Constraint Equations**
DEPL	$I_{D,PRESAT}^{DEP} = \frac{W}{L}\sigma h\{(1+\frac{C_S}{C_G})V_D - \frac{2}{3}V_P[(\frac{C_S^2}{C_G^2}+\frac{V_G}{V_P})^{\frac{3}{2}} - (\frac{C_S^2}{C_G^2}+\frac{V_{GD}}{V_P}$	$V_{ON} < V_G < 0$ $V_D < V_{DSAT}$
DEPL-SAT	$I_{D,SAT}^{DEP} = \frac{W}{L}\sigma h\{(1+\frac{C_S}{C_G})V_{DSAT} - \frac{2}{3}V_P[(\frac{C_S^2}{C_G^2}+\frac{V_G}{V_P})^{\frac{3}{2}} - (\frac{C_S^2}{C_G^2}+\frac{V_{ON}}{V_P}$	$V_{ON} < V_G < 0$ $V_D \geq V_{DSAT}$

ACC	$I_{D,PRESAT}^{ACC} = \frac{W}{L}\left[\mu C_G (V_G V_D - \frac{V_D^2}{2}) + \sigma h V_D\right]$	$V_G \geq 0$ $V_D < V_G$
ACC-DEP	$I_{D,PRESAT}^{ACC-DEP} = \frac{W}{2L}\mu C_G V_G^2 + \frac{W}{L}\sigma h V_G +$ $\frac{W}{L}\sigma h\{(1+\frac{C_S}{C_G})(V_D - V_G) - \frac{2}{3}V_P[(\frac{C_S^3}{C_G^3} - (\frac{C_S^2}{C_G^2} + \frac{V_{GD}}{V_P})^{\frac{3}{2}}]\}$	$V_G \geq 0$ $V_G \leq V_D < V_{DSAT}$
ACC-SAT	$I_{D,SAT}^{ACC} = \frac{W}{2L}\mu C_G V_G^2 + \frac{W}{L}\sigma h V_G +$ $\frac{W}{L}\sigma h\{(1+\frac{C_S}{C_G})(-V_{ON}) - \frac{2}{3}V_P[(\frac{C_S^3}{C_G^3} - (\frac{C_S^2}{C_G^2} + \frac{V_{ON}}{V_P})^{\frac{3}{2}}]\}$	$V_G \geq 0$ $V_D \geq V_{DSAT}$

Model parameters	**Equation**
Channel conductance	$\sigma = \mu q N_D$
Turn-on voltage	$V_{ON} = V_P - \frac{qN_D h}{C_G}$
Pinch-off voltage	$V_P = -\frac{qN_D h^2}{2\varepsilon_S}$
Saturation voltage	$V_{DSAT} = V_G - V_{ON}$
Geometrical-based	W(width), L(length), h(channel thickness), C_G(gate insulator capacitance density)
Channel-based	N_D (donor concentration) μ (channel mobility), C_S(channel layer capacitance density)

Table 3.4 A summary of n-channel TFT drain current equations and voltage constraint equations for the modified comprehensive depletion-mode TFT model introduced herein. Differences between the original and the modified model are indicated in red.

Regime of operation	**Drain Current Equation**	**Voltage Constraint Equations**
DEPL	$I_{D,PRESAT}^{DEP} = \frac{W}{L}\sigma h\{(1+\frac{C_S}{C_G})V_D - \frac{2}{3}V_P[(\frac{C_S^2}{C_G^2}+\frac{V_G}{V_P})^{\frac{3}{2}} - (\frac{C_S^2}{C_G^2}+\frac{V_{GD}}{V_P})^{\frac{3}{2}}]\}$	$V_{PO} < V_G < 0$ $V_D < V_{DSAT}$
DEPL-SAT	$I_{D,SAT}^{DEP} = \frac{W}{L}\sigma h\{(1+\frac{C_S}{C_G})V_{DSAT} - \frac{2}{3}V_P[(\frac{C_S^2}{C_G^2}+\frac{V_G}{V_P})^{\frac{3}{2}} - (\frac{C_S^2}{C_G^2}+\frac{V_{PO}}{V_P})^{\frac{3}{2}}]\}$	$V_{PO} < V_G < 0$ $V_D \geq V_{DSAT}$
ACC	$I_{D,PRESAT}^{ACC} = \frac{W}{L}\left[\mu_{\text{interface}} C_G (V_G V_D - \frac{V_D^2}{2}) + \sigma h V_D\right]$	$V_G \geq 0$ $V_D < V_G$
ACC-DEP	$I_{D,PRESAT}^{ACC-DEP} = \frac{W}{2L}\mu_{\text{interface}} C_G V_G^2 + \frac{W}{L}\sigma h V_G + \frac{W}{L}\sigma h\{(1+\frac{C_S}{C_G})(V_D - V_G) - \frac{2}{3}V_P[(\frac{C_S^3}{C_G^3} - (\frac{C_S^2}{C_G^2}+\frac{V_{GD}}{V_P})^{\frac{3}{2}}]\}$	$V_G \geq 0$ $V_G \leq V_D < V_{DSAT}$
ACC-SAT	$I_{D,SAT}^{ACC} = \frac{W}{2L}\mu_{\text{interface}} C_G V_G^2 + \frac{W}{L}\sigma h V_G + \frac{W}{L}\sigma h\{(1+\frac{C_S}{C_G})(-V_{PO}) - \frac{2}{3}V_P[(\frac{C_S^3}{C_G^3} - (\frac{C_S^2}{C_G^2}+\frac{V_{PO}}{V_P})^{\frac{3}{2}}]\}$	$V_G \geq 0$ $V_D \geq V_{DSAT}$

Model parameters	**Equation**
Channel conductance	$\sigma = \mu_{\text{bulk}} q n_{co}$

Pinch-off voltage	$V_{PO} = V_P - \frac{qn_{co}h}{C_G}$
Channel layer pinch-off voltage	$V_P = -\frac{qn_{co}h}{2C_S}$
Saturation voltage	$V_{DSAT} = V_G - V_{PO}$
Geometrical-based	W(width), L(length), h(channel thickness), C_G(gate insulator capacitance density)
Channel-based	n_{co} (electron concentration in the conduction band at zero bias) $\mu_{interface}$ (interface mobility), μ_{bulk} (bulk mobility), C_S(channel layer capacitance density)

Some terms (in red) in Table 3.4 are modified compared to the original model as summarized in Table 3.3 in order to describe depletion-mode TFT behavior (i.e., V_{PO} (pinch-off voltage), n_{co} (electron concentration in the conduction band at zero bias), $\mu_{interface}$ (interface mobility), μ_{bulk} (bulk mobility)). These model modifications are discussed in the following.

First, in the modified comprehensive depletion-mode model, the pinch-off voltage acquires a new algebraic symbol, i.e., V_{PO} rather than V_P. Furthermore, V_{PO} in the modified comprehensive depletion-mode model is identical to what was termed V_{ON} in the original model. This change is undoubtedly confusing, to the reader.

However, this and other notational changes are deemed essential in order to unambiguously distinguish between depletion- and enhancement-mode TFT behavior.

V_{PO} is equal to the applied gate voltage required to fully deplete the full width of the channel layer, h. This requires dropping voltage across the channel (first term below) and also across the gate insulator (second term below)

$$V_{PO} = -\frac{qn_{co}h}{2C_S} - \frac{qn_{co}h}{C_G}, \tag{3.19}$$

where n_{co} is the electron concentration in the conduction band at zero bias, h is the thickness of channel layer, C_S is the channel layer capacitance density, and C_G is the gate insulator capacitance density. The negative sign of V_{PO} for an n-channel TFT means that electrons are present in the channel even when no accumulation gate voltage is applied. n_{co} replaces N_D in the modified comprehensive depletion-mode model since it offers a more accurate picture of the operation of a depletion-mode TFT, although it does not alter the model in any mathematically meaningful way. Recognizing that C_S is equal to $\frac{\varepsilon_S}{h}$, the factor of 2 in the denominator of the first term on the right side of Eq. (3-19) is associated with fact that the charge centroid of a fully depleted channel layer is located at the center of the channel.

Second, mobility $\mu_{\text{interface}}$ and μ_{bulk} are distinguished from channel mobility μ in the original comprehensive depletion-mode model in order to differentiate between carrier transport at the interface and in the 'bulk'. The original comprehensive depletion-mode model equations are derived by considering the channel conductance

in the linear regime of device operation, G_D^{LIN} [16]. For an n-channel, depletion-mode TFT, the channel conductance in the linear regime can be modeled as,

$$G_D^{LIN} = \frac{Z}{L}\mu q N_e , \tag{3.20}$$

where N_e is the density of electrons per cm^2 of gate area. Because drain current can flow in both depletion and accumulation, two kinds of carriers – interface and 'bulk' – contribute to current in a depletion-mode TFT. Thus, in a depletion-mode TFT in accumulation, 'bulk' electrons are present in the channel even at zero gate bias, while interface electrons present in the accumulation layer are induced by a positive gate bias. In the context of N_e, 'bulk' and interface electrons are modelled according to

$$N_e = n_{co}h + \frac{C_G V_G}{q}, \tag{3.21}$$

where n_{co} is the 'bulk' electron (assume to be uniform) concentration per unit area in the channel, h is the thickness of channel, and C_G is the gate capacitance density. The first term in Eq. (3.19) is associated with 'bulk' electrons while the second term is due to gate voltage-induced electrons in an accumulation layer created near the gate insulator – channel interface. The mobility of an interface electron in the accumulation layer, $\mu_{\text{interface}}$, is expected to be smaller than the mobility of a 'bulk' electron, μ_{bulk}, due to interface roughness and other types of interface scattering. Thus, the channel conductance in the linear regime of device operation in accumulation, $G_D^{LIN}\big|_{ACC}$, is modeled as

$$G_D^{LIN}\big|_{ACC} = \frac{Z}{L}\left(q\mu_{\text{bulk}} n_{co}h + \mu_{\text{interface}} V_G C_G\right). \tag{3.22}$$

Finally, the comprehensive depletion-mode for a p-channel TFT is shown in Table 3.5. The main differences between Table 3.4 (n-channel) and 3.5 (p-channel) are the signs of the drain current and voltage constraints equations associated with the fact that conduction in a p-channel TFT involves the flow of holes, not electrons. In addition, the hole concentration in the valence band at zero bias, p_{vo} is used in the p-channel TFT model instead of n_{co} as is used in the n-channel TFT model.

Table 3.5 A summary of p-channel, TFT drain current equations and voltage constraint equations for the modified comprehensive depletion-mode TFT model. Differences in equations between n- and p-channel layer modeling are marked in blue.

Regime of operation	**Drain Current Equation**	**Voltage Constraint Equations**
Compre-hensive depletion-mode model	$I_{D,PRESAT}^{DEP} = \frac{W}{L}\sigma h\{(1+\frac{C_S}{C_G})V_D - \frac{2}{3}V_P[(\frac{C_S^2}{C_G^2}+\frac{V_G}{V_P})^{\frac{3}{2}} - (\frac{C_S^2}{C_G^2}+\frac{V_{GD}}{V_P})$	$0 < V_G \le V_{PO}$ $V_D < V_{DSAT}$
	$I_{D,SAT}^{DEP} = \frac{W}{L}\sigma h\{(1+\frac{C_S}{C_G})V_{DSAT} - \frac{2}{3}V_P[(\frac{C_S^2}{C_G^2}+\frac{V_G}{V_P})^{\frac{3}{2}} - (\frac{C_S^2}{C_G^2}+\frac{V_{PO}}{V_P}$	$0 < V_G \le V_{PO}$ $V_D \ge V_{DSAT}$
	$I_{D,PRESAT}^{ACC} = \frac{W}{L}\left[-\mu_{\text{interface}} C_G (V_G V_D - \frac{V_D^2}{2}) + \sigma h V_D\right]$	$V_G \le 0$ $V_D < V_G < V_D$
	$I_{D,PRESAT}^{ACC-DEP} = -\frac{W}{2L}\mu_{\text{interface}} C_G V_G^2 + \frac{W}{L}\sigma h V_G -$	$V_G \le 0$ $V_G \le V_D < V_D$

	$\frac{W}{L}\sigma h\{(1+\frac{C_S}{C_G})(V_D-V_G)-\frac{2}{3}V_P[(\frac{C_S^3}{C_G^3}-(\frac{C_S^2}{C_G^2}+\frac{V_{GD}}{V_P})^{\frac{3}{2}}]\}$	
	$I_{D,SAT}^{ACC}=-\frac{W}{2L}\mu_{\text{interface}}C_G V_G^2+\frac{W}{L}\sigma h V_G-$ $\frac{W}{L}\sigma h\{(1+\frac{C_S}{C_G})(-V_{PO})-\frac{2}{3}V_P[(\frac{C_S^3}{C_G^3}-(\frac{C_S^2}{C_G^2}+\frac{V_{PO}}{V_P})^{\frac{3}{2}}]\}$	$V_G \le 0$ $V_D \ge V_{DSAT}$

Model parameters	**Equation**
Channel conductance	$\sigma=\mu_{\text{bulk}}qp_{vo}$
Pinch-off voltage	$V_{PO}=\frac{qp_{vo}h}{2C_S}+\frac{qp_{vo}h}{C_G}>0 \quad (V_P=\frac{qp_{vo}h}{2C_S})$
Saturation voltage	$V_{DSAT}=V_G-V_{PO}$
Geometrical-based	W(width), L(length), h(channel thickness), C_G(gate insulator capacitance density)
Channel-based	p_{vo} (hole concentration in the valence band at zero bias), $\mu_{\text{interface}}$ (interface mobility), μ_{bulk} (bulk mobility), C_S(channel layer capacitance density)

3.4 Subpinchoff and off current

3.4.1 Subpinchoff current in a depletion-mode TFT

As mentioned in Section 3.2 for a depletion-mode TFT, when the gate bias is below the pinch-off voltage and the channel interface is in weak depletion, the corresponding drain current is denoted as a subpinchoff current. In the original comprehensive depletion-mode model, only drift current was considered when deriving the expressions for the pre-saturation or saturation regime drain current. However, the assumption of drift current only is not valid for the subpinchoff regime, in which the drain current is dominated by diffusion. Thus, diffusion current should be included when the drain current in a depletion-mode TFT is in the subpinchoff regime of device operation.

The diffusion current component of the drain current is derived by considering the electron density gradient in the channel [16] as given by

$$I_D(y) = -WqD_n \frac{dn(y)}{dy} \approx W\mu_{\text{bulk}} k_B T \frac{n(L)-n(0)}{L}, \tag{3.22}$$

where n is the electron density, which is equal to $\frac{Q_n}{qt}$, where Q_n is the electron charge density in channel, and t is the channel thickness. Based on the charge-sheet model [64], Eq. (3.22) can be rewritten as

$$I_D(y) = \frac{W}{L}\mu_{\text{bulk}} \frac{k_B T}{q}\left[Q_n(L) - Q_n(0)\right]. \tag{3.23}$$

Assessing Q_n at y = 0 and L [62], the subpinchoff current $I_{D,SUB}$ in a p-channel, depletion-mode TFT can be expressed as

$$I_{D,SUB} = -\frac{W}{L}\mu_{bulk} C_G \left(\frac{k_B T}{q}\right)^2 \exp\left[\frac{-q\left(V_G - V_{OFF}\right)}{\left(1+\frac{C_{DOS}}{C_G}\right)k_B T}\right]\left(1 - e^{\frac{+qV_D}{k_B T}}\right), \qquad (3.24)$$

where μ_{bulk} is the 'bulk' mobility, V_{OFF} is the turn-off voltage, and C_{DOS} is the channel layer density of states capacitance density. From Eq. (3-24), the subpinchoff swing (S) in a depletion-mode TFT is given by

$$S = \left[\frac{d\left(\log I_{D,SUB}\right)}{dV_G}\right]^{-1} = \frac{2.3k_B T}{q}\left(1+\frac{C_{DOS}}{C_G}\right). \qquad (3.25)$$

C_{DOS} accounts for the density of states within the bandgap in a depletion-mode TFT [65]. C_{DOS} is defined as the first derivation of the semiconductor charge density Q_S with respect to the surface potential ψ_S,

$$C_{DOS} = \frac{\partial Q_S}{\partial \psi_S}. \qquad (3.26)$$

As shown in Figure 3.3, ψ_S is obtained by recognizing that the overvoltage ($V_G - V_{OFF}$) capacitively divides across the gate insulator capacitance density C_G and C_{DOS}, leading to the term $1+\frac{C_{DOS}}{C_G}$ in the denominator of the first exponential term in Eq. (3.24). C_{DOS} is used to denote the semiconductor capacitance density in a depletion-mode TFT in order to distinguish it from the interface trap capacitance density (C_{IT}) in an enhancement-mode TFT [5]. Although C_{DOS} and C_{IT} are essentially equivalent in the context of how they are employed in an equation such as

Eq. (3.24), physically they are distinctly different since they correspond to 'bulk' states within the bandgap and interface traps, respectively.

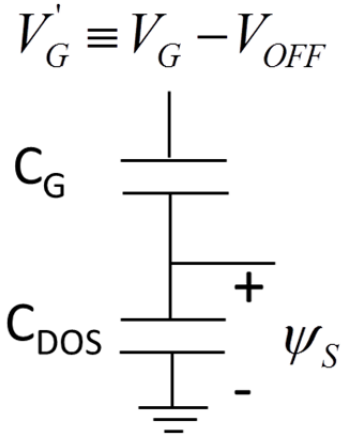


Figure 3.3: An equivalent circuit illustrating how the gate overvoltage ($V_G - V_{OFF}$) capacitively divides across the gate insulator capacitance density (C_G) and channel layer density of states capacitance density (C_{DOS}). The surface potential (ψ_S) corresponds to the total voltage drop across the semiconductor.

The current-voltage relations for both drift ($I_{D,PRESAT}$ and $I_{D,SAT}$) and diffusion ($I_{D,SUB}$) contributions are given in Table 3.4 (in Section 3.3) and Eq. (3.24), respectively. However, neither of these expressions remain applicable over the entire range of V_G. Various strategies have been employed in FET modeling to account for the drain current over the entire range of V_G [66-69]. One popular method for combining these two operation regions (subpinchoff and presaturation/saturation) is to simply add them to obtain the total drain current, yielding [66]

$$I_D = I_{D,SUB} + I_{D,PRESAT}, \quad V_D < V_{D,SAT}, \tag{3.31}$$

or

$$I_D = I_{D,SUB} + I_{D,SAT}, \quad V_D \geq V_{D,SAT}, \tag{3.32}$$

In this strategy, a piecewise-defined function is applied in order to get smooth transition at $V_G = V_{PO}$ as

$$I_D = \begin{cases} 0, & V_G < V_{OFF} \\ I_{D,SUB}, & V_{OFF} \leq V_G < V_{PO} \\ I_{D,SUB}(V_G = V_{PO}) + I_{D,PRESAT}, & V_G \geq V_{PO}, V_D < V_{D,SAT} \end{cases}, \tag{3.33}$$

or

$$I_D = \begin{cases} 0, & V_G < V_{OFF} \\ I_{D,SUB}, & V_{OFF} \leq V_G < V_{PO} \\ I_{D,SUB}(V_G = V_{PO}) + I_{D,PRESAT}, & V_G \geq V_{PO}, V_D \geq V_{D,SAT} \end{cases}. \tag{3.34}$$

However, this piecewise-defined function is problematic due to the fact that its derivatives of arbitrary order are discontinuous, rendering this model inconsistent with the ∞-differentiability rule [66].

Another strategy for accounting for the drain current over the full range of V_G is to add current contributions in a reciprocal fashion in order to smooth the transition from subpinchoff to presaturation/saturation in an n-channel TFT[67, 68],

$$\frac{1}{I_D} = \frac{1}{I_{D,PRESAT}} + \frac{1}{I_{D,SUB}}, \quad V_D < V_{D,SAT}, \tag{3.35}$$

or

$$\frac{1}{I_D} = \frac{1}{I_{D,SAT}} + \frac{1}{I_{D,SUB}}, \quad V_D \geq V_{D,SAT}. \tag{3.36}$$

Use of reciprocal addition means that I_D is mainly determined by the smaller contribution of the diffusion and drift current. In presaturation/saturation, $I_{D,SUB}$ is

extremely large compared to $I_{D,PRESAT} / I_{D,SAT}$ due to its exponential dependence upon V_G. Thus, I_D is almost exclusively determined by $I_{D,PRESAT} / I_{D,SAT}$ when $I_{D,SUB}$ and $I_{D,PRESAT} / I_{D,SAT}$ are combined in this reciprocal fashion. Although a physical motivation for using the reciprocal form is obscure, its use indeed solves the problem of having to transition from subpinchoff to above-pinchoff in a smooth manner. However, one pitfall of using the Eq. (3.35) and (3.36) reciprocal method is that it can lead to a discontinuity in I_D near the V_{PO} transition when a small V_G sweep step (e.g., 0.1 V) is used in the simulation. This discontinuity problem can be circumvented by increasing the V_G step size to a larger value (e.g., 1 – 5 V).

3.4.2 Off current in a p-channel, depletion-mode TFT

When a p-channel TFT is turned off ($V_G < V_{OFF}$), it is typically observed that an appreciable drain current is still measured. This residual drain current is denoted as off current (I_{OFF}). I_{OFF} is typically found to be extremely small (i.e., ~10^{-12} A) in amorphous oxide semiconductor (AOS) TFTs, which are n-channel devices [70]. In an AOS TFT, I_{OFF} is usually attributed to gate leakage, leading to the normal assumption that off current is identical to the gate leakage current. However, much larger off currents (i.e., ~10^{-9} A) are invariably reported for p-channel, depletion-mode oxide TFTs [39, 44]. Thus, it is necessary to more carefully account for off current when accurately modeling a p-channel, depletion-model TFT.

Three possible I_{OFF} current paths are through the gate, through the ‘bulk’ of the channel, and near the surface of the channel, as shown in Fig. 3.4. I_{OFF} through

the gate, I_G, can be modeled as a current source. I_{OFF} through the 'bulk' of the channel and near the surface of the channel can be modeled as two resistors in parallel, denoted as R_{bulk} and R_{surface}, respectively.

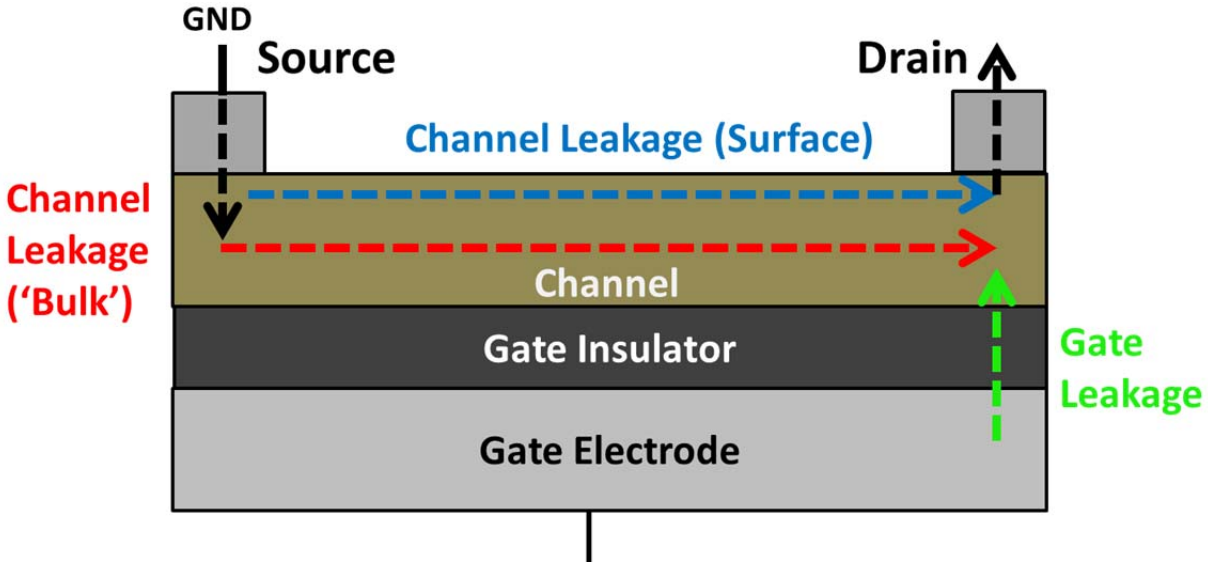


Figure 3.4 Three possible off current leakage paths are through the gate (green), through the 'bulk' of the channel (red), and near the surface of the channel (blue).

Thus, I_{OFF} in a depletion-mode TFT involve three contributions, and can be modeled as

$$I_{OFF} = I_G + V_D\left(\frac{1}{R_{\text{surface}}} + \frac{1}{R_{bulk}}\right). \tag{3.37}$$

R_{bulk} can be calculated as

$$R_{bulk} = \frac{\rho L}{A} = \frac{1}{q\left(\mu_{n,bulk} n_o + \mu_{p,bulk} p_o\right)} \frac{L}{Wh}, \tag{3.38}$$

where ρ is resistivity, L is channel length, A is the cross-sectional area of current flow, $\mu_{n,bulk}$ is bulk electron mobility, n_o is electron density in equilibrium, $\mu_{p,bulk}$ is

bulk hole mobility, p_o is hole density in equilibrium, W is channel width, and h is channel thickness. For a p-channel TFT, Eq. (3.38) can be simplified to be

$$R_{bulk} = \frac{1}{q\mu_{bulk} p_o} \frac{L}{Wh}, . \tag{3.39}$$

and p_o can be calculated as

$$p_o = N_V \exp\left[(E_F - E_V)/k_B T\right]. \tag{3.40}$$

where N_V is the valence band effective density of states, E_F is the Fermi energy, E_V is the top of valence band energy, k_B is Boltzmann constant, and T is temperature.

Drain current and voltage constraint equations used to incorporate the subpinchoff current into the simulation of a n-channel, depletion-mode TFT transfer curve are summarized in Table 3.6. The total drain current $I_{D,TOTAL}$ is the sum of drain current (involving the drift and diffusion current) and off current, $I_{D,TOTAL} = I_D + I_{OFF}$. These equations can be used in both the square-law model and the comprehensive depletion-mode model if $I_{D,PRESAT}$ and $I_{D,SAT}$ are presented by their appropriate equivalents, i.e., $I_{D,PRESAT}^{DEP}$, $I_{D,PRESAT}^{ACC}$, $I_{D,PRESAT}^{ACC-DEP}$ or $I_{D,SAT}^{DEP}$, $I_{D,SAT}^{ACC}$, respectively. The drain current and voltage constraint equations used to simulate a p-channel, depletion-mode TFT transfer curve for the entire range of V_G are summarized in Table 3.7. The differences between p-channel and n-channel, depletion-mode TFTs in Table 3.7 and 3.6 involve the signs of $I_{D,SUB}$ and the voltage constraint equations

Table 3.6. A summary of drain current and voltage constraint equations used to incorporate the subpinchoff current into the simulation of an n-channel, depletion-mode TFT transfer curve. Identical equations are applicable for square-law modeling of n-channel, enhancement-mode TFT except that V_{OFF} is replaced by V_{ON} and C_{DOS} is replaced by C_{IT}, the interface trap capacitance density.[62]

Drain Current Equation	**Voltage Constraint Equation**
$I_{OFF} = I_G + V_D\left(\frac{1}{R_{\text{surface}}} + \frac{1}{R_{bulk}}\right)$	$V_G < V_{OFF}$
$I_{D,SUB} = \frac{W}{L}\mu_{bulk}C_G\left(\frac{k_BT}{q}\right)^2 \exp\left[\frac{q(V_G - V_{OFF})}{\left(1+\frac{C_{DOS}}{C_G}\right)k_BT}\right]\left(1-e^{\frac{-qV_D}{k_BT}}\right)$	$V_G \geq V_{OFF}$
$\frac{1}{I_D} = \frac{1}{I_{D,PRESAT}} + \frac{1}{I_{D,SUB}}; I_{D,TOTAL} = I_D + I_{OFF}$	$V_G \geq V_{OFF}$ $V_D < V_{DSAT}$
$\frac{1}{I_D} = \frac{1}{I_{D,SAT}} + \frac{1}{I_{D,SUB}}; I_{D,TOTAL} = I_D + I_{OFF}$	$V_G \geq V_{OFF}$ $V_D \geq V_{DSAT}$
R_{surface} (surface resistance), R_{bulk} (bulk resistance), I_G (gate leakage current), C_{DOS} (channel layer density of states capacitance density)	

Table 3.7. A summary of drain current and voltage constraint equations used to incorporate the subpinchoff current into the simulation of a p-channel, depletion-mode TFT transfer curve.

Drain Current Equation	**Voltage Constraint Equation**
$I_{OFF} = I_G + V_D\left(\frac{1}{R_{\text{surface}}} + \frac{1}{R_{bulk}}\right)$	$V_G > V_{OFF}$
$I_{D,SUB} = -\frac{W}{L}\mu_{bulk}C_G\left(\frac{k_BT}{q}\right)^2 \exp\left[\frac{-q(V_G - V_{OFF})}{\left(1+\frac{C_{DOS}}{C_G}\right)k_BT}\right]\left(1-e^{\frac{qV_D}{k_BT}}\right)$	$V_G \le V_{OFF}$
$\frac{1}{I_D} = \frac{1}{I_{D,PRESAT}} + \frac{1}{I_{D,SUB}}; I_{D,TOTAL} = I_D + I_{OFF}$	$V_G \le V_{OFF}$ $V_D > V_{DSAT}$
$\frac{1}{I_D} = \frac{1}{I_{D,SAT}} + \frac{1}{I_{D,SUB}}; I_{D,TOTAL} = I_D + I_{OFF}$	$V_G \le V_{OFF}$ $V_D \le V_{DSAT}$
R_{surface} (surface resistance), R_{bulk} (bulk resistance), I_G (gate leakage current), C_{DOS} (channel layer density of states capacitance density)	

3.5 Mobility expressions for the comprehensive depletion-mode model

As mentioned in Section 2.1.3, a high channel mobility is desired because a larger mobility means that a TFT can conduct more current. Thus, precise estimation of channel mobility in a TFT is essential for evaluating its performance.

Five mobility extraction methodologies, all derived from the square-law model, are summarized in Table 3.8, and include the effective mobility μ_{EFF}, field-effect mobility μ_{FE}, average mobility μ_{AVG}, incremental mobility μ_{INC} and saturation mobility μ_{SAT}. As indicated in Table 3.8, each mobility expression is classified according to whether it is assessed in the linear regime (i.e., μ_{EFF}, μ_{FE}, μ_{AVG}, μ_{INC}) or in the saturation regime (μ_{SAT}).

One common approach for assessing mobility is to linearize $I_{D,PRESAT}$ by ignoring the term $V_D^2/2$ in Eq. (2.2) for $I_{D,PRESAT}$, define the channel conductance as $G_D = I_D / V_D$ [18], and extract mobility in terms of G_D. As shown in Table 3.8, μ_{EFF} and μ_{AVG}, are both obtained in this manner. μ_{INC} is assessed by differentiating G_D with respect to V_G. μ_{FE} is also defined in a differential manner, but by differentiating I_D with respect to V_G, recognized as small-signal transconductance in the linear regime of TFT operation, i.e., $g_m(V_G) = \partial I_D / \partial V_G$ when $V_D \to 0$.

Although the μ_{EFF} and μ_{FE} are commonly employed in FET mobility assessment [20], and are almost identical to μ_{AVG} and μ_{INC}, respectively, μ_{AVG} and

μ_{INC} are exclusively employed herein since they were derived specifically for TFT mobility assessment and physical basis for their use is clearer [17]. As evident from Table 3.8, the expression for μ_{AVG} is identical to that of μ_{EFF} except that V_T is replaced by V_{ON}. This is an advantage since V_{ON} is more easily and accurately estimated from a log (I_D) versus V_G TFT transfer curve. Also, μ_{AVG} can be evaluated in subthreshold ($V_{ON} < V_G < V_T$) for an enhancement-mode TFT or subpinchoff ($V_{OFF} < V_G < V_{PO}$) for a depletion-mode TFT). μ_{AVG} and μ_{EFF} are found to be very similar for a TFT with a small subthreshold slope since V_{ON} and V_T are almost equal to each other. μ_{INC} is identical to μ_{FE} once it is recognized that,

$$\frac{\partial G_D(V_G)}{\partial V_G} = \frac{\partial I_D(V_G)}{\partial V_G}\frac{1}{V_D} = \frac{g_m(V_G)}{V_D}. \qquad (3.41)$$

Another common approach for assessing mobility involves TFT evaluation in the saturation region by taking the square root of $I_{D,SAT}$ in Eq. (2.6) and then differentiating with respect to V_G. This leads to the saturation mobility, μ_{SAT}, which is determined from the slope of an $\sqrt{I_{D,SAT}}$ versus V_G curve [20],

$$\mu_{SAT} = \frac{2}{\frac{W}{L}C_G}\left(\frac{\partial\sqrt{I_{DSAT}}}{\partial V_G}\right)^2. \qquad (3.42)$$

All five mobility extraction methodologies are derived from the square-law model, in which it is assumed that drift dominates in an enhancement-mode TFT. In order to accurately estimate the mobility for a depletion-mode TFT, the

comprehensive depletion-mode model must be applied in order to derive corresponding mobility expressions. Table 3.9 summarizes mobilities derived using the comprehensive depletion-mode model for an n-channel, depletion-mode TFT.

Table 3.8 Summary of five mobilities often used in the assessment of an n-channel, enhancement-mode TFT.

Mobility	**Operation regime**	**Mobility expression**
μ_{EFF}	Linear	$\mu_{EFF} = \dfrac{G_D(V_G)}{\dfrac{W}{L}C_G\left(V_G - V_T\right)}$
μ_{FE}	Linear	$\mu_{FE} = \dfrac{g_m(V_G)}{\dfrac{W}{L}C_G V_D}$
μ_{AVG}	Linear	$\mu_{AVG} = \dfrac{G_D(V_G)}{\dfrac{W}{L}C_G\left(V_G - V_{ON}\right)}$
μ_{INC}	Linear	$\mu_{INC} = \dfrac{\dfrac{\partial G_D(V_G)}{\partial V_G}}{\dfrac{W}{L}C_G}$
μ_{SAT}	Saturation	$\mu_{SAT} = \dfrac{2}{\dfrac{W}{L}C_G}\left(\dfrac{\partial\sqrt{I_{D,SAT}(V_G)}}{\partial V_G}\right)^2$
$G_D(V_G) = \left.\dfrac{I_D}{V_D}\right\|_{V_D\to 0}$; $g_m(V_G) = \left.\dfrac{\partial I_D}{\partial V_G}\right\|_{V_D\to 0}$		

Table 3.9 Defining mobility expression and its square-law model or the comprehensive depletion-mode model equivalent for a n-channel, depletion-mode TFT.

Mobility expression	**Square-law model**	**Comprehensive depletion-mode model**
$\mu_{EFF} = \left.\dfrac{G_D(V_G)}{\dfrac{W}{L}C_G\left(V_G - V_{PO}\right)}\right\|_{V_D \to 0}$	$\mu_{EFF} = \mu_{Interface}$	$\mu_{EFF}^{DEPL} = \dfrac{qn_{co}h}{C_G(V_G - V_{PO})}(1 + \dfrac{C_S}{C_G} - \sqrt{k})\mu_{\text{bulk}}$; $\mu_{EFF}^{ACC} = \dfrac{1}{C_G(V_G - V_{PO})}(\mu_{\text{interface}}C_G V_G + \mu_{bulk}qn_{co}h)$
$\mu_{FE} = \left.\dfrac{g_m(V_G)}{\dfrac{W}{L}C_G V_D}\right\|_{V_D \to 0}$	$\mu_{FE} = \mu_{Interface}$	$\mu_{FE}^{DEPL} = \dfrac{qn_{co}h}{C_G}(\dfrac{1}{2V_P\sqrt{k}})\mu_{\text{bulk}}$; $\mu_{FE}^{ACC} = \mu_{\text{interface}}$
$\mu_{AVG} = \left.\dfrac{G_D(V_G)}{\dfrac{W}{L}C_G(V_G - V_{OFF})}\right\|_{V_D \to 0}$	$\mu_{AVG} = \mu_{Interface}$	$\mu_{AVG}^{DEPL} = \dfrac{qn_{co}h}{C_G(V_G - V_{OFF})}(1 + \dfrac{C_S}{C_G} - \sqrt{k})\mu_{\text{bulk}}$; $\mu_{AVG}^{ACC} = \dfrac{1}{C_G(V_G - V_{OFF})}(\mu_{\text{interface}}C_G V_G + \mu_{bulk}qn_{co}h)$
$\mu_{INC} = \left.\dfrac{\dfrac{\partial G_D(V_G)}{\partial V_G}}{\dfrac{W}{L}C_G}\right\|_{V_D \to 0}$	$\mu_{INC} = \mu_{Interface}$	$\mu_{INC}^{DEPL} = \dfrac{qn_{co}h}{C_G}(\dfrac{1}{2V_P\sqrt{k}})\mu_{\text{bulk}}$; $\mu_{INC}^{ACC} = \mu_{\text{interface}}$
$k = \dfrac{C_S^2}{C_G^2} + \dfrac{V_G}{V_P}$		

The first column in Table 3.9 specifies the defining mobility equation for μ_{EFF}, μ_{FE}, μ_{AVG} and μ_{INC}. Using these defining mobility expressions in the context of the square-law model leads to the conclusion that each of these four mobilities are identical to the interface mobility, $\mu_{Interface}$. This is as expected since these defining equations were derived from the square-law model. In contrast, the mobility expressions derived from the comprehensive depletion-mode model are more complicated. There are five regimes of TFT operation, the depletion (DEPL), depletion-saturation (DEPL-SAT), accumulation (ACC), accumulation-depletion (ACC-DEPL), and accumulation-saturation (ACC-SAT) according to the comprehensive depletion-mode model. Since μ_{EFF}, μ_{FE}, μ_{AVG} and μ_{INC} are obtained in the linear region, only DEPL and ACC regimes are involved to assess these four mobilities, and denoted as μ_{EFF}^{DEPL} and μ_{EFF}^{ACC}, respectively.

Finally, mobilities derived using the comprehensive depletion-mode model for a p-channel TFT are shown in Table 3.10. The main differences between Table 3.9 (n-channel) and 3.10 (p-channel) are the signs associated with voltages and the symbols specific carrier concentration. Simulation results in which different mobilities are plotted as a function of V_G are discussed in Chapter 4.

Table 3.10 Defining mobility expression and its square-law model or the comprehensive depletion-mode model equivalent for a p-channel, depletion-mode TFT.

Mobility expression	**Square-law model**	**Comprehensive depletion-mode model**
$\mu_{EFF} = \left.\dfrac{G_D(V_G)}{\dfrac{W}{L}C_G\left(V_{PO}-V_G\right)}\right\|_{V_D\to 0}$	$\mu_{EFF} = \mu_{Interface}$	$\mu_{EFF}^{DEPL} = \dfrac{qp_{vo}h}{C_G(V_{PO}-V_G)}(1+\dfrac{C_S}{C_G}-\sqrt{k})\mu_{\text{bulk}}$; $\mu_{EFF}^{ACC} = \dfrac{1}{C_G(V_{PO}-V_G)}(-\mu_{\text{interface}}C_GV_G+\mu_{bulk}qp_{vo}h)$
$\mu_{FE} = \left.\dfrac{g_m(V_G)}{\dfrac{W}{L}C_G(-V_D)}\right\|_{V_D\to 0}$	$\mu_{FE} = \mu_{Interface}$	$\mu_{FE}^{DEPL} = \dfrac{qp_{vo}h}{C_G}(\dfrac{1}{2V_P\sqrt{k}})\mu_{\text{bulk}}$; $\mu_{FE}^{ACC} = \mu_{\text{interface}}$
$\mu_{AVG} = \left.\dfrac{G_D(V_G)}{\dfrac{W}{L}C_G(V_{OFF}-V_G)}\right\|_{V_D\to 0}$	$\mu_{AVG} = \mu_{Interface}$	$\mu_{AVG}^{DEPL} = \dfrac{qp_{vo}h}{C_G(V_{OFF}-V_G)}(1+\dfrac{C_S}{C_G}-\sqrt{k})\mu_{\text{bulk}}$; $\mu_{AVG}^{ACC} = \dfrac{1}{C_G(V_{OFF}-V_G)}(-\mu_{\text{interface}}C_GV_G+\mu_{bulk}qp_{vo}h)$
$\mu_{INC} = \left.\dfrac{\dfrac{\partial G_D(V_G)}{\partial V_G}}{\dfrac{W}{L}C_G}\right\|_{V_D\to 0}$	$\mu_{INC} = \mu_{Interface}$	$\mu_{INC}^{DEPL} = \dfrac{qp_{vo}h}{C_G}(\dfrac{1}{2V_P\sqrt{k}})\mu_{\text{bulk}}$; $\mu_{INC}^{ACC} = \mu_{\text{interface}}$
$k = \dfrac{C_S^2}{C_G^2}+\dfrac{V_G}{V_P}$		

4. COMPREHENSIVE DEPLETION-MODE MODEL SIMULATION RESULTS

In this chapter, simulation results of depletion-mode thin-film transistors (TFTs) using the comprehensive depletion-mode model are presented and discussed.

4.1 Simulation Trends

Consider a p-channel TFT with two different hole concentrations, p_{vo} =10^{15} and 10^{18} cm^{-3}. The comprehensive depletion-mode model (Table 3.5) is used to simulate the I-V characteristics shown in Figs. 4.1 and 4.2 for these two hole concentrations, assuming that $\mu_{interface}$ = 1 $cm^2V^{-1}s^{-1}$ and μ_{bulk} =10 $cm^2V^{-1}s^{-1}$. Other model parameters employed in these simulations are listed in the captions of Fig. 4.1 and 4.2.

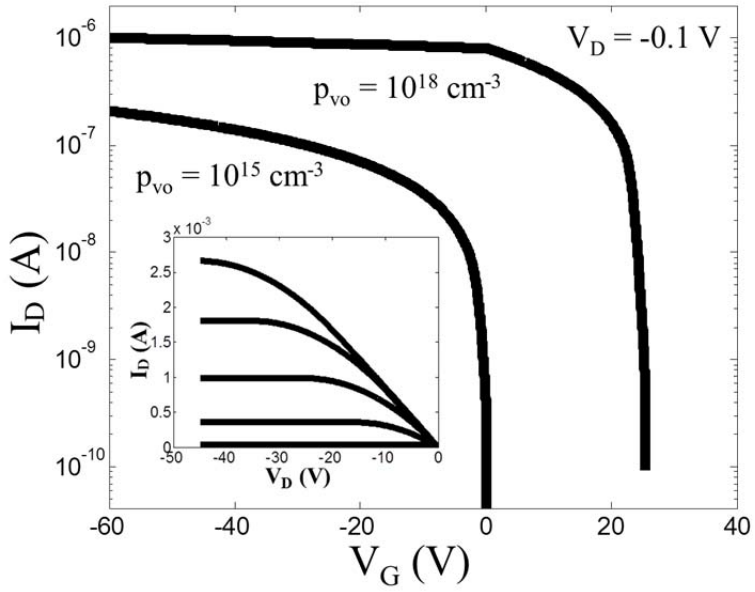


Figure 4.1 Simulated drain current-gate voltage (log (I_D) - V_G) TFT transfer curves for p_{vo} = 1×10^{15} (left) and 1×10^{18} cm^{-3}(right) at V_D = -0.1 V. The inset figure shows simulated drain current - drain voltage (I_D - V_D) output curves, in which V_G is increased from -30 V (top curve, showing maximum current) to 20 V in 10 V steps for p_{vo} = 1×10^{18} cm^{-3}. Other model parameters used in this simulation are: $\mu_{interface}$ = 1 $cm^2V^{-1}s^{-1}$, μ_{bulk} = 10 $cm^2V^{-1}s^{-1}$, W/L = 10, h = 50 nm, ε_s = 10, C_G = 3.45 $\times10^{-8}$ Fcm^{-2}, and C_{DOS} = 0 Fcm^{-2}.

The log(I_D)-V_G transfer curves included in Fig. 4.1 reveal a turn-on voltage, V_{ON} = 0 V and a turn-off voltage, V_{OFF} = 25.5 V for $p_{vo} = 10^{15}$ and 10^{18} cm^{-3}, respectively. Thus, a low (high) hole concentration leads to enhancement-mode (depletion-mode) TFT behavior [71]. In fact, in the limit of low doping as p_{vo} approaches 0, the comprehensive depletion-mode model reverts to the square-law model since $\sigma \rightarrow 0$ and $V_P \rightarrow 0$. The log (I_D) - V_G transfer curves given in Fig. 4.1 also show that at any given V_G, I_D is larger for the depletion-mode TFT since more holes are available to conduct current and 'bulk' holes have a higher mobility than gate voltage-induced holes in the accumulation layer. The I_D -V_D output curve shown in the insert of Fig. 4.1 is simulated for the $p_{vo} = 10^{18}$ cm^{-3} case. The corresponding I_D - V_D output curve for $p_{vo} = 10^{15}$ cm^{-3} (not shown) display significantly reduced drain current.

Figure 4.2 shows two simulated $\sqrt{I_{D,SAT}}$ - V_G transfer curves plotted for p_{vo} = 10^{15} and 10^{18} cm^{-3}. The saturation mobility, μ_{SAT}, is estimated as

$$\mu_{SAT} = \frac{m^2}{\frac{W}{2L} C_G}, \tag{4.1}$$

where m is the slope of a regression fit to the straight line portion of the $\sqrt{I_{D,SAT}}$ - V_G transfer curve. The saturation mobility extraction procedure works well for $p_{vo} = 10^{15}$ cm^{-3}, yielding a saturation mobility identical to the value of the interface mobility assumed as a simulation parameter. However, this saturation mobility extraction procedure fails miserably for $p_{vo} = 10^{18}$ cm^{-3}, providing an estimate of the saturation

mobility that is much closer to the value of the bulk mobility assumed as a simulation parameter.

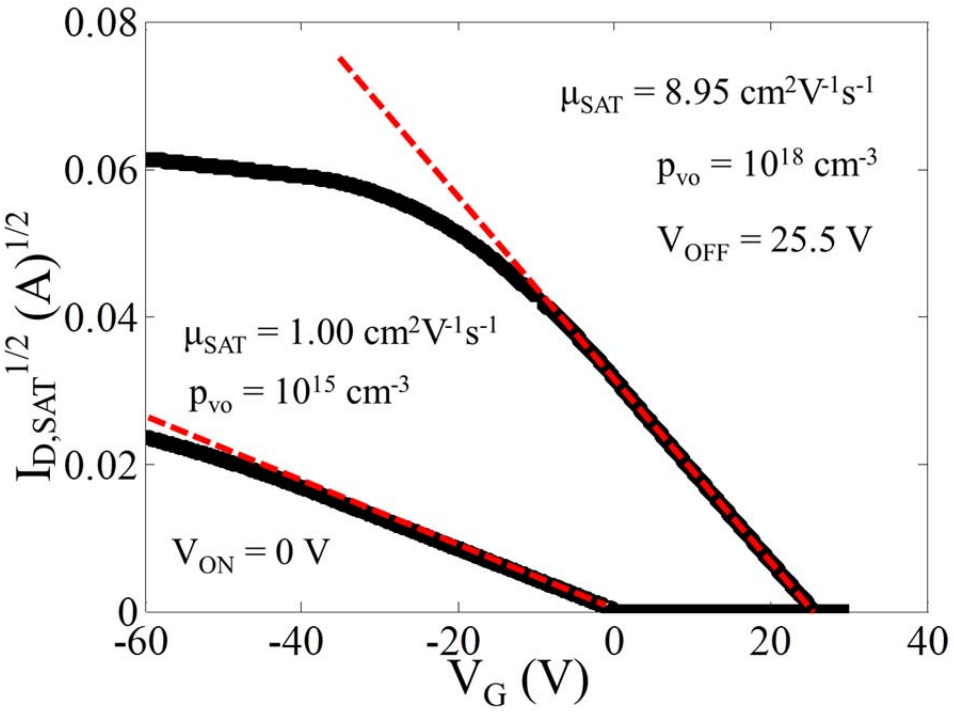


Figure 4.2 Simulated $(I_D)^{1/2}$ - V_G TFT transfer curves for p_{vo} = 1×10^{15} (left) and 1×10^{18} cm^{-3} (right) at V_D = -40 V. Model parameters used in this simulation are: $\mu_{interface}$ = 1 cm^{2}V^{-1}s^{-1}, μ_{bulk} = 10 cm^{2}V^{-1}s^{-1}, W/L = 10, h = 50 nm, ε_s = 10, C_G = 3.45 $\times10^{-8}$ Fcm^{-2}, and C_{DOS} = 0 Fcm^{-2}. The dash line is used to extract the slope of the $(I_D)^{1/2}$ - V_G curve.

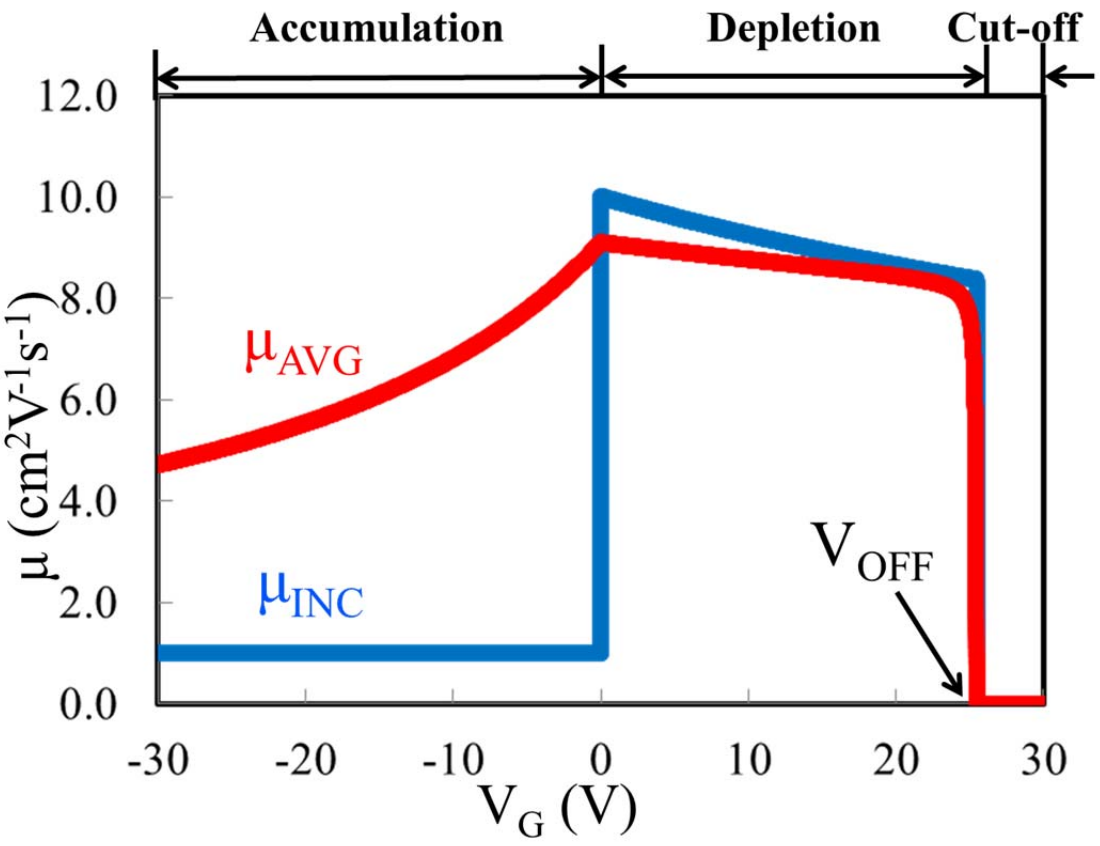


Figure 4.3 Extracted average mobility, μ_{AVG} (red) and incremental mobility, μ_{INC} (blue) in the linear region at V_D = -0.1 V as a function of gate voltage (V_G) from the previous simulation (a subpinchoff current is not included). Model parameters used in this simulation are: p = 1×10^{18} cm^{-3}, $\mu_{interface}$ = 1 $cm^2V^{-1}s^{-1}$, μ_{bulk} = 10 $cm^2V^{-1}s^{-1}$, W/L = 10, h = 50 nm, ε_s = 10, $C_G = 3.45\times10^{-8}$ Fcm^{-2}, and C_{DOS} = 0 Fcm^{-2}.

A channel mobility comparison of a simulated p-channel, depletion-mode TFT for p = 10^{18} cm^{-3} is provided in Fig. 4.3. The TFT is turned off when $V_G > V_{OFF}$. Note that the incremental mobility is higher than the average mobility in depletion, but lower than the average mobility in accumulation. Also, in depletion, μ_{AVG} and μ_{INC} are nearly equal to μ_{bulk}, while in accumulation, $\mu_{INC} = \mu_{interface}$ whereas $\mu_{AVG} \rightarrow \mu_{interface}$ as the TFT is more strongly accumulated by decreasing V_G (i.e., a negative gate voltage with a larger magnitude). This simulation reveals that $\mu_{interface}$ will be significantly overestimated for most applied gate voltages except for the case in

which μ_{INC} is assessed when the TFT is biased in accumulation. These $\mu_{interface}$ mobility overestimation trends can be elucidated by examining the relevant comprehensive depletion-mode model equations, collected by Table 3.10. For example, μ_{AVG} is given by μ_{AVG}^{DEPL} and μ_{AVG}^{ACC} in depletion and accumulation, respectively, i.e.,

$$\mu_{AVG}^{DEPL} = \frac{qp_{vo}h}{-C_G(V_G - V_{OFF})}\left(1 + \frac{C_S}{C_G} - \sqrt{\frac{C_S^2}{C_G^2} + \frac{V_G}{V_P}}\right)\mu_{\text{bulk}}, \tag{4.2}$$

and

$$\mu_{AVG}^{ACC} = \frac{1}{-C_G(V_G - V_{OFF})}\left(-\mu_{\text{interface}}C_G V_G + \mu_{bulk}qp_{vo}h\right), \tag{4.3}$$

where, the parameters shown in red (p_{vo}, h, $C_S(h, \varepsilon_S)$, V_P) are channel related while $C_G(\varepsilon_{OX}, t_{OX})$ is gate insulator related. As shown in Fig. 4.3, when V_G approaches zero from either accumulation or depletion, a maximum μ_{AVG} occurs, and is given by

$$\mu_{AVG}^{MAX} = \mu_{AVG}^{DEPL}(V_G \to 0) = \mu_{AVG}^{ACC}(V_G \to 0) = \frac{qp_{vo}h}{C_G V_{OFF}}\mu_{bulk} = \frac{1}{1 + \frac{C_G}{2C_S}}\mu_{bulk}. \tag{4.4}$$

Thus, $\mu_{AVG}^{MAX} < \mu_{bulk}$ as found in Fig. 4.3.

The effect of the gate insulator relative dielectric constant ε_{OX} and thickness t_{OX} with respect to μ_{AVG}^{MAX} according to Eq. 4.4 are simulated in Fig. 4.4 and 4.5, respectively. Figure 4.4 (4.5) shows that μ_{AVG}^{MAX} decreases (increases) with increasing ε_{OX} and t_{OX}. Note that these trends are not 'real', i.e., the interface mobility is not actually increasing with decreasing ε_{OX} and increasing t_{OX}; Rather, The increase in

μ_{AVG}^{MAX} is a consequence of the fact that bulk carriers are making a carrier contribution in establishing μ_{AVG}^{MAX}. Thus, the trends shown in Fig. 4.4 and 4.5 are artifacts associated with improperly interpreting depletion-mode TFT electrical characteristics.

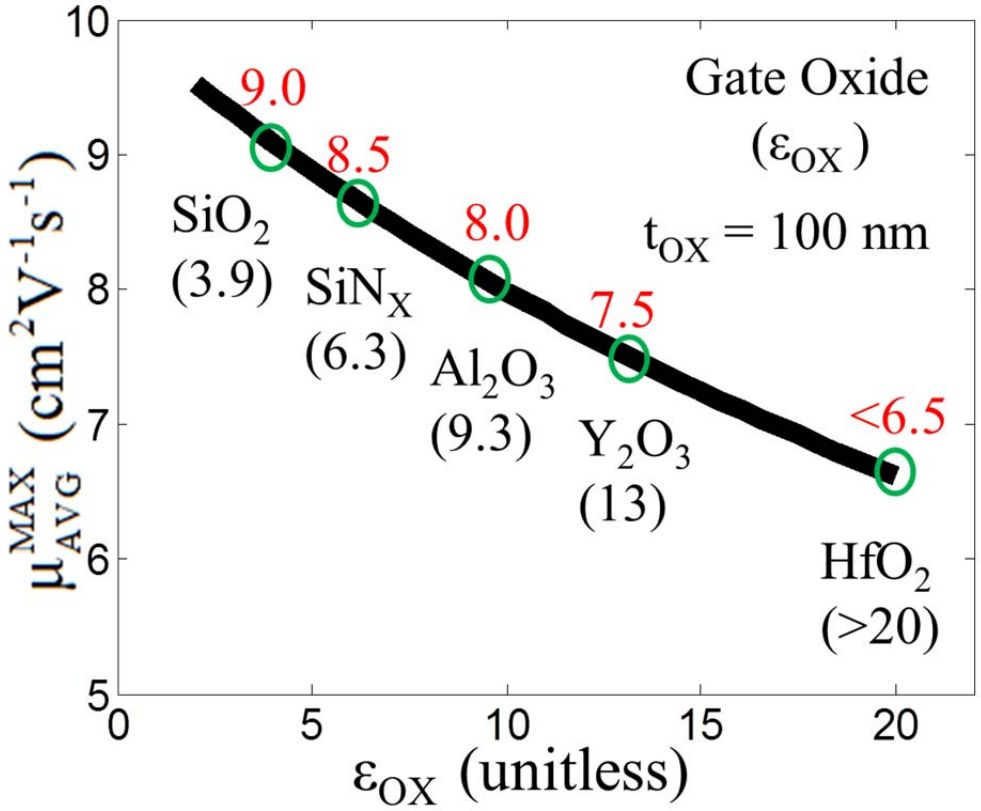


Figure 4.4 Simulated maximum average mobility, μ_{AVG}^{MAX} in the linear region at V_D = -0.1 V as a function of relative permittivity (ε_{ox}). Model parameters used in this simulation are: $\mu_{interface}$ = 1 cm^{2}V^{-1}s^{-1}, μ_{bulk} = 10 cm^{2}V^{-1}s^{-1}, p_{vo} = 10^{18} cm^{-3}, W/L = 10, h = 50 nm, ε_s = 10, and C_{DOS} = 0 Fcm^{-2}. The relative permittivity (in black) and corresponding μ_{AVG}^{MAX} (in red) for some particular dielectric materials are marked.

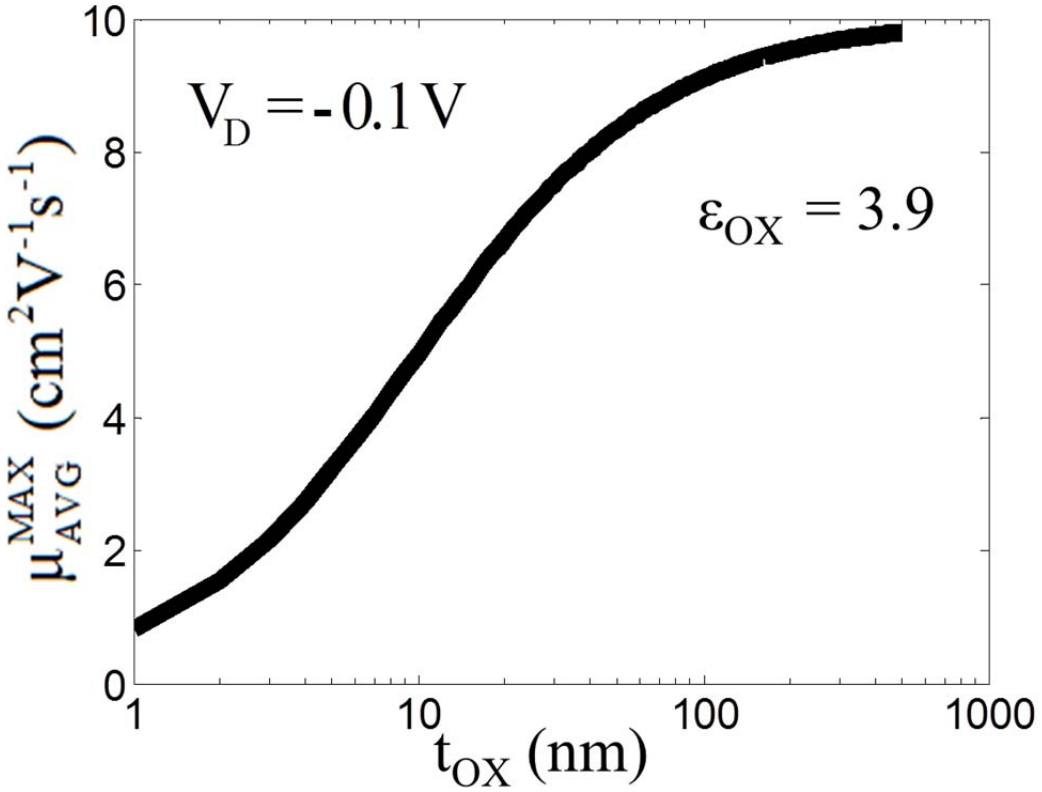


Figure 4.5 Simulated maximum average mobility, μ_{AVG}^{MAX} in the linear region at V_D = -0.1 V as a function of gate insulator thickness (t_{ox}). Model parameters used in this simulation are: $\mu_{interface}$ = 1 $cm^2V^{-1}s^{-1}$, μ_{bulk} = 10 $cm^2V^{-1}s^{-1}$, p_{vo} = 10^{18} cm^{-3}, W/L = 10, h = 50 nm, ε_s = 10, and C_{DOS} = 0 Fcm^{-2}.

Figure 4.6 shows a simulation of μ_{AVG} at a constant overvoltage of -20 V as a function of carrier concentration (p_{vo}). A low hole concentration (<10^{16} cm^{-3}) leads to $\mu_{AVG} \approx \mu_{interface}$, while a high concentration (>$5\times10^{17}$$cm^{-3}$) leads to $\mu_{AVG} \rightarrow \mu_{bulk}$. As indicated in Fig. 4.6, a peak μ_{AVG} of 9.1 $cm^2V^{-1}s^{-1}$ occurs at p_{vo}=8×10^{17} cm^{-3}, and then decreases and saturates at 8.5 $cm^2V^{-1}s^{-1}$ for p_{vo}=1×10^{20} cm^{-3}. It is found that V_{OFF} is 20.4 V when p_{vo}=8×10^{17} cm^{-3} so that V_G = 0.4 V. Thus, the μ_{AVG} mobility peaks indicated in Fig. 4.3 and 4.6 are consistent with one another.

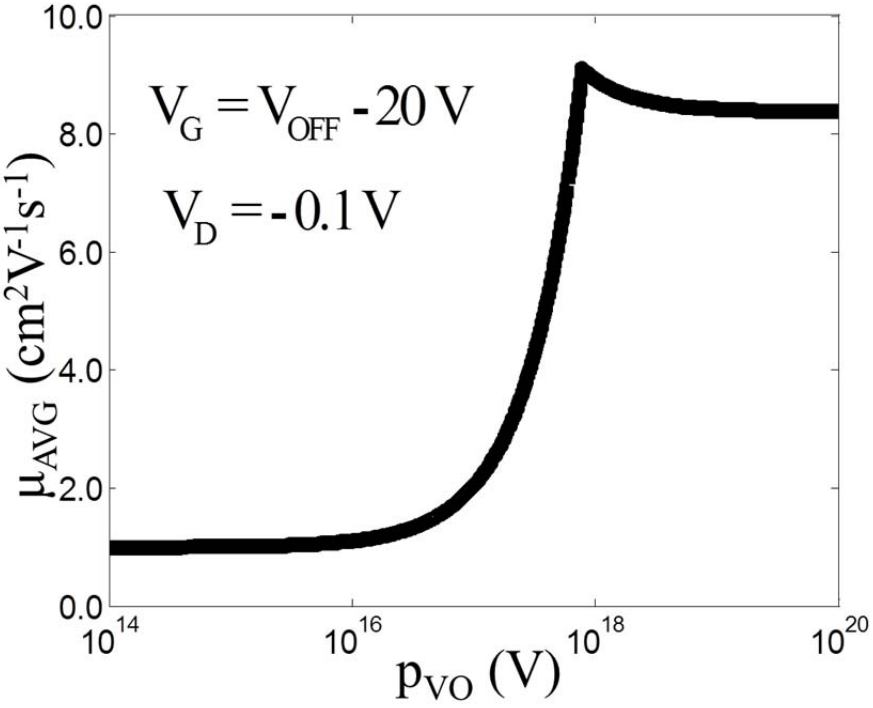


Figure 4.6 Simulated average mobility (μ_{AVG}) as a function of carrier concentration (p_{vo}). Model parameters used in this simulation are: $\mu_{interface}$ = 1 $cm^2V^{-1}s^{-1}$, μ_{bulk} = 10 $cm^2V^{-1}s^{-1}$, W/L = 10, h = 50 nm, ε_s = 10, $C_G = 3.45\times10^{-8}$ Fcm^{-2}, and $V_G = V_{OFF} - 20$ V (V_{OFF} varies as p_{vo} changes).

Figure 4.7 shows log(I_D)-V_G transfer curves for two different channel thicknesses, h = 5 and 50 nm. V_{OFF} decreases from 25.5 to 2.3 V as h is reduced from 50 to 5 nm. Thus, reducing h leads to TFT performance approaching enhancement-mode behavior, but with decreasing current since a smaller fraction of the current is due to the transport of bulk electrons with higher mobility.

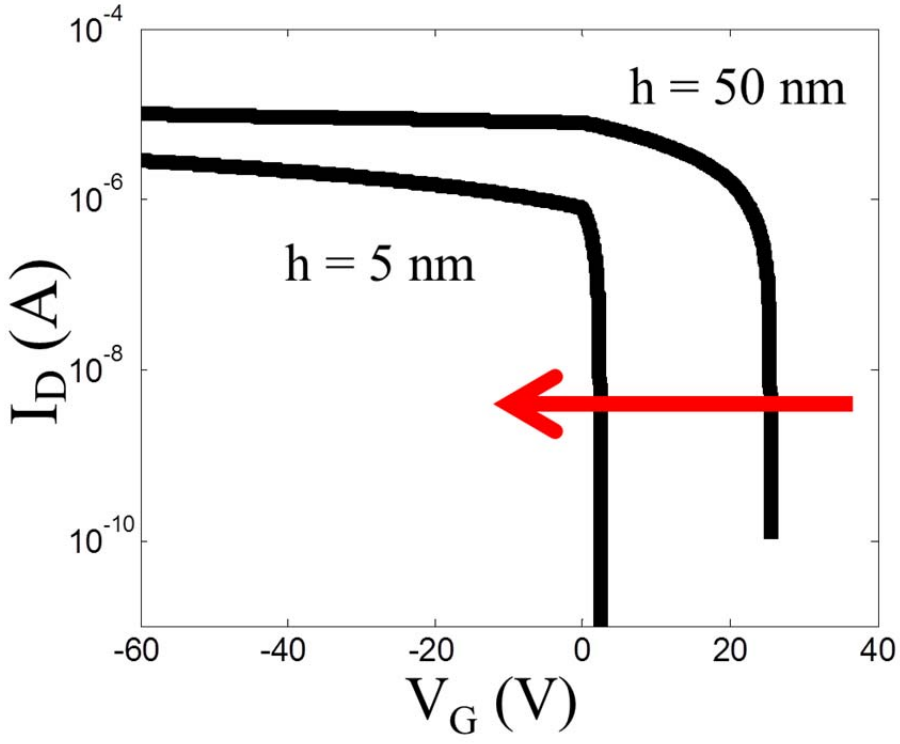


Figure 4.7 Simulated drain current-gate voltage (log (I_D) - V_G) TFT transfer curves for h = 5 (left) and 50 nm (right) at V_D = -0.1 V. Other model parameters used in this simulation are: $\mu_{interface}$ = 1 $cm^2V^{-1}s^{-1}$, μ_{bulk} = 10 $cm^2V^{-1}s^{-1}$, p_{vo} = 1×10^{18} cm^{-3}, W/L = 10, ε_s = 10, C_G = 3.45 $\times10^{-8}$ Fcm^{-2}, and C_{DOS} = 0 Fcm^{-2}.

Figure 4.8 shows a simulation of μ_{AVG} as a function of V_G at various combinations of p_{vo} and h for which the hole density in the channel is constant, i.e., $Q = qp_{vo}h$ = constant. A thinner channel has a larger *apparent* mobility, especially in depletion. This trend is consistent with Eq. 4.4, in which μ_{AVG}^{MAX} increases with decreasing channel thickness h. Thus, once again, the *apparent* mobility trend shown in Fig. 4.8 is an artifact due to improperly interpreting depletion-mode TFT electrical characteristics trend.

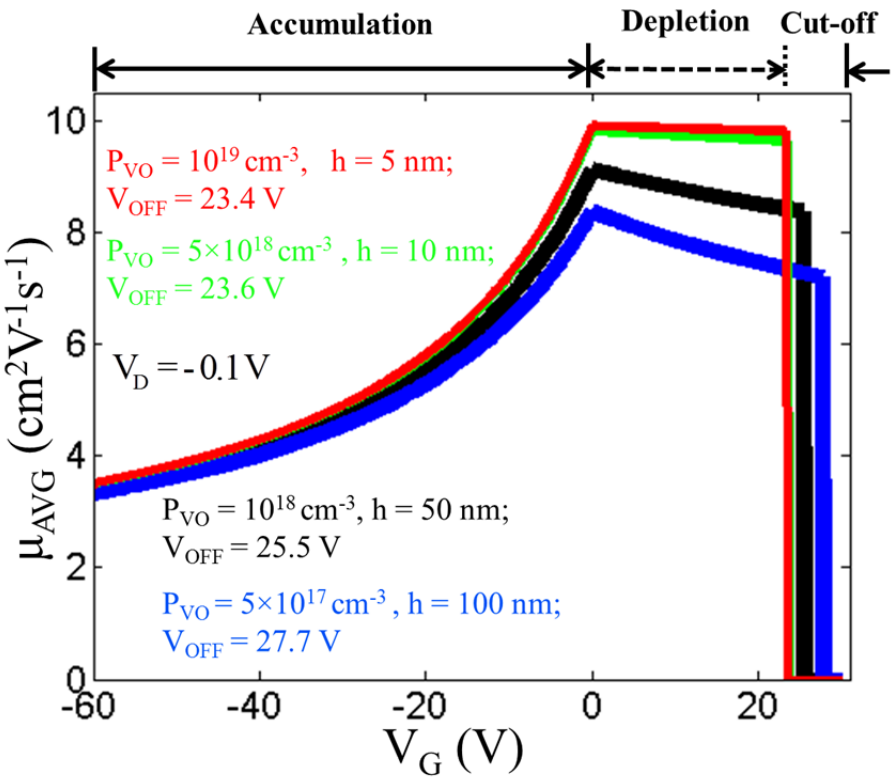


Figure 4.8 Simulated average mobility(μ_{AVG}) as a function of gate voltage (V_G) with different carrier concentration (p_{vo}) and channel thickness (h). Model parameters used in this simulation are: $\mu_{interface}$ = 1 cm^{2}V^{-1}s^{-1}, μ_{bulk} = 10 cm^{2}V^{-1}s^{-1}, W/L = 10, ε_s = 10, $C_G = 3.45\times10^{-8}$ Fcm^{-2}, and C_{DOS} = 0 Fcm^{-2}. For the simulated curves from top to bottom, p_{vo} are 10^{-19}, 5×10^{-18}, 10^{-18}, 5×10^{-17} cm^{-3}, and h are 5, 10, 50, and 100 nm, respectively.

4.2 p-channel, depletion-mode TFT simulation to elucidate experimental data

In this section, several sets of experimental data reported in the literature for p-channel, depletion-mode TFTs are simulated using the comprehensive depletion-mode model.

Figure 4.9 shows measured and simulated I_D -V_D output curves and log(I_D) - V_G transfer curves for a SnO depletion-mode TFT [56]. Simulations are accomplished using the comprehensive depletion-mode model in conjunction with subpinchoff and

off current contributions, using the procedure summarized in Table 3.7. The simulation fit is quite good. Simulated interface and bulk mobilities are 4.8 and 6.75 $cm^2V^{-1}s^{-1}$, respectively, suggesting that the reported channel mobility of 6.75 $cm^2V^{-1}s^{-1}$ is a bit overestimated. A notable and undesirable aspect of the transfer curve shown in Fig. 4.9 (and of all p-channel oxide TFTs reported to date) is the very large off current (i.e., I_{OFF} = 2 nA), leading to very small drain current on-to-off ratios (I_D^{ON-OFF}= 5×10^3 for the transfer curve shown in Fig. 4.9) . I_{OFF} is simulated (see Table 3.7) by specifying that $R_{surface} = 2\times10^9$ Ω since the reported gate current is negligible (~10^{-12} A) and $R_{bulk} \approx 10^{11}$ Ω (assuming a bulk mobility of 6.75 $cm^2V^{-1}s^{-1}$ and a carrier concentration equal to the intrinsic carrier concentration of a ~0.7 eV bandgap semiconductor[4], i.e., $n_i(SnO) = \sim7\times10^{12}$ cm^{-3}). This relatively low value of the simulation parameter $R_{SURFACE}$ is likely a consequence of enhanced leakage associated with grain boundaries in the polycrystalline layer since enhanced leakage is known to occur in polycrystalline silicon TFTs [72].

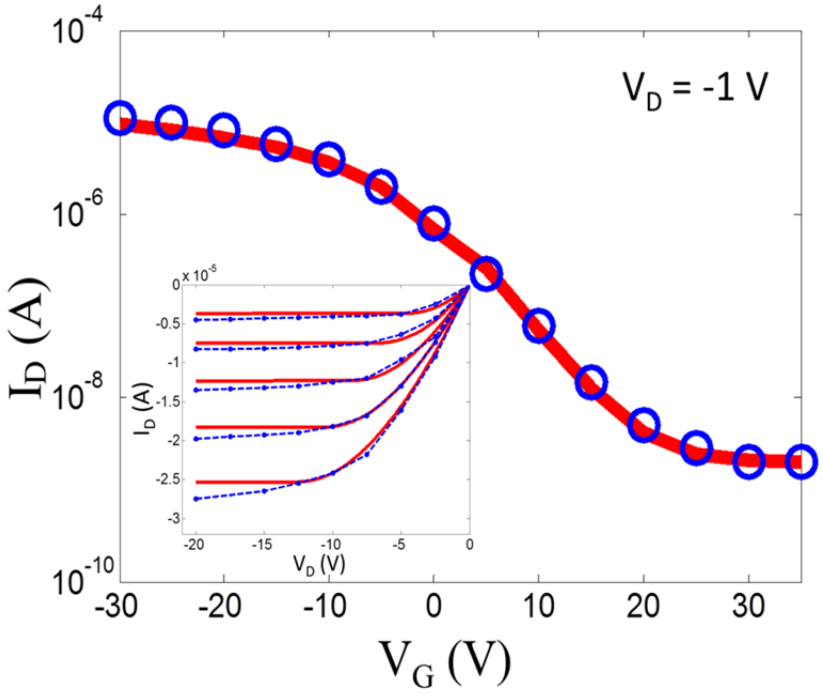


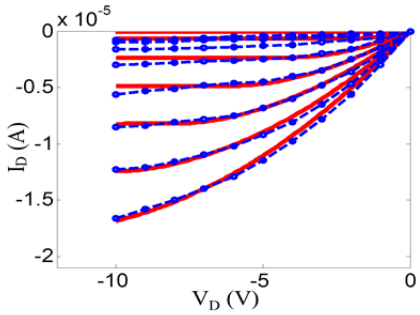
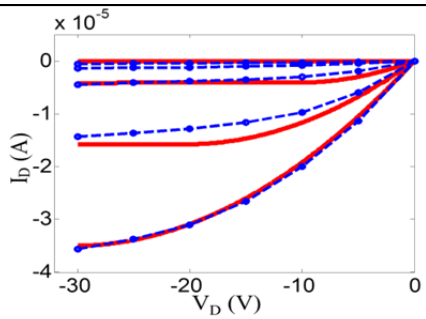
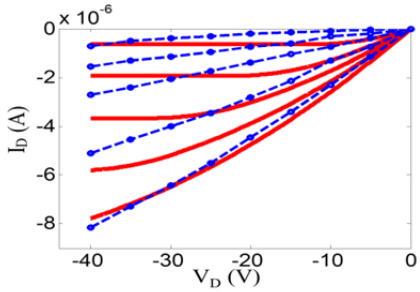
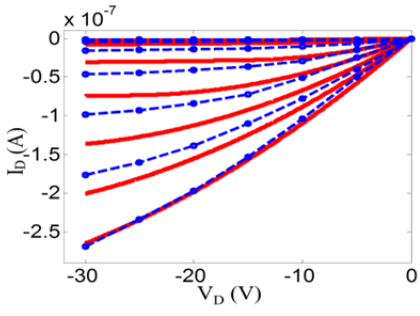
Figure 4.9 Simulated (red solid line) and measured (blue circle) drain current - gate voltage (log (I_D) - V_G) transfer curves for a depletion-mode SnO TFT [56], using the comprehensive depletion-mode model, including subpinchoff current, off-current, and other components. Model parameters used in this simulation are: $p_{vo} = 1\times10^{18}$ cm^{-3}, $\mu_{interface} = 4.8$ $cm^2V^{-1}s^{-1}$, $\mu_{bulk} = 6.75$ $cm^2V^{-1}s^{-1}$, W/L = 1, h = 15 nm, $\varepsilon_s = 10$, $C_G = 5.6\times10^{-8}$ Fcm^{-2}, $C_{DOS} = 6.8\times10^{-6}$ Fcm^{-2} (S = ~7.2 V/decade), $R_{surface} = 2\times10^9$ Ω, and V_D = -1 V. The inset figure is a set of simulated (red solid line) and measured (blue circle) drain current - drain voltage (I_D - V_D) output curves in which V_D = -8, -6, -4, -2, and 0 V from bottom to top.

Table 4.1 shows a comparison between the measured output curves of four p-channel, depletion-mode TFTs reported in the literature and corresponding output curves simulated using the comprehensive depletion-mode model. Reported and simulated mobility estimates are also compared in Table 4.1. Simulations of output curves obtained for SnO channel layers from reference 44 and 53 provide relatively accurately fits to the measured data, indicating that reported mobilities correspond to the 'bulk' mobilities while estimated interface mobilities are ~60% - 70% of their bulk values. The quality of the simulation fits is less satisfying for the output curves

obtained for CuO channel layers from reference 37 and 39, suggesting that these devices may possess some additional non-idealities not accounted for in the simulation. In both of these CuO channel layer cases, simulation suggests that the reported mobilities are significantly overestimated compared to simulated interface mobility estimates.

For the CuO TFT simulation of the data from reference 39, the reported p_{vo} = 3.0×10^{13} cm^{-3} is used in the comprehensive depletion-mode simulation. However, this simulation is of questionable viability since this low of a carrier concentration is expected to exhibit enhancement-mode behavior. In fact, this CuO TFT is indeed reported to operate as an enhancement-mode device in which V_T = -12 V, and V_{ON} = 1 V. Thus. It is more appropriate to simulate this enhancement-mode CuO TFT using the square-law model. Figure 4.10 displays a output curve comparison between the enhancement-mode CuO TFT of reference 39 as simulated using the square-law and the comprehensive depletion-mode model. Although the square-law fit is considered more appropriate since the CuO TFT is enhancemnet-mode, the comprehensive depletion-mode fit is almost indentical to that of the square-law fit and the estimated mobilities are quite close, i.e., 0.0008 $cm^2V^{-1}s^{-1}$ and 0.0012 $cm^2V^{-1}s^{-1}$ for the comprehensive depletion-mode and square-law fit, respectively.

Table 4.1 Measured and simulated output curves and mobility estimates for p-channel, depletion-mode TFTs, reported in the literature with SnO[44,53] and CuO[37,39]channel layers.

Measured and simulated output curves [4-7]	Reported mobility ($cm^2/V\cdot s$)	Simulated mobility ($cm^2/V\cdot s$)	Simulated carrier density(cm^{-3})
 [44]	$\mu_{FE}=1.3$	$\mu_{bulk}=1.3$ $\mu_{interface}=0.9$	$p_{vo}=2.5\times10^{17}$
 [53]	$\mu_{FE}=1.2$	$\mu_{bulk}=1.2$ $\mu_{interface}=0.75$	$p_{vo}=5.0\times10^{16}$
 [37]	$\mu_{FE}=0.4$	$\mu_{bulk}=0.12$ $\mu_{interface}=0.05$	$p_{vo}=3.0\times10^{17}$
 [39]	$\mu_{FE}=3.9$	$\mu_{bulk}=3.9$ $\mu_{interface}=8\times10^{-4}$	$p_{vo}=3.0\times10^{13}$

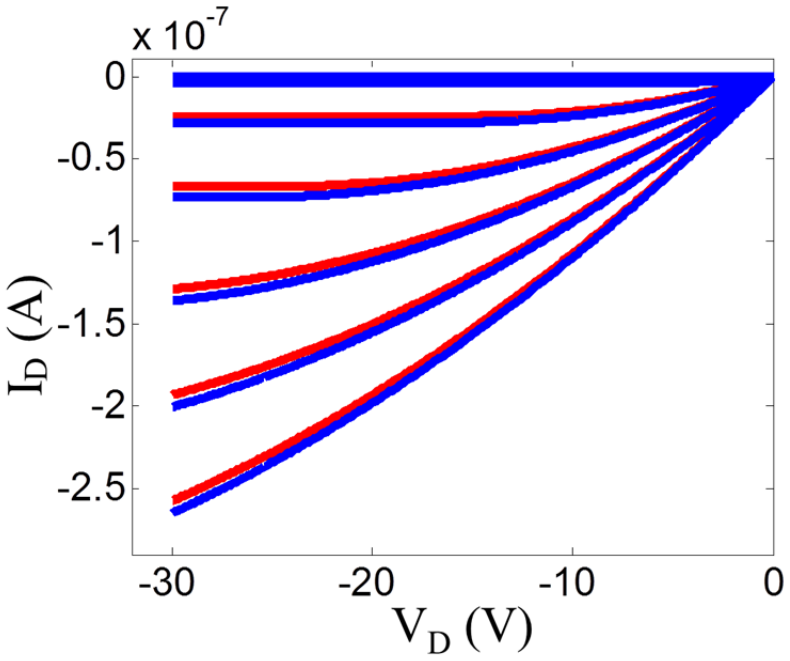


Figure 4.10 Simulated drain current - drain voltage (I_D - V_D) output curves in which V_D = -55, -45, -35, -25, -15 and -5 V from bottom to top, using square-law model and comprehensive depletion-mode model. Model parameters used in the square-law model are: V_T = -12 V, μ = 0.0012 $cm^2V^{-1}s^{-1}$, W/L = 3.3, and $C_G = 8.0\times10^{-8}$ Fcm^{-2}. Extracted $n_{to} = 1.25\times10^{17}$ cm^{-3} since V_{ON} = 1 V. Model parameters used in the comprehensive depletion-mode model are: $p_{vo} = 3\times10^{13}$ cm^{-3}, $\mu_{interface} = 0.0008$ $cm^2V^{-1}s^{-1}$, $\mu_{bulk} = 3.9$ $cm^2V^{-1}s^{-1}$, W/L = 3.3, h = 40 nm, $\varepsilon_s = 7.1$, $C_G = 8.0\times10^{-8}$ Fcm^{-2}.

Figure 4.11 illustrates the utility of the comprehensive depletion-mode model in assessing TFT performance, even for a TFT of very poor quality. Measured and simulated transfer and output curves for a Cu_3SbS_4 TFT in an early stage of development are given in Fig. 4.11. Since this device cannot be turned off and does not exhibit saturation, it is more appropriately classified as a nonlinear, voltage-controlled resistor rather than a TFT. In any event, although this device is of very poor quality, it can be accurately simulated using the comprehensive depletion-mode model. Moreover, the estimated model parameters are revealing. Best fits are obtained assuming $p_{vo} = 4.0\times10^{18}$ cm^{-3}, $\mu_{interface} = 0.05$ $cm^2V^{-1}s^{-1}$, $\mu_{bulk} = 0.45$ $cm^2V^{-1}s^{-1}$[1]. The simulated result of p_{vo} is close to the bulk concentration of 1.7×10^{18} cm^{-3} as

obtained from Hall measurement (film thickness is 1 μm). Improvement of this material for p-channel TFT applications requires reducing the hole concentration by about three orders of magnitude. Since this development task appears daunting, and the estimated value of $\mu_{interface}$ is so low, further development of this material as a TFT channel layer was not pursued. As a final note, although it cannot be claimed that p_{vo}, $\mu_{interface}$, and μ_{bulk} are accurately and uniquely determined, there is very little leeway in modifying these simulation parameter if accurate fit to measured transfer and output curves is to be obtained within the framework of the comprehensive depletion-mode model.

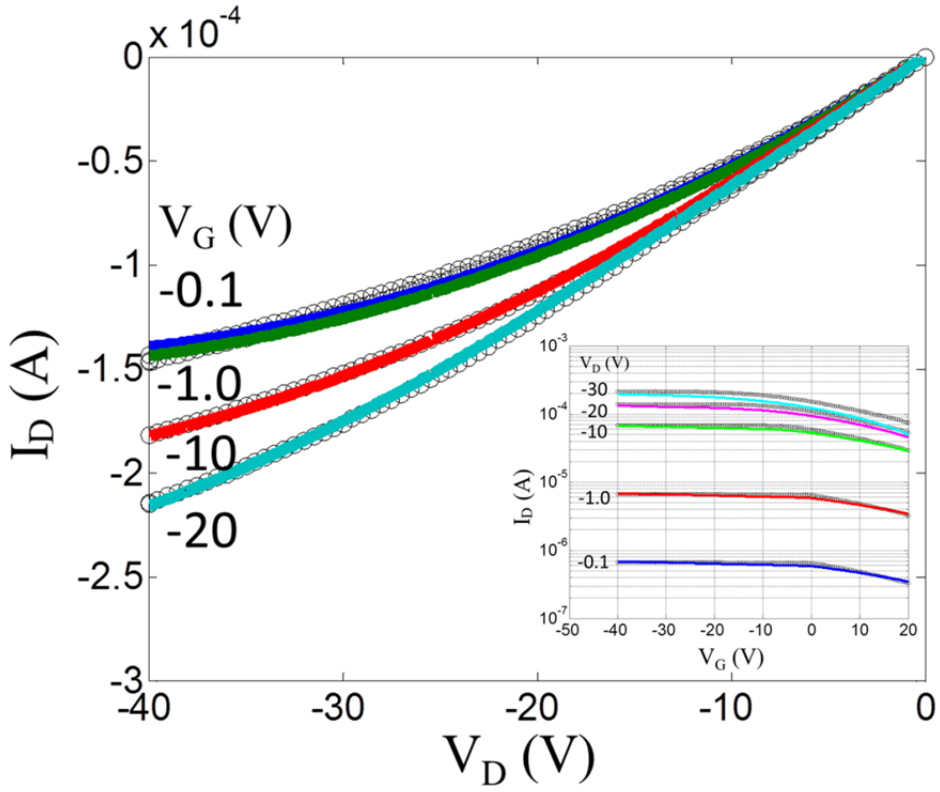


Figure 4.11 Measured drain current - drain voltage (I_D - V_D) output curves (open circles) for Cu_3SbS_4 TFT and simulated output curves (continuous lines) using the comprehensive depletion-mode model. V_G from top to bottom is -0.1, -1.0, -10, and -20 V, respectively. Model parameters used in this simulation are: $p_{vo} = 4.0\times10^{18}$ cm^{-3}, $\mu_{interface} = 0.05$ $cm^2V^{-1}s^{-1}$, $\mu_{bulk} = 0.45$ $cm^2V^{-1}s^{-1}$, W/L = 10, h = 22 nm, $\varepsilon_s = 18.5$, $C_G = 3.45\times10^{-8}$ Fcm^{-2}. The inset figure is a set of measured and simulated drain current-gate voltage ($\log(I_D)$ - V_G) transfer curves in which V_D = -0.1, -1, -10, -20, and -30 V from bottom to top.

4.3 n-channel, depletion-mode TFT simulation to elucidate experimental data

In this section, one set of experimental data reported in the literature for an n-channel, depletion-mode TFT is simulated using the comprehensive depletion-mode model.

Figures 4.12 shows measured and simulated I_D-V_D output curves for a ZnInO depletion-mode TFT [73]. The simulation result (red curves) fits experimental data

(blue circles) well at V_G = -8 and -6 V, in which the TFT operates in strong depletion, and it also provides a close fit to experimental at V_G = -4, -2 and 0 V. From the simulated output curves, carrier concentration n_{co} and bulk mobility μ_{bulk} are extracted, and are equal to 3.65×10^{17} cm^{-3} and 55 $cm^2V^{-1}s^{-1}$, respectively, which are quite close to the reported p_{vo} of 7.1×10^{17} cm^{-3} and μ_{INC} of 45~55 $cm^2V^{-1}s^{-1}$. Notice that interface mobility $\mu_{interface}$ in this simulation cannot be accurately estimated due to the lack of experimental data in accumulation (V_G > 0 V).

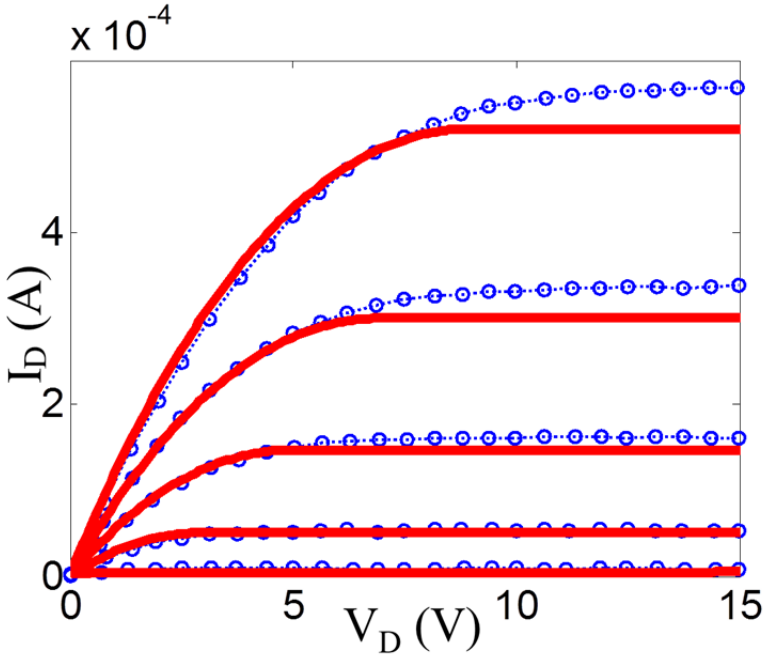


Figure 4.12 Simulated (red solid lines) and measured (blue circles) drain current - drain voltage (I_D - V_D) output curves in which V_D = 0, -2, -4, -6, -8, and -10 V from top to bottom for a depletion-mode ZnInO TFT. Model parameters used in this simulation are: $n_{co} = 3.65\times10^{17}$ cm^{-3}, μ_{bulk} = 55 $cm^2V^{-1}s^{-1}$, W/L = 4.7, h = 85 nm, ε_s = 10, and $C_G = 8.0\times10^{-8}$ Fcm^{-2}.

Figure 4.13 shows an I_D-V_G transfer curve simulation for a ZnInO depletion-mode TFT. Simulations are accomplished using the comprehensive depletion-mode model in conjunction with subpinchoff and off current contributions. The simulation

succeeds in fitting the measured data quite well as evident from the fact that the simulated curve (red) covers most of the measured data points (blue circles). Only a few simulation data points are shown in Fig. 4.13 (the V_G step size is large, i.e., 3 V) in order to avoid a discontinuity in I_D near V_{PO} (-9 V), due to inclusion of subpinchoff current, as discussed in Section 3.4.1. When a small V_G step size (i.e., 0.1 V) is used, as shown in the insert of Fig. 4.13, the I_D discontinuity is clearly evident. The viability of output curve estimates of n_{co} and μ_{bulk} (Fig. 4.12) are further validated by the good transfer curve agreement between simulated and measured data. Undertaking the $I_D - V_G$ transfer curve simulation allows estimation of the channel layer density of states capacitance $C_{DOS} = 1.0\times10^{-6}$ Fcm^{-2} and the channel layer surface resistance $R_{surface} = 5\times10^{10}$ Ω.

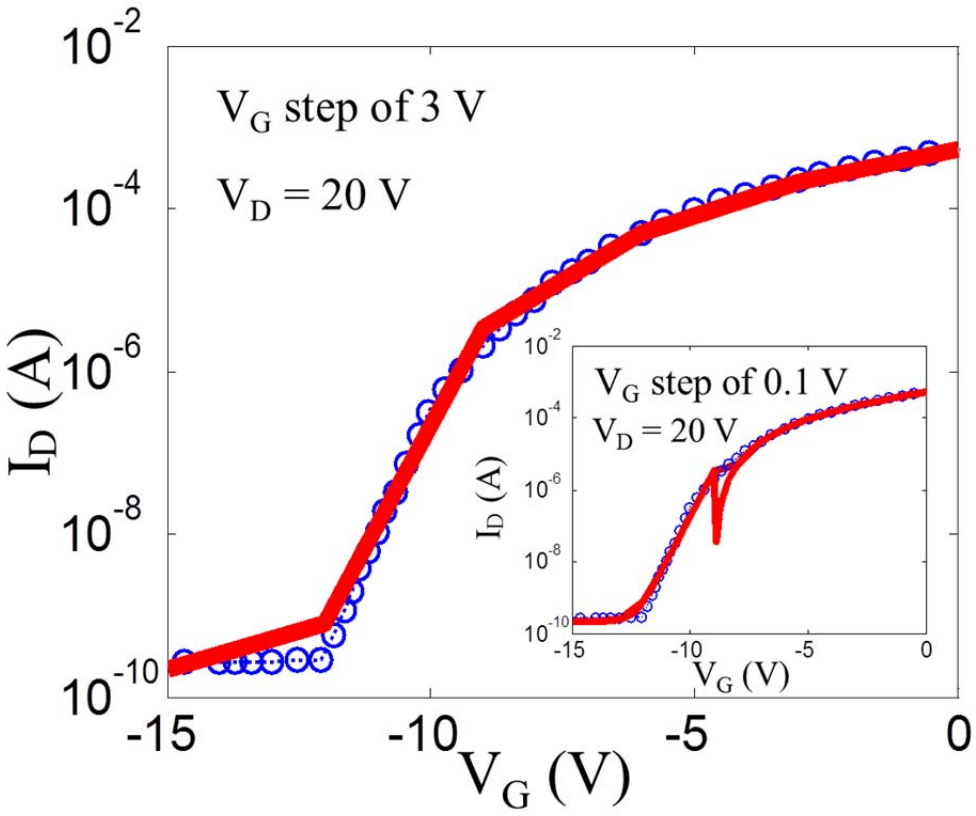


Figure 4.13 Simulated (red solid line) and measured (blue circles) drain current - gate voltage (log (I_D) - V_G) transfer curve for a depletion-mode ZnInO TFT, using the comprehensive depletion-mode model, including subpinchoff current, off-current, and other components. Model parameters used in this simulation are: $n_{co} = 3.65\times10^{17}$ cm^{-3}, $\mu_{bulk} = 55$ $cm^2V^{-1}s^{-1}$, W/L = 4.7, h = 85 nm, $\varepsilon_s = 10$, $C_G = 8.0\times10^{-8}$ Fcm^{-2}, $C_{DOS} = 1.0\times10^{-6}$ Fcm^{-2} (S = ~0.8 V/decade), $R_{surface} = 5\times10^{10}$ Ω, V_D = 20 V. The insert shows a simulated and a measured transfer curve using identical simulation parameters, except for a simulation V_G step size of 0.1 V.

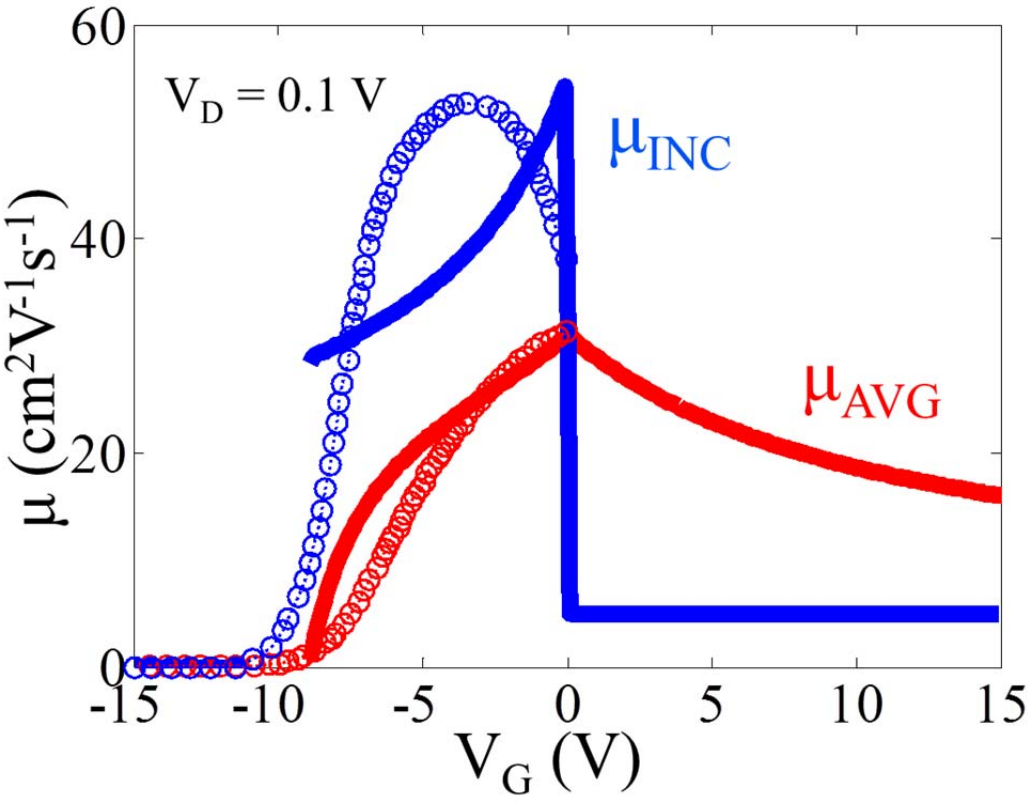


Figure 4.14 Simulated (solid line) and measured (circles) average mobility, μ_{AVG} (red) and incremental mobility, μ_{INC} (blue) as a function of gate voltage (V_G) for a depletion-mode ZnInO TFT. Model parameters used in this simulation are: n_{co} = 3.65×10^{17} cm^{-3}, μ_{bulk} = 55 $cm^2V^{-1}s^{-1}$, $\mu_{interface}$ = 5 $cm^2V^{-1}s^{-1}$, W/L = 4.7, h = 85 nm, ε_s = 10, $C_G = 8.0\times10^{-8}$ Fcm^{-2}, $R_{surface} = 5\times10^{10}$ Ω, and V_D = 0.1 V.

A channel mobility comparison of the simulated and the measured depletion-mode ZnInO TFT is provided in Fig. 4.14. In order to simulate the incremental mobility μ_{INC} and average mobility μ_{AVG}, a small V_D is used and the same simulation parameters as employed in Fig. 4.12 are used, i.e., $n_{co} = 3.65\times10^{17}$ $cm^{-3}$and μ_{bulk} = 55 $cm^2V^{-1}s^{-1}$. In addition, in an attempt to account for mobility trends in accumulation, it is assumed that $\mu_{interface}$ = 5 $cm^2V^{-1}s^{-1}$. As shown in Fig. 4.14, simulated and measured μ_{AVG} curves are somewhat similar to one another and show the same peak mobility of 30 $cm^2V^{-1}s^{-1}$ at V_G = 0 V. The simulation indicates that μ_{AVG} is expected to slowly

decrease towards $\mu_{interface}$ = 5 $cm^2V^{-1}s^{-1}$ as V_G increases in accumulation. In contrast, the agreement between simulated and measured μ_{INC} curves is much less satisfying. Notably, the simulated (measured) μ_{INC} curve exhibits positive (negative) curvature and a peak mobility of 55 $cm^2V^{-1}s^{-1}$ that occurs at $V_G \approx 0$ V ($V_G \approx -3$ V). Furthermore, while the measured μ_{INC} curve decreases over the gate voltage range V_G = -3 – 0 V, the simulated μ_{INC} curve decreases abruptly to $\mu_{interface}$ = 5 $cm^2V^{-1}s^{-1}$ at V_G = 0 V. It is likely that observed decrease in μ_{INC} vs V_G approaches 0 V arises as a consequence of either interface roughness scattering or series resistance [18], neither of which are accounted for in the present model.

5 CONCLUSIONS AND RECOMMENDATION FOR FUTURE WORK

5.1 Conclusions

The objective of this thesis is to modify and extend the applicability of the comprehensive depletion-mode model and to employ it to simulate depletion-mode TFTs. The major modification of the comprehensive depletion-mode model accomplished herein is distinguishing between the interface mobility $\mu_{INTERFACE}$ and bulk mobility μ_{BULK}. The comprehensive depletion-mode model is extended from n- to p-channel behavior, and is also extended account for subpinchoff current, the transition from subpinchoff to above-pinchoff, and off current.

Using the modified comprehensive depletion-mode model, average, incremental, field-effect, effective, and saturation mobilities for depletion-mode TFT were derived, and several sets of experimental data reported in the literature were simulated. From the simulation results, conclusions are presented as following:

1. Accurate fitting of measured depletion-mode TFT output and transfer curves can be employed to extract estimates of carrier concentration in the channel, μ_{BULK} and $\mu_{INTERFACE}$.
2. Because both μ_{BULK}, and $\mu_{INTERFACE}$ contribute to establishing the channel mobility, the interface mobility is almost always overestimated in p-channel, depletion-mode TFTs.

5.2 Recommendations for Future Work

Although the comprehensive depletion-mode model provides insight into the operation of depletion-mode TFTs and elucidates mobility artifacts in depletion-mode TFTs, there are still areas where it can be improved.

1. Series resistance modeling. Simulated output curves did not always provide an accurate fit to measured data (see Table 4.1), suggesting that additional non-idealities are not accounted for in the simulation. Series resistance is a notable unaccounted for non-ideality. Inclusion of series resistance in the comprehensive depletion-mode model would improve the accuracy of output curve fitting.
2. Technology computer-aided design (TCAD) modeling. TCAD tools complement comprehensive depletion-mode modeling. Concomitantly employing both types of modeling could provide new insight into subtle aspects of TFT operation.
3. Smoothing functions. Although the reciprocal method [67-68] was adopted for combining diffusion and drift currents to account for subthreshold (subpinchoff), development of a single equation smoothing function [69] , to describe depletion-mode TFT characteristics across all operating regions is desirable in order to achieve a more robust model.

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