AN ABSTRACT OF THE THESIS OF

Wei Tjan Lim (Richard) for the degree of Master of Science in Electrical and Computer Engineering presented on May 29, 1996. Title: Suppression of Substrate Noise in a Mixed-Signal CMOS Integrated Circuit.

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Leonard Forbes

Substrate switching noise is becoming a concern as integrated circuits get larger and speeds get faster. Mixed-mode integrated circuits are especially affected as the substrate noise interferes with sensitive analog circuits resulting in limited signal to noise ratios. This thesis serves to study the cause of the noise at the point where it is generated to the way it propagates to the analog circuits, and presents several approaches to reduce the switching noise. In addition, it examines the substrate impedance as being a key element to successful and reliable design for low-noise CMOS mixed-signal integrated circuits. Utilizing the substrate lead inductance and current-variable capacitances through the use of guard ring diodes, resonant frequencies which provide a low impedance path to ground are created. These can be tuned to coincide with problematic noise frequency components or to cancel the pin and package resonance, thus suppressing noise and improving reliability.

Suppression of Substrate Noise in a Mixed-Signal CMOS Integrated Circuit

by

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Going through graduate school is not without much sweat and sacrifice for which I acknowledge Jesus Christ for unfailingly carrying me throughout this phase of life's journey.

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SUPPRESSION OF SUBSTRATE NOISE IN A MIXED-SIGNAL CMOS INTEGRATED CIRCUIT

1. Introduction

The definition of mixed-signal integrated circuit can be categorized into devices having a majority portion of analog circuitry with some digital circuitry for control (in A/D, D/A, Phase-Locked Loops), or a large portion of digital circuitry (microprocessor) with minimal analog circuitry for peripheral interactions. With the advancement in VLSI technology, we see more and more mixed-signal circuits being fabricated on the same chip for cost and efficiency reasons [1-4]. ICs that incorporate mixed-signal circuits include disk drives, bar code readers, digital audio/video processing etc.

The push for these high-speed, low power, and low noise mixed-signal ICs have led to crosstalk being a concern and a pitfall in high performance ICs. This resulted in several published research papers that study the various aspects of noise generation and propagation through the substrate [5-10]. The problem goes back to the fundamental difference in the operation of digital and analog circuits. Digital circuits are known to have high noise immunity due to the binary representation of two discrete fixed potentials, namely Vdd and ground. Analog circuits, on the other hand, are capable of taking all sets of values without the discrete representation in time. When these two operations are combined onto one wafer sharing the same substrate, switching noise from the digital side,which is caused by the rise and fall times of the clock signals or the

charging/discharging of node capacitances, finds its way into sensitive analog sections through interconnect or transistor capacitive couplings to and through the substrate. They result in ground bounce and false data, being typically several orders of magnitude higher than the thermal and flicker noise which is associated with the physical silicon devices[11]. There is cause for concern as it limits the accuracy of the analog signals to typically 16 bits [12]. Not to be confused with thermal noise (white) or flicker noise (1/f frequency dependent), switching noise in general is broad-band, possessing mainly high frequency components. However, to a first order, the dominant frequency component lies mainly in the rise and fall times of the clock edges or the charging/discharging times of the various capacitive nodes, and hence the switching frequencies. We will look at this in more detail in Chapter 4.

Well known noise reductions include (i)separate power supply and ground bus for digital and analog sections, (ii)decoupling capacitors to provide local current to switching circuits, thus minimizing disturbances to the power lines [3,11,13], (iii)slowing down the rise and fall times of digital signals and/or special circuit design to reduce the $\partial I/\partial t$ and simultaneous switching noise [9,14]. These can be categorized mainly in isolating the noise from the sensitive circuits or reducing the noise right at the source. This thesis addresses the isolation aspect and suggests a scheme in suppressing it, thus improving reliability and elevating the signal-to-noise ratios of analog circuits.

2. Background

2.1 Substrate Noise

Substrate noise has been studied quite extensively where the problem lies in the capacitive coupling from the source/drain diffusions, as well as interconnects, power/ground bus contacts, and well capacitance coupling to the substrate[15]. Perturbations in the substrate due to switching result in threshold voltage variations and capacitive coupling back to sensitive analog source/gate/drain terminals which limits performance of analog signal processing and data conversion circuits [4,16]. Figure 2.1 shows a typical mixed-signal integrated circuit structure and the various noise coupling possibilities into the substrate. Figure 2.2 is the cross-section profile of the integrated circuit. Su et.al [5] found that substrate doping levels have a lot to do in the way the noise currents travel. For lightly doped substrates, the majority of the injected noise current tends to travel on the die surface due to the absence of a low-resistance bulk. Therefore, physical separation and guard rings in the vicinity of the digital as well as analog sections are the solutions to suppressing switching transients in the sensitive analog circuits. In the case of the more common trend of a heavily doped substrate where there is a low resistance bulk with an epitaxial layer, noise current travels through the epitaxial layer and vertically into the bulk, and progresses horizontally in the bulk, eventually showing up vertically through the epitaxial layer and into the substrate contact. As a consequence, physical separation doesn't cause significant noise reduction as long as it is at least four times the thickness of the epi-layer, and so the bulk can be treated as a single node [5].

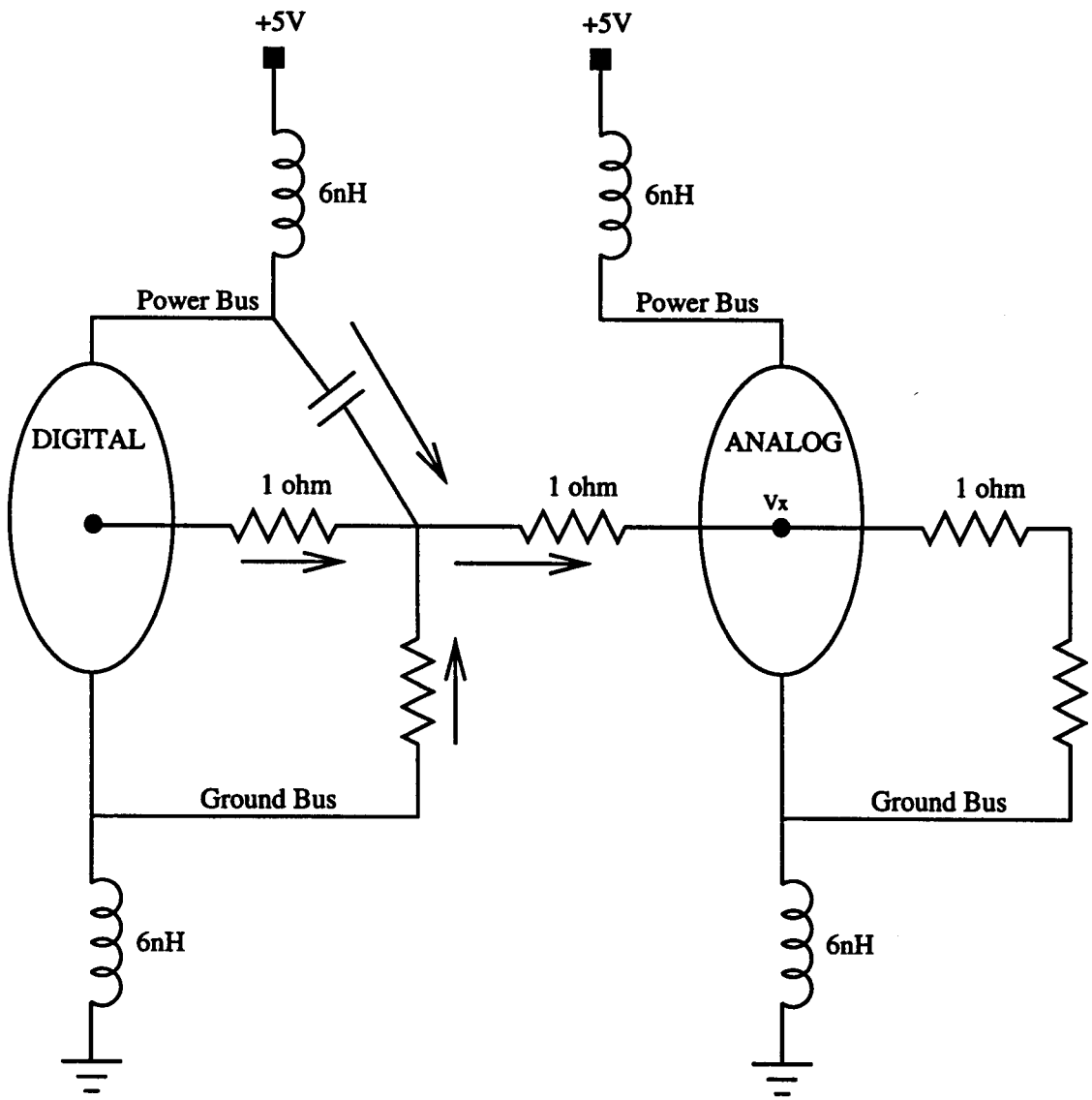

Fig. 2.1: Noise Coupling possiblilities in a Mixed-Signal Integrated Circuit

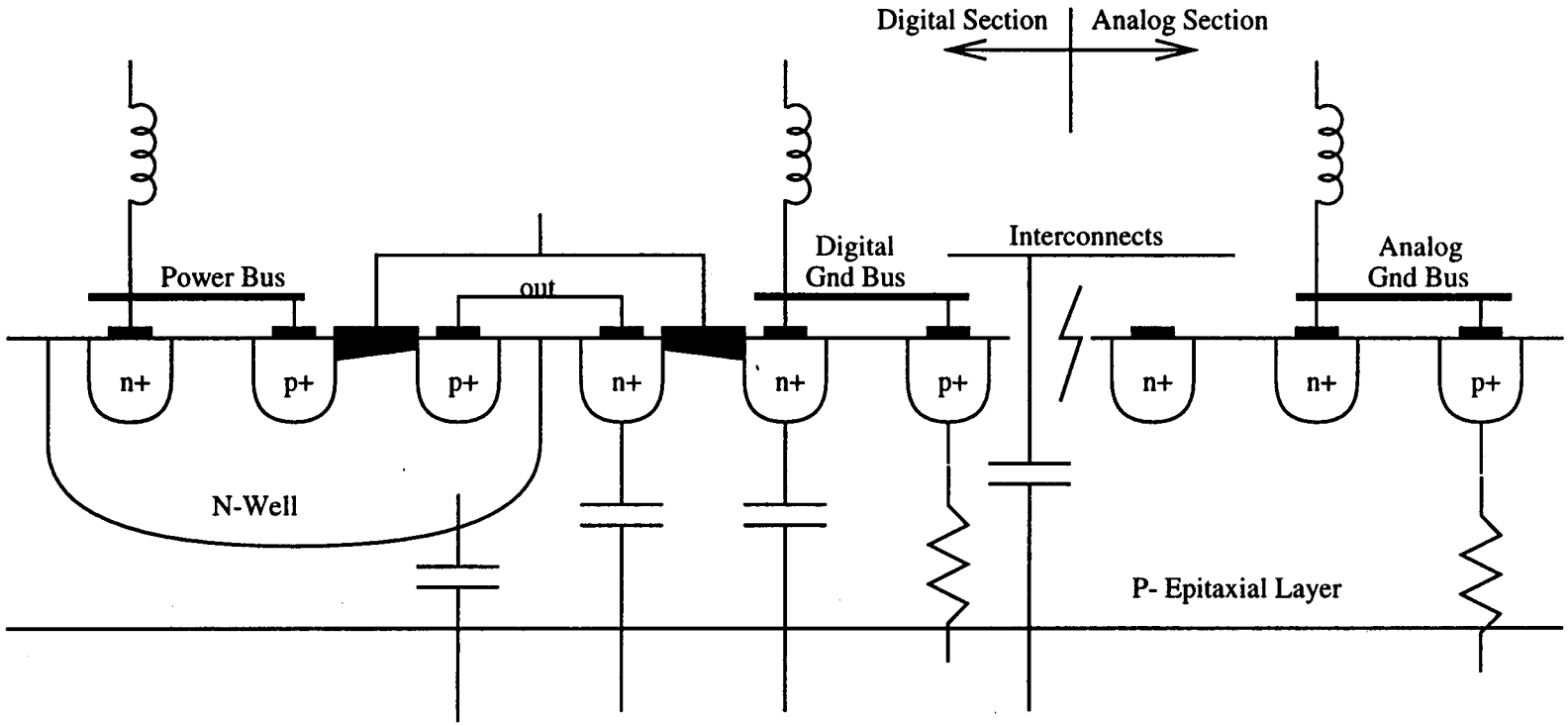

Fig. 2.2: Cross-Section Profile of a Mixed-Signal Integrated Circuit

The focus from this point onwards will then be on epi-substrate low bulk resistance CMOS technology. Evidently, noise suppression can be achieved by either reducing the strength of the noise at its source or/and silencing the heavily-doped bulk.

2.2 Reducing Noise at its Source

Noise voltage is being generated at the power/ground bus during switching which satisfies the equation $V_n = L\partial I/\partial t$, where L is the effective lumped inductance from bond-wires, package plane and package pins, and $\partial I/\partial t$ is the current spike that is the result of overlap current and the displacement(charging/discharging) current from the power bus or into the ground bus during the time of switching. Overlap current is defined as the current that flows directly from Vdd to ground when both p- & n- channel transistors are in the saturation region. The displacement currents simply refer to the current that is used to charge/discharge the node capacitances. Usually, the noise contribution due to the overlap current is insignificant compared to the displacement currents [17]. The amplitude and slope of the spike are, however, related to the sizes of the transistors by

$$C_{load}V_{dd} = I_{ave}t_{r/f} = I_{ave}RC_{load} \qquad (2.1)$$

where $t_{r/f}$ corresponds to the rise/fall times of the switching node, and R is inversely proportional to the transistor sizes and will vary throughout the charge/discharge cycle. I_{peak} is thus equal to V_{dd}/R where R has the minimal resistance when the transistor is in saturation. This can be a problem especially in output drivers as they are capable of sourcing/dumping milliamps of current from/onto the power/ground bus in minimal time.

This V_{dd} / V_{ss} bounce is the cause of false data and unreliability especially when output drivers switch simultaneously. Circuit techniques are thus employed to increase the width of the current spike [9] as shown in figure 2.3. Yet another circuit technique that serves to reduce this current spike is the folded source-coupled logic (FSCL) illustrated in figure 2.4. This circuit technique utilizes differential current steering circuits in the logic stages which serves to maintain a more or less equal current pull at all times.

2.3 Silencing the Noise Transmission Medium (bulk)

Guard rings are substrate contacts strapped with metal that completely enclose a given region. They serve to collect the minority carriers present in the substrate from causing latch-up and inducing noise to the region of interest. Conventionally, they are inserted around sensitive analog circuits or around digital circuits to collect noise transients. Noise reduction is approximately 30% [5]. Apart from guard rings, noise isolation can be such a big deal as to motivate separate dice for the digital and analog sections [25-26] or using advance SOI (silicon on insulator) with trench oxide as shown in figure 2.5. The latter is only effective for noise at low frequencies (< 300MHz).

The key to a silent substrate node would be to study the impedance of the substrate. This is not simply a matter of substrate lead inductance of sL. In actual fact, a typically dense mixed-mode integrated circuit would have substantial stray and well capacitances that couple the substrate to the power supply and ground bus, thus resulting

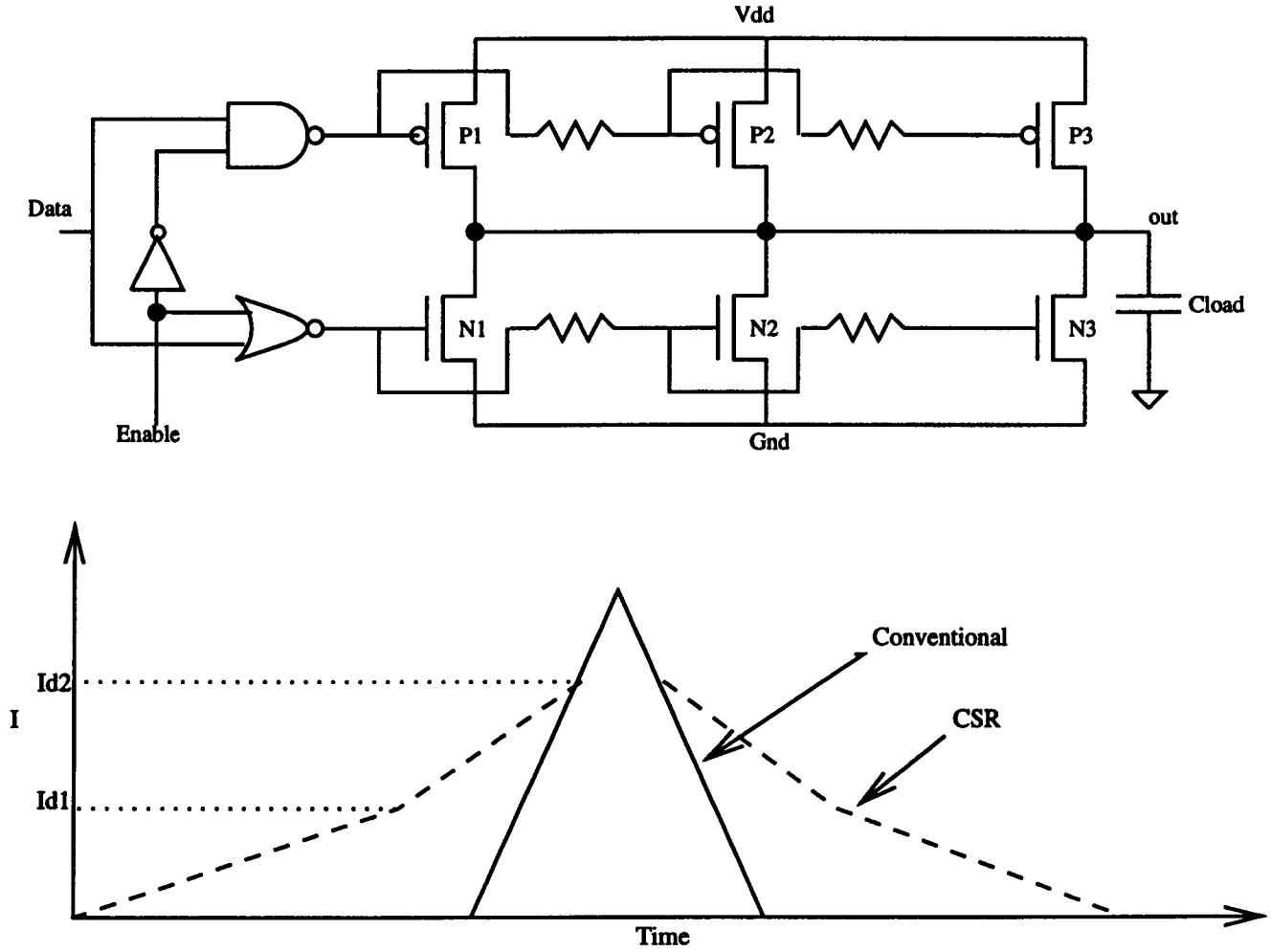

Fig. 2.3: (a) Controlled Slew Rate (CSR) Output Driver;
(b) Current Switching Characteristics

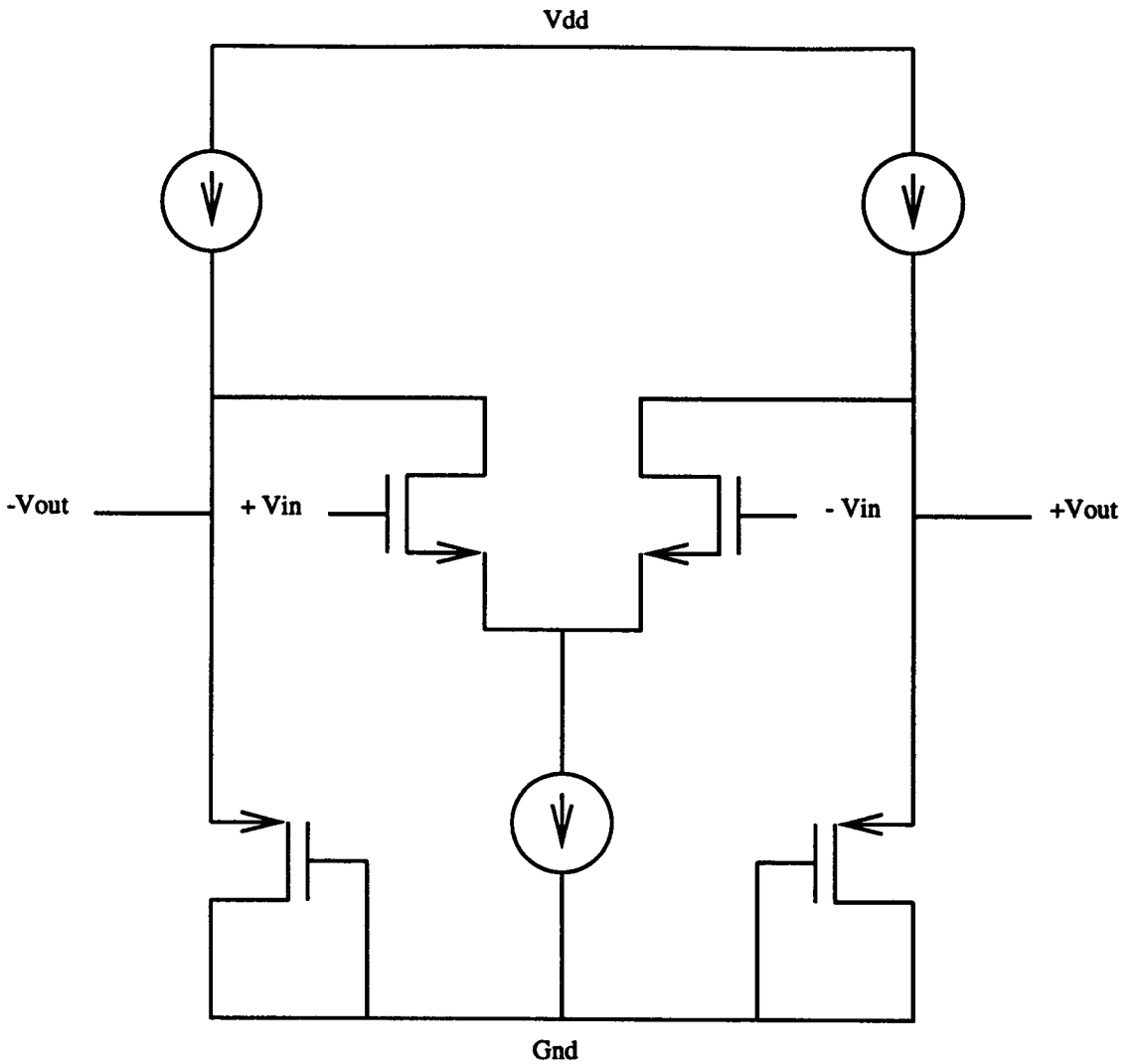

Fig. 2.4: CMOS Folded Source-Coupled Logic Inverter

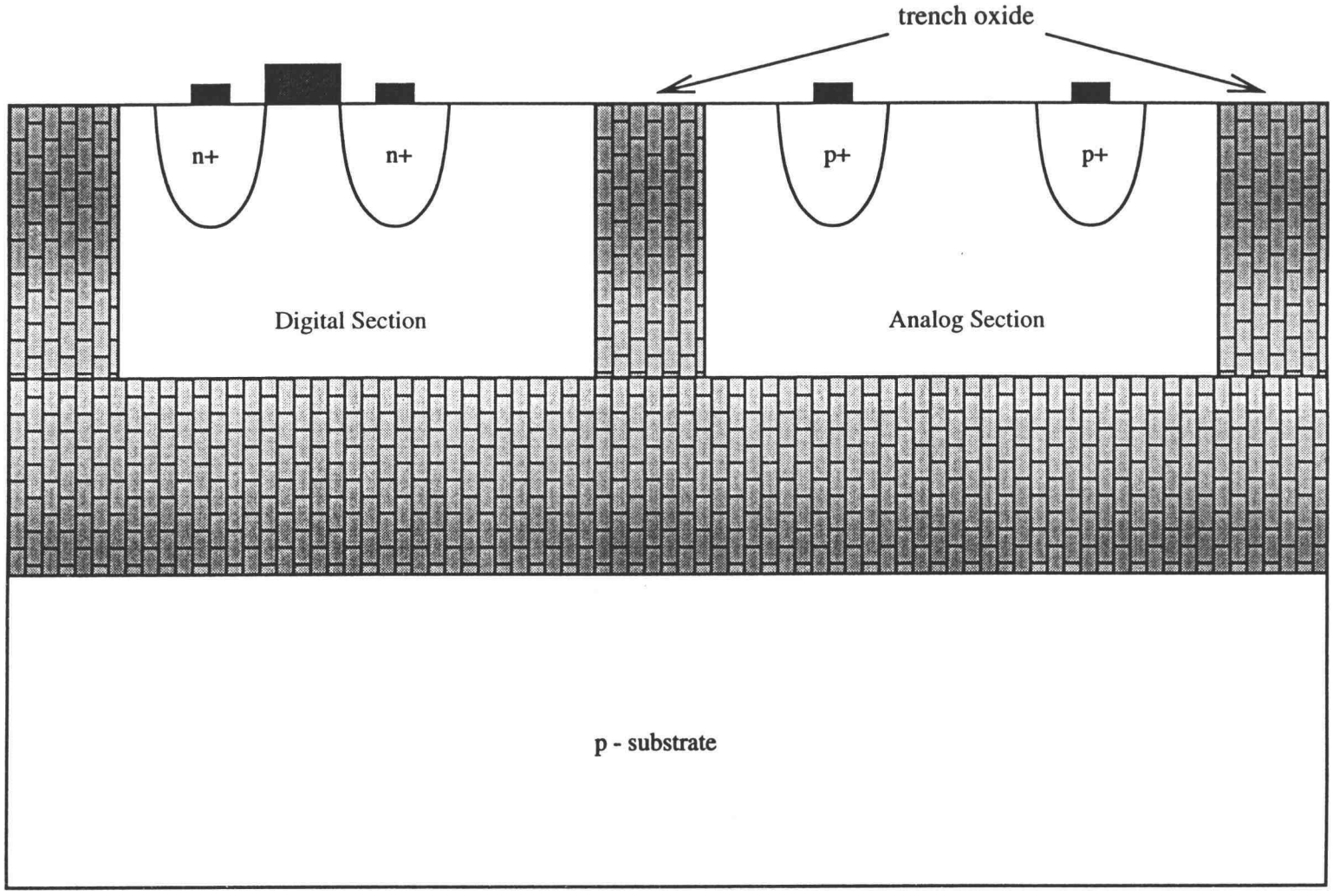

Fig. 2.5: SOI with Trench Oxide for Isolation

in the simple model shown in figure 2.6. The impedance of the substrate then works out to be, in the simplest case of equal inductances,

$$z = \frac{s^2LC+1}{sC} // (r+sL) \tag{2.2}$$

$$= \frac{(s^2LC+1)(r+sL)}{s^2LC+1+srC+s^2LC} \tag{2.3}$$

$$= \frac{(s^2LC+1)(sL+r)}{2s^2LC+srC+1} \tag{2.4}$$

$$= \frac{LC(s^2+1/LC)L(s+r/L)}{2LC(s^2+sr/2L+1/2LC)} \tag{2.5}$$

$$= \frac{L(s^2+1/LC)(s+r/L)}{2(s^2+sr/2L+1/2LC)} \tag{2.6}$$

Assuming r, the spreading resistance between the substrate contact and the bulk, to be negligible, we have the pole and zeros at $\frac{j}{\pm\sqrt{2LC}}$, 0, & $\frac{j}{\pm\sqrt{LC}}$ respectively. It is thus obvious that chip and package modeling is important in low-noise mixed signal systems [1-2]. The switching frequencies (noise generators) should avoid the vicinity of the package/pin's pole frequency. Also, extreme caution should be exercised by the addition of on-chip capacitances as it lowers the pole frequency which causes potential problems.

The other overlooked problem is to conveniently tie substrate contacts to the local ground bus. In high-speed designs, the output drivers are made very large. As a

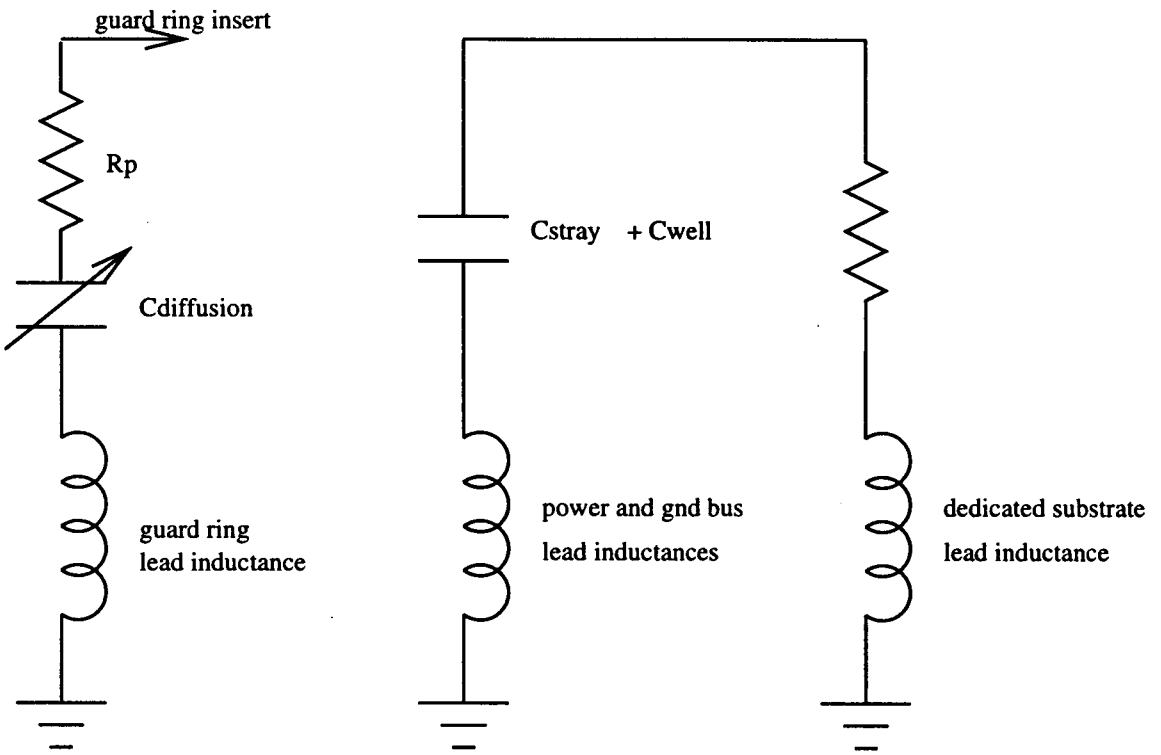

Fig. 2.6: Simple Model of Integrated Circuit Substrate Impedance

consequence, the increase in current drive induces huge amounts of power/ground noise on the digital side. Even with separate digital/analog ground buses, the noisy V_n induced in the digital ground bus can still find an ohmic path into the substrate via the substrate contacts as illustrated in figure 2.1. The solution would be to strap all substrate contacts to the analog ground bus or to have a ring of substrate contacts at the edge of the chip tied to a dedicated pin to prevent latch-up [1]. When this is done, noise in the substrate is contributed only by the well capacitances, n+ source capacitances, and interconnect couplings. Incidentally, noise due to interconnect couplings is generally smaller than other forms of coupling [6].

3. Resonant Forward Biased Guard Rings

3.1 Theory

A series resonant network is formed by the combination of the diffusion capacitance of the forward biased guard ring and the lead inductance, typically ranging from 3-10nH. This network provides a very low impedance path to ground for the substrate, limited only by the series resistance of the diode contributed by the bulk n+ regions and/or the contacts [20-21]. For CMOS n-well technology on epitaxial layers of typically 10um, we have the case of a short base-width diode where p^- is the lighter doped side (see figure 3.1). This implies $W << L_n$, where W is the length of the region of the p^- epitaxial layer, and L_n is the mean diffusion length of the minority carriers in the p^- region. Very little recombination takes place in the p^- region, and in the limit, all minority carriers (electrons) recombine at the epi-substrate layer interface. It is thus appropriate to replace the minority carrier lifetime, t_n, by the mean transit time, TT [22].

Since $t_n = TT = rC_D$ where r is the dynamic resistance of the diode ($r = \Delta V / I_{dc}$) and C_D is the diffusion capacitance,

$$\Rightarrow C_D = \frac{TT}{r} = \frac{TT * I_{dc}(mA)}{25} \qquad (3.1)$$

If the resonant frequency, $\omega_0 = 1/\sqrt{LC}$

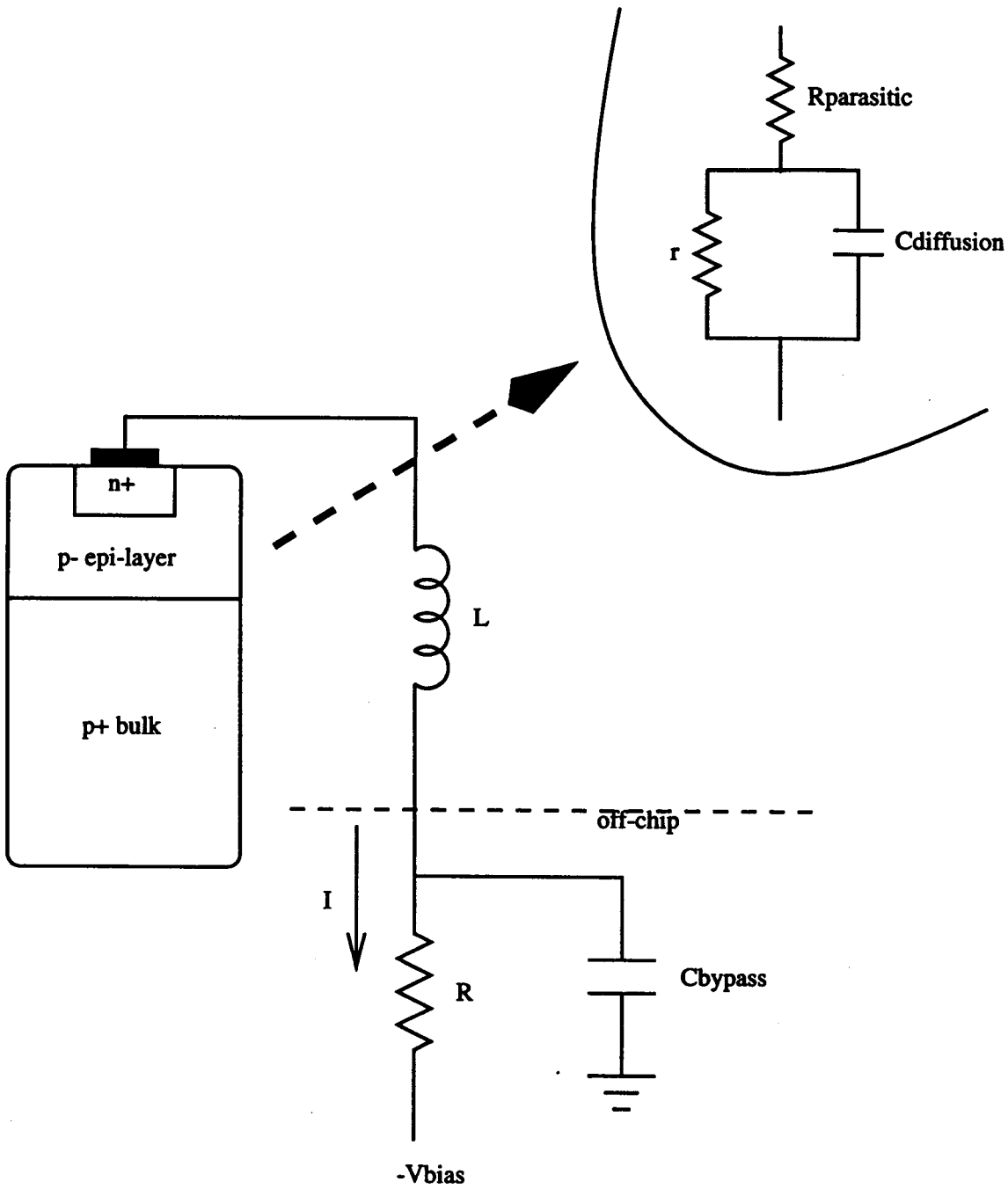

Fig. 3.1: Forward-Biased Resonant Guard Ring Diode Structure

$$\Rightarrow \omega_0 = \frac{1}{\sqrt{L*TT*{}^{I_{dc}}/_{25}}} \qquad (3.2)$$

We thus see that suppression of noise at any particular frequency is possible by the simple adjustment of forward current through the diode guard ring.

The impedance looking into the guard ring from the substrate node is given by

$$Z(s) = \frac{s^2 + s/(r \cdot C) + 1/(L \cdot C)}{s + 1/(r \cdot C)} \cdot L \qquad (3.3)$$

$$|Z(j\omega)| = \frac{\sqrt{r^2(1-\omega^2 \cdot L \cdot C)^2 + (\omega \cdot L)^2}}{\sqrt{1+(\omega \cdot r \cdot C)^2}} \qquad (3.4)$$

Because $\omega_0 \cdot r \cdot C >> 1$

$$|Z(\omega_0)| = \frac{\omega_0 \cdot L}{\sqrt{1+(\omega_0 \cdot r \cdot C)^2}} \approx \frac{L}{r \cdot C} = \frac{L}{TT} \qquad (3.5)$$

With a typical lead inductance of 10nH and transit time of 20nS, the theoretical impedance could go as low as 0.5Ω. Using more than one lead bond wire can result in even lower impedance figures.

3.2 The 'Q' Factor

The other important parameter is the quality factor, Q, which is defined by the ratio of the resonant frequency to the bandwidth. It determines the effectiveness of the

guard ring in suppressing noise at particular range of frequencies. To find out the Q of the guard ring with minimal parasitic resistance, we need to refer back to its impedance

$$Z(s) = \frac{s^2 + s/rC + 1/LC}{s + 1/rC} \cdot L. \tag{3.6}$$

Assuming the Q to be high, the *s* term in the denominator does not change much around the resonant frequency. Therefore, to find Q, one needs to only consider

$$s^2 + s/rC + 1/LC. \tag{3.7}$$

This happens to be the case of a parallel resonance with

$$Q = \frac{r}{\omega_0 L} = TT * \omega_0 \text{ [21].} \tag{3.8}$$

The characteristics are, however, just the opposite in that the guard ring circuit possesses a very low impedance at the resonant frequency, as opposed to high impedance in a parallel resonance circuit. With values consistent with [23], where C=3.3pF, r=6.1KΩ and L=10nH, an impedance plot (figure 3.2) of the guard ring model is generated to verify Q. The resonant frequency is at 876MHz and the bandwidth is about 8MHz which leads to a high Q of 110. The approximation of

$$Q = \frac{r}{\omega_0 L} = 111 \tag{3.9}$$

is therefore valid. This high Q guard ring circuit provides a very low impedance path at the resonant frequency and may not be effective when noise components over a broad spectrum are present or are undetermined. Therefore, a figure of merit is

$$Q * |Z(\omega_0)| = \omega_0 L. \tag{3.10}$$

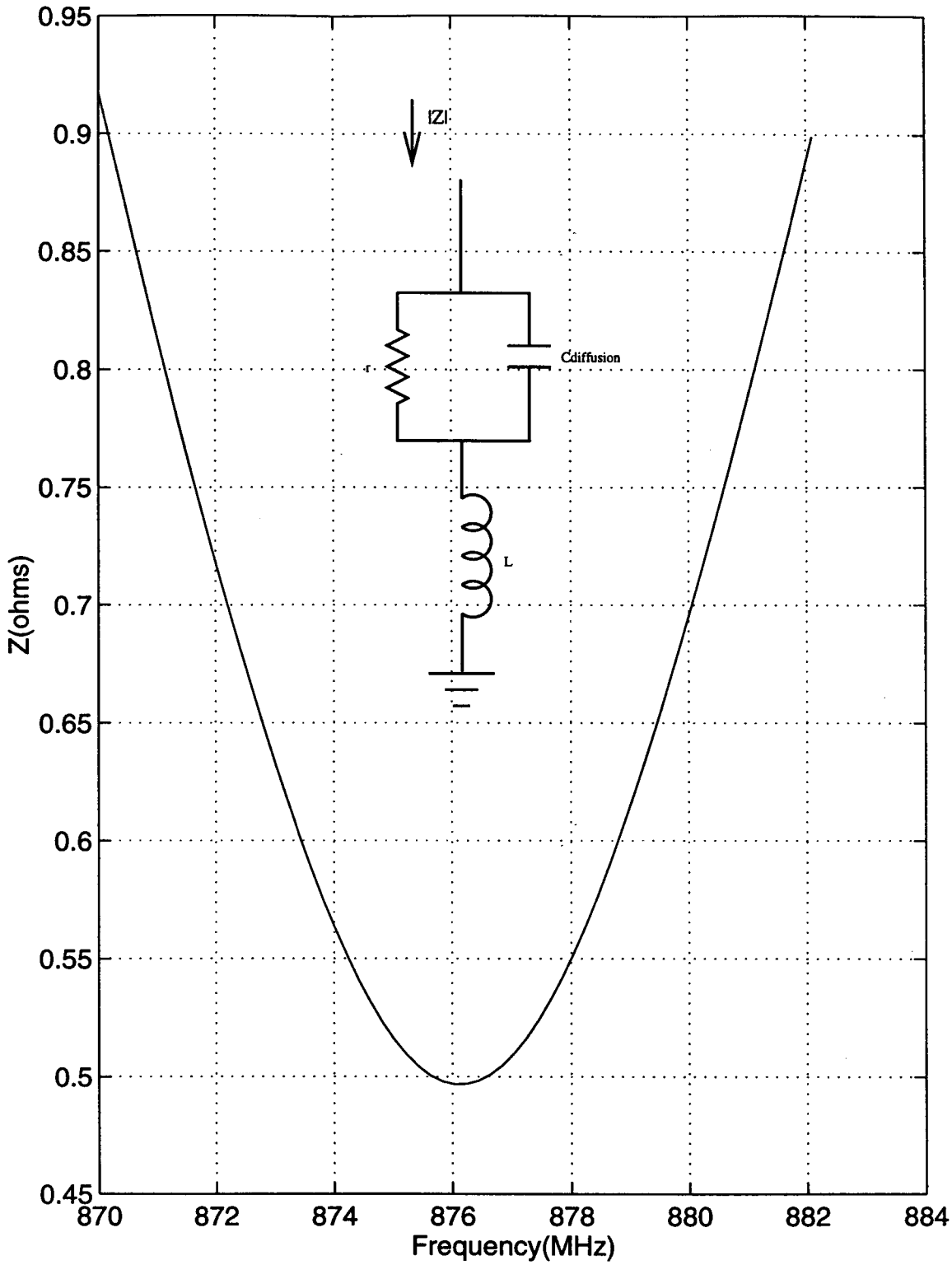

Fig. 3.2: High Q Guard Ring Circuit Model

Obviously, for broadband suppression of noise, a low Q and low Z is desired. A compromise would have to be reached by lowering Q and increasing the parasitic resistance R_s. This results in the series resonance where

$$Q = \frac{\omega_0 L}{R_s}. \tag{3.11}$$

This is shown in figure 3.3 with R_s=50 resulting in a much lower Q of 1. Optimization could thus be done to achieve a desired broadband noise coverage.

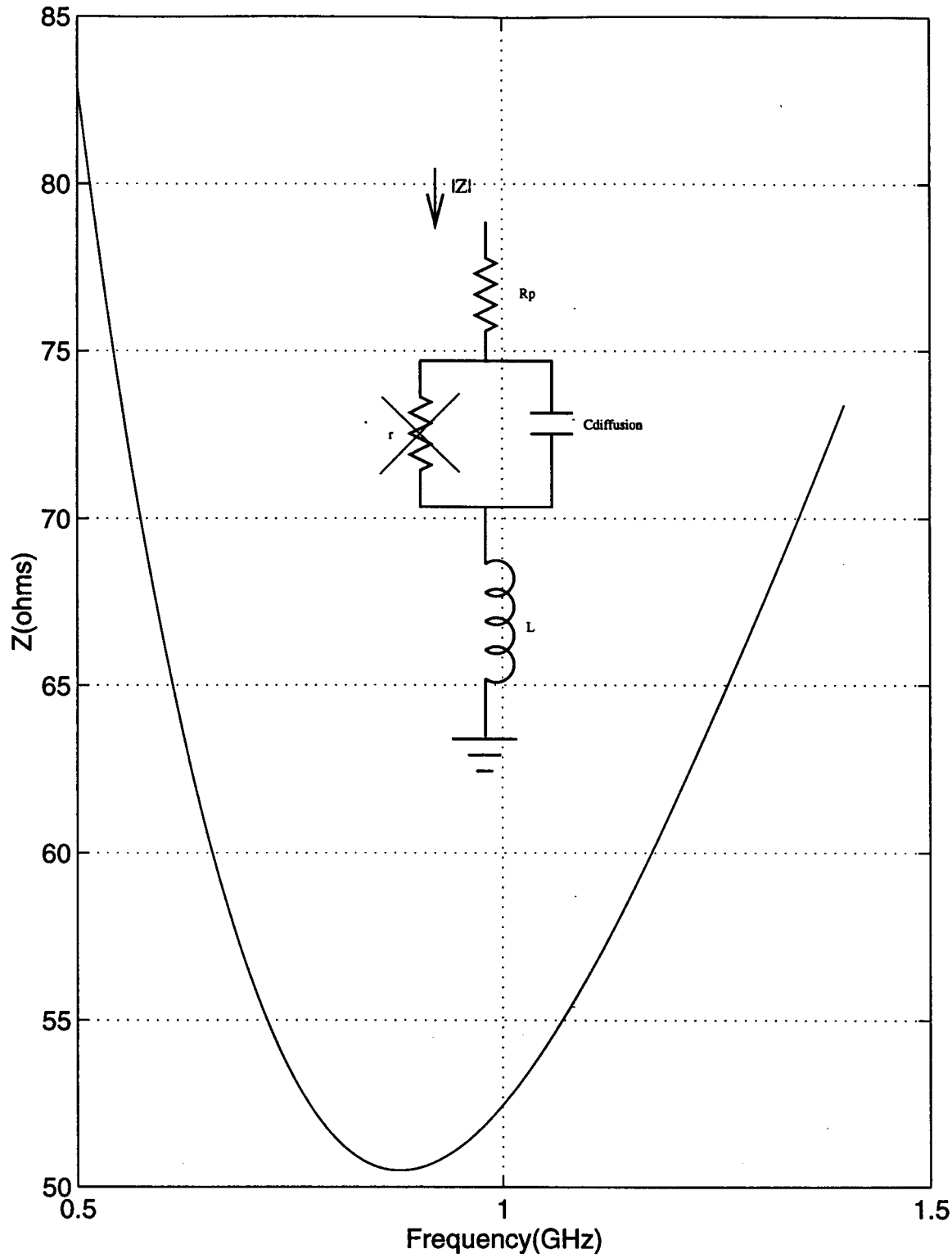

Fig. 3.3: Low Q Guard Ring Circuit Model

4. Simulations

4.1 Dedicated Substrate Lead Bond with shared Power/Ground Bus

This configuration is a typical case of DRAMs where the digital section consists of the memory cells, and the analog section is a sense amplifier. Figure 4.1 shows this simple one dimensional representation of the substrate circuit in a mixed-mode circuit on low resistance substrates. The 0.9Ω and 0.1Ω substrate resistances reflect the proportions of the typically 90% digital and 10% analog areas in a mixed-mode circuit. The 1Ω represents the horizontal bulk resistance where the substrate contact is sitting at the edge of the chip. The 3Ω represents an appreciable spreading resistance between the substrate contact and the heavily doped bulk [5]. The 10nH is a typical lead bond wire inductance for the dedicated substrate contact. The digital circuit comprises a 49-stage CMOS ring oscillator. 2.0μ length devices, W/L = 4.8/2.0, have been employed everywhere to achieve switching transients in the 500MHz to 1GHz range. The coupling to the substrate is primarily through the drain to substrate capacitance of the NMOS transistors[6] and the parasitic wiring capacitance of about 8fF. The analog circuit comprises a typical 2-stage differential operational amplifier with inputs at AC ground. Here minimum channel length, 1.0μm devices have been used to increase the bandwidth. The compensated bandwidth of this amplifier is about 2.6MHz and the unity voltage gain frequency is 270MHz. These circuits have been laid out and all parasitic capacitances, as well as n-well to substrate capacitances, are included in the simulations. Also, both digital and analog sections share

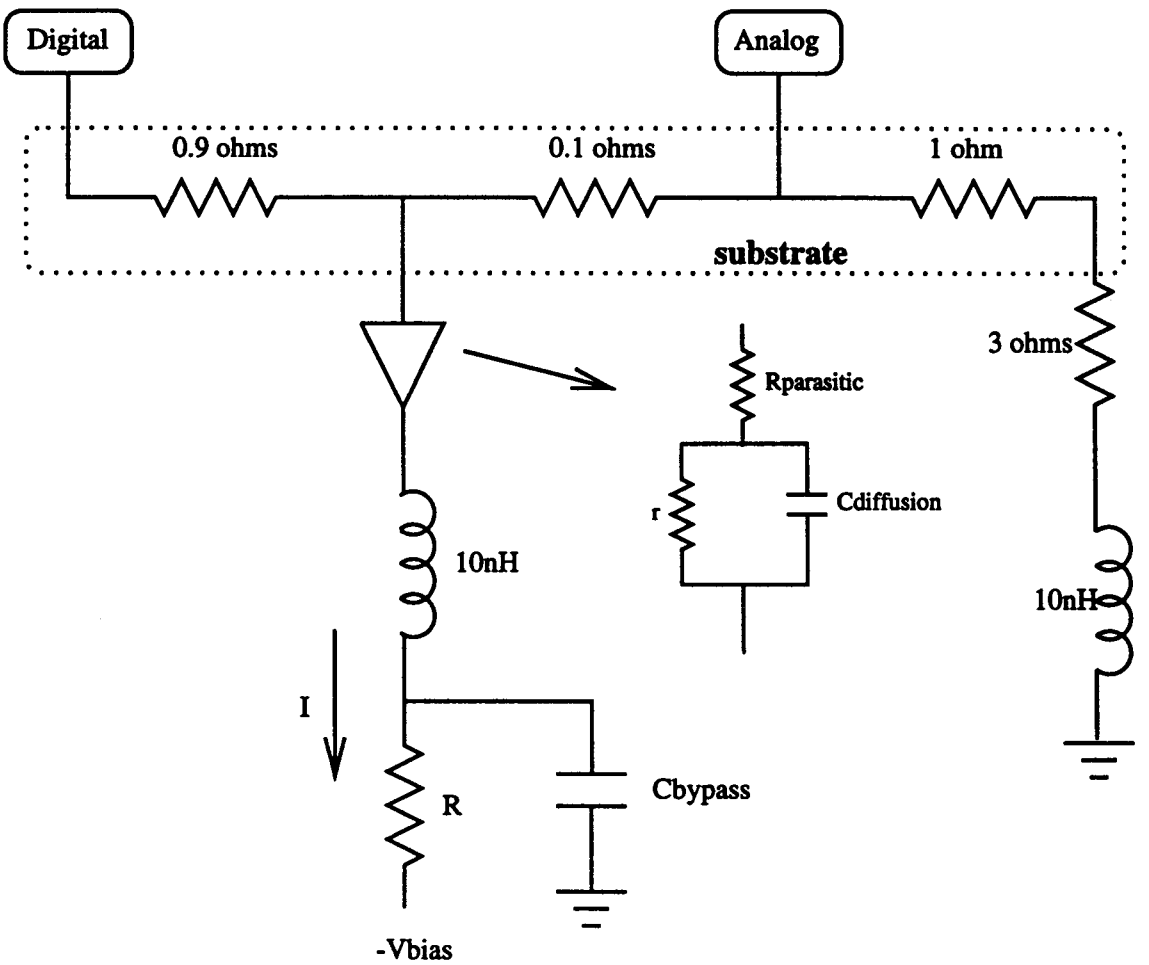

Fig. 4.1: One Dimensional Substrate Model with Capacitive Guard Ring Included

the same power supply and ground bus with lead bond wire inductances of 3nH each. The complete schematic is shown in figure 4.2.

To simulate the substrate noise which might be induced by switching at different frequencies in a digital circuit, the loop of a chain of 49 inverters is opened and a 10μA AC current source drives the local area substrate node behind the digital circuit. This serves to study the substrate impedance as shown in figure 4.3. The voltage "Vx" represents the substrate impedance at the local area node behind the analog circuit at different frequencies. The "no guard ring" case, with finite substrate resistances included, shows the pole/zero locations which causes the substrate impedances to ground to be extremely high, with peak value at 780MHz, far exceeding the impedance of just the substrate lead inductance alone. The conclusion is that single discrete transistor structures for the study of substrate noise [5,6,8] may be misleading by stating that substrate lead inductance is the main problem. In reality, one needs to appreciate the pin and package resonance of a particular chip that can result in high impedances at the substrate node.

The addition of a low resistance P+ guard ring [5, 8] will not help reduce the substrate impedance but simply move the pole to a lower frequency due to the additional stray/well capacitances added to the circuit. The correct solution is to add a low "Q" resonant circuit in parallel, employing a variable on-chip capacitor via the biased guard ring. This technique, then, is one of pole-zero cancellation; except that the "Q" of the added circuit (the guard ring) must be adjusted to lower values to avoid another low

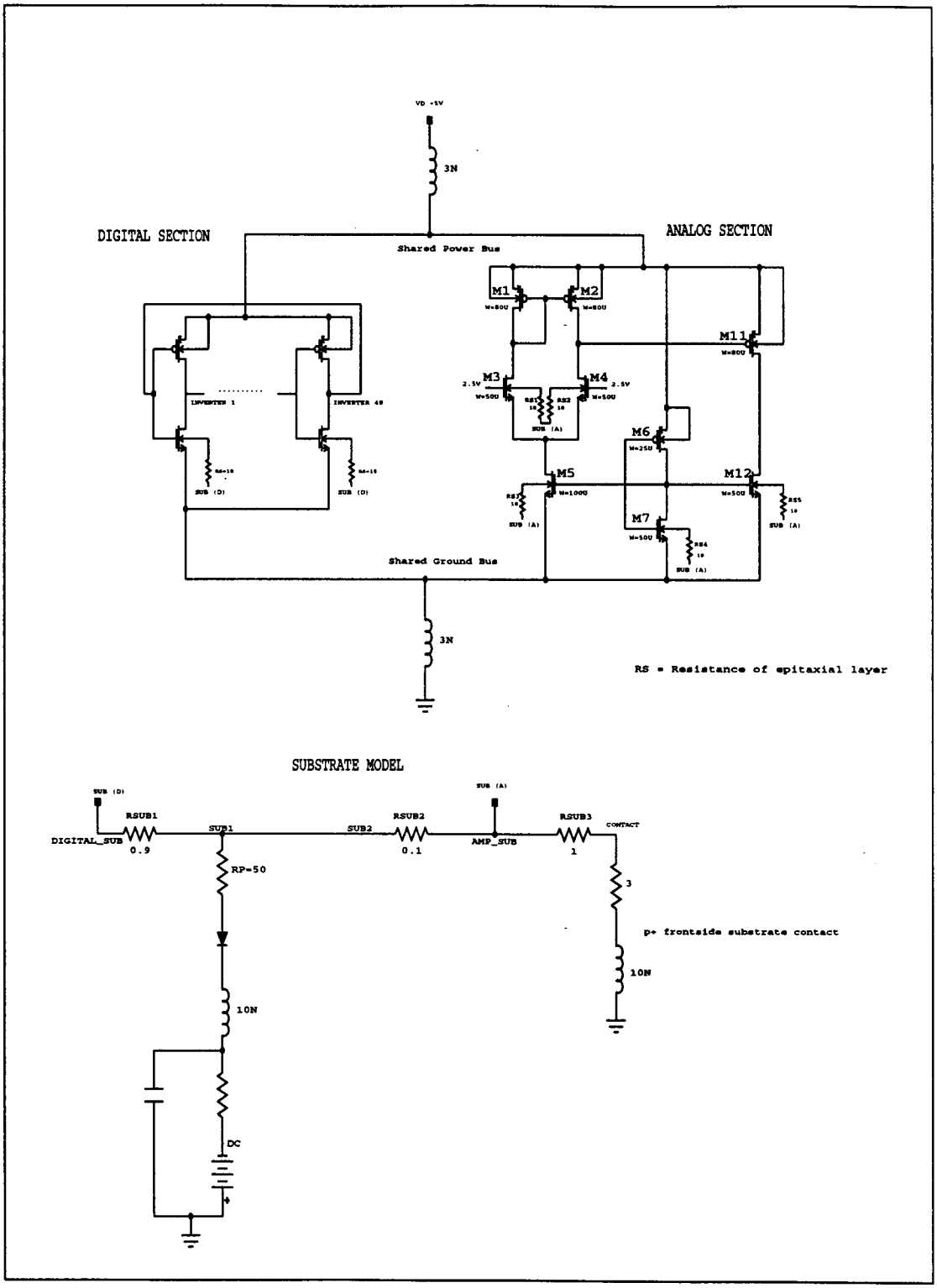

Fig. 4.2: Shared Vdd/Ground Bus with Dedicated Substrate Lead Bond Wire

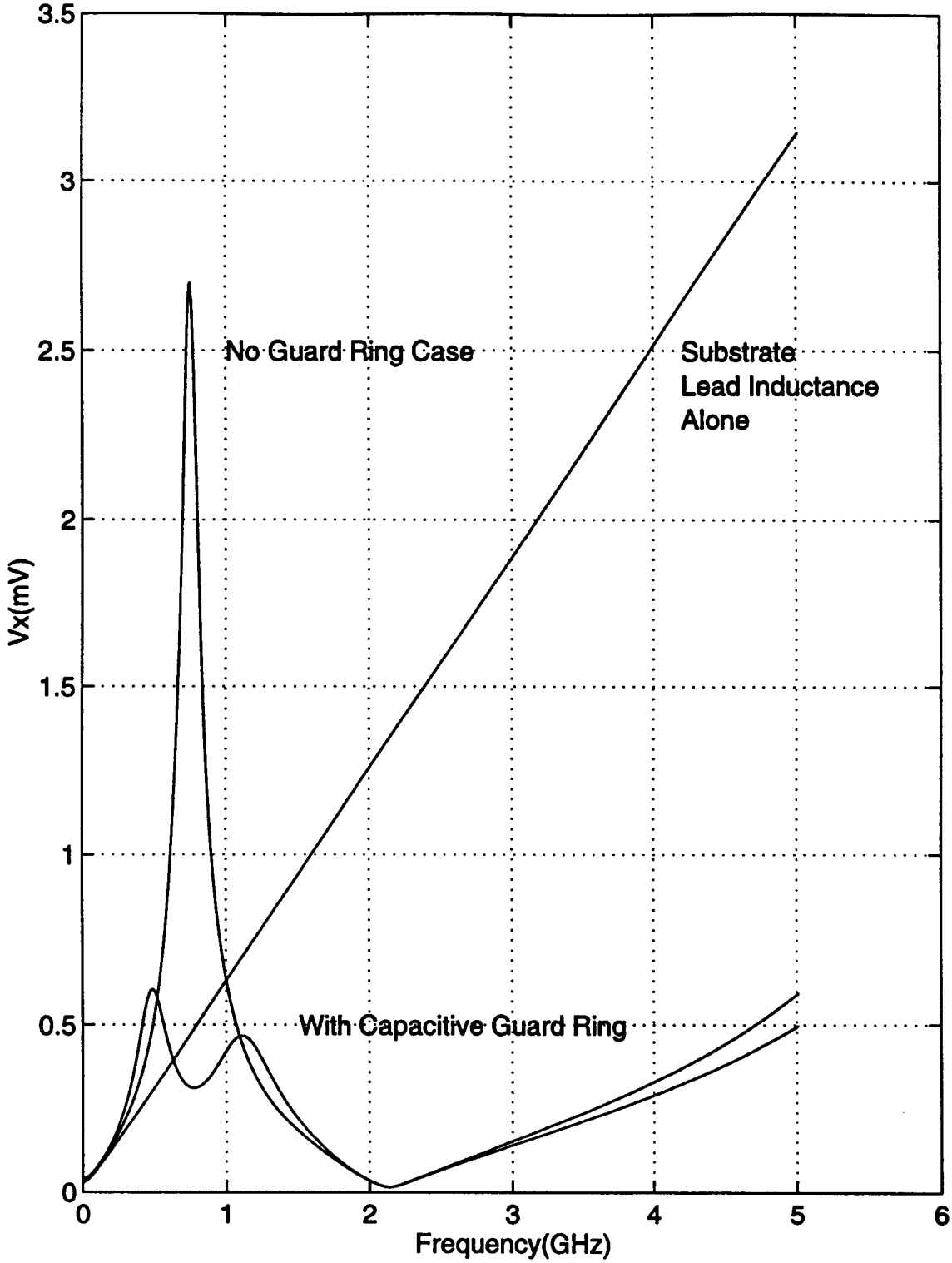

Fig. 4.3: Impedance Plot of Substrate Node driven with 10uA Current Source

frequency pole. Figure 4.3 also then shows the results of simulations using the relatively large on-chip variable capacitance ($1000\mu m^2$) of a forward biased N+ diode guard ring [24]. This serves to cancel the pin/package resonance of the chip, hence improving reliability and suppressing switching noise.

To test out the theory of noise suppression, the loop in the ring oscillator is closed where the substrate noise is generated by the switching of the inverters. Thus, the ring oscillator and analog amplifier emulate the mechanism of substrate crosstalk that corrupts analog signals in typical mixed-mode CMOS circuit applications. The major noise component at the amplifier output due to noise coupling to the substrate was at about 875MHz for a 49-stage ring oscillator. This frequency is the reciprocal of twice the average propagation delay per stage in the ring oscillator and reflects the period of the switching transients at the drain nodes of the NMOS transistors in the ring oscillator.

A substrate noise of 6mV pp. was generated at the output of the amplifier as shown in figure 4.4. When 5.5μA current was applied to the diode formed by the guard ring, the noise at the output of the amplifier was reduced to 750μV pp., and the primary component at 875MHz reduced by about an order of magnitude. Varying the bias current of the guard ring allows optimum results to be obtained and if necessary more than one guard ring can be used. This could reduce the substrate noise by at least an order of magnitude or more. This scheme can have a great effect in making mixed-mode circuits a practical reality and in improving the reliability of mixed-mode circuits [25].

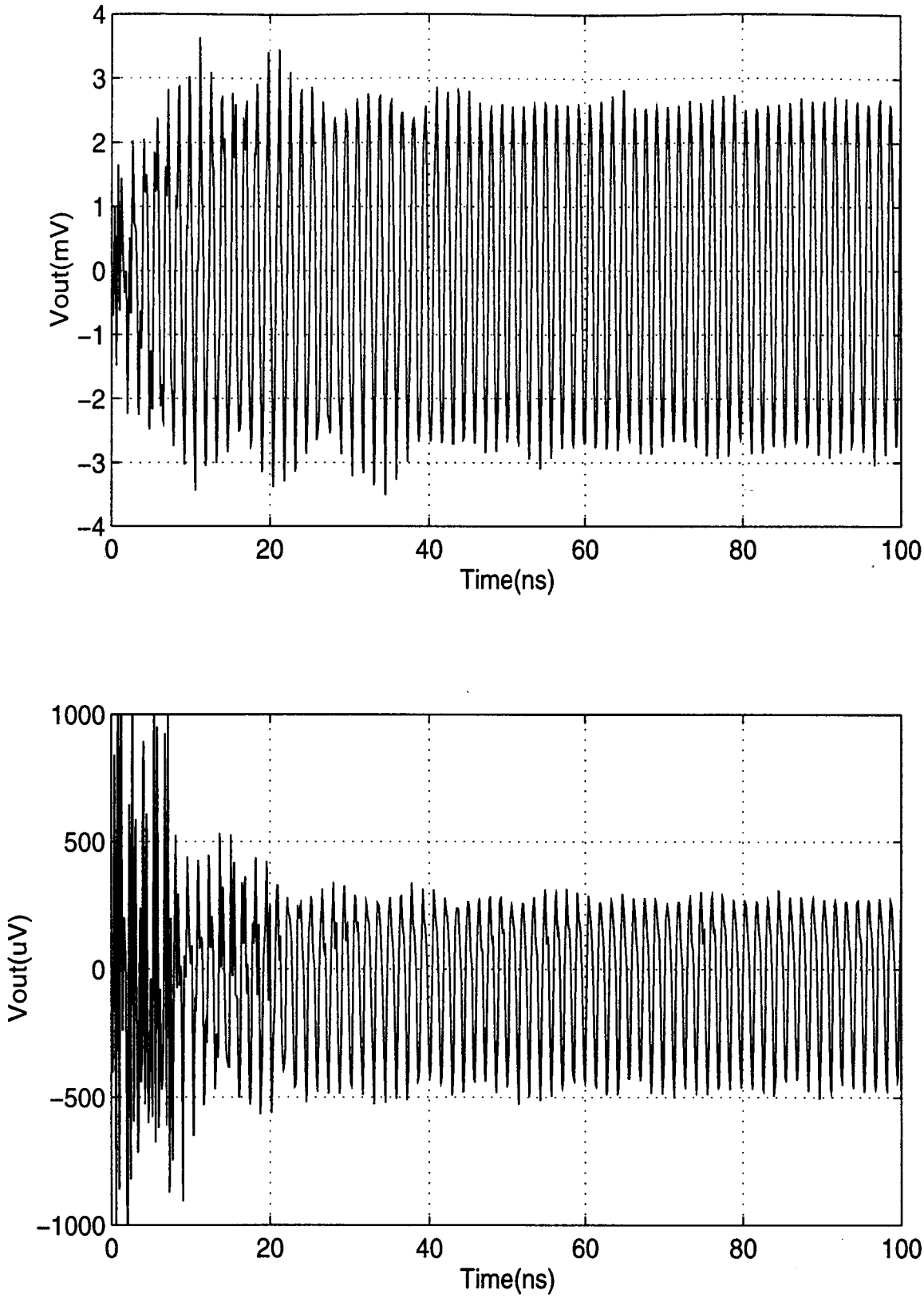

Fig. 4.4: Noise Waveform at the Output of Amplifier, (a) without Guard Ring; (b) with 1 Guard Ring

In mixed-mode circuits, it would be desirable to have separate power supply and ground buses for the analog and digital portions of the circuit and a substrate contact separate from the ground bus to avoid cross-talk through the ground bus due to power supply current transients associated with switching in the digital circuit. Concerns about latch-up can be avoided by design rules or substrate bias in which "Generation of Substrate Bias and Current Sources in CMOS Technology" [26] supports this noise suppression scheme. Extreme caution should be exercised in applying simple P+ guard rings in mixed-mode circuits and expecting significant reductions in substrate noise. Such may not be the case, or worse yet, large resonances may exist. In practice, the impedance of the substrate to ground should probably be measured, or at least simulated as shown in figure 4.3, if substrate noise and cross-talk is a concern.

4.2 Separate Power/Ground Bus with Substrate strapped to Analog Ground Bus

This configuration is perhaps the easiest modification to make to existing integrated circuits by simply removing the substrate connection from the digital ground bus as shown in figure 4.5. A more elaborate simulation is done where an additional non-overlapping clock generator and a switched capacitor filter is inserted into the digital section (figure 4.6). An impedance plot at the substrate node behind the analog circuit shows a leftward shift in the resonant frequency (figure 4.7). This is due to the additional capacitance being introduced by transistors as circuit size increases. The pin/package resonance in this case is 790MHz.

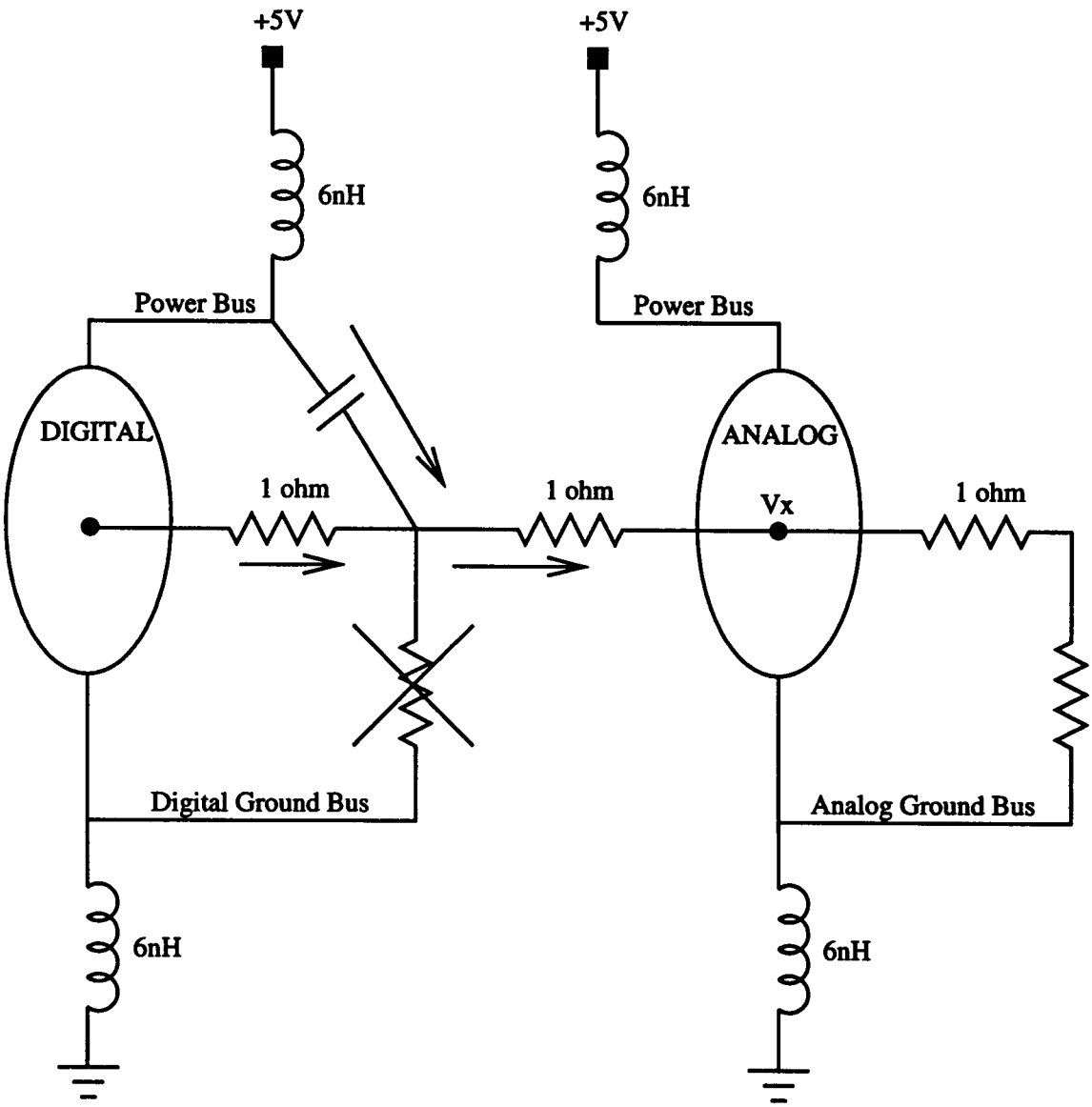

Fig. 4.5: Low Substrate Noise Solution by Removing Substrate Connection from Digital Ground Bus

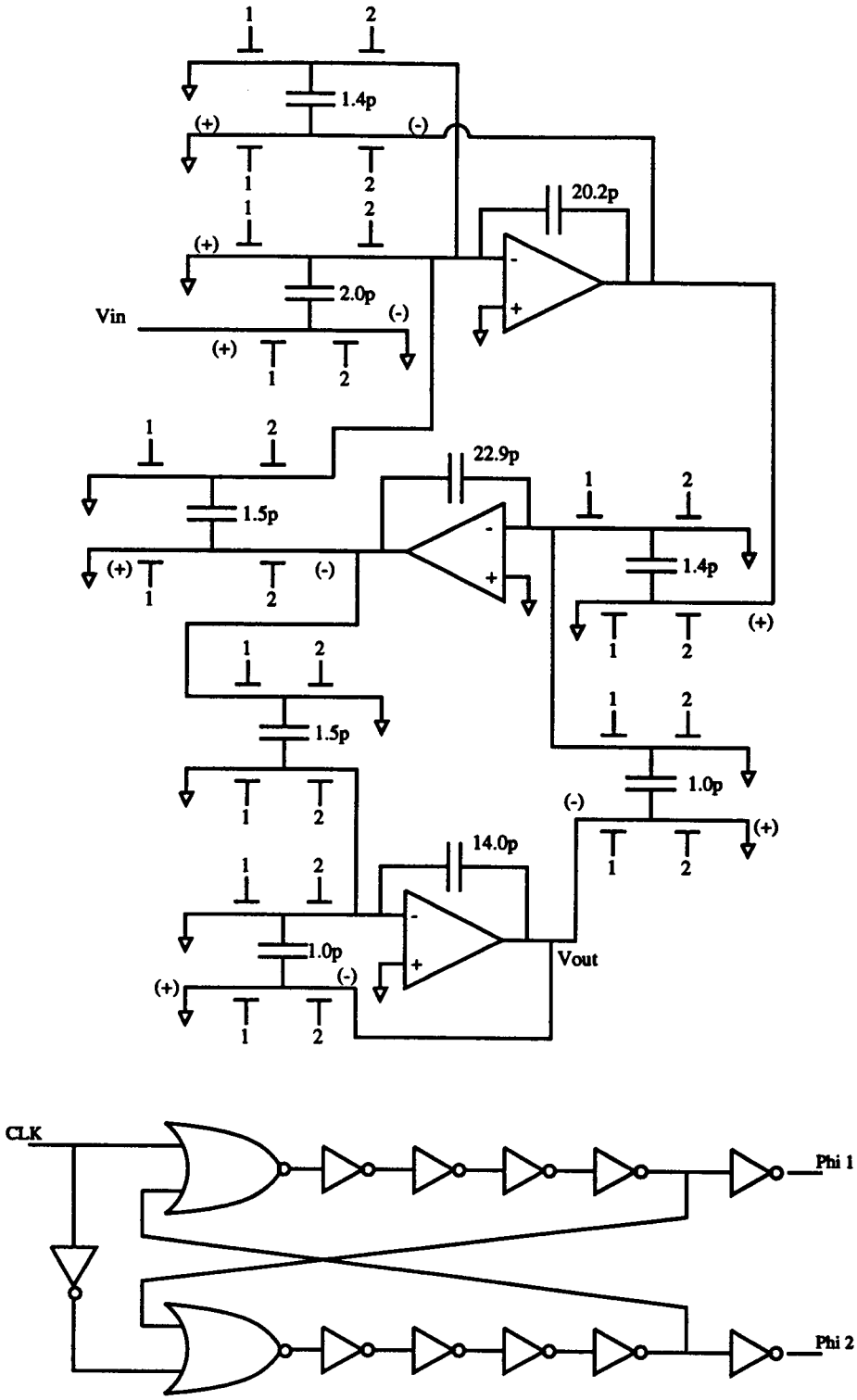

Fig. 4.6: Added Switching Activity - (a) 3rd Order Low-Pass SC Filter;
(b) 2 Phase Non-Overlapping Clock Generator

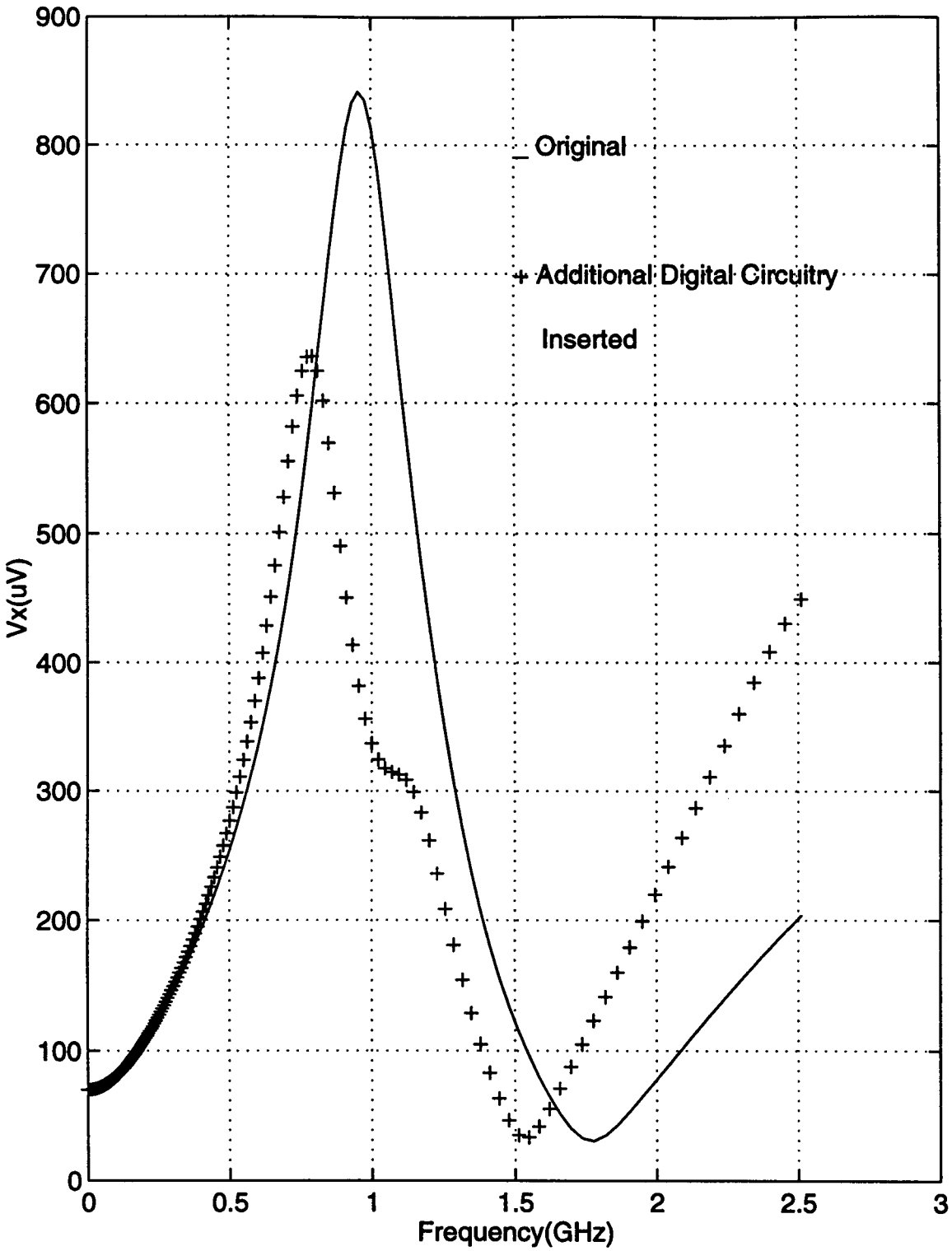

Fig. 4.7: Impedance Plot Showing Pin/Package Resonance with Added Circuit

The transient analysis is simulated with the ring oscillator not oscillating. The switches in the filter circuit are implemented with PMOS and NMOS transmission gates driven by the non-overlapping clock generator where an external clock of 256KHz drives the clock generator.

Note the noise waveform at the substrate node, V_x, behind the analog opamp circuit in figure 4.8(a). The glitches that occur at twice the 256KHz clock frequency (rise & fall switching) is the result of current injection into the substrate as the charges are transferred between capacitors and as the rising/falling edge of the clock signal is capacitively coupled into the substrate. Doing a Fourier transform of the waveform reveals the range of frequency components that stand out during the glitches, in this case, 380MHz to 550MHz (figure 4.8(b)). Figure 4.8(c) shows that the peak frequencies are about 15-20db higher than the rest of the spectrum. Note that this range does not fall at the pin/package resonant frequency (790MHz).

Two guard rings are used to create a low impedance path at the substrate by tuning them to this range as shown in fig. 4.9(a). Next, a re-run of the transient analysis, this time with the guard rings inserted, is made. The results show more than a factor of two improvement in noise suppression (figure 4.9(b)).

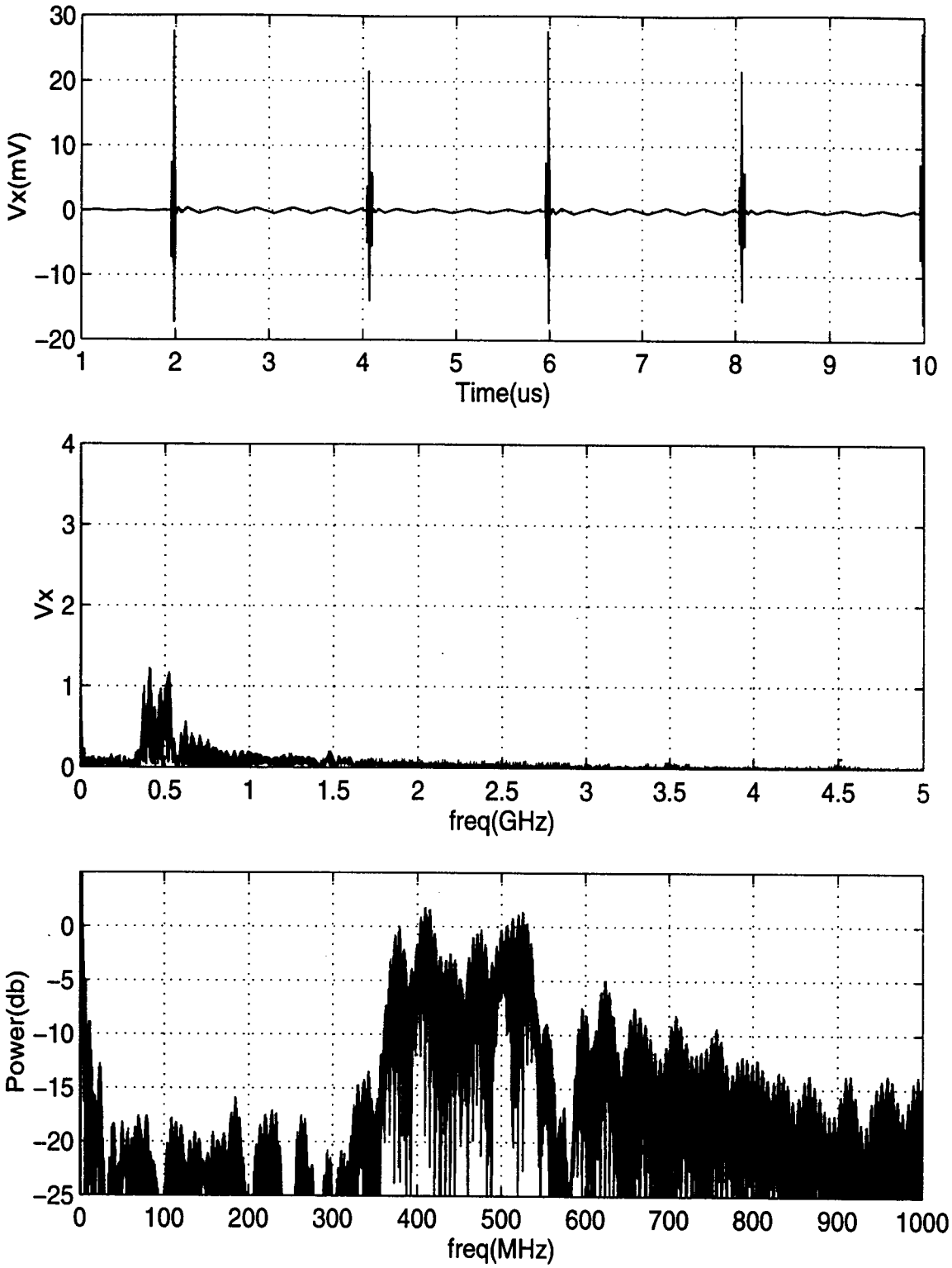

Fig. 4.8: (a) Noise Component at Substrate;
(b) Frequency Spectrum of Noise Component;
(c) Relative Power of Highest Frequency Component

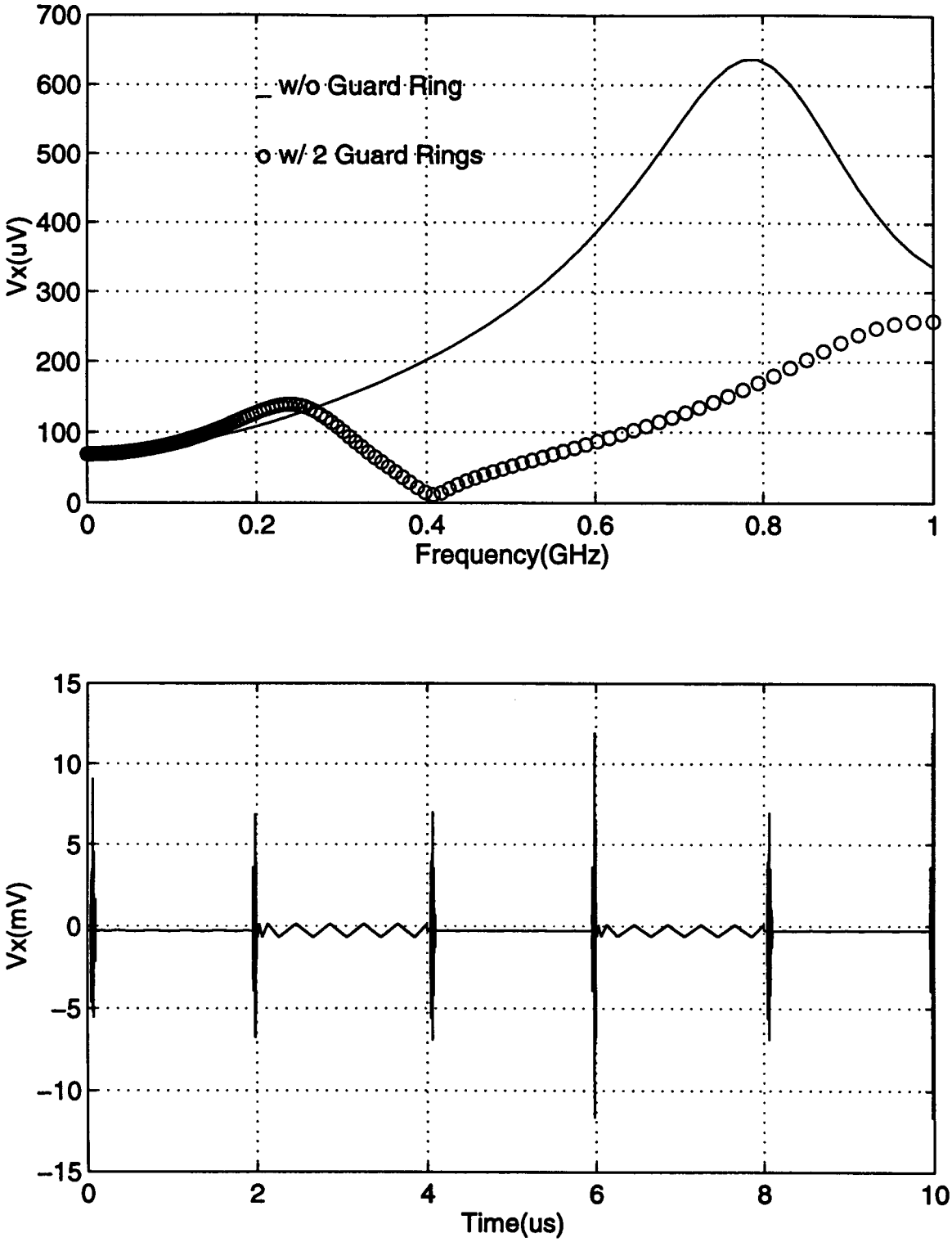

Fig. 4.9: (a) Guard Ring Tuning showing Lower Impedance Levels;
(b) Transient Plot of Reduced Substrate Noise Level

5. Conclusion

We have seen the cause of switching noise and the effect it has in modulating the threshold and backgate voltages in sensitive analog sections. The various noise reduction schemes, both at quieting the generator and isolating the substrate have been presented. Adding simple guard rings with the hope of suppressing noise may not necessarily be a solution as the added capacitances will simply lower the pin/package pole frequency which could result in extremely high impedances at the substrate node. The technique of using a variable-capacitance guard ring that resonates with the substrate lead inductance, thus providing a low impedance path to ground, has been shown to be effective in suppressing noise especially at those frequencies that reside around the pin/package resonant frequencies. In addition, using multiple lead-bond wires for the substrate contacts that serves to reduce the inductance can also reduce unwanted noise.

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APPENDICES

APPENDIX A: HSPICE SOURCE FILES

```
*MODEL FILE
.MODEL N-MOSIS_HP1U NMOS(LEVEL=3 LD=0.15U WD=0.3U VTO=0.73 TOX=200E-10
+ UO=520 NSUB=2.8E16 VMAX=1.35E5 ETA=0.02 THETA=0.07 KAPPA=0.1
+ DELTA=0.6 XJ=0.1U NFS=5E11 RSH=1000 RD=0 RS=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=3.2E-4 CJSW=2.8E-10
+ MJ=0.95 MJSW=0.12 JS=1E-3 FC=0 PB=0.8 ACM=2)
.MODEL P-MOSIS_HP1U PMOS(LEVEL=3 LD=0.0U WD=0.4U VTO=-0.9 TOX=200E-10
+ UO=180 NSUB=2.8E16 VMAX=1.9E5 ETA=0.09 THETA=0.13 KAPPA=3
+ DELTA=0.3 XJ=0.0U NFS=1E12 RSH=1400 RD=0 RS=0
+ CGDO=1.85E-10 CGSO=1.85E-10 CGBO=2.5E-10 CJ=5.2E-4 CJSW=2.8E-10
+ MJ=0.5 MJSW=0.33 JS=1E-3 FC=0 PB=0.9 ACM=2)
*@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@
*HIGH Q GUARD RING MODEL
.options brief post
i 0 1 ac 10u
c1 1 2 3.3p
l1 2 0 10n
r 1 2 6.1k
.ac dec 10000 870Meg 884Meg
.print v(1)
*@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@
*LOW Q GUARD RING MODEL
i 0 9 ac 10u
rp 9 1 50
c1 1 2 3.3p
l1 2 0 10n
r 1 2 6.1k
.ac dec 10000 500Meg 1.4G
.print v(9)
*@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@
*SUBSTRATE LEAD INDUCTANCE ALONE
i1 0 1 ac 10u
r1 1 2 .9
r2 2 3 .1
r3 3 4 1
r4 4 5 3
l1 5 0 10n
.ac dec 100 1k 5Ghz
.print v(3)
*@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@
*DEDICATED SUBSTRATE LEAD BOND W/SHARED POWER/GROUND BUS
.include '49.sub'
.options nomod brief convergence=3 post
.model diode1 d(level=1 is=5.6e-15 tt=20e-9 rs=35)
*-------------------------
*Inverter SUBCircuit
.subckt inv 1 2 3 4 5
*( VSS VDD OUT IN SUB )
m0 3 4 2 2 P-MOSIS_HP1U L=2U W=4.8U AS=25.92P AD=25.92P PS=20.4U PD=20.4U
m1 3 4 1 s N-MOSIS_HP1U L=2U W=4.8U AS=25.92P AD=25.92P PS=20.4U PD=20.4U
```

```
*The following capacitances are from layout:
cw 4 s 5.68f
c_inv_out 3 s 2.40f
r1 5 s 10
.ends inv
*---------------------------------
*AMPLIFIER SUBCIRCUIT
*CMOS Differential Amplifier With Output Stage
.subckt amp 1 2 3 4 9 amp_sub
*(input1 input2 output vdd gnd substrate)
M1 6 6 4 4 P-MOSIS_HP1U L=1U W=80U AS=432P AD=432P PS=170.8U PD=170.8U
M2 7 6 4 4 P-MOSIS_HP1U L=1U W=80U AS=432P AD=432P PS=170.8U PD=170.8U
M3 6 1 5 s1 N-MOSIS_HP1U L=1U W=50U AS=270P AD=270P PS=110.8U PD=110.8U
M4 7 2 5 s2 N-MOSIS_HP1U L=1U W=50U AS=270P AD=270P PS=110.8U
PD=110.8U
*OUTPUT STAGE
M11 3 7 4 4 P-MOSIS_HP1U L=1U W=80U AS=432P AD=432P PS=170.8U PD=170.8U
M12 3 8 9 s3 N-MOSIS_HP1U L=1U W=50U AS=270P AD=270P PS=110.8U PD=110.8U
M13 4 3 10 s6 N-MOSIS_HP1U L=1U W=80U AS=432P AD=432P PS=170.8U PD=170.8U
M14 10 10 9 s7 N-MOSIS_HP1U L=1U W=10U  AS=54P AD=54P PS=21.35U PD=21.35U
*BIAS CIRCUIT
M5 5 8 9 s4 N-MOSIS_HP1U L=1U W=100U AS=540P AD=540P PS=210.8U PD=210.8U
M6 8 8 4 4 P-MOSIS_HP1U L=1U W=25U AS=135P AD=135P PS=60.8U PD=60.8U
M7 8 8 9 s5 N-MOSIS_HP1U L=1U W=50U AS=270P AD=270P PS=110.8U PD=110.8U
*SUBSTRATE CONNECTIONS (resistances due to epitaxial layer)
rs1 s1 amp_sub 10
rs2 s2 amp_sub 10
rs3 s3 amp_sub 10
rs4 s4 amp_sub 10
rs5 s5 amp_sub 10
rs6 s6 amp_sub 10
rs7 s7 amp_sub 10
*SUBSTRATE CONNECTIONS (resistances due to epitaxial layer)
rs1 s1 amp_sub 10
rs2 s2 amp_sub 10
rs3 s3 amp_sub 10
rs4 s4 amp_sub 10
rs5 s5 amp_sub 10
rs6 s6 amp_sub 10
rs7 s7 amp_sub 10
*STRAY CAPACITANCES FROM LAYOUT EXTRACTION
c1 6 amp_sub 41.7f
c2 1 amp_sub 10.7f
c3 7 amp_sub 27.6f
c4 2 amp_sub 10.8f
c5 3 amp_sub 11.9f
*COMPENSATION
cc 7 99 1p
rc 99 3 1k
cl 3 0 1p
.ends amp
*--------------------------------
*GUARD RING CIRCUIT
.subckt gr1 sub2
```

```
d1 sub2 node_n+1 diode1
L1 node_n+1 bypass1 10n
RBIG1 bypass1 neg_terminal1 1
cbypass1 bypass1 0 .1uf
V_bias1 neg_terminal1 0 -0.532
.ends gr1
*--------------------
* common supply
v 1 0 5
*node 2 is lead inductance node to power supply
*node 4 is lead inductance node to true ground
lp 2 1 3n
lg 4 0 3n
xamp 6 7 out 2 4 amp_sub amp
vb1 6 0 2.5V
vb2 7 0 2.5V
*selection of output analysis
I 0 digital_sub ac 10u
.ac dec 500 1k 5Ghz
.tran    .1n 100n
*Measurement At Substrate or Amplifier Output Node
.print v(amp_sub)
Vmeasure 10000 0 1.9829V
.print tran V(out, 10000)
*selection for guard ring inclusion
xgr1 sub2 gr1
* Well Capacitance
cwellinv 2 digital_sub 1.1pf  *49-stage*
cwellamp 2 amp_sub 22ff
*Resistors between RO and amp substrate connections
Rsub2 digital_sub sub2 0.9
Rsub3 sub2 amp_sub .1
Rsub4 amp_sub sub3 1
Rsub5 sub3 contact 3
l_sub contact 0 10n
*@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@
*SEPARATE VDD/GND BUS W/ SUBSTRATE STRAPPED TO ANALOG GND BUS
*with non-overlap clk generator and switch cap filter circuits added
.model diode1 d(level=1 is=5.6e-15 tt=20e-9 rs=10)
.model diode2 d(level=1 is=5.6e-15 tt=20e-9 rs=1)
*--------------------------------
*GUARD RING 1 CIRCUIT
.subckt gr1 sub1
d1 sub1 node_n+1 diode1
L1 node_n+1 bypass1 10n
RBIG1 bypass1 neg_terminal1 1
cbypass1 bypass1 0 .1uf
v_bias1 neg_terminal1 0 -0.565    *400MHz*
.ends gr1
*--------------------------------
*GUARD RING 2 CIRCUIT
.subckt gr2 sub1
d2 sub1 node_n+2 diode2
L2 node_n+2 bypass2 10n
```

```
RBIG2 bypass2 neg_terminal2 1
cbypass2 bypass2 0 .1uf
*2nd guard ring diode current tuning V_bias2 neg_terminal2 0 -0.565     *400MHz*
.ends gr2
*@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@
*3RD ORDER SWITCHED CAP FILTER
.subckt sc in 15 phi phib d1 gnd sub
xsw1  in 2  phi  d1 gnd sub sw
xsw2  2  0  phib d1 gnd sub sw
xsw3  3  0  phi  d1 gnd sub sw
xsw4  3  6  phib d1 gnd sub sw
xsw5  4  0  phi  d1 gnd sub sw
xsw6  4  7  phib d1 gnd sub sw
xsw7  5  0  phi  d1 gnd sub sw
xsw8  5  6  phib d1 gnd sub sw
xsw9  9  10 phi  d1 gnd sub sw
xsw10 9  0  phib d1 gnd sub sw
xsw11 8  0  phi  d1 gnd sub sw
xsw12 7  8  phib d1 gnd sub sw
xsw13 13 0  phi  d1 gnd sub sw
xsw14 13 14 phib d1 gnd sub sw
xsw15 12 0  phi  d1 gnd sub sw
xsw16 12 15 phib d1 gnd sub sw
xsw17 15 16 phi  d1 gnd sub sw
xsw18 16 0  phib d1 gnd sub sw
xsw19 10 17 phi  d1 gnd sub sw
xsw20 17 0  phib d1 gnd sub sw
xsw21 18 0  phi  d1 gnd sub sw
xsw22 14 18 phib d1 gnd sub sw
xsw23 19 11 phi  d1 gnd sub sw
xsw24 19 0  phib d1 gnd sub sw
xsw25 20 0  phi  d1 gnd sub sw
xsw26 11 20 phib d1 gnd sub sw
xsw27 21 0  phi  d1 gnd sub sw
xsw28 6  21 phib d1 gnd sub sw
c1  2  3  2p
c2  4  5  1.44p
c3  6  7  20.17p
c4  8  9  1.44p
c5  10 11  22.9p
c6  12 13  1p
c7  14 15  14.01p
c8  16 17 1p
c9  18 19 1.47p
c10 20 21 1.47p
e1 7 0 0 6 5000
e2 11 0 0 10 5000
e3 15 0 0 14 5000
.ic v(6)=0 v(10)=0 v(14)=0
.ends
*@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@
*NON-OVERLAPPING CLOCK GENERATOR
*.subckt clkgen clk 11  10  d1  gnd sub
*clkgen clk phi phib vdd gnd sub*
```

```
.subckt nor a b out vdd gnd sub
m1 out a gnd sub N-MOSIS_HP1U w=1.8u l=1.2u as=6.84p ad=6.84p ps=10.8u pd=10.8u
m2 out b gnd sub N-MOSIS_HP1U w=1.8u l=1.2u as=6.84p ad=6.84p ps=10.8u pd=10.8u
m3 out a 1 vdd P-MOSIS_HP1U w=1.8u l=1.2u  as=6.84p ad=6.84p ps=10.8u pd=10.8u
m4 1 b vdd vdd P-MOSIS_HP1U w=1.8u l=1.2u as=6.84p ad=6.84p ps=10.8u pd=10.8u
.ends
x1 clk 1 d1 gnd sub inv1
x2 clk 11 2 d1 gnd sub nor
x3 1   10 3 d1 gnd sub nor
x4 2 4 d1 gnd sub inv1
x5 3 5 d1 gnd sub inv1
x6 4 6 d1 gnd sub inv1
x7 5 7 d1 gnd sub inv1
x8 6 8 d1 gnd sub inv1
x9 7 9 d1 gnd sub inv1
x10 8 10 d1 gnd sub inv1
x11 9 11 d1 gnd sub inv1
x12 10 12 d1 gnd sub inv1
x13 11 13 d1 gnd sub inv1
.ends
*-------------------------------------
.subckt sw in out phi v gnd sub
m1 in phi out sub N-MOSIS_HP1U w=1.8u l=1.2u as=6.84p ad=6.84p pd=10.8u ps=10.8u
m2 out phib in v  P-MOSIS_HP1U w=5.4u l=1.2u as=27p ad=27p pd=16.8u ps=16.8u
x1 phi phib v gnd sub inv2
.ends
*-------------------------------------
.subckt inv1 in out vdd gnd sub
m1 out in gnd sub N-MOSIS_HP1U w=1.8u l=1.2u as=9p ad=9p ps=13.6u pd=13.6u
m2 out in vdd vdd P-MOSIS_HP1U w=5.4u l=1.2u as=27p ad=27p ps=20.8u pd=20.8u
.ends
.subckt inv2 in out vdd gnd sub
m1 out in gnd sub N-MOSIS_HP1U w=3.6u l=1.2u as=18p ad=18p ps=17.2u pd=17.2u
m2 out in vdd vdd P-MOSIS_HP1U w=10.8u l=1.2u as=54p ad=54p ps=31.6u pd=31.6u
.ends
*---------------------------------------------
*seperate digital/analog power supplies
vd d1 0 5
va a1 0 5
vclk clk 0 pulse(0 5 0 .1u .1u 1.8u 4u)          *256KHz external clk*
vin in 0 sin(0 .5 2k)                            *Input analog signal
* xclk clk phi phib 2 4 digital_sub clkgen       *clk generator*
xsc in scout phi phib d1 4 sub1 sc               *sc filter*
*selection of output analysis
I 0 digital_sub ac 10u
.ac dec 100 1k 1G
.tran .1n 10u
.probe v(amp_sub)
.print v(amp_sub)
*selection of guard ring inclusion
xgr1 sub2 gr1
xgr2 sub1 gr2
*node 2 is lead inductance node to digital power supply
*node 3 is lead inductance node to analog power supply
```

```
*node 4 is digital lead inductance node to ground bus
*node 5 is analog lead inductance node to ground bus
*lead inductances from digital/analog to power supply / ground
ldp d1 2 6n
lap a1 3 6n
ldg 4 0 6n
lag 5 0 6n
xamp 6 7 out 3 5 amp_sub amp
Vb1 6 0 2.5V
Vb2 7 0 2.5V
*Well Capacitance
cwellinv 2 digital_sub 1.1pf   *49-stage*
cwellamp 3 amp_sub 22ff
*Resistances in the substrate layer
Rsub_sub1 digital_sub sub1 0.5
Rsub1_sub2 sub1 sub2 0.4
Rsub2_amp sub2 amp_sub .1
Ramp_sub3 amp_sub sub3 1
Rsub3_agb sub3 5 6
.end
```

APPENDIX B: MATLAB FILE

```
%File for generating fig. 4.8
clear all
figure(1)
set(gcf,'PaperPosition',[1.1 1.5 6.9 9]);
load intscnogr
t1=intscnogr(:,1)';
v1=intscnogr(:,2)';
t =t1(10001:100001);
v =v1(10001:100001);
subplot(311), plot(t.*1e6,v.*1e3);
ylabel('Vx(mV)');
xlabel('Time(us)');
grid;

y1=fft(v.*hann(90001)); f=1e+10*(0:45000)/90001;
subplot(312), plot(f.*1e-9,abs(y1(1:45001)));
ylabel('Vx');
xlabel('freq(GHz)');
grid;

subplot(313), plot(f.*1e-6,20*log10(abs(y1(1:45001))));
axis([0 1e3 -25 5]);
ylabel('Power(db)');
xlabel('freq(MHz)');
grid;
end

%@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@@
```

Script that converts SPICE data file to MATLAB format

```
#!/bin/csh
cat $1 | sed '/H S P I C E/,/analysis/d' | sed '/y/,/PST 1996/d' | sed 's/k/e+3/ g' | sed 's/x/e+6/g' | sed 's/g/e+9 /g' | sed 's/p/e-12/g' | sed 's/n/e-9/g' | s ed 's/u/e-6/g' | sed 's/m/e-3/g' > /tmp/jj1
tail -n+4 /tmp/jj1 > $2
rm /tmp/jj1
```