# AN ABSTRACT OF THE DISSERTATION OF

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Title: A Multi-Bit Delta Sigma Audio Digital-to-Analog Converter

Abstract approved:

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Digital-to-analog converters (DACs) with wide dynamic range and high linearity are required for high-end audio applications. A multi-bit delta sigma audio DAC, using a novel gain-correction technique, is described in this thesis. For widely varying on-chip RC time constant, the DAC gain can be accurately controlled by the correction circuitry. To overcome the nonlinearity caused by the mismatches of the internal unit-element DAC, a new dynamic element matching (DEM) algorithm, named split-set data-weighted averaging (SDWA), is proposed. In-band tones can be effectively removed by the proposed algorithm while signal-to-noise ratio (SNR) is high. Hardware implementation of SDWA is cost-effective and low-latency which makes it practical in high speed applications. A headphone driver integrated together with the analog reconstruction filter in the delta sigma audio DAC allows the designed DAC to driver the headphone directly.

An experimental headphone driver was designed and fabricated in a 0.35μm CMOS technology. The prototype delta sigma audio DAC integrated with the headphone driver was built using the same technology. Simulation and measured results show that they both meet the requirements for a typical high-end audio system.

A Multi-Bit Delta Sigma Audio Digital-to-Analog Converter


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Ruopeng Wang, Author

# ACKNOWLEDGEMENTS

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# A Multi-Bit Delta Sigma Audio Digital-to-Analog Converter

## Chapter 1   Introduction

Delta sigma digital-to-analog converters (DACs) are usually designed to achieve the high accuracy with the moderate conversion rate. By using noise shaping and oversampling techniques, the requirement for analog components matching accuracy in such kind of DACs are much relaxed. Thus in the narrow-band signal processing applications such as digital audio, delta-sigma modulation is widely used.

## 1.1   Motivation

Digital-to-analog converters (DACs) with wide dynamic range and high linearity are typically required for today's high-end audio applications [1]. Considering the analog components matching accuracy in the DAC circuit implementation, the traditional Nyquist-rate DACs can only achieve moderate effective number of bits (ENOB) which is less than 14-bit in general. Careful layout, better process technologies and post laser beam correction can improve the performance of those DACs to a nearly perfect level. However, it increases the cost at the same time. In the applications such as digital audio, high accuracy of 16 to 20 ENOB and low cost are generally desired [2]. In such a situation, oversampling delta sigma DACs structure is often preferred because of their

advantages such as high resolution, insensitivity to circuit non-idealities and low cost [3].

Although the single-bit modulator used to be the primary choice in the early audio DAC works [4] [5], the multi-bit modulation is becoming the primary choice of the present time [1] [2] [6] [7]. Given a small input signal such as -60 dBFS-a featured input for audio DACs, comparing with the single-bit modulator, the outputs of the multi-bit modulator mainly center around zero code level with few adjacent levels while those of the single-bit modulator fluctuate between maximum and minimum levels. This fluctuation makes the single-bit modulator generate larger quantization noise [1]. In addition to the lower noise, the multi-bit modulator is more stable given the same order of noise shaping. As a result, the multi-bit modulator is preferred in the high-end audio DACs though the single-bit modulator has the inherent good linearity [3].

Using the multi-bit modulator in a delta sigma DAC does require the use of the correction techniques to deal with the nonlinearity caused by the multi-bit internal DAC. The nonlinearity can be seen as an additive error to the ideal output of the DAC and may directly limit the overall resolution and linearity achievable by the DAC [8]. For an internal DAC built from equal-valued capacitors in the switched-capacitors circuit or equal-valued current sources in the current-steering DAC, called a unit-element DAC, dynamic element matching (DEM) is widely used technique to reduce the nonlinearity caused by it. There are various proposed DEM algorithms [9] and the common point among them is to make the usage of

the unit elements carried in such a way that both the input-dependent tones and the mismatch noise in the interested signal band are reduced to a certain tolerable level. The existing of the trade-off [3] between small in-band tones and high noise floor in those algorithms sometimes leads to the other direction of dealing with nonlinearity which is digital correction technology. In stead of trying to reduce nonlinearity caused by mismatch errors, digital correction techniques try to completely eliminate the mismatch errors in the unit-element DACs [3] [10] [11].

DEM usually works fairly well in audio applications because a high (>64) oversampling ratio (OSR) can be applied due to the relative narrow audio signal bandwidth (20 Hz ~ 20 KHz). A problem associated with currently used DEM algorithms is the increased noise floor in the signal band which is caused by the process converting the in-band tones into pseudo-random noise. Finding a solution for achieving a high spur-free dynamic range (SFDR) in combination with a high signal-to-noise (SNR) performance is of great interest.

Audio DACs are usually designed to drive a speaker or headphone with the aid of a separate power amplifier (speaker or headphone driver). Current audio units fail to integrate the driver as part of the audio DACs system. Full integration would improve the quality of audio DACs as well as reduce the cost of production.

## 1.2    Contribution of this work

A multi-bit delta sigma audio DAC, using a novel gain-correction technique, is described in this thesis. For widely varying on-chip RC time constant, the DAC gain can be accurately controlled by the correction circuitry. To overcome the nonlinearity caused by the mismatches of the internal unit-element DAC, a new DEM algorithm, named split-set data-weighted averaging (SDWA), is proposed. In-band tones can be effectively removed by the proposed algorithm while the signal-to-noise ratio (SNR) is high. Hardware implementation of SDWA is cost-effective and low-latency which makes it practical in high speed applications. A headphone driver integrated together with the analog reconstruction filter in the delta sigma audio DAC allows the designed DAC to drive the headphone directly.

An experimental headphone driver was designed and fabricated using $0.35\mu m$ CMOS technology. The prototype delta sigma audio DAC integrated with the headphone driver was built using the same technology. Simulation and measured results show that they both meet the requirements for a typical high-end audio system.

## 1.3    Dissertation organization

The seven chapters of this dissertation are organized in the following structure:

In chapter 2, fundamentals of the delta sigma audio DACs are described. Nyquist sampling and oversampling are compared. Noise shaping technique is reviewed. The unit-element DAC and nonlinearity, introduced by its mismatch errors, are analyzed. The introduction to signal-to-out-band-noise (SNRout) is provided. A general audio DAC structure and the function of each block are discussed.

In chapter 3, design of a digital interpolation filter and noise shaper are covered. An interpolator with a 128 interpolation factor and a third-order, seven-level delta sigma noise shaping loop are included. The simulation results of these two blocks are presented.

In chapter 4, the DWA algorithm is briefly described and the problems with it are discussed. A novel DEM algorithm, named Split-set data weighted averaging (SDWA), is proposed to overcome problems in the basic DWA algorithm. The simulations demonstrate the effectiveness of SDWA. A gate-level implementation of SDWA is presented and the simulations of this SDWA circuit are included.

In chapter 5, low-distortion driver design techniques are discussed and an experimental headphone driver is presented. The comparisons of various amplifier output stages are given. After describing the noise and distortion calculations in the designed headphone driver, the measurement results of the experimental headphone driver are presented.

In chapter 6, a prototype audio DAC is presented. The internal DAC is a switched-capacitor structure composed of six unit elements. The correction circuitry proposed to maintain an accurate DAC gain with a large on-chip R·C time constant variance is introduced. The headphone driver, integrated as a part of the analog reconstruction filter, is discussed and the measurement results of the audio DAC are included.

In chapter 7, a summary of the thesis as well as the suggestions on future work are discussed.

# Chapter 2   Delta Sigma Digital-to-Analog Converters

A digital-to-analog converter (DAC) is a device that reconstructs a continuous-time analog signal from its digital representation. Figure 2-1 shows a typical DAC system. In such a configuration, the digital input sequence x(n) passes an ideal digital-to-analog interface to generate an inter-stage output $y_1(t)$ which is discrete only in time. A following zero-order hold circuit turns $y_1(t)$ into an analog staircase waveform $y_2(t)$ which is then lowpass filtered by passing through a reconstruction block (smoothing filter) to eliminate all the replicas of the spectrum outside the signal band and to output the desired analog signal y(t). As can be seen from this conversion process, a DAC serves as the bridge between digital and analog domains.
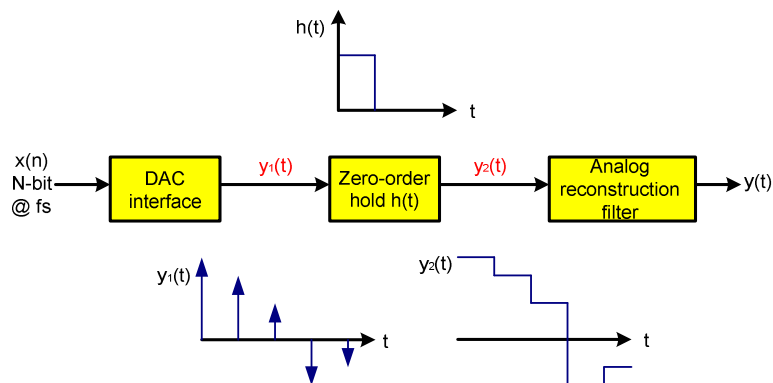


**Figure 2-1 The DAC system**

This chapter reviews some basic principles of the DACs. Nyquist sampling, oversampling and delta sigma noise shaping are going to be described. A general

structure of the delta sigma DAC is then presented, which is followed by a brief review of the audio DACs.

## 2.1 Nyquist-rate sampling

According to the sampling theorem, as long as an analog signal is sampled at a frequency $f_s$ that is at least twice the signal bandwidth $f_B$, which is called Nyquist rate, the signal can be completely represented by and recoverable from the sampled values [12]. A DAC working at the Nyquist rate, called Nyquist rate DAC, needs an analog reconstruction filter with a very small transition band because the image of the signal is just next to the signal itself. In addition to the stringent requirements on the smoothing filter, Nyquist-rate DACs can only achieve moderate accuracy because the matching problems among the analog components directly limit the precision of those DACs.

Digital signal x(n) contains the quantization errors due to its finite N-bit resolution. The spectrum of the quantization errors can be considered as white if certain conditions are met [8]. By making this assumption, the analysis of the quantization errors in the DAC becomes easier [3]. The signal and quantization noise power spectrum for x(n) under Nyquist sampling is shown in Figure 2-2.
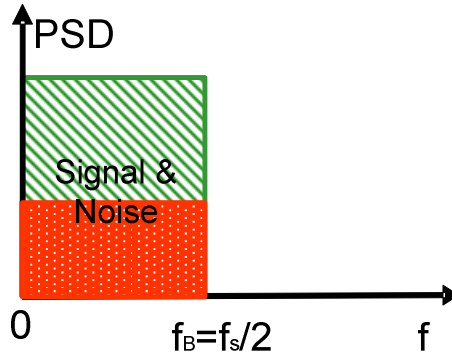
**Figure 2-2 Signal and quantization noise spectrum under Nyquist sampling**

For a full scale sinusoid signal x (t), with the white quantization noise assumption, the SNR of x (n) is given by [13]

$$SNR = 6.02N + 1.76 \text{ (dB)} \tag{2-1}$$

In general, the SNR of a full scale digital input improves by 6.02 dB for each additional bit of resolution [14].

## 2.2 Oversampling

The digital sequence, x (n), can also be obtained by oversampling the analog signal x (t) with a frequency $f_s$ much higher than the Nyquist rate. Under oversampling, the first image of the signal x (n) is far away from the signal itself which allows the use of a reconstruction filter with a large transition band so that the filter design is simplified. Calculations show that the quantization noise power density for an N-bit signal can be expressed by [15]

$$P_{e,n} = \frac{(\Delta V)^2}{6F_T} \qquad \textbf{(2-2)}$$

Here, $\Delta V$ is the smallest voltage step represented by N bits. A plot of Equation 2-2 is shown in Figure 2-3. As can be seen from the plot, the noise for the higher sampling frequency in the interested signal band is smaller than that for the lower sampling frequency, although the total noise power is the same,
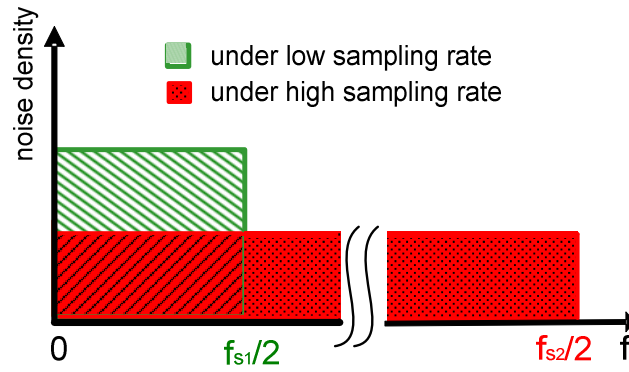


**Figure 2-3 Noise density under oversampling**

In an oversampling situation, the ratio of the sampling frequency to the twice of the signal bandwidth is defined as the oversampling ratio (OSR). The increase in the resolution of an N-bit conversion due to oversampling is given by [13]

$$ENOB_{increase} = \frac{\log_2(OSR)}{2} \qquad \textbf{(2-3)}$$

Equation 2-3 shows that doubling of the OSR increases 0.5 bit ENOB. For example, a 12-bit converter has 15 ENOB with OSR=64.

In contrast to the Nyquist sampling, the cost for the oversampling is that the digital circuits in the system are running at a higher speed which is practical with the development of VLSI technology. In today's applications, oversampling technique is widely used to achieve high resolution in data converters.

## 2.3    Noise shaping

As shown in Figure 2-3, the noise in the signal band is low under oversampling. For a given OSR, the in-band noise can be further reduced by using so called delta-sigma modulation [15]. Figure 2-4 gives a first-order delta-sigma modulator in z-domain. The name of delta sigma comes from the fact that the difference (delta) between the input signal x (z) and the delayed output $z^{-1}$y (z) is added (sigma) together during the operation. Although it is not quite right to model the quantization noise as a white noise source e(z), it is much more convenient to do analysis of delta sigma modulator by doing so. Because of this assumption, simulations need to be executed to verify the correctness of the results made from the analysis based on this model.
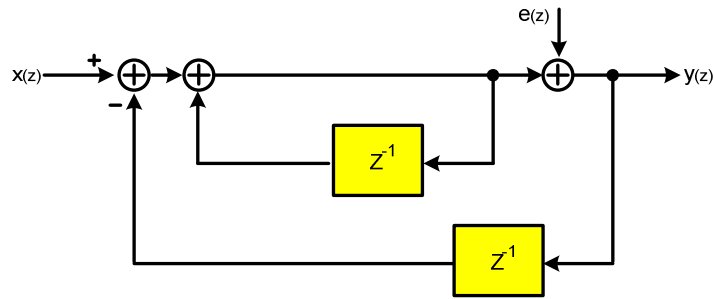
**Figure 2-4 First-order delta sigma modulator**

Calculations based on Figure 2-4 show the output of the first order delta sigma modulator is given by

$$Y(z) = X(z) + (1 - z^{-1})E(z) \tag{2-4}$$

This can be written in the form

$$Y(z) = STF(z)X(z) + NTF(z)E(z) \tag{2-5}$$

Here, stf (=1) is called signal transfer function and ntf (=1-z$^{-1}$) is called noise transfer function. In frequency domain, ntf can be written as

$$|NTF(f)| = 2\sin(\pi f) \tag{2-6}$$

the plot of Equation 2-6 is shown in Figure 2-5. Clearly, it is a highpass response and thus the in-band noise is shaped as desired.
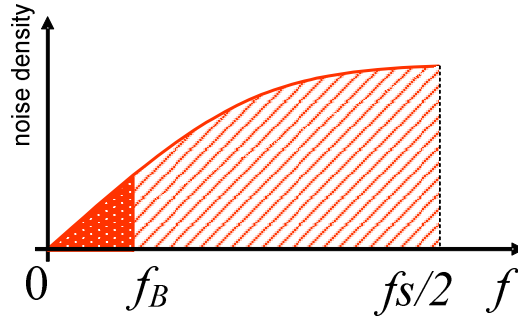
**Figure 2-5 First-order noise shaping**

The signal is not affected during the modulation because of the unit gain signal transfer function. Thus comparing with oversampling but no delta sigma modulation, the SNR with delta sigma modulation is improved by [15]

$$\text{SNR}_{improve} = 20\log_{10}\left(\frac{\sqrt{3}}{\pi} \cdot OSR\right)(\text{dB}) \qquad \textbf{(2-7)}$$

A higher order noise shaping can also be achieved by making a higher order of noise transfer function. For example, by cascading two first-order loops, a second-order noise shaping function $(1\text{-}z^{-1})^2$ is formed. Generally speaking, a higher order loop is less stable than a lower order loop [3]. The multi-stage noise shaping (MASH) is a method to achieve high order shaping without increasing stability problems [3]. For such a structure, the stability performance of the whole loop follows that of each stage used to construct the high order shaping loop. The disadvantage of MASH structure is the possible noise leakage, which limits the actually achievable resolution [3].

## 2.4    Oversampling delta-sigma DACs

The complete block diagram of a typical oversampling delta sigma DAC is shown in Figure 2-6. The input signal x (n) is an N-bit sampled datum with sampling frequency $f_s$, which is often slightly larger than Nyquist rate. By passing through an interpolation filter, its sampling frequency is increased to OSR· $f_s$, and the images introduced by oversampling are removed. The word length of $x_1(n)$ is changed from N to $N_1$ (where $N_1$ is equal to N or greater). $x_1(n)$ then feeds into the delta sigma modulator to output the signal $x_2(n)$ whose word length is usually M-bit (M is much smaller than N and can be as small as 1). $x_2(n)$ is converted to the analog signal x (t) by an internal M-bit DAC. The quantization noise brought by the delta sigma modulation process (most of the noise power is out of the interested signal band) is filtered by the following lowpass reconstruction filter and the smoothed analog signal y (t) results.



**Figure 2-6 Block diagram of a delta-sigma DAC**

For the delta sigma DAC shown in Figure 2-6, its ideal SNR can be calculated by

$$\text{SNR} = 6.02M + 1.76 + (20L + 10)\log_{10} OSR - 10\log_{10} \frac{\pi^{2L}}{2L+1} \text{ (dB)} \quad \textbf{(2-8)}$$

Here, $L$ is the order of the delta sigma modulator and M is the number of bits of the internal DAC. Equation 2-8 shows that a large SNR can be achieved by increasing the levels of the internal DAC, using a high order modulator and applying a high OSR.  Increasing the levels of the internal DAC usually needs more analog components, which is not desired in general. A high order modulator makes the loop less stable in addition to being a more complex design itself, and high OSR pushes the circuits to run in the high speed. Thus, different stratagems need to be applied according to the different applications.

A widely used structure for the M-bit internal DAC in the delta-sigma DAC is a so called unit-element DAC which is built from unit elements such as capacitors in a switched-capacitor circuit or current sources in a current-steering DAC. An advantage of such a DAC is that there are no glitches at its output [13]. Figure 2-7 shows the diagram of the unit-element DAC.
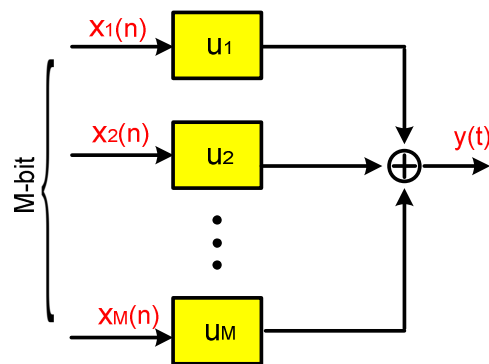


**Figure 2-7 the unit-element DAC**

An M-bit unit-element DAC usually has M+1 output levels and for an M-bit input data, the output of the unit-element DAC can be expressed by

$$y(t) = \sum_{m=1}^{M} u_m \cdot x_m(n)$$
(2-9)

where $u_m$ is the unit-element value and $x_m(n)$ is the input data. Instead of the binary weighted codes, the input data to a unit-element DAC is the thermometer codes. In a thermometer code, the number of 1s is the decimal value that a code represents. Table 2-1 shows the thermometer codes for a seven-level unit-element DAC with consecutive input decimal values 4, 3, 1 and 5.

**Table 2-1 the thermometer codes**

| Input | 4 | 3 | 1 | 5 |
|-------|---|---|---|---|
| x(6)  | 0 | 0 | 0 | 0 |
| x(5)  | 0 | 0 | 0 | 1 |
| x(4)  | 1 | 0 | 0 | 1 |
| x(3)  | 1 | 1 | 0 | 1 |
| x(2)  | 1 | 1 | 0 | 1 |
| x(1)  | 1 | 1 | 1 | 1 |

As can be seen from Table 2-1, thermometer codes have a highest priority to select the first unit-element and lowest priority to select the last one. Since mismatches usually exist among all the unit elements, signal dependent tones are unavoidably

generated in a unit-element DAC by such a selection process. The nonlinearity in a multi-bit modulator caused by the multi-level internal DAC, also called mismatch error, should be reduced in order to achieve high accuracy. Dynamic element matching (DEM) block is then a necessary part in a multi-bit delta sigma DAC. Among those proposed DEM algorithms, data-weighted averaging (DWA) is a very popular one due to its simplicity, effectiveness and easy hardware implementation [16]. By cyclically selecting the unit-element, DWA algorithm achieves zero long-term mismatch error and a first-order mismatch shaping. Because of this selection, for DC or low frequency signals, DWA algorithm suffers from tone problems which limit its application. A brief review on DWA algorithm is going be given in chapter 4. The DWA encoded data for the inputs shown in Table 2-1 is listed in Table 2-2.

**Table 2-2 the DWA encoding**

| Decimal | 4 | 3 | 1 | 5 |
|---------|---|---|---|---|
| x(6) | 0 | 1 | 0 | 1 |
| x(5) | 0 | 1 | 0 | 1 |
| x(4) | 1 | 0 | 0 | 1 |
| x(3) | 1 | 0 | 0 | 1 |
| x(2) | 1 | 0 | 1 | 0 |
| x(1) | 1 | 1 | 0 | 1 |

## 2.5    Features of audio DACs

There are some features in audio delta sigma DACs which are described as followings:

Applying a high oversampling ratio is practical because of the relative narrow audio signal band which is 20 Hz to 20 kHz. With a higher OSR, a lower order delta sigma modulator can be used to achieve similar targets.

Not like in the other applications, the cut-off frequency of the analog reconstruction filter in a delta-sigma audio DAC is generally set as 100 kHz ~ 200 kHz which means 5 ~10 times of the upper edge frequency of the audio band. The reason for this is that the frequency components beyond 20 kHz can not be detected by human ears while the large out-of-band noise should be somewhat attenuated to avoid overloading the headphone or speaker.

The dynamic range (DR) of an audio DAC, measured with 1 kHz, -60 dB relative to full-scale (dBFS) input, is one of the important specifications to evaluate the performance of an audio DAC. DR is calculated by adding 60 dB to the measured signal-to-distortion and noise ratio (SNDR) given such an input.

As shown in Figure 2-8, for small input signals such as -60dBFS, the outputs of a multi-bit modulator mainly center on a zero code level with few adjacent levels, while those of a one-bit modulator jump between maximum and minimum levels, which makes a one-bit modulator generate larger quantization

noise [1]. As a result, a multi-bit modulator with odd levels is often used in the audio DACs, though single-bit modulator has inherent good linearity.
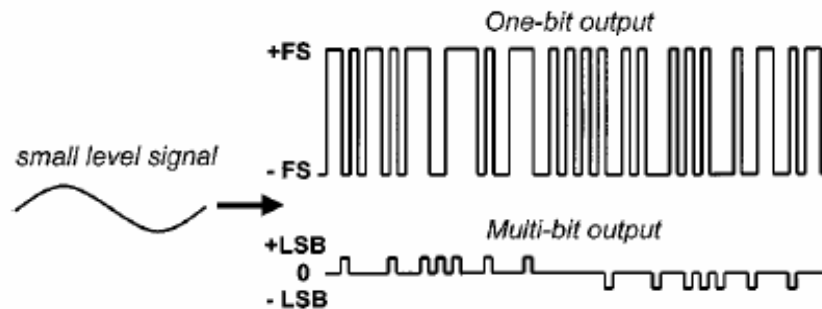


**Figure 2-8 Multi-bit and one-bit quantization**

Based on the structure shown in Figure 2-6, many delta-sigma audio DAC have been reported. In [2], a low-voltage and low-power audio DAC with 90 dB dynamic range for portable use was presented. A third-order modulator was used and a 15-level direct charge transfer (DCT)-switched-capacitor internal DAC was built. DWA algorithm was used in the design to suppress its nonlinearity. A 120 dB dynamic range DAC for DVD-audio was reported in [1]. A third-order modulator and a 31-level switched-capacitor internal DAC with hybrid filter were used in the design. The concept of partial DWA was introduced and implemented here. Another low-power audio DAC was presented in [6]. Un-symmetrical DWA was used and the concept of $SNR_{out}$ was introduced.

## 2.6    Conclusion

The fundamentals to the delta sigma DACs are described in this chapter. After comparing Nyquist sampling and oversampling, the noise shaping technique is reviewed. The unit-element DAC and the nonlinearity introduced by its mismatch errors are discussed. A general delta sigma audio DAC structure and the function of each block are presented. Finally, the features of the audio DACs are presented.

# Chapter 3   Digital interpolation filter and delta sigma modulator

As shown in Figure 2-6, the first block in a delta sigma audio DAC is an interpolation filter followed by a delta sigma modulator. In this chapter, the design of a digital interpolator with a 128 up-sampling factor and a third-order, seven-level delta sigma modulator for testing purpose are described.

## 3.1    Digital interpolation filter design
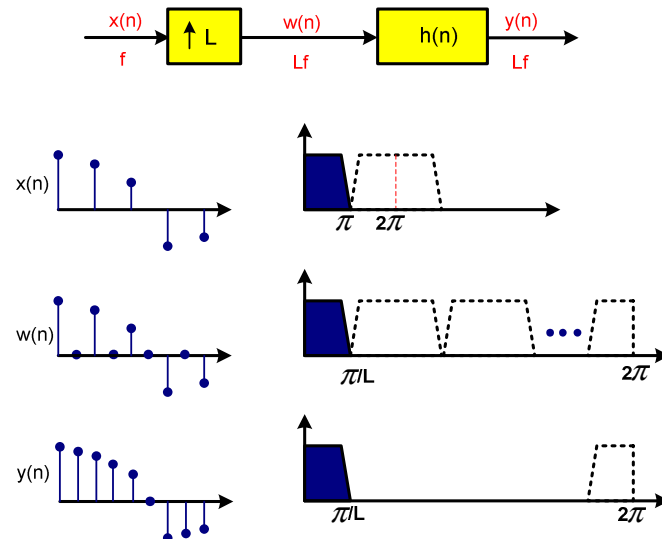


**Figure 3-1 Interpolator and its spectrum**

The interpolation filter used in the delta sigma DAC is built by an up-sampler and a lowpass filter as shown in Figure 3-1. An up-sampler with an up-sampling factor L is a device which inserts L-1 zero-valued samples between two consecutive samples of the input sequence x(n). The output of the up-sampler, w(n), now works at rate $L \cdot f_s$ and images are introduced due to this insertion

process. A following digital lowpass filter h(n), thus, is used to remove those images which replace the inserted zero value samples with proper values in time domain. The output y(n) is then a sequence with the rate $L \cdot f_s$ which contains all the signal components as x(n) does. The signals x (n), w (n) and y(n) are shown in Figure 3-1, both in time and frequency domains.

Because a finite-impulse-response (FIR) filter has linear phase response and good stability [15], the digital lowpass filter is typically realized using a FIR filter with the transfer function

$$H(z) = \sum_{n=0}^{N} h(n) \cdot z^{-n} \qquad \text{(3-1)}$$

here, the impulse response h (n) is symmetric which means h (n) =h (N-n). The filter order N can be calculated approximately by Equation 3-2 given the passband ripple $\delta_p$ , the stopband attenuation $\delta_s$ and the normalized transition bandwidth $\omega_s - \omega_p$ [15]

$$N \approx \frac{-20\log\left(\sqrt{\delta_s \delta_p}\right) - 13}{\dfrac{14.6}{2\pi}\left(\omega_s - \omega_p\right)} \qquad \text{(3-2)}$$

As can been seen from Equation 3-2, the filter order is proportional to its sampling frequency ( $\omega = \dfrac{2\pi f}{f_s}$ ) and inversely proportional to its transition bandwidth.

In a multi-rate system with a large oversampling ratio, using a single up-sampler and a single lowpass filter often leads to the high computation complexity [15]. By decomposing an up-sampling factor L into products of several integers $L_1$ $\cdots$ Ln and cascading the single stage realization of each up-sampling factor, a multi-stage implementation of such an interpolator is realized and is often adopted to avoid the high computation complexity.
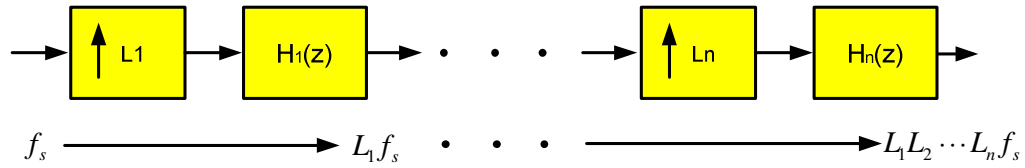


**Figure 3-2 Multi-stage interpolator**

When a multi-stage structure as shown in Figure 3-2 is used, the first digital lowpass filter is the most complex one to be designed since the transition band for this filter is often very small. For example, if sampling frequency is 48 kHz and the audio signal bandwidth is considered as 20 kHz, the transition band for the first filter is only 48/2-20=4 kHz. As Equation 3-2 indicates, this small transition band causes a large filter order N. For a trade-off method, in this case, signal components between 20 ~ 24 kHz can be allowed to mix with their mirror components, which doubles the transition band to 8 kHz. Given the same passband ripple and stopband attenuation, the filter order is now reduced to N/2. For the next following lowpass filters, larger transition bands make their order much smaller than N/2. If the up-sampling factor is equal to 2, a half band lowpass filter is a

hardware efficient implementation for $H_i(n)$ because around 50% of its coefficients are zeros [15]. The ripple in passband and attenuation in stopband should be also properly set to avoid a huge computation and complex hardware. Finally, the last stage of the interpolation filter is often implemented by using a digital sinc filter whose transfer function is given by [3]

$$H(z) = \left( \frac{1}{N} \frac{1 - z^{-N}}{1 - z^{-1}} \right)^k \qquad \qquad \textbf{(3-3)}$$

where N is the interpolation factor.

Figure 3-3 shows the designed interpolator. $H_i(z)$ is realized by a half band filter and the transition band is overlapped with its mirror components. The input is a 24-bit sine signal with a sampling frequency of 48 kHz and the output signal has a rate of 6.144 MHz which is interpolated by a factor of 128. The output spectrum of the designed interpolator with this input is given in Figure 3-4 and the signal bandwidth is 20 kHz (the dotted line is the integrated PSD).
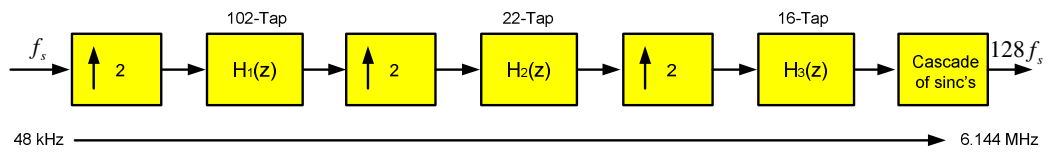


**Figure 3-3 Implemented interpolator**
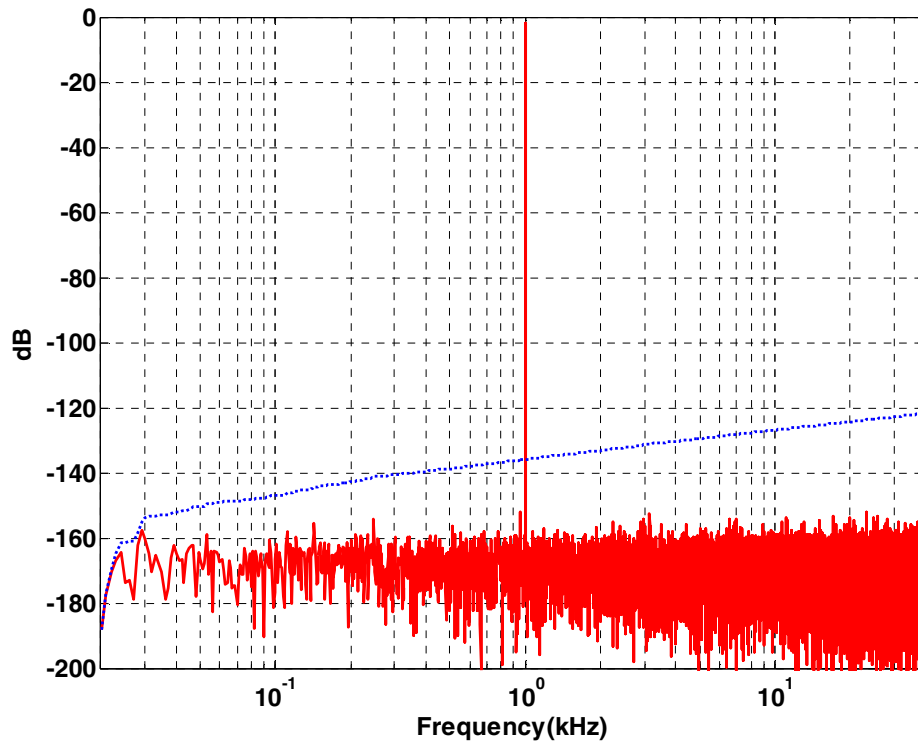
**Figure 3-4 Output spectrum of the designed interpolator**

## 3.2    Delta sigma modulator design

As shown in Figure 2-6, the delta sigma noise shaping loop reduces the word-length of its input signal, N1, to a few bits, M. A large amount of out of band quantization noise is generated during this process, and a lowpass, analog reconstruction filter needs to be used to remove that noise. To reduce the design complexity for the reconstruction filter, a multi-bit modulator (M>1) is typically desirable instead of a single-bit modulator although the single-bit modulator has inherent good linearity. Unfortunately, using a multi-bit noise shaping loop

requires a dynamic element matching (DEM) block which is often needed to suppress the DAC mismatch errors.

**Table 3-1 Modulator specifications**

| parameter | Value |
|---|---|
| Input sampling rate | 48 kHz |
| Signal bandwidth | 20 kHz |
| Signal-to-noise ratio | 120 dB |
| Modulator sampling rate | 6.144 MHz |
| Internal DAC levels | 7 |

With the specification listed in Table 3-1, a third-order modulator with the standard cascade-of-integrators, feedback (CIFB) structure [17], as shown in Figure 3-5, was implemented in Simulink. The maximum out-of-band gain of NTF (NTFmax) was set at 1.9 to make sure the loop was stable. The coefficients for the modulator were obtained by using delta-sigma toolbox [17] and are given in Table 3-2. These values are scaled so that the maximum values of the internal states stay less than one. Since this application is software, the word length can be realized by the computer default length which is considered to have infinite accuracy. In the hardware implementation, those scaled values should be expressed as the closest summation of the powers of 2 which are called quantized coefficients. Enough word length should be used to make sure those quantized values do not change the noise transfer function too much [3].
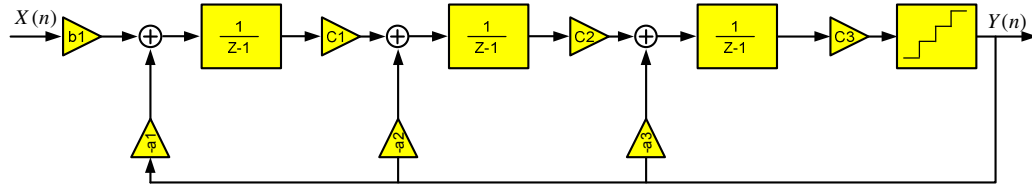
**Figure 3-5 The modulator implementation**

Combining this modulator with the designed interpolator given in subsection 3.1 and applying a -2 dBFS sine input signal provides us with the output spectrum of this subsystem which is shown in Figure 3-6 (the dotted line is the integrated PSD). The signal bandwidth is 20 kHz and the integrated noise is around 125 dB which satisfies the test requirement for the designed audio DAC.

**Table 3-2 Modulator coefficients**

| Coefficient | Before | After scaling |
|:-----------:|:------:|:-------------:|
| a(1) | 0.0347 | 0.0313 |
| a(2) | 0.0800 | 0.0751 |
| a(3) | 0.1340 | 0.1427 |
| b(1) | 0.0347 | 0.0313 |
| c(1) | 0.4802 | 0.5000 |
| c(2) | 0.8808 | 1.0000 |
| c(3) | 9.2460 | 8.6832 |
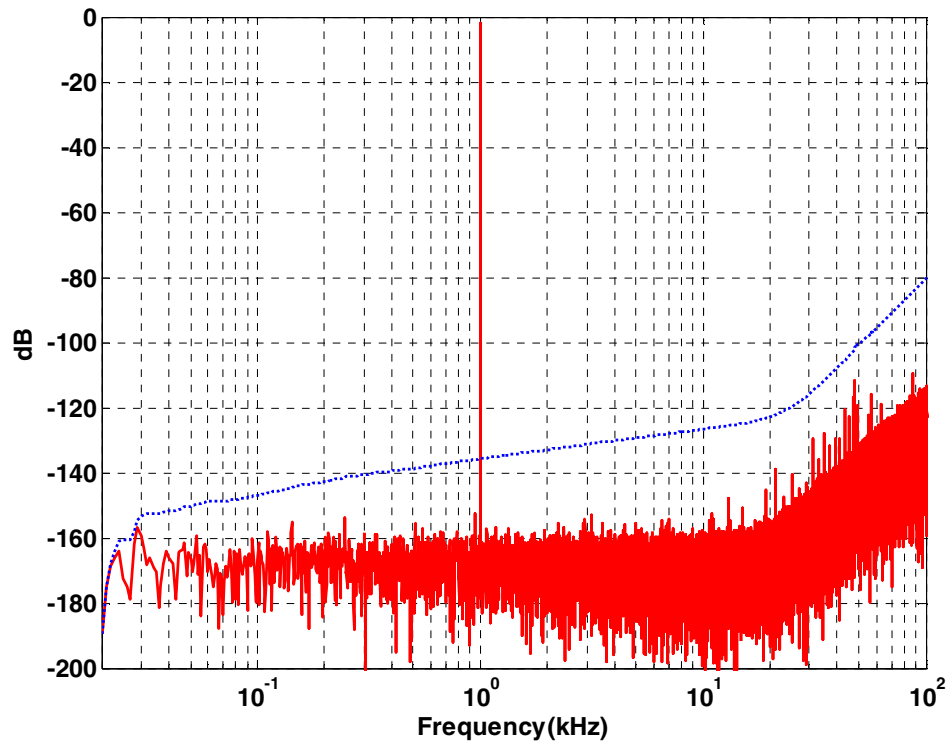
**Figure 3-6 Output spectrum of the modulator and interpolator**

## 3.3 Conclusion

An interpolator with a 128 interpolation factor and a third-order delta sigma noise shaping loop with seven output levels have been implemented in Matlab and simulink for the audio DAC test purposes. Simulation results show that the design subsystem satisfies the test requirements for the audio DAC which is presented in chapter 6.

## Chapter 4   Split-set data weighted averaging

Multi-bit quantization improves the stability and the signal-to-quantization-noise performance of delta sigma converters, but it also necessitates the use of dynamic element matching (DEM) to filter the nonlinearity error in the signal band. Data weighted averaging (DWA) is the most widely used DEM algorithm, due to its simplicity and the speed with which it equalizes the usage of the unit elements of the DAC [16]. However, for signal levels rationally related to the full-scale output of the DAC, DWA generates tones, so its spur-free dynamic range (SFDR) performance may be poor. In audio applications, in-band tones generated by the basic DWA algorithm are unacceptable. Several modifications of the basic DWA algorithm, based on randomization, have been proposed [18] [19] [20]. They break up the DWA tones; however, they all disturb the equal unit-element usage pattern, and hence raise the noise floor reducing the signal-to-noise ration (SNR). A novel element selection algorithm, split-set data weighted averaging (SDWA), was developed [21]. SDWA improves the SFDR of DWA significantly while keeping the SNR high.

## 4.1   The tone generation of DWA algorithm

DWA uses the unit-element cyclically in order to make the long-term average use of each unit element in the DAC the same. The power spectrum of mismatch errors at DAC output is given by [3]

$$E(\omega) = \left|1 - e^{-j\omega}\right|^2 \cdot S(\omega) \tag{4-1}$$

As can be seen, first-order DAC mismatch errors shaping is achieved by using DWA. However, if the DAC input is a DC or a low-frequency signal, the mismatch errors are not first-order shaped [3]. For example, for a six-element DAC with consecutive inputs 2, 2, 2, 2 $\cdots$, the selected unit elements are going to be (U1 U2), (U3 U4), (U5 U6), (U1 U2) $\cdots$ , then the output mismatch errors are periodic, which results in an undesired situation. With a random input signal, the maximum achievable resolution of a unit-element DAC with oversampling factor M is given by [22]

$$resolution = \log_2\left(\frac{\sqrt{3 \cdot N \cdot M^3}}{\pi \cdot \sigma_W \cdot \left(1 - \dfrac{1}{N}\right)}\right) \; [bits] \tag{4-2}$$

Here, $\sigma_W$ is the variance of the unit elements and N is the number which signifies unit elements. For a DC input signal to the same unit-element DAC, the spectrum of the mismatch errors depends on the DC levels [22]. Generally, a low order error component of high power is folded back into the baseband for some values of DC inputs and the equivalent resolution is then decreased.

## 4.2  The SDWA algorithm

In order to overcome the tone problem, a novel algorithm, named split-set data weighted averaging (SDWA), was proposed. SDWA operates by splitting the unit element set into subsets in a special way, and randomizing each subset independently. For an N-element DAC, SDWA is carried out in the following steps:

1.     Apply DWA to the N unit elements of the DAC for M-1 clock cycles, i.e., use them consecutively in a cyclic manner [14];

2.     In clock cycle M (where M may be predetermined, or identified by a pseudorandom digital signal reaching a predetermined value), split the set of all unit elements into two subsets. Subset $S_K$ contains elements 1 through k, where k is the highest unit-element index used in clock cycle M; its complement $\overline{S_K}$ contains elements with indices k+1 through N;

3.     Rotate or scramble all elements of $S_K$ within the subset $S_K$, and similarly rearrange the elements of $\overline{S_K}$ internally within the subset $\overline{S_K}$.

4.     Return to Step 1, starting with the unit element now occupying position k+1.

It is easy to see that this randomization only minimally disturbs the equal usage of unit elements, and specifically that all unit elements are used at least L

times before any one is used L+1 times. Hence, the noise floor should not be significantly affected by the process, while the tones are prevented by the randomization performed in Step 3. M determines the trade-off between SFDR and SNR: for larger SFDR, M should be smaller; for higher SNR, it should be larger.

In Figure 4-1, SDWA is illustrated for a seven-level DAC with the input sequence 4, 3, 1, 5. We assume M=1, so that scrambling is performed in all clock periods. The initial order of the unit elements is U1, U2, U3, U4, U5, U6. Starting with an input code 4, unit elements U1, U2, U3 and U4 are used. Then the unit elements are split into two subsets (U1, U2, U3, U4) and (U5, U6), which are rotated by one position independently in order to give (U2, U3, U4, U1) and (U6, U5). The new order of all unit elements is thus (U2 U3 U4 U1 U6 U5). A second input data 3 is then going to chose unit elements (U6 U5 U2). Again the unit elements are split into (U2), (U3 U4 U1 U6 U5) and are rotated separately. The new order of unit elements now is (U2 U4 U1 U6 U5 U3). Figure 4-1 illustrates the rotations for subsequent inputs 1 and 5.
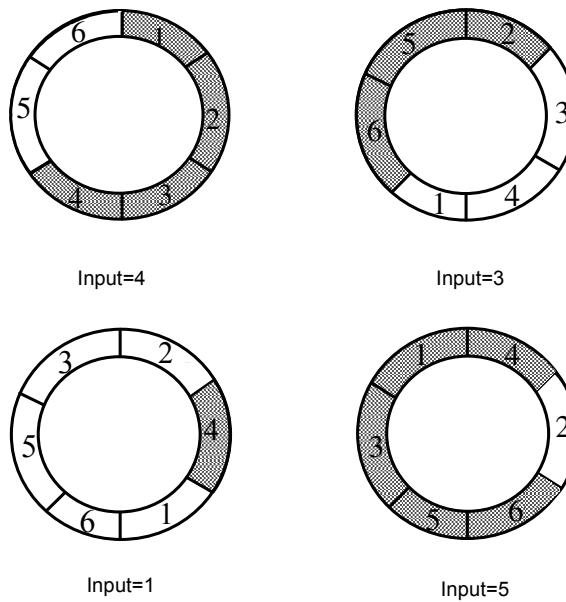
**Figure 4-1 The SDWA algorithm**

## 4.3    Comparison of SDWA and DWA

To see the effectiveness of SDWA, the simulations of both DWA and SDWA are given here. Given a -45 dBFS input, Figure 4-2 shows the output spectrum of an ideal DAC without mismatch errors which gives an 81.49dB SNDR in 20 kHz bandwidth. Applying DWA to a practical DAC with 1% unit-element mismatch errors will reveal an output spectrum which is shown in Figure 4-3. SNDR now comes down to 62.20dB and the maximum in-band tone is -116.77dB. Output spectra for the same DAC using SDWA with M=5000 and M=10000 are shown in Figure 4-3 and Figure 4-5 respectively. While the SNDR is similar, the maximum inband tones are around 15dB smaller comparing with the DWA. As can be seen from those simulation results, SDWA does improve the DAC performance.
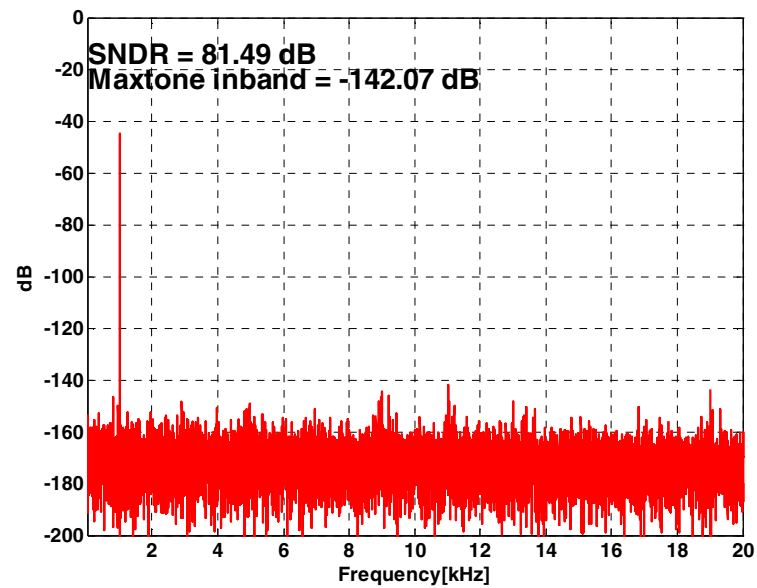
**Figure 4-2 Output spectrum of an ideal DAC**
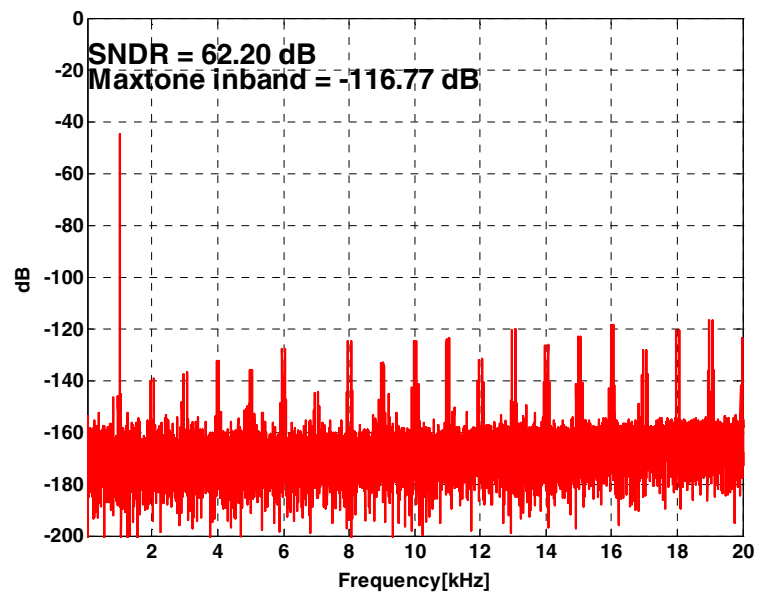


**Figure 4-3 Output spectrum with DWA**
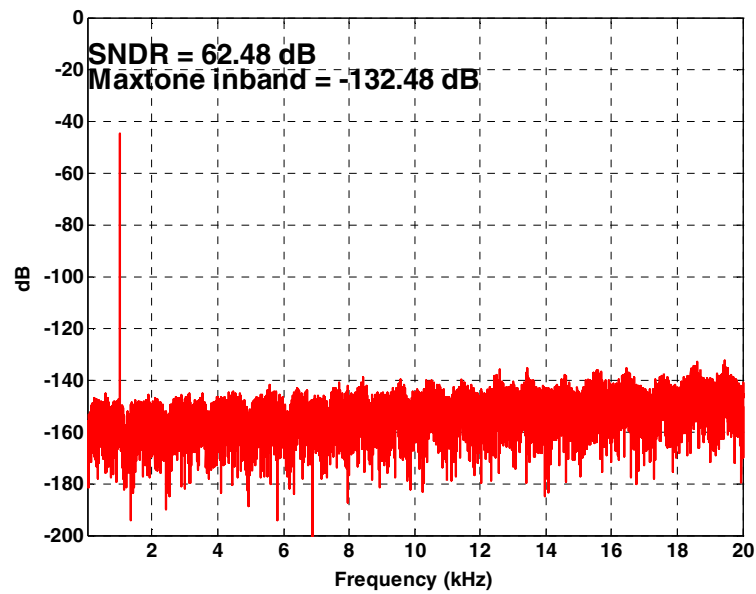
**Figure 4-4 Output spectrum with SDWA (M=5000)**
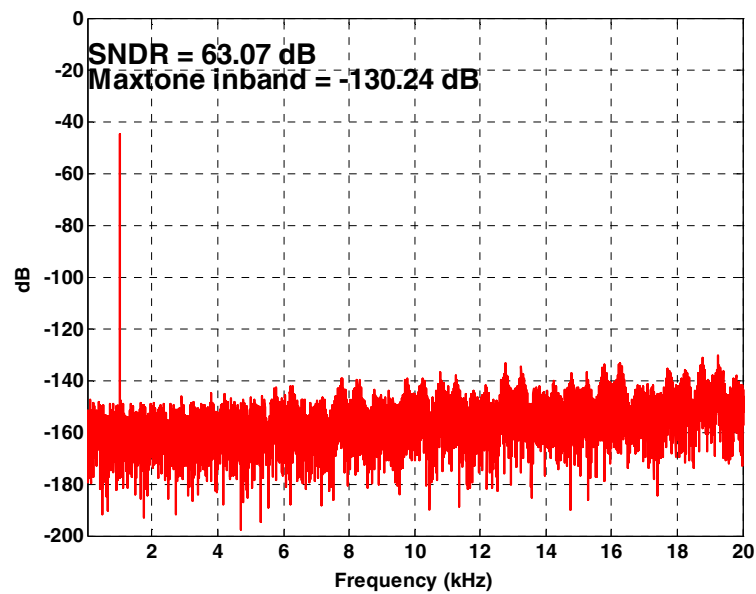


**Figure 4-5 Output spectrum with SDWA (M=10000)**

## 4.4    An efficient circuit implementation of SDWA

The block diagram of a fast and efficient gate-level implementation of the proposed SDWA algorithm for a seven-level unit-element DAC with M=16 is shown in Figure 4-6. A simple shifting is used in this implementation to change the order of the unit elements in the subsets which indicates it is a cost-effective implementation which has low latency.
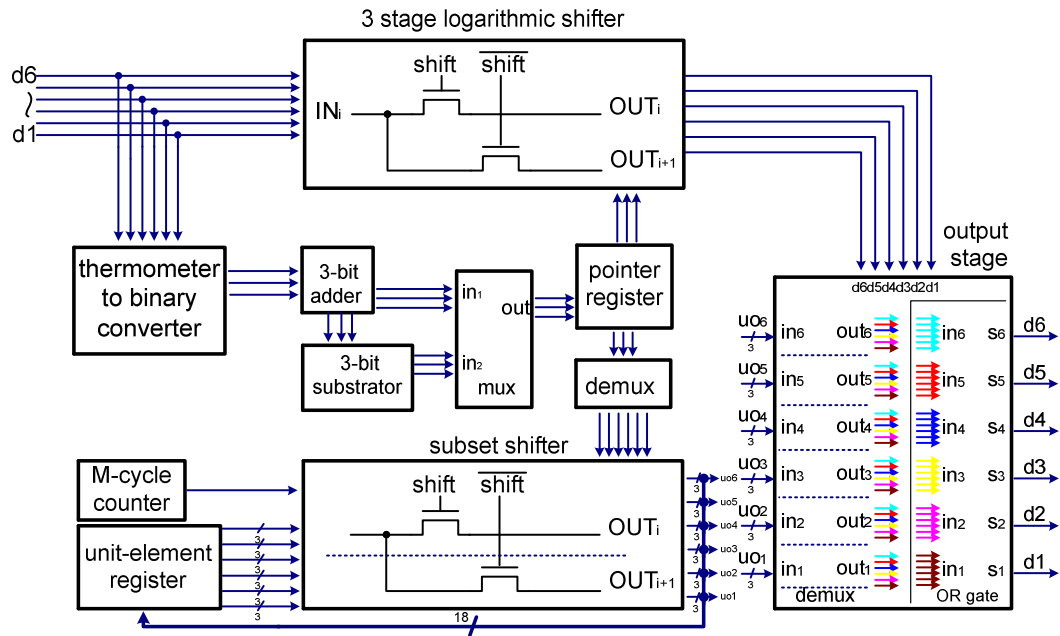


**Figure 4-6 The SDWA implementation**

In Figure 4-6, d1 ~ d6 are six input thermometer bits, a 3-stage logarithmic shifter is used to rotate these thermometer bits to generate DWA data required by the SDWA algorithm. Subset shifter is used to shift the order of unit elements every M cycle. The unit-element register stores the updated element order given by the output of the subset shifter. The output block is built by demuxes and OR gates

array to form the final SDWA data. As can been seen, the implementation does not add much additional delay comparing to basic DWA implementation.

For the input codes given by (4, 3, 1, 5), the details of this implementation are described as: the unit elements on chip is (6, 5, 4, 3, 2, 1) which is fixed and can not be changed. The initial order of the unit elements, (6, 5, 4, 3, 2, 1), is stored in the register. So the demuxes' inputs at the output stage is (6, 5, 4, 3, 2, 1), DWA generates the code 001111 for input code 4 which gives the output of demuxes out6=(000000), out5=(000000), out4=(001000), out3=(000100), out2=(000010), out1=(000001). These six groups of demux outputs then drive six OR gate to form the SDWA output (001111) which selects the unit elements (U4, U3, U2, U1). Then the stored unit-element order is updated to (5, 6, 1, 4, 3, 2) which is also the inputs of demuxes, DWA generates the code 110001 for input code 3 which makes the output of the demuxes out6=(010000), out5=(100000), out4=(000000), out3=(000000), out2=(000000), out1=(000010). So the SDWA output is (110010), since the unit elements on chip is fixed which means (110010) it is going to choose the on chip unit elements U6 U5 and U2. The stored unit-element order is now updated to (3 5 6 1 4 2) and DWA then generates the code 000010 for input code 1 and the outputs of the demuxes are out6=(000000), out5=(000000), out4=(000000), out3=(000000), out2=(001000), out1=(000000) which gives the SDWA output (001000). Unit element U4 is going to be selected and then the stored unit-element order is updated to (1, 3, 5, 6, 2, 4). DWA generates the code 111101 and the outputs of the demuxes are out6=(000001),

out5=(000100), out4=(010000), out3=(100000),   out2=(000000), out1=(001000).

So the SDWA output is 111101 which is going to select U6 U5 U4 U3 U1.

Checking above results with Figure 4-1, the accuracy is verified. Table 4-1 gives

the summary of above operation.

**Table 4-1 SDWA circuit operation**

| Din | 4 | | | 3 | | | 1 | | | 5 | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| (6) | 0 | 000000 | (5) | 1 | 010000 | (3) | 0 | 000000 | (1) | 1 | 000001 |
| (5) | 0 | 000000 | (6) | 1 | 100000 | (5) | 0 | 000000 | (3) | 1 | 000100 |
| (4) | 1 | 001000 | (1) | 0 | 000000 | (6) | 0 | 000000 | (5) | 1 | 010000 |
| (3) | 1 | 000100 | (4) | 0 | 000000 | (1) | 0 | 000000 | (6) | 1 | 100000 |
| (2) | 1 | 000010 | (3) | 0 | 000000 | (4) | 1 | 01000 | (2) | 0 | 000000 |
| (1) | 1 | 000001 | (2) | 1 | 000010 | (2) | 0 | 000000 | (4) | 1 | 001000 |
| | | 001111 | | | 110010 | | | 001000 | | | 111101 |

## 4.5    Building blocks: subset shifter and SDWA output stage

The key building blocks for the SDWA circuit are the logarithmic shifter,

the subset shifter and the output stage. The design of a logarithmic shifter can be

its standard design [23].

### 4.5.1 Subset shifter

Subset shifter is the key part for updating the stored unit-element order.

Figure 4-7 shows six-bit circuit implementation. The pointer position divides six

unit elements into two subsets with the control of shift/shiftb signals. Input data D6 ~ D1 will rotate separately in each subset. The rotated data B6 ~B1 are stored in the unit-element register as the new order.
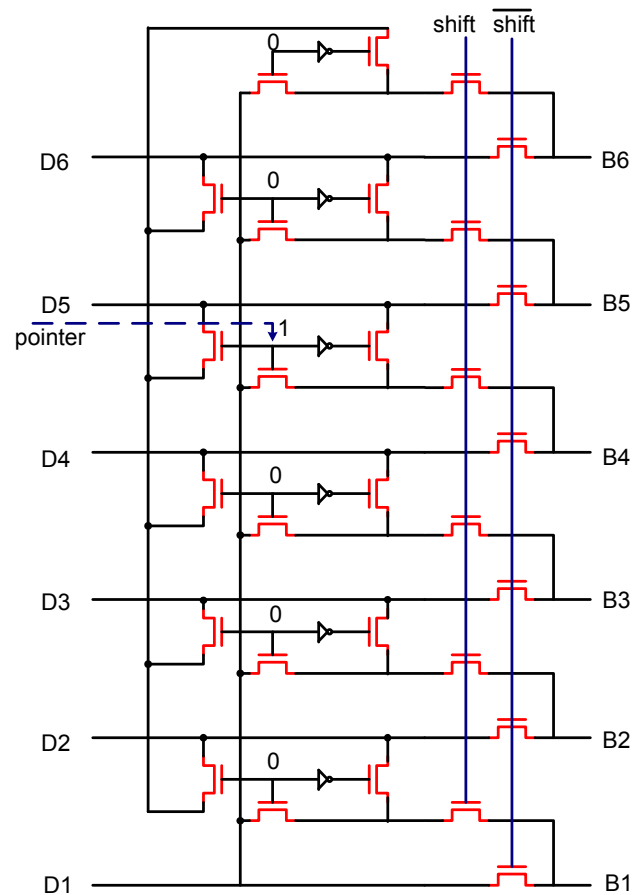


**Figure 4-7 The subshifter**

## 4.5.2 SDWA output stage

SDWA output stage is constructed by six demuxes and six OR gates as shown in Figure 4-8. The DWA data is the enable signal for these demuxes, if DWA input is 1, the demux outputs the data according to the input, otherwise the

demux output is 000000. Each bit of the output (6-bit) of each demux goes to the six OR gates, respectively.
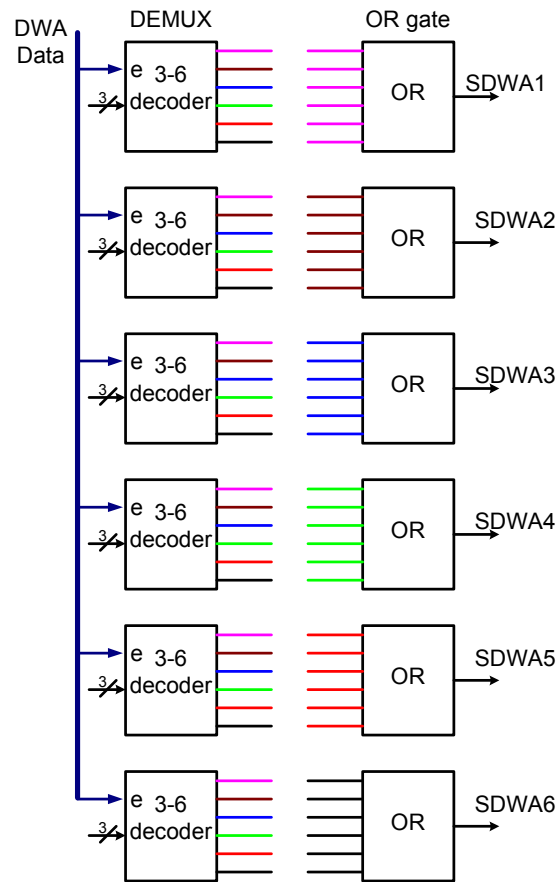
**Figure 4-8 Output stage**

## 4.6   Simulations of the SDWA circuit

Figure 4-9 shows the SDWA circuit simulation results with M = 16 and clock frequency 6.25 MHz. Figure 4-10 shows simulation results with a faster clock frequency 50 MHz. As can be seen from the plots, the circuit can perform its function with high speed. Given a 3.3V power supply, the power consumptions are

0.538 mA and 1.926 mA, respectively. Six hundred and seventy one transistors were used to build this SDWA circuit.
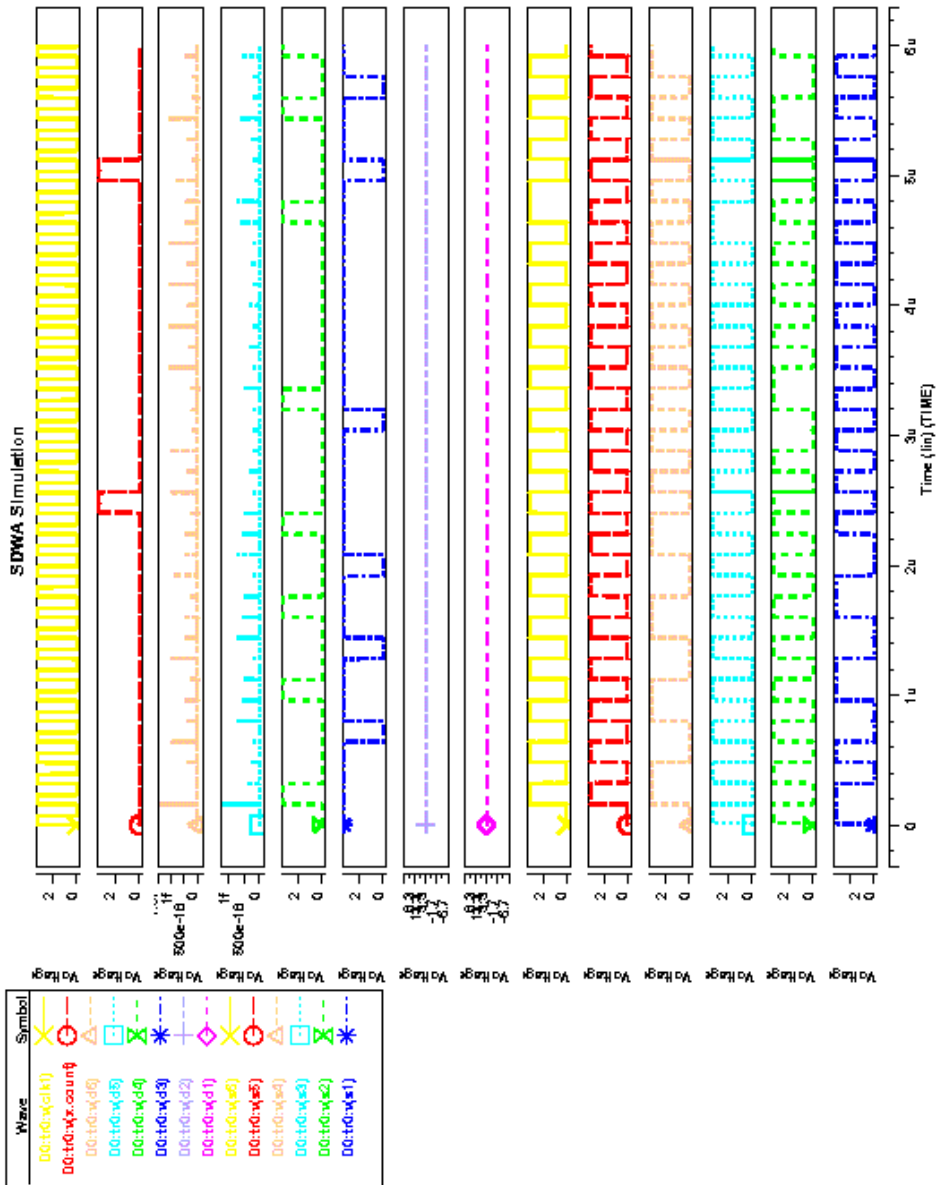
**Figure 4-9 Simulation with 6.25 MHz**
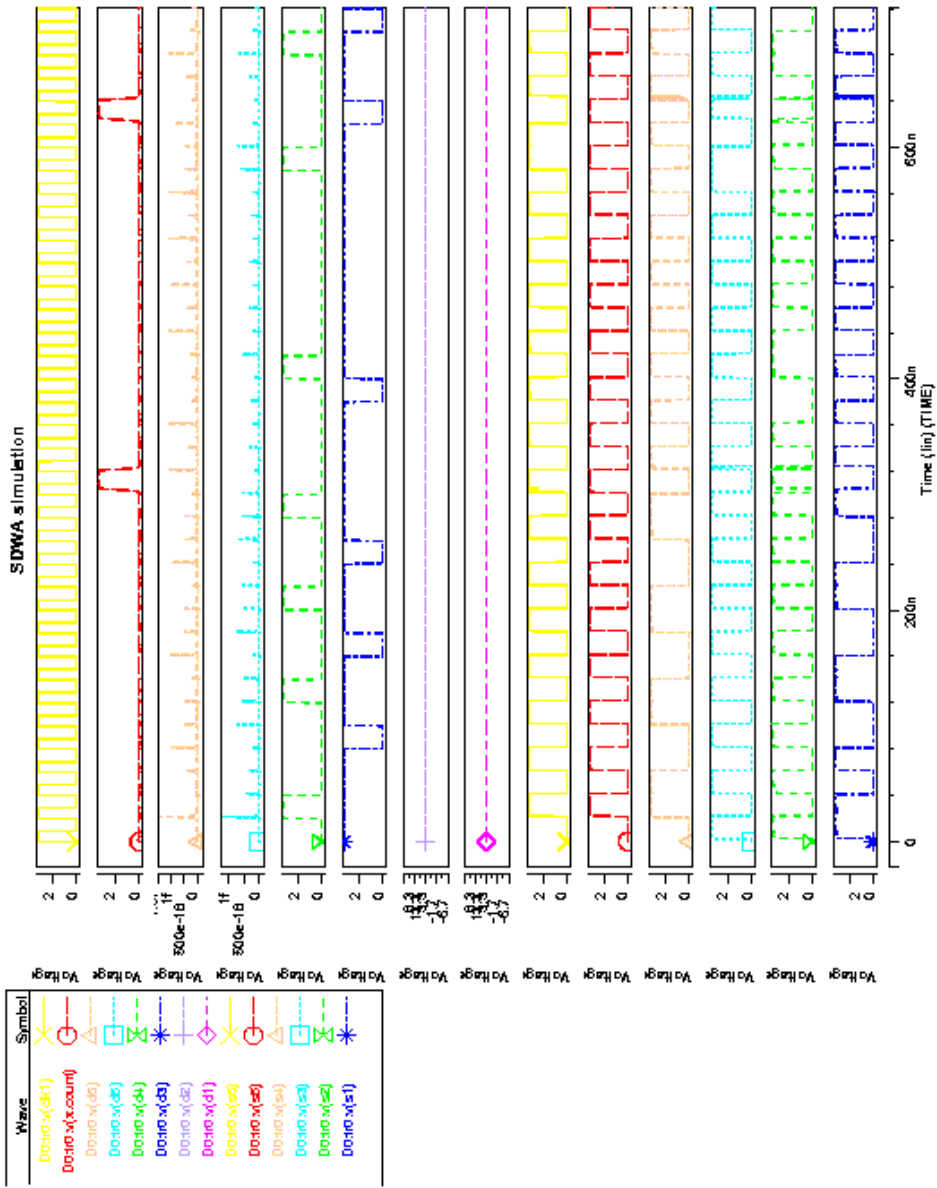
**Figure 4-10 Simulation with 50 MHz**
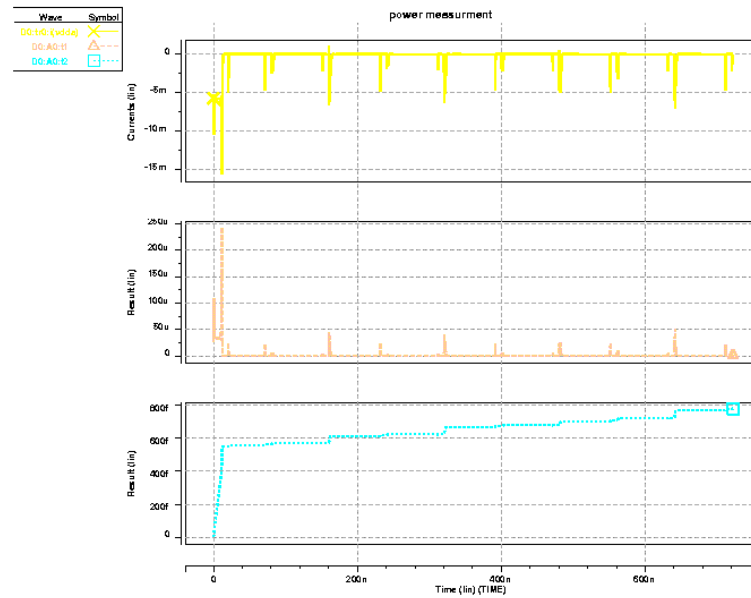
**Figure 4-11 Power consumption with 6.25 MHz clock**
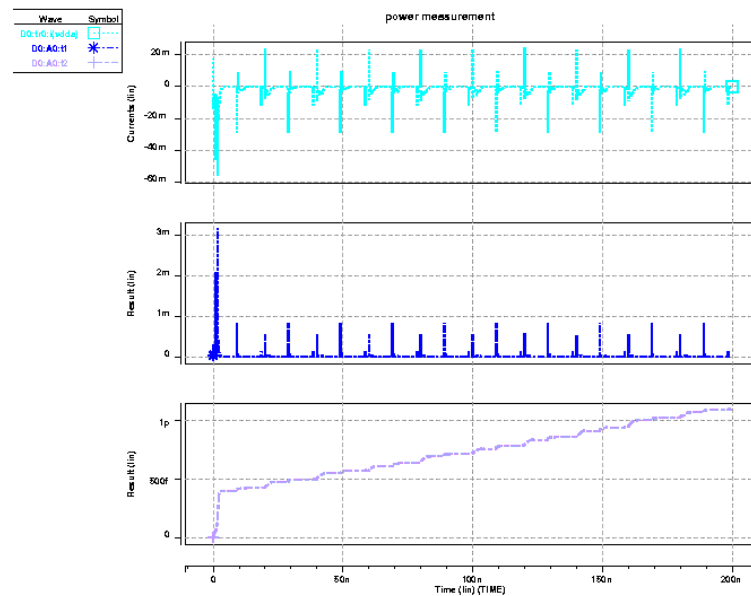


**Figure 4-12 Power consumption with 50 MHz clock**

## 4.7    Conclusion

The details of the proposed split-set data weighted averaging algorithm have been discussed and its ability to overcome the tone generation in basic DWA algorithm was demonstrated. The cost-effective and low-latency gate-level implementation was given. Simulation results show this implementation can meet the requirements for high-speed applications.

# Chapter 5   Distortion in the headphone driver and an experimental headphone driver

The headphone driver is a key part in the audio applications which may define the performance of the overall system. A driver is an amplifier which can drive a low resistance and large capacitance load and has a small quiescent current. There are many different drivers (Class A, Class B, Class AB and Class D) that are classified according to their output stages. A Class A output stage uses the same transistors for both halves of the waveform and thus it has good linearity but poor efficiency due to its nonzero DC current. With a better efficiency, a Class B output stage uses complimentary transistors for each half of the waveform and no output present, given a zero or small input, because of its zero DC current which causes a so called crossover distortion. A Class AB output stage biases the transistors with a small non-zero quiescent current in order to eliminate the crossover distortion which degrades the efficiency. All drivers with above output stages are sometimes called linear drivers. A Class D amplifier is popular in audio amplifiers nowadays. It is a switching (PWM) amplifier with inherent high efficiency due to fully on and off switches [24]. In contrast to the low-frequency control signal used in conventional output stages, the switching output stage is often controlled by a high-frequency digital signal. Depending on the order and cut-off frequency of the demodulation filter, the output spectrum from a Class D amplifier always contains some level of frequency intermodulation (IM) components around the switching

frequency and/or its harmonics as shown in Figure 5-1 [24]. Thus, it has greater

noise as compared with the other amplifiers.
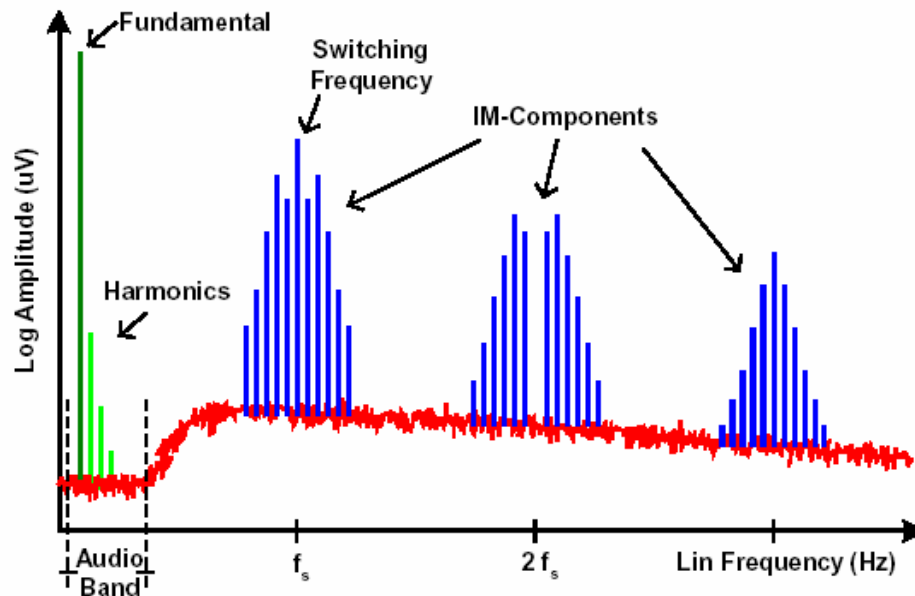


**Figure 5-1  The typical output spectrum of a class D amplifier**

In this chapter, the distortions in the linear headphone drivers are going to

be analyzed and an experimental headphone driver with a class AB output stage is

then described. Specially, the designed headphone driver is integrated with a

lowpass filter which can serve as the analog reconstruction filter in an audio DAC.

## 5.1    Distortions in the headphone driver

Given an input Vin, the output of a nonlinear circuit can be expressed by a

Taylor expansion

$$V_{out} = k_1 V_{in} + k_2 V_{in}^2 + k_3 V_{in}^3 + \cdots \tag{5-1}$$

For a sinusoid input signal, a·cos(ωt), Equation 5-1 becomes

$$
\begin{aligned}
V_{out} &= \frac{k_2 a^2}{2} + \left( k_1 a + \frac{3k_3 a^3}{4} \right) \cos(\omega t) + \frac{k_2 a^2}{2} \cos(2\omega t) + \frac{k_3 a^3}{4} \cos(3\omega t) + \cdots \\
&= a_0 + a_1 \cos(\omega t) + a_2 \cos(2\omega t) + a_3 \cos(3\omega t) + \cdots
\end{aligned}
\tag{5-2}
$$

The kth harmonic distortion (HD$_k$) is defined as

$$HD_k = \frac{a_k^2}{a_1^2} \quad (k > 1) \tag{5-3}$$

The total harmonic distortion (THD) can be defined as

$$THD = \frac{a_2^2 + a_3^2 + \cdots + a_k^2 + \cdots}{a_1^2} \tag{5-4}$$

Because the audio bandwidth is 20 kHz, the largest distortion in a headphone driver is found to 20 kHz. When the input signal is 1 kHz (a typical test frequency), the k is 20 in Equation 5-4. When the headphone driver is in a feedback loop, the low distortion can be achieved by increasing the loop gain as long as the loop gain is large enough in the signal band. In some books [25] [26], the distortions are analyzed using the nonlinear coefficients and complicated equations are introduced. Here, distortions at the amplifier's input stage, output stage and in a feedback loop are examined by directly analyzing the circuits themselves.

## 5.1.1 The distortions at amplifier input stage
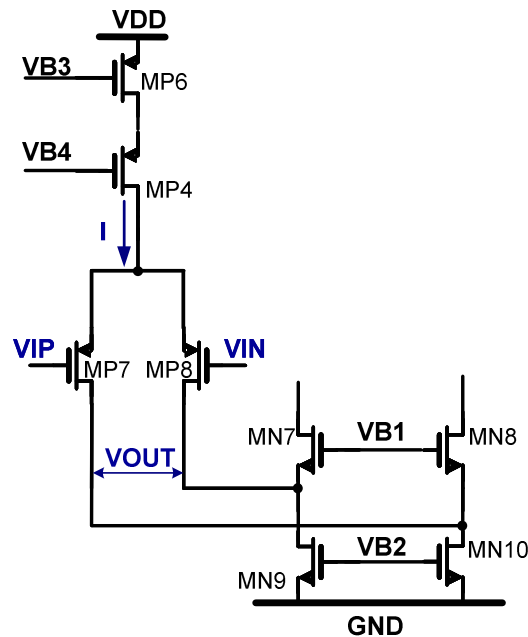


**Figure 5-2  The differential input pair**

Figure 5-2 shows the differential input pair for a folded-cascade amplifier. Assuming no mismatches between the transistors MP7 and MP8, distortion caused by this input stage can be calculated by finding its output voltage using the square-law MOSFET model.

$$v_{out} = \frac{(v_{ip} - v_{in})r_0 I}{2} \cdot \frac{\sqrt{4\Delta^2 - (v_{ip} - v_{in})^2}}{\Delta^2} \tag{5-5}$$

Here, $r_o$ is the resistance at the output node, $\Delta = V_{gs} - V_{th}$ is overdrive voltage of the input differential pair at the balance situation (with $I/2$ flowing through each

device) and I is the bias current provided by high output impedance current source (transistors MP6 and MP4). Because the Taylor expansion of sqrt(1+x) is given by

$$T(x) = \sum_{k=0}^{\infty} \frac{f^{(k)}(a)}{k!}(x-a)^k \qquad \textbf{(5-6)}$$

Equation 5-5 can be rewritten as

$$v_{out} = \frac{r_o I}{\Delta} \cdot (v_{ip} - v_{in}) - \frac{r_o I}{8\Delta^3} \cdot (v_{ip} - v_{in})^3 - \frac{r_o I}{128\Delta^5} \cdot (v_{ip} - v_{in})^5 \cdots \qquad \textbf{(5-7)}$$

As can be seen from Equation 5-7, no even order distortion is introduced due to no mismatching between MP7 and MP8 assumption. The odd order distortion can be reduced by enlarge overdrive voltage $\Delta$. Given a fixed bias current, increasing $\Delta$ means decreasing transconductance, $g_m$, which reduces the small signal gain. At the same time, larger $\Delta$ means a larger Vds is needed to bias the transistor at the saturation region. This is an undesired result and simulations should be done to find the optimized $\Delta$. It is clearer by finding the equivalent Gm of the input stage which is given by

$$G_m = \frac{\partial i}{\partial(v_{ip} - v_{in})} = \frac{I}{\Delta} - \frac{3I}{8\Delta^3} \cdot (v_{ip} - v_{in})^2 - \frac{5I}{128\Delta^5} \cdot (v_{ip} - v_{in})^4 \cdots \qquad \textbf{(5-8)}$$

Equation 5-8 shows that a relatively constant Gm can only be obtained by increasing $\Delta$ because the input signal is not controllable in general (in a feedback loop, increasing loop gain leads to a smaller input signal).

So far, transistors MP7 and MP8 are assumed to be a perfect match. If there are mismatches between these two input transistors, the even order harmonics are going to be present. These calculations are much more complex. As long as we take care of device matching, both in the design and layout, the second harmonic distortion should be small compared with the third one and the THD performance is not affected a lot.

## 5.1.2 The distortions at amplifier output stage

Crossover distortions at the Class AB output stage may limit the distortion performance and can be minimized by setting a proper quiescent current. The major distortion for Class AB output stage may be caused by a large output swing which makes the output devices go into the triode region.
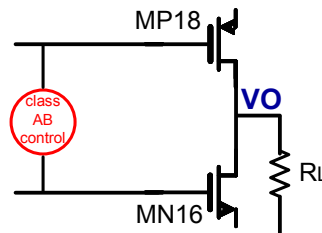


**Figure 5-3 the output stage**

For an output stage such as the one shown in Figure 5-3, when the transistor MN16 is in the saturation region, the incremental current through it is

$$i = \frac{2I}{\Delta} \cdot v_{in} + \frac{I}{\Delta^2} \cdot v_{in}^2 \tag{5-9}$$

Here, I is the bias current and $\Delta$ is overdrive voltage ($V_{gs}$-$V_{th}$). Equation 5-9 shows that the only parameter that can be controlled in the design to affect the distortions is $\Delta$. This is clearer when the equivalent transconductance Gm is calculated

$$G_m = \frac{\partial i}{\partial v_{in}} = g_m \cdot \left(1 + \frac{v_{in}}{\Delta}\right) \qquad (5\text{-}10)$$

Equation 5-10 shows that Gm is varying with a factor, $\frac{v_{in}}{\Delta}$. The only way to make Gm relatively constant is to make this factor small. Since $v_{in}$ is the input signal and can not be reduced in general, the only way is to increase $\Delta$ to achieve small distortion.

When the output transistor MN16 is working in the triode region, ignoring the effect of the transistor MP18, its output current becomes

$$i = -\frac{2v_{in}}{R_L} \qquad (5\text{-}11)$$

Given input $v_{in}$, this is a linear output current, thus, there is no distortion at the output. When transistor MP18 is considered, the distortion is still small, because the major current at the output is provided by transistor MN16 (MP18 works in the saturation region at this time and the distortion can be referred to Equation 5-9). Since the transistor changes from saturation region to triode region, this discontinuity causes distortion.

### 5.1.3 Distortion in a feedback system
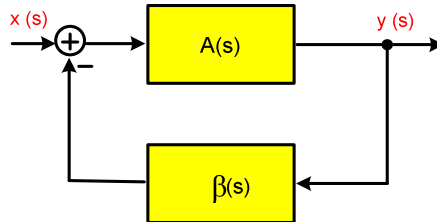


**Figure 5-4 A feedback loop**

As mentioned before, the distortion in an amplifier can be reduced in the feedback loop whose loop gain is large. In a general feedback system shown in Figure 5-4, the output is given by

$$H(s) = \frac{A(s)}{1 + A(s) \cdot \beta(s)} \tag{5-11}$$

Here, A(s) and β(s) are two stable systems. The loop gain is defined as

$$L(s) = A(s) \cdot \beta(s) \tag{5-12}$$

Equation 5-11 shows that the transfer function of A(s) is degraded by a factor 1+L(s). It can be proved that the distortion caused by the nonlinear effects of the system A(s) will be lowed by the factor 1+L(s) [26].

When the nonlinear effects of the feedback system β(s) is considered, its distortions are no longer reduced by loop gain. Suppose the input x(s) is linear, the

feedback forces the signal at the output of β(s) linear, so if β(s) is nonlinear, y(s) must be nonlinear too. This can also be seen from Equation 5-11 which can be expressed as 1/ β(s) with a large A(s). The output is the inverse of the feedback system. Then the distortions caused by β(s) limit the output distortion performance and a linear feedback should be used in a low distortion design.
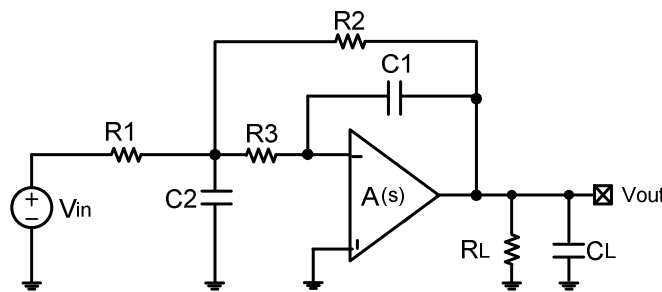


**Figure 5-5  Headphone driver in a feedback loop**

As shown in Figure 5-5, the headphone driver is put into a feedback loop and is configured as an analog lowpass Sallen-Key filter. The single-ended circuit is used for calculation simplification, and the loads $R_L$ and $C_L$ are considered part of the A(s). Although the system transfer function can be directly calculated, a different calculation is shown here to demonstrate the role of A(s) and β(s) in the distortions. The feedback transfer function, β(s), can be found by putting a signal at the node Vout and calculate the output at the negative node of the opamp input which is found to be

$$\beta(s) = \frac{R_1 R_2 R_3 C_1 C_2 s^2 + (R_1 R_2 + R_2 R_3 + R_1 R_3)C_1 s + R_1}{R_1 R_2 R_3 C_1 C_2 s^2 + (R_1 R_2 C_1 + R_2 R_3 C_1 + R_1 R_3 C_1 + R_1 R_2 C_2)s + R_1 + R_2} \qquad \textbf{(5-13)}$$

The transfer function from the input of the feedback system to the opamp negative node can be found by putting a signal at the node Vin and calculating the output at the negative node of the opamp input which is found to be

$$N(s) = \frac{R_2}{R_1 R_2 R_3 C_1 C_2 s^2 + (R_1 R_2 C_1 + R_2 R_3 C_1 + R_1 R_3 C_1 + R_1 R_2 C_2)s + R_1 + R_2} \quad \textbf{(5-14)}$$

The headphone driver feedback system shown in Figure 5-5 then can be represented as in Figure 5-6.



**Figure 5-6  Block diagram of the headphone driver in a feedback loop**

The transfer function of the system shown in Figure 5-6 can be found as

$$H(s) = -\frac{N(s) \cdot A(s)}{1 + A(s) \cdot \beta(s)} \quad \textbf{(5-14)}$$

and the feedback factor is

$$\frac{\beta(s)}{N(s)} = R_1 R_3 C_1 C_2 s^2 + (R_1 + R_3)C_1 s + \frac{R_1 R_3}{R_2} C_1 s + \frac{R_1}{R_2} \quad \textbf{(5-15)}$$

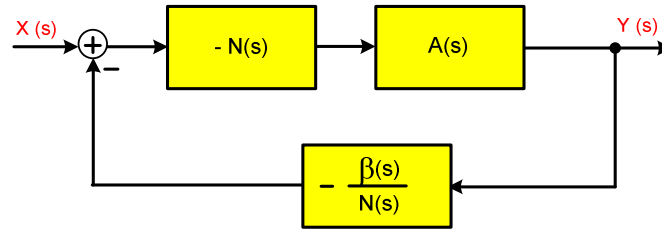As can be seen from Equation 5-15, the distortion in the feedback path can possibly be caused by the resistor R2, since the voltage across this resistor may have a large swing which is different with the input signal swing. Since this distortion is not suppressed by the loop, resistor R2 should be carefully laid out to make the system have linear feedback, and a general solution for this is to make R2 as long as possible [27]. At The distortions in the feed forward path now are mainly caused by the nonlinearity of the amplifier, A(s), since distortion in N(s) possibly caused by the resistor R2 has been minimized when the linear feedback has been realized.

Now, consider the distortion caused by opamp, A(s), which is a two-stage structure in the design. The largest contributions to the nonlinear distortion at the output of an amplifier originate from the circuit elements close to or at the output where signal swings are large, which has been proved [26]. In the headphone driver shown in Figure 5-5, the signal swing at the input of the amplifier is small, and distortions are mostly caused by the output stage (MP18 and MN17). Since the load at the output stage of the amplifier is dominated by the small headphone impedance which is 32 Ohms in the design, the gain of the second stage at low frequency can be approximately expressed as

$$A_2 = g_{m16} \cdot R_L \qquad \textbf{(5-16)}$$

and the overall gain can be increased by using a large $g_{m16}$ which means a large W/L ratio should be used for the transistors MP18 and MN16. The loop gain is

given by A(s) · β(s) which means large loop gain can be achieved by increasing the gain of A(s) and β(s). In the audio band, A(s) · β(s)=A(s)/(1+R2/R1) which means R2/R1 should be as small as possible. At the same time, the frequency response of the loop gain is mainly decided by A(s), which means the UGBW of the amplifier should be large enough to keep the loop gain large throughout the audio band.

In most low-distortion audio amplifier designs, three-stage structures are used instead of two-stage, due to its larger achievable DC gain and distortion suppressed by its local feedback[28] [29]. The two-stage folded cascade amplifier is however a good choice for combining high linearity and low complexity.

## 5.2    Prototype headphone driver design

Appling the techniques described in Section 5.1, a headphone driver with a feedback loop was designed. Such a structure can also be used as the analog reconstruction filter in a delta sigma audio DAC, as well as a driver.

### 5.2.1 Structure of the headphone driver

Figure 5-7 shows the structure of the designed headphone driver, it is configured as a Sallen-Key lowpass filter.
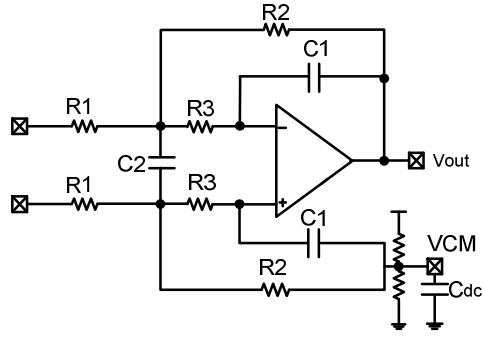
**Figure 5-7 Designed headphone driver**

The transfer function of the headphone driver is given by

$$H(S) = \frac{-R_2/R_1}{2 \cdot R_2 R_3 C_1 C_2 \cdot S^2 + (R_2 + R_3 + R_2 R_3/R_1) \cdot C_1 \cdot S + 1} \tag{5-16}$$

By setting the parameters as

$$R_2 = R_1 = R; \quad R_3 = m \cdot R; \quad C_1 = C; \quad C_2 = n \cdot C \tag{5-17}$$

In the audio band, the noise spectrum at the output, the Q and the cut-off frequency are given by

$$\overline{V}^2(f)_{out\_noise} = 2 \cdot (4KTR_1 + 4KTR_2 + 16KTR_3) = 16KTR(1 + 2 \cdot m) \tag{5-18}$$

$$Q = \sqrt{2 \cdot m \cdot n}/(1 + 2 \cdot m) \tag{5-19}$$

$$f_{cutoff} = \frac{1}{2 \cdot \pi \cdot R \cdot C \cdot \sqrt{2 \cdot m \cdot n}} \tag{5-20}$$

respectively. Equations 5-18, 5-19 and 5-20 give the value of the capacitance

$$C = \frac{8KT}{f_{cutoff} \cdot \pi \cdot Q \cdot \overline{V}^2(f)} \qquad \textbf{(5-21)}$$

As can been seen from Equation 5-21, the capacitor value can be calculated according to the given SNR requirement, Q value and lowpass filter cutoff frequency. The opamp input referred noise power is amplified by a factor 4 to the LPF output. Since $a + b \geq 2\sqrt{ab}$ ($a,b \geq 0$, "=" holds when a=b), for the equation:

$$n = 2 \cdot Q^2 \cdot m + \frac{Q^2}{2 \cdot m} + 2 \cdot Q^2 \qquad \textbf{(5-22)}$$

The minimum $n$ can be found from

$$n \geq 2 \cdot \sqrt{2 \cdot Q^2 \cdot m \times \frac{Q^2}{2 \cdot m}} + 2 \cdot Q^2 = 4 \cdot Q^2 \qquad 2 \cdot Q^2 \cdot m = \frac{Q^2}{2 \cdot m} \Leftrightarrow m = \frac{1}{2} \quad \textbf{(5-23)}$$

Because $Q$ is equal to 0.707 in the design, the minimum value of $n$ is equal to 2. The minimum total capacitance is then:

$$C_t = 2 \cdot C_1 + C_2 = 4 \cdot C \qquad \textbf{(5-24)}$$

According the above calculation, given the LPF noise spec 5.2uV and cutoff frequency 180 kHz, the optimized value of C in the design is 60pF and the total

capacitance is 240pF. A similar calculation can be done for single-ended input situation. In such a case, the corresponding equations are changed to

$$H(s) = \frac{-R_2/R_1}{R_2 R_3 C_1 C_2 \cdot S^2 + (R_2 + R_3 + R_2 R_3/R_1) \cdot C_1 \cdot S + 1} \qquad \textbf{(5-25)}$$

$$\overline{V}^2(f)_{LPF\_out\_noise} = 4KTR_1 + 4KTR_2 + 16KTR_3$$
$$= 8KTR(1 + 2 \cdot m) \qquad \textbf{(5-26)}$$

$$C = \frac{4KT}{f_{cutoff} \cdot \pi \cdot Q \cdot \overline{V}^2(f)} \qquad \textbf{(5-27)}$$

$$C_t = (1 + n) \cdot C = 5 \cdot C \qquad \textbf{(5-28)}$$

The headphone driver design parameters are given in Table 5-1

**Table 5-1 headphone driver design parameters**

| parameter | condition | value |
|-----------|-----------|-------|
| Noise power | 20 ~ 20 kHz | 13.56 μV |
| Power dissip. | 3.3v | 1.4 mA |
| SNR | No A-weighting | 97.35 dB |
| THD | -2 dBFS | 74.48 dB |
| R1 | differential | 10 K |
| R2 | differential | 10 K |
| R3 | differential | 5 K |
| C1 | differential | 60 pF |
| C2 | differential | 120 pF |

## 5.2.2 Amplifier design

Figure 5-8 shows the schematic of the class AB amplifier used in the headphone driver. Its performance is listed in Table 5-2 and its device sizes are given in Table 5-3.
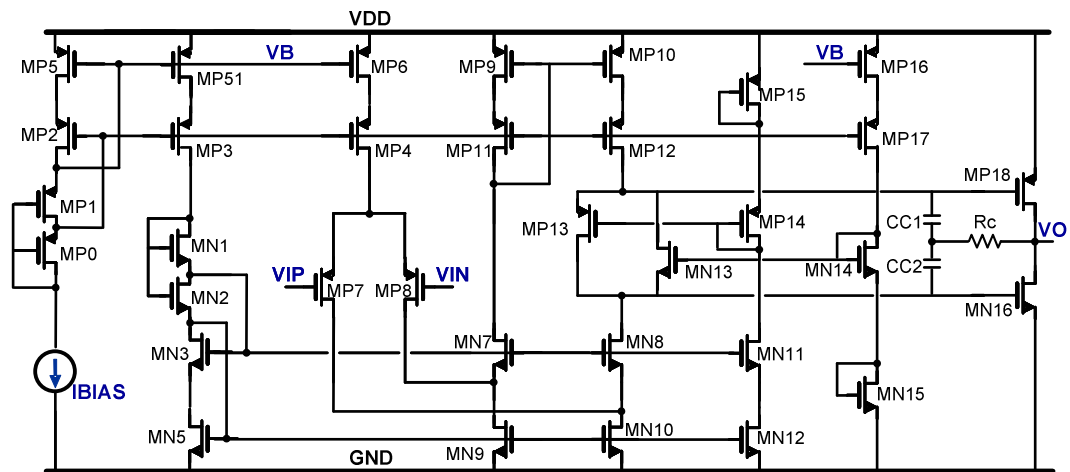


**Figure 5-8 the amplifier circuit**

**Table 5-2 Amplifier performance**

| parameter | condition | value |
|---|---|---|
| Noise power | Input reffered | 6.2029 μV |
| Power dissip. | 3.3 V | 1.2770 mA |

**Table 5-3 Amplifier device size**

| Device | Size (μm) | Device | Size (μm) |
|--------|-----------|--------|-----------|
| MP5 | 12/0.8 | MN9 | 220/8 |
| MP2 | 12/0.8 | MP10 | 220/8 |
| MP1 | 4/0.8 | MN12 | 124/4 |
| MP0 | 12/0.8 | MP13 | 21/0.8 |
| MP51 | 12/0.8 | MN13 | 7/0.8 |
| MP3 | 12/0.8 | MN8 | 43/4 |
| MN1 | 4/0.8 | MN10 | 220/8 |
| MN2 | 1.1/0.8 | MP15 | 21/0.8 |
| MN3 | 4/0.8 | MP14 | 21/0.8 |
| MN5 | 4/0.8 | MN11 | 4/0.8 |
| MP6 | 86/0.8 | MN12 | 4/0.8 |
| MP4 | 100/0.8 | MP16 | 12/0.8 |
| MP7 | 1000/2 | MP17 | 12/0.8 |
| MP8 | 1000/2 | MN14 | 7/0.8 |
| MP9 | 220/8 | MN15 | 7/0.8 |
| MP11 | 120/4 | MP18 | 950/0.8 |
| MN7 | 40/4 | MN16 | 400/0.8 |

## 5.2.3 Chip layout

The die photo of the designed headphone driver is show in Figure 5-9. It was fabricated in Samsung's 3.3V, 0.35-µm CMOS process. The devices are covered by an extra layer and only metal 3 can be seen here. The chip is packaged in a 48-pin LQFP.
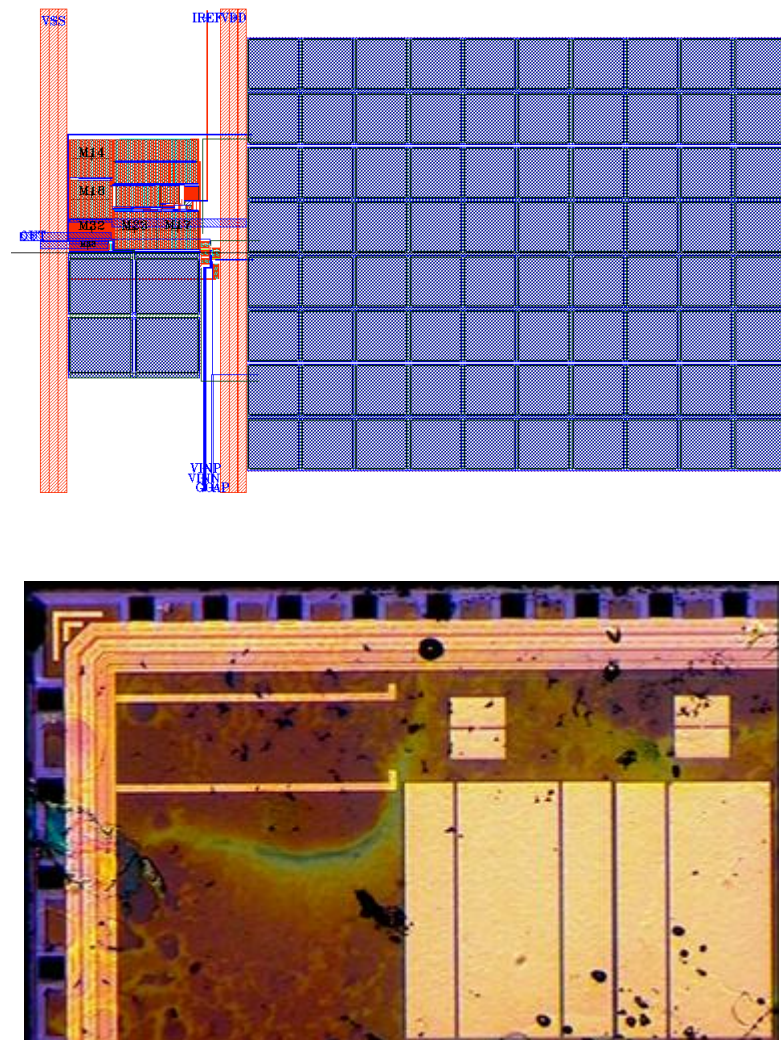
**Figure 5-9 Chip layout and die photo of the headphone driver**

## 5.2.4 Measured results

The chip was measured using the Audio Precision System Two 2322 with software APWIN 2.24. The test input signal was 1 kHz and the load was 220 pF ‖ 32Ω. The measurement bandwidth was 20 Hz to 20 kHz.

Figure 5-10 shows the measured output spectrum for a -60dBFS input which gives the dynamic range around 102 dB. Figure 5-11 shows the measured output spectrum for a -2dBFS input which gives the THD around 72 dB.
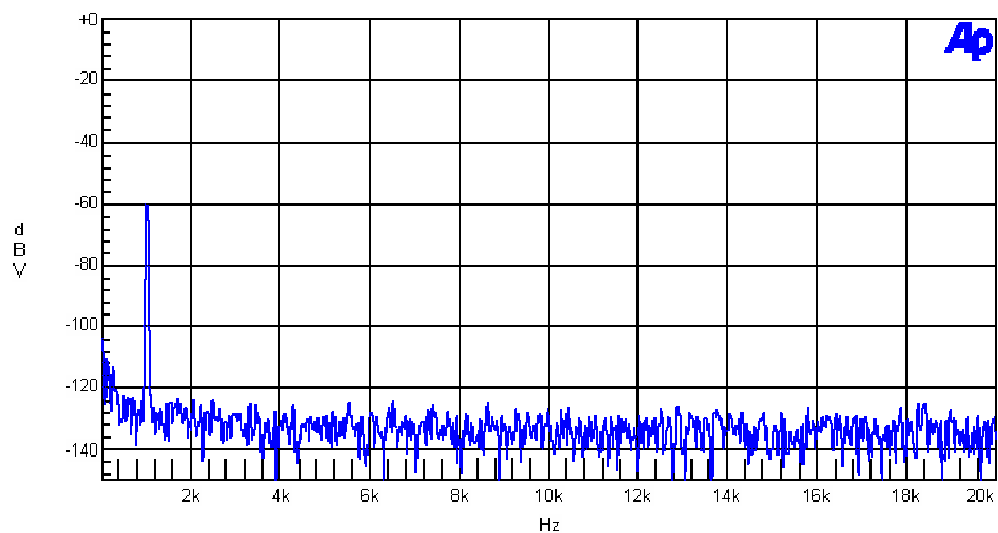


**Figure 5-10 Output spectrum with -60dBFS input**
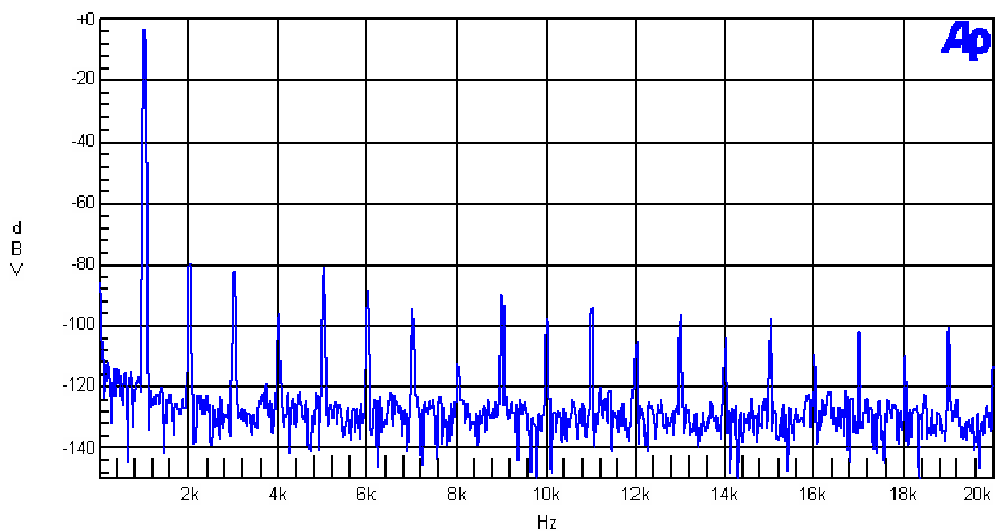


**Figure 5-11 Output spectrum with -2dBFS input**

## 5.3    Conclusion

In this chapter, the low-distortion headphone driver design techniques were described. The distortions at the input stage, output stage and in a feedback loop were examined, and a headphone driver configured as a lowpass filter was designed and fabricated in 0.35µm CMOS process applying these techniques. The measured results show the effectiveness of these techniques

## Chapter 6   An experimental delta sigma audio DAC

Digital-to-analog converters (DACs) with wide dynamic range and high linearity are required for high-end audio applications. Several audio DACs have been reported recently using a switched-capacitor (SC) hybrid postfilter [1] [2] [6] [7] whose output then feeds a separate headphone driver. In this work, an audio DAC was built by using an SC array to transfer the sampled charges directly into the integrated headphone driver. The headphone driver was designed using the technology discussed in chapter 5. Due to poorly controlled values of the RC time constants on a chip, the gain of the DAC is likely to be inaccurate. To obtain accurate gain, a correction circuit was implemented, which forces the DAC reference voltage to track the variation of the DAC RC time constant. This keeps the DAC gain accurately controlled even under widely varying mismatch conditions. In the design, the SDWA algorithm discussed in chapter 4 was used to overcome the tone generation in the audio band. Figure 6-1 shows the overall block diagram of the DAC.
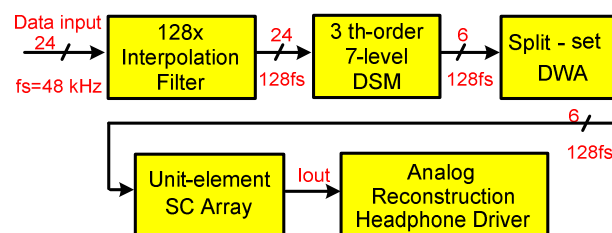


**Figure 6-1 The delta sigma audio DAC**

The specifications of the experimental DAC integrated with the headphone driver are decided according to the commercial requirement [30] and are listed in Table 6-1

**Table 6-1 Design specifications**

| parameter | value |
|---|---|
| SNR (A-weighted) | 90dB ~ 97 dB |
| THD (-5dBFS) | -60 dB ~ -65 dB |
| THD (-2dBFS) | -45 dB ~ -40 dB |

## 6.1 DAC structure

Figure 6-2 shows the second-order Sallen-Key filter which is commonly used as the reconstruction filter in audio delta sigma DACs. The DAC output is applied to this filter to remove out-of-band noise. The transfer function of this filter is given by

$$H(S) = \frac{-R_2/R_1}{2 \cdot R_2 R_3 C_1 C_2 \cdot S^2 + (R_2 + R_3 + R_2 R_3/R_1) \cdot C_1 \cdot S + 1} \tag{6-1}$$

In this design, the input resistor $R_1$ is replaced by a switched-capacitor structure as shown in Figure 6-3. By digitally controlling the SC branch, it can be used to perform the DAC function, saving hardware. Delta sigma modulator outputs are the control signals to these switches.
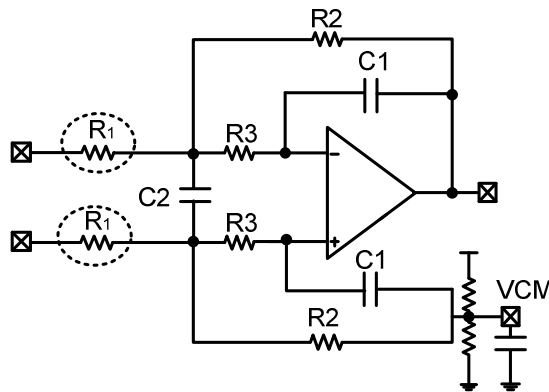
**Figure 6-2 The 2$^{nd}$ order Sallen-Key filter**



**Figure 6-3 Modification to the filter**

## 6.2 Correction circuitry

A problem with the new configuration shown in Figure 6-3 is that the dc gain of the DAC is poorly controlled. As can been seen from Equation 6-1, the dc gain of the traditional Sallen-Key filter is given by the ratio of $R_2$ and $R_1$, which is well controlled on the chip. However, in the modified structure, the amplitude A of the filter output signal at dc is given by

$$A = 2 \cdot n \cdot V_{rsc} \cdot R_2 \cdot C_{DAC} / T_1 \qquad \textbf{(6-2)}$$

Here, $V_{rsc}$ is the reference voltage sampled by the SC array, n is the number of the unit elements in the SC array, and $T_1$ is the clock period in the DAC. Equation 6-2 shows that amplitude A depends on the time constant $R_2 \cdot C_{DAC,}$ which is poorly controlled on the chip. To control the amplitude A accurately, a gain correction stage was introduced, as shown in Figure 6-4. In steady state, the dc currents entering nodes Ⓐ and Ⓑ through the resistive and SC branches equal zero.
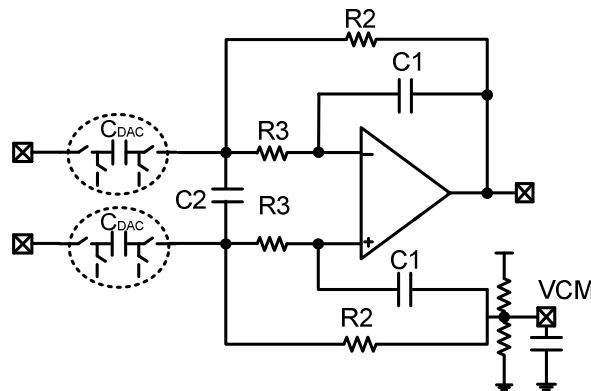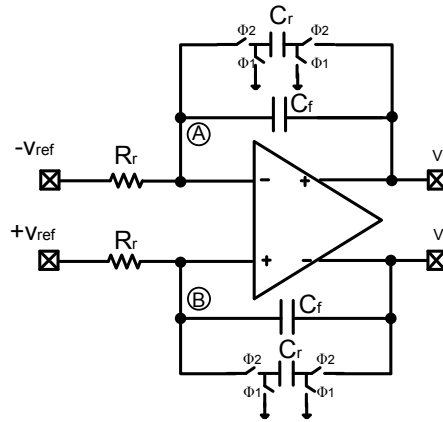


**Figure 6-4 Correction circuit**

The output voltages are then given by

$$V^{+} = +V_{ref} \cdot T_2 / (R_r \cdot C_r) \qquad \textbf{(6-3)}$$

$$V^{-} = -V_{ref} \cdot T_2 / (R_r \cdot C_r) \qquad \textbf{(6-4)}$$

Here, $T_2$ is the clock period in the correction circuit. This stage generates the reference voltage for the DAC output stage. Combining Equations 6-2, 6-3 and 6-4 gives

$$A = 2 \cdot n \cdot V_{ref} \cdot (T_2/T_1) \cdot (R_2/R_r) \cdot (C_{DAC}/C_r) \qquad \textbf{(6-5)}$$

Equation 6-5 shows that amplitude A now depends on ratios of R and C values, which can be accurately controlled with careful layout. In general, $T_1$ and $T_2$ can be different, but in our design they were both set equal to the input data rate.

## 6.3    Implementation of the DAC and headphone driver

As mentioned earlier, the filter opamp acts also as the headphone driver in the DAC. Figure 6-5 shows the proposed DAC architecture which includes the correction circuit, switched-capacitor arrays providing a seven-level analog output, and the headphone driver which also acts as the analog reconstruction filter. Capacitors Cb are used to filter the output voltage of the correction circuit. The switches of the SC circuit are controlled by the output bits of the delta-sigma modulator, and scrambled using the SDWA algorithm. The SC array samples one of the correction circuit outputs, V+ or V-, depending on the SDWA data. For a single-ended SC array, the load of the correction circuit would thus depend on the SDWA data, and would be unbalanced. Hence, a differential SC array is used in the design to improve the noise immunity, and also to avoid an unbalanced load on the correction circuit.

The sampled charges generated by the DAC are fed directly into the headphone driver, which is embedded in the second-order Sallen-Key reconstruction low-pass filter.
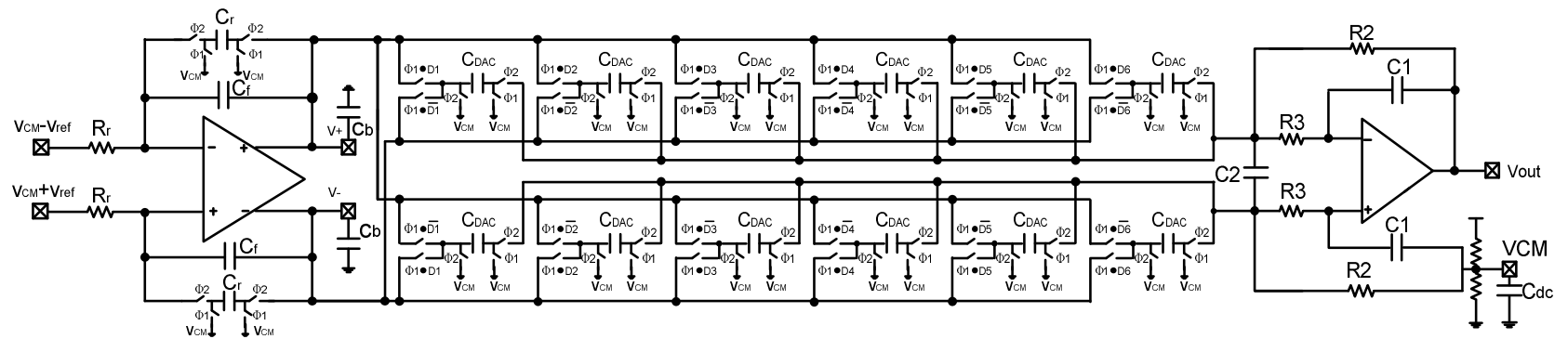
**Figure 6-5 proposed DAC**

## 6.4    Amplifier design

The differential amplifier designed to provide DAC reference voltages is similar with the driver amplifier, except without a Class AB output stage. The schematic of this amplifier is shown in Figure 6-6.
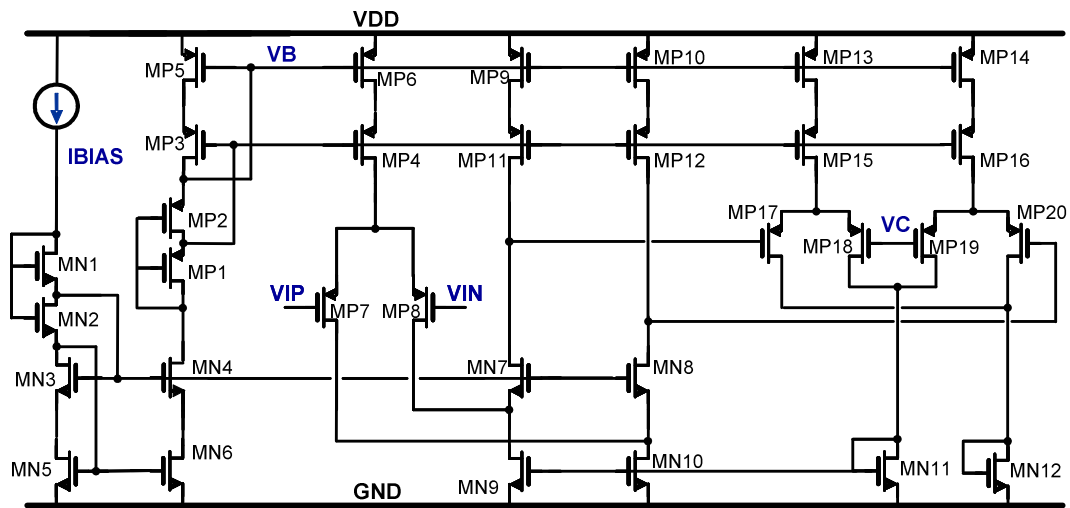


**Figure 6-6 Schematic of the reference amplifier**

Figure 6-7 shows the schematic of the designed Class AB amplifier, which is similar with the amplifier described in chapter 5. Crossover distortion is controlled by making MP18 and MN16 not turn off completely in the quiescent condition. Since the $V_{gs}$ of the transistor MP15 is equal to the $V_{gs}$ of MP18, and the $V_{gs}$ of transistor MN15 is equal to the $V_{gs}$ of MN16 in quiescent condition, the quiescent currents flowing through transistors MP18 and MN16 are set by MP15 and MN15, respectively.
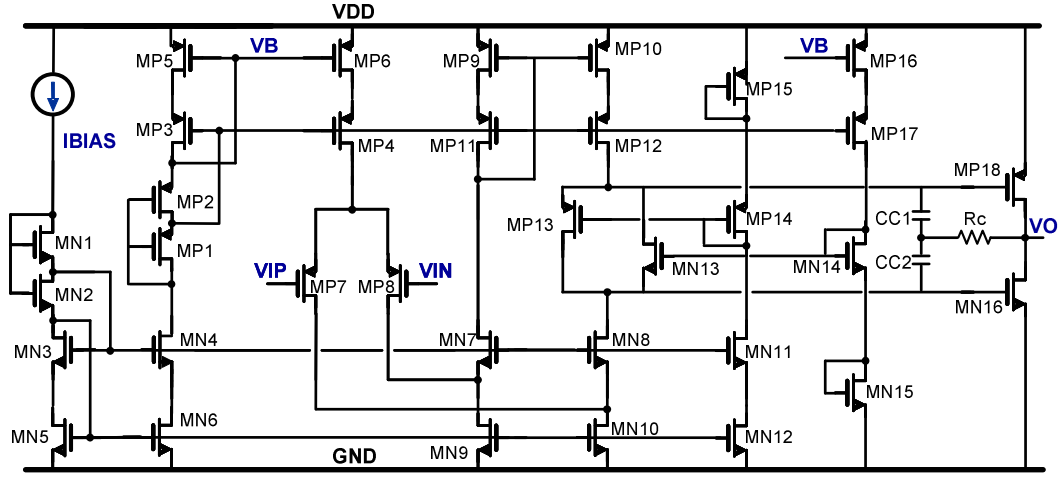
**Figure 6-7 Schematic of the amplifier**

The low-frequency voltage gain of the amplifier with the load $R_L$ can be calculated as

$$Av = g_{MP7} \left( ro_{MN10} g_{MN8} ro_{MN8} \; // \; ro_{MP10} g_{MP12} ro_{MP12} \right) g_{MN16} \left( ro_{MN16} \; // \; ro_{MP18} \; // \; R_L \right) \quad \textbf{(6-6)}$$

The load $R_L$ is a small resistor (32 Ohms). Hence the low-frequency voltage gain can be simplified to

$$Av = g_{MP7} \left( ro_{MN10} g_{MN8} ro_{MN8} \; // \; ro_{MP10} g_{MP12} ro_{MP12} \right) g_{MN16} R_L \quad \textbf{(6-7)}$$

The input referred noise power can be calculated as the sum of all the output-referred noises divided by the low-frequency gain

$$\frac{P}{\Delta f} = 2 \left\{ \overline{V_{MP7}^2} + \left( \frac{g_{MP10}}{g_{MP7}} \right)^2 \overline{V_{MP10}^2} + \left( \frac{G_{MP12}}{g_{MP7}} \right)^2 \overline{V_{MP12}^2} + \left( \frac{g_{MN10}}{g_{MP7}} \right)^2 \overline{V_{MN10}^2} + \left( \frac{G_{MN8}}{g_{MP7}} \right)^2 \overline{V_{MN8}^2} \right\} + \frac{\overline{V_{MP18}^2}}{g_{MP7}^2 ro_1^2} + \frac{\overline{V_{MN16}^2}}{g_{MP7}^2 ro_1^2} \quad \textbf{(6-8)}$$

where $r_{o1}$ is the output impedance of the first stage, and is given by

$$ro_1 = ro_{MN10} \, g_{MN8} \, ro_{MN8} \,/\!/\, ro_{MP10} \, g_{MP12} \, ro_{MP12} \tag{6-9}$$

$$G_{MP12} = \frac{g_{MP12}}{1 + g_{MP12} \, ro_{MP9}} \tag{6-10}$$

$$G_{MN8} = \frac{g_{MN8}}{1 + g_{MN8} \, ro_{MN10}} \tag{6-11}$$

The noise due to the transistors MP13 and MN13 is neglected, because the noise is degraded by the two cascade transistors MP10 MP12 and MN8 MN10. The noise caused by transistors MP12 and MN8 can also be neglected because the noise is degraded by transistors MP10 and MN10. The noise caused by the two output transistors MP18 and MN16 can be neglected, since they are divided by the gain of the first stage. The equation 6-8 is then reduced to

$$P = 2 \left\{ \overline{V_{MP7}^2} + \left( \frac{g_{MP10}}{g_{MP7}} \right)^2 \overline{V_{MP10}^2} + \left( \frac{g_{MN10}}{g_{MP7}} \right)^2 \overline{V_{MN10}^2} \right\} \cdot \Delta f \tag{6-12}$$

The noise sources are given by

$$\overline{V^2} = 4KT \frac{2}{3} \frac{1}{gm} + \frac{KF}{C_{OX} WL f^{\,a}} \tag{6-13}$$

$$P_{thermol} = 2 \cdot 4kT \frac{2}{3} \frac{1}{g_{MP7}} \left( 1 + \frac{g_{MP10} + g_{MN10}}{g_{MP7}} \right) \cdot \Delta f \tag{6-14}$$

$$P_{flick} = 2 \cdot \frac{KF}{C_{OX}} \left( \frac{1}{(WL)_{MP7}} + \frac{g^2_{MP10}}{g^2_{MP7}} \frac{1}{(WL)_{MP10}} + \frac{g^2_{MN10}}{g^2_{MP7}} \frac{1}{(WL)_{MN10}} \right) \frac{1}{f^a} \cdot \Delta f \quad \textbf{(6-15)}$$

When the amplifier is put into the feedback loop as shown in chapter 5, the output noise can be calculated according to Equation 6-16.

$$V_{OUT\_OP}(f)^2 = \left| \frac{A(s)}{1 + A(s)\beta(s)} \right|^2 V_{OPAMP}(f)^2 \quad \textbf{(6-16)}$$

$$\beta(s) = \frac{R_1 R_2 R_3 C_1 C_2 s^2 + (R_1 R_2 + R_2 R_3 + R_1 R_3) C_1 s + R_1}{R_1 R_2 R_3 C_1 C_2 s^2 + (R_1 R_2 C_1 + R_2 R_3 C_1 + R_1 R_3 C_1 + R_1 R_2 C_2) s + R_1 + R_2} \quad \textbf{(6-17)}$$

A direct calculation using Equation 6-16 is tedious, and the alternative calculation is to approximate the feedback system as a one-pole system by

$$H(s) = \frac{\dfrac{1}{\beta}}{1 + \dfrac{C_0 s}{\beta g_{m1}}} \quad \textbf{(6-18)}$$

where $g_{m1}$ is the transconductance of the opamp input transistor, $\beta$ is the feedback factor, $C_0$ is the compensation capacitor. With this assumption, the output thermal noise power can be calculated as

$$P_{thermol} = \int_0^\infty P_{OP}(f) \left| \frac{\dfrac{1}{\beta}}{1 + \dfrac{C_0 s}{\beta g_{m1}}} \right|^2 df = P_{OP}(f) \frac{g_{MP7}}{4 C_0 \beta} = 2 \cdot 4kT \frac{2}{3} \left( 1 + \frac{g_{MP10} + g_{MN10}}{g_{MP7}} \right) \cdot \frac{1}{4 C_0 \beta} \quad \textbf{(6-19)}$$

As can been seen from Equation 6-19, the noise can be reduced by increasing $C_0$ or $\beta$, by decreasing the ratio of $(g_{mp10}+g_{mn10})/g_{mp7}$.

The flicker noise can be calculated from

$$P_{tflick} = \int_0^\infty P_{OP}(f) \left| \frac{\frac{1}{\beta}}{1 + \frac{C_0 s}{\beta g_{m1}}} \right|^2 df = \int_0^\infty P_{OP}(f) \frac{G_0^2}{1 + 2\pi\tau f} df = \int_0^\infty \frac{K}{f} \frac{G_0^2}{1 + 2\pi\tau f} df = a\{\ln(f) - \ln(bf + 1)\}\Big|_0^\infty$$

$$= a \ln\left( \frac{1}{b + \frac{1}{f}} \right)\Bigg|_0^\infty = a \ln\left( 1 + \frac{1}{bf_{\to 0}} \right) \qquad \textbf{(6-20)}$$

where $K = 2 \cdot \dfrac{KF}{C_{OX}} \left( \dfrac{1}{(WL)_{MP7}} + \dfrac{g_{MP10}^2}{g_{MP7}^2} \dfrac{1}{(WL)_{MP10}} + \dfrac{g_{MN10}^2}{g_{MP7}^2} \dfrac{1}{(WL)_{MN10}} \right)$,

$a = KG_0^2$, $b = 2\pi\tau$, $\tau = \dfrac{C_0}{\beta g_{m1}}$ and $G_0 = \dfrac{1}{\beta}$

To reduce flicker noise, Equation 6-20 shows that $a$ should be decreased and $b$ should be increased.

Noise calculation in the switched-capacitor circuit can be done by replacing the switched-capacitor branch (the dotted part in Figure 6-8) with a resistor with value R=T/C, where T is the clock period. The noise at the output can be calculated according to the previous analysis in chapter 5.
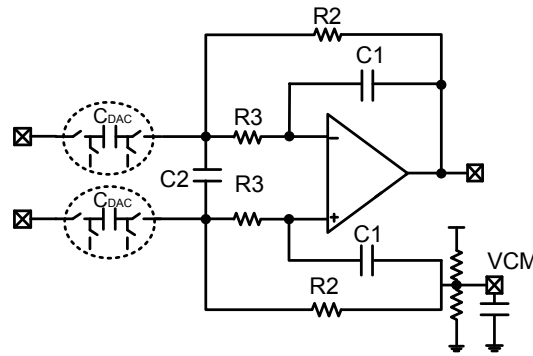
**Figure 6-8 Noise calculation**

Given R2=20k R3=10k, C1=60pF C2=240pF Cdac=0.6pF T=12ns, the two simulations using PSS Pnoise as a comparison. Using the equivalent resistors, the integrated noise from 20 Hz to 20 kHz is $3.71409e\text{-}10V^2$ which is 19.272uV. While using the switched-capacitor branch, the integrated noise is $4.67328e\text{-}10V^2$ which is 21.617uV. As can be seen from Figure 6-9, the difference between these two can be ignored.

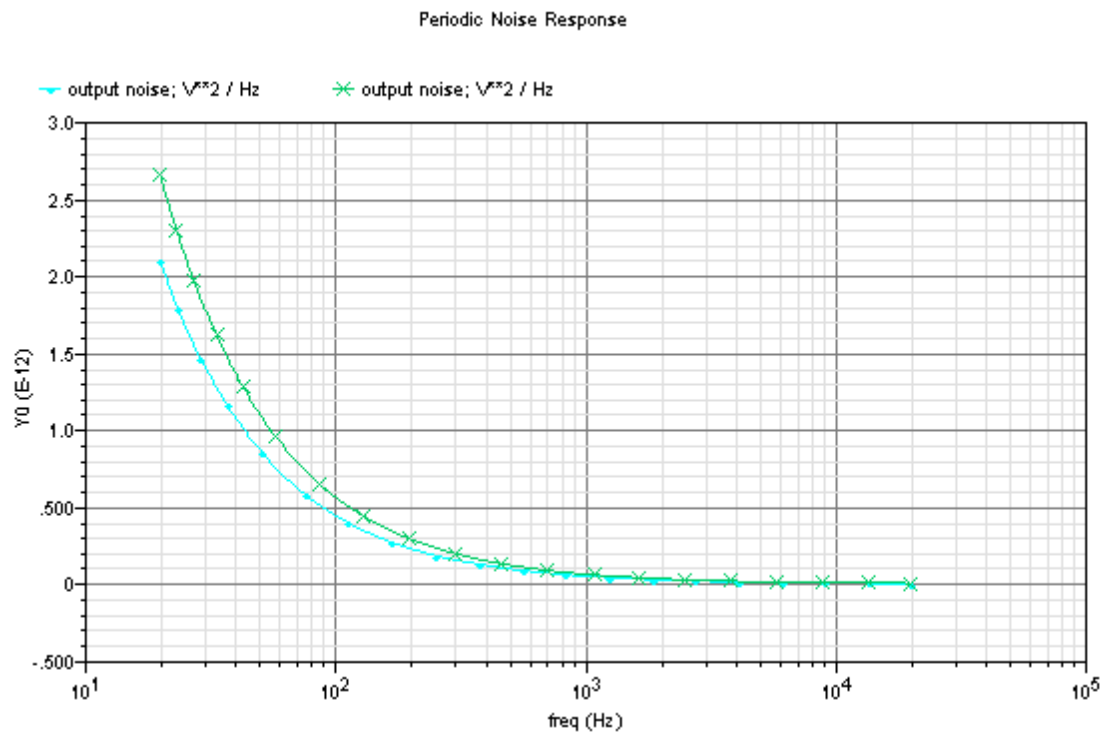**Figure 6-9 Noise spectrum in two structures**

## 6.5 Chip layout

The die photo of the designed DAC is show in Figure 6-10. It was fabricated in Samsung's 3.3V, 0.35-µm CMOS process. The core area is about 1.12- mm$^2$. The devices are covered by an extra layer and only metal 3 can be seen here. The chip is packaged in a 48-pin LQFP.
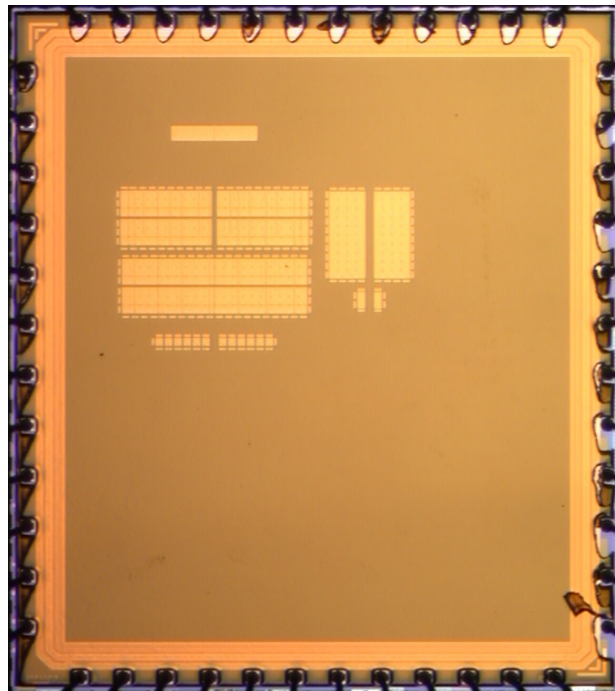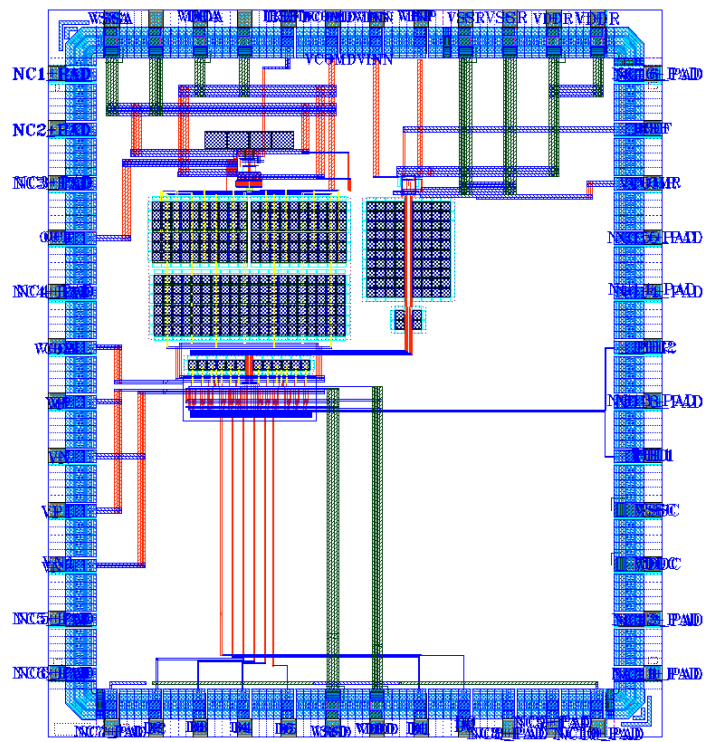
**Figure 6-10 Chip layout and die photo of the audio DAC**

## 6.6    Measurement results

The SC audio DAC was fabricate and tested. All measurements were taken by the Audio Precision System Two 2322 with software APWIN 2.24 in the audio band (20 Hz to 20 kHz), using the SDWA algorithm. To drive the DAC, the third-order seven-level delta-sigma modulator designed in chapter 3 was used. The signal bandwidth was 20 kHz and the sampling frequency was 48 kHz. The oversampling ratio was 64. The SDWA algorithm was used to process the delta sigma output data, and to generate the input data for the switched-capacitor array. The test board for the audio DAC is shown in Figure 6-11 which is a four-layer printed circuit board (PCB).
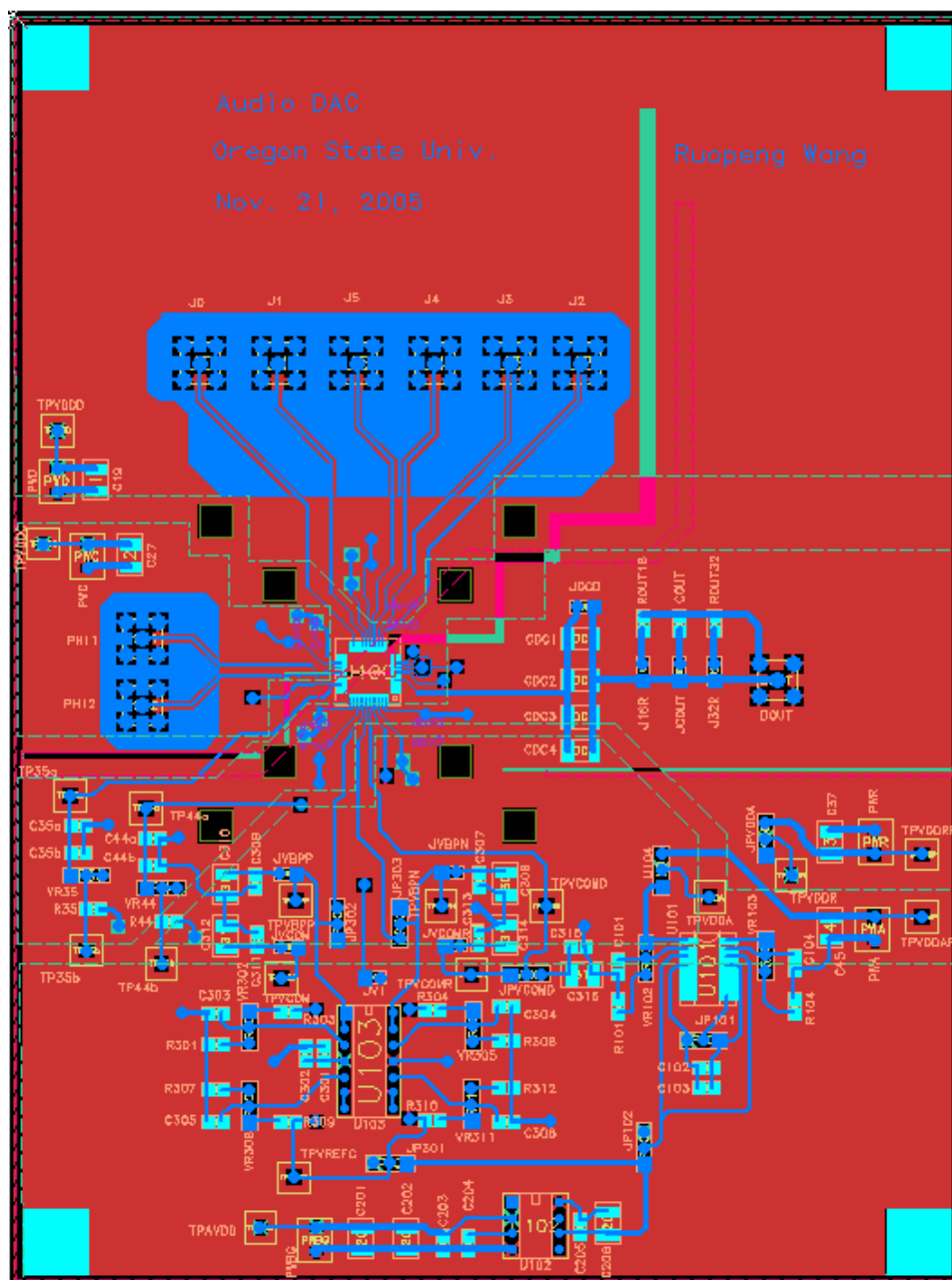
**Figure 6-11 PCB design for the DAC test**
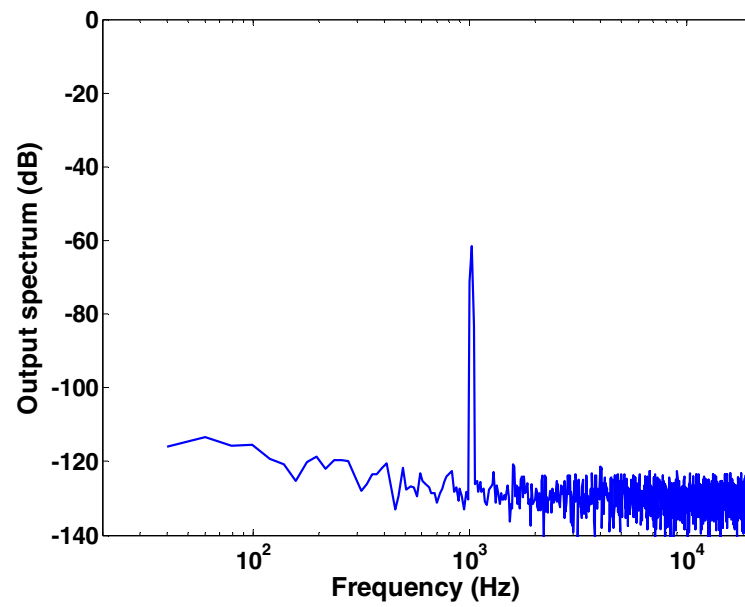
**Figure 6-12 Output spectrum given -60 dBFS input**
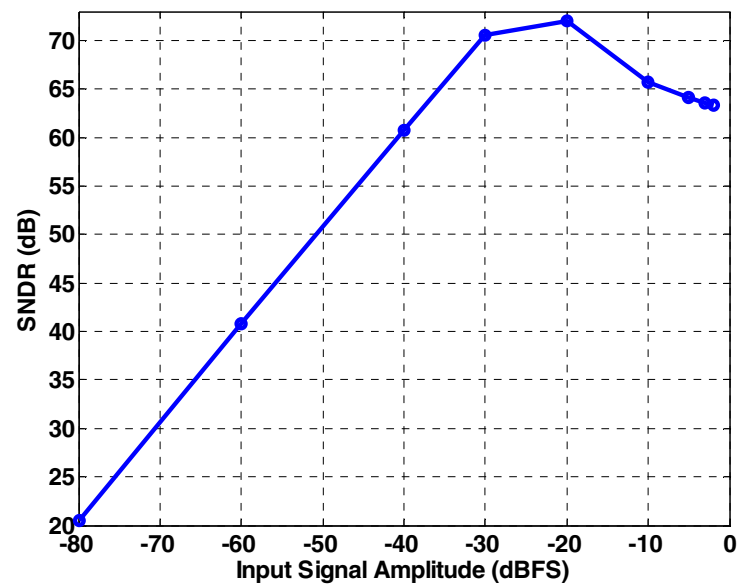


**Figure 6-13 SNDR vs. input amplitude**
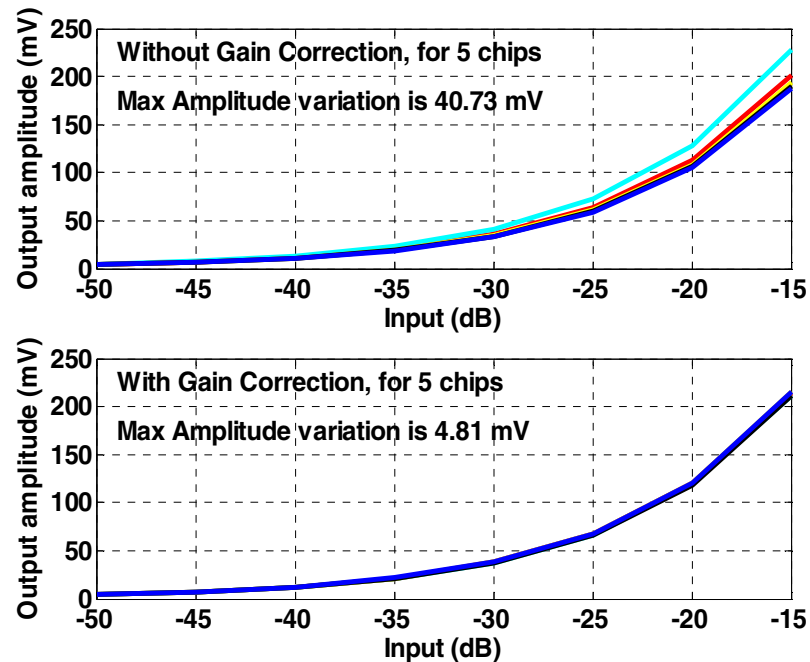
**Figure 6-14 DAC gain correction**

Figure 6-12 shows the output spectrum for a -60 dBFS input test signal. The noise floor was around -130 dBFS and the inband tones were below -120 dBFS. Figure 6-13 shows the A-weighted SNDR versus input level characteristics from –80 dBFS to –2 dBFS with a 1.008 kHz input signal. The load was a 32 Ohms resistor in parallel with a 220 pF capacitor. The dynamic range, calculated as the SNDR at –60 dBFS, is 100.83 dB. The peak SNDR is 72 dB, and is limited by the distortion of the single-ended headphone driver (the peak SNDR is around 88 dB with the 500 Ohms load). Figure 6-14 shows the gain correction performance, measured on five devices. The top curves show the spread of output amplitudes without correction; the bottom curves illustrate the uniform performance with correction.

Above test results show that the designed DAC with driver meets the specifications for the commercial high-end audio systems. A summary of the measured performance is given in Table 6-2.

**Table 6-2 Measurement summary**

| Parameter | Value |
|---|---|
| Power Supply | 3.3 V |
| Power dissipation | 9.57 mW |
| Dynamic range (SDWA, A-weighted) | 100.83 dB |
| Peak SNDR | 72 dB |
| Load | 32 Ω ‖ 220 pF |
| Signal bandwidth | 20 kHz |
| Die area | 1.12 mm$^2$ |
| Process | 0.35 µm CMOS |

## 6.7    THD performance improvement

As shown in Figure 6-12, the SNDR performance for large input signal is limited by the integrated headphone driver. If higher performance is desired, using a larger loop gain and increasing output devices are effective ways in addition to reduce the amplifier distortion itself by using the techniques discussed in chapter 5. For example, without changing above design a lot, Figure 6-15 shows an improved driver amplifier design. Here one more branch is added to and output device MP18 and MN16 are doubled to provide a larger DC gain.

**Figure 6-15 An improved amplifier**

## 6.8 Conclusion

A delta-sigma audio DAC, using a novel gain-correction technique, was described. It uses a novel algorithm for dynamic element matching. The designed DAC also successfully integrates the headphone drive. Test results verify that it meets the requirements for a typical high-end audio system.

## Chapter 7   Conclusions

## 7.1    Summary

Oversampling delta-sigma techniques used in the audio DACs were analyzed in this dissertation. The associated topics have also been studied in detail. These include:

The fundamentals of delta-sigma DACs and special aspects when they are used in the audio applications

A digital interpolator and noise shaper have been designed and analyzed.

A novel DEM algorithm based on DWA, named Split-set DWA, was proposed to deal with the nonlinearity caused by multi-bit modulation. Low-cost and high-efficient implementation of the proposed algorithm was realized.

Different headphone driver structures have been compared and low distortion design techniques were studied. A prototype class AB headphone driver integrated with the reconstruction filter was designed and tested.

An audio DAC with novel gain correction circuitry was built, and measurements showed it met a typical high-end audio requirement.

## 7.2    Future work

Currently, the SDWA circuit is realized on the gate level. Circuit level simulations show it works very well. Implementation of this circuit on a chip is of great interest.

Appling the techniques studied for very low-distortion headphone driver design in chapter 5 to a prototype chip will be interesting.

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