AN ABSTRACT OF THE DISSERTATION OF

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Digitally controlled switching DC-DC converters have recently emerged as an
attractive alternative to conventional switching converters based on analog control
techniques. This research focuses on eliminating the issues associated with the
state of the art switching converters by proposing three novel control techniques:
(1) a digitally controlled Buck-Boost converter uses a fully synthesized constant
ON/OFF time-based fractional-N controller to regulate the output over a 3.3V-
to-5.5V input voltage range and provides seamless transition from buck to buck-
boost modes (2) a hysteretic buck converter that employs a highly digital hybrid
voltage/current mode control to regulate output voltage and switching frequency
independently (3) a 10MHz continuous time PID controller using time based sig-
nal processing which alleviates the speed limitations associated with conventional
analog and digital.

All the three techniques employ digitally assisted control techniques and
require no external compensation thus making the controllers fully integrated and
highly cost effective.

Digitally Assisted Control Techniques for High Performance Switching DC-DC
Converters

by

Qadeer Ahmad Khan

A DISSERTATION

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Dean of the Graduate School

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Qadeer Ahmad Khan, Author

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With immense faith, first of all I want to thank Almighty GOD, the creator of all worlds, the creator of intellectual and beautiful human being, the provider of sustenance to each and every living creature in this universe, the most merciful, the listener to every grief and the provider of relief, Who has given me this opportunity to accomplish my dream of Ph.D.

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DIGITALLY ASSISTED CONTROL TECHNIQUES FOR HIGH PERFORMANCE SWITCHING DC-DC CONVERTERS

CHAPTER 1. INTRODUCTION

1.1   Motivation and Research Contribution

This research is motivated by the growing demand of high performance switching DC-DC converters in the consumer market. As shown in Fig. 1.1, there is hardly any application untouched by a dc-dc converter. According to a study [1] shown in Fig. 1.2, almost one third of $30bn power market is contributed by the dc-dc converters (voltage regulators) and growing at a rapid pace with the rising demand of solar and LED.

As technology is advancing with an effort of integrating various features in portable and hand-held devices such as smart-phones, tablet PCs and media players, the power density requirement is growing exponentially due to limited board size available on these gadgets. The high efficiency and capability of operating across wide load and input/output voltage make switching dc-dc converters an ideal choice over linear regulators (which require bulky heat sinks due to poor efficiency) to cater this power density need. These switching converters can be implemented with a fixed frequency based pulse width modulation (PWM) or a
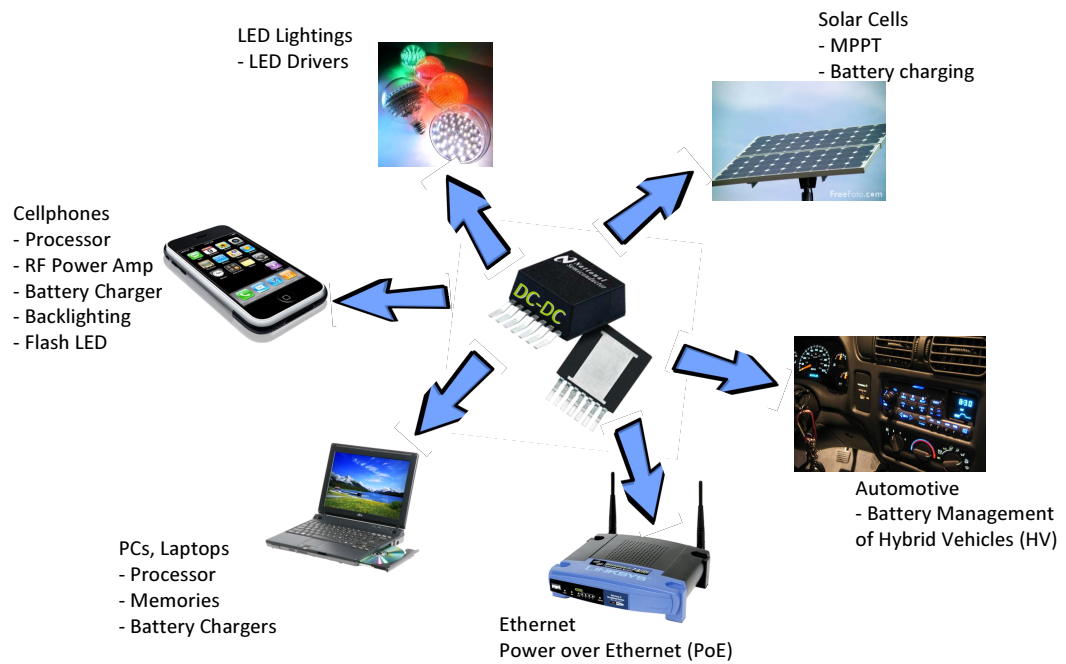
Figure 1.1: Various applications requiring dc-dc converters
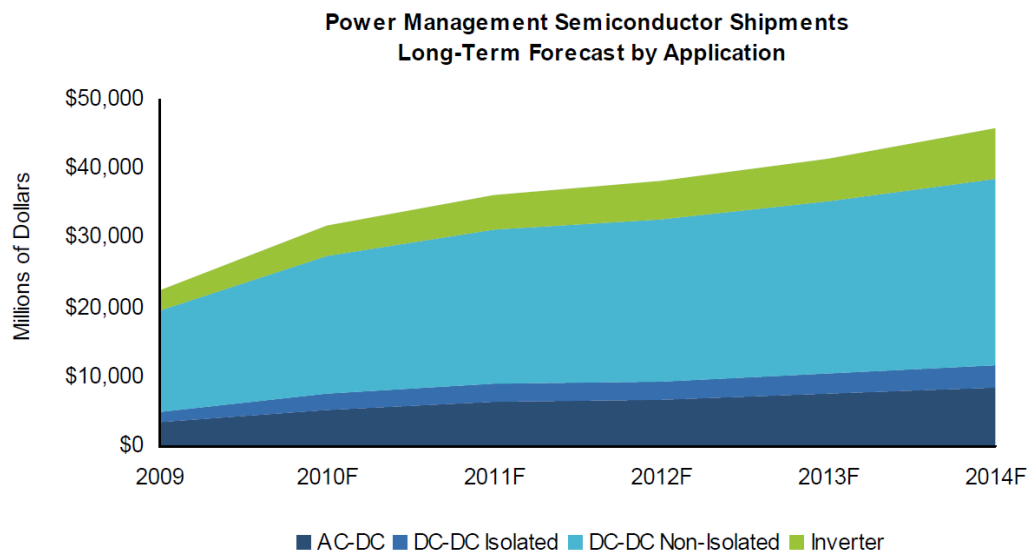
Figure 1.2: DC-DC Converter market. Source: isupply [1]

variable frequency hysteretic controller. In applications where wide variation in switching frequency is tolerable, hysteretic controller is preferred because of its simpler design and faster dynamic response. However, in noise sensitive applications such as mobile phones and other wireless applications, fixed frequency PWM controllers are mostly used but they are expensive due to external compensation. Since state of the art semiconductor device technologies provide ease of integration and power switches can easily be integrated with the controller on a single chip, the size of a power module is mainly limited by its on-board passive components such as LC filter (inductor and capacitor) and external compensation. In an effort to integrate a PWM controller on a single chip, digital PWM controllers have gained popularity in the recent few years [16] and provided another research platform in the area of power converters. Even though a significant amount of research has been done in this area, the complexity and challenges associated with a digital PWM controller still provide an opportunity for current and future research. For instance, the requirement of high resolution Analog-to-Digital converter and high resolution PWM [20] either limit the switching frequency or require high quiescent current. This research work seeks to address the various issues of state of the art control techniques by providing ingenious solutions.

The first solution is aimed for a buck-boost converter which uses a fully synthesized digital fractional-N controller to solve the mode transition issue and eliminates the need of an external compensation capacitor. The technique is quite effective for applications powered by Lithium-ion batteries such as flash LED drivers which are quite inefficient if not driven by a buck-boost converter [10].

Second design presented in this research provides a cost effective and fully integrated alternative to a fixed frequency PWM controller. The technique is based on a hysteretic converter which resolves the various issues such as wide frequency

variation, poor load regulation and large output ripple associated with state of the hysteretic converters.

Although the above two fully integrated controllers save external compensation, the on board LC filter is inevitable due to lack of technology capable of fabricating high power on-chip inductors and high density capacitors. Therefore pushing the converter switching frequency high is the only viable solution to achieve smaller size of passive components. As a matter of fact, the converter switching frequency is rapidly advancing and has surpassed several MHz in the last couple of years. With the present availability of 6MHz-8MHz converter in the market [2]-[3], it will not be surprising to see above 10MHz converter in the near future. Following the latest market trend, third and final design addresses the limitations with high frequency operation of existing control topologies by proposing a 10MHz continuous time PWM controller based on ultra low power and highly integrated time based proportional-integral-derivative (PID) compensator.

1.2   Thesis Organization

This thesis is organized as follows: Chapter 2 provides an overview of switching dc-dc converter.

Chapter 3 starts with an introduction of buck-boost converter and challenges associated with the existing designs. A buck-boost converter based on constant ON/OFF time fractional-N digital control is presented in this chapter and design details are discussed. The chapter is concluded with measurement results of the prototype build to demonstrate the proposed technique.

Chapter 4 gives insight of a hysteretic dc-dc converter and analyzes its behavior under different conditions. The various conditions for stable operation of a

hysteretic converter are studied. The benefits and drawbacks of both voltage and current mode hysteretic converters are discussed. A hybrid controller comprising of both voltage and current mode is proposed with a scheme for regulating the switching frequency to get the fixed frequency operation.

Chapter 5 introduces the concept of time based PWM controller using time domain signal processing. A proportional-integral-derivative (PID) compensator is realized in time domain using voltage controlled oscillators (VCO) and voltage controlled delay lines (VCDL). Detailed design procedure of a 10MHz buck converter is presented and various design parameters are calculated. Issues with the proposed technique are also discussed with the possible solutions.

Even though the techniques presented in Chapter 4 and 5 were implemented with a buck converter, their application is not limited and can be employed with any type of converter (boost or buck-boost). The designs were demonstrated only for continuous conduction mode (CCM). The standard PFM (pulse frequency modulation) mode can also be implemented with these controllers under discontinuous conduction mode (DCM) to achieve higher efficiency at light load.

CHAPTER 2. AN OVERVIEW OF SWITCHING DC-DC CONVERTER

2.1 Linear vs. Switching Converter

It is a well known fact that switching converters (or regulators) offer superior efficiency over wide range of input and output voltages therefore always preferred over linear regulators. Since a linear regulator, as shown in Fig. 2.1, regulates the output voltage by dropping extra voltage across the pass transistor (M_P), it suffers from poor efficiency.
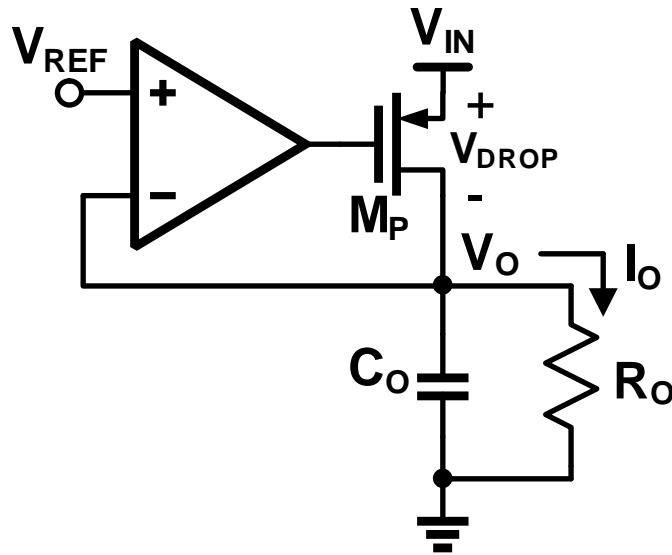
Figure 2.1: A linear regulator

When linear regulators are operated at higher current, the drop-out power is dissipated into heat and requires bulky heat sink. A switching converter on the

other hand, by virtue of its operation, does not require a heat sink and despite using external inductor it offers a compact power solution.
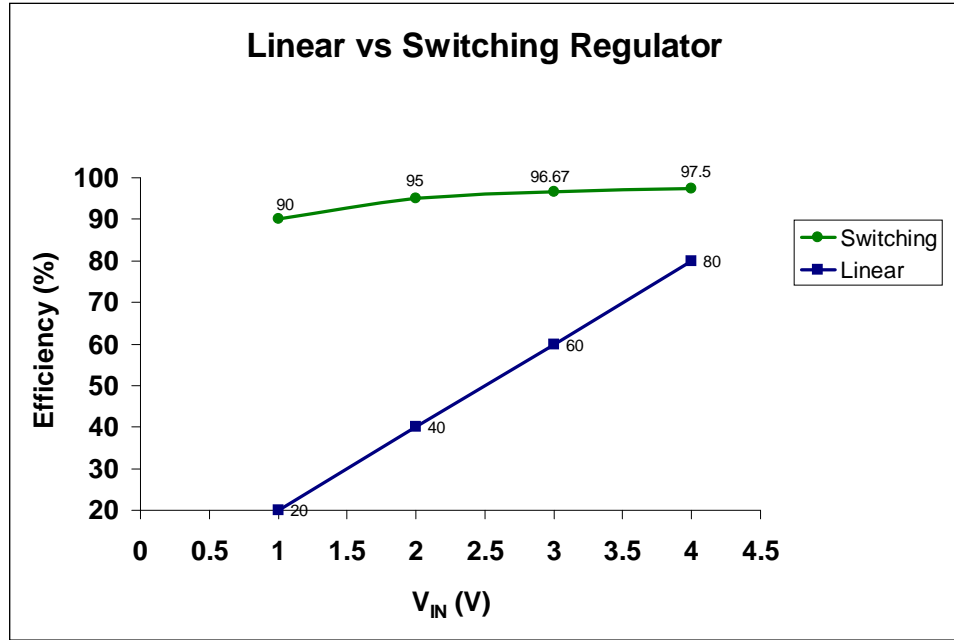
Figure 2.2: Efficiency comparison of switching and linear regulators

Fig. 2.2 shows the efficiency comparison of switching converter with a linear regulator when both are operated at 5V input while output is varied from 1V to 4V at load current of 1A. The difference is quite obvious and it could be noticed that at 1V, 80% of the total power is lost in the linear regulator while switching converter maintains an efficiency of above 90% throughout the entire range. Since the linear regulator efficiency is improved at higher output to input voltage ratio (due to less drop-out voltage), they might be preferred if regulated output voltage is close to input but application is quite limited.

2.2 Switching DC-DC Converter

A PWM based dc-dc converter works on the averaging concept of a variable width square pulse or PWM signal. This pulse when passed through a high Q low pass LC filter, all the ac harmonics are suppressed leaving only the the average dc voltage at the output . The output voltage can be regulated simply by controlling the width of the square pulse.
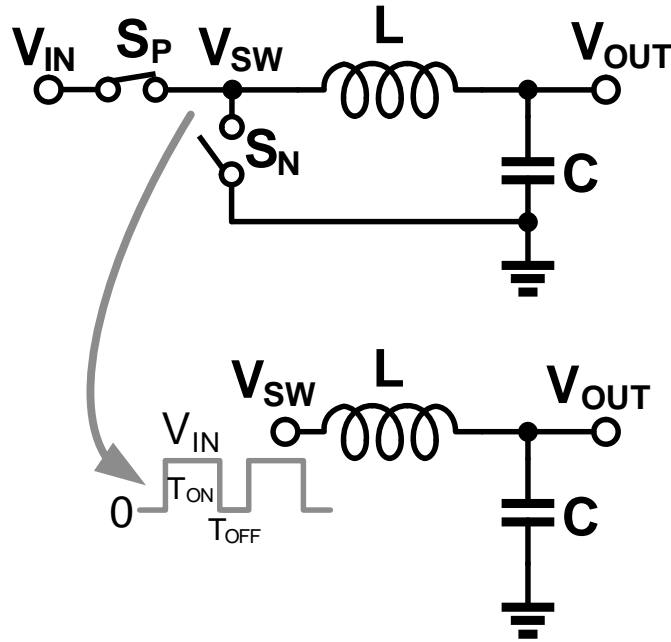
Figure 2.3: Switching action of a dc-dc converter

As shown in Fig. 2.3, the width of square wave can be controlled with the switches S_P and S_N. Assuming that the V_{SW} is at V_{IN} when switch S_P is ON, S_N is OFF and 0 when S_N is ON, S_P is OFF then the output voltage V_{OUT} can be expressed as:

$$V_{OUT} = DV_{IN} \qquad (2.1)$$

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where D is the duty cycle (a measure of pulse width) expressed as:

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \frac{T_{ON}}{T_{SW}} \tag{2.2}$$

and T_{SW} is the clock period, T_{ON} is the ON time and T_{OFF} is the OFF time of the square pulse.

From eq. 2.1, it can be understood that in order to get the constant V_{OUT} under varying V_{IN}, D must be changed accordingly. This is usually accomplished by the PWM feedback loop which controls the duty cycle to regulate the output voltage under variable operating conditions. Fig. 2.4 shows the block diagram of a dc-dc converter based on analog PWM control.
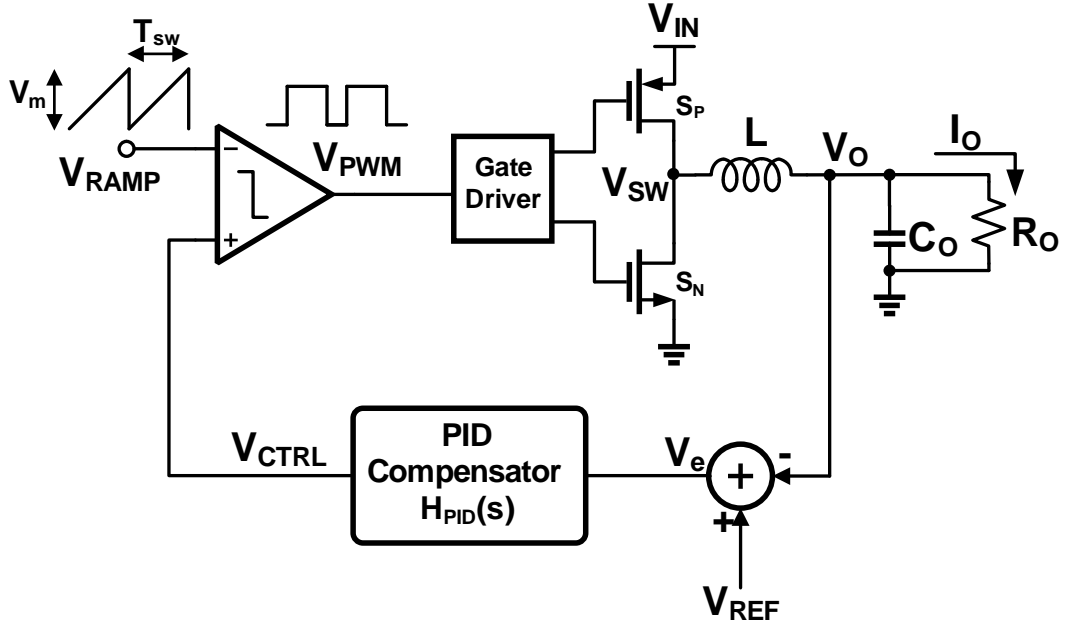
Figure 2.4: A PWM controlled switching dc-dc converter

The output voltage V_O is compared with a fixed reference voltage, V_{REF}. The resulting error voltage, Ve, is passed through a PID compensator which generates the control voltage, V_{CTRL}. The PWM signal is generated by comparing V_{CTRL}

with a fixed frequency ramp signal, V_{RAMP} as shown in Fig. 2.5 and controls the ON/OFF time of power MOSFET switches, S_P and S_N.
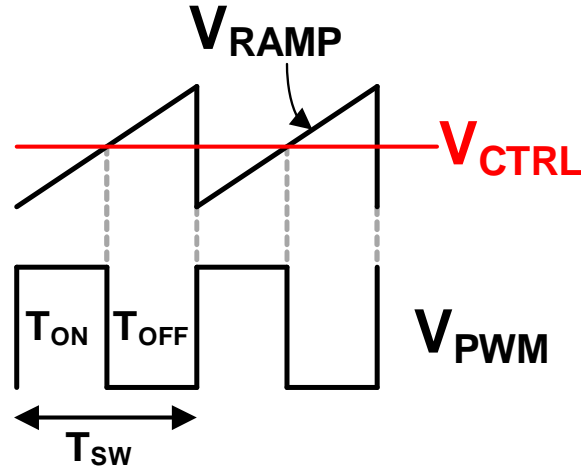
Figure 2.5: A pulse width modulated signal

2.3 Types of DC-DC Converters

Based on input to output conversion ratio, dc-dc converters are mainly classified into three categories.

(1) *Buck (Step − Down) Converter*: output voltage is always less than or equal to input voltage.

(2) *Boost (Step − Up) Converter*: output voltage is always higher or equal to input voltage

(3) *Buck − Boost Converter*: combines the features of both buck and boost hence output voltage could be either equal, lower or higher than the input voltage.

Fig. 2.6 shows the different converters along with their input-output voltage and current relationship with duty cycle.

All these three converters operate on the switching principle where output
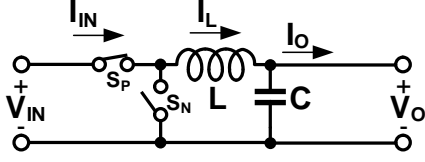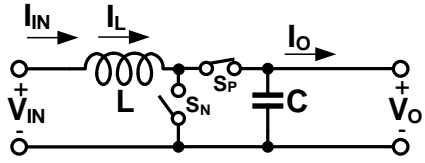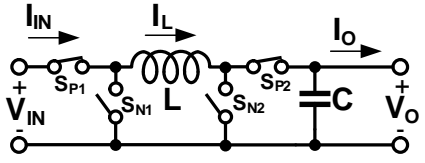
BUCK		$V_O = DV_{IN}$ $I_L = I_O$ $I_{IN} = DI_O$	$V_O \leq V_{IN}$
BOOST		$V_O = \dfrac{1}{1-D} V_{IN}$ $I_L = \dfrac{I_O}{1-D}$ $I_{IN} = I_L$	$V_O \geq V_{IN}$
BUCK BOOST		$V_O = \dfrac{D}{1-D} V_{IN}$ $I_L = \dfrac{I_O}{1-D}$ $I_{IN} = I_O$	$V_O \geq V_{IN}$ $V_O \leq V_{IN}$

Figure 2.6: Different classes of switching dc-dc converters

voltage is controlled by changing the duty cycle. The main difference lies in the power stage where switches are configured differently. In case of synchronous converters, the buck and boost can be used interchangeably by swapping the input/output voltages.

2.4   Switching Converter Control Techniques

The two most widely used control techniques in switching converters are (1) PWM Control and (2) Hysteretic Control. The main difference is that the PWM control is linear and operates with a fixed frequency as shown in Fig. 2.4.

A hysteretic control on the other hand is non-linear control and does not need any clock as it relies on self oscillations. The feedback loop is much simpler and does not require any compensation but it suffers from wide variation in

switching frequency. The details about hysteretic control technique are discussed in Chapter 4.

2.5 Voltage Mode vs. Current Mode PWM Control

Depending upon how feedback loop of a dc-dc converter is closed they can be classified into two categories, (1) voltage mode control (VMC) and (2) current mode control (CMC). The buck converter shown in Fig. 2.4 is essentially a VMC converter as it uses only voltage information in the feedback. A current mode converter on the other hand employs both current and voltage information.
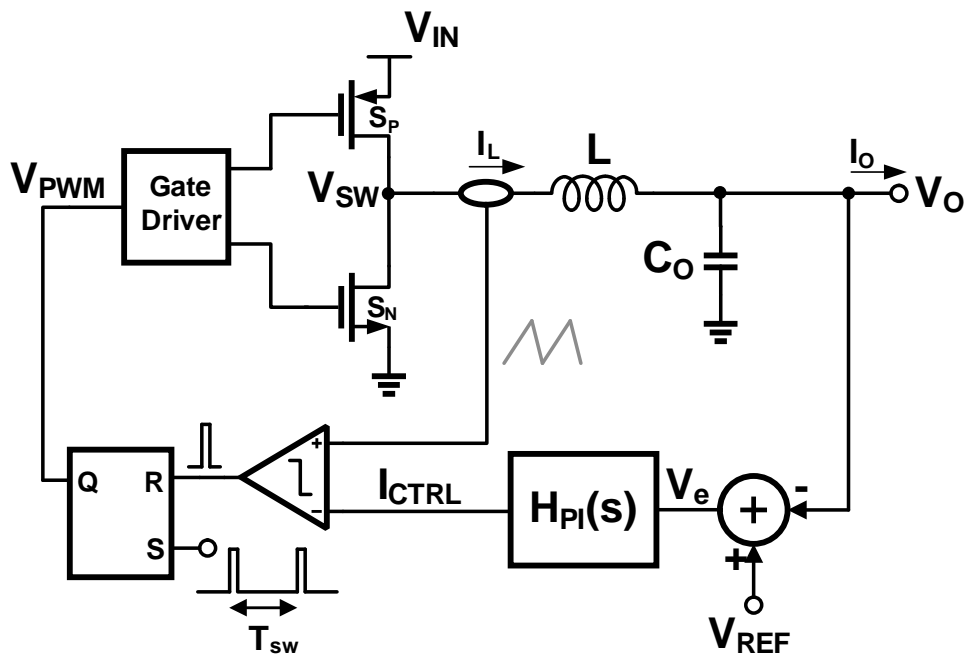
Figure 2.7: A current mode controlled dc-dc converter

As shown in Fig. 2.7, it has two feedback loops. Unlike an external PWM ramp signal used in voltage mode, the current mode converter uses inductor current, I_L as a ramp. The peak of this current is compared with a control current

which is generated from error signal processed through a compensator. The PWM signal is set at every edge of the clock period, T_{SW} and allows the inductor current to ramp up as seen from Fig. 2.8.
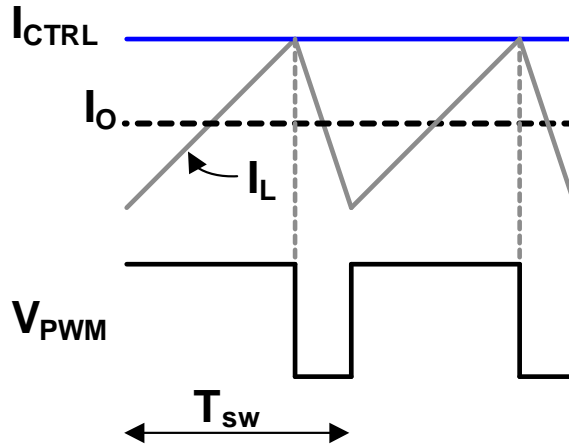
Figure 2.8: Pulse width modulation in a peak current mode converter

As soon as this current crosses the control current, the PWM signal is reset. Since feedback loop limits the peak of inductor current, it is called as peak current mode control (in a valley current mode current the valley limited). The current limiting action actually forces the inductor to behave like a constant current source and kills the resonance action of LC filter. The complex LC poles are therefore converted into a single real pole which is only due to the output capacitor, C_O and load resistor, R_O and requires only one zero for the loop compensation. A proportional-integral (PI) compensator is therefore used instead of PID which greatly reduces the complexity of control circuitry. The feed-forward action of current loop also offers much better response to line transients as compared to a voltage mode control where line suppression relies on the voltage feedback loop. However, the subharmonic oscillation due limiting only one side of the current (peak or valley) needs to be corrected by ramp compensation. A current mode

converter is also quite vulnerable to any noise at the switching node, V_{SW} and may cause false reset of the PWM signal or even cause unwanted oscillations [8], [9].

2.6   Efficiency of A Switching DC-DC Converter

The efficiency of an ideal dc-dc converter is 100% due to the fact that both inductor and capacitor used as output LC filter are lossless. However in practical scenario this is not true and the eq. 2.1 is no longer valid due to losses associated with the power switches and inductor dc resistance (DCR) as shown in Fig. 2.9.
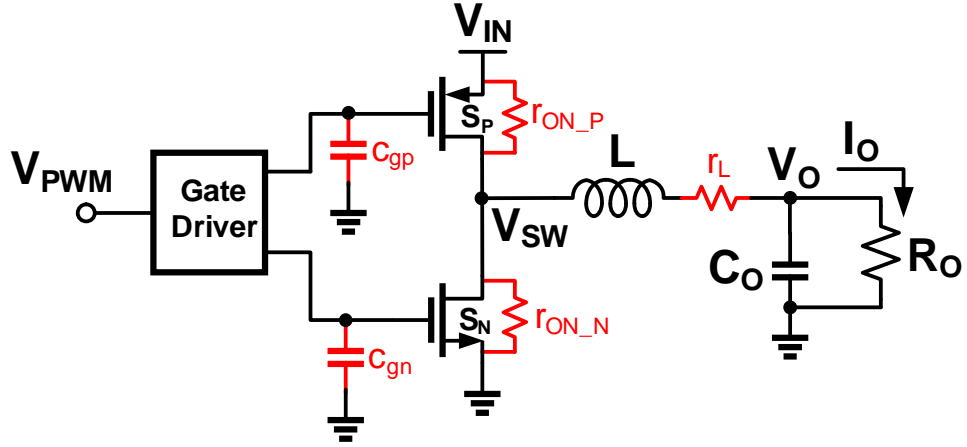
Figure 2.9: Different loss components associated with a dc-dc converter

The relationship between input and output voltages under loss is redefined as:

$$V_{OUT} = DV_{IN} - V_{loss} \tag{2.3}$$

Where V_{loss} is the voltage drop in the power stage due to losses. Therefore in order to keep the output voltage constant, the duty ratio D must be increased proportionally as loss goes higher. The current drawn from the input supply is

expressed as:

$$I_{IN} = DI_O \qquad (2.4)$$

Since input current drawn from the supply is proportional to the duty ratio, it could be observed that if losses in the power stage are higher then for the same output power the current drawn from the input supply increases thereby reducing the efficiency of the converter. The efficiency of a dc-dc converter is defined by the expression:

$$\eta = \frac{P_O}{P_{IN}} = \frac{P_{IN} - P_{loss}}{P_{IN}} \qquad (2.5)$$

Where P_O is the delivered output power , P_{IN} is the supplied input power and P_{loss} is the power loss.

The total power loss consists of following components:

$$P_{LOSS} = P_{cond} + P_{sw} + P_{dead} + P_{gate} + P_q \qquad (2.6)$$

The conduction loss, P_{cond} is mainly caused by the resistive losses such as ON resistance of the switches (r_{ON_P} and r_{ON_N}) and DCR of the inductor (r_L) as shown in Fig. 2.9. The conduction loss can be expressed as:

$$P_{cond} = I_O^2 \big(r_{P\_ON}D + r_{N\_ON}(1 - D) + r_L \big) \qquad (2.7)$$

The switching loss, P_{sw} is usually associated with the switching behavior of MOSFET switches [6] which depends upon various factors such as, parasitic junction capacitance, drain current and voltage across its terminals (Vgs and Vds). The presence of gate resistance and finite gate capacitance causes rise/fall time in

turning ON and OFF the MOSFET. Due to this finite rise/fall time, the MOS-FET exhibits high ON resistance and causes switching loss in the converter. The switching characteristic of a MOSFET is shown in Fig. 2.10. Faster the MOSFET is turned ON or OFF, lesser is the switching loss. The switching loss, P_{sw} is defined by:
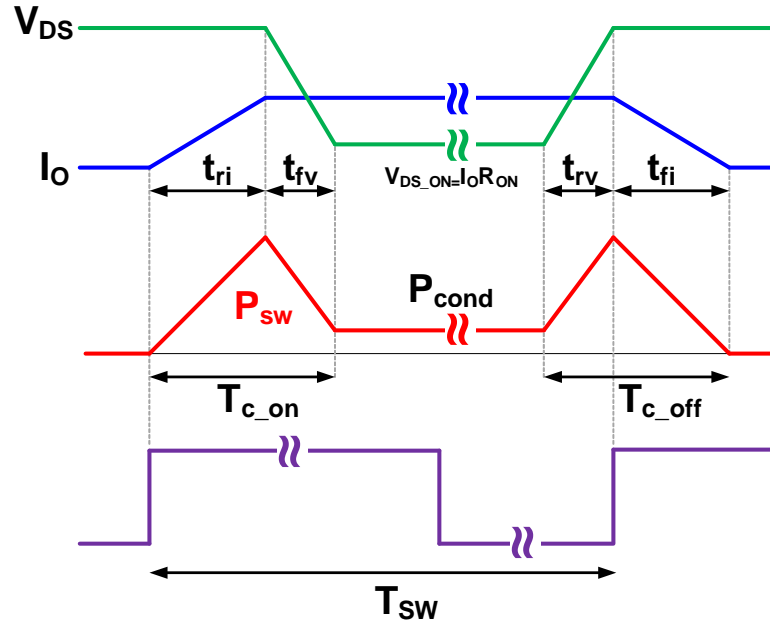
Figure 2.10: Hard switching losses (P_{sw}) in a dc-dc converter

$$P_{sw} = \frac{1}{2}V_{IN}I_O(t_{c\_on} + t_{c\_off})F_{SW} \tag{2.8}$$

Where t_{c_on} and t_{c_off} are the turn-on and turn-off times of the MOSFETs and F_{SW} is the switching frequency.

The dead time loss P_{dead} is due to non-overlap time between top and bottom switches as shown in Fig. 2.11. This dead time (t_{dead}) is needed in order to avoid short circuit due to simultaneous conduction of top and bottom switches. During this dead time, both top and bottom switches are OFF hence the conduction takes
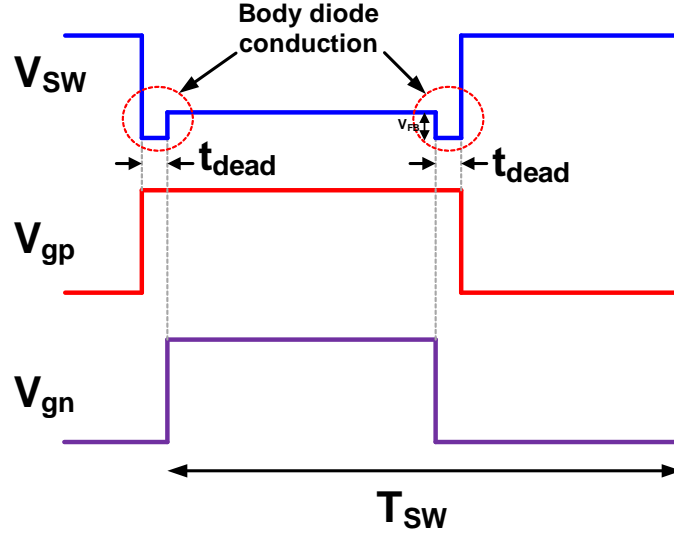
Figure 2.11: Dead time switching losses (P_{dead}) due to body diode conduction

place through body diode of the bottom MOSFET (S_N). The loss due to dead time is defined by:

$$P_{dead} = 2V_{FB}I_O t_{dead} F_{SW} \qquad (2.9)$$

Where V_{FB} is the forward bias voltage of the body diode which is $0.7V \sim 0.8V$ in most of the cases.

The gate switching losses are usually associated with the parasitic gate capacitors (c_{gp} and c_{gn}) of the MOSFET switches and expressed as:

$$P_{gate} = (c_{gp} + c_{gn})V_{IN}^2 F_{SW} \qquad (2.10)$$

The quiescent loss P_q is the controller power.

It could be observed from the above equations that both hard switching (P_{sw}) and conduction loss increases with the load current while the gate drive loss is fixed and independent of the load current. At lighter load current, conduction

and switching losses are negligible and gate drive loss starts dominating. When load current is much less compared to the gate switching losses, the converter is quite often operated in the PFM mode where switching frequency is scaled down with the load current to reduce losses. Dynamic FET sizing [7] is another effective technique to reduce the gate switching losses .

2.7   Control Loop Dynamics of DC-DC Converter

Transfer function of the LC filter of dc-dc converter shown in Fig. 2.4 is expressed as:

$$H_{LC}(s) = \frac{1}{LC_O^2 s + \frac{L}{R_O} s + 1} \tag{2.11}$$

Which exhibits a pair of complex poles causing $\approx 180°$ phase shift around resonance frequency ($w_O = \frac{1}{\sqrt{LC_O}}$) and making the loop unstable. The loop can be stabilized by simply using an integrator which provides the dominant pole compensation and pushes the complex poles out of the unity gain bandwidth (UGB). Although high dc gain of the integrator provides good voltage regulation but this type of compensation limits the loop bandwidth and degrades the transient performance of the converter. For better transient response a proportional-integral-derivative (PID) compensator is used in a voltage mode PWM controller. A PID compensator is defined by the following transfer function [4]:

$$H_{PID}(s) = K \frac{\left(1 + \frac{w_L}{s}\right)\left(1 + \frac{s}{w_z}\right)}{1 + \frac{s}{w_p}} \tag{2.12}$$

The integral term amplifies the error voltage at dc in order to regulate the output voltage around V_{REF} while the two zeros (w_L and w_Z) provide phase boosting to inhibit the effect of complex poles due to LC filter and provide a sufficient

phase margin around the crossover frequency. w_p is a high frequency pole used to suppress the high frequency noise due to switching and kept outside the UGB. The overall loop transfer function of a compensated buck converter can be expressed as [4]:

$$T(s) = \frac{V_{IN}}{V_m} H_{PID}(s) H_{LC}(s) \tag{2.13}$$

Where, $\frac{V_{IN}}{V_m} = G_{PWM}$ is the gain of PWM modulator and power MOSFET stage. The bode plot of a PID compensator is shown in Fig. 2.12. The location of two zeros (w_L and w_Z) is chosen such that enough phase boost is obtained to suppress the resonance due to LC filter and K is adjusted to get the desired crossover frequency. The detailed design of a PID compensator is discussed in Chapter 5.
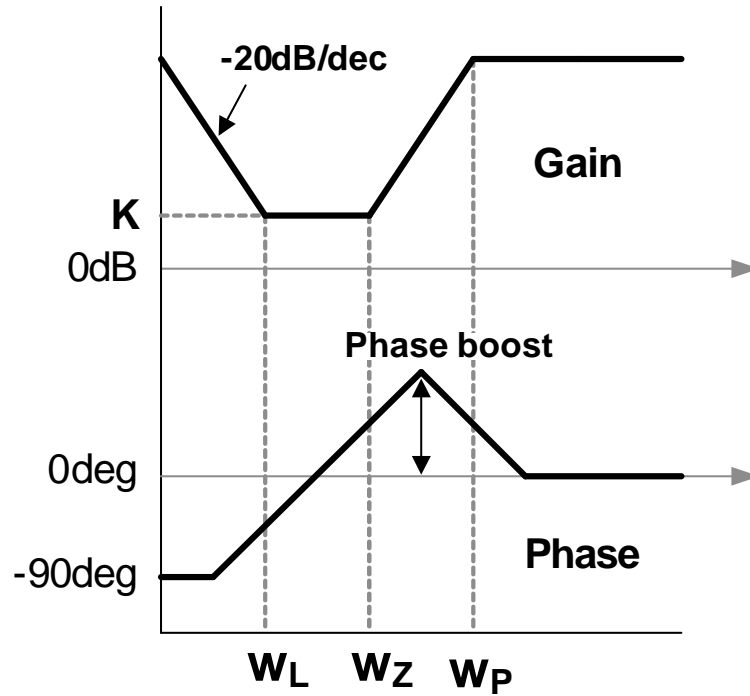
Figure 2.12: Bode plot of the PID compensator

Simulated loop gain and phase response of a an uncompensated and compensated buck converter is shown in Fig. 2.13. The uncompensated loop has phase margin of only 8° and therefore unstable.
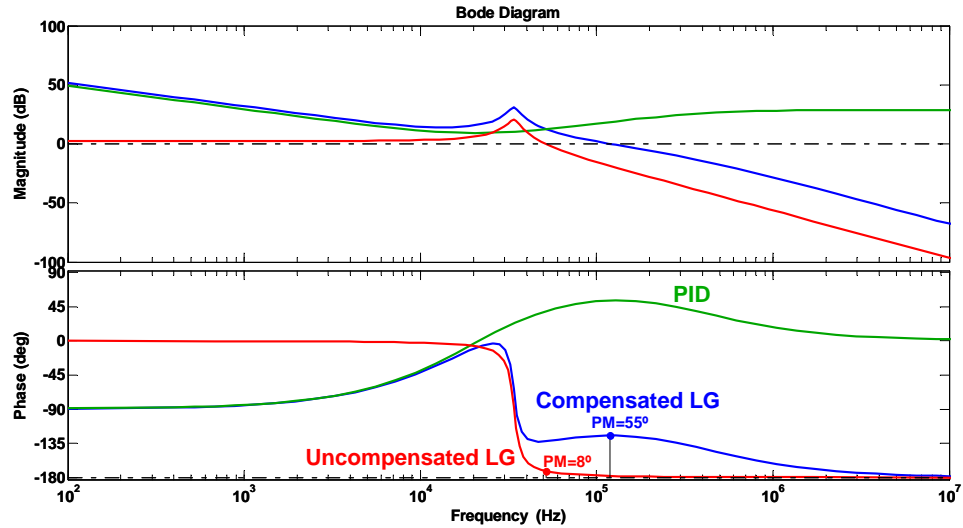
Figure 2.13: Bode plot of an uncompensated and compensated buck converter

2.8 Switching Noise Caused by DC-DC Converter

Just like any other switching circuit, the dc-dc converter has tendency to produce switching noise. There are mainly three types of noise generated by switching converter.

2.8.1 Substrate Injection

The substrate noise is caused by the body diode conduction of NMOS switch during dead time. During dead time, the current flows from ground (GND) to the inductor through body diode which is formed between the drain terminal of

bottom switch (S_N) and p-substrate as shown in Fig. 2.14.
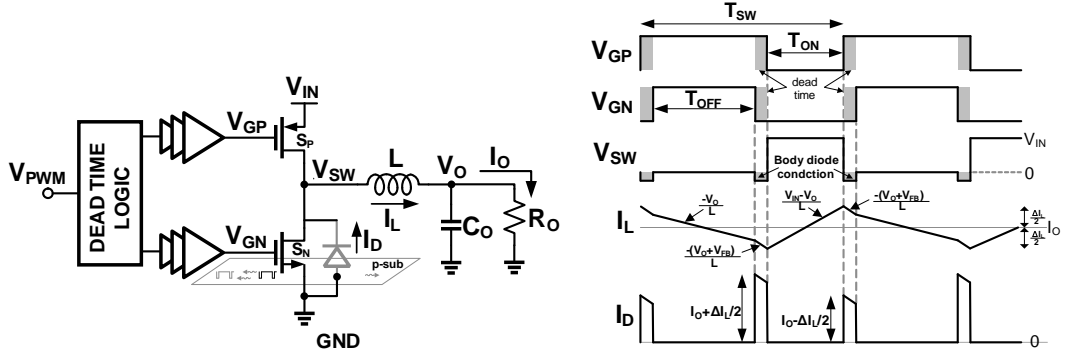
Figure 2.14: Substrate noise injection due to body diode conduction

This negative current injection disturbs the substrate potential (which is connected to GND) causing substrate noise. This noise may propagate through the substrate causing issue for the neighboring noise sensitive circuits. To prevent this noise from propagation, the bottom switch should be surrounded by enough substrate contacts connected to GND. This provides a local low resistive path to the substrate noise and prevents it from propagating further. An isolated p-well (in case of deep n-well process) also helps in preventing the substrate noise by completely isolating the body diode of bottom switch from the chip substrate.

2.8.2   Supply and Ground Bounce

The switching action of V_{PWM} causes S_P to connect to the internal supply voltage, V_{IN} during ON time and S_N to connect to internal ground, VSS during OFF time causing a switching current drawn from the supply, PWR and ground GND as shown in Fig. 2.15.

Considering the fast turn ON/OFF time of the switches, the finite parasitic inductances (L_{PP} and L_{PN}) associated with power and ground causes large $L\frac{di}{dt}$
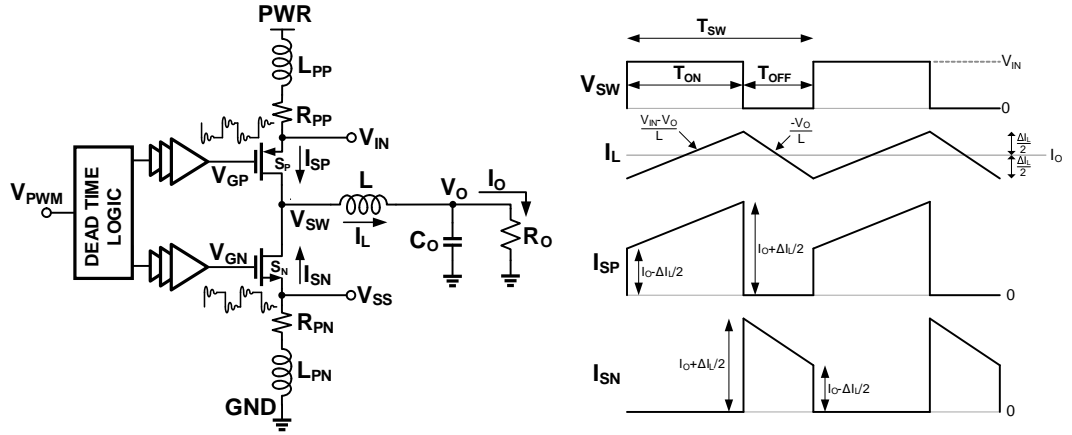
Figure 2.15: Supply and Ground noise in a DC-DC converter

noise in V_{IN} and V_{SS}. These parasitics inductances, when coupled with parasitic capacitance, also produce resonance and may even cause breakdown of the switches if amplitude of the ringing (due to resonance) is large. Another issue cause by this switching noise is electromagnetic interference (EMI). The problem could be suppressed by reducing the parasitic inductances which is mainly due to the bond wires and board traces. Putting decoupling capacitors between V_{IN} and V_{SS} also damps the resonance and helps in reducing noise.

$NOTE$: In case of a boost converter, the switching action takes place between output and ground so the noise generated in V_{IN} is not significant.

2.8.3 Output Ripple

The finite bandwidth of the output LC filter and capacitor's ESR does not completely filters out the high frequency noise of PWM switching node, V_{SW} and appears as ripple in the output voltage. This ripple consists of two components, capacitive ripple and ESR ripple as shown in Fig. 2.16.

Figure 2.16: Output voltage ripple of a buck converter

If ΔV_{CO} is the capacitor ripple voltage then, output voltage ripple can be expressed as:

$$\Delta V_O(t) = \Delta V_{ESR}(t) + \Delta V_{CO}(t) \tag{2.14}$$

In case of small ESR, the output ripple is mostly dominated by the capacitive component, and pk-pk ripple can be found by charge transfer theorem. The total positive charge stored in the inductor during time $t_1 - t_2$ is simply the area under triangle, Q_P i.e.

$$Q_P = \frac{1}{2}\left(\frac{1}{2}T_{SW}\right)\left(\frac{\Delta I_L}{2}\right) = \frac{1}{8F_{SW}}\Delta I_L \tag{2.15}$$

The change in capacitor voltage due to this charge can be given as (using $Q = CV$):

$$\Delta V_{CO} = \frac{1}{C_O} \frac{1}{8F_{SW}} \Delta I_L \tag{2.16}$$

Substituting inductor ripple current, $\Delta I_L = \frac{V_{IN} - V_O}{L} DT_{SW}$, the output ripple voltage can be expressed as:

$$\Delta V_O = \frac{V_{IN} D(1-D)}{8F_{SW}^2 LC_O} \tag{2.17}$$

Which is the expression for output ripple voltage in case of small ESR.

In case of large ESR, the output ripple is dominated by ΔV_{ESR} and can be expressed as:

$$\Delta V_O = \Delta I_L R_{ESR} = \frac{V_{IN} D(1-D)}{F_{SW} L} R_{ESR} \tag{2.18}$$

Which shows that the output voltage ripple can be controlled by properly choosing F_{SW}, L and C_O. Capacitor with low ESR also helps in reducing the output ripple.

2.9 Discontinuous Conduction Mode (DCM)

In a switching dc-dc converter, the direction of inductor current is always positive i.e. towards output if we assume zero inductor ripple current. However, in reality the inductor ripple current, can not be ignored as it may cause the reversal of inductor current when load current is low. Since the inductor ripple current is given by $\Delta I_L = \frac{V_{IN} - V_O}{L} DT_{SW}$, the valley of inductor current hits 0 when load current goes to $\Delta I_L / 2$ as shown in Fig. 2.17.

If the converter is operated in continuous conduction mode (CCM), i.e the current is always flowing through the inductor, further reduction in load current
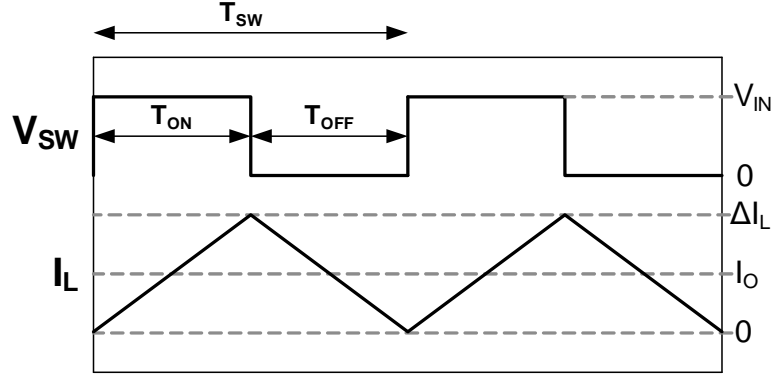
Figure 2.17: Inductor current valley hitting zero in case of light load

causes output capacitor to discharge through bottom switch and reduces the efficiency. In order to prevent this, the current through inductor should be cut-off as soon as the ripple valley hits zero. This could be achieved by detecting the zero crossing voltage at V_{SW}, which indicates the change of current direction, and turning the bottom switch OFF. The implementation for DCM operation is shown in Fig. 2.18.
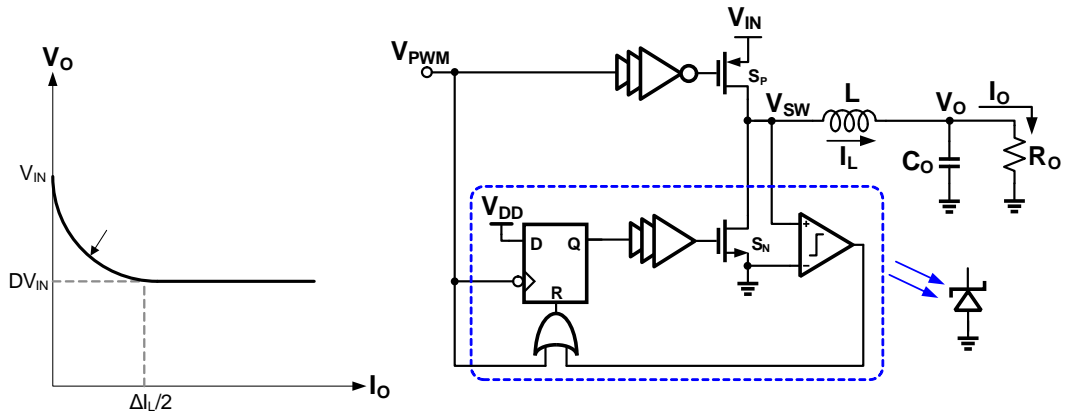
Figure 2.18: Implementation of DCM in a buck converter

The condition at which the converter enters DCM can be derived as follows: The valley of inductor ripple current hits zero when $I_O = \frac{\Delta I_L}{2}$, i.e.

$$I_O = \frac{1}{2}\frac{V_{IN} - V_O}{L}DT_{SW} \qquad (2.19)$$

Assuming, R_O is the load resistor then $I_O = \frac{V_O}{R_O}$, the above expression can be written as:

$$\frac{V_O}{R_O} = \frac{V_{IN} - V_O}{2L}DT_{SW} \qquad (2.20)$$

or

$$V_O = D(V_{IN} - V_O)\frac{R_O T_{SW}}{2L} \qquad (2.21)$$

Term $\frac{2L}{R_O T_{SW}}$ is defined as K_{crit} which marks the boundary condition for DCM [4]. The converter remains in CCM as long as $\frac{2L}{R_O T_{SW}} > K_{crit}$ and output voltage is expressed as $V_O = DV_{IN}$. However in DCM the output voltage keeps rising with reduction in load current and expressed as:

$$V_O = \frac{2}{1 + \sqrt{1 + \frac{4K}{D^2}}} \qquad (2.22)$$

where $K = \frac{2L}{R_O T_{SW}}$ and valid for $K < K_{crit}$

Therefore in DCM, the feedback control should reduce the duty cycle with reducing load current to regulate the output voltage otherwise output voltage will eventually saturate to V_{IN} as shown in Fig. 2.18.

Usually, the converter is operated in PFM mode in DCM where switching frequency is reduced with load. This helps in maintaining the output regulation when duty cycle is saturated to its minimum value and also reduces the gate switching losses associated with the top and bottom switches.

$NOTE$: In a non-synchronous converter, the DCM operation is automatic due the bottom diode as it goes reverse biased when for negative inductor cur-

rent and cuts-off the conduction. The DCM implementation in Fig. 2.18 actually emulates an active diode.

CHAPTER 3. DIGITAL CONSTANT ON/OFF TIME DELTA-SIGMA FRACTIONAL-N CONTROL FOR BUCK-BOOST CONVERTER

This chapter presents an all-digital Buck-Boost converter that obviates the need for a high resolution DPWM and external compensation capacitor while maintaining high efficiency over a wide input range. We further leverage the highly digital architecture to achieve seamless transitioning between the modes of operation reliably under all operating conditions.

The chapter is organized as follows. Section 3.1 gives an introduction to buck-boost dc-dc converter and discusses trade-offs with the existing designs. The concept of constant ON/OFF time is demonstrated in Section 3.2. The proposed architecture is introduced in Section 3.3. Section 3.4 discusses the design of fractional-N controller. The measurement results are shown in Section 3.5.

3.1 Introduction to Buck-Boost Converter

A typical Li-ion battery output voltage, as shown in Fig. 3.1, is at $5.5V$ when fully charged and drops to $2.7V$ when fully discharged. Therefore, a buck converter fails to regulate the output at $3.3V$ over the entire range of battery voltage and using only boost converter on the other hand would be inefficient.

A conventional buck-boost converter [4], [10] shown in Fig. 3.2, implemented using a single duty cycle control, is highly inefficient due to higher average inductor current.
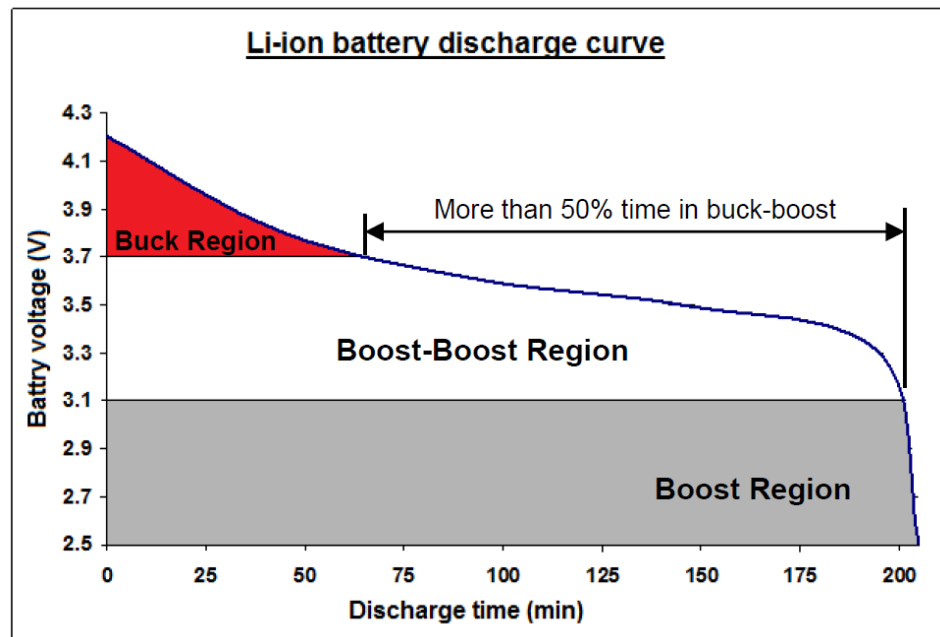
Figure 3.1: Discharging profile of a Li-ion battery

$$S_1 = S_3 = S \qquad S_2 = S_4 = \overline{S}$$
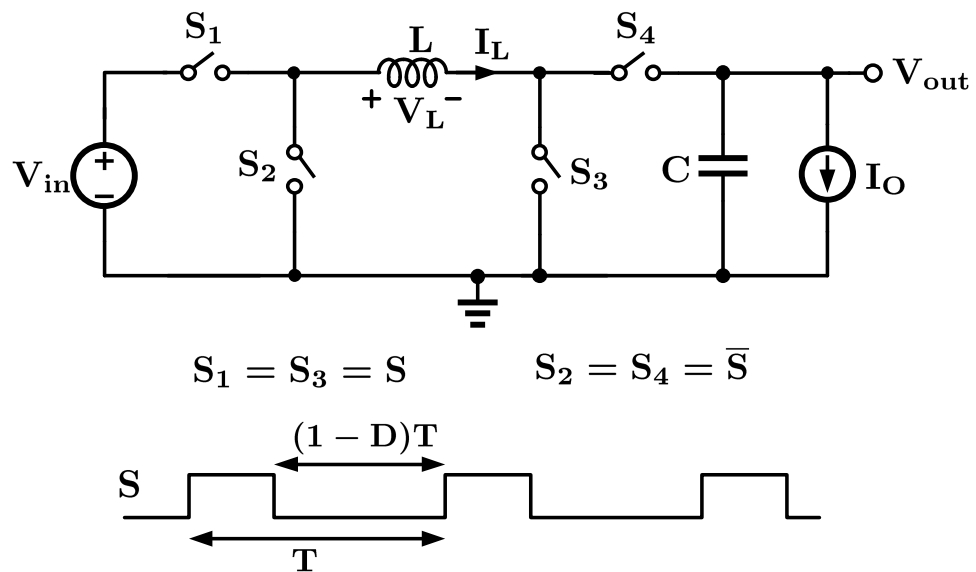
Figure 3.2: Conventional single-mode Buck-Boost converter.

Such type of converter operates in both Buck and Boost modes even when the input voltage is large (or small) enough to operate only in the Buck (or Boost)

mode. The impact of such an operation on the converter efficiency can be best understood by referring to the output voltage, V_{OUT}, and inductor current I_L in the expressions shown below.

$$V_{OUT} = \frac{D}{1-D}V_{in} \quad \text{and} \quad I_L = \frac{1}{1-D}I_O \tag{3.1}$$

Since the inductor current is stepped up, the efficiency degrades with increasing duty cycle. For instance, if $V_{IN} = V_{OUT}$ then the desired duty cycle according to above equation should be, $D = 0.5$. The corresponding inductor current is 2x of the output load current, I_O, thereby increasing the conduction losses (as expressed in eq. 2.7 of Chapter 2) by 4 times. This causes a significant drop in the efficiency.

The higher inductor current problem is resolved by independently controlling buck and boost switches (tri-mode operation) as shown in Fig. 3.3 and activating buck-boost mode only when the input is around output voltage [11], [10].
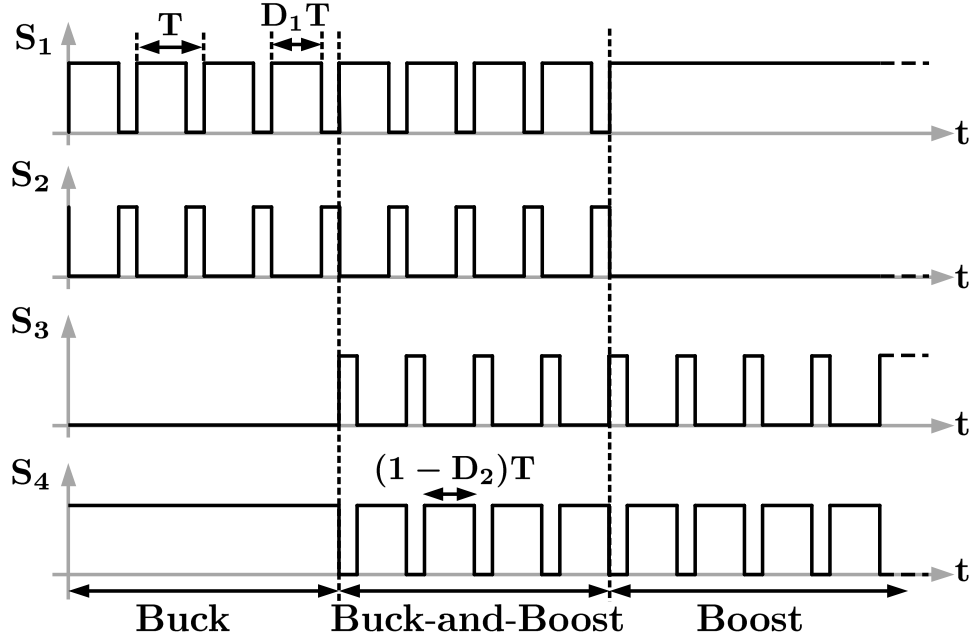
Figure 3.3: Tri-mode converter timing diagram.

Assuming that buck and boost duty cycles are controlled independently, the
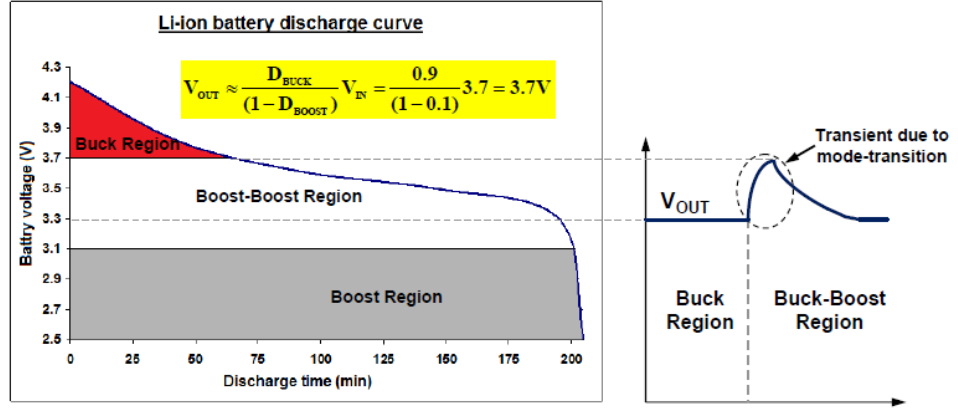
Figure 3.4: Overshoot during mode transition in a tri-mode buck-boost converter

eq. 3.1 can be written for a tri-mode buck-boost converter as below:

$$V_{out} = \frac{D_1}{1 - D_2}V_{in} \quad \text{and} \quad I_L = \frac{1}{1 - D_2})I_O \qquad (3.2)$$

Where D_1 is the duty cycle of buck switches (S_1 and S_2) and D_2 is the duty cycle of boost switches (S_3 and S_4). A close observation of eq. 3.2 indicates that condition $V_{IN} = V_{OUT}$ can still be met by limiting D_1 and D_2 to their maximum and minimum values respectively. For instance if $D_1 = 0.9$ and $D_2 = 0.1$ then V_{OUT} becomes equal to V_{IN} while keeping the inductor current $\approx I_O$ and reducing the conduction losses. Even though this technique greatly improves the efficiency, there exists a dead zone between boundaries of the operating modes where converter's behavior becomes non-linear and switching is unpredictable [12]. Since the maximum buck duty cycle at the boundary is larger than the required for making smooth transition, it causes a large overshoot in the output voltage (3.4). This overshoot and settling becomes even worse in case of only integral compensated loop due to sluggish response [10].

Therefore ensuring smooth transition between different modes of operation

in tri-mode buck-boost converter becomes challenging. The solutions proposed in [10], [13] address mode transition issue, however the analog nature of the controller makes it susceptible to operating conditions and the controller also requires external compensation capacitor.

This chapter presents an all-digital Buck-Boost converter that obviates the need for a high resolution DPWM and external compensation capacitor while maintaining high efficiency over a wide input range [14]. We further leverage the highly digital architecture to achieve seamless transition between the modes of operation reliably under all operating conditions.

Unlike the conventional PWM method, the proposed converter uses constant ON/OFF time to regulate the output voltage. The next section discusses how a constant ON/OFF time technique helps in minimizing the overall inductor ripple current and leads to the design of proposed Fractional-N digital buck-boost controller.

3.2   Constant ON/OFF Time Operation

Considering a standard buck converter, the inductor ripple current during ON time (T_{ON}) can be expressed as:

$$\Delta I_{L\_ON} = \frac{V_{IN} - V_{OUT}}{L} T_{ON} \tag{3.3}$$

Where V_{IN} is the input voltage, V_{OUT} is the output voltage and L is the inductor value. Inductor ripple current during OFF time (T_{OFF}) is given by

$$\Delta I_{L\_OFF} = \frac{V_{OUT}}{L} T_{OFF} \tag{3.4}$$

If converter duty cycle is fixed at 50% and operated at 10MHz ($T_{ON} = T_{OFF}$ = 50ns), assuming $L = 1\mu H$ and V_{OUT} is regulated at 3.3V, the inductor ripple current during ON and OFF time can be calculated as:

$$\Delta I_{L\_ON} = \Delta I_{L\_OFF} = \frac{3.3}{1\mu} 50n = 165mA \tag{3.5}$$

If the required duty cycle is more than 50%, simply making the ON time proportional to V_{IN} while keeping the OFF time constant time can still regulate V_{OUT}. Although this would make the switching frequency proportional to V_{IN}, the voltage across inductor also decreases inversely with ON time making Voltage-Time product constant. Hence inductor ripple current remains constant. This scenario is illustrated in Fig. 3.5 where V_{OUT} is regulated at 3.3V by making the ON time inversely proportional to V_{IN} while OFF time is fixed at $50ns$.
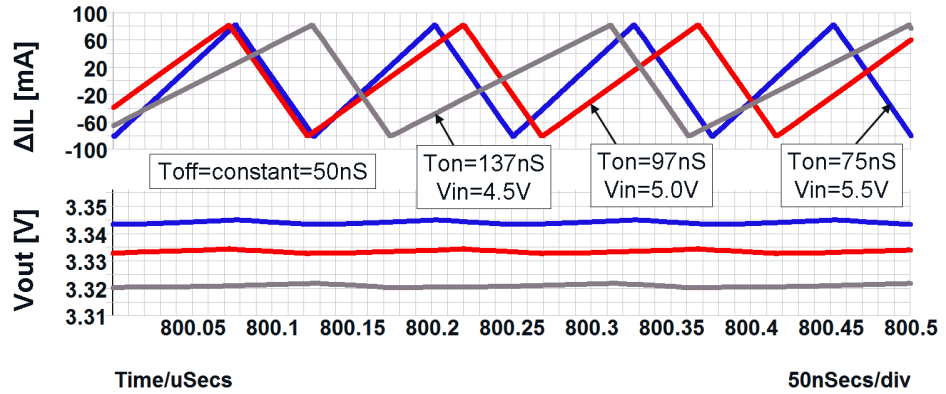
Figure 3.5: Inductor ripple current and output voltage of a buck converter for constant OFF time (variable ON time).

A similar argument applies for duty cycle less than 50%, where ON time can be fixed at $50ns$ and OFF time is varied proportional to V_{IN} for regulating the output voltage. Since inductor ripple current and ESR of the capacitor govern output voltage ripple, as long as switching frequency is significantly higher than

LC cutoff, the output voltage ripple still remains lower.

Since regulating the output voltage with only ON time would again require a high resolution scheme similar to that of PWM. Therefore we exploit the benefit of lower inductor ripple current of constant ON/OFF time technique in the proposed converter by using only two duty cycles as discussed next.

3.3 Proposed Architecture

The block diagram of the proposed digitally controlled Buck-Boost converter [14] is shown in Fig. 3.6. Power-FETs, P_{BU}, N_{BU}, P_{BO} and N_{BO} are controlled by two independent control signals, D_{BUCK} and D_{BOOST}.
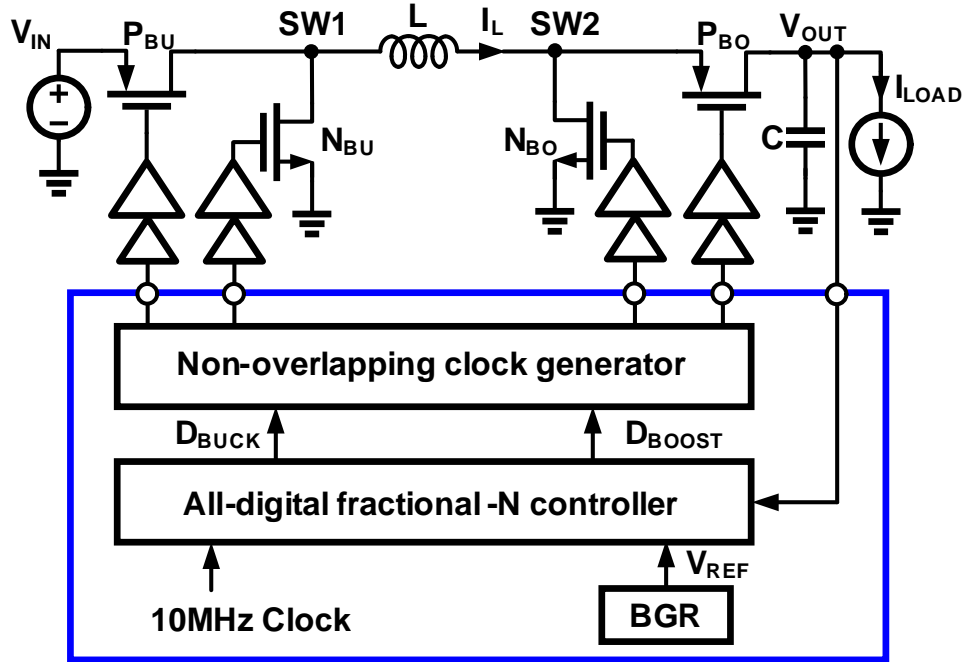
Figure 3.6: Proposed digital Buck-Boost converter

Unlike in a conventional controller, the power-FETs are operated in only two well-defined duty cycles of 50% and 100% or 50% and 0% by keeping either

ON or OFF time constant. Based upon the number (N) of 50% duty cycles, the entire input voltage region is divided into 11 pre-defined states ($ST1$ to $ST11$) and stored in a look-up table (LUT) shown in Fig. 3.7. The output is regulated by dithering between the two adjacent states. Since the power-FETs are either ON/OFF for a fixed period of time in every clock cycle, high-resolution digital PWM is not needed. The fixed 50% and 100% (or 0%) duty cycles also makes it possible to operate the converter at much higher frequency (10 MHz) as compared to conventional PWM.

Operating States	Control Code	Fraction N:1
Buck Mode		50%Buck:100%Buck
ST1	0001	5:1
ST2	0010	4:1
ST3	0011	3:1
ST4	0100	2:1
ST5	0101	1:1
Buck-Boost Mode		50%Buck:50%Boost
ST6	0110	1:1
Boost Mode		50%Boost:0%Boost
ST7	0111	1:1
ST8	1000	2:1
ST9	1001	3:1
ST10	1010	4:1
ST11	1011	5:1

Decreasing V_{IN}

Figure 3.7: Lookup table for control mapping

Depending upon whether V_{IN} is higher, equal or lower than V_{OUT}, the converter automatically switches between modes of operations, as discussed below.

3.3.1 Buck Mode and Boost Mode

The converter operates in buck-mode if V_{IN} is significantly higher than V_{OUT}. During this mode, D_{BOOST} is always 0% and D_{BUCK} outputs either 50% or 100% duty cycle of a 10MHz clock. Number of 100% buck cycle is always kept one while number of 50% cycles (N) is varied depending upon V_{IN}. N varies from 1 to 5 making total of five states ($ST1$ to $ST5$) in the buck mode.

Similarly when V_{IN} falls much below V_{OUT}, the converter operates in boost mode. During boost-mode, D_{BUCK} is always 100% and D_{BOOST} outputs the control signal which is one cycle of 0% boost and N cycles of 50% boost. The integer N is varied from 1 to 5 again making a total of five states ($ST7$ to $ST11$).

3.3.2 Buck-Boost Mode

If V_{IN} falls between any value for which either buck or boost mode fails to regulate V_{OUT} then converter goes into buck-boost mode. The last state of buck ($ST5$) and first state of boost ($ST7$) mark the boundaries of the buck-boost region. Only one state ($ST6$) corresponding to buck-boost is stored in the LUT where both D_{BUCK} and D_{BOOST} switch between 50% buck and 50% boost duty cycles respectively every alternate clock period. For any other input voltage in this mode, the output voltage is regulated by dithering between states $ST5$ and $ST6$ or $ST6$ and $ST7$ depending upon whether V_{IN} is higher or lower than V_{OUT}.

The inductor current profile in various states ($ST1$-$ST5$) of buck mode is shown in Fig. 3.8. The average inductor current remains same as load current which is $500mA$ while maximum peak-to-peak ripple current is $340mA$ and occurs

in state $ST1$. It should be noted that a fixed frequency PWM converter for the same $\frac{V_{OUT}}{V_{IN}}$ would require L of $2\mu H$ in order to achieve the same ripple current. This shows $2X$ reduction in L by using the proposed constant ON/OFF time method.
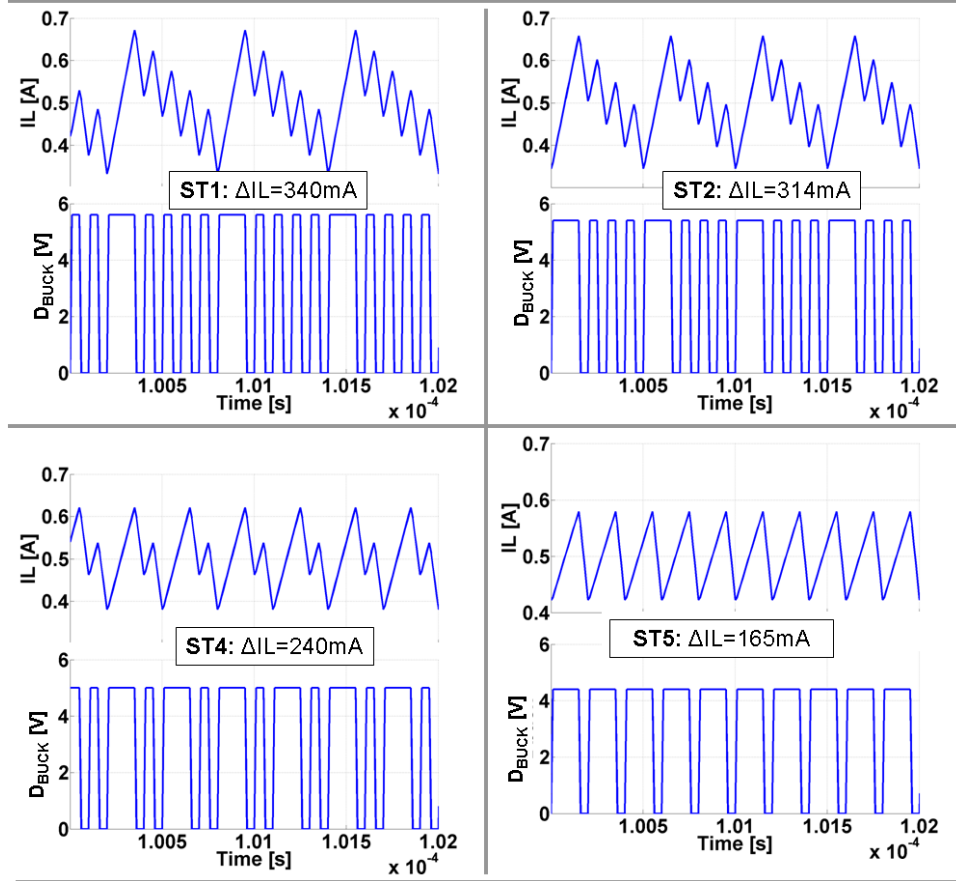
Figure 3.8: Profile of inductor current in different states of buck-mode

The inductor currents for buck-boost state ($ST6$) and boost state ($ST7$) are shown in Fig. 3.9. The ripple current in both $ST6$ and $ST7$ remains low but the average inductor current increases to $650mA$ due to 1 : 1 boost operation. However, this increase in average current is still 70% lower as compared to a single duty cycle controlled buck-boost converter.
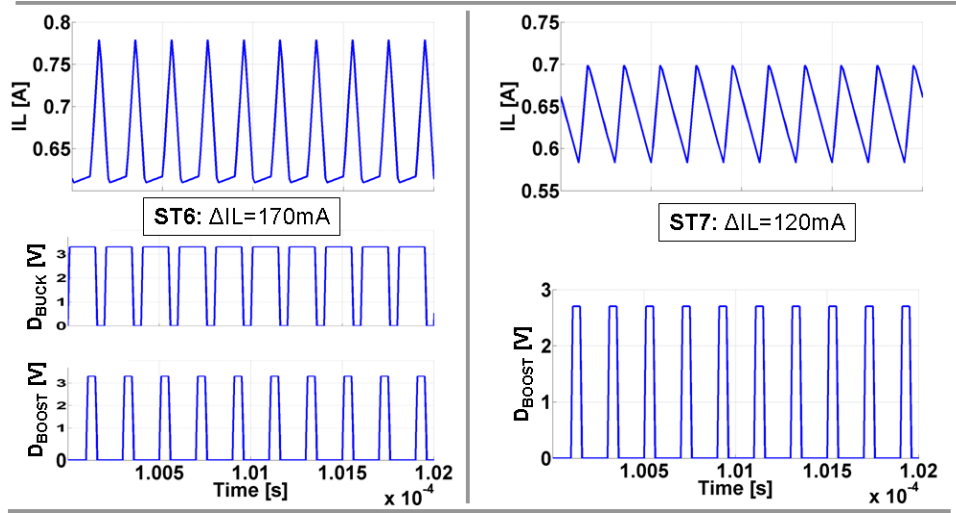
Figure 3.9: Profile of inductor current in buck-boost and boost states

3.4 Fractional-N Controller Design

The proposed digital Fractional-N controller is shown in Fig. 3.10. The controller is composed of a comparator, an accumulator, and look-up table (LUT) that outputs D_{BUCK} and D_{BOOST}. The comparator detects the sign of the voltage error between the scaled output voltage and the reference voltage (V_{REF}) and drives 18-bit digital accumulator. Because of the hard non-linearity introduced by the comparator, the steady state of the converter is a bounded limit cycle that manifests itself as output voltage dithering [20]. To attenuate the resulting output ripple, the lower 7 least significant bits (LSBs) in the accumulator output are dropped. A $1st$-order digital delta-sigma ($\Delta\Sigma$) modulator truncates the 11 most significant bits (MSBs) to 4 bits which dither between two adjacent states of LUT. This 11-bit to 4-bit conversion greatly simplifies the implementation of fractional-N control circuit.

The LC low-pass filter, following the power stage, suppresses the high fre-
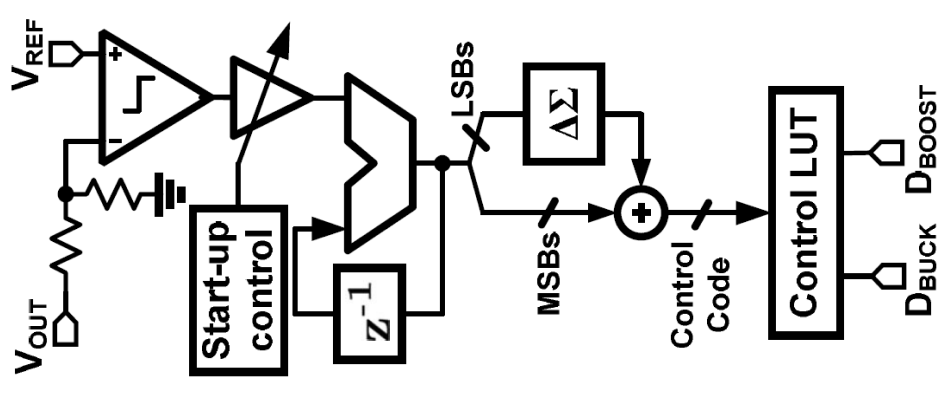
Figure 3.10: Digital Fractional-N controller implemented the proposed buck-boost converter

quency quantization error introduced in the fractional-N control and generates a constant DC output voltage. A start-up control circuit increases the loop gain on power up to improve the turn-on time of the converter. The loop gain is reduced as soon as first negative edge of comparator output (Comp Out) occurs indicating that V_{OUT} had risen up to $3.3V$. Once the output is settled, the LSB code toggles between $+/-1$ LSB. The various control signals and output voltage are shown in Fig. 3.11. For the ease of reading, the control codes are shown in decimal instead of binary in the plot.

The use of higher switching clock frequency and N:1 dither pattern ensures lower fractional tone at the output that remains well below 50dB and peak to peak ripple remains within 10mV. The output voltage for buck and buck-boost modes of operation with their corresponding frequency spectrum is shown in Fig. 3.12. The amplitude in frequency spectrum is normalized to $3.3V$.

The proposed Fractional-N control also enables seamless transition between modes. The voltage ripple in the output voltage is only $20mV$ when converter switches from buck mode to buck-boost as shown in Fig. 3.13.
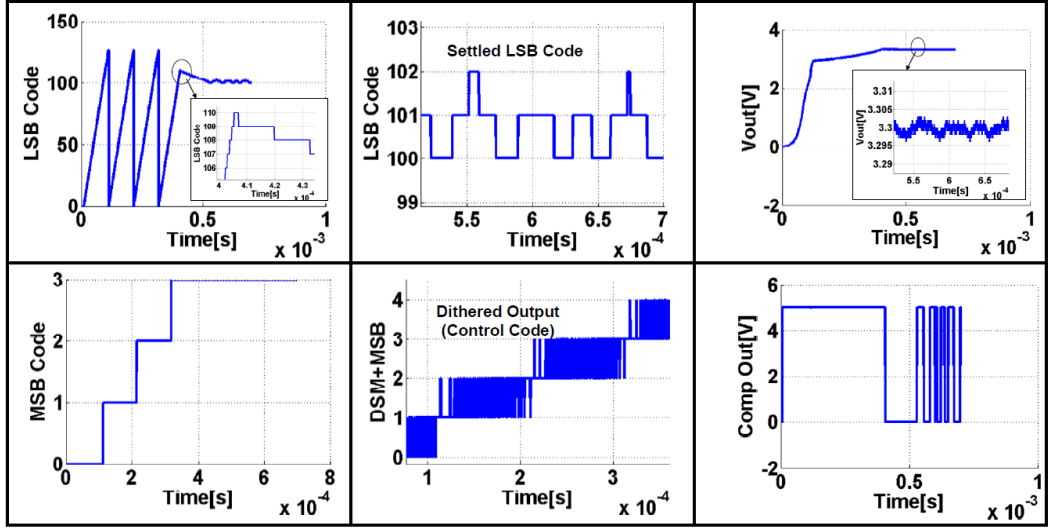
Figure 3.11: Control signals and output voltage of the proposed controller

3.5 Experimental Results

The proposed Buck-Boost DC-DC converter was fabricated in 500nm CMOS process and packaged in a 4x4 micro SMD package. The die size is $4mm^2$ as shown in Fig. 3.14. Using an off-chip $1\mu H$ inductor and a $10\mu F$ capacitor the prototype operates at 10MHz clock frequency and regulates the output voltage to $3.3V$.

The output voltage, measured by slowly varying the input voltage from $3.3V$ to $5.5V$, shown in Fig. 3.15. illustrates robust regulation immune to any mode-transition transients present in conventional analog PWM-controlled buck-boost converters.

Fig. 3.16 shows the measured switching profile in different operating states. It could be observed that the number of boost cycles is 0 in ST5 (buck mode) and dithers between between ST5 and ST6 as V_{IN} decreases.

The efficiency plot is shown in Fig. 3.17 . The converter achieves efficiency
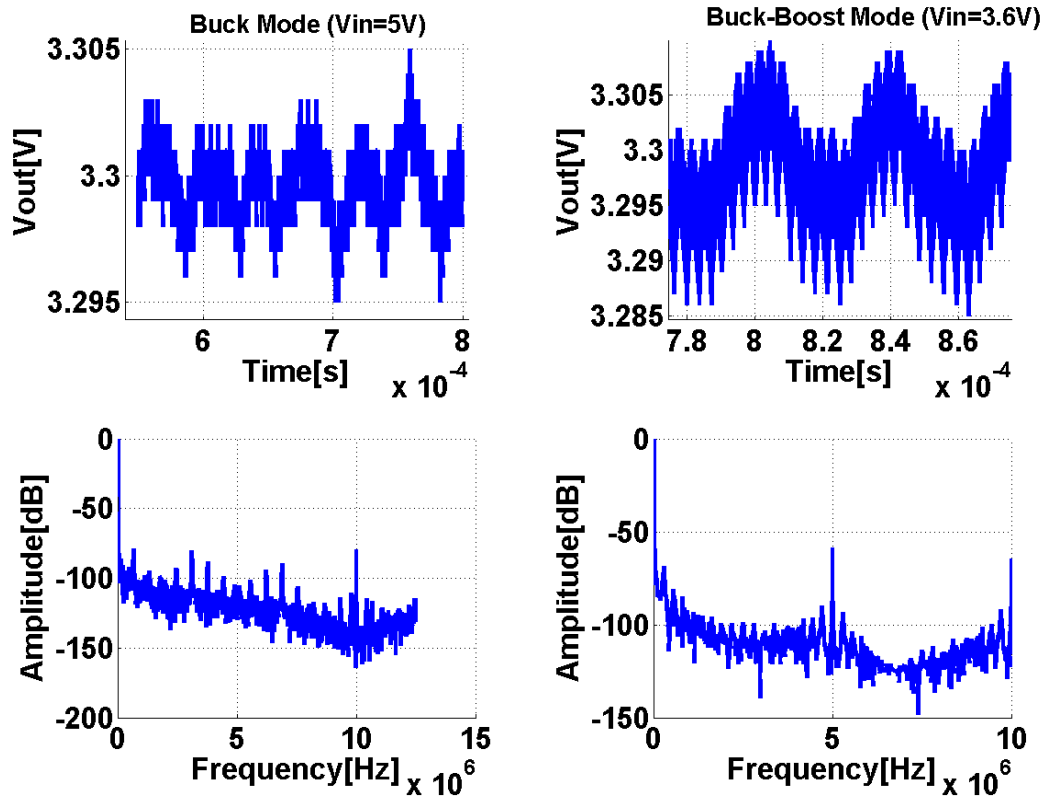
Figure 3.12: Output voltage and spectrum plot of the proposed converter in buck and buck-boost modes
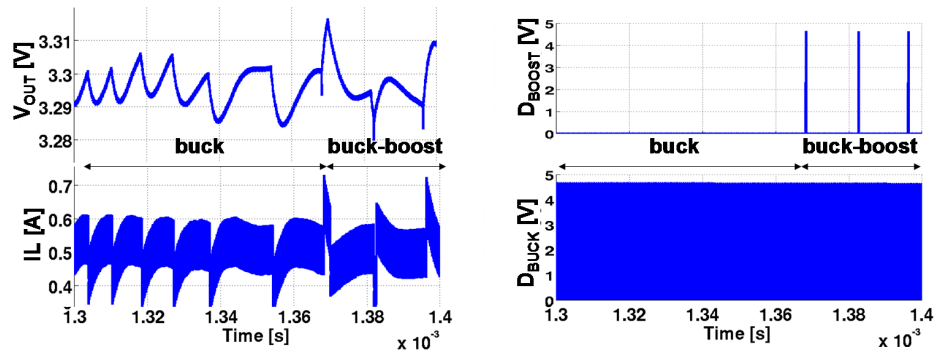
Figure 3.13: Output waveforms of the proposed converter during buck to buck-boost mode transition.

of $85\% - 92\%$. The reduction in efficiency at lower input voltage is mainly due to increased ON resistance of power switches.

Technology	0.5µm CMOS
L	1µH
C	10µF
ESR in C	10mΩ
ESR in L	50mΩ - 100mΩ
Vout	3.3V
Vin	3.3V to 5.5V
Load Current	500mA
Efficiency	85% - 92%
Area Digital Total	0.24 mm² 4 mm²
Power FETs	On-chip
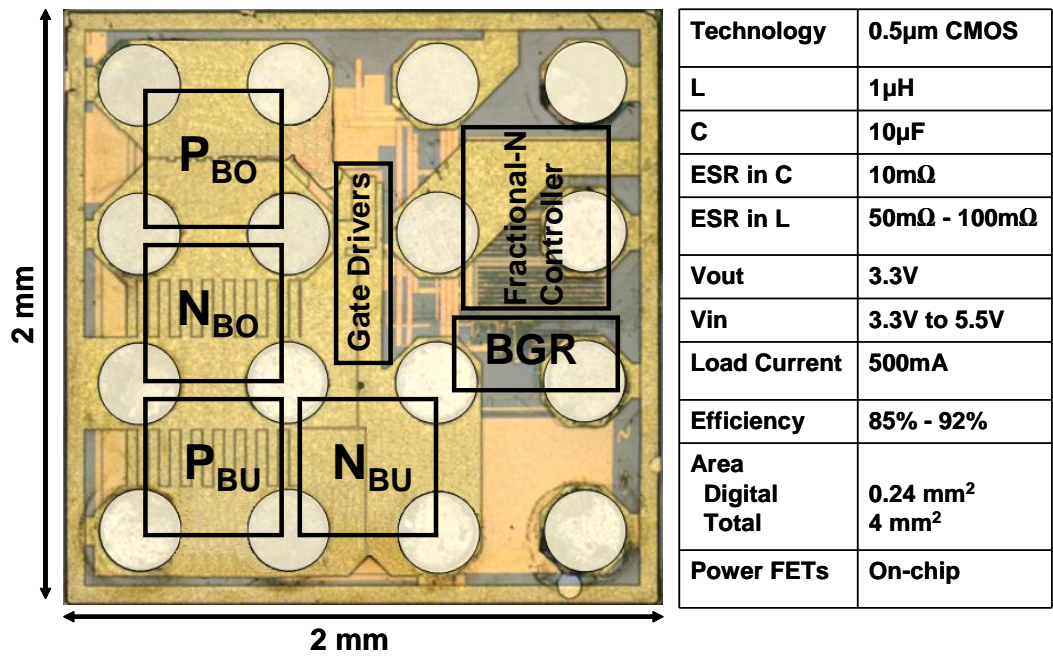
Figure 3.14: Die photo of the proposed digital buck-boost converter
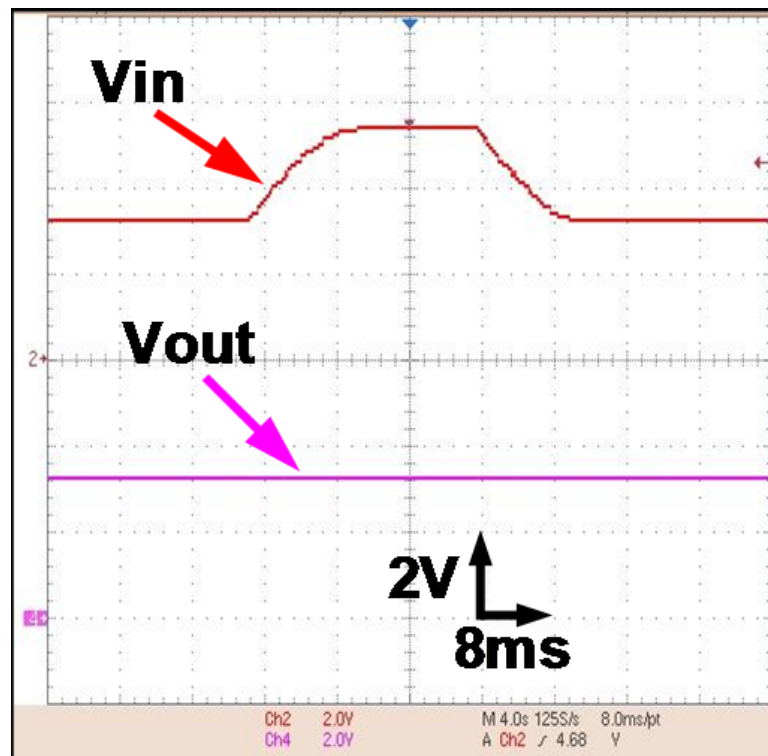
Figure 3.15: Measured V_{IN} versus V_{OUT}
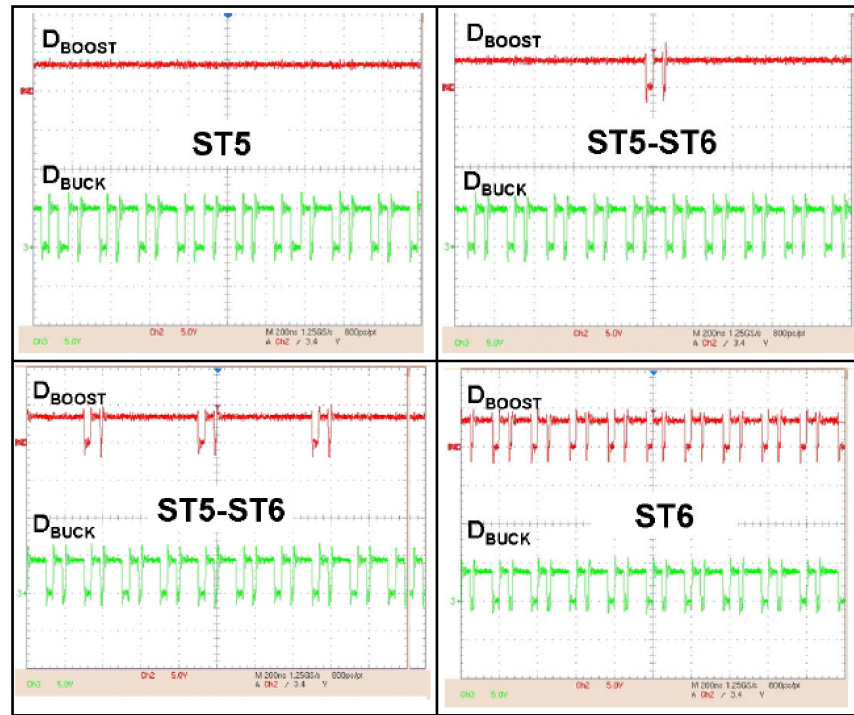
Figure 3.16: Measured switching profile in different operating states
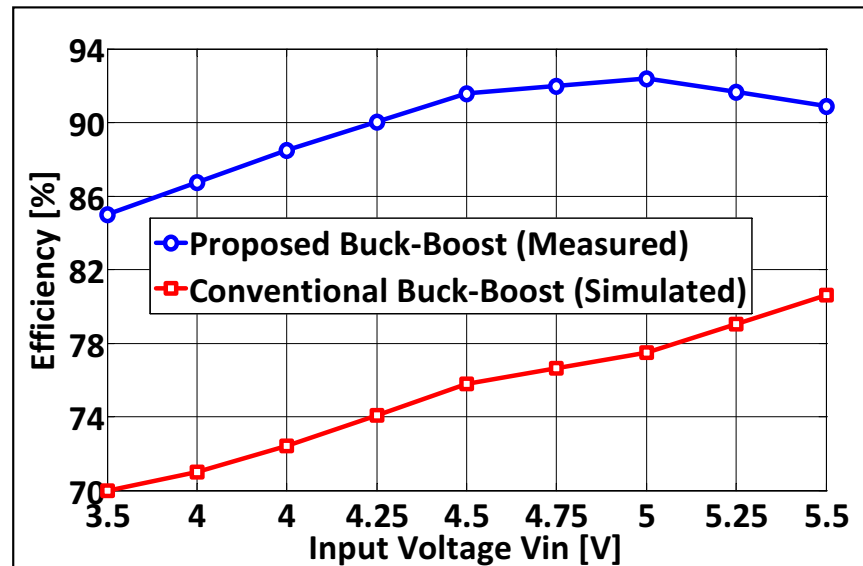
Figure 3.17: Measured efficiency versus input voltage

CHAPTER 4. FIXED FREQUENCY HYBRID VOLTAGE AND CURRENT MODE HYSTERETIC BUCK CONVERTER

This chapter discusses the design of a hybrid voltage and current-mode hysteretic control which overcomes the issues associated with conventional hysyteretic converters such as wide frequency variation, large output ripple and poor voltage regulation. The chapter is organized as follows. Sections 4.1 and 4.2 give an introduction to voltage and current mode hysteretic dc-dc converters and discuss their advantages and drawbacks. The proposed hybrid hysteretic control is discussed in Section 4.3 along with its design details. The chapter is concluded with the measurement results discussed in Section 4.4.

4.1 A Voltage mode Hysteretic DC-DC Converter

Fig. 4.1 shows the simplified circuit of a conventional voltage mode hysteretic dc-dc converter [21]. The main advantage of the converter is its simplicity as it requires only a comparator in the feedback control and no additional compensation circuit is needed. The ability to respond faster (because of no sampling and compensation loop delays) to a load transient makes the converter an attractive choice over PWM based converters for applications that require stringent transient response such as powering microprocessors, solid state driver and RF power amplifiers. The output voltage of a hysteretic converter is regulated in the same manner as of PWM converter by changing the ON time (duty cycle) of the switching clock

and expressed as:

$$V_O = DV_{IN} \qquad (4.1)$$

where D is the duty cycle.
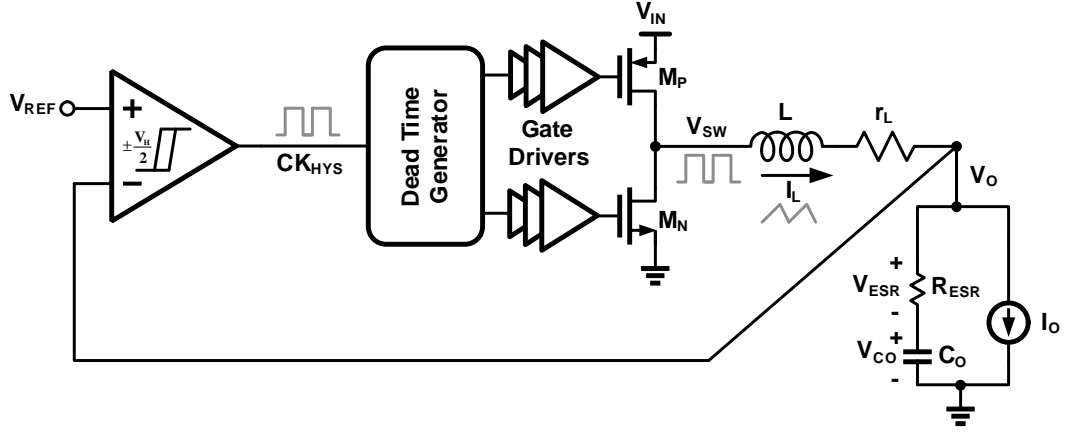
Figure 4.1: A voltage mode hysteretic converter.

The switching behavior of the hysteretic converter is shown in Fig. 4.2. Unlike a PWM based converter which uses a fixed frequency switching clock, a hysteretic converter does not require any clock. A closer look at Fig. 4.1 indicates that a hysteretic converter resembles an RC relaxation oscillator where RC filter is replaced by an LC filter. Since it relies on self oscillation, the switching frequency depends on various circuit parameters and given by[25]

$$F_{SW} = \frac{V_{IN}D(1-D)R_{ESR}}{\Delta V_H L} \qquad (4.2)$$

where L is the inductor value, R_{ESR} is the equivalent series resistance of the output capacitor, C_O, and ΔV_H is the hysteresis of the comparator.
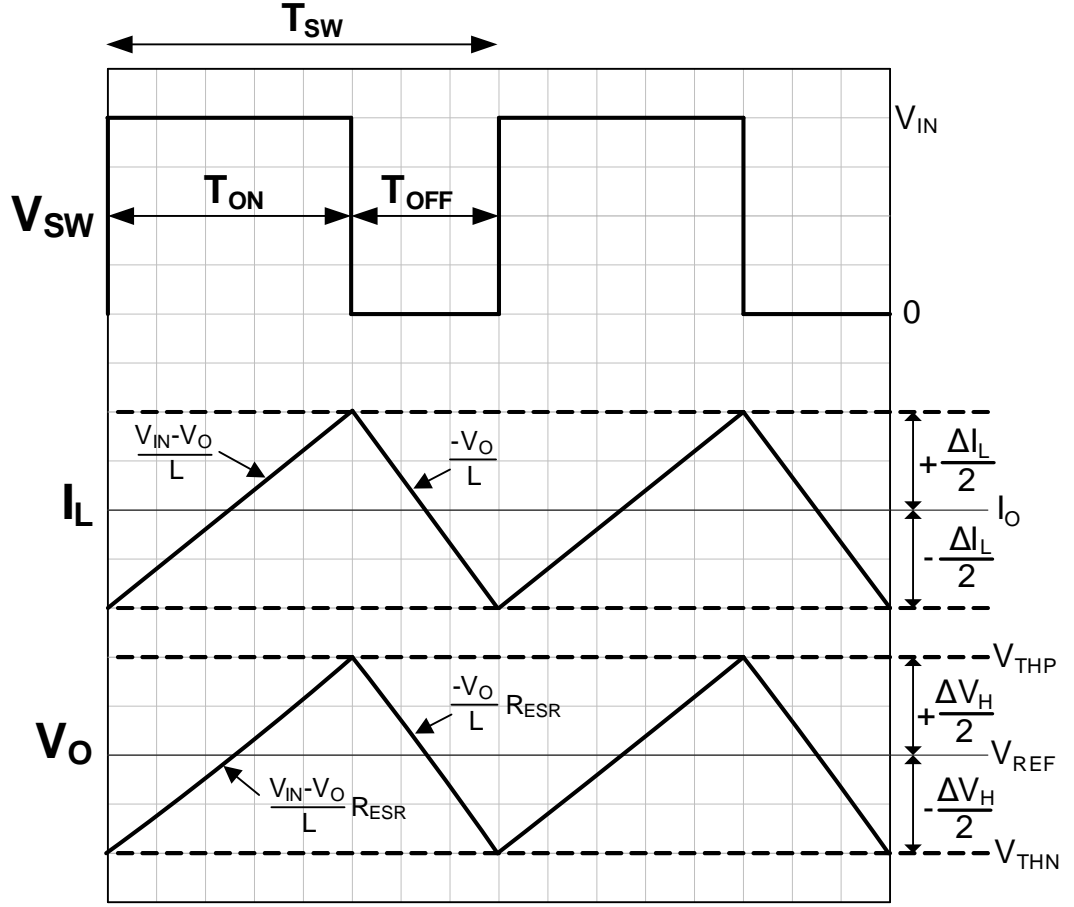
Figure 4.2: Switching behavior of a hysteretic converter.

4.1.1 Stability of a Hysteretic DC-DC Switching Converter

Since operation of a hysteretic converter strongly relies on the output ripple (sometimes also called ripple converter), it becomes important to analyze the ripple and how different circuit parameters affect its behavior. Referring again to Fig. 4.1, the output voltage consists of two components: capacitor voltage, V_{CO} and ESR voltage V_{ESR} as shown in Fig. 4.3. If ΔV_{CO} is the capacitor ripple voltage then,

output voltage ripple can be expressed as:

$$\Delta V_{OV}(t) = V_{ESR}(t) + \Delta V_{CO}(t) \tag{4.3}$$

Voltage across ESR is given by

$$V_{ESR}(t) = \Delta I_L(t) R_{ESR} \tag{4.4}$$

$I_L(t)$ is the inductor ripple current given by

$$\Delta I_L(t) = \Delta I_L(0) + \frac{V_L}{L} t \tag{4.5}$$

where $\frac{V_L}{L}$ is the inductor current slope ($V_L = V_{IN} - V_O$ during T_{ON} and $V_L = -V_O$ during T_{OFF}). Substituting eq. 4.5 in eq. 4.4, we get

$$V_{ESR}(t) = \left(\Delta I_L(0) + \frac{V_L}{L} t \right) R_{ESR} \tag{4.6}$$

The capacitor ripple voltage can be expressed as:

$$\Delta V_{CO}(t) = \frac{1}{C_O} \int \left(\Delta I_L(0) + \frac{V_L}{L} t \right) dt \tag{4.7}$$

Substituting eq. 4.7, after integrating, and eq. 4.6 into eq. 4.3, we get

$$\Delta V_O(t) = \Delta I_L(0) R_{ESR} + \left(\frac{V_L}{L} R_{ESR} + \frac{\Delta I_L(0)}{C_O} \right) t + \frac{1}{2} \frac{V_L}{LC_O} t^2 \tag{4.8}$$

which is the expression for output ripple voltage in the presence of ESR. The condition for ripple peak/valley can be obtained by differentiating eq. 4.8 w.r.t. time and equating to 0, which gives

$$t_{peak,valley} = -\frac{\Delta I_L(0)}{V_L} L - R_{ESR} C_O \tag{4.9}$$

where t_{peak} and t_{valley} are measured with reference to falling and rising edge of the PWM signal, respectively.
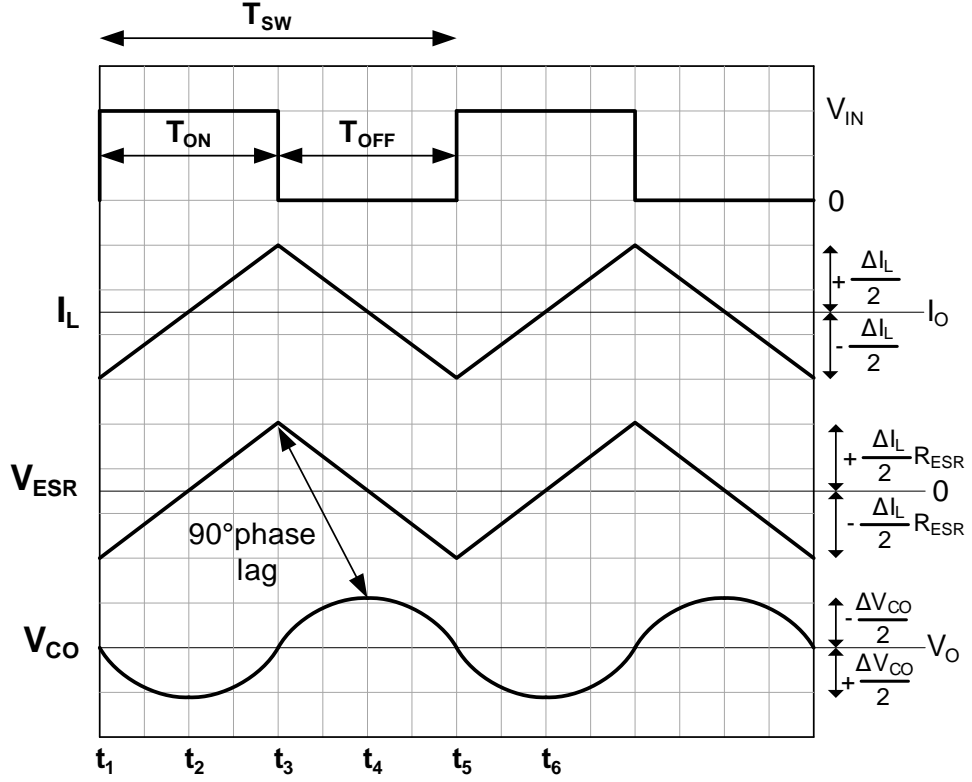
Figure 4.3: Ripple of a hysteretic converter.

Since ripple peak will occur during T_{OFF} (due to phase lag) and $V_L = -V_O$, $\Delta I_L(0) = \frac{1}{2}\frac{V_O}{L}T_{OFF}$ during OFF time, eq. 4.9 can be re-written for peak as:

$$t_{peak} = \frac{1}{2}T_{OFF} - R_{ESR}C_O \qquad (4.10)$$

Similarly ripple valley will occur during T_{ON} and $V_L = V_{IN} - V_O$, $\Delta I_L(0) = \frac{1}{2}\frac{V_{IN}-V_O}{L}T_{ON}$ during ON time, eq. 4.9 can be re-written for valley as:

$$t_{valley} = \frac{1}{2}T_{ON} - R_{ESR}C_O \qquad (4.11)$$

In order to bound the output ripple between hysteresis window, both t_{peak} and t_{valley} should be zero i.e. t=0 in eq. 4.8 will make the ripple voltage same as voltage across ESR which is in-phase with the inductor ripple current and bound

it within the hysteresis window (assuming no delay in the comparator). From eq. 4.10, the condition for stable operation during T_{ON} i.e. $t_{peak} = 0$ will be

$$\frac{1}{2}T_{OFF} \leq R_{ESR}C_O \quad \text{or} \quad \frac{1}{2}(1-D)T_{SW} \leq R_{ESR}C_O \qquad (4.12)$$

and from eq. 4.11, the condition for stable operation during T_{OFF} i.e. $t_{valley} = 0$ will be

$$\frac{1}{2}T_{ON} \leq R_{ESR}C_O \quad \text{or} \quad \frac{1}{2}DT_{SW} \leq R_{ESR}C_O \qquad (4.13)$$

It is observed from eq. 4.12 and eq. 4.13 that the RC time constant should be more than half of the ON or OFF time for stable operation[23]. If this condition is not met then ripple will no longer be bounded between the hysteresis window and the converter becomes uncontrollable. It should also be noticed that if these conditions are satisfied only for $D = 0.5$ then no peaks are observed for higher duty cycle but it causes a valley in the output and vice versa for the lower duty cycle as shown in Fig. 4.4. The converter under such condition behaves like a single bound hysteretic converter and introduces dc error in the output voltage. Therefore ideal condition for stable operation across entire range of duty cycle ($D = 0$ to $D = 1$) is

$$\frac{1}{2}T_{sw} \leq R_{ESR}C_O \qquad (4.14)$$

Equation 4.14 shows that either a large ESR or large output capacitor is required for stable operation of a hysteretic converter. For instance, if the converter is designed to operate at switching frequency of $1MHz$ with $C_O = 10\mu F$, the required ESR would be $50m\Omega$. Even though large ESR ensures stability, it drastically affects the transient response as discussed next.
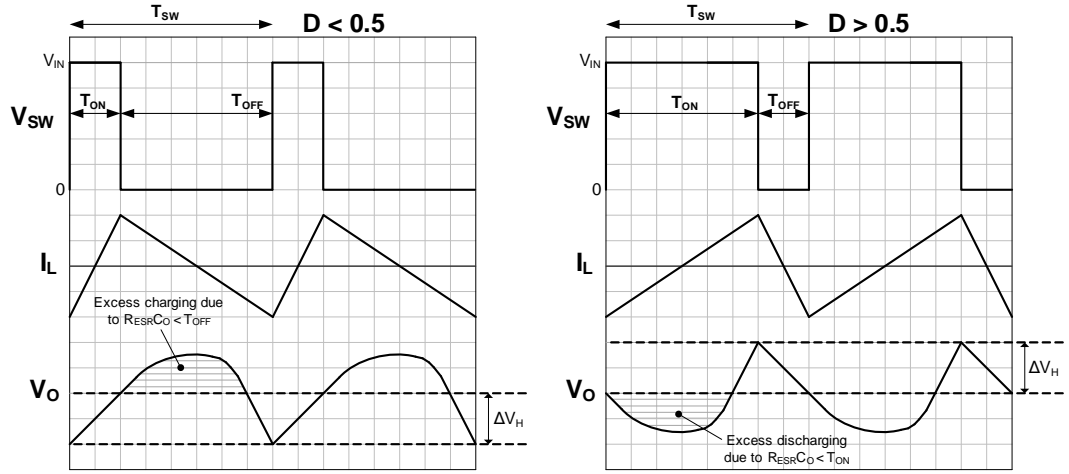
Figure 4.4: Offset in the output ripple due to lower $R_{ESR}C_O$.

4.1.2 Transient Response of a Hysteretic DC-DC Switching Converter

In order to understand the transient behavior of a hysteretic converter, lets first analyze the transient response of an ideal switching converter and then see how it gets affected by various circuit parameters of a hysteretic converter. Fig. 4.5 shows the load transient response of an ideal converter [24] depicting the behavior of output voltage, V_O and inductor current, I_L under a sudden change in the output load current, I_O. Suppose that the output voltage is initially regulated at V_{REF} and current load step of ΔI_O is applied at $t = t_1$. Since we have assumed an ideal converter, it responds quickly to the perturbation applied at the output and keeps the switch M_P ON until the output voltage is recovered. Due to the slow rate of change of inductor current, the extra current due to change in load is drawn from the output capacitor C_O between the time duration $t_1 - t_2$ until the inductor current reaches to the final value of I_O i.e. I_{O2}. This slow rate of

change in the inductor current causes an undershoot V_{UV} in the output voltage whose value depends upon the size of the capacitor and how quickly the inductor current is recovered, therefore it is a function of inductor current slope. If V_{IN} is the input voltage and L is the inductor value then change in the inductor current is given by
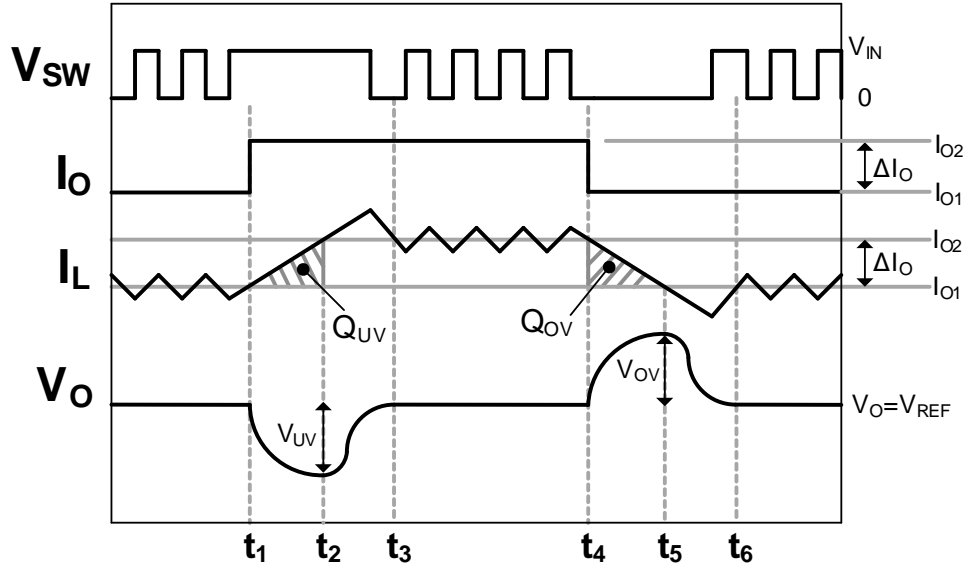
Figure 4.5: Transient response of an ideal buck dc-dc converter.

$$\Delta I_O = \frac{V_{IN} - V_O}{L} \Delta t \qquad \text{where } \Delta t = t_2 - t_1 \qquad (4.15)$$

$$\text{or} \qquad \Delta t = \frac{\Delta I_O}{V_{IN} - V_O} L \qquad (4.16)$$

The average charge, Q_{UV} stored in the inductor between $t_1 - t_2$ is given by area under the triangle as:

$$Q_{UV} = -\frac{1}{2} \Delta t \Delta I_O \qquad (4.17)$$

Substituting Δt from eq. 4.16, we get

$$Q_{UV} = -\frac{1}{2}\frac{\Delta I_O{}^2}{V_{IN} - V_O}L \tag{4.18}$$

Since charge stored in the inductor should be transferred to capacitor C_O, the change in voltage across C_O will be

$$V_{UV} = \frac{Q_{UV}}{C_O} = -\frac{1}{2}\frac{\Delta I_O{}^2}{V_{IN} - V_O}\frac{L}{C_O} \tag{4.19}$$

It could be observed from the above expression that the transient response of an ideal converter is mainly limited by the inductor slew rate and output capacitor. For large inductor values, increasing bandwidth of the control loop beyond some point may not lead to any improvement in the transient response. The transient response can be optimized by keeping inductor to capacitor ratio fixed i.e. for large values of inductors, the output capacitor should be increased proportionally. The transient response could also be improved by maintaining a lower slew rate in the load current. For instance, if the load current is changed at the same rate of inductor current or slower, the output voltage will not experience any undershoot/overshoot as shown in Fig. 4.6. It could also be noticed that the undershoot is a square function of load current i.e. if step in load current is reduced by half, it reduces the overshoot by four times or vice versa. The large voltage across the inductor, $(V_{IN} - V_O)$, also improves undershoot as it increases the inductor current slew rate. Since for a fixed output voltage, duty cycle is inversely proportional to V_{IN}, it could be noticed that the output voltage experiences less undershoot at lower duty cycle as compared to higher duty cycle. A similar expression can be derived during negative load transient applied at the time, t_4 (Fig. 4.5), the overshoot voltage, V_{OV} is given by

$$V_{OV} = \frac{Q_{OV}}{C_O} = \frac{1}{2}\frac{\Delta I_O{}^2}{V_O}\frac{L}{C_O} \tag{4.20}$$
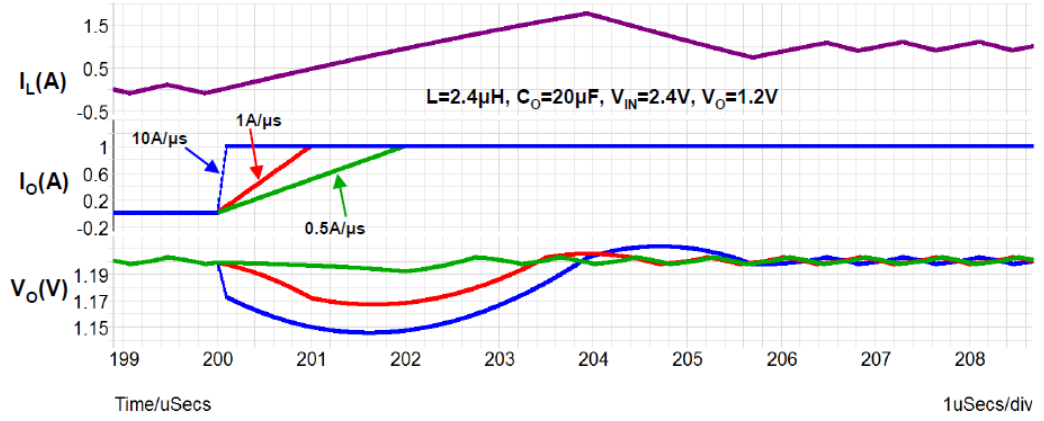
Figure 4.6: Effect of load current slew rate (dI_O/dt) on transient response of a dc-dc converter.

The relationship between V_{UV} and V_{OV} in terms of duty cycle can be determined by dividing (4.19) by (4.20)

$$\frac{V_{UV}}{V_{OV}} = \frac{V_O}{V_{IN} - V_O} = \frac{D}{1-D} \qquad (4.21)$$

which shows that undershoot and overshoot voltages are same at $D = 0.5$ while different at other duty cycles.

Theoretically, a hysteretic converter is considered to be fastest and more closer to an ideal converter exhibiting a good transient response but in reality, it is hampered by the large ESR (as it is required for stable operation discussed in previous section) and circuit non-idealities such as comparator delay, switch turn ON/OFF delay and hysteresis. Let us first analyze the effect of ESR on transient response. Considering the hysteretic converter shown in Fig. 4.1, the transient response with ESR is shown in Fig. 4.7 [24].

The load step ΔI_O is applied at time t_1 causes a sudden voltage drop across the ESR i.e. $V_{ESR} = \Delta I_O R_{ESR}$. The comparator turns the switch M_P ON and
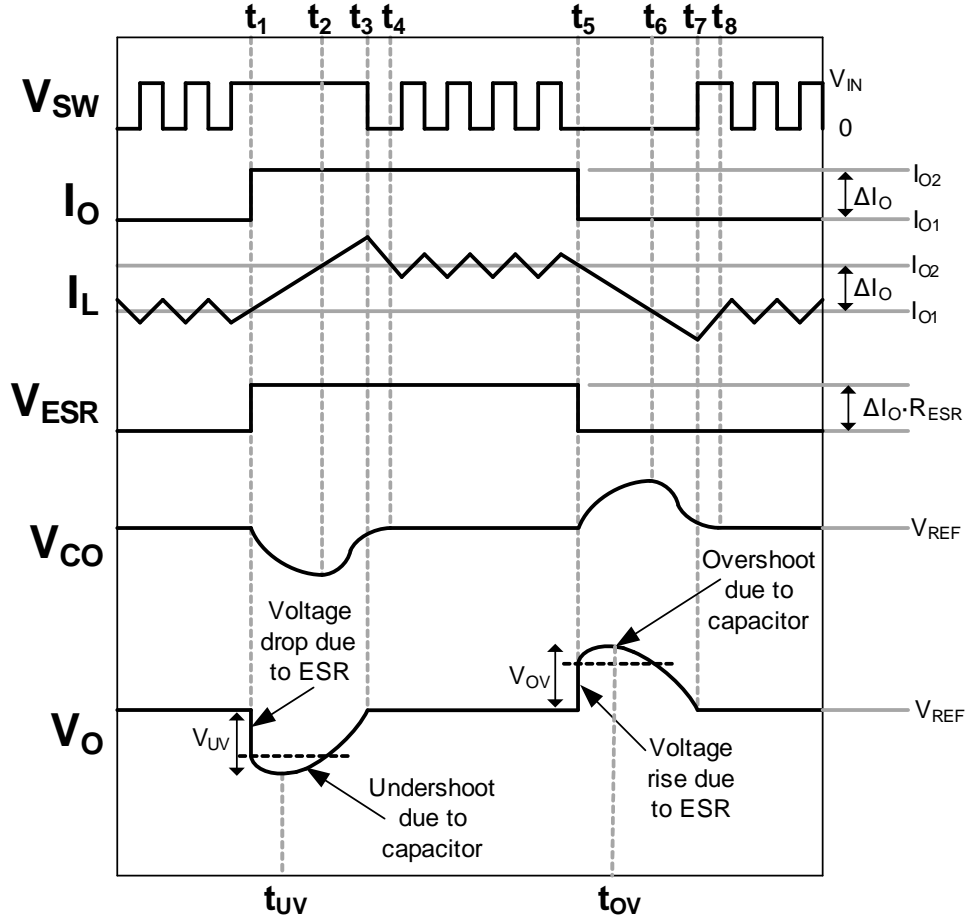
Figure 4.7: Effect of ESR on transient response of an ideal dc-dc buck converter.

inductor current, I_L starts rising. The capacitor voltage, V_{CO} starts dropping until it hits the bottom at time t_2 before inductor current rises to the final value of I_O. The expression for change in output voltage ΔV_O can be derived as follows:

$$\Delta V_O(t) = \left(-\Delta I_O + \frac{V_{IN} - V_O}{L}t \right) R_{ESR} + \frac{1}{C_O} \int \left(-\Delta I_O + \frac{V_{IN} - V_O}{L}t \right) dt \quad (4.22)$$

which after integrating and re-arranging becomes:

$$\Delta V_O(t) = -\Delta I_O R_{ESR} + \left(\frac{V_{IN} - V_O}{L} R_{ESR} - \frac{\Delta I_O}{C_O}\right)t + \frac{1}{2C_O}\frac{V_{IN} - V_O}{L}t^2 \quad (4.23)$$

The time $t = t_{UV}$ at which undershoot, V_{UV} occurs can be found by differentiating $\Delta V_O(t)$ and equating to 0 which gives

$$t_{UV} = \frac{\Delta I_O}{V_{IN} - V_O}L - R_{ESR}C_O \quad (4.24)$$

and the value of undershoot voltage, V_{UV} can be determined by substituting t_{UV} in eq. 4.23 as:

$$V_{UV} = -\frac{1}{2}\frac{\Delta I_O{}^2}{V_{IN} - V_O}\frac{L}{C_O} - \frac{1}{2}(V_{IN} - V_O)R_{ESR}^2\frac{C_O}{L} \quad (4.25)$$

which shows that the undershoot with ESR increases by a factor of $(V_{IN} - V_O)R_{ESR}^2\frac{C_O}{L}$ as compared to no ESR derived in eq. 4.19 but it appears earlier in time and settles faster (due to reduced phase lag) as shown in Fig. 4.7.

From eq. 4.24, if $R_{ESR}C_O \geq \frac{\Delta I_O}{V_{IN}-V_O}L$ then t_{UV} becomes zero or negative and maximum undershoot from eq. 4.23 (by substituting $t = 0$) is simply $-\Delta I_O R_{ESR}$. In that case, C_O has negligible or no effect on undershoot and settling. However, if $R_{ESR}C_O$ is smaller than $\frac{1}{2}\frac{\Delta I_O}{V_{IN}-V_O}L$ then the transient response exhibits ringing and degrades the settling. The simulated transient response for different $R_{ESR}C_O$ time constant is shown in Fig. 4.8 which indicates degradation in settling and undershoot with reduced $R_{ESR}C_O$.

Expression for maximum overshoot during negative transient can also be derived in similar manner and given by

$$V_{OV} = \frac{1}{2}\frac{\Delta I_O{}^2}{V_O}\frac{L}{C_O} + \frac{1}{2}V_O R_{ESR}^2\frac{C_O}{L} \quad (4.26)$$

and time at which overshoot occurs is

$$t_{OV} = \frac{\Delta I_O}{V_O}L - R_{ESR}C_O \quad (4.27)$$
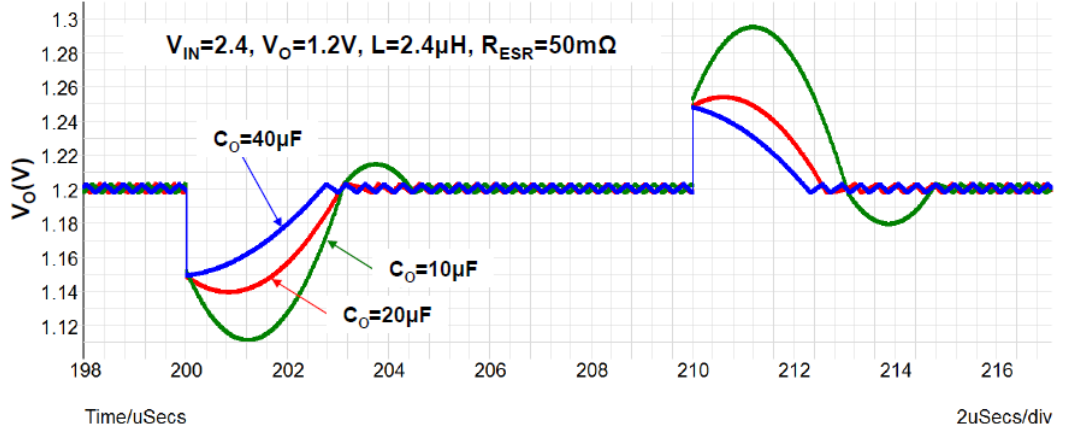
Figure 4.8: Transient response showing degradation with reduced $R_{ESR}C_O$ time constant.

4.1.3 Effect of Loop Delay on Switching Frequency and Voltage Regulation

The expression for switching frequency, F_{SW}, in eq. 4.2 assumes that there is no loop delay in the converter but in reality, there is some finite delay associated with the comparator and switches. In presence of loop delay is (t_d), the switching behavior becomes slightly different from the one shown in Fig. 4.2 and output voltage charges and discharges for a slightly longer time during T_{ON} and T_{OFF}, respectively, as shown in Fig. 4.9 [22]. This extra charging/discharging causes the ripple voltage to go out of the hysteresis window. If ΔV_{ep} and ΔV_{en} are errors in the ripple voltage due to t_d during ON and OFF time, respectively which can be expressed as:

$$\Delta V_{ep} = \frac{V_{IN} - V_O}{L} t_d R_{ESR} \tag{4.28}$$

and
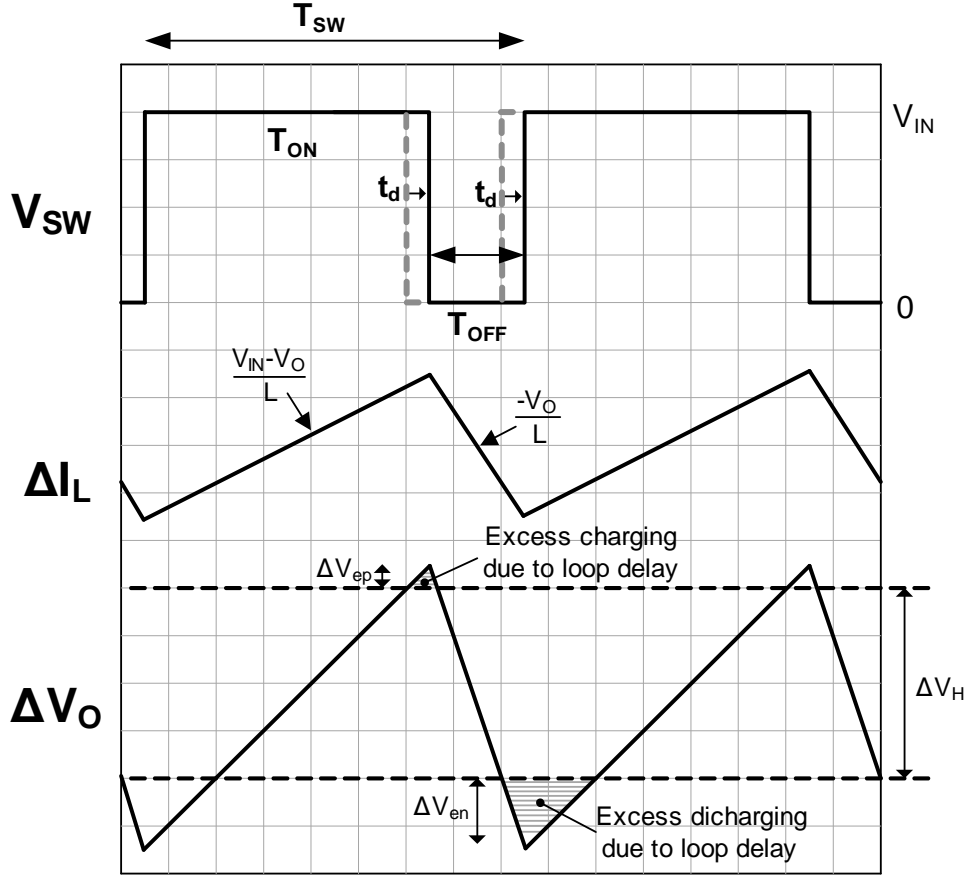
Figure 4.9: Offset in the output ripple due to loop delay.

$$\Delta V_{en} = -\frac{V_O}{L} t_d R_{ESR} \qquad (4.29)$$

then pk-pk ripple voltage during T_{ON} is given by

$$\Delta V_H + \Delta V_{ep} - \Delta V_{en} = \frac{V_{IN} - V_O}{L} T_{ON} R_{ESR} \qquad (4.30)$$

Substituting ΔV_{ep} and ΔV_{en} from eq. 4.28 and eq. 4.29, we get

$$\Delta V_H + \frac{V_{IN} - V_O}{L} t_d R_{ESR} + \frac{V_O}{L} t_d R_{ESR} = \frac{V_{IN} - V_O}{L} T_{ON} R_{ESR} \qquad (4.31)$$

After solving for T_{ON}

$$T_{ON} = \frac{\Delta V_H L + V_{IN} t_d R_{ESR}}{(V_{IN} - V_O) R_{ESR}} \tag{4.32}$$

Since $T_{ON} = DT_{SW} = \frac{D}{F_S W}$ and $D = \frac{V_O}{V_{IN}}$, we can write above equation as

$$F_{SW} = \frac{V_{IN} D(1-D) R_{ESR}}{\Delta V_H L + V_{IN} t_d R_{ESR}} \tag{4.33}$$

which is the expression for switching frequency of a hysteretic converter in presence of loop delay, t_d. From eq. 4.28 and eq. 4.29, offset in the output ripple voltage can be calculated as

$$V_{os} = \frac{\Delta V_{ep} + \Delta V_{en}}{2} = \frac{V_{IN}(1-2D) R_{ESR}}{L} t_d \tag{4.34}$$

which shows that t_d causes an offset in the output voltage and degrades the voltage regulation. This offset is zero at $D = 0.5$ and maximum at extreme duty cycles (negative when $D > 0.5$ and positive when $D < 0.5$).

From analysis in this section, we may conclude that the voltage mode hysteretic converter shown in Fig. 4.1, despite having good transient response, suffers from three major drawbacks: (1) requires a large ESR, (2) has a dc voltage offset, and (3) exhibits wide variation in switching frequency. The requirement for large ESR makes it difficult to design a voltage mode hysteretic converter with low output ripple thus making the converter unsuitable for noise sensitive applications such as RF and audio. The wide variation in switching frequency also causes electro-magnetic interference (EMI). The problem of dc offset is mostly design dependent and could be reduced by ensuring minimum delay in the comparator and switches.

Owing to these drawbacks, a voltage mode hysteretic converters have not been able to overpower the noise performance of a fixed frequency PWM converters

irrespective of the fact that they offer a low cost alternative with better transient response. There have been some improvements overcoming these issues and leading to the design of an improved hysteretic converter, known as current mode hysteretic converter [26], [28] as discussed in the following section.

4.2   Current Mode Hysteretic Converter

A current mode hysteretic converter is shown in Fig. 4.10. Unlike a voltage mode hysteretic converter which relies on output voltage ripple, the ripple in current mode hysteretic control is generated internally through an RC low-pass filter consisting of R_F and C_F. A closer look at the circuit indicates that it forms an RC relaxation oscillator with LC filter at its output, V_{SW}. If RC time constant of the $R_F C_F$ filter is large enough then it actually emulates the inductor ripple current by integrating the switching signal V_{SW}. This technique has two main advantages: (1) it is independent of the output ripple hence can be operated with low ESR, and (2) the switching frequency is independent of ESR and inductor. The switching behavior of a current mode hysteretic converter is shown in Fig. 4.11.
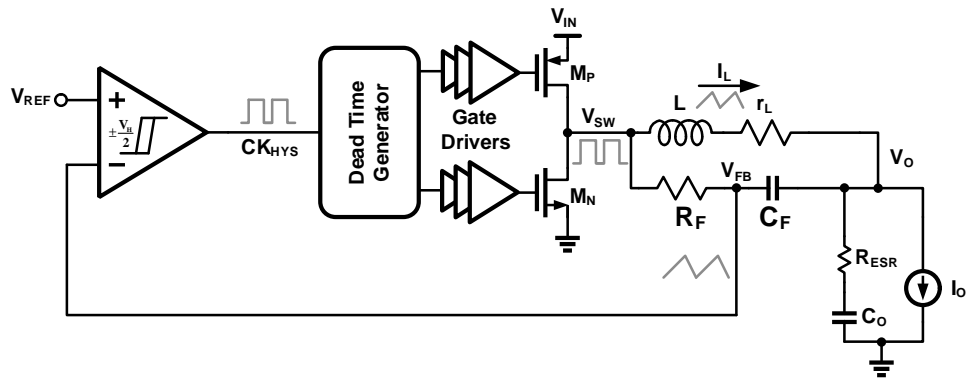
Figure 4.10: A current mode hysteretic dc-dc converter.
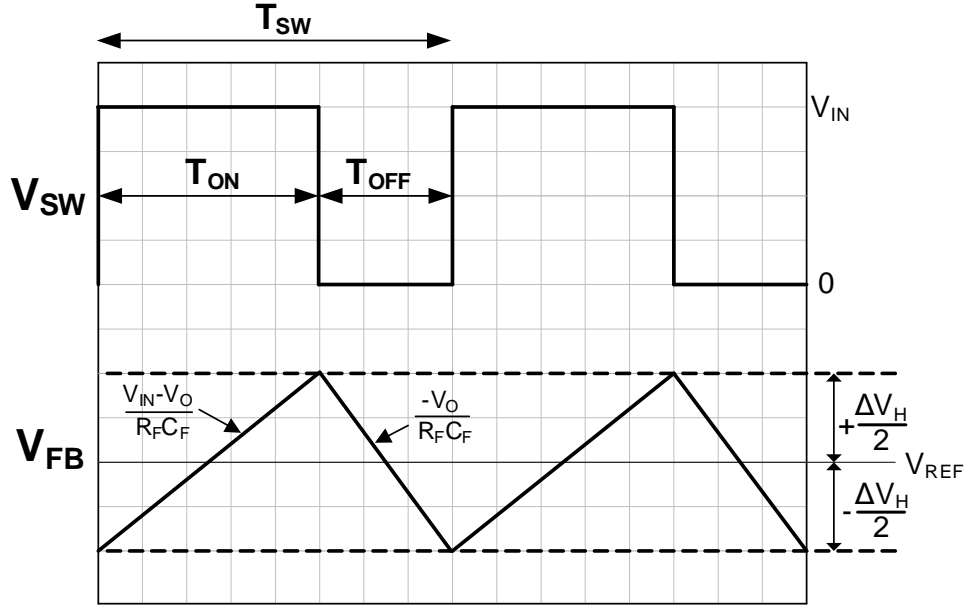
Figure 4.11: Switching behavior of a current mode hysteretic converter.

If V_{FB} is regulated at a dc voltage of V_{REF}, the rising and falling slopes of the ripple at V_{FB} can be expressed as $\frac{V_{IN}-V_{REF}}{R_F C_F}$ and $-\frac{V_{REF}}{R_F C_F}$ respectively. Since ripple voltage is bounded between hysteresis window ΔV_H, we can express

$$\Delta V_H = -\frac{V_{IN} - V_{REF}}{R_F C_F} T_{ON} \tag{4.35}$$

which can be solved for F_{SW}, giving

$$F_{SW} = \frac{V_{IN} D(1 - D)}{\Delta V_H R_F C_F} \quad \text{(considering } D = \frac{V_{REF}}{V_{IN}}) \tag{4.36}$$

and in presence of the loop delay, t_d, the switching frequency is given by

$$F_{SW} = \frac{V_{IN} D(1 - D)}{\Delta V_H R_F C_F + V_{IN} t_d} \tag{4.37}$$

Comparing with the switching frequency of a voltage mode hysteretic converter in eq. 4.2, the switching frequency of a current mode hysteretic converter

is only a function of input voltage, V_{IN} and duty cycle, D assuming that ΔV_H is fixed and $R_F C_F$ has small variations. Hence for a fixed V_{IN} and V_O, we can choose ΔV_H and $R_F C_F$ to make it operate at a fixed switching frequency across varying L and R_{ESR}. This is the major advantage of a current mode over voltage mode hysteretic control. Another advantage is the flexibility in choosing larger ΔV_H independent of the output ripple voltage thus making the converter less sensitive to noise. However, the current mode hysteretic converter has a drawback when operated at higher load current. Since there is no direct feedback from output, V_O and it regulates the output of $R_F C_F$, which senses only ac component of V_O through C_F, it suffers from poor load regulation due to inductor dc resistance(DCR), r_L as shown in Fig. 4.12 . For instance, if the inductor DCR is $50 m\Omega$ and output load current, I_O is $1A$, the output will have a dc error of $I_O r_L = 50 mV$. Hence it never settles back to the original voltage level when a load step is applied as it is shown in Fig. 4.13. Therefore a conventional current mode hysteretic converter is suited only for low current applications or in high voltage applications where $50 mV - 100 mV$ error in the output is a small percentage of the regulated voltage. It is also not suited for applications with varying V_{IN} or V_O as its switching frequency is a function of duty cycle.

The error in output voltage due inductor DCR could be corrected by adding an integrator in the feedback and using the integrated dc error as reference to the hysteretic comparator [30]-[31]. Even though this technique is effective and achieves good regulation, it requires an error amplifier and large capacitor which not only increases the overall chip area but also increases the quiescent current of the converter.

In view of this, we seek to resolve the aforesaid drawbacks of a conventional hysteretic converter by proposing a hybrid voltage and current mode hysteretic
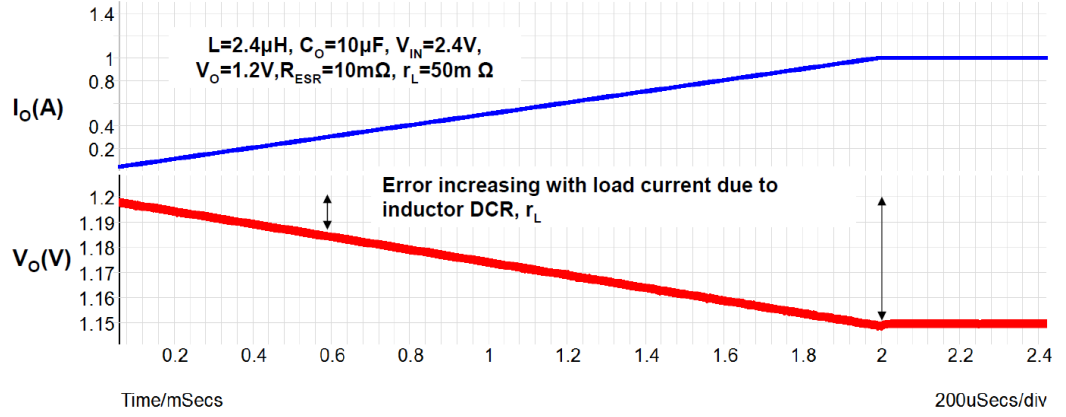
Figure 4.12: Simulated output of a current mode hysteretic converter under varying current showing poor load regulation.
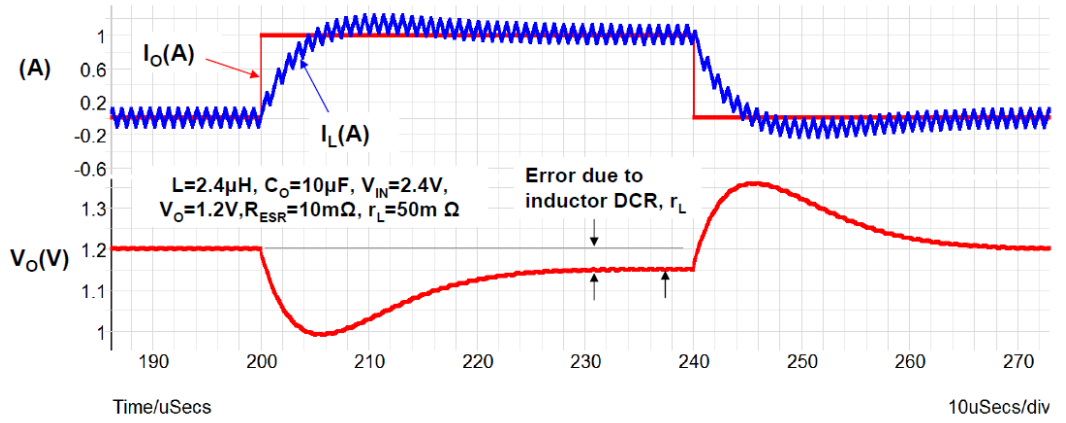
Figure 4.13: Simulated transient response of a current mode hysteretic converter showing effect of inductor DCR.

control [32] to accurately regulate the output voltage with a constant switching frequency across varying output voltage, V_O, inductor, L and output load current, I_O. Unlike the previously proposed fixed frequency hysteretic converters [27] which relies strongly on output ripple (requires large ESR) and [28] that suffers from output inaccuracy, the proposed control technique decouples the trade-off between the requirement of low ripple and high accuracy as discussed in the forthcoming

sections.

4.3 Proposed Fixed Frequency Hybrid Voltage and Current Mode Hysteretic Converter

The block diagram of the proposed hysteretic buck converter is shown in Fig. 4.14. It consists of a voltage regulation loop (VRL), frequency regulation loop (FRL) and an RC current sensor. In the VRL, a hysteretic slicer compares the feedback voltage, V_{FB}, with a reference voltage, V_{REF}, and drives the output DC voltage to the desired value much like a conventional voltage-mode hysteretic converter. The RC network consisting of resistors, R_P, R_I and capacitor, C_F low-pass filters the switching node voltage, V_{SW}, and generates an internal ramp voltage, V_{RAMP}. The RC time constant sets the slope of V_{RAMP} and determines F_{SW}. The switching frequency of the converter is expressed by the same expression as in eq. 4.36. The FRL compares the switching frequency F_{SW} with a desired reference frequency, F_{REF}, and tunes resistors R_P and R_I to achieve $F_{SW} = F_{REF}$. By ac-coupling V_{RAMP} onto the sensed output voltage, βV_O, using a small on-chip capacitor, C_C, the proposed architecture precisely regulates both V_O and F_{SW} independently without affecting the output voltage ripple. The design details of the voltage and frequency regulation loops are discussed in the following sections.

4.3.1 Design of Voltage Regulation Loop (VRL)

As shown in Fig. 4.15, the voltage regulation loop consists of a reference generator and pre-amplifier (pre-amp) followed by a zero-crossing comparator (ZXC). The reference generator outputs two threshold voltages V_{THP} and V_{THN} such that
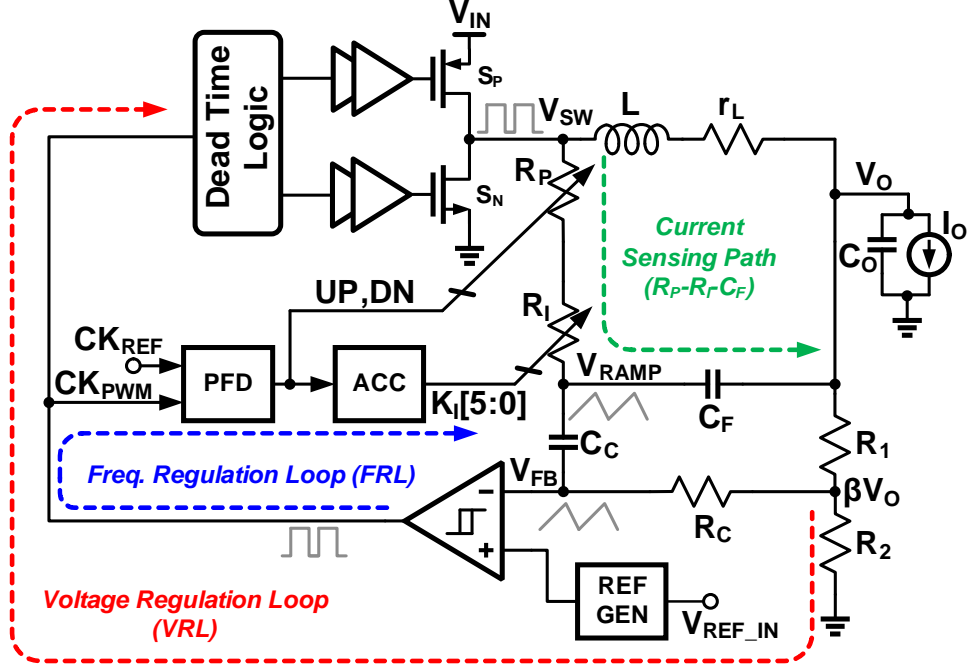
Figure 4.14: Architecture diagram of the proposed hysteretic dc-dc converter.

the difference between them is equal to the hysteresis window, ΔV_H and average is V_{REF}. These two threshold voltages are selected alternatively during ON and OFF times of the comparator output which is a pulse width modulated signal, CK_{PWM}. The sensed output node, βV_O is regulated by bounding V_{FB} between the hysteresis window which is centered at V_{REF}. The pre-amp is purposely used to relax the offset requirement of ZXC so that smaller device sizes could be used to reduce the propagation delay (since large t_d causes dc error in the output as discussed earlier). The pre-amp shown in Fig. 4.16 is designed to be low offset and high bandwidth with small differential gain ($\approx 20dB$). Since the dc component of V_{FB} is same as βV_O which is regulated at V_{REF}, the output voltage of the converter, V_O is given by
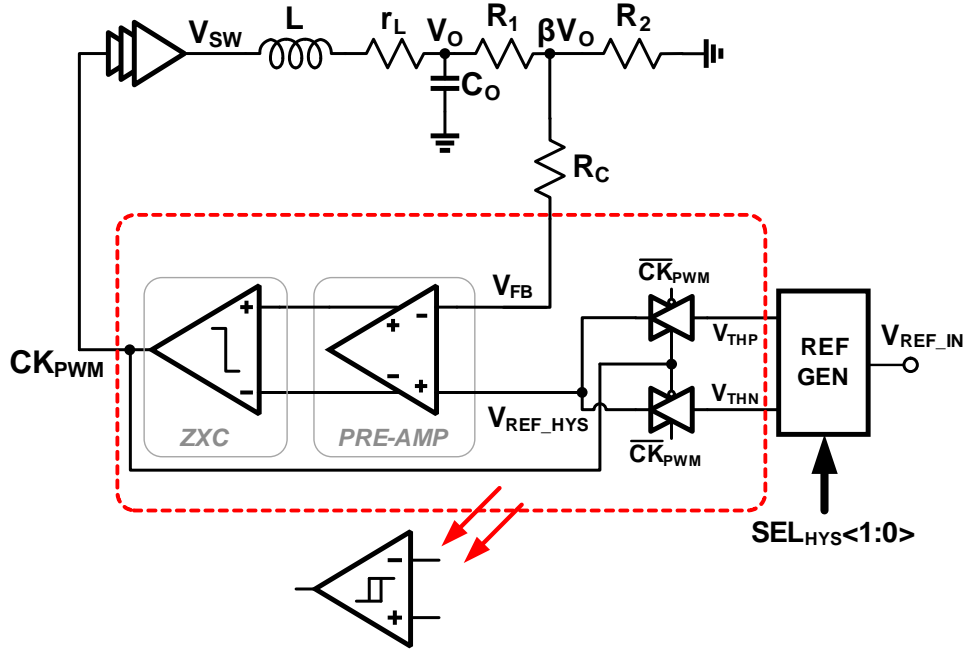
Figure 4.15: Circuit diagram of the voltage regulation loop (VRL).

$$V_O = \left(1 + \frac{R_1}{R_2}\right)V_{REF} \tag{4.38}$$

The hysteresis window was made to be programmable with 2-bit code, $SEL_{HYS} < 1:0 >$ just for testing purposes and it's not the requirement.

4.3.2 Design of Frequency Regulation Loop (FRL)

The block diagram of the FRL is shown in Fig. 4.17. The ramp generator consisting of R_P, R_I, and C_F along with the hysteretic comparator form a digitally-controlled relaxation oscillator (DRXO), whose frequency can be tuned by varying resistors R_P and R_I (which represent R_F of eq. 4.36. A bang-bang frequency-only detector implemented by re-sampling the UP/DN outputs of a 3-
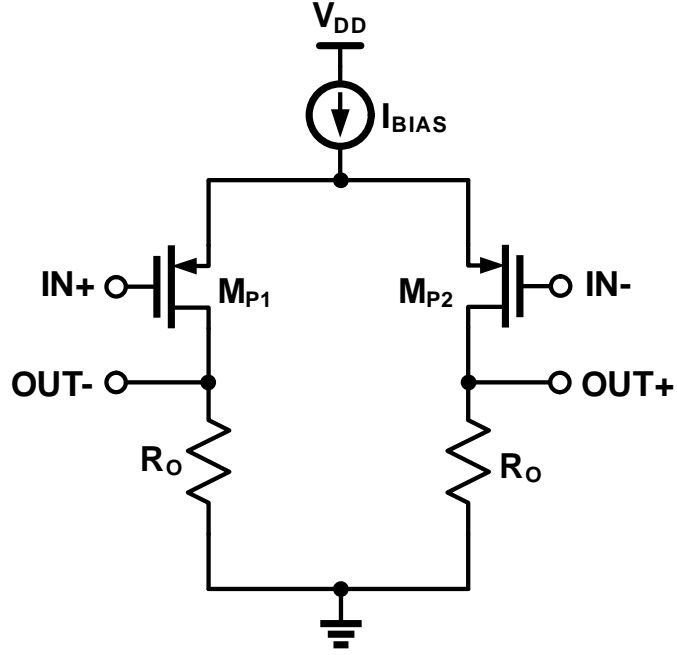
Figure 4.16: Circuit diagram of the pre-amplifier.

state phase detector measures the sign of the frequency error between F_{REF} and F_{SW}. The accumulator (ACC) integrates the error and drives DRXO towards frequency lock ($F_{REF} \approx F_{SW}$) by varying R_I which in turn controls the slope of ramp signal V_{RAMP}. Because of the bang-bang nature of frequency detector, the steady-state of the FRL loop is a bounded limit cycle which manifests as dithering of the switching frequency. To eliminate unpredictable spurious tones resulting from such dithering, a linear phase control is added, wherein UP/DN pulses vary the switching frequency by varying switched-resistor R_P. The linear proportional control also alleviates the resolution requirement of the digital frequency tuning control. Consequently, only 5-bit tuning of R_I is sufficient in the prototype to achieve near perfect frequency locking.

Figure 4.17: Circuit diagram of the frequency regulation loop (FRL).

4.4 Measured Results

The proposed hysteretic buck converter was implemented in a 130nm CMOS process and occupies an active area of $0.7mm^2$. Fig. 4.18 shows the die photo of the fabricated chip. Operating with an input voltage of $2.5V$, the converter regulates the output to any desired voltage in the range of $0.7V$ to $1.8V$. Measured performance of the proposed frequency regulation scheme is shown in Fig. 4.19. When the FRL is turned ON, F_{SW} varies by less than 0.5% over the entire output voltage range compared to 30% variation without the FRL. Fig. 4.20 shows the spectrum of CK_{PWM} with and without proportional path. When the proportional path was turned OFF, frequency spreading due to limit cycles is observed, but becomes a single $1MHz$ tone when proportional path is turned on, indicating no error in the switching frequency. The spectrum of the output voltage in Fig. 4.21 shows a ripple of $-43dBm$ at $1MHz$ and no other frequency tones were observed.

The behavior of ramp signal, V_{RAMP} with CK_{PWM} and CK_{REF} in Fig. 4.22 show that the ramp signal is bounded between the hysteresis window of $50mV$
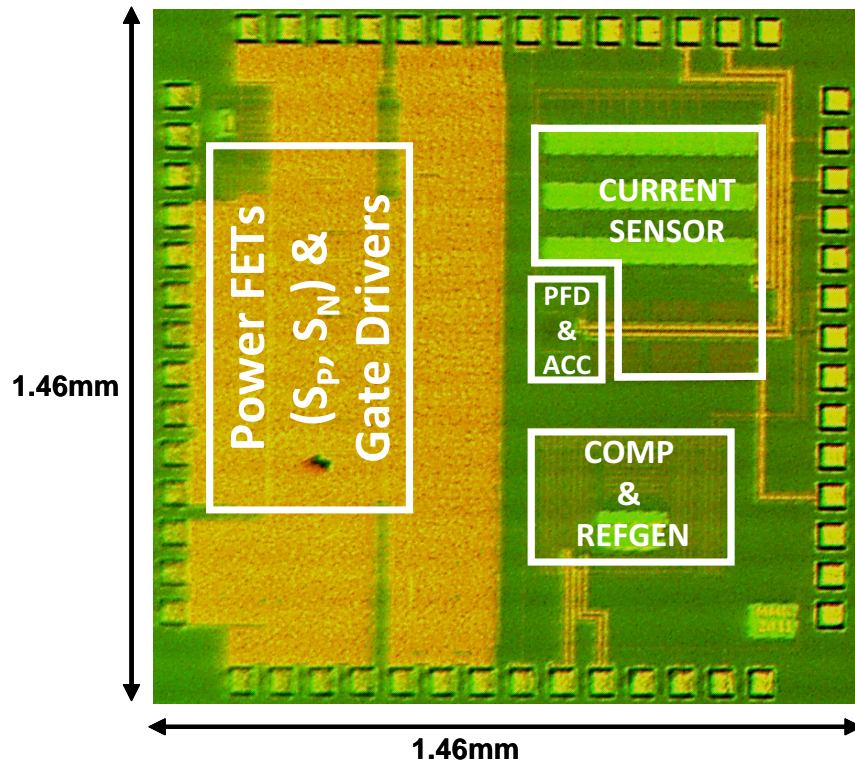
Figure 4.18: Die photo of the proposed hysteretic converter.

and time period of CK_{PWM} is locked with CK_{REF}. The phase offset between the two clocks is caused by the proportional path which switches R_P with this time offset to correct the error caused by the integral path. This could be observed from the behavior of V_{RAMP} where slope is different for the time duration of this phase offset.

The transient response of the converter, measured by applying a fixed load step of $600mA$ current with a rise/fall time of $100ns$, with different inductor values at an output voltage of $1.2V$ are shown in Fig. 4.23 - 4.25 . The converter is stable across a wide range of inductor values and the measured undershoot/overshoot is $61mV/72mV$ with $1.8\mu H$ inductor and $10\mu F$ capacitor and the settling time is less than $10\mu s$. The transient performance at higher inductor values is degraded

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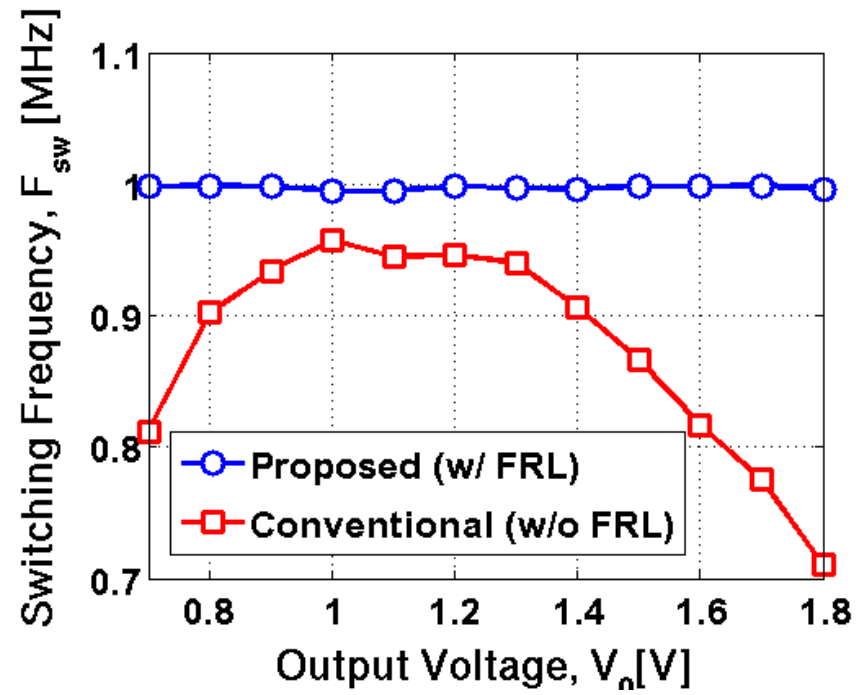
Figure 4.19: Switching frequency, F_{SW} vs input voltage, V_{IN} at $V_O = 1.2V$.
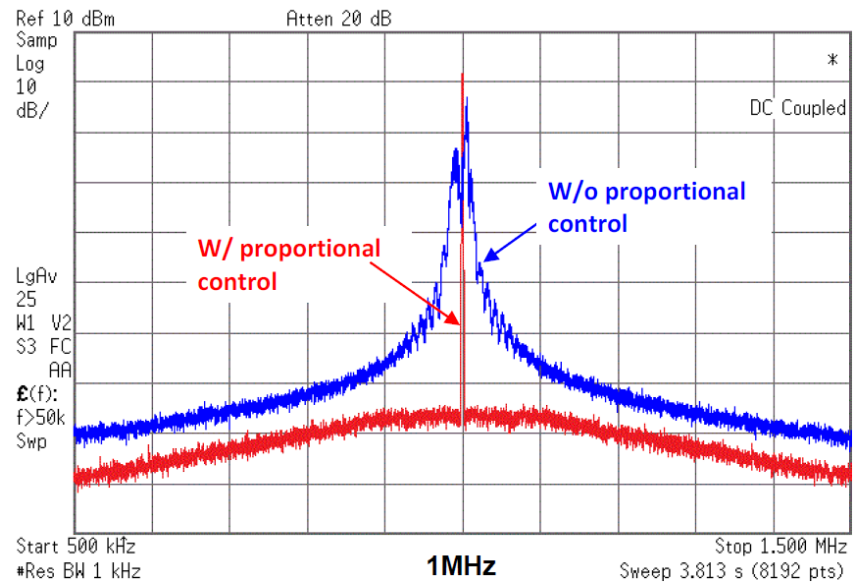
Figure 4.20: Spectrum of the switching clock, CK_{PWM}.
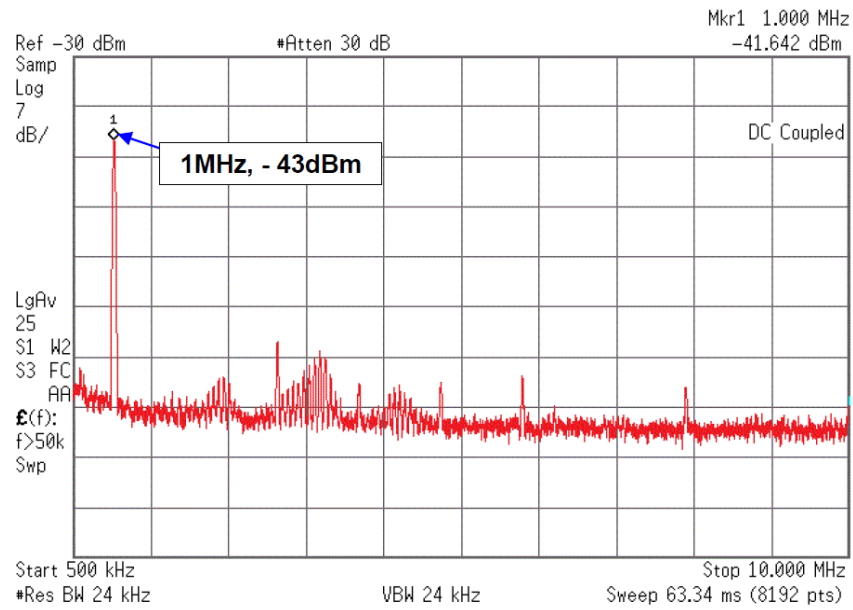
Figure 4.21: Output voltage spectrum.
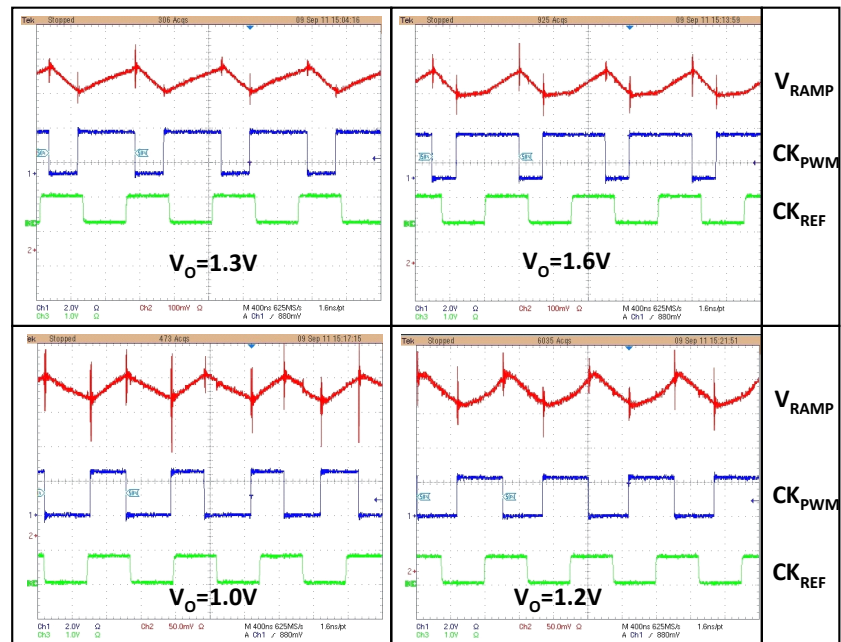
Figure 4.22: Measured V_{RAMP} and clock signals under locked condition for different duty cycles.

by the slower inductor current slew rate. Line regulation shown in Fig. 4.26 was measured by applying a $650mV$ pk-pk low frequency signal at V_{IN}. The result shows about $5mV/V$ line regulation which translates to $46dB$ suppression to line disturbances. Fig. 4.27 shows the efficiency of the converter measured as a function of load current and performance is summarized in Fig. 4.28. The peak efficiency is 93% at lower load current and stays above 90% up to 950mA of load current.
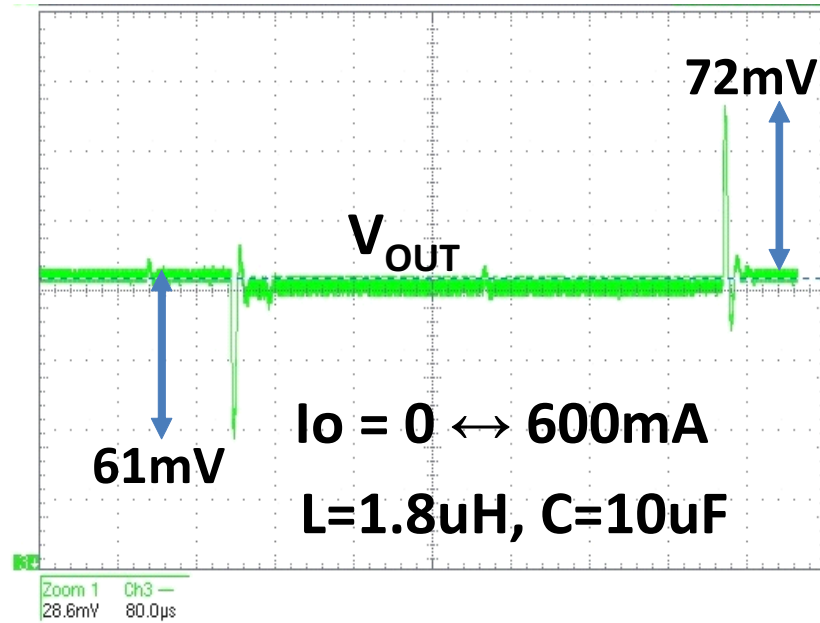
Figure 4.23: Measured output transient response at $L = 1.8\mu H$.
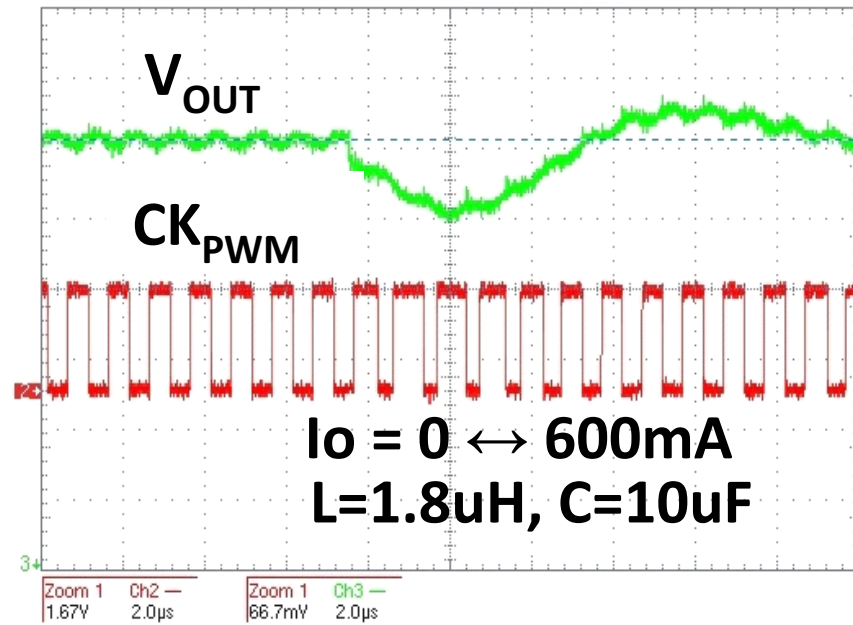
Figure 4.24: Ouput setlling at $L = 1.8\mu H$.
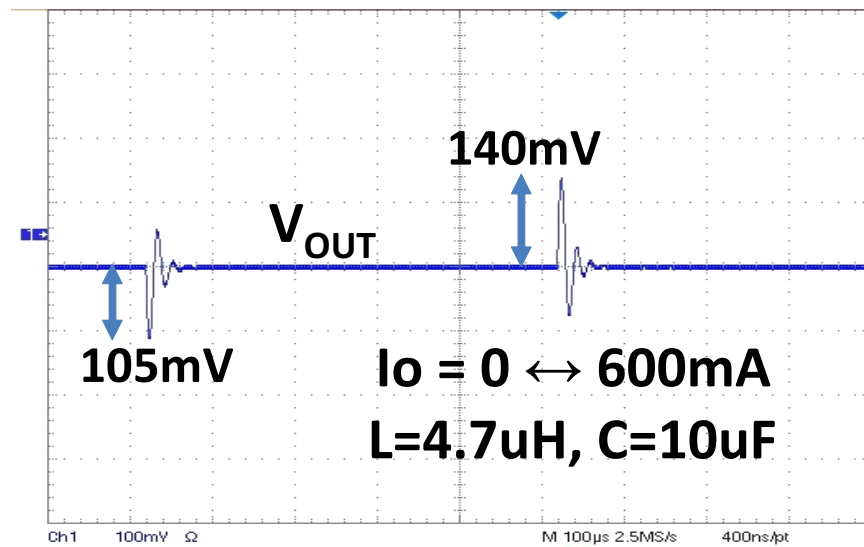
Figure 4.25: Measured output transient response at $L = 4.7\mu H$.
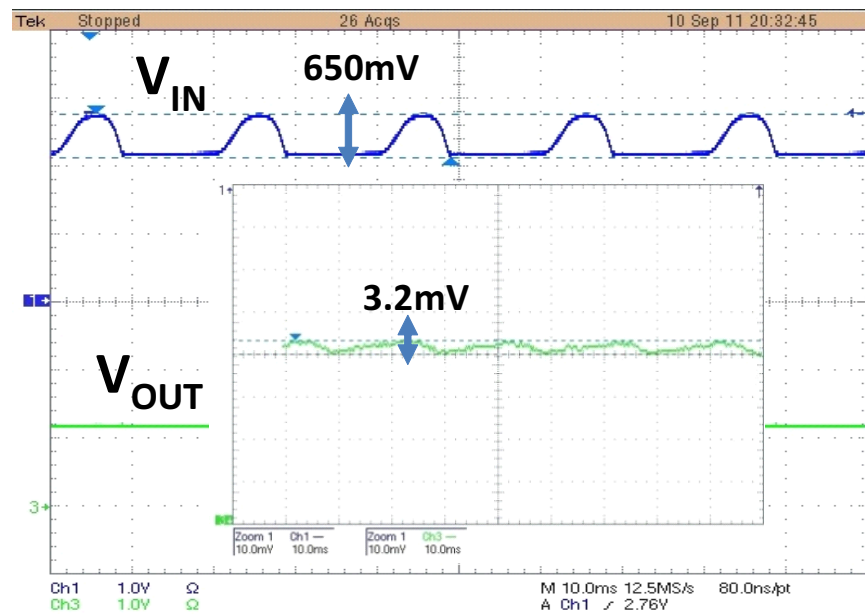
Figure 4.26: Measured line regulation.
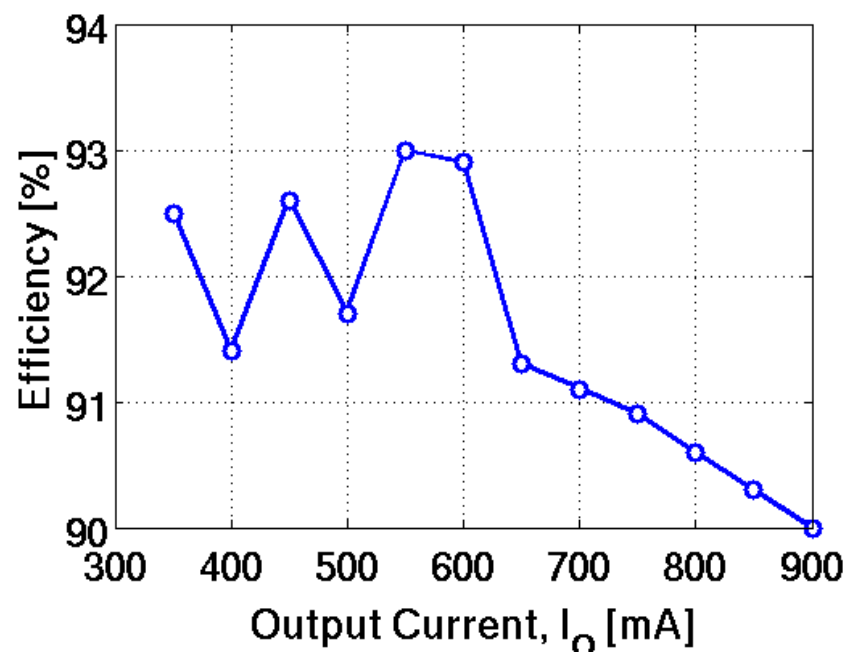
Figure 4.27: Measured efficiency vs. I_O.

Fabrication Process	130nm CMOS
Die size with Pad	2.13 mm² (1.46mm x 1.46mm)
Active Area	0.7 mm²
Input Supply Voltage (Vin)	2.5V
Output Voltage Range (Vout)	0.7V – 1.8V
Inductor	1μH – 5μH (DCR 50mΩ – 70mΩ)
Capacitor	10μF (ESR <20mΩ)
Total on-chip Capacitor	50pF
External Compensation Cap.	None
Load Current	350mA – 900mA
Efficiency	90% - 93% @ Iload = 0.35A – 0.9A
Switching Frequency	1 MHz
Switching Frequency Variation	0.1% - 0.5%
Load Regulation	< 2mV / A
Line Regulation	5mV/V @ Vout = 1.2V
Load Transient (0 ↔ 600mA) Undershoot/Overshoot/Set.Time	@ 1.2V, L=1.8uH, C=10μF 61mV/72mV/< 10μs
Output Ripple Quiescent/ no switching Current (Iq)	5mV (p-p) 50μA

Figure 4.28: Performance summary.

CHAPTER 5. TIME BASED PWM CONTROLLER FOR HIGH FREQUENCY DC-DC CONVERTERS

This chapter presents design of a highly integrated, ultra low power continuous time PWM controller using time based signal processing (TSP). By virtue of the continuous time digital nature of the proposed time based PWM (TPWM) controller, it is capable of achieving very high resolution and speed without using any error amplifier and large capacitor or any high resolution ADC and DPWM while preserving all the benefits of both analog and digital PWM controllers. The chapter is organized as follows. Sections 5.1 discusses trade-off involved in the high speed design of conventional analog and digital PWM based switching converters. Section 5.2 gives an introduction to time domain signal processing and realizes different building blocks in time domain. Section 5.3 introduces the concept of time based proportional-integral-derivative (PID) compensator used in the proposed controller. Architecture of the proposed TPWM based buck converter is presented in Section 5.4. Implementation and circuit design details are discussed in Sections 5.5 and 5.6, respectively. The chapter is concluded with simulation results and issues related to the proposed controller with possible solutions.

5.1 Trade-offs in high speed Switching Converter

As switching DC-DC converters are progressing towards miniaturization by operating at higher speed, achieving high efficiency while meeting the desired output voltage accuracy and transient response is highly challenging. In the converter

shown in Fig. 5.1, the proportional-integral-derivative (PID) compensator occupies most of the controller's area due to large size of capacitors (mainly the integrator). The need of high gain-bandwidth error amplifier(EA) also puts a constraint on quiescent power when converter is operated at higher speed.
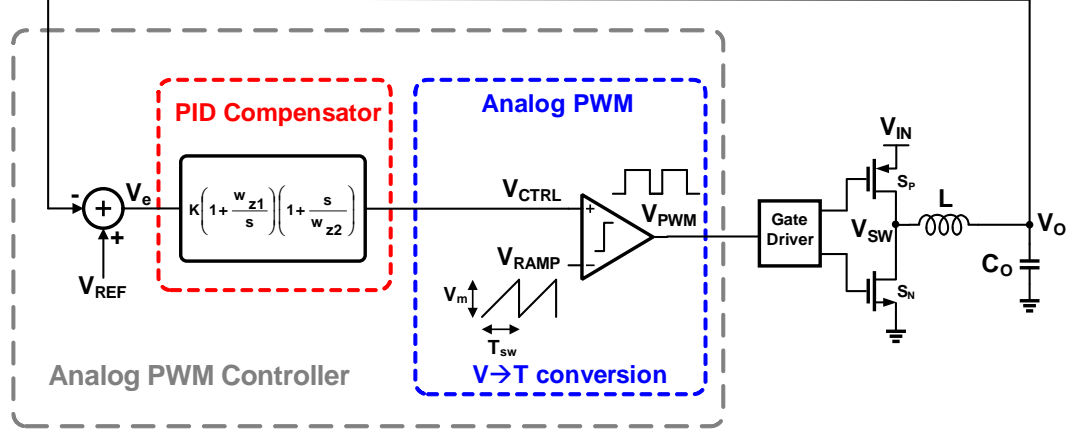
Figure 5.1: An analog PWM based dc-dc converter.

Another limiting factor in high speed converters is finite delay associated with the PWM comparator and ON/OFF time of power switches S_P and S_N. Assuming t_p is the propagation delay in PWM comparator, t_r is the reset time of PWM ramp and t_{d_sw} is the delay of power switches (including gate driver delay), the total loop delay can be expressed as:

$$t_d = t_p + t_r + t_{d\_sw} \tag{5.1}$$

In order to operate at $10MHz$ with the duty cycle range of $10\% - 90\%$, the required delay should be less $5ns$ which is quite difficult to achieve with low power consumption. In such a case, the converter's duty cycle range is limited. Limiting the duty cycles to a narrow range will not only affect the transient response but also limit the input/output operating voltage range. In a digitally controlled converter on the other hand, error voltage, V_e is digitized and processed in a digital PID

compensator, as shown in Fig. 5.2. The digital-to-time (D-T) conversion takes place in a digital PWM (DPWM) which generates the desired duty cycle. However, it requires high precision analog-to-digital converter (ADC) and DPWM to avoid limit cycling [20] and maintain good accuracy in the regulated output voltage. Since power consumption of both ADC and DPWM grows exponentially with speed and resolution, it becomes hard to meet the low power requirement when converter is switching at high speed.
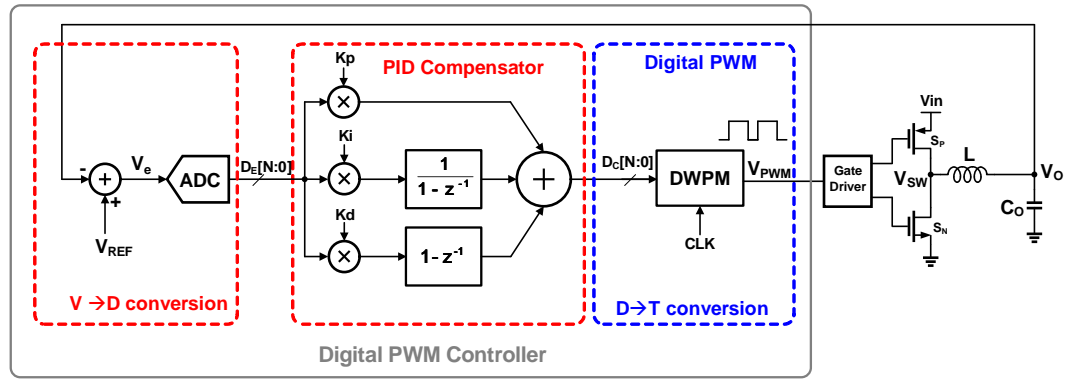
Figure 5.2: A digital PWM based dc-dc converter.

In an effort to overcome the above issues with conventional analog and digital PWM controllers, a highly integrated, ultra low power continuous time PWM controller based on time based signal processing (TSP) is presented. By virtue of the continuous time digital nature of the proposed time based PWM (TPWM) controller, it is capable of achieving very high resolution and speed without using any error amplifier and large capacitor or any high resolution ADC and DPWM while preserving all the benefits of both analog and digital PWM controller.

5.2   Time (phase) domain signal processing

The concept of time domain signal processing (TSP) was originally derived from phase locked loop where VCO is a phase integrator. So far the application of TSP has been in ADC where op-amp based integrators are replaced with VCOs [33]-[34]. Previously published work have shown application of VCOs in dc-dc converter but only in the PWM generation while still requiring a separate PID compensator for stabilizing the loop therefore posing the same challenges discussed in previous section [35]-[36]. In this section we will discuss the basic building blocks which lead to implementation of a complete PID compensator in time domain.

5.2.1   Time Domain Amplifier

A time domain amplifier can be realized with a voltage controlled delay line (VCDL) as shown in Fig. 5.3. It consists of a chain of delay cells. Assuming delay of each cell is proportional to input supply voltage then the delay with respect to a reference clock, CK_{REF} can be varied by controlling V_{IN}. If this delayed clock, CK_{IN} is passed through a phase detector (which is a RS flip-flop in this case) clocked with CK_{REF} the pulse width output clock, CK_{OUT} is a function of input voltage V_{IN}.

Assuming K_{VCDL} be the small signal phase gain in rad/V of the VCDL, output phase transfer function can be represented as,

$$\frac{\phi_p}{v_{in}} = K_{VCDL} \tag{5.2}$$

which represents a time domain amplifier whose gain can be controlled by
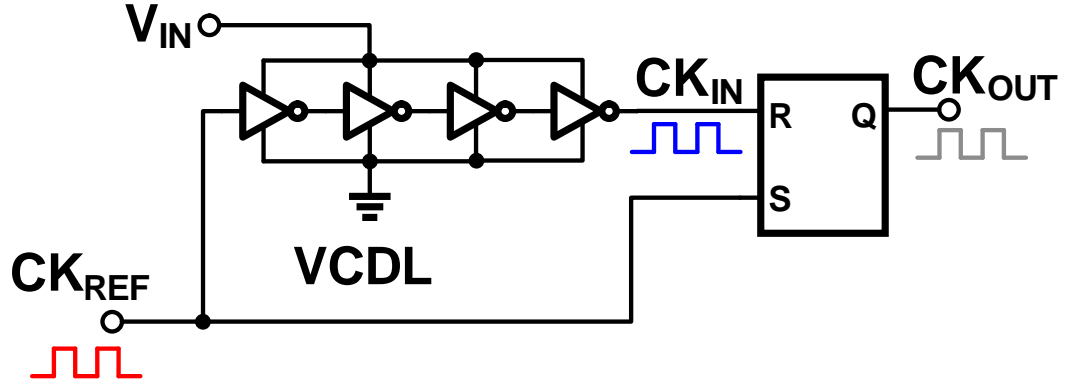
Figure 5.3: A VCDL used as phase amplifier

K_{VCDL}. In time domain, the delay can be represented as:

$$t_p(v) = \frac{T_{REF}}{2\pi} K_{VCDL} v_{in} \qquad (5.3)$$

where T_{REF} is the clock period of the reference clock.

The step response of the VCDL is shown in Fig. 5.4 where a small step voltage ΔV is applied at the input changing the output delay by an amount of ΔT.
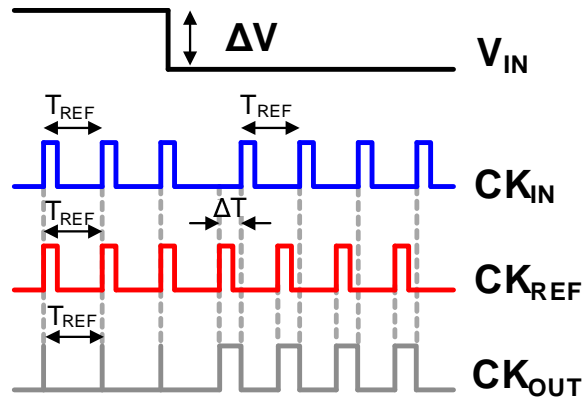
Figure 5.4: Step response of a VCDL

Note : The above equations assume that the delay of VCDL is a linear func-

tion of voltage (in actual implementation a linear delay cell or current controlled delay cell is used because delay of an inverter is not a linear function of supply voltage. Inverter delay cells here are only used for illustration purposes and should be treated as a generic delay cell. Term VCDL here is used as a generic term and could be interchangeable with current controlled delay line (CCDL). The same is true for voltage controlled oscillators (VCO) and current controlled oscillators (CCO) as well.

The VCDL can also be used to implement the differentiator. As shown in Fig. 5.5, V_{IN} can be passed through a first order high pass RC filter before feeding to the VCDL.
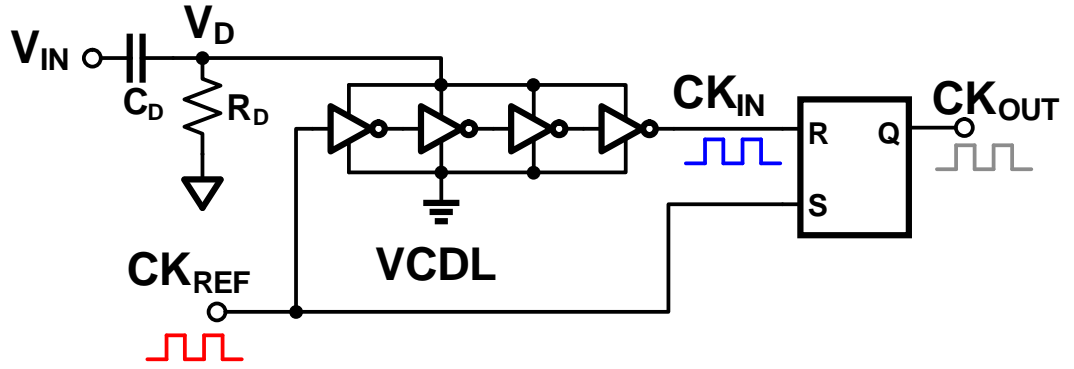
Figure 5.5: A phase differentiator using VCDL

The input to VCDL, V_D is given by

$$v_d(s) = \frac{R_D C_D s}{1 + R_D C_D s} v_{in} = v_{in} R_D C_D s \qquad \text{if } R_D C_D << \qquad (5.4)$$

Assuming $R_D C_D$ low, the above transfer function can be written as:

$$v_d(s) = R_D C_D s \qquad (5.5)$$

Representing a differentiator and derivative phase transfer function can be

expressed as:

$$\frac{\phi_d(s)}{v_{in}(s)} = R_D C_D K_{VCDL} s \qquad (5.6)$$

Step response of time based differentiator is shown in Fig. 5.6. It could be observed that the output of VCDL responds to only high frequency changes at V_{IN} and delay goes back to zero in steady state.
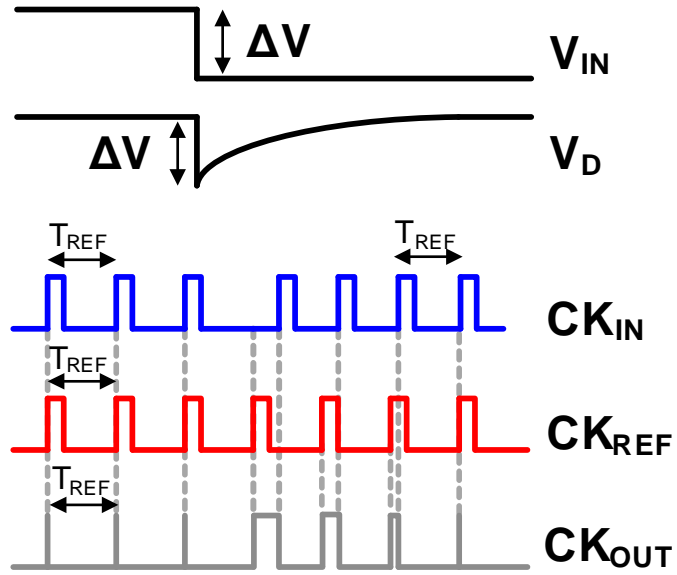
Figure 5.6: Step response of a phase differentiator

5.2.2 Time Domain Integrator

The relationship between phase and frequency of an oscillator is given by:

$$w = \frac{d\phi}{dt} \qquad \text{or} \qquad \phi = \int w \, dt \qquad (5.7)$$

Hence phase can be represented as integral of frequency. Assuming a voltage controlled oscillator having frequency proportional to input voltage, the phase

transfer function can be represented as:

$$\frac{\phi_i(s)}{v_{in}(s)} = \frac{K_{VCO}}{s} \tag{5.8}$$

Where K_{VCO} is the VCO gain in rad/sec. The integrator's time constant is represented as $\frac{1}{K_{VCO}}$

A VCO integrator is shown in Fig. 5.7 and the step response in Fig. 5.8. We can see the phase of CK_{IN} gets accumulated in every clock cycle of CK_{REF} just like an analog integrator which accumulates the voltage.
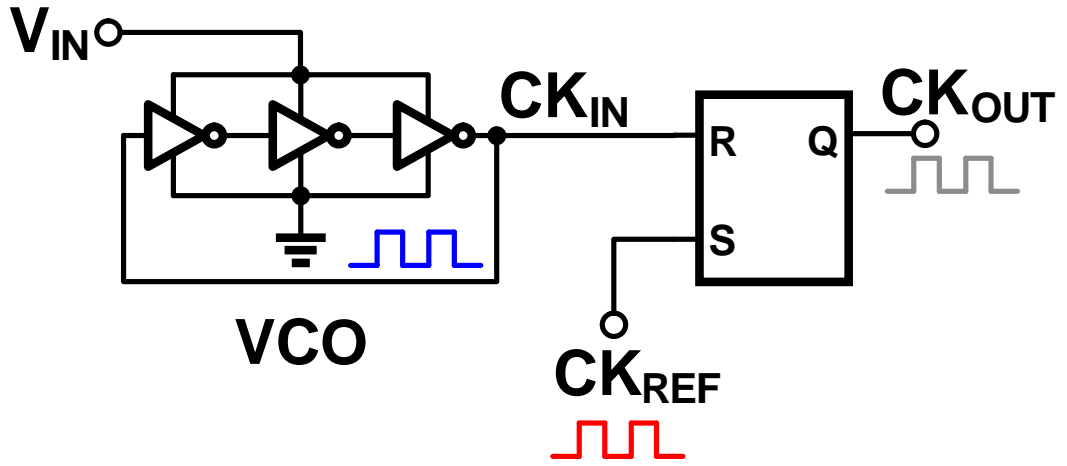
Figure 5.7: A time based integrator using VCO

5.3 Time based PID compensator (TPID)

The transfer function of a voltage mode PID compensator shown in Fig. 5.1 is given by [4]:

$$H_{PID}(s) = \frac{v_{CTRL}(s)}{v_O(s)} = K \left(\frac{w_{z1}}{s} + 1 \right) + \left(\frac{s}{w_{z2}} + 1 \right) \tag{5.9}$$
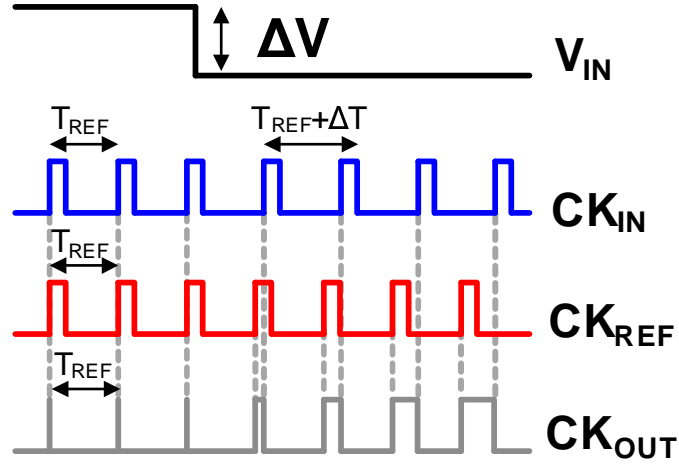
Figure 5.8: Step response of time based integrator

which could also be written as:

$$H_{PID}(s) = K\left(1 + \frac{w_{z1}}{w_{z2}}\right) + \frac{Kw_{z1}}{s} + \frac{K}{w_{z2}}s \qquad (5.10)$$

Comparing above with a standard PID transfer function $H_{PID}(s) = K_P + \frac{K_I}{s} + K_D s$, we can get:

Proportional Gain,

$$K_P = K\left(1 + \frac{w_{z1}}{w_{z2}}\right) \qquad (5.11)$$

Integral Gain,

$$K_I = Kw_{z1} \qquad (5.12)$$

and derivative gain:

$$K_D = \frac{K}{w_{z2}} \qquad (5.13)$$

which shows that the PID transfer function of eq. 5.9 can be implemented by using three building blocks: (1) a time based amplifier for proportional path, (2) a time based integrator, and (3) a time based differentiator as realized in the previous section.

The block diagram of the complete PID compensator is shown in Fig. 5.9. The proportional and derivative functions are added together to eliminate one VCDL and gain A_D added to control the derivative gain.
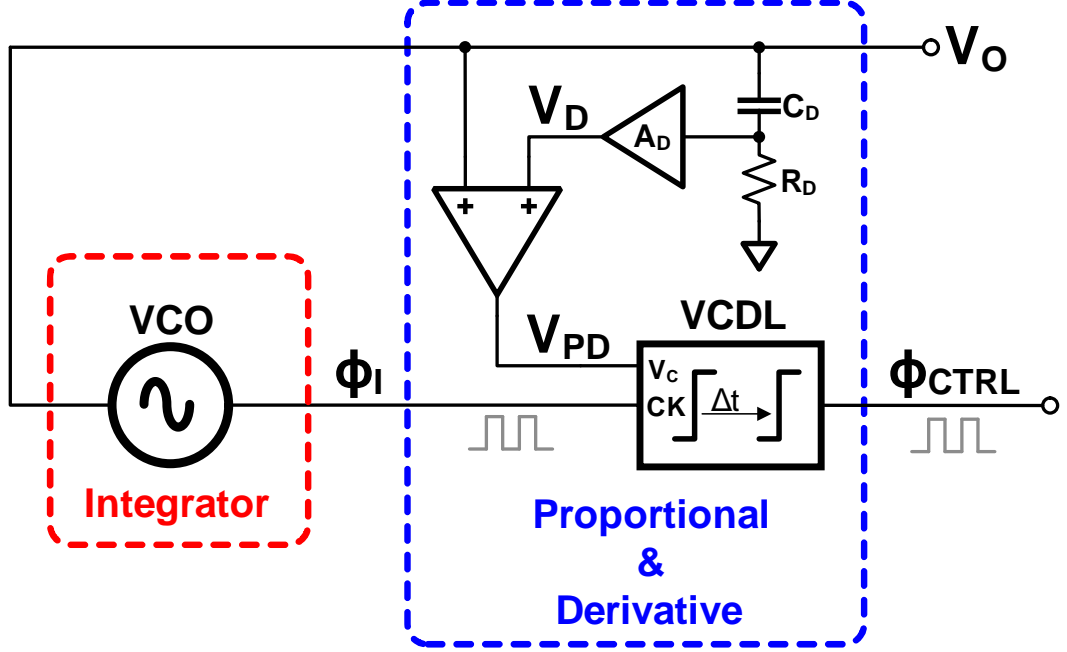
Figure 5.9: Block diagram of a time based PID compensator

The voltage to phase transfer function can be expressed as:

$$H_{TPID}(s) = \frac{\phi_i(s)}{v_O(s)} + \frac{\phi_{CTRL}(s)}{v_{PD}(s)} \qquad (5.14)$$

from eqs. 5.2, 5.6 and 5.8

$$H_{\phi PID}(s) = \frac{K_{VCO}}{s} + K_{VCDL} + K_{VCDL}A_D R_D C_D s \qquad (5.15)$$

and the proportional, integral and derivative gains in terms of phase can be given as:

Proportional Gain,

$$K_{P\phi} = K_{VCDL} \qquad (5.16)$$

Integral Gain,

$$K_{I\phi} = K_{VCO} \tag{5.17}$$

and Derivative Gain:

$$K_{D\phi} = K_{VCDL}A_DR_DC_D \tag{5.18}$$

Comparing with the K_P, K_I and K_D of voltage domain PID compensator (eq. 5.11-5.13), we can write:

$$K_{VCDL} = K\left(1 + \frac{w_{z1}}{w_{z2}}\right) \tag{5.19}$$

$$K_{VCO} = Kw_{z1} \tag{5.20}$$

$$K_{VCDL}A_DR_DC_D = \frac{K}{w_{z2}} \tag{5.21}$$

Once we know the location of compensation zeros (w_{z1} and w_{z2}), K_{VCDL}, K_{VCO}, A_D and R_DC_D can be calculated for designing a time based PID compensator. This PID compensator forms the basis of proposed TPWM controller discussed in the following section.

5.4 Proposed Time based PWM (TPWM) Controller

The architecture of a buck converter based on proposed TPWM controller is shown in Fig. 5.10. The controller consists of three main blocks, reference clock generator, TPID compensator and phase comparator. Since output of TPID compensator is phase (time), the duty cycle is obtained directly by comparing ϕ_{CTRL} with a reference phase ϕ_{REF}. The reference clock generator is designed

in such a way that the reference VCO (RVCO) is locked at the desired converter switching frequency, F_{SW} when it is biased with a reference voltage V_{REF} at which the output voltage, V_O needs to be regulated. The feedback VCO (FVCO) receives V_O as input and outputs a clock with phase ϕ_I and acts as an integrator. If FVCO is precisely matched with RVCO then the frequency of the two VCOs should be locked only in one condition i.e. $V_O = V_{REF}$.
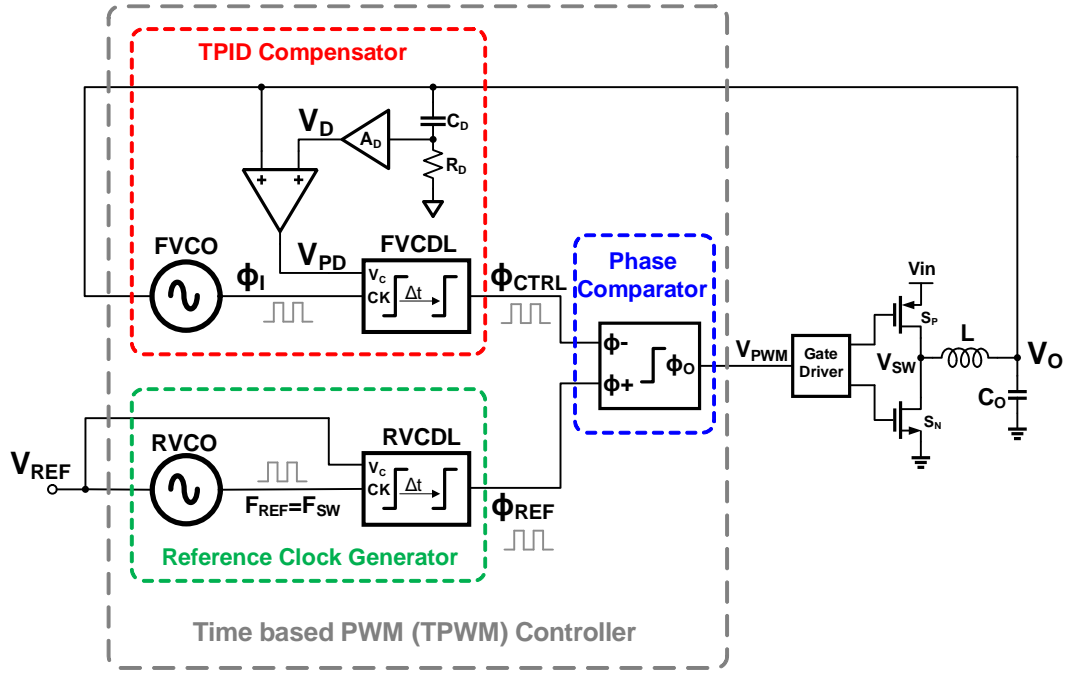
Figure 5.10: Block diagram of the proposed time based PWM controller.

In order to understand the regulation mechanism let us first consider a buck converter with only VCO integrator in the loop as shown in Fig. 5.11.

Assuming the two VCOs are matched and have same K_{VCO}, the phase outputs can be represented as:

$$\phi_{CTRL} = \int w_{FB}dt = K_{VCO} \int V_O dt \qquad (5.22)$$

and
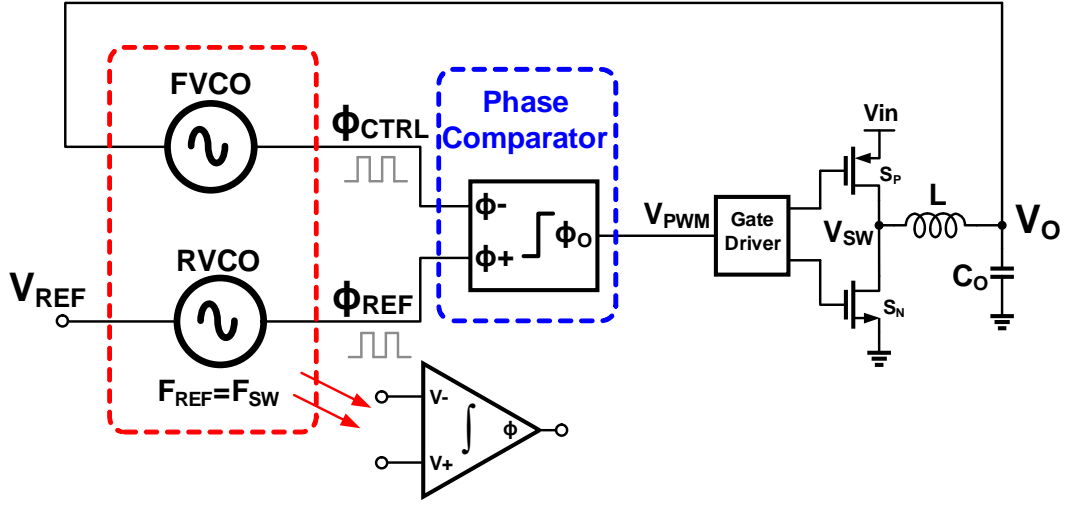
Figure 5.11: A converter with only integral loop.

$$\phi_{REF} = \int w_{REF}dt = K_{VCO} \int V_O dt \tag{5.23}$$

where w_{FB} and w_{REF} are the frequencies of FVCO and RVCO respectively in rad/sec.

The output of phase subtractor is given by:

$$\phi_{PWM} = \phi_{REF} - \phi_{CTRL} = K_{VCO} \int (V_{REF} - V_O)dt \tag{5.24}$$

The above equation indicates that any error voltage between V_{REF} and V_O is integrated just like any other integrator but output is phase instead of voltage. Upon closing the converter loop with integrator, the FVCO should force the phase difference between ϕ_{REF} and ϕ_{CTRL} such that the two VCOs are locked at the same frequency which is only possible if $V_{REF} = V_O$. This phase difference when translated into time domain, is the ON time of PWM signal, V_{PWM} and given by:

$$T_{ON} = \frac{T_{SW}}{2\pi} \phi_{PWM} \tag{5.25}$$

Implying that the duty cycle, $D = \frac{T_{ON}}{T_{SW}}$ will be,

$$D = \frac{\phi_{PWM}}{2\pi} \tag{5.26}$$

which eliminates the need of any PWM generator as required by a conventional analog or digital PWM controller. The relationship between phase and duty cycle is plotted in Fig. 5.12 which is perfectly linear.
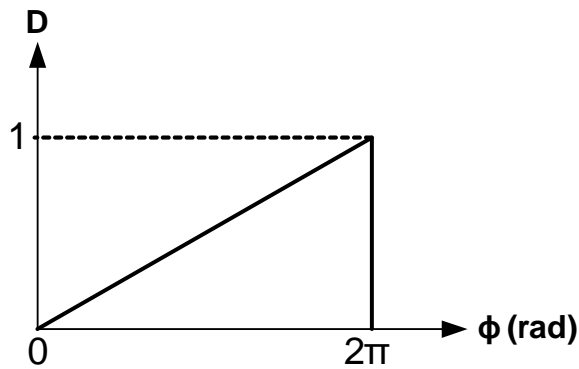
Figure 5.12: Duty cycle vs. phase.

Since integrator's time constant is inversely proportional to K_{VCO}, a large time constant could be achieved with low K_{VCO} without any large capacitor.

The PID compensator shown in Fig. 5.10 uses RVCDL in the reference clock generator to match with the phase of feedback path so that the converter always starts with minimum duty cycle. However, any phase difference in reference and feedback path will not affect the regulation as FVCO will alway lock to F_{REF} thus forcing $V_O = V_{REF}$. Any transient at V_O is corrected by the proportional and derivative paths implemented with FVCDL by providing rapid change in the control phase. The next section discusses the circuit design.

5.5 Designing TPID parameters

The proposed TPWM based buck converter was designed for following specifications:

$V_{IN} = 1.8V, V_O = 0.6 - 1.8V, F_{SW} = 10MHz, L = 200nH, C_O = 5\mu F, F_{UGB} \approx 1MHz, PM \approx 60deg$

The different parameters of PID compensator can be calculated using following procedure [4]:

The DC gain of uncompensated loop, G_O for $V_{IN} = 1.8V$ and $V_O = 0.6V$, $V_{REF} = 0.6V$ is given by:

$$G_O = \beta G_{PWM} = 1 \tag{5.27}$$

where $\beta = \frac{V_{REF}}{V_O}$ is the feedback factor and G_{PWM} is the gain of PWM modulator which is 1 as time based controller has no PWM modulator.

The loop gain at desired UGB of 1MHz can be calculated as:

$$G_{UGB} = G_O \left(\frac{F_{UGB}}{F_{LC}}\right)^2 = 0.0256 \tag{5.28}$$

where F_{LC} is the resonance frequency of output LC filter which is $\frac{1}{2\pi\sqrt{LC_O}} = 160KHz$ in this case.

The location of second zero (f_{z2}) for 60° phase margin needs to be:

$$f_{z2} = F_{UGB}\sqrt{\frac{1 - \sin(60°)}{1 + \sin(60°)}} = 268KHz \tag{5.29}$$

and high frequency pole (f_p) due to $R_D C_D$ should be located at:

$$f_p = F_{UGB}\sqrt{\frac{1 + \sin(60°)}{1 - \sin(60°)}} = 3.73MHz \tag{5.30}$$

The required compensator gain, K can be calculated as:

$$K = \frac{1}{G_{UGB}} \sqrt{\frac{f_{z2}}{f_p}} = 10.6 \tag{5.31}$$

The first zero (f_{z1}) is chosen to be between $\frac{1}{2}F_{LC}$ and F_{LC} for sufficient phase margin. For this example we choose $f_{z1} = \frac{1}{2}F_{LC} = 80KHz$

The calculated PID parameters from eq. 5.11-5.13 are:

$K_I = 5.3e6 rad/sec$, $K_P = 13.7$ and $K_D = 6.3e-6 sec/rad$

And required parameters for TPID are calculated from eq. 5.19-5.21 as:

$K_{VCDL} = 13.7$, $K_{VCO} = 5.3e6 rad/sec$ and $A_D = 10.8$

and in time domain:

$K_{VCDL\_t} = \frac{K_{VCDL}}{2\pi F_{SW}} = 220nsec/V$, $K_{VCO\_t} = \frac{K_{VCO}}{2\pi} = 842KHz/V$

The loop gain and phase response of the converter with above parameters modeled in MATLAB are shown in Fig. 5.13 indicating the phase margin of around $60°$ at all the voltages. The bandwidth reduces at higher voltage due to change in feedback factor, β.

5.6 Design and implementation

Since K_{VCO} is mostly technology dependent and running at 10MHz, the VCO gain is normally around 10-20MHz/V. Therefore realizing such a low K_{VCO} requires some additional circuit techniques. In the proposed design, the large time constant of VCO integrator was realized by first converting the voltage into current and current to phase by a low gain transconductance amplifier using current controlled oscillators (CCO) as output loads as shown in Fig. 5.14.

This topology offers following benefits: (1) by controlling the difference of
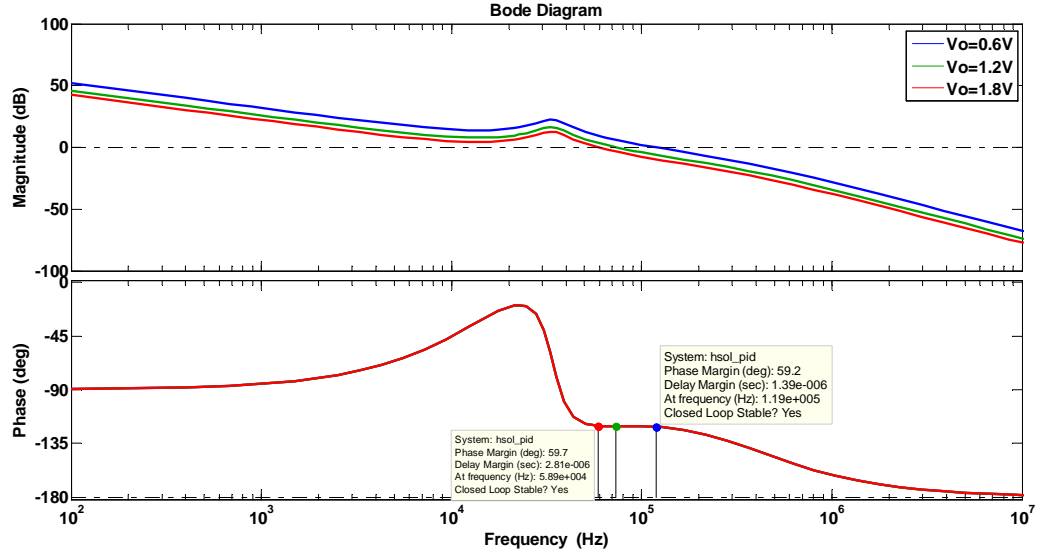
Figure 5.13: Magnitude and phase response of the compensated dc-dc buck converter at different output voltages

G_{m1} and G_{m2}, we can realize a large time constant, (2) since output is fully differential, if one of the outputs is used as reference while other as feedback phase, it offers dual edge pulse width modulation [36] and provides 2x faster response as compared to a single edge modulation, (3) the voltage-to-phase relationship can be linearized by de-generating the source with resistor (R_S). The differential phase output to differential input voltage transfer function of the integrator can be expressed as:

$$\frac{\phi_o(s)}{v_{in}(s)} = \frac{G_m K_{CCO}}{s} \tag{5.32}$$

where K_{CCO} is the current-phase gain of CCO expressed in $\frac{rad/sec}{Amp}$, which gives voltage-phase gain as:

$$K_{VCO} = G_m K_{CCO} \tag{5.33}$$
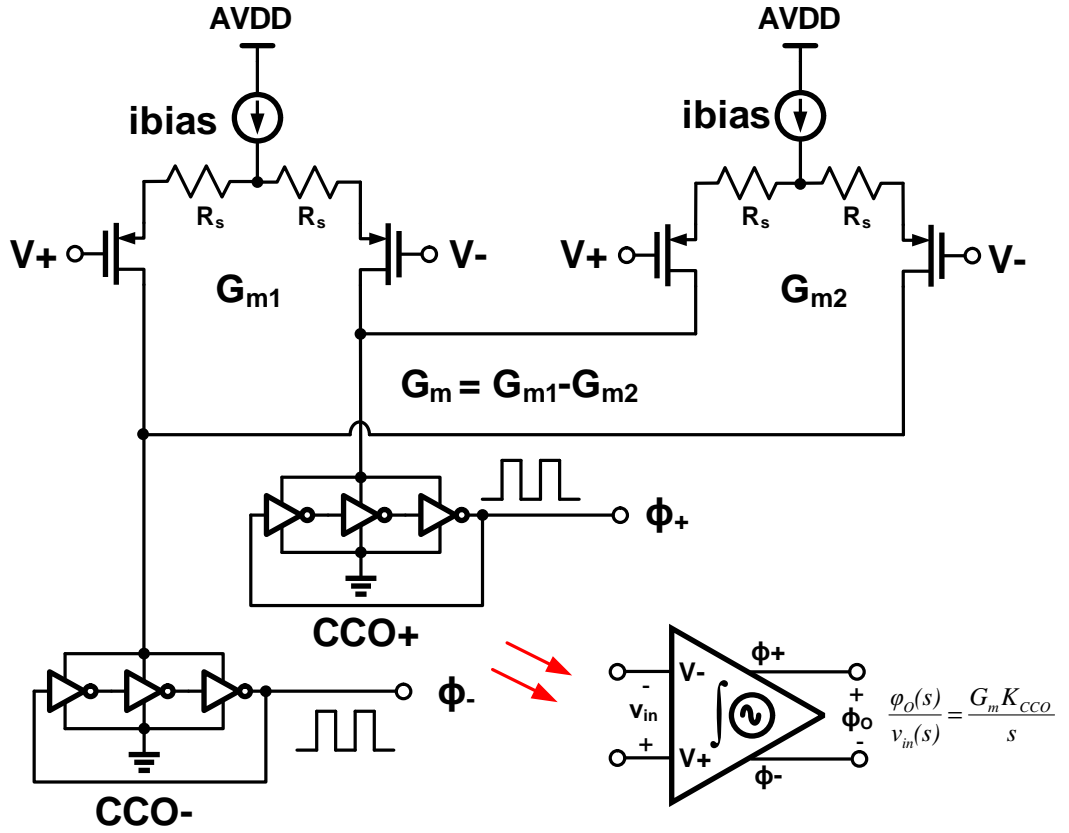
Figure 5.14: A fully differential phase integrator with large time constant

On the other hand, proportional and derivative (PD) control uses two separate transconductance, G_{mP} and G_{mD} where input of G_D is fed with the high pass filtered V_O. The complete architecture is shown in Fig. 5.15.

The low swing output clocks of CCO and CCDL are re-shaped in level shifters (LVSF) to provide rail-rail clock signals with sharp edges. The phase subtractor is simply an RS flip-flop with positive edge detector. The duty cycle of pulse width modulated signal, V_{PWM} is set at every positive edge of the positive control phase, ϕ_{CTRL+} and reset at every positive edge of the negative control phase, ϕ_{CTRL-} hence giving a duty cycle proportional to the difference of two control phases.
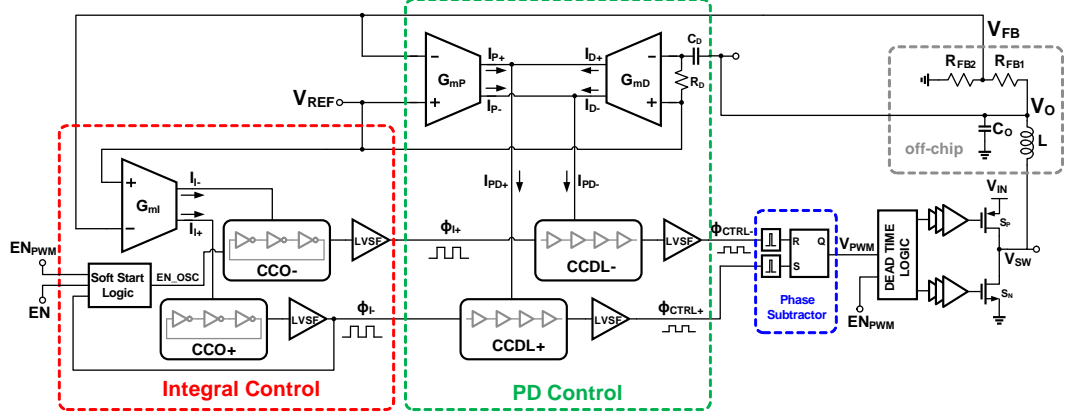
Figure 5.15: Architecture of the buck converter implemented with proposed time based PID controller

Overall output-to-input transfer function of the buck converter can be expressed as:

$$H(s) = -\beta H_{TPID}(s) H_{LC}(s) \tag{5.34}$$

Where β is the feedback factor expressed as: $\beta = \frac{R_{FB2}}{R_{FB1} + R_{FB2}}$

H_{LC} is the transfer function of output LC filter.

and H_{TPID} is the transfer function of time based PID compensator which is given as:

$$H_{TPID}(s) = G_{mP} K_{CCDL} + \frac{G_{mI} K_{CCO}}{s} + \frac{1}{\beta} G_{mD} K_{CCDL} R_D C_D s \tag{5.35}$$

Which shows that the proportional, integral and derivative gains can be controlled independently by G_{mP}, G_{mI} and G_{mD} respectively.

5.7   Simulation Results

The proposed TPWM based dc-dc converter was implemented in $0.18\mu m$ CMOS technology targeted for 500mA max load current and switching frequency of 10MHz. The entire PWM controller consumes only $25\mu A$ current. Fig. 5.16 shows the full chip layout along with zoomed-in controller. It can be noticed that the controller occupies only 150um x 250um active silicon area.
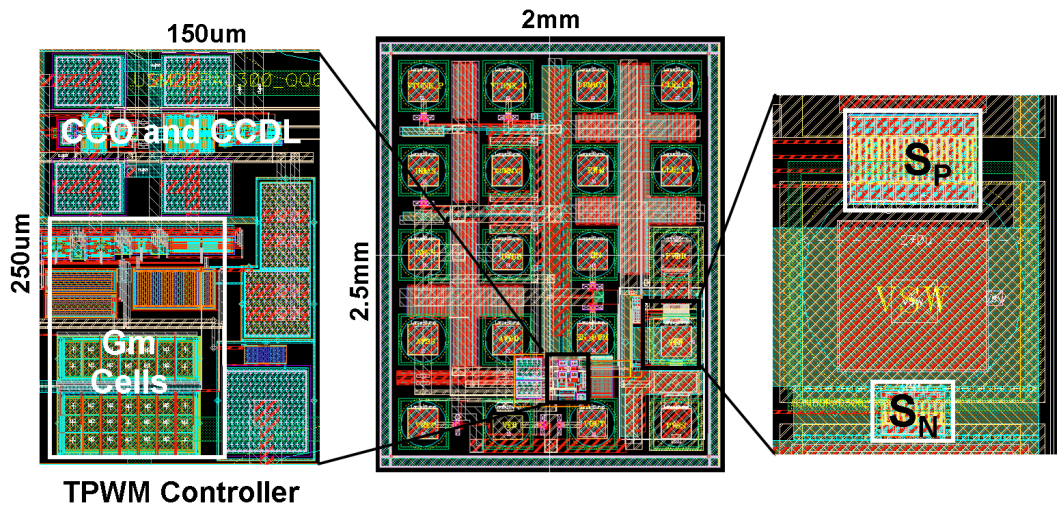
Figure 5.16: Layout of the full chip dc-dc converter implemented with TPWM controller

Simulated transient results across various process and temperature corners are shown in Fig. 5.17 to Fig. 5.22. Maximum overshoot/undershoot was 40mV and output settles within $5\mu s$

The simulated efficiency across load current is shown in Fig. 5.23. The peak efficiency is 96% around CCM-DCM boundary when load current is 100mA. The efficiency simulation was carried out at typical process corner with inductor DCR of $50m\Omega$. At worst corner, efficiency might drop by 4-5% due to increase in the ON resistances of power switches, S_P and S_N.
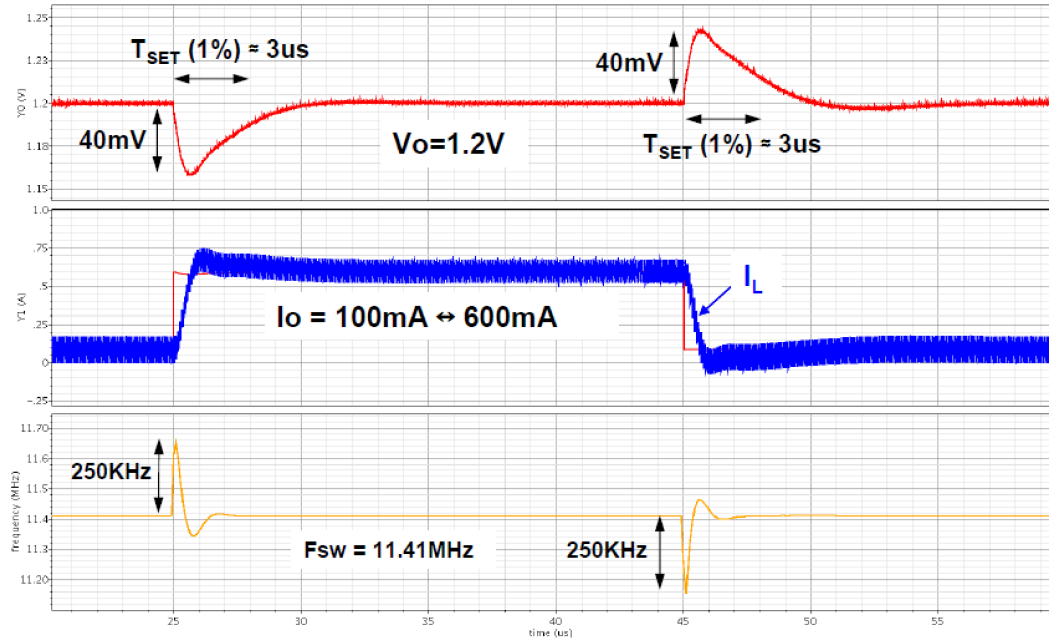
Figure 5.17: Transient response at V_O=1.2V, typical process and 27 deg.

5.8 Issues with time based PWM controller

Even though the TPWM controller shown in Fig. 5.15 has many advantage over conventional PWM, it has some inherent issues which need to be addressed. These problems are discussed below with their possible solutions:

5.8.1 Duty Cycle Slipping

The cycle slip is a well known problem in phase locked loops (PLL) and by the virtue of time based signaling employed in TPWM, it also suffers from the same. The main reason for cycle slipping is limited range of phase subtractor (detector). Any linear phase detector has a maximum phase detector range of 2π

Figure 5.18: Transient response at V_O=1.2V, fast process and -40 deg.

Figure 5.19: Transient response at V_O=1.2V, slow process and 27 deg.
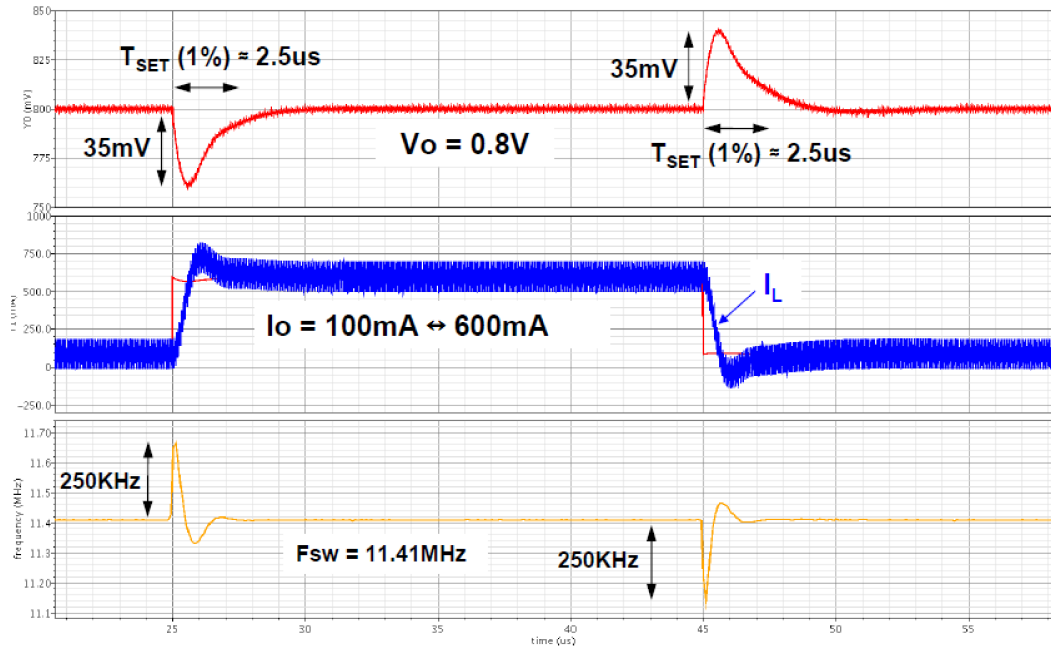
Figure 5.20: Transient response at V_O=0.8V, typical process and 27 deg.

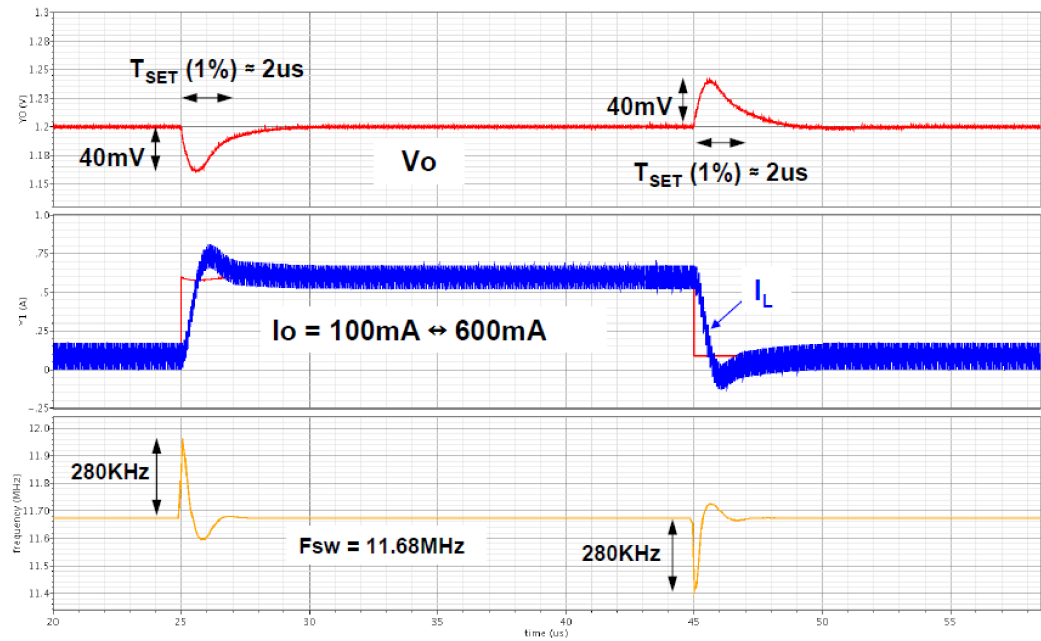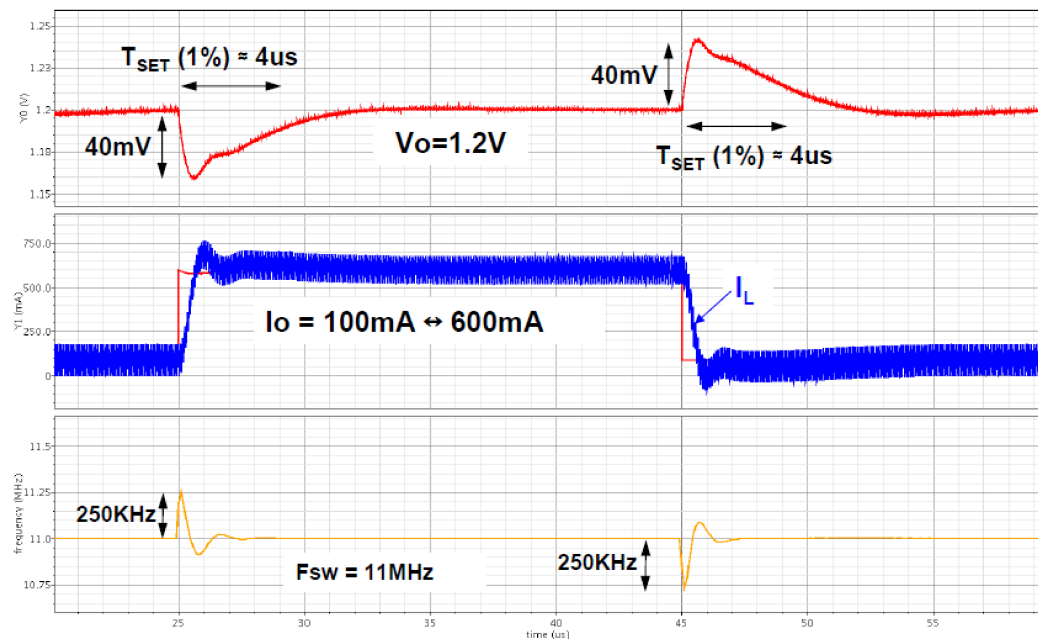(i.e. one clock cycle) due to phase folding nature of a clock ($2n\pi = 2\pi$). Therefore phase output is reset if input phase difference becomes multiple of 2π. This causes duty cycle of PWM to go to 0 if the phase difference becomes 2π, as shown in Fig 5.24, and phase integrator loses the steady state operating point.

In a voltage mode integrator, the output of the integrator is stored on a capacitor so it will cause the duty cycle to saturate at 100%. Since phase cannot be stored like a voltage, the resetting of duty cycle causes the dc-dc converter to lose the output regulation. This will cause an undesirable transient behavior at the output as showing in Fig. 5.25. The transient voltage and recovery time depends upon the loop bandwidth.

As seen in Fig. 5.25, the converter's output V_O is initially regulated such that duty cycle is close to 90%. The output voltage slightly drops due to load tran-

Figure 5.21: Transient response at V_O=0.8V, slow process and 27 deg.

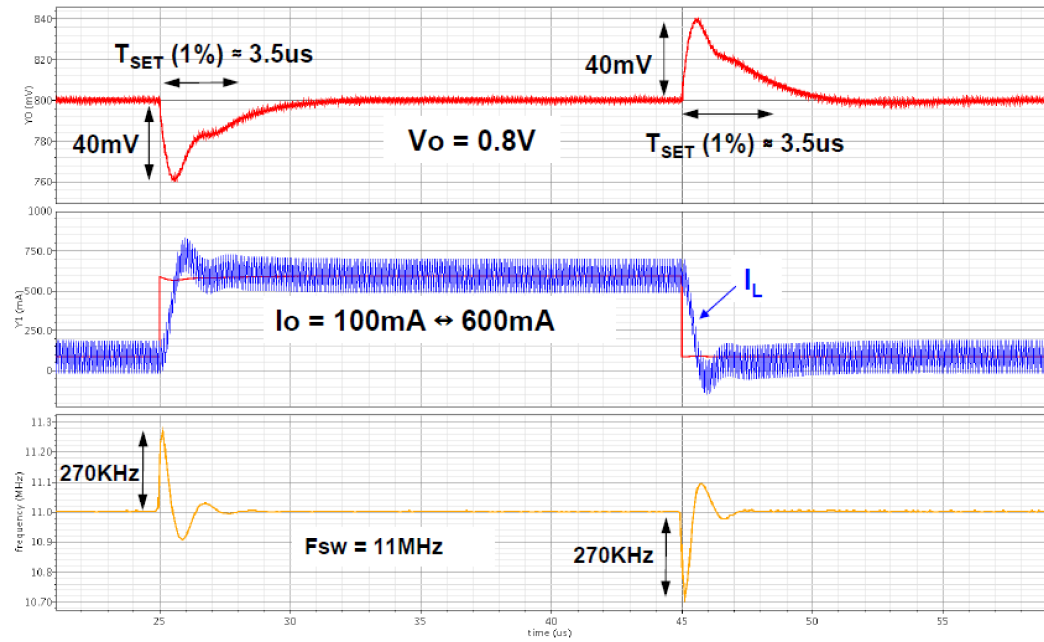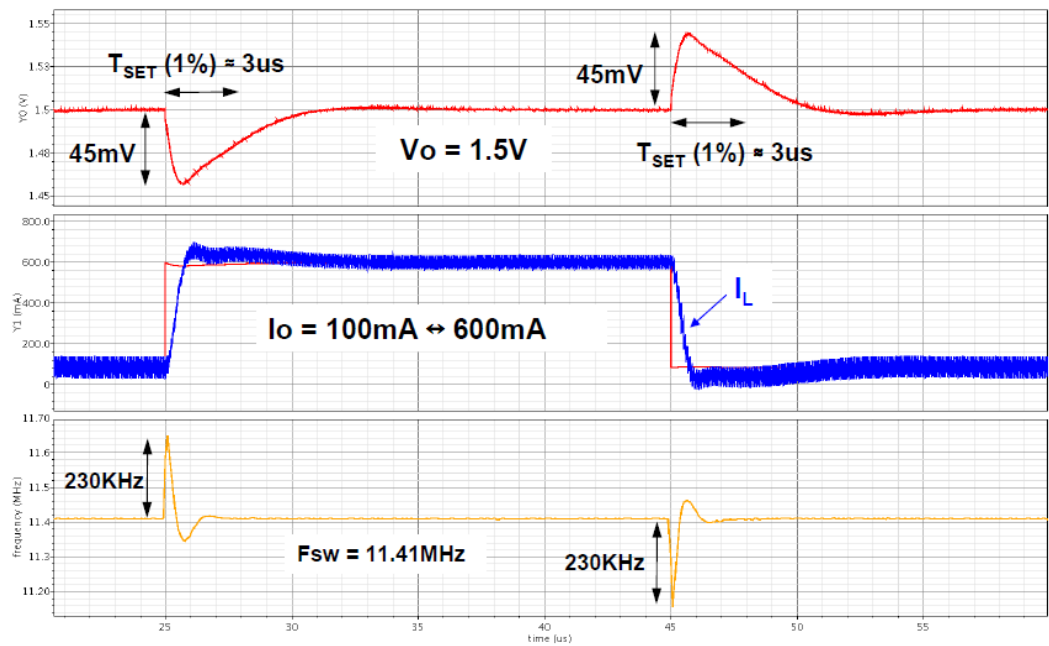Figure 5.22: Transient response at V_O=1.5V, typical process and 27 deg.
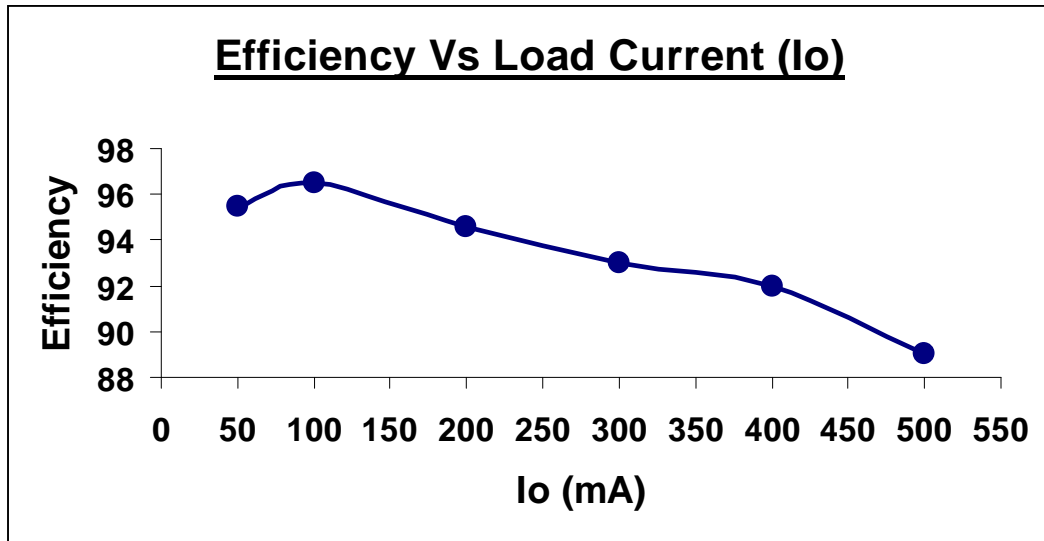
Figure 5.23: Efficiency of the TPWM based buck converter vs load current

sient (ΔI_O). The negative feedback causes decrease in the switching frequency of control phase in order to correct this transient and increases duty cycle of V_{PWM}. If transient is large, the controller misses one edge of the control phase and loses the duty cycle information. The control phase in next clock cycle is highly unpredictable and may even cause the duty to reduce initially before loop forces it back in the correct direction. This might degrade the transient response as shown in Fig. 5.25. Once the cycle slip happens it cannot be corrected so the only way to mitigate the undesired transient is to avoid the cycle slip. This requires to limit the phase difference (duty cycle). In order to achieve this, an early control phase is needed.

The duty cycle limit (DCL) implemented with time domain PWM controller is shown in Fig. 5.26. The PWM and inverted PWM signals are sampled at phases ϕ_{LIM+} and ϕ_{LIM-} respectively. For duty cycle less than 89%, the negative edge of V_{PWM} will always appear before ϕ_{LIM+} hence will be sampled as logic 0. As soon
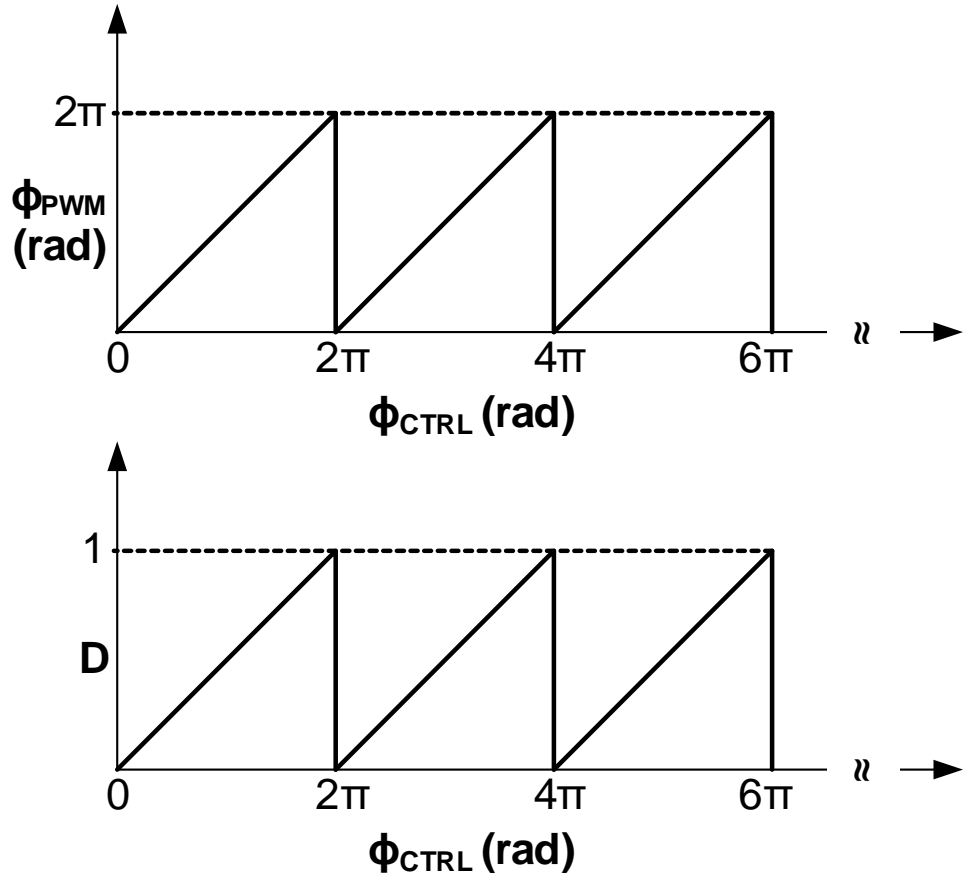
Figure 5.24: Duty Cycle vs phase characteristic of phase subtractor

as duty cycle goes above 89%, the negative edge appears after ϕ_{LIM+} and sampled as logic 1 activating the control signal, D_{LIM}. The timing diagram for maximum duty cycle limit is shown in Fig. 5.27.

Since CCO is a chain of delay of cells, it inherently has multiple phases which could be used for phase limiting. Fig. 5.28 shows a current controlled ring oscillator with 9 stages. The output of 8th delay stage (ϕ_{LIM+} is used to limit the maximum duty cycle at 89%. Similarly the output of 1st stage (ϕ_{LIM-} is used to limit the minimum duty cycle at 11%. In case we want to increase the min-max range of duty cycle, a higher stage ring oscillator can be used.
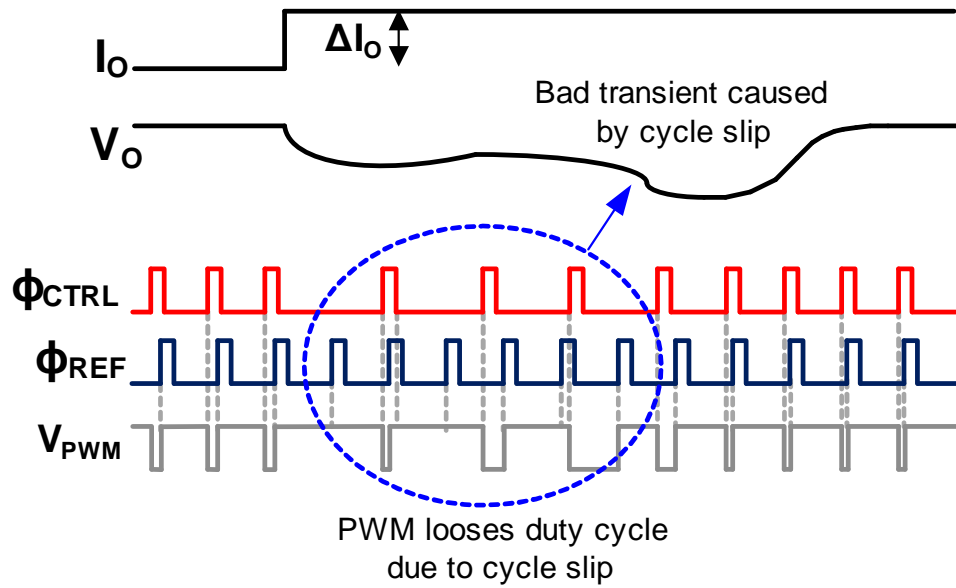
Figure 5.25: Duty cycle slipping in TPWM controller
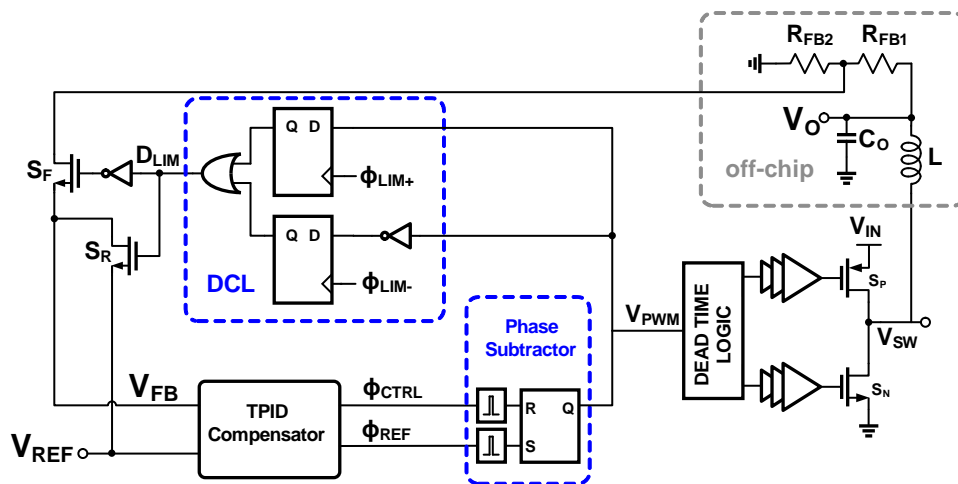
Figure 5.26: Duty cycle limit (DCL) logic implemented with TPWM

Similarly for limiting minimum duty cycle, if duty cycle is more than 11%, the negative edge of V_{PWM} will always appear after ϕ_{LIM-} and sampled as logic 1 (or logic 0 of $\overline{V_{PWM}}$). As soon as duty cycle goes below 11%, the negative edge of V_{PWM} will appear before ϕ_{LIM-} and $\overline{V_{PWM}}$ is sampled as high activating D_{LIM}.
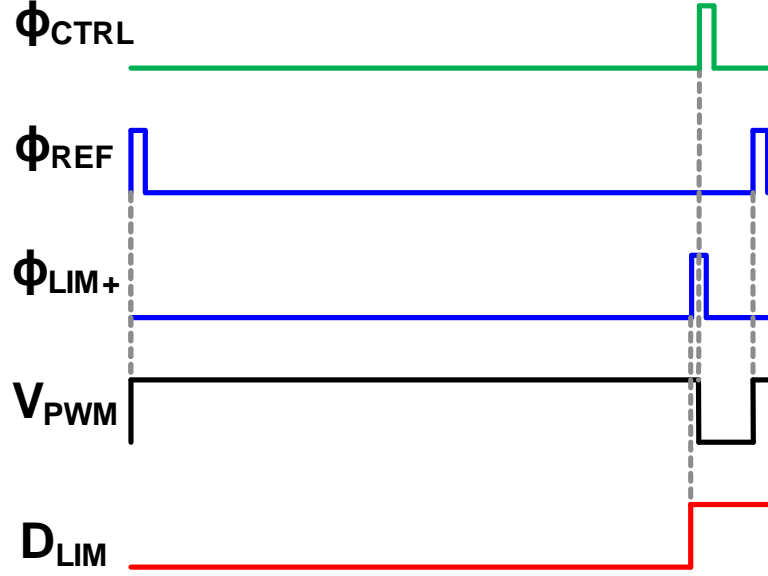
Figure 5.27: Timing diagram showing maximum duty cycle limit
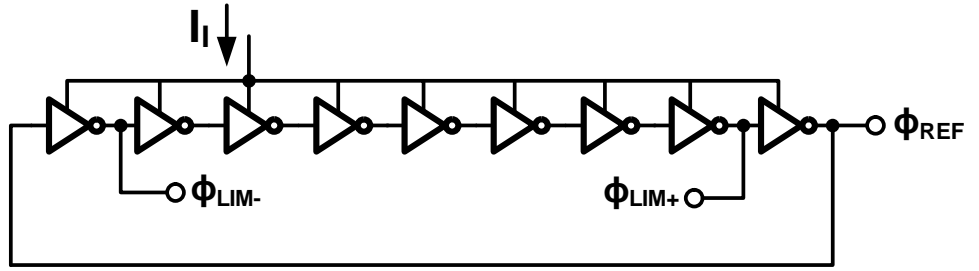
Figure 5.28: A 9-stage ring oscillator

The timing diagram for minimum duty cycle limit is shown in Fig. 5.29.

In order to saturate the phase of CCO and CCDL for limiting duty cycle, feedback is disconnected from V_{FB} and connected to V_{REF} through switches S_F and S_R. This holds the phase of ϕ_{CTRL} at its current value by making the error voltage PID compensator 0.
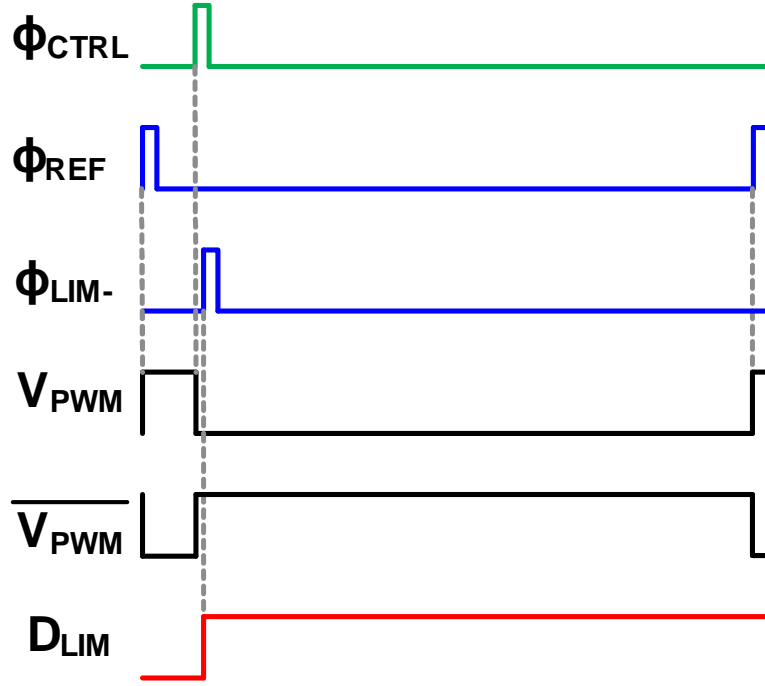
Figure 5.29: Timing diagram showing minimum duty cycle limit

5.8.2 DC offset in output voltage

Another problem with TPWM which cannot be ignored is large dc offset in the output voltage due to mismatch between the frequencies of two CCOs. Unlike in voltage mode integrators where the systematic offset due to transistors mismatch is suppressed by the transconductance, the low gain of phase domain integrator makes the offset due to mismatch appear even larger at the input. This can be easily understood by considering the requirement of K_{VCO} derived in Section 5.5 which is 842 KHz/V. Since CCOs are biased at 10MHz, a 1% mismatch in the two CCOs will cause a frequency difference of $100KHz$. Therefore, according to 842 KHz/V of K_{VCO}, this 100 KHz frequency difference will appear at input as $\frac{100\ KHz}{842\ KHz/V} \approx 118mV$ offset which seems to be quite large. A generalized equation

for offset voltage can be written as:

$$V_{OS} = \frac{\Delta F}{K_{VCO}} \tag{5.36}$$

Where ΔF is the frequency difference between two CCOs due to mismatch. Since input to VCO integrator is V_{FB} which is regulated at V_{REF}, the percentage offset will be:

$$\%V_{OS} = \frac{1}{V_{REF}} \frac{\Delta F}{K_{VCO}} X100\% \tag{5.37}$$

A 0.5%-1% process mismatch is not every uncommon even after ensuring a good matching in the layout. Therefore according to the above expression, this offset can only be reduced either by increasing the K_{VCO} or V_{REF} which are usually fixed by the design as per the specifications of the dc-dc converter. With V_{REF} of 600mV, this offset could be as large as 10% even if we consider only 0.5% mismatch in the CCOs. Such a large offset will defeat all the purpose of voltage regulation and needs to be corrected. Thanks to the phase integrator property of VCO, a very small frequency difference could be detected and corrected by running the integral control in frequency locked loop mode. As shown in Fig. 5.30, the FLL mode is enabled with SRT during startup before enabling the dc-dc converter. During FLL mode, the V_{FB} input to integrator is disconnected and connected to V_{VREF}. Since the error input to integrator is 0, any mismatch in frequencies of ϕ_{I+} and $\phi I-$ will account to mismatch between the CCOs. This frequency error is accumulated in the accumulator and tunes one of the CCOs (or both) to bring them in the locked state (by changing the bias current or delay of the CCOs through D/A converter). Once the CCOs are the tuning bits F_{TUNE} are latched and FLL mode is disabled by making $SRT = 0$ which connect the negative input back to V_{FB}.
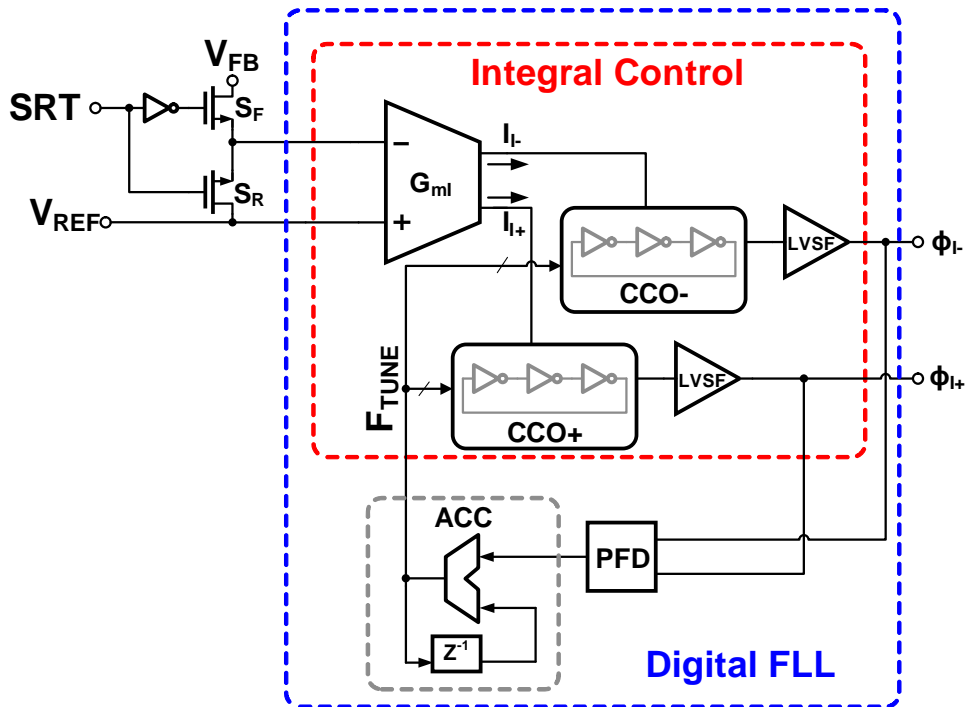
Figure 5.30: Offset correction by using VCO integrator in FLL

Since the offset calibration is performed only during startup, it does not affect the normal operation of the converter. This technique also has an inherent advantage that is to correct the offset of transconductance amplifiers as well. Since any mismatch in the offset of Gm will introduce a frequency error in the CCOs, this offset is automatically canceled when offset calibration is performed in the FLL mode. The only shortcoming of the technique is that it cannot be operated in the background while converter is running. However, the technique is still quite effective considering that the process mismatch is fixed and should not change with the temperature and voltage variation.

An alternate method which can run at the background is shown in Fig. 5.31. Instead of comparing the frequencies, the error voltage is detected in a comparator and accumulated bits are are used to tune the frequency of CCO. If we ensure

that the accumulator is slow enough not to interfere with converter operation then it will always track the steady state error and correct it in the background. The offset correction here is limited by the comparator offset so a low offset comparator must be used.
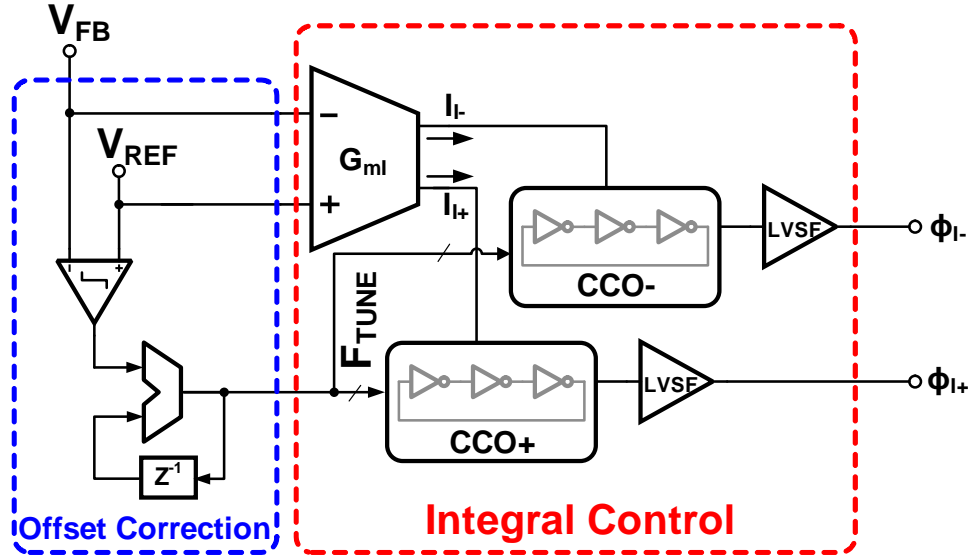
Figure 5.31: Offset correction using a comparator

It should be noted that any mismatch between the CCDLs needs to be corrected as it will not accumulate the phase. Any error in the duty cycle due to mismatch in CCDLs will be corrected by the feedback loop as integral control will always force $V_{FB} = V_{REF}$.

5.9 Future Research

With the capability of running at much higher speed and very low power consumption, the TPWM provides a new opportunity in the field of dc-dc converter. Though, the concept was verified only with a single phase voltage mode

converter but can be easily extended to multi-phases. The use of voltage/current controlled ring oscillator does not require any extra circuitry to generate multiple phases while in case of a conventional ramp based analog PWM controller, it requires as many ramp signals as number of phases. Also the reset time associated with each ramp signal limit the number of phases when running at higher speed. On the other hand, the inherent multiphase nature of the ring oscillator can be exploited to design a converter with many phases. The only extra blocks needed will be a CCDL and a phase subtractor to generate a separate PWM signal for each phase. The concept is demonstrated in Fig. 5.32 with the realization of a 5-phase. This can be extended to many phase by increasing the number of delay elements in the ring oscillator and adding a CCDL and phase subtractor for each extra phase.
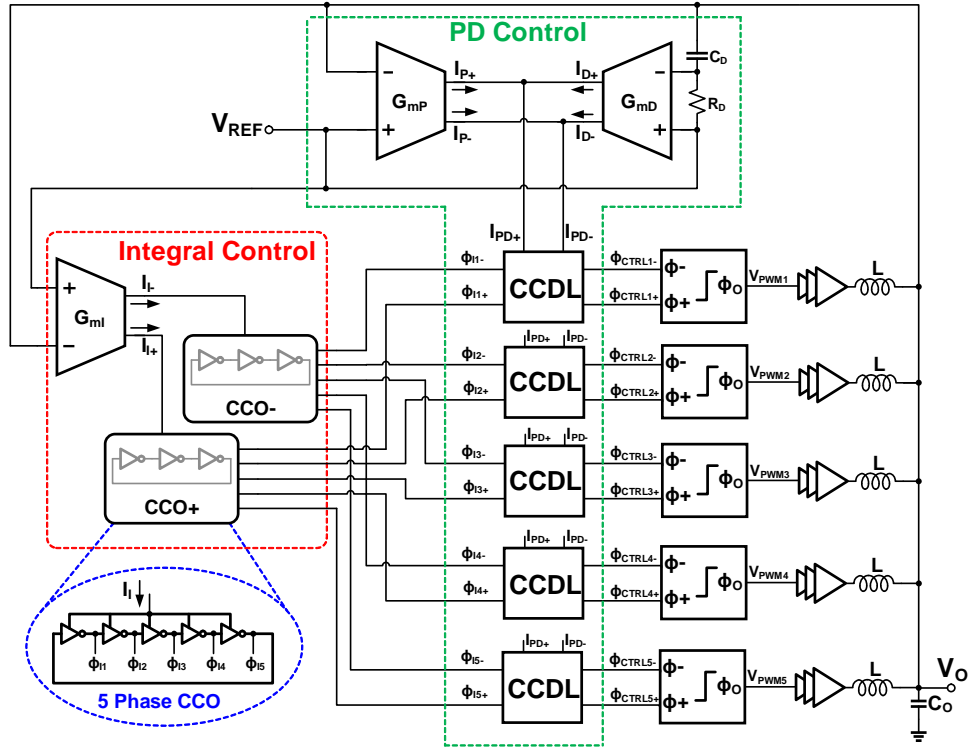
Figure 5.32: A multi-phase buck converter using TPWM

Another research prospect is to explore the TPWM concept in a current mode control. Design of a current sensor using time based signal processing could be the starting point. The TPWM concept could also be explored with other converter topologies such as boost and buck-boost. Implementation of PFM mode in TPWM to improve the light load efficiency is another topic which could also be explored.

CHAPTER 6. CONCLUSION

Several digitally assisted control techniques for switching dc-dc converters were explored in this research work. The proposed techniques were proved to be highly effective to resolve the issues of conventional controllers.

A buck-boost converter based on constant ON/OFF time fractional-N digital control was presented which solves the mode transition issue between buck and buck-boost. Hybrid hysteretic controller comprising of both voltage and current mode is proposed with a scheme for regulating the switching frequency to get the fixed frequency operation. The digital frequency regulation utilizes switched-R fine control to alleviate the high resolution requirement of digital-to-analog converter. Both the designs were successfully implemented and verified on the silicon.

The concept of a time based PWM controller using time domain signal processing was introduced for implementing high speed switching converters. A proportional-integral-derivative (PID) compensator was realized in time domain using voltage controlled oscillators (VCO) and voltage controlled delay lines (VCDL). Detailed design procedure of a 10MHz buck converter was presented.

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