cally varies as,

$$C_D = \frac{C_0}{\sqrt{1 + \frac{|V_D|}{\Phi_i}}} \tag{2.1}$$

where Φ_i is the built in potential of the diode and C_0 is the capacitance with zero bias. Figure 2.2 shows how the capacitance varies with the bias voltage. It can be seen that the capacitance is highly non-linear and hence it is advisable to keep the photodiode bias variation to a minimum.

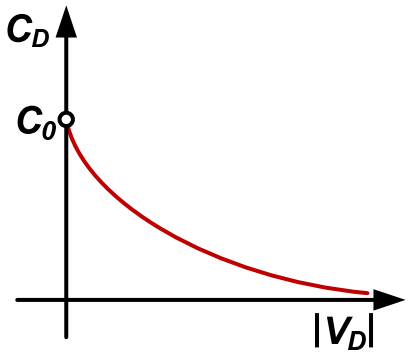

Figure 2.2: Junction capacitance variation for the diode.

Figure 2.3 shows a generic electrical model of such a photodiode sensor. R_{SH}

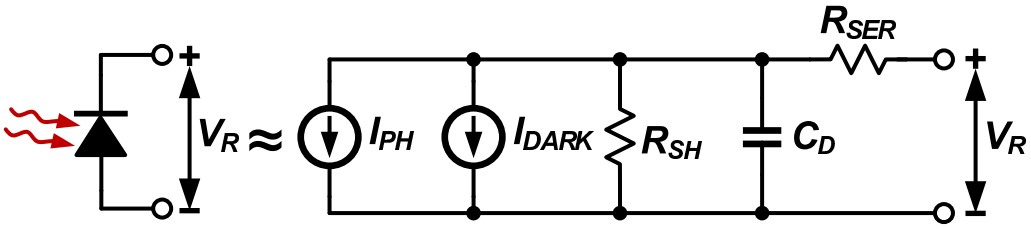

Figure 2.3: Electrical model of a photodiode sensor.

is the shunt resistance which represents the variation of the diode current with applied bias and R_{SER} is the bulk resistance of the diode. With sufficient reverse

bias, R_{SH} is usually of the order of hundreds to thousands of MΩ and R_{SER} is of the order of a few Ω and hence both of them can be safely ignored for design. Dark current is an offset in the conversion process and there are ways to cancel this offset in system level [6]. Consequently, this kind of sensor can be treated as a current source with a non-linear capacitance across it. Even for other types of sensors, for example a piezoelectric sensor, modeling it as a current source (or charge source) with a capacitance across it is a fair assumption without loosing much accuracy [7].

2.2 Current Sensing Digital Readout Circuits

This section discusses various existing current sensing digital readout architectures and briefly describes their advantages and disadvantages. It is assumed the electrical model of the sensor element is as shown in Figure 2.3 irrespective of the type of the sensor.

2.2.1 Transimpedance Amplifier

Transimpedance amplifier (TIA) is used to convert a low level input current to a reasonably high voltage output. A closed loop TIA is essentially a high gain opamp with a large feedback resistor. Figure 2.4 shows the block diagram of a closed loop TIA. The opamp in feedback makes the sensor node, V_C, a virtual ground and the input current is fully diverted to the output. The bias for the sensor is also easily obtained from the virtual short. The voltage domain ADC converts the output

voltage to a digital word, D_{OUT}.

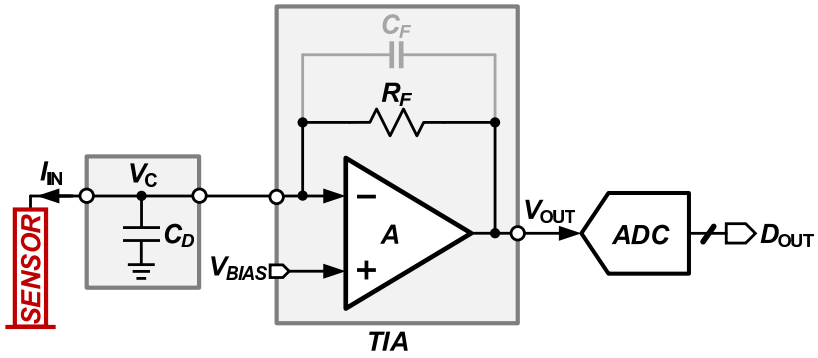

Figure 2.4: Architecture of transimpedance amplifier based readout circuit.

For small signal calculations, TIA looks like a differentiator circuit with large noise gain at high frequency. Hence, a feedback capacitance, C_F, is almost always used to limit the bandwidth of the system. The DC gain of the TIA can be easily calculated as

$$\frac{\mathrm{V_{OUT}}}{\mathrm{I_{IN}}} = \mathrm{R_F} \tag{2.2}$$

The capacitance of the sensor is shown separately for a simpler analysis. In reality the input capacitance of the opamp also contributes to an extra capacitance at the sensor node.

The feedback resistance, R_F, usually consumes large area and the opamp consumes a large current to meet the stability, noise and offset specifications. In addition, the architecture being analog in nature, is not very friendly for process scaling. One advantage of this architecture is that the gain is fairly independent of the sensor capacitance and since the swing at the virtual node is small, the capacitance non-linearity does not affect the performance much. However, for stability,

the total sense node capacitance, feedback resistance, and amplifier bandwidth have to be optmized carefully.

2.2.2 Dual Slope ADC Architecture

Dual Slope ADC belongs to a category of ADC architectures known as "Integrating ADCs" where the output represents the integral of the input over a fixed time period [8]. Figure 2.5 shows the architecture of a dual slope ADC which processes

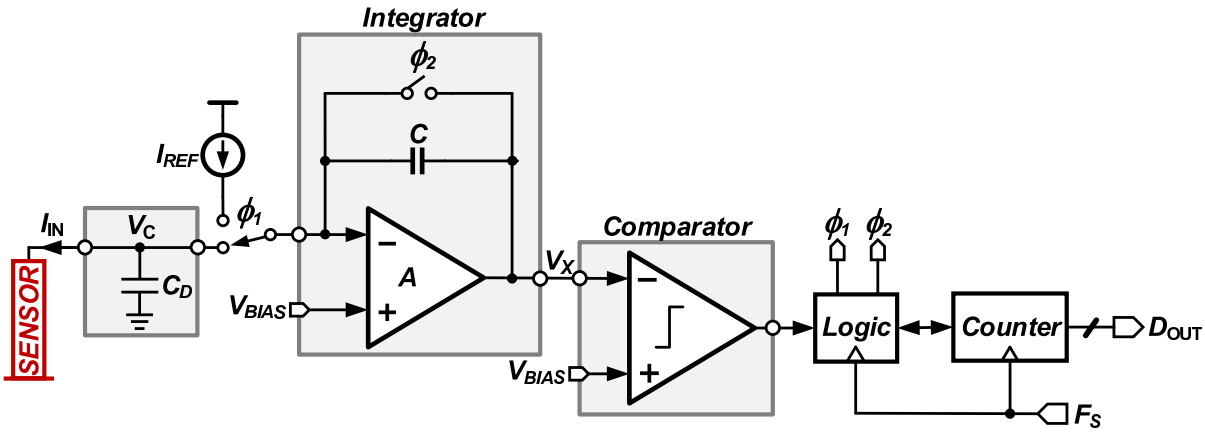

Figure 2.5: Architecture of a Dual Slope ADC based readout circuit.

a current input. The dual slope operation can be easily understood from the integrator output waveform shown in Figure 2.6. There are mainly two phases of operation in a dual slope architecture. In the first phase, the input signal is integrated for a fixed number of clock cycles (usually obtained from an accurate clock source). In the second phase, the integrated output is discharged down using a fixed reference until the comparator output trips. It can be seen the number of clock pulses counted during the second phase is a digital measure of the input. In

some implementations, the first phase might include an auto zero phase where the offset within the system is nulled out. It can be shown that [9] that the number

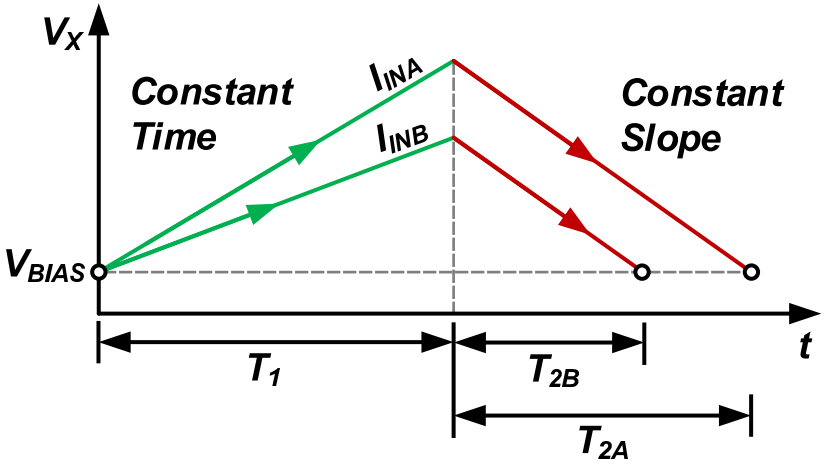

Figure 2.6: Transient waveforms in Dual Slope ADC based readout circuit.

of clock cycles in second phase (T_2) is related to the input signal as,

$$T_2 = T_1 \frac{I_{IN}}{I_{REF}} \tag{2.3}$$

In a dual slope operation, the output does not depend on the feedback capacitance value assuming the value does not change during a single conversion. However, the value of integration capacitance has to be chosen depending on the input current range and clock frequency such that a reasonable value of V_X is obtained without clipping. This makes sure that the noise effects are minimized and the dynamic range of the ADC is maximized. The conversion speed of such an ADC has a strong dependence on its resolution. For an N bit converter, the

worst case conversion time will be,

$$T_{CONV} = 2^{N+1}T_S \tag{2.4}$$

where T_S is the clock time period. It can be seen that the integrate and self reset behavior of this ADC produces a sinc filtering [9]. So by choosing T_1 carefully, the undesirable components like the power supply ripple (at 60Hz) can be significantly attenuated. Figure 2.7 shows the null locations in the magnitude response of the ADC. In a practical design, errors including capacitor droop due to finite leak-

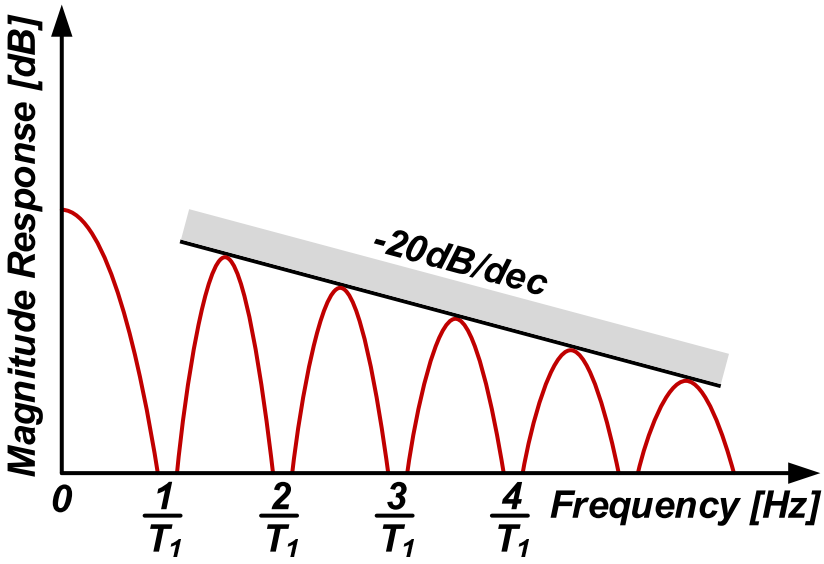

Figure 2.7: Magnitude Response of a Dual Slope ADC.

age, charge injection, non-linearity of integrator and capacitor, and high frequency limitations of the integrator and comparator, need to be accounted for. Design of such integrator opamps and comparators is still a challenge in fine processes.

2.2.3 CMOS Image Sensor Architecture

Figure 2.8 shows a typical CMOS image sensor architecture. In image sensor terminology, this architecture is called an Active Pixel Sensor (APS) because of the presence of an active buffer in the pixel. There are Passive Pixel Sensors (PPS) as well but recent CMOS image sensors employ APS due to its improved performance [1], [10]. The operation of the circuit is demonstrated in Figure 2.9.

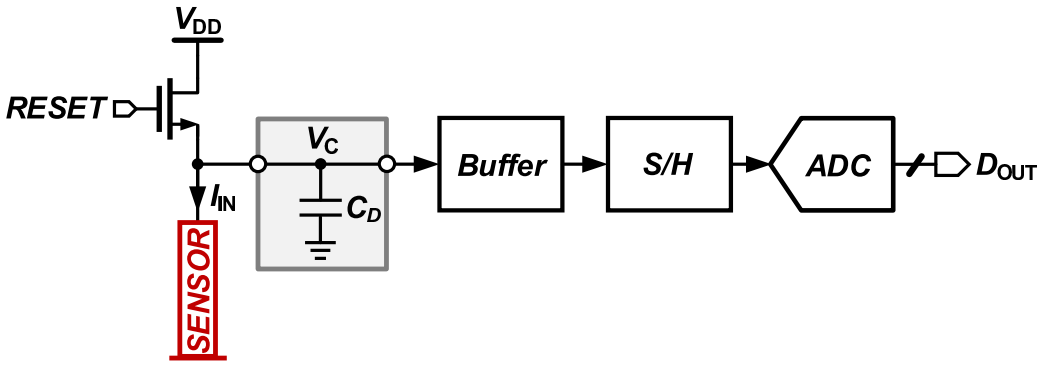

Figure 2.8: CMOS Image Sensor Architecture.

Initially, the sense node, V_C, is reset to a voltage typically close to the supply. After the reset phase, the input sensor current discharges the total capacitance at the sense node for a finite duration with a rate determined by the input current. A sample and hold circuit then samples the voltage at the end of conversion phase which is proportional to the input current. Finally, an ADC converts this sampled voltage into its digital equivalent.

The total capacitance at the sense node includes the sensor capacitance (C_D), input capacitance of the buffer and the parasitic capacitance of the reset transistor. Since the voltage at end of conversion depends on the rate of discharge, the front

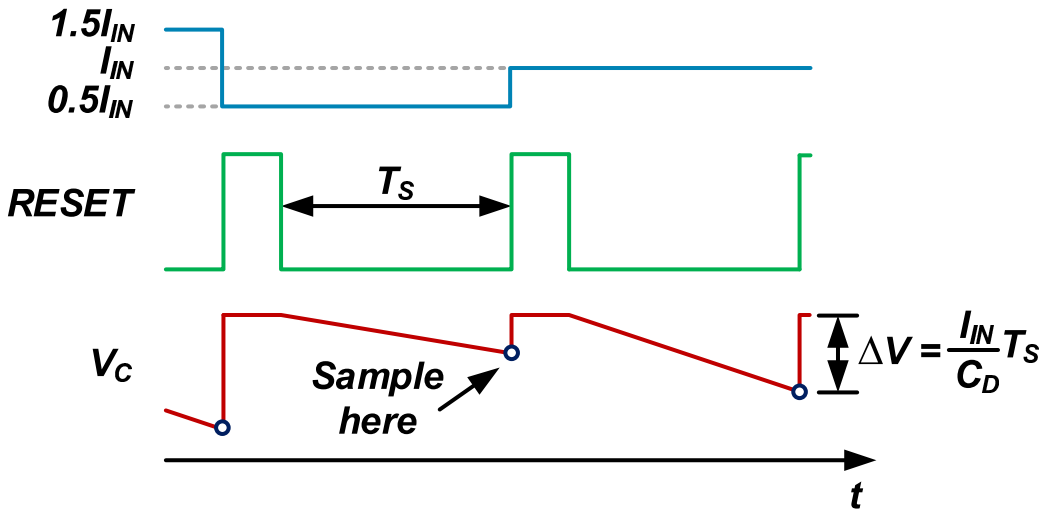

Figure 2.9: RESET and sense node voltage waveforms.

end gain ($\frac{\Delta V}{I_{IN}}$) is dependent on the exact capacitance value. As the voltage swing across the non-linear sensor capacitance changes during a conversion, the effective capacitance is difficult to calculate which results in gain error. More importantly, the variation of C_D with V_C (which in turn is proportional to I_{IN}), leads to an input dependent gain which results in non-linearity. For high dynamic range applications, the conversion time has to be small enough not to saturate the output level but large enough to efficiently use the maximum input range for the ADC.

2.2.4 Pulse Frequency Modulation Architecture

The Pulse Frequency Modulation (PFM) architecture is a technique that is used in many CMOS image sensors to achieve a large dynamic range [5]. Figure 2.10 shows a block diagram of the PFM architecture. Assuming OUT initially goes from 0 to V_{DD}, the sensor current discharges C_D at a constant rate from V_{DD}. Once the sense

voltage crosses V_{BIAS}, the comparator output goes to 0 and resets the sense node again after a very small delay. This results in a self-oscillating structure where the oscillation frequency is controlled by the input current. If the input current increases, the time required for the comparator to trip decreases and the frequency of the comparator output waveform increases linearly. Therefore, if the reset time is small enough, the frequency of the output waveform is linearly proportional to the input current. The comparator output is processed by a Frequency to Digital (FDC) converter which gives out the digital output. Figure 2.11 shows the transient

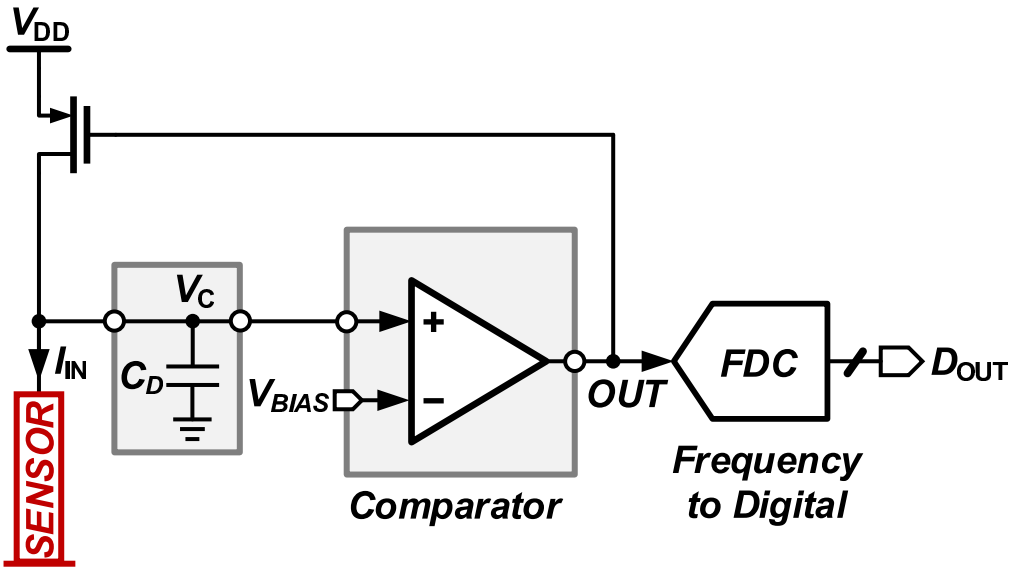

Figure 2.10: Pulse Frequency Modulation Architecture.

waveforms in the PFM circuit with different DC input currents. The frequency at the output of the comparator with a finite reset time is given by,

$$F_{OUT} = \frac{1}{\frac{C_D(V_{DD}-V_{BIAS})}{I_{IN}} + T_{RST}} \tag{2.5}$$

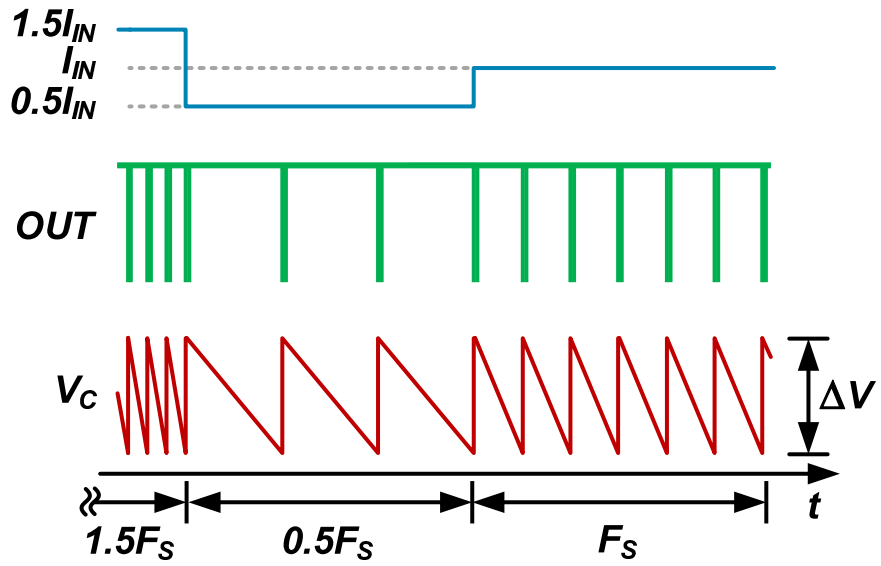

Figure 2.11: Transient waveforms in Pulse Frequency Modulation Architecture.

where T_{RST} is the finite reset time. Reset time mainly includes delays in the comparator and the reset switch. It can be seen that if the T_{RST} is small, the output frequency is linearly proportional to the input current. Figure 2.12 shows the frequency of output vs. the input current. It can be seen that for a large input current, the output frequency saturates to a value dictated by the reset time.

Getting a higher dynamic range from the PFM architecture translates to accurately measuring small to large frequencies. Since FDC can be implemented as a simple counter, extending the counter width (area) is the only penalty in getting more dynamic range. Also since the output frequency scales with the input, the dynamic power consumption also scales with the input current. However, the gain in the conversion process has a strong dependence on the capacitance value. The non-linearity in conversion is significantly reduced compared to the APS architec-

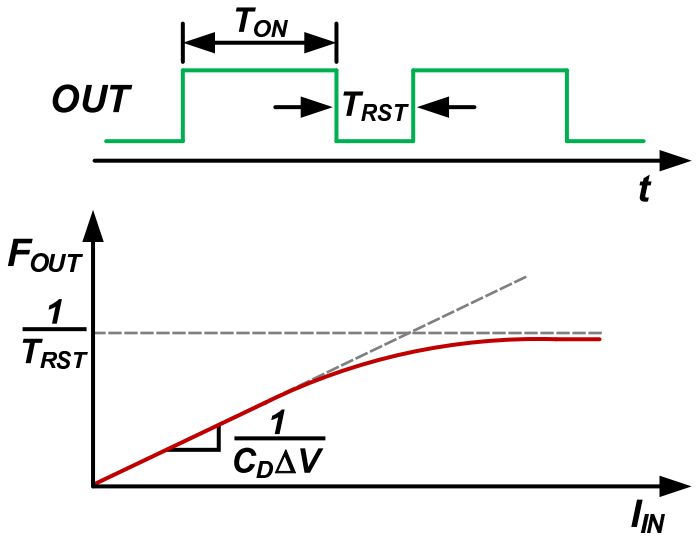

Figure 2.12: Output frequency vs. input current.

ture as the input current does not change the average voltage across the non-linear capacitance. The design of a low power high speed comparator (or zero crossing detector) is still non-trivial with the reduced supply and gain in fine processes.

CHAPTER 3

ARCHITECTURE DESIGN

VCO based ADCs (VCO based Quantizers) [11] have recently emerged as power efficient ADC architectures for many applications. They take advantage of the improved time resolution in finer technology nodes and open loop noise shaping [12]. Circuit techniques to tackle the degradation in performance due to the non-linearity of VCOs are described in [13–15]. Almost all of these designs were implemented for high bandwidth applications with large clock frequency. After a brief overview of the VCO based ADCs, this chapter discusses the proposed digital sensor readout circuit where a VCO based ADC architecture specifically suited for very low bandwidth applications, is used.

3.1 Overview of the VCO Based ADCs

Figure 3.1 shows the conceptual diagram of a VCO based ADC. The input analog voltage, V_{IN}, is converted to a frequency information, F_{OUT}, using a voltage controlled oscillator (VCO). By counting the number of VCO cycles in a fixed time

period, we can get an accurate measure of the VCO frequency. This is implemented using a block called a frequency-to-digital converter (FDC) which converts the frequency information to its digital equivalent. Since the VCO frequency itself is proportional to the analog input, we can see that the digital output represents the analog input to the VCO. Typically, VCOs are implemented using supply controlled or current starved ring oscillators (discussed later).

3.1.1 Small Signal Model

An equivalent small signal block diagram of a VCO based ADC is shown in Figure 3.2. Since the VCO integrates phase continuously (phase is time integral of frequency), it is shown as a continuous time phase integrator where K_{VCO} is the gain (sensitivity) of the VCO in Hz/V. The FDC can be implemented as a phase quantizer or a frequency quantizer. For the purpose of demonstrating noise shaping easily, it shown here as a phase quantizer. The phase is quantized at a sampling rate, F_S. Digital version of the frequency is obtained by passing the quantized phase through a digital differentiator $(1 - z^{-1})$. It can be seen that the

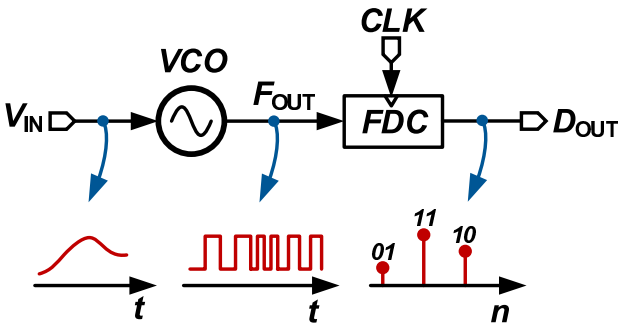

Figure 3.1: Conceptual block diagram of a VCO-based ADC.

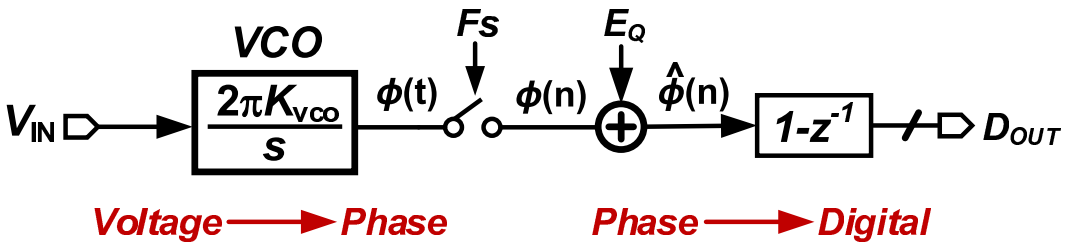

Figure 3.2: Equivalent small signal block diagram of a VCO ADC.

quantization noise, E_Q, gets first order noise shaped as it goes through the digital differentiator. Hence the noise transfer function, NTF of the VCO-based ADC is,

$$\mathrm{NTF}(z) = 1 - z^{-1} \tag{3.1}$$

For frequencies much smaller than the sampling rate, the digital differentiator performs the exact inverse of a continuous integration. Thus the signal transfer function (STF) is just a gain as the signal gets first integrated and then differentiated later in the digital domain. Another advantage of a VCO-based ADC is that it has inherent anti-aliasing much like a continuous time $\Delta\Sigma$ modulator since the signal travels through an integrator before it gets sampled and quantized [16].

For high bandwidth applications, the VCO frequency and the clock frequency are of similar magnitude (usually $\max[F_{VCO}] \approx \frac{F_S}{2}$) and a phase quantizer with a high speed differentiator is used for frequency detection. If input bandwidth is small, a low frequency clock (hundreds of kHz) can be used for saving power. However, using a phase quantizer based approach to extract frequency would necessitate low VCO frequency which is not easy to achieve when implemented with ring oscillator chains with a reasonable K_{VCO} value. In such a case, a counter

based FDC can be implemented as discussed in next section.

3.1.2 Counter Based Frequency Detection

Figure 3.3 shows a practical implementation of a VCO based ADC for low sampling rates. The VCO is implemented as a ring oscillator with 5 stages. The input to

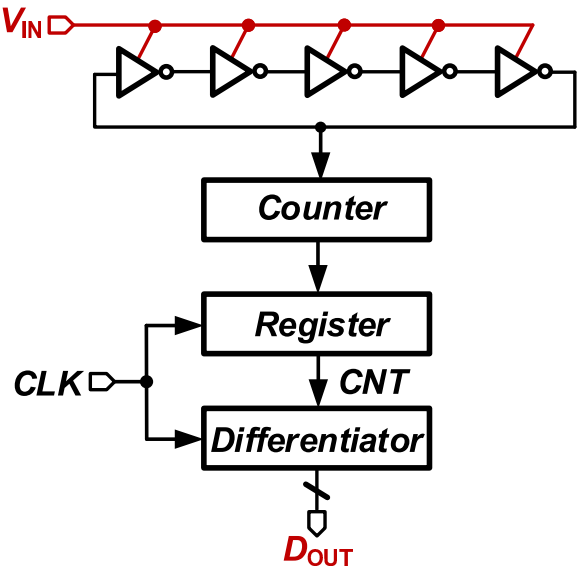

Figure 3.3: Implementation of a VCO based ADC for low sampling rates.

the VCO is the inverter supply itself and the delay of each inverter is dependent on the supply. Hence the output frequency is dependent on the input, though in a non-linear fashion. On every positive edge (or negative) of the VCO output, counter increases its count by one and the register stores the count at the end of the clock cycle. The stored count is a measure of the accumulated phase at the end of that clock cycle. A digital differentiator is used to subtract the stored count values at the end of two consecutive cycles. This gives out the frequency

information in digital representation. In such an implementation, the counter does not have to reset every clock cycle and thus the detrimental effects of finite reset time on noise shaping is eliminated.

Without a reset for the counter, the output of the counter will overflow after

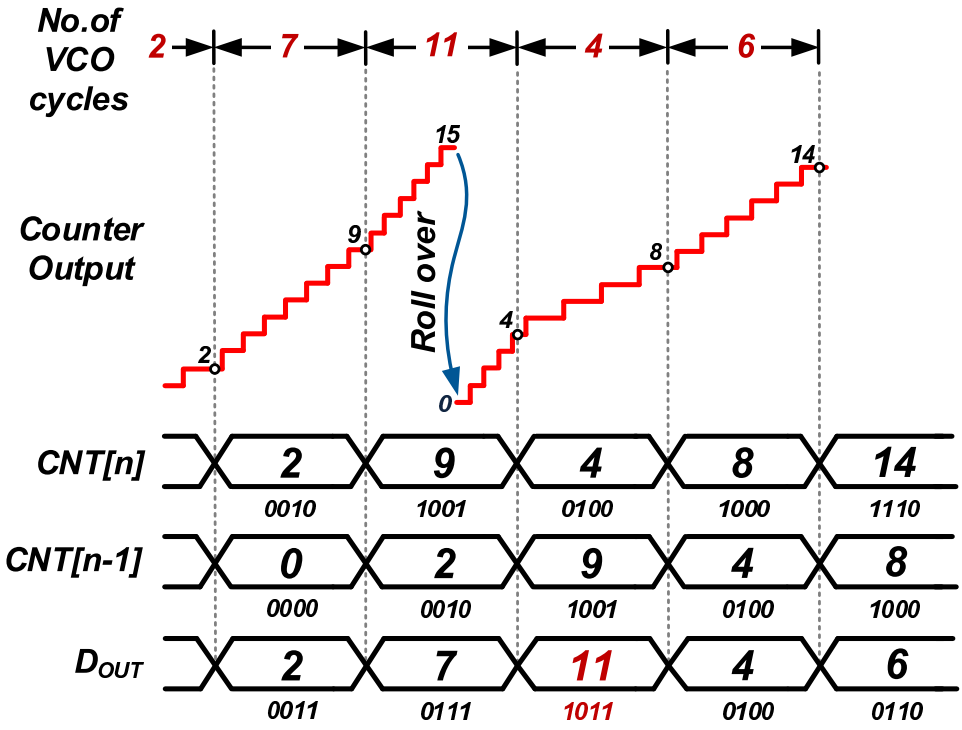

Figure 3.4: Counter with phase wrapping logic

it reaches its highest count. This does not pose a problem if there is only one overflow within a clock cycle, provided 2's complement phase wrapping logic is used. Figure 3.4 shows an example where the 2's complement subtraction is able to retrieve the right frequency output inspite of an overflow. In this example, $D_{OUT} = 11$ represents the case where the digital output is correct even though there was an overflow. Note that there is one clock delay in output due to the

presence of a sampling register.

3.1.3 Gain of a VCO based Quantizer with Counter based FDC

Gain of a VCO based quantizer with counter based frequency detection can be obtained from the small signal diagram shown in Figure 3.5. Since the counter

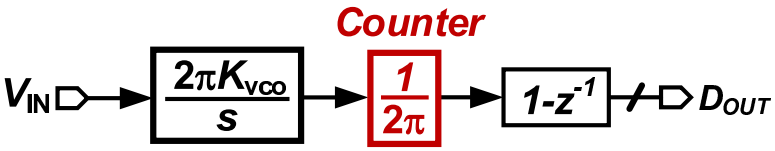

Figure 3.5: Small signal model of VCO based quantizer for gain calculations.

increments its output code by 1 for every 2π radian change in its input, the counter gain is given as $\frac{1}{2\pi}$ (code/radian). The digital differentiation can be written as a continuous time differentiation,

$$1 - z^{-1} = 1 - e^{-sT_s} \tag{3.2}$$

where T_S is the clock period. For frequencies much smaller than the clock frequency,

$$\begin{aligned} 1 - e^{-sT_S} &= 1 - (1 - sT_S + \frac{(sT_S)^2}{2!} + \dots) \\ &\approx sT_S \end{aligned} \tag{3.3}$$

Thus the gain of a VCO based quantizer with counter based FDC becomes,

$$A_{VCOQ} \approx K_{VCO} T_S \tag{3.4}$$

To get more insight into the range of values for the gain, we can look at a typical implementation of a current starved ring oscillator as a VCO. This implementation is shown in Figure 3.6. The control voltage, V_C, generates a proportional current,

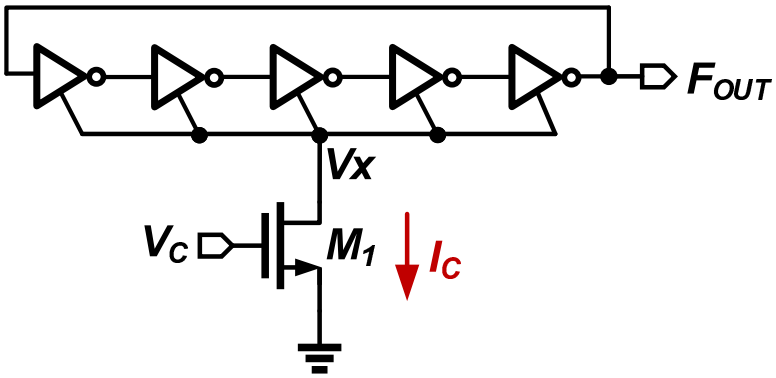

Figure 3.6: nMOS controlled current starved ring oscillator VCO

I_C, which determines the inverter delay. When V_C increases, the current available to discharge the inverter load capacitance, C_L, increases, which reduces the inverter delay or increases the VCO frequency. Let us consider an $N+1$ bit counter used for the frequency detection such that when the VCO is oscillating with maximum frequency, the FDC gives out a code $= 2^{N+1}$. Assuming the center frequency of VCO is half its maximum frequency, we can write the frequency of the VCO for very small input as,

$$F_{VCO} = 2^N F_S \tag{3.5}$$

Assuming the delay of the inverter is proportional to the time required for C_L to discharge from the supply, V_{DD}, we can write

$$F_{VCO} = \alpha \frac{I_C}{C_L V_{DD}} \tag{3.6}$$

where I_C (assuming long channel equations are valid) is given by,

$$I_C = \beta (V_C - V_T)^2 \tag{3.7}$$

Therefore up to a first order approximation, we can write F_{VCO} as,

$$F_{VCO} = \gamma (V_C - V_T)^2 \tag{3.8}$$

The sensitivity (gain) of the VCO, K_{VCO}, then becomes,

$$K_{VCO} = \frac{\partial F_{VCO}}{\partial V_C} = \frac{2F_{VCO}}{V_C - V_T} \tag{3.9}$$

Equation 3.9 shows a strong dependence of K_{VCO} on the frequency of oscillation. So we cannot get arbitrarily large values of K_{VCO} for a fixed value of F_{VCO}. The gain of the VCO quantizer then becomes,

$$A_{VCOQ} = \frac{2^{N+1}}{V_C - V_T} \tag{3.10}$$

For $N = 4$ and $V_C - V_T = 800\text{mV}$, we have $A_{VCOQ} = 40$. In practical designs, the nMOS transistor might be degenerated for improving noise and linearity. In such

cases and cases where parallel current sources are used across M1 for increasing the center frequency, the gain will be much smaller than the value predicted by Equation 3.10.

A VCO based quantizer with its open loop noise shaping, anti-aliasing property, and performance improvement in finer process, comes out as a power efficient architecture for a digital sensor readout circuit. However, the small DC gain of such an architecture limits the performance when used in a high dynamic range application with a wide range of bias voltages for the sensor. Next section describes an architecture where a method to get infinite DC loop gain for a VCO based ADC operating at low sampling rates, is proposed. The architecture also makes efficient use of the implicit sensor capacitance to get the required performance.

3.2 Proposed Architecture

The conceptual block diagram of the proposed VCO-based sensor current readout circuit is shown in Figure 3.7. A passive integrator, H(s), which is the implicit sensor capacitance, integrates the error current $I_{IN} - I_{DAC}$ and generates voltage V_C. A VCO-based quantizer (VCOQ) digitizes the difference between V_C and the desired sensor bias voltage, V_{BIAS}, and generates digital output, D_F. Because VCOQ exhibits first-order noise shaping, quantization error, E_Q, is shaped by a second-order noise transfer function, thanks to the additional order provided by H(s). While this adequately suppresses E_Q, because of the finite gain of VCOQ, V_C is not forced to be equal to V_{BIAS} in steady state. To circumvent this bottleneck, a

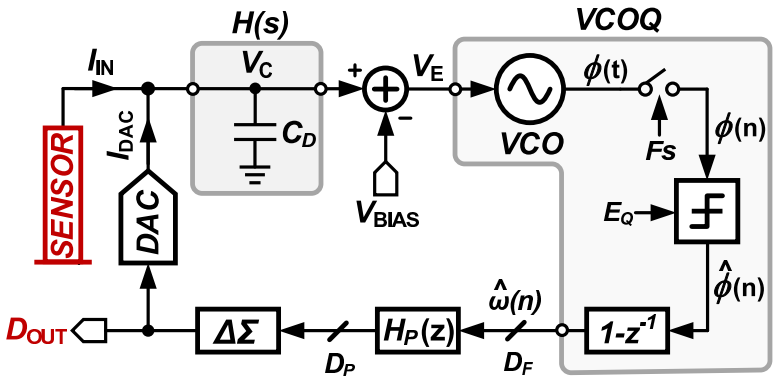

Figure 3.7: Conceptual block diagram of the proposed readout circuit.

digital filter $H_P(z)$ is proposed as shown in Figure 3.7, to provide infinite DC gain so that $V_C = V_{BIAS}$. $H_P(z)$ can be implemented as a simple IIR filter as discussed later. By suppressing variations in V_C, $H_P(z)$ also helps suppress VCOQ non-linearity. To ease hardware complexity, the feedback DAC is implemented using $\Delta\Sigma$ architecture, wherein the digital word (D_P) is first truncated before feeding it to a low-resolution DAC.

3.3 Detailed Architecture

The detailed architecture of the current readout circuit is shown in Figure 3.8. Leveraging the sensor's intrinsic capacitance, passive integrator is realized by feeding the error current, $I_{IN} - I_{DAC}$, into the sense node. The passive integrator capacitance, C_D, includes sensor capacitance and any extra capacitance added at the sense node to minimize ripple on V_C. The VCO is implemented as a cascade of an open-loop transconductor (G_M) and a current-controlled ring oscillator (CCO).

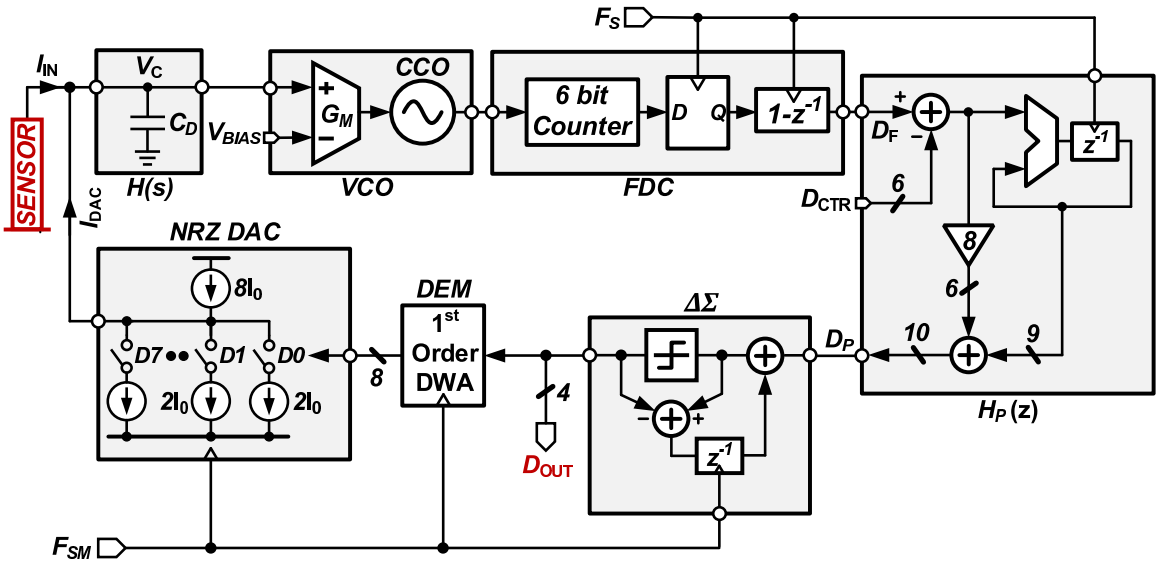

Figure 3.8: Detailed Architecture of the proposed readout circuit.

A Counter-based FDC digitizes VCO output frequency by taking the difference between the number of VCO cycles in two consecutive rising edges of a 160kHz sampling clock, F_S. The $1 - z^{-1}$ block is implemented using two's complement arithmetic, which ensures automatic phase wrapping and obviates the need for resetting the counter on every clock cycle. The FDC output, D_F, is filtered by $H_P(z)$ and fed back to the input through the $\Delta\Sigma$ DAC.

Filter $H_P(z)$ is implemented by an accumulator and a feed-forward path across it. Accumulator provides the high gain needed to force $V_C = V_{BIAS}$ in steady state and the feed-forward path stabilizes the feedback loop that is otherwise unstable because of the presence of two integrators. The feed-forward path gain is set to 8 considering the trade off between the accuracy of V_C and modulator stability. The digital code corresponding to the center frequency of VCO, D_{CTR}, is subtracted

from the FDC output to prevent the accumulator from saturating.

Because $H_P(z)$ output is 10-bit wide in this work, a feedback DAC with more than 1000 levels is needed. Such a DAC occupies a large area and requires very small unit elements that are difficult to implement. For instance, the unit element of a 10-bit thermometric current-mode DAC with 4μA full-scale current is only 4nA. To overcome these issues, $H_P(z)$ output, D_P, is truncated to 9 levels using a first-order $\Delta\Sigma$ modulator, implemented using error-feedback architecture. The 9 levels are converted to current using a non-return to zero (NRZ) bipolar current-mode feedback DAC. Dynamic element matching (DEM) is used to suppress the DAC mismatch errors. For the truncation error to have negligible impact on the sensor performance, the $\Delta\Sigma$ modulator clock, F_{SM}, is set at 2.56MHz ($\gg F_S = 160$kHz). Performance degradation due to the excess loop delay in the feedback path is negligible as the clock period ($\frac{1}{F_S}$) is very large compared to the delay ($\approx \frac{1}{F_{SM}}$).

3.4 Small Signal Model

The continuous time (CT) small signal model for the proposed readout circuit is shown in Figure 3.9. The differentiator block has been replaced by sT_S. The DAC and $\Delta\Sigma$ blocks are denoted by their gains G_{DAC} and $G_{\Delta\Sigma}$ respectively. $H_P(s)$ is the CT equivalent of $H_P(z)$. We can identify mainly three important transfer functions from this model. First, the gain from input current to output digital code given

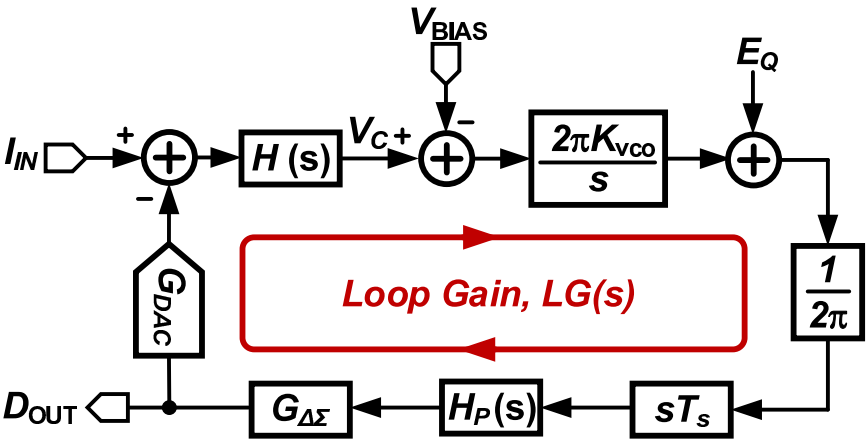

Figure 3.9: Small signal model of the proposed readout circuit.

as,

$$\frac{\mathrm{D_{OUT}}}{\mathrm{I_{IN}}} = \frac{1}{\mathrm{G_{DAC}}} \frac{\mathrm{LG(s)}}{1+\mathrm{LG(s)}} \tag{3.11}$$

Second, the sensitivity of $\mathrm{V_C}$ to input current,

$$\frac{\mathrm{V_C}}{\mathrm{I_{IN}}} = \frac{\mathrm{H(s)}}{1+\mathrm{LG(s)}} \tag{3.12}$$

Third, the sensitivity of $\mathrm{V_C}$ to input bias, $\mathrm{V_{BIAS}}$,

$$\frac{\mathrm{V_C}}{\mathrm{V_{BIAS}}} = \frac{\mathrm{LG(s)}}{1+\mathrm{LG(s)}} \tag{3.13}$$

where the loop gain LG(s) is given as,

$$\mathrm{LG(s)} = \mathrm{H(s)H_P(s)G_{\Delta\Sigma}G_{DAC}K_{VCO}T_S} \tag{3.14}$$

If the LG(s) is assumed to be large,

$$\begin{aligned} \frac{D_{OUT}}{I_{IN}} &\approx \frac{1}{G_{DAC}} \\ \frac{V_C}{V_{BIAS}} &\approx 1 \\ \frac{V_C}{I_{IN}} &\approx \frac{1}{H_P(s)G_{\Delta\Sigma}G_{DAC}K_{VCO}T_S} \end{aligned} \tag{3.15}$$

It can be seen from Equation 3.15 that without the presence of $H_P(s)$ (in such a case, we do not need $G_{\Delta\Sigma}$ as well), the sense node voltage, V_C, would vary depending on the input current. In this particular implementation, $K_{VCO}T_S \approx 27$ and $G_{DAC} = 2\mu$A/code. So for a 4μA range variation in input, V_C would have changed by 74mV. This is under the assumption that K_{VCO} remains constant over the entire input range of the VCO. But in reality, K_{VCO} would drop down to very low value thereby increasing the deviation of V_C further more. Figure 3.10 shows the variation of V_C in behavioral simulations with and without an accumulator in $H_P(z)$. It can be seen that the accumulator helps in keeping the bias node of the sensor to be a virtual node.

Since the proposed circuit resembles a continuous time $\Delta\Sigma$ modulator with a digital $\Delta\Sigma$ in its feedback path, a discrete time (DT) equivalent model was used to simulate and Figure 3.11 shows an ideal out of band magnitude spectrum obtained using transient simulations in MATLAB. Due to the presence of two integrators, a 2^{nd} order noise shaping is achieved. The out of band spectrum contains nulls at multiples of F_S (160kHz) because of the up sampling operation inside the digital

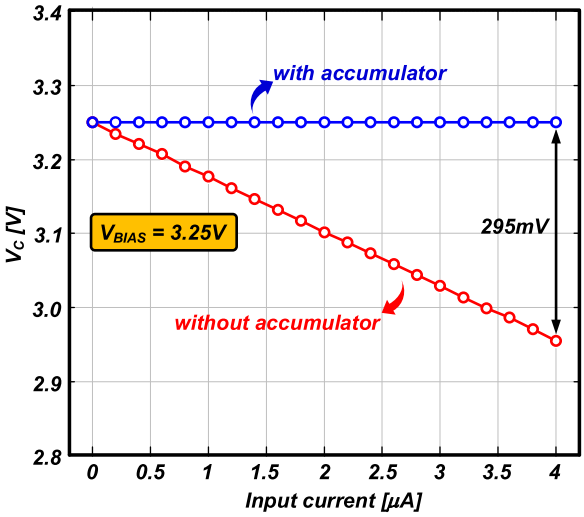

Figure 3.10: Bias node variation with and without accumulator in IIR filter.

$\Delta\Sigma$ modulator. Since the $\Delta\Sigma$ is running at $16F_S$, 8 nulls can be observed within $[0, \frac{F_{SM}}{2}]$ as evident from Figure 3.11.

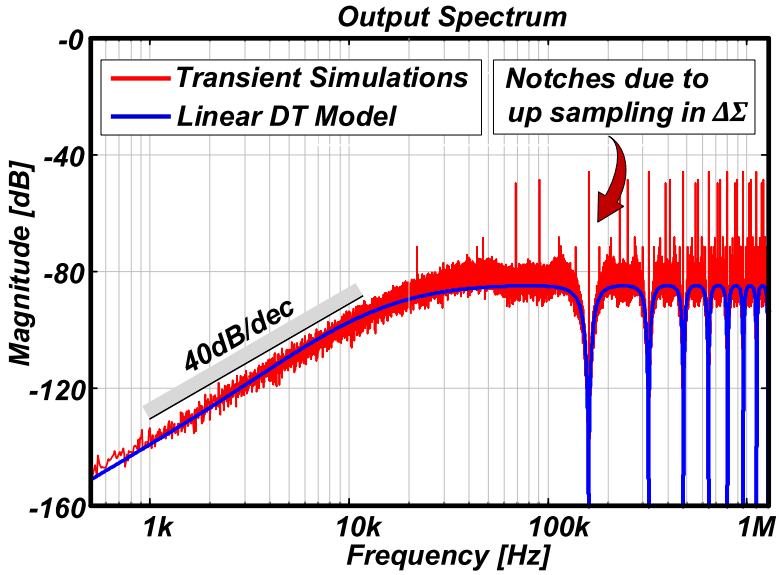

Figure 3.11: Ideal out of band magnitude spectrum.

CHAPTER 4

CIRCUIT DESIGN

This chapter discusses the design of the current controlled ring oscillator VCO, DAC and other blocks. The prototype sensor readout circuit is designed such that it can be interfaced with the photodiode specified in [4]. Since this diode requires around 5V reverse bias, the analog sections of the VCO and DAC are designed with thick oxide devices working at 5V supply and rest of the blocks are designed for 1.8V.

4.1 VCO Design

The schematic of the VCO is shown in Figure 4.1. The G_M stage is implemented as a resistive degenerated nMOS differential pair. The input pair is sized to keep the random mismatch to a minimum. A few mV of offset at the bias of the sensor does not degrade the sensitivity of the sensor element. Hence, extensive offset reduction methods are not needed. A large degeneration resistor is used to increase the linear input range of the VCO hence allowing a wide range of bias

voltages for the sensor interface. The degeneration resistor also helps to reduce the flicker noise contribution of the input pair. However, linearity and lower noise are obtained at the expense of a reduced K_{VCO} since the degeneration resistor reduces the equivalent G_M of the input pair. A dummy circuit is used on one side of the differential pair to make sure that the currents in both the arms match when $V_C = V_{BIAS}$. The VCO delay cells are implemented using CMOS inverters

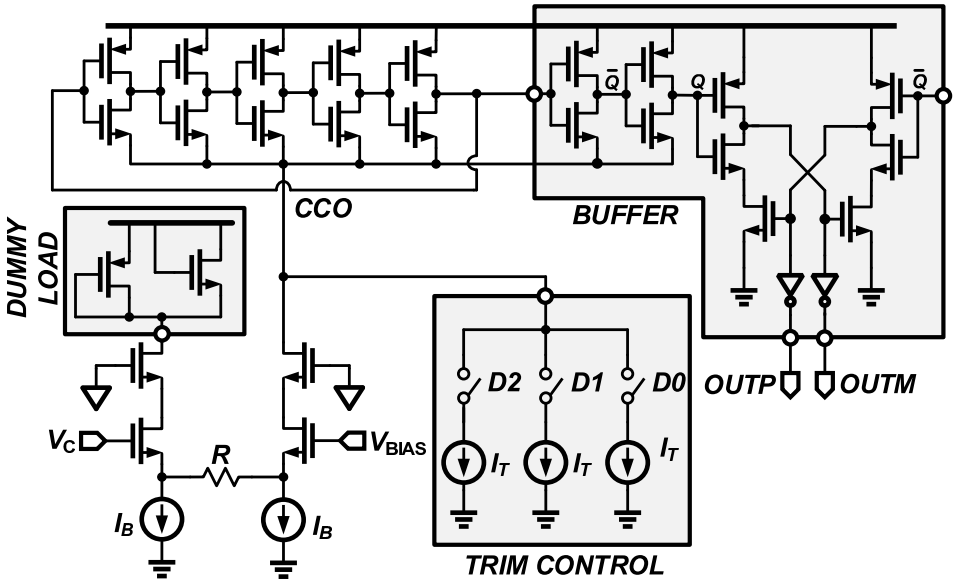

Figure 4.1: VCO and buffer schematic.

that are sized to achieve a center frequency of 2.56MHz with a G_M bias current of 400nA. Fortunately, the VCO phase noise requirement is greatly relaxed due to the presence of an integrator preceding it. An output buffer converts delay cell output to rail-to-rail CMOS levels.

4.2 DAC Design

Figure 4.1 shows the implementation of the feedback DAC. A 9 level current steering architecture is used to implement the feedback DAC. Thermometric implementation is used owing to its inherent monotonicity and ease of implementation with current steering sources. To get large output impedance, cascode devices

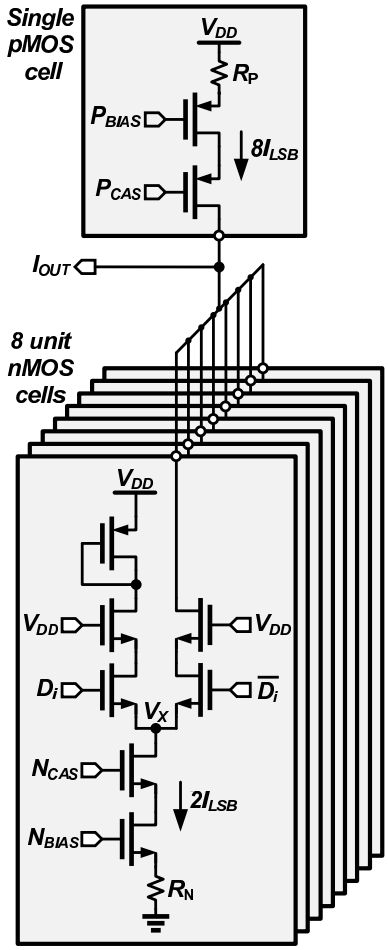

Figure 4.2: DAC schematic.

were used. nMOS cells had more voltage headroom than pMOS cells as the DAC output node in steady state is biased to a voltage close to the supply, V_{DD}. Only the nMOS cells in the DAC switch according to the input while the pMOS side pumps in a constant current. This implementation has less spurious tones (at the expense of more power) than the implementation where both nMOS and pMOS cells switch. Since DAC flicker noise is the major noise contributor in this implementation, large transistors and degeneration resistors are used to keep the noise to an acceptable level. A non return to zero (NRZ) switching scheme is implemented compared to return to zero (RZ) since the performance degradation due to clock jitter in NRZ is smaller.

The DAC is designed as a bipolar implementation which helps to interface the readout circuit with sensors that source or sink current. The clocks for the DAC, DEM and digital $\Delta\Sigma$ are obtained from a 10.24MHz external clock. This high frequency clock is used to generate four phases of 2.56MHz clock which is needed for accurately timing the data from the DAC, DEM and digital $\Delta\Sigma$.

4.3 Digital Design

The digital section involves the FDC, $H_P(z)$ filter, digital $\Delta\Sigma$ and DEM. Standard place and route tools are used to synthesize the digital blocks. The digital $\Delta\Sigma$ is implemented using a first order error feedback architecture. A clock frequency of 2.56MHz is found to be enough to keep the digital truncation noise below the noise floor of the main VCO based quantizer. The presence of a digital $\Delta\Sigma$ modulator

within the global VCO based continuous time $\Delta\Sigma$ modulator loop helps to dither the main modulator to a certain extent.

DEM is implemented using a first order data weighted averaging architecture (DWA). This makes the implementation simple and occupies smaller area compared to a second order DWA. Randomization within DWA is not required as the tones generated do not deteriorate the in-band performance of the readout circuit. The DAC cells are designed for 8 bit matching and the DWA improves the linearity to more than 12 bits.

4.4 Measurement Results

A prototype readout circuit was fabricated in 0.18μm CMOS process and it occupies an active area of 0.36mm^2. The measurement setup is shown in Figure 4.3. Low Dropout Regulators (LDO) are used to generate clean on board supplies from an external 5V supply. Keithley 6221 current source is used to provide an accurate input current. However, the capacitance of the input current source will change the passive integrator transfer function. Fortunately, this only changes the NTF slightly without much degradation in the performance. The output digital data is captured using TLA7000 series logic analyzer from Tektronix and post processing is done using MATLAB.

The DC transfer characteristic, measured with a V_{BIAS} of 3.25V, is shown in Figure 4.4. The prototype achieves an input range of 4μA (limited by the maximum DAC current) with a gain/offset corrected accuracy of 900pA. Below 1nA

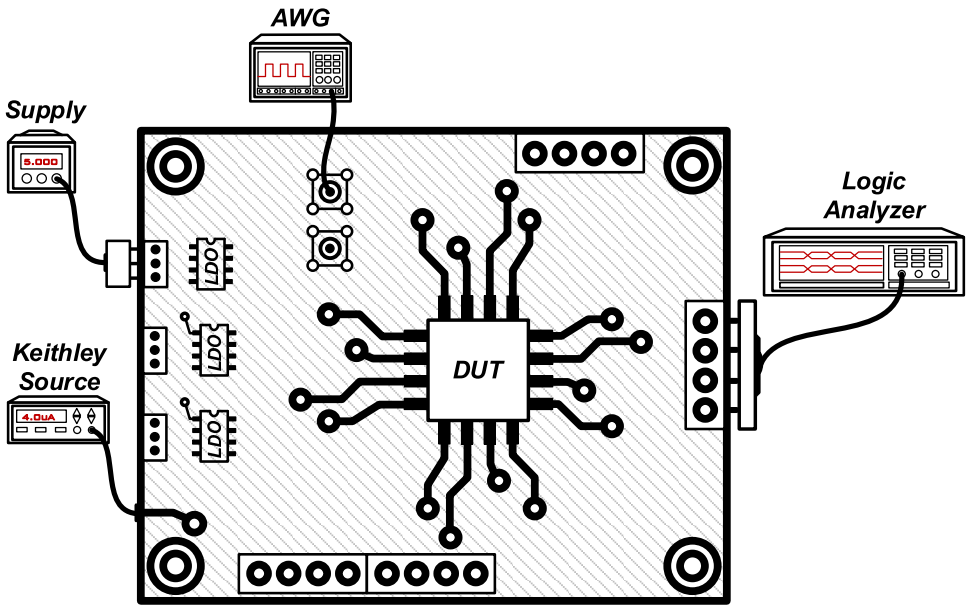

Figure 4.3: Measurement Setup.

input, the resolution is limited by the test setup. Figure 4.5(a), (b), (c) and (d) show measured start-up transient, sensitivity of the error voltage, V_E, to the bias voltage, the ripple on the sensor bias node, and the sensitivity of V_C to the input current, respectively. Thanks to the high DC gain of $H_P(z)$, the sense node always settles to V_{BIAS} independent of the input current. The steady-state ripple is about 10mV, which is largely due to the switching activity of the DAC. The total current consumption is 77.8μA out of which 62.5μA is consumed from the 5V supply and 15.3μA from the 1.8V supply. Table 4.1 summarizes the performance comparison and summary of the proposed readout IC. The die photograph is shown in Figure 4.6.

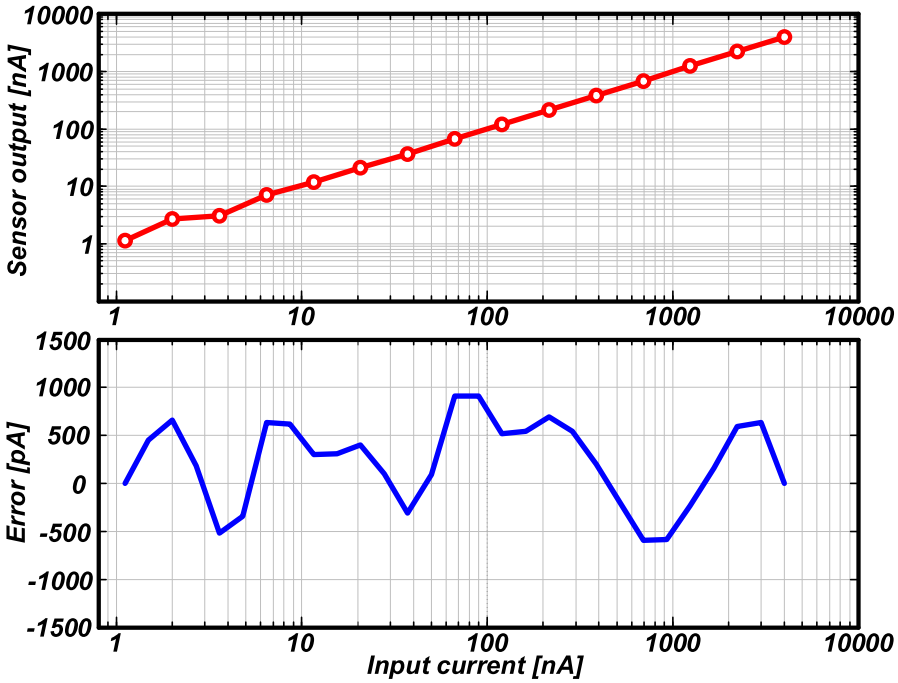

Figure 4.4: Measured DC transfer curve and absolute error plot.

Table 4.1: Performance comparison and summary.

	This work	[17]	[18]
Architecture	Mostly digital	Analog	Analog
Technology [nm]	180	180	180
V_{DD} [V]	5/1.8	1.8	1.8
I_Q [μA]	77.8	1300	110
T_{CONV} [ms]	400	—	—
Area [mm^2]	0.36	1.26	1.69
Input [nA]	1 to 4000	0.004 to 21	1 to 1000
Accuracy [nA]	0.9	0.004	1
Dynamic Range [dB]	73	77	—

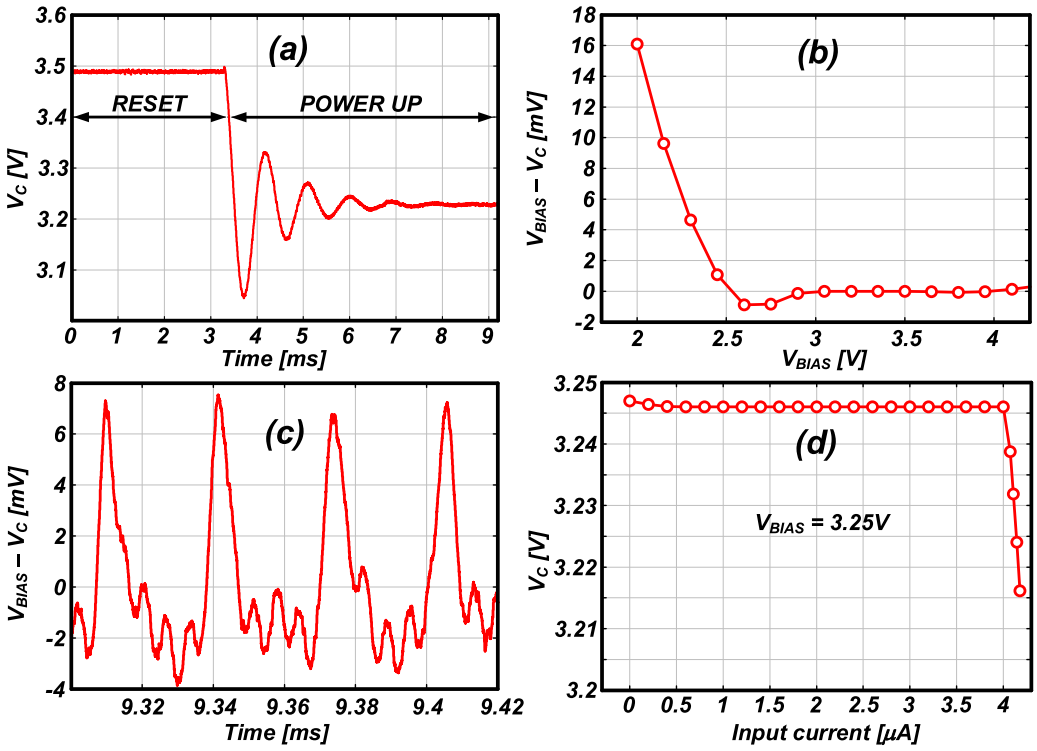

Figure 4.5: Measured transient response and bias sensitivity plots

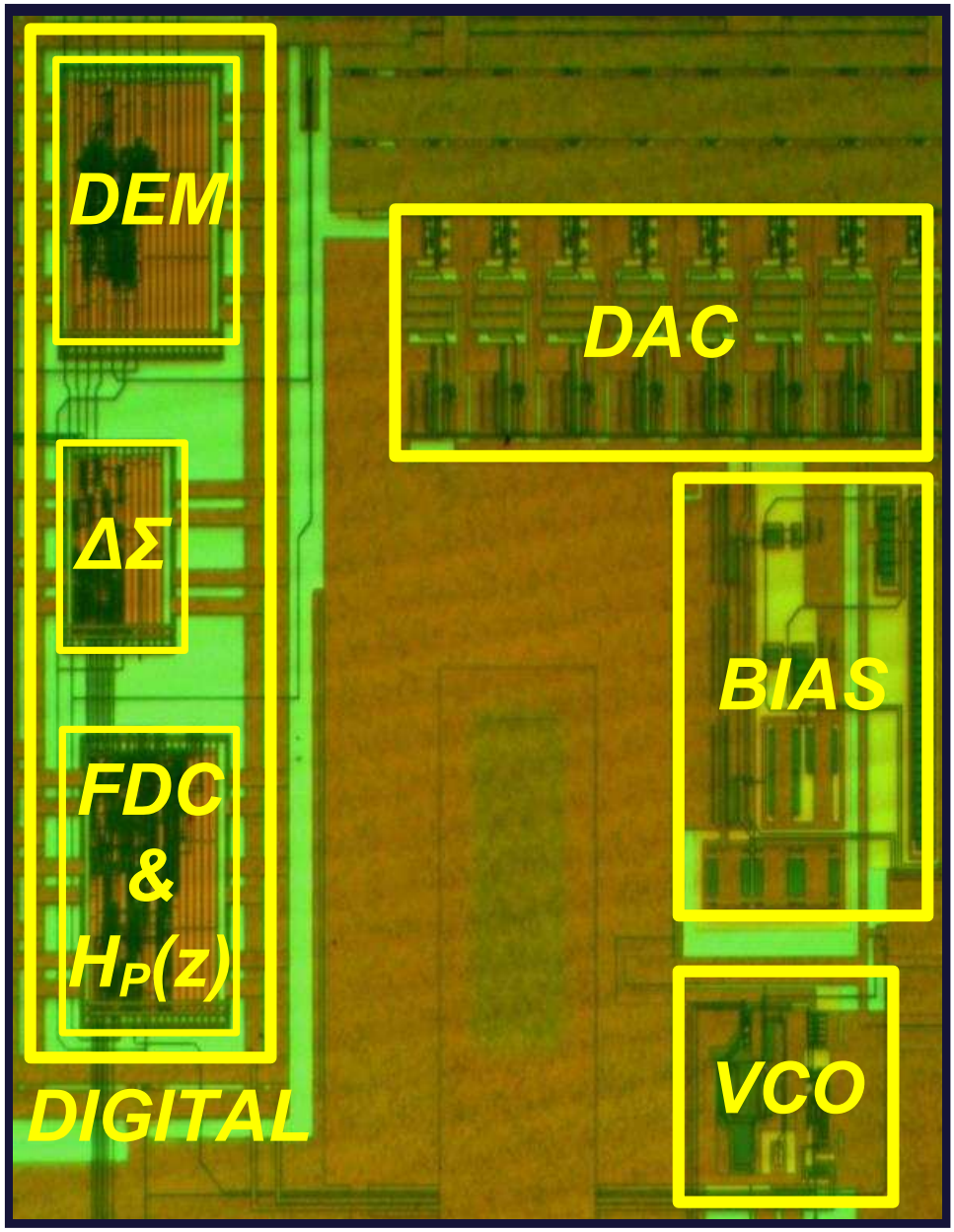

Figure 4.6: Die micrograph of the proposed readout circuit.

CHAPTER 5

CONCLUSION

In this thesis, a new architecture for digital sensor current readout circuit using a VCO based quantizer has been proposed. A major portion of the architecture is digital in nature which can benefit from the improved time resolution when implemented in a finer process. The ability of a VCO quantizer to provide open loop first order noise shaping is used effectively to get the required performance. The implicit non-linear capacitance of the sensor is used as a passive integrator to get another order of noise shaping.

To remove the detrimental effects of the finite reset time in counter based FDCs, a counter with a phase wrapping logic is used for the frequency detection. The effectiveness of such a method is demonstrated using an example wherein the FDC is shown to provide accurate results even in the presence of an overflow in the counter.

The finite gain of the VCO quantizer using an nMOS current starved ring oscillator VCO is formulated in a quantitative way in Chapter 3. To tackle this

issue, an architectural technique using a digital IIR filter in the global feedback path, is proposed. The IIR filter is implemented as a simple feedforward gain path and an accumulator. The measured bias sensitivity plots show the efficacy of the proposed IIR filter in increasing the loop gain and thereby reducing the swings at the sensitive nodes. In addition, the reduced swings allow a VCO which is highly non-linear, to be used without the need for extensive linearity improvement techniques. However, the use of an accumulator necessitates a large number of elements in the feedback DAC. This is taken care of, using a $\Delta\Sigma$ DAC wherein the digital output of the filter is truncated before feeding it to a low resolution DAC. Such an architecture is specifically suited for low bandwidth applications as the group delay in a $\Delta\Sigma$ DAC would be too large for a high frequency closed loop implementation.

Compared to the conventional approaches, the proposed architecture does not need a power hungry opamp for maintaining a virtual ground at the sensing node. Measured results from the prototype demonstrates the ability of the VCO based quantizer with an IIR filter feedback to accurately convert the input current to a digital representation. The 5V supply used for the analog sections can be reduced down depending on the application, which will further improve the power efficiency. The digital sections including the FDC, IIR filter, $\Delta\Sigma$, and DEM are coded using a hardware description language and synthesized using place and route tools. Consequently, porting this architecture to a finer process requires little redesign.

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