AN ABSTRACT OF THE THESIS OF

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Alternating-current thin-film electroluminescent (ACTFEL) devices are metal-insulator-semiconductor-insulator-metal (MISIM) structures which emit light under high field, pulsed excitation. One aspect of ACTFEL operation that is not well understood is the aging of such devices with operating time. One of the primary goals of this thesis is to characterize the kinetics of ACTFEL aging and to determine the associated activation energy which is then used as an aid in identifying the physical mechanism responsible for aging. Toward this end a new method, the capacitance-voltage (C-V) technique, for electrical characterization of ACTFEL devices is developed and refined. The threshold voltage ,V_{th}, total capacitance C_{tot}, and the insulator capacitance, C_{ins}, as well as some information about the relative interface state density are

available from C-V analysis.

SPICE simulation and a discrete ACTFEL model are used to verify and refine the C-V technique. The heart of the SPICE model is the standard ACTFEL circuit model which consists of three capacitors representing the phosphor and two insulator layers and a pair of back-to-back Zener diodes which account for conduction in the phosphor above threshold. Model enhancements are the inclusion of five resistances which account for 1) the resistance of the transparent conducting layer, R_{ito}, 2) and 3) the bulk insulator resistances, R_{i1} and R_{i2}, 4) the phosphor layer bulk resistance, R_p, and 5) a diode resistance, R_d, which is in series with the back-to-back Zener diodes and is termed a hot electron resistor since it is associated with the emission of electrons from interface trap states. The refined SPICE equivalent circuit is found to give good agreement with experimental C-V curves and with C-V curves generated using a discrete ACTFEL model which is built using discrete capacitors and Zener diodes.

Aging experiments are conducted using the C-V technique to monitor the threshold voltage as a function of aging time over a temperature range of -50 °C to 80 °C. An incubation period, in which the threshold voltage is constant, occurs for temperatures below 20 °C but no incubation period is observed for temperatures above 20 °C. After the incubation period, if any exists, the threshold

voltage increases logarithmically with time to a saturated value which is temperature-dependent; logarithmic and saturated aging are collectively referred to as constituting short-term aging. Short-term aging is characterized by C_{tot}, C_{ins}, and phosphor threshold voltage which are independent of aging time, rigid shifts in the C-V transition to higher threshold voltages with aging time, and decreases in the conduction and polarization charges with aging time. A kinetic analysis of the variable-temperature ACTFEL aging characteristics results in an activation energy of 0.2 eV. Such experimental observations lead to a model for ACTFEL aging in which conduction electrons are trapped in deep level, fixed charge states which arise from atomic rearrangement at the interface. This trapped charge reduces the polarization charge with a corresponding increase in the threshold voltage.

Capacitance-Voltage Analysis, SPICE Modeling, and Aging Studies of AC Thin-Film Electroluminescent Devices

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Capacitance-Voltage Analysis, SPICE Modeling, and Aging Studies of AC Thin-Film Electroluminescent Devices.

CHAPTER 1 - INTRODUCTION

Alternating-current thin-film electroluminescent (ACTFEL) devices are currently used for monochrome flat panel display applications. The ultimate goal of this technology is to have displays with full color, grey scale, long operating lifetime, and to meet high definition television (HDTV) standards. These goals are believed to be achievable[1,2].

To meet these goals, ACTFEL process technology needs to be developed so that red, green, and blue ACTFEL phosphors may be patterned onto glass substrates in matrix-addressable patterns. Currently a two-color, red/green display has been designed. The prototype of the two-color display was unveiled at the Society for Information Display (SID) conference in 1991. A possible configuration for a three-color display is shown in Fig. 1-1.

Addressing circuitry must also be developed that meets the criteria for HDTV. The 40-inch diagonal size for HDTV may present some production problems since no defects are allowable. As a further consideration, brightness must be stable and controllable over the rated lifetime.

Aging instabilities which affect panel brightness are a poorly understood phenomenon that currently is circumvented by pre-aging ACTFEL panels prior to commercial usage.

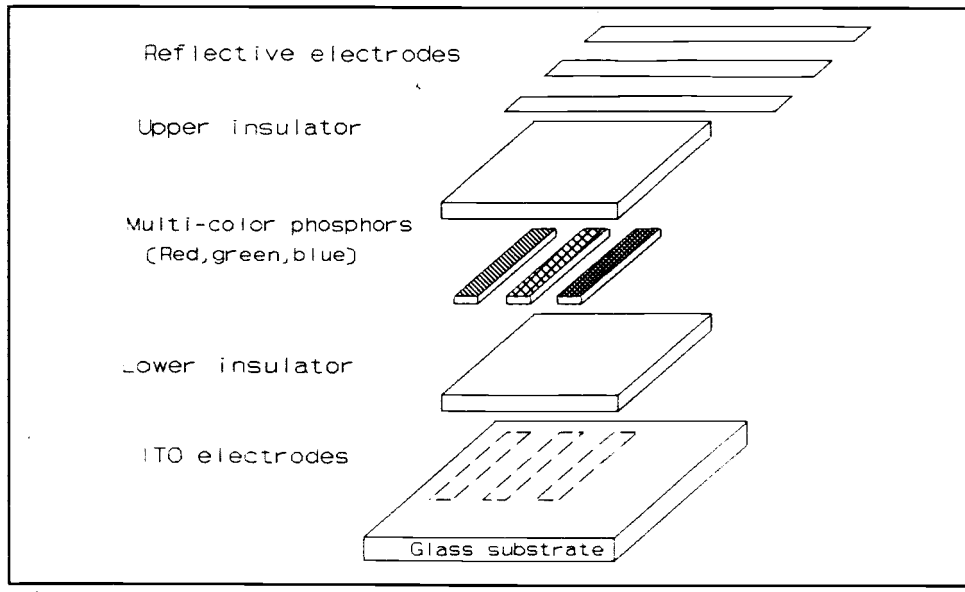

Figure 1-1. A possible three-color ACTFEL process.

The purpose of the work described in this thesis is to understand the nature of the aging instability by relating shifts in the threshold voltage to changes associated with the aging process. To this end we have developed and refined a capacitance-voltage (C-V) technique for the electrical characterization of ACTFEL devices and have used the C-V technique to monitor the threshold voltage shift during aging. The refinements of the C-V technique consist of optimization of the current limiting resistor used in the data acquisition circuit and optimization of the digital sampling period which increases the signal-to-noise ratio of the C-V measurement system. Additionally, a simple equivalent circuit for the ACTFEL in conjunction with SPICE

modeling is used for verification and refinement of the C-V technique as well as for further exploration of the basic device physics of ACTFEL performance.

Once the C-V technique is refined, it is used to track the threshold voltage shift as a function of aging time and as a function of temperature. Subsequently, the aging kinetics are modeled and Arrhenius analysis is used to deduce an activation energy for the aging process of 0.2 eV. The aging mechanism associated with this activation energy is believed to be due to atomic migration at the interfaces.

In Chapter 2 a discussion of the current understanding of ACTFEL device physics and operation is provided. The C-V technique and SPICE modeling are presented in Chapter 3. Chapter 4 consists of an examination of aging instabilities and an analysis of the aging kinetics. Conclusions and recommendations for further work are given in Chapter 5. It should be noted that some of the work described in this thesis has been previously published or submitted for publication[3,4,5,6,7].

CHAPTER 2 - LITERATURE REVIEW OF ACTFEL DEVICES

2.1 HISTORY AND BACKGROUND

The use of high electric fields to produce light from phosphor powders was first discovered in the early 1900's. However, not until the advent of thin-film technology has this phenomenon been useable for display technology. ACTFEL devices with long-term stability were first introduced in 1974 by Inoguchi[8]. These devices have matured from laboratory experiments to commercial mass production of 18-inch diagonal, monochrome displays. Additional research is necessary to understand all the phenomena associated with ACTFEL devices.

Degradation of light output with operating time limits the useful lifetime of production devices. Currently ACTFEL devices show an initial rapid change in light output followed by very small changes over the rest of the expected lifetime. The cause of the initial change in light output is the focus of the work in this thesis.

Much research is centered on developing full color capability. The future of ACTFEL flat panel displays holds much promise since the ability to generate the three primary colors has been demonstrated in several laboratories[9,10,11]. The major technical problems impeding the development of full color ACTFEL display technology are attainment of a blue phosphor with sufficient luminescent

intensity and proper chromaticity and the integration of a three color system onto a single substrate. Recently, two-color (red/green) displays have been demonstrated[12]. A demonstration of three-color ACTFEL display is expected from Planar Systems by 1993[13].

2.2 DEVICE DESCRIPTION

ACTFEL devices are built using low temperature processing methods. The low temperature is needed to protect the ITO conducting layer and the glass substrate. Currently, production ACTFEL devices are built using either sputtering, evaporation, or atomic layer epitaxy (ALE)[14].

The ACTFEL structure is shown in Fig. 2-1. The devices tested in this thesis use the materials and thicknesses shown in Fig. 2-1. The glass substrate is 7059 Corning glass which is covered with a transparent layer of indium-tin-oxide (ITO). The insulator layers are sputtered silicon-oxy-nitride and the phosphor layer is evaporated zinc sulfide doped with manganese (Mn). The ACTFEL device is annealed before Al deposition at 450 °C for 60 minutes. The aluminum layer is then applied by evaporation. The sputtered insulator layers are amorphous and the ZnS layer is polycrystalline in nature.

Other material systems are also used for ACTFEL fabrication. Some insulators which have been used include

Y_2O_3, Al_2O_3, Ta_2O_5, Al_2O_3-TiO_2, and, Si_3N_4[15-19]. ZnS:Mn, which emits a yellow luminescence characteristic of the Mn dopant, is the most common monochrome display phosphor. CaS and SrS are phosphors that use rare-earth dopants to produce primary colors. Some of the most notable rare-earth dopants include europium (Eu), terbium (Tb) and cerium (Ce) which are used to produce red, green, and blue-green light, respectively.

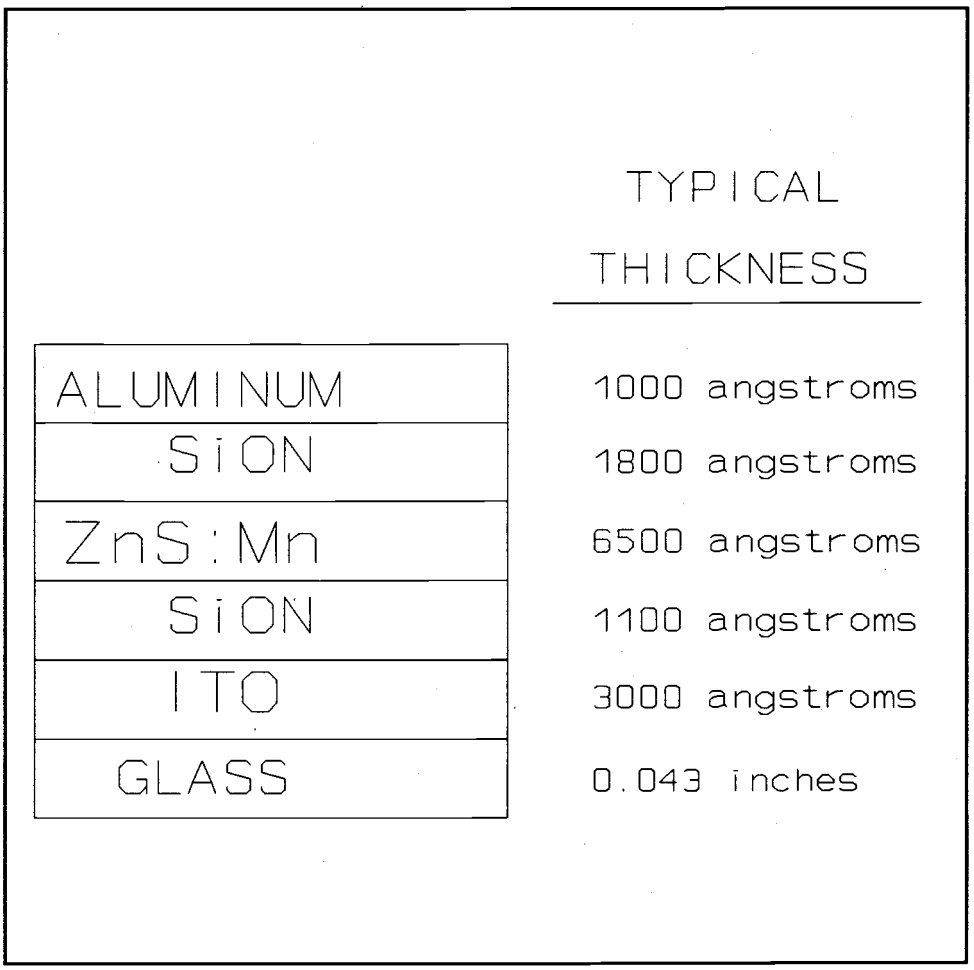

Figure 2-1. Typical ACTFEL structure and dimensions.

2.3 PHYSICS OF DEVICE OPERATION

2.3.1 - introduction

Various authors have described the operation of ACTFEL devices, including Sahni[20], Mach[21] and Inoguchi[8]. In the following section simplified energy band diagrams for virgin and aged devices are examined in order to provide an understanding of how ACTFEL devices operate. This is followed by a brief description of the various techniques used to characterize ACTFEL devices. The physical phenomena observed by using these characterization methods are discussed along with limitations of each particular technique.

2.3.2 - simplified energy band diagrams of ACTFEL devices

The band gap of ZnS is 3.68 eV and the band gap of the SiON insulators is about 5.8 eV. The ACTFEL structure is assumed to be homogeneous for each region. The nature of the ZnS-SiON interface is not completely known. However, it is generally accepted that the interface regions are depleted of sulfur and that a large number of interface states exist ($\approx 10^{13}/cm^3$). To understand the operation of the ACTFEL device under an alternating voltage waveform, simplified band diagrams as shown in Figs. 2-2 through 2-6 are used. In these diagrams the interface is modeled as ideal.

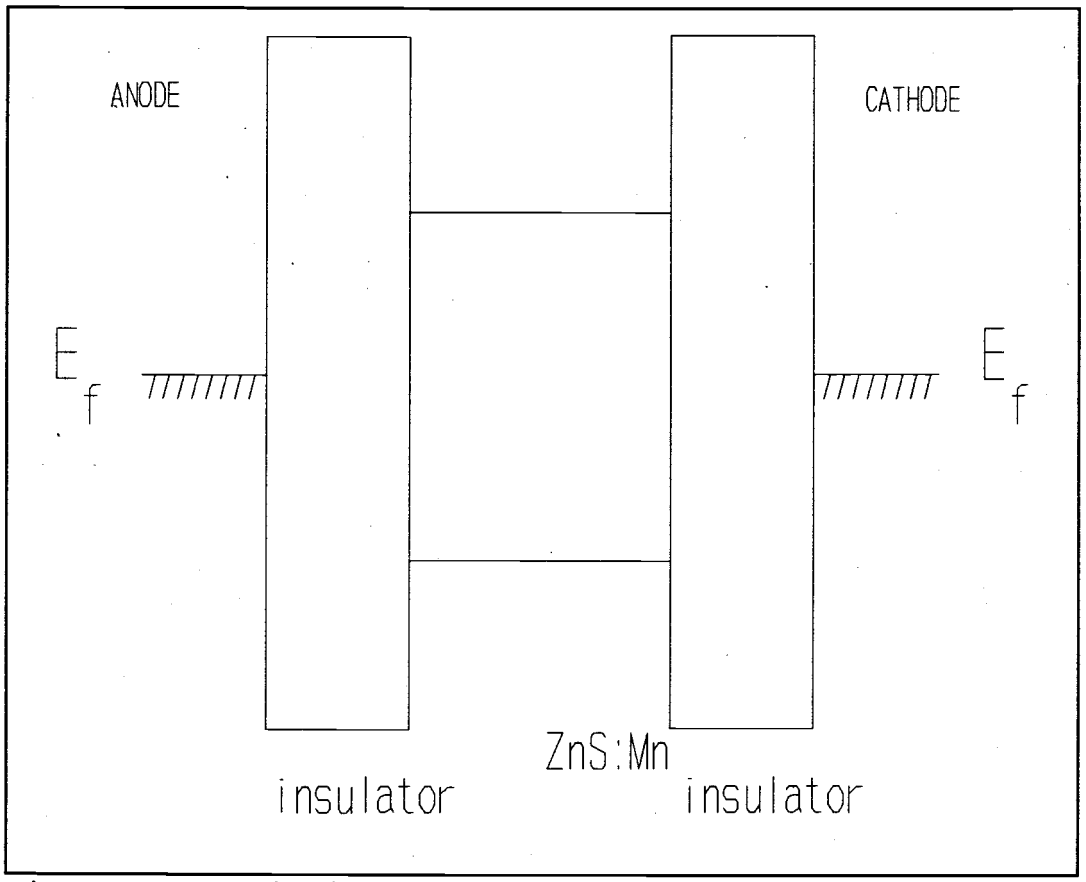

Figure 2-2. Virgin energy band diagram of ACTFEL device.

Under a symmetric bipolar voltage waveform there is a tilting of the energy band diagram from the virgin state and a build-up of polarization charge at the ZnS-SiON interfaces. The virgin state is considered to be that state where the internal polarization charge is identically zero. The virgin state energy band diagram is shown in Fig. 2-2. The effect of positive and negative biasing is explained as follows.

Assume that positive biasing of the device occurs at the anode. Under this bias the energy band diagram is as

shown in Fig. 2-3. Electric potential is dropped across each region until the ZnS-SiON interface starts to tunnel-emit electrons. When electron conduction occurs across the ZnS layer, the ZnS electric field is effectively clamped due to an abundance of tunnel-injected electrons from interface states. As positive bias is further increased the electric potential is dropped across the SiON insulators. Tunnel-injected electrons transit the ZnS region under the applied field, are trapped at the cathodic interface, and set up an opposing electric potential. When the positive bias returns to zero, the external electric potential goes to zero, but the internal electric field in the ZnS due to electron trapping at the cathode interface remains, and is referred to as the internal polarization field. The energy band diagram, as shown in Fig. 2-4, results after the polarization charge is transferred during the positive bias, and after the external voltage goes to zero. The polarization charge is assumed to remain constant during the delay time between alternating pulses which is typically, at a frequency of 1000 Hertz, of the order of 0.5 milliseconds.

During the subsequent opposite polarity pulse the internal polarization field aids the external electric field causing electrons to tunnel from interface trap states at a lower external bias magnitude than for the

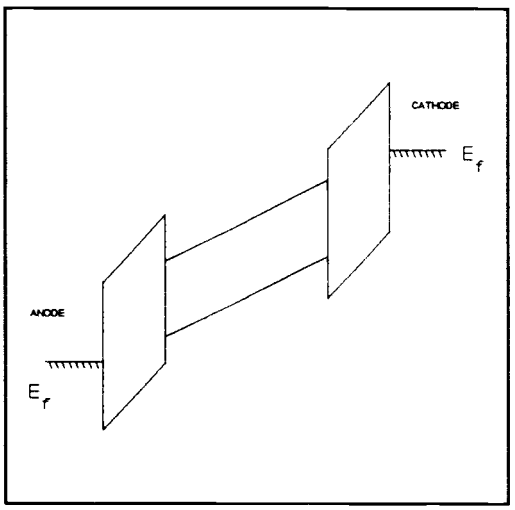

Figure 2-3. ACTFEL energy band diagram during positive bias.

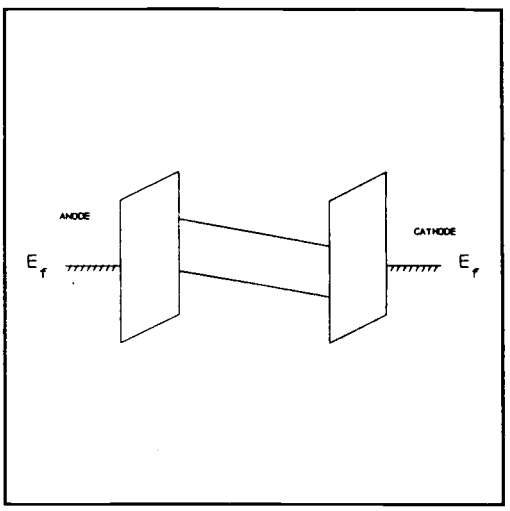

Figure 2-4. ACTFEL energy band diagram after positive bias.

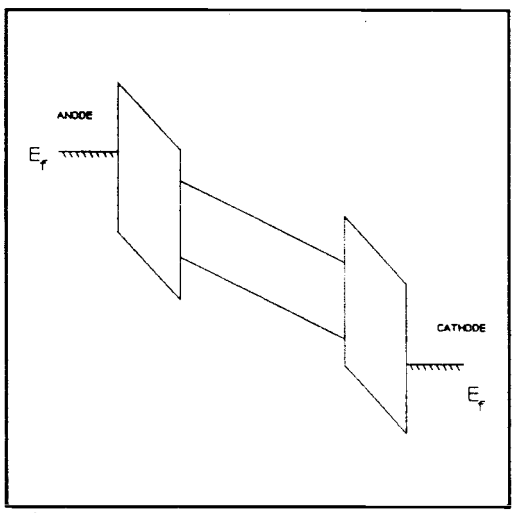

Figure 2-5. ACTFEL energy band diagram during negative bias.

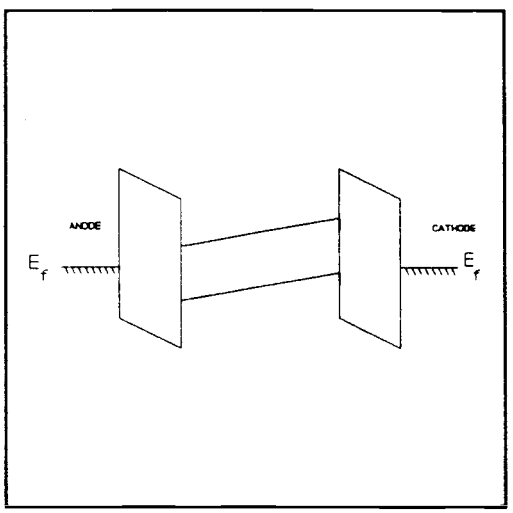

Figure 2-6. ACTFEL energy band diagram after negative bias.

previous polarity pulse. This results in an increase in the internal charge transferred and a concomitant increase in the polarization field. This process repeats until a steady state is reached at which time the magnitude of the

internal polarization charge for each voltage pulse is the same. Figures 2-5 and 2-6 show the energy band diagram during and after, respectively, the negative bias waveform.

2.3.3 - analysis techniques

The methods typically used to characterize ACTFEL device operation are the charge-voltage (Q-V), luminance-voltage (L-V), also called brightness-voltage (B-V), and current-voltage (I-V) methods. All three methods may be used to define a threshold voltage. Q-V also may be used to determine total and insulator capacitance, and the conduction and polarization charges. L-V is a production tool used to set panel brightness and grey scale and to monitor luminance shift with operating time. I-V is the only technique that directly attempts to determine the internal operation of ACTFEL devices. In this thesis a new method is developed, the capacitance-voltage (C-V) technique, which is discussed in Chapter 3.

The Q-V technique[22] employs the Sawyer-Tower method for determining charge as shown in Fig. 2-7. Q_{pol}, Q_{tot}, Q_{cond} and the threshold voltage are determined directly from the Q-V curves. C_{tot} and C_{ins} are determined from the slope of the Q-V curve before and after the threshold voltage. Figure 2-8 shows an ideal Q-V waveform. Through experimentation it is found that this technique is

sensitive to the type and quality of the sense capacitor, C_{sense}, used in the circuit. The dissipation of C_{sense} must be very small to ensure that significant charge does not leak from C_{sense} during the long delay time associated with using a pulsed voltage waveform. Also C_{sense} is generally 100 times the total capacitance of the ACTFEL device to ensure the voltage change across C_{sense} is small compared to the voltage across the ACTFEL device. A modification of this method gives the charge-time (Q-t) waveform which is a plot of the charge accumulated on C_{sense} as a function of time. Again, these charge techniques are sensitive to the type of sense capacitor used in the test circuit.

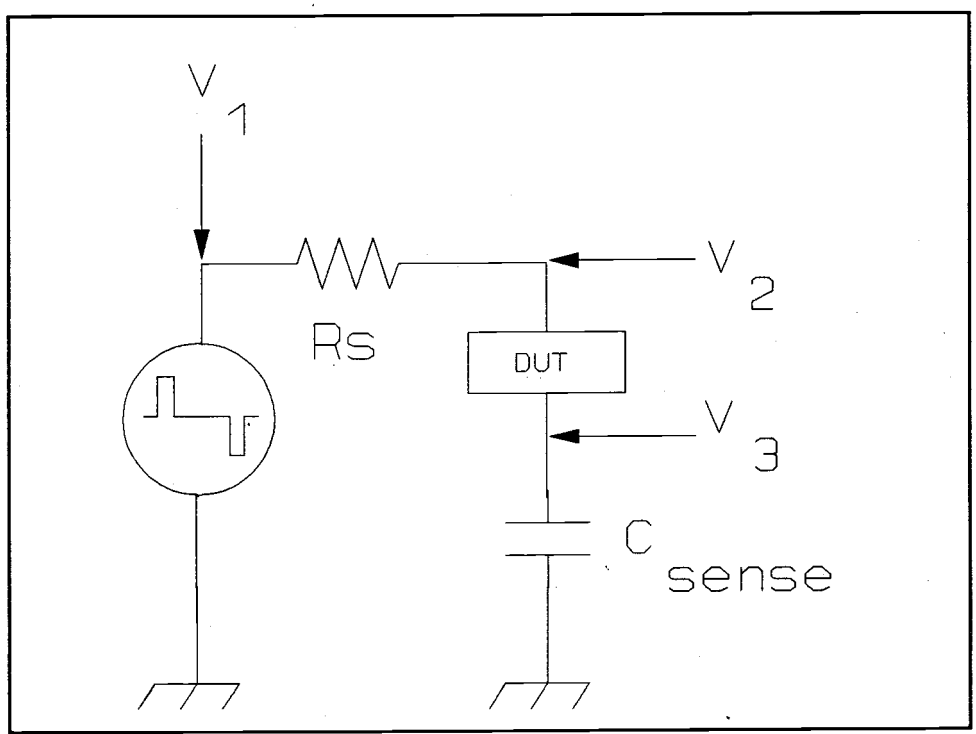

Figure 2-7. Typical Q-V measurement circuit.

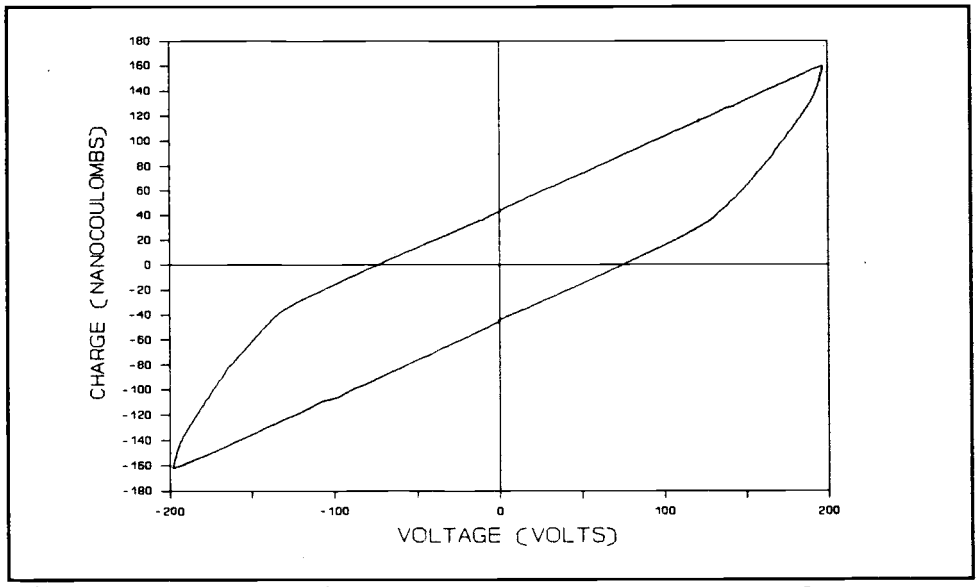

Figure 2-8. Typical Q-V measurement result.

Another widely used characterization method is the L-V technique. The L-V method[23] measures the light output as a function of applied bias. The peak of the voltage waveform is ramped from zero volts to 40 volts above the threshold voltage and the luminance is monitored.

Light output is a function of many factors such as, 1) the transmission through each layer, 2) the doping concentration, and 3) viewing angle. Since many factors affect luminance, it is extremely difficult to relate changes in brightness to changes in the electronic nature of the ACTFEL structure. However, luminance versus applied voltage is the final criterion for the determination of how well an ACTFEL device operates.

The I-V technique[22] attempts to measure the conduction

current through ACTFEL devices by the use of a capacitor bridge. This technique is susceptible to measurement errors since the ACTFEL device can not strictly be modeled as a capacitor when electron conduction occurs at and above the threshold voltage. The I-V test circuit is shown in Fig. 2-9.

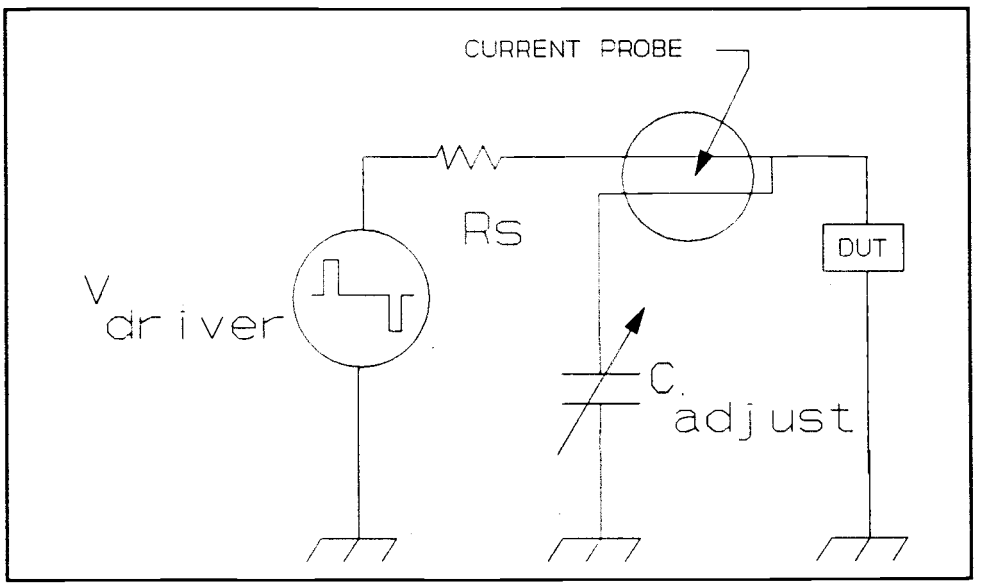

Figure 2-9. The I-V measurement circuit.

The I-V measurement system is calibrated by nulling the current through the ACTFEL device, using a variable capacitor, while the device is operated at a sub-threshold voltage. The ACTFEL device is then operated above threshold and the conduction current through the ZnS layer is determined by multiplying the measured current by the ratio $\frac{(C_{ins} + C_p)}{C_{ins}}$, where C_{ins} is the capacitance due to both insulating layers and C_p is the phosphor layer

capacitance of the device. Most measurement error occurs at the initiation of conduction and before field clamping takes place. The reason is explained as follows.

Before conduction the bridge circuit is balanced. After initiation of conduction the ACTFEL device capacitance increases due to conduction through the ZnS layer. Once field clamping occurs then the ACTFEL capacitance is fixed at C_{ins}. Between the subthreshold and field clamping regimes, as described in Chapter 3, the capacitance is transitory and is not accurately modelled by the given equations. This results in an error when calculating conduction current. Several authors have provided methods to decrease the error in conduction current calculations[24,25].

2.4 SUMMARY

ACTFEL devices show a promising future. Full color capability and grey scale should soon be available in smaller display sizes. Problems associated with aging instabilities and color technology integration are surmountable.

There are currently three methods of characterizing ACTFEL devices; Q-V, L-V, and I-V. A fourth method, the C-V technique, is discussed in Chapter 3. Each of the four characterization methods is simple to implement and the

results are easy to understand. However, improvements to the basic characterization techniques need to be made in order to increase the accuracy and information that may be obtained.

CHAPTER 3 - THE C-V TECHNIQUE AND SPICE MODELING

3.1 INTRODUCTION

Electrical characterization of ACTFEL devices is usually accomplished by charge-voltage (Q-V), luminance-voltage (L-V), or current-voltage (I-V) analysis. We have recently described[3] the C-V technique as an alternative method for ACTFEL electrical characterization. Our goal for the work described herein is to show that the C-V technique, in conjunction with SPICE modeling using a simple equivalent circuit, provides a powerful means of probing ACTFEL device physics.

The SPICE model for the ACTFEL structure is discussed in Section 3.2. The C-V technique and driving waveform are discussed in Section 3.3 of this chapter. Section 3.4 examines how values are obtained for the enhanced SPICE model parameters. Section 3.5 compares C-V curves obtained from SPICE simulation, an ideal discrete ACTFEL device, and real ACTFEL devices. Parametric variations of selected SPICE model elements are examined in Section 3.6. Section 3.7 is a summary of the chapter.

3.2 THE SPICE CIRCUIT MODEL

The simple equivalent circuit for SPICE simulation of the ACTFEL device[26] is shown in Fig. 3-1. C_{i1} and C_{i2} are the insulator capacitances and C_p is the phosphor

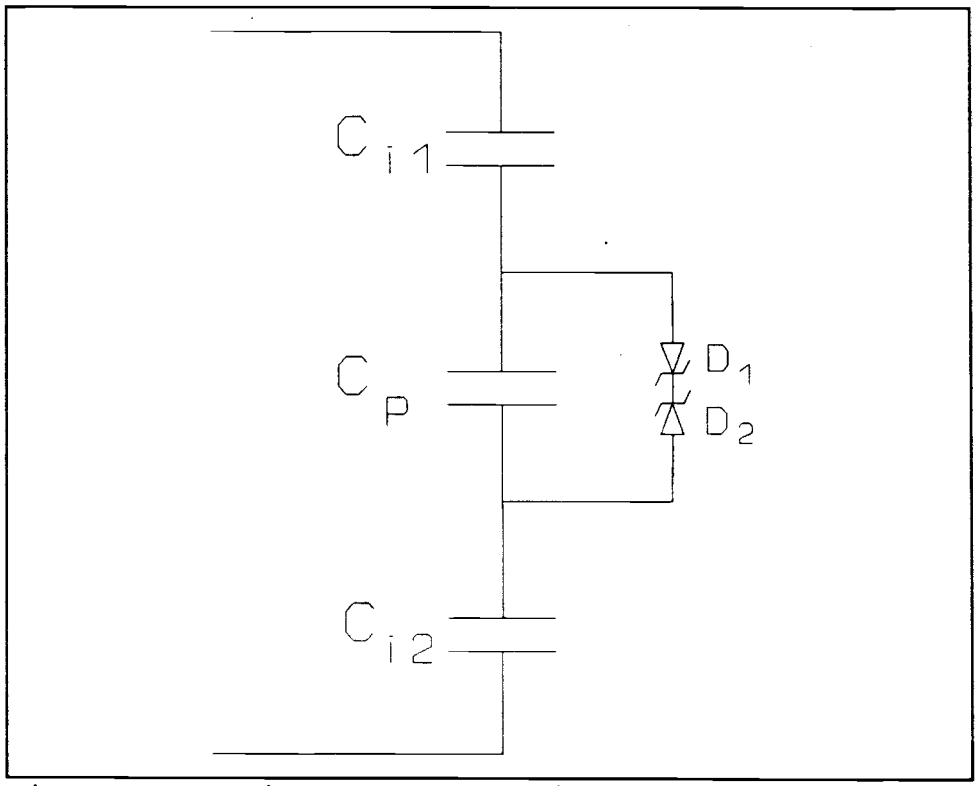

Figure 3-1. Simple SPICE equivalent circuit model.

capacitance. The phosphor capacitance is shunted by two back-to-back Zener diodes. These diodes are characterized by only one parameter, the breakdown voltage, BV, beyond which conduction occurs. These circuit components constitute what is termed an ideal circuit model for the ACTFEL device.

This circuit provides a general description of ACTFEL device operation. In order to more completely describe the electrical characteristics of ACTFEL devices, five additional resistors are added to the ideal equivalent circuit to obtain the SPICE equivalent circuit of Fig. 3-2.

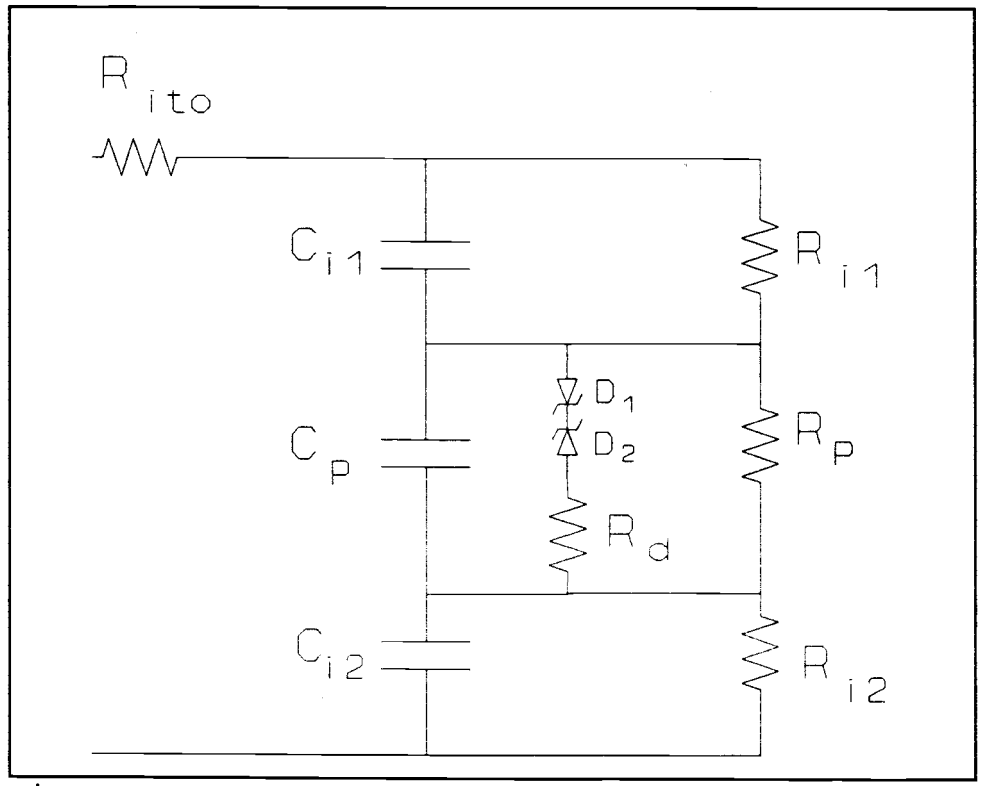

Figure 3-2. Enhanced SPICE equivalent circuit model.

R_{i1}, R_{i2}, and R_p represent the parallel shunt resistances of the respective insulator or phosphor layers which are associated with dc leakage through these layers. R_{ito} is a lumped resistance accounting for the non-zero series resistance of the ITO electrode. R_d is used to model tunneling from interface states which limits the current flow during conduction in the ZnS layer. R_d is denoted the diode resistor or is alternately referred to as a hot electron resistor. The effects on C-V curves due to parametric variations of these resistances are discussed in Section 3.6.3 of this chapter.

3.3 THE C-V TECHNIQUE

C-V analysis is accomplished using the circuit shown in Fig. 3-3. An arbitrary waveform generator (Wavetek model 275) in conjunction with a high-voltage operational

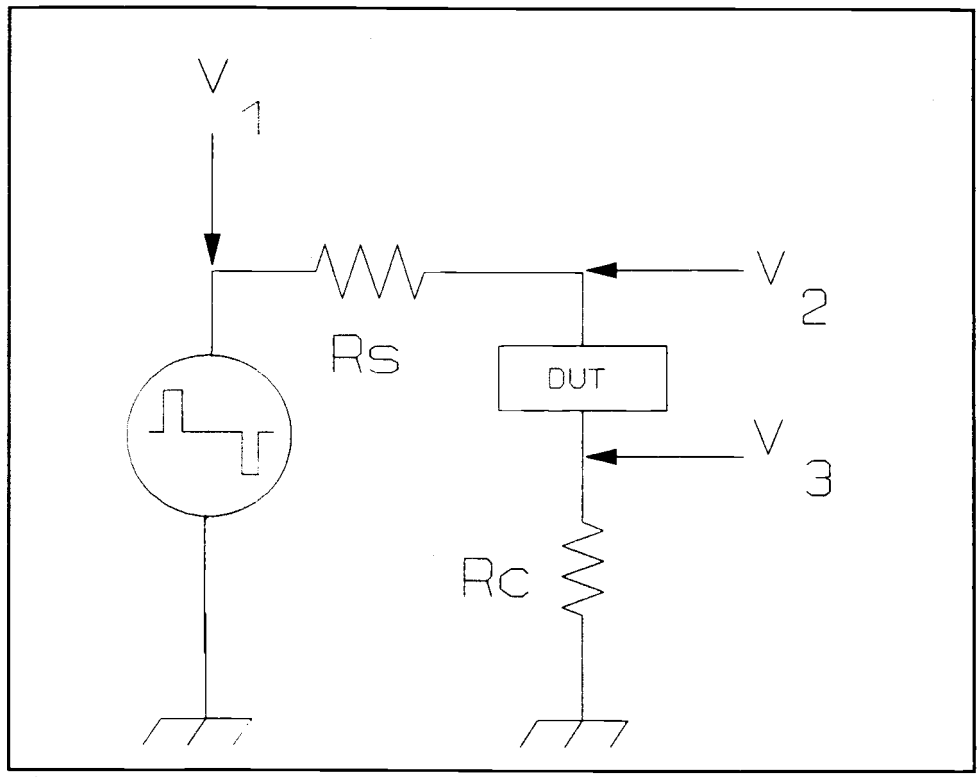

Figure 3-3. Measurement circuit for C-V analysis.

amplifier (Apex PA-85) generates the small duty cycle bipolar pulse waveform which drives a series resistor, R_s, the ACTFEL device, and a current sense resistor, R_c, as shown in Fig. 3-3. R_s is chosen to be large, typically 1200 ohms. This ensures that the driving waveform does not destroy the ACTFEL device because the current is limited by R_s. R_c is chosen to be about 10 ohms so that the voltage

drop across R_c is negligible. The three voltages indicated in Fig. 3-3 (V_1, V_2, and V_3) correspond to the driver, the ACTFEL device, and the current sense voltages, respectively. The standard waveform employed is shown in Fig. 3-4. The waveform consists of symmetric, bipolar pulses of trapezoidal shape with 5μs rise and fall times and a pulse width of 30μs where rise and fall times are defined as the time between 0% and 100% of the maximum amplitude and the pulse width is defined as the duration during which the pulse is at its maximum amplitude. The frequency of the waveform is 1000 Hertz. This waveform is

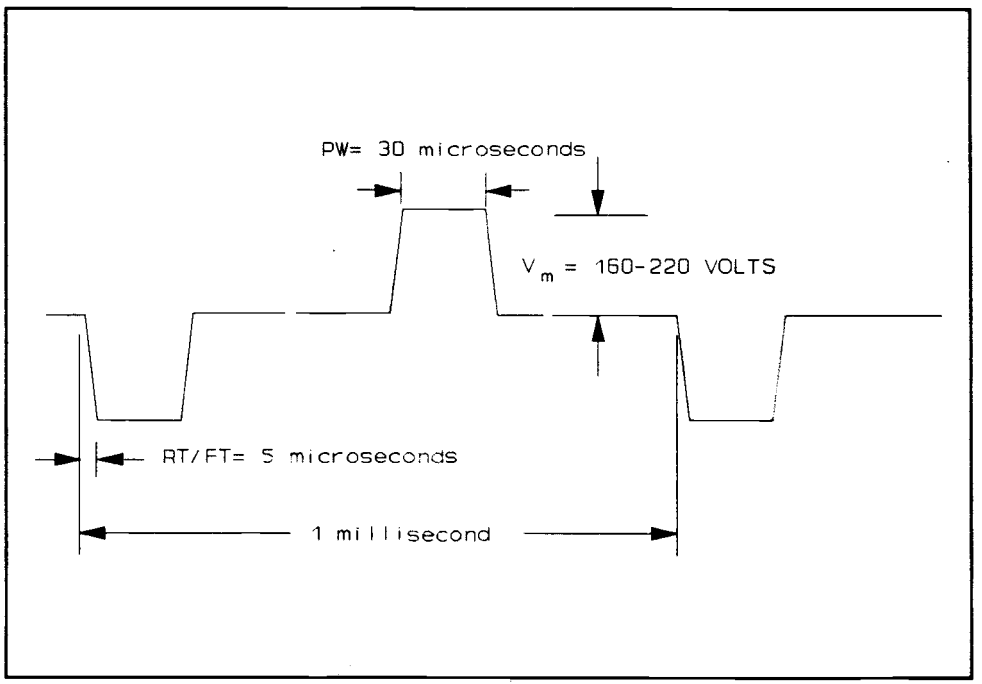

Figure 3-4. Standard driving waveform. RT - rise time, FT - fall time, PW - pulse width, and V_m - maximum driving voltage.

typical of driving waveforms used for commercial ACTFEL drivers with the exception of frequency, which is usually 60 Hz. Note that standard definitions of rise time, fall time, and pulse width are not used for the waveform definition.

The measurement is performed in the following manner. Voltages $V_2(t)$ and $V_3(t)$ are obtained using a Tektronix model 7854 digitizing oscilloscope with high input impedance probes. A 100 point average of the respective voltages, an oscilloscope time base setting of 2 μs per division, and 128 points per waveform give best results. The calculation of C-V curves then proceeds as follows.

Referring to the circuit shown in Fig. 3-3, the current through the ACTFEL device is obtained from the voltage across the sense resistor, R_c,

$$I(t) = \frac{V_3(t)}{R_C} . \qquad (3\text{-}1)$$

The capacitance is equal to the current divided by the derivative of the voltage across the ACTFEL device, so that the C-V curve is obtained as

$$C(V_2\text{-}V_3) \triangleq \frac{I(t)}{d[V_2(t)-V_3(t)]/dt} . \qquad (3\text{-}2)$$

The resulting C-V curve is labelled as shown in Fig. 3-5.

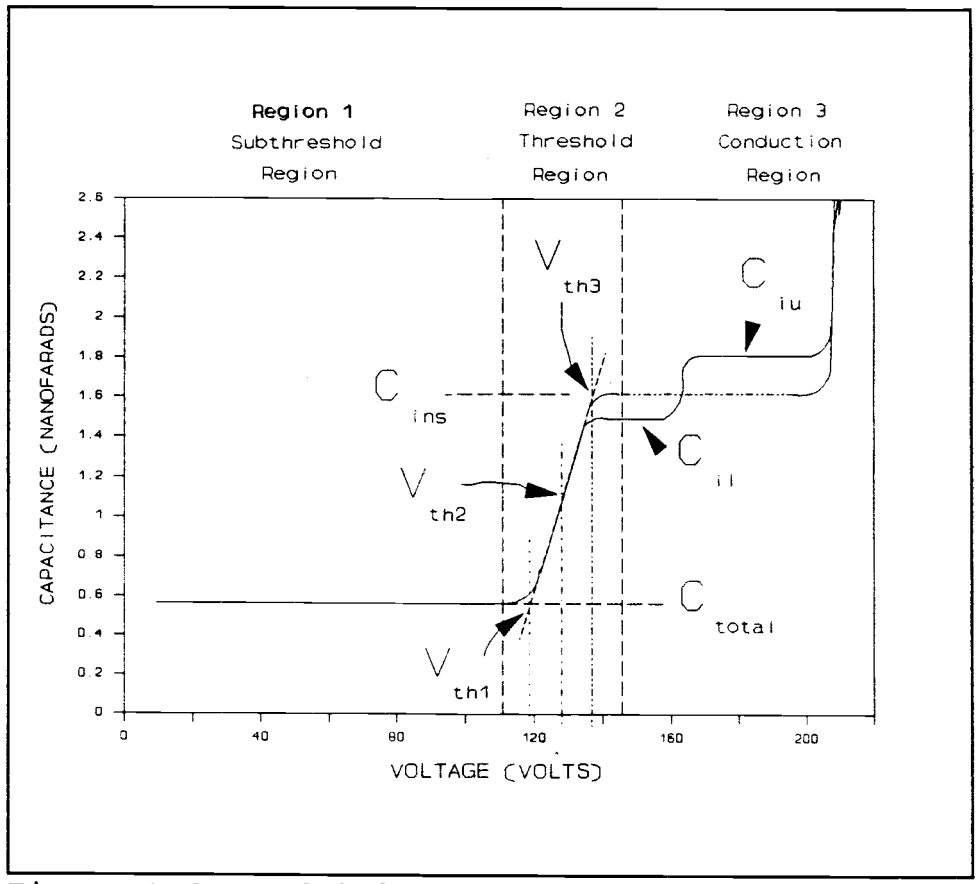

Figure 3-5. A labeled C-V curve showing capacitances, threshold voltages, and standard terminology.

The labels are required to explain changes in the C-V curves due to aging or other causes. The curve is divided into three voltage regions denoted subthreshold, threshold, and conduction. Also, three threshold voltages are distinguished as follows:

1) V_{th1}, the onset of conduction,
2) V_{th3}, the field clamping voltage, and
3) V_{th2}, the Q-V threshold voltage.

Two constant capacitance regimes, C_{tot} and C_{ins} are also labeled. These refer to the pre-breakdown capacitance,

C_{tot}, which corresponds to the total capacitance of the ACTFEL structure prior to breakdown and the insulator capacitance, C_{ins}, which is the capacitance due exclusively to the insulator layers after breakdown when the phosphor capacitance is shunted by conduction through the phosphor.

Under certain conditions, described in Section 3.6.3, C_{ins} splits into what is called an upper insulator capacitance, C_{iu}, and a lower insulator capacitance, C_{il}. This condition is due to non-field clamping conduction. Field clamping requires that two conditions be met.

1) the C_{ins} value is flat after breakdown, and
2) C_{ins} is the expected insulator capacitance as determined by Eqn. 3-3.

3.4 PARAMETER EXTRACTION

In this section simple methods for determining SPICE model parameter values are discussed. These methods are used to obtain nominal values for the ACTFEL devices tested. Part of SPICE analysis is to determine how variations from nominal values affect charge, capacitance, and threshold voltage. The parameter values used in the SPICE model are estimated in accordance with the following considerations. C_{i1}, C_{i2}, and C_p are calculated as parallel plate capacitors,

$$C = \epsilon * \frac{A}{d} \qquad (3\text{-}3)$$

where ϵ is the permittivity of the respective layer, **A** is the area, and **d** is the thickness of the layer.

V_{th1} and V_{th3} are obtained graphically by drawing a straight line through the most linear portion of the C-V transition to the points at which this line intersects an extension of C_{tot} or C_{ins}, respectively. V_{th2} is obtained as the average of V_{th1} and V_{th3}. V_{th2} is found to correspond well with the threshold voltage obtained from Q-V analysis. This external threshold voltage may be used to estimate an internal diode breakdown voltage using the following equation; $BV = V_{pol} + V_p^{ext}$ Using the circuits shown in Figs. 3-1 and 3-3 and assuming quasi-static conditions prevail when V_2 approaches V_{th1}, by capacitance division the voltage across C_p due to the current voltage pulse may be determined. This voltage is determined as follows:

$V_p^{ext} = \frac{Q_{ext}}{C_p}$ where Q_{ext} is the charge accumulated on the device up to V_{th1} and C_p is the phosphor layer capacitance. By adding the polarization voltage, V_{pol}, and V_p^{ext} a value for BV is obtained. The evaluated range of BV for C-V curve variations is 88 to 96 volts.

R_i values are determined by the quality of the insulators. SiON insulators, processed similar to the

devices used in this work, evaluated using a corona discharge method at the David Sarnoff Research Center, are found to have a very high resistivity,[27] on the order of 10^{15}-10^{16} Ω-*cm* . Using this value it is possible to determine the resistance of the SiON layers. The resistance is calculated using the simple bulk resistance method,

$$R = \rho \frac{L}{A} \qquad (3\text{-}6)$$

where ρ is the resistivity of the material, **L** is the length, and **A** is the area. The insulator resistivity could range from 10^{12} *to* 10^{17} Ω-*cm* which would give corresponding resistance variations from 2.5×10^{8} to 2.5×10^{13} ohms.

R_{ito} is determined by evaluating the sheet resistance per square of the ITO layer and determining the number of squares associated with the contact regions. The resistance per square is 10 ohms. For the glass samples used, R_{ito} has a value of approximately 30 ohms. Also, for reasonable process variations R_{ito} is not expected to exceed 100 ohms.

R_p is estimated using a typical value for the bulk resistivity of polycrystalline ZnS[28]. The resistance is again calculated using the simple bulk resistance method in accordance with Eqn. (3-6). This yields a value of R_p of order 2×10^{6} ohms. Parametric variations of R_p are

evaluated over the range $1 x 10^4$ to $1 x 10^7$ ohms.

R_d is an internal parameter that is not easily evaluated. Generally R_d is adjusted, as necessary, to fit SPICE C-V simulations to actual C-V curves. The nominal value of R_d is 40 ohms and realistic limits of R_d are approximately 20 to 200 ohms. Parametric variations of Rd are obtained from 0 to 1000 ohms in order to examine trends over a broad range.

3.5 VERIFICATION OF THE ACCURACY OF THE C-V TECHNIQUE

The C-V technique accuracy is verified using three methods. First, SPICE simulation using nominal parameter values is used to determine the accuracy of the C-V equations discussed in Section 3.3. It is found that C_{tot}, C_{ins}, and V_{th} are easy to extract and that their values are as expected. Deviations from expected C-V curve results occur under certain parameter variations and are discussed in Section 3.6.

Second, SPICE C-V simulation curves are compared with the C-V curves of an ACTFEL device built from discrete components of the ideal model shown in Fig. 3-1. This is done to optimize the oscilloscope settings and R_s value. It is found that good agreement is achieved using the oscilloscope settings and R_s value previously described. Variations from these settings tend to increase the

observed noise in the C-V curve. The comparison of a SPICE simulated C-V curve to a discrete component C-V curve is shown in Fig. 3-6. For this simulation resistance values are set to their ideal values in the SPICE model (i.e. R_{ito}=30 ohms, R_{i1}=infinity, R_{i2}=infinity, R_p=infinity, R_d=0 ohms, C_{i1}=2.2 nF, C_{i2}=2.18 nF, C_p=0.987 nF, BV=92 volts).

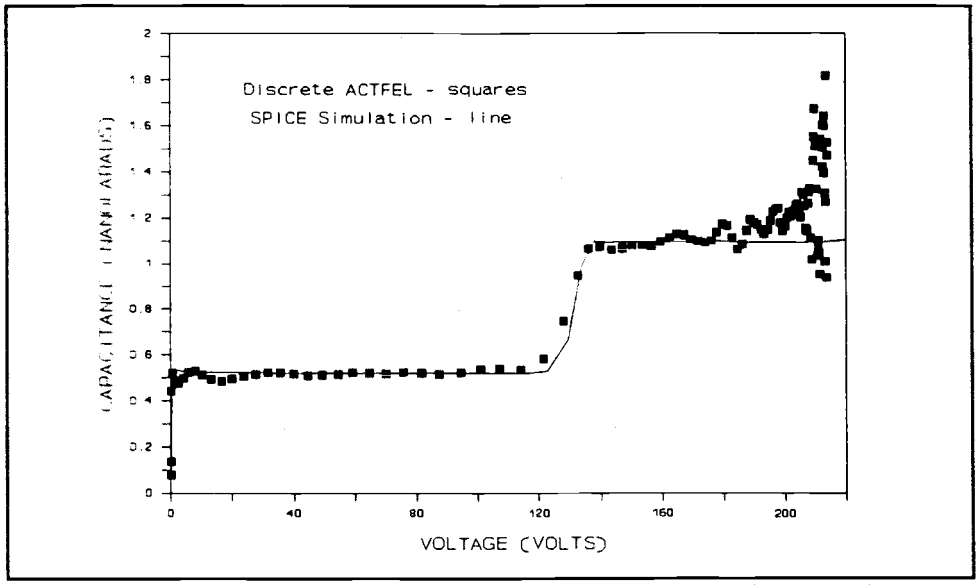

Figure 3-6. Comparison of SPICE C-V simulations with the discrete component ACTFEL device.

Finally, once the C-V measurement system is optimized it is necessary to compare measured and simulated ACTFEL C-V curves. A comparison of a typical measured ACTFEL C-V curve with a SPICE simulation of the same ACTFEL device is shown in Fig. 3-7. The agreement between the experimental and simulated curve is reasonably good except for the threshold region and near the maximum applied voltage. The

maximum applied voltage region of the C-V curve is noisy because capacitance arises from a ratio of the measured current and the derivative of the voltage across the ACTFEL device; these signals are both very small near the maximum applied voltage which results in a small signal-to-noise ratio.

The threshold region of actual ACTFEL C-V curves cannot be fit using the enhanced ACTFEL model. A further modification of the ACTFEL model is required which involves adding another capacitance, C_d. This capacitor is added in series in the diode branch and is placed between R_d and D_2. In combination with R_d this capacitor causes a time delay which extends the width of the threshold region to actual ACTFEL device widths as shown in Fig. 3-7.

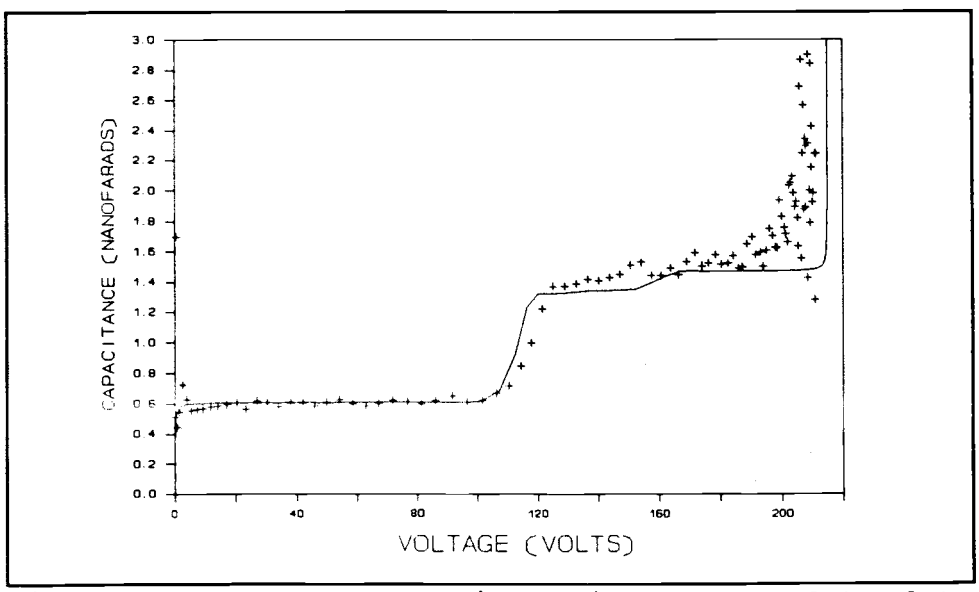

Figure 3-7. SPICE C-V simulation compared to data from a real ACTFEL device.

Please note that the need for this modification was recognized at the latter stages of the theses write-up and is not included in the SPICE-generated C-V variations that follow. Also, preliminary checks indicate that this capacitance does not affect C-V curves other than to adjust the width of the threshold region. The typical C_d value is of the order 100 nF.

3.6 SPICE SIMULATIONS

3.6.1 - introduction

In general, the ACTFEL electrical characteristics of interest are displacement and conduction currents, capacitance values, and threshold voltage. Using SPICE modeling these currents, capacitances, and threshold voltages are examined. The conduction charge, Q_{cond}, is found as the integral of conduction current through R_d, $I_{(Rd)}$. Q_{total} is the total charge, conduction and displacement, across the ACTFEL device and is evaluated as the integral of the total current through R_c, $I_{(R_c)}$. Analysis of the C-V curves provide C_{tot}, C_{ins}, and V_{th}. From evaluation of these parameters it is possible to show that variations in C-V curves are directly related to circuit parameters which represent specific layers of the ACTFEL structure.

SPICE simulation is used to examine trends that result

from parametric variations of R_{ito}, R_{i1}, R_{i2}, R_p, and R_d around nominal parameter values. Variations of R_s, the current limiting resistor in the C-V setup, are not examined. R_s is an external parameter that affects charge, capacitance, and threshold voltage; however, it is fixed at a value that causes little C-V curve variation. Table 3-1 shows circuit component values and ranges for SPICE modeling.

The nominal values are arrived at using a typical ACTFEL structure and process information supplied by Planar Systems and the methods described in Section 3.2.2. The ranges listed in Table 3-1 are for parameter variations that do not cause C-V curves to have unreasonable results.

Table 3-1. A summary of nominal circuit component values and their range of variation for SPICE modeling.

Parameter	Ideal Value	Nominal Value	Range
R_{ito}	0 ohms	30 ohms	0-100 ohms
R_i	infinite ohms	10^{11} ohms	10k-10^{14} ohms
R_p	infinite ohms	$2x10^6$ ohms	10^4-10^7 ohms
R_d	0 ohms	40 ohms	0-1000 ohms
R_s	1200 ohms	1200 ohms	not varied
BV	92 V	92 V	88-96 V

3.6.2 - charge, capacitance, and threshold voltage variations

The results of the parametric variation analysis are shown in Figs. 3-8 through 3-13. These trends are divided into three categories; charge, capacitance, and threshold voltage. Over the range of parameter variation many trends are evident.

Examining the charge trends first it is found that R_d, R_p, R_{ito} and R_i have little effect on Q_{total}, Q_{pol}, or Q_{rd}; since this is the case no plots of charge as a function of these parameters are provided. BV affects the charge and, as shown in Fig. 3-8, it is observed that BV causes a linear decrease in all charges with increasing BV. This is reasonable since the charge flowing is a function of the time during which the applied voltage is above threshold.

The capacitance trends are shown in Figs. 3-9 and 3-10 as a function of the parameters which displayed significant capacitance variation, R_d and R_{ito}, respectively. The first trend to observe is that there is no change in the total capacitance. The second is to observe there is a step change in the insulator capacitance in the conduction region of the C-V curve which depends upon R_d and R_{ito}. When the step occurs neither value of capacitance, C_{iu} or C_{il}, is the true insulator capacitance. This insulator capacitance step is due to modeling the ACTFEL device as a parametric capacitor specified by Eqn. (3-2); such a model

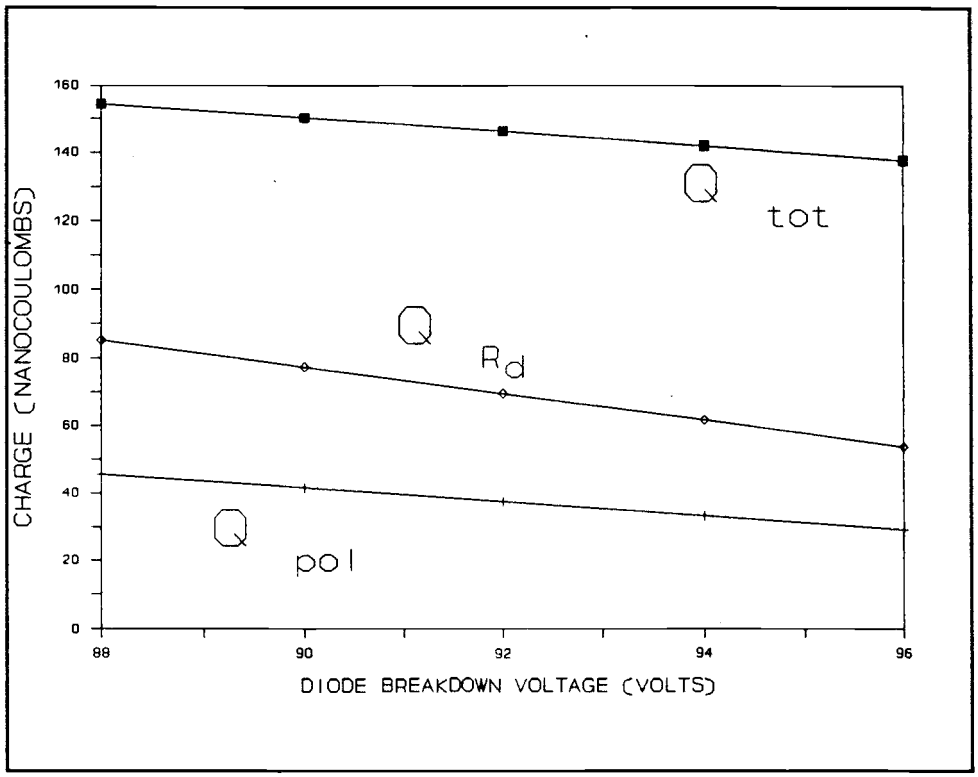

Figure 3-8. SPICE simulated charge versus diode breakdown voltage, BV.

does not adequately account for non-zero internal resistances present in the ACTFEL device. This effect is further explained later in this section. Parameter variations, for the ranges listed in Table 3-1, show that only R_d, causes a significant C_{ins} step as shown in Fig. 3-9. R_{ito} essentially causes the same step as R_d; however, R_{ito} is not expected to exceed 100 ohms for standard devices and for this range the C_{ins} step is not significant. Increasing the value of R_d causes an increase in the separation of C_{il} and C_{iu}.

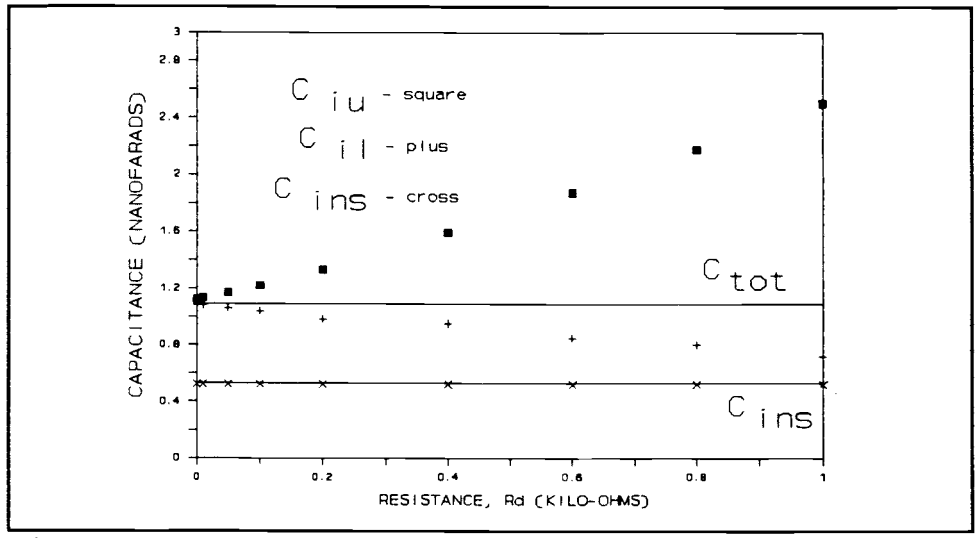

Figure 3-9. SPICE simulated capacitance versus resistance, R_d.

The threshold voltage is dramatically affected by R_d, BV, and R_p. These effects are shown in Figs. 3-11 through 3-13. Threshold voltage changes of over 30 volts are observed.

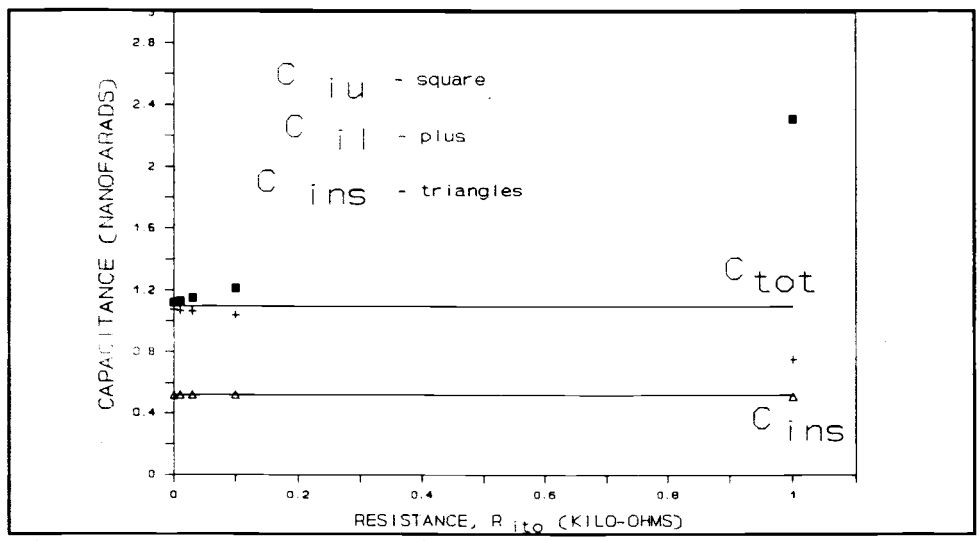

Figure 3-10. SPICE simulated capacitance versus resistance, R_{ito}.

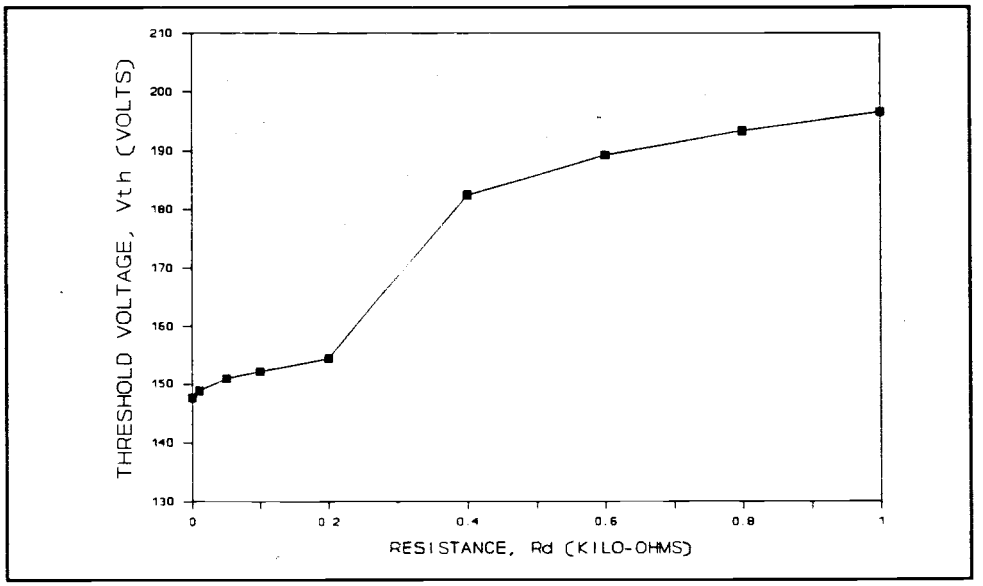

Figure 3-11. SPICE simulated threshold voltage, V_{th2}, versus resistance, R_d.

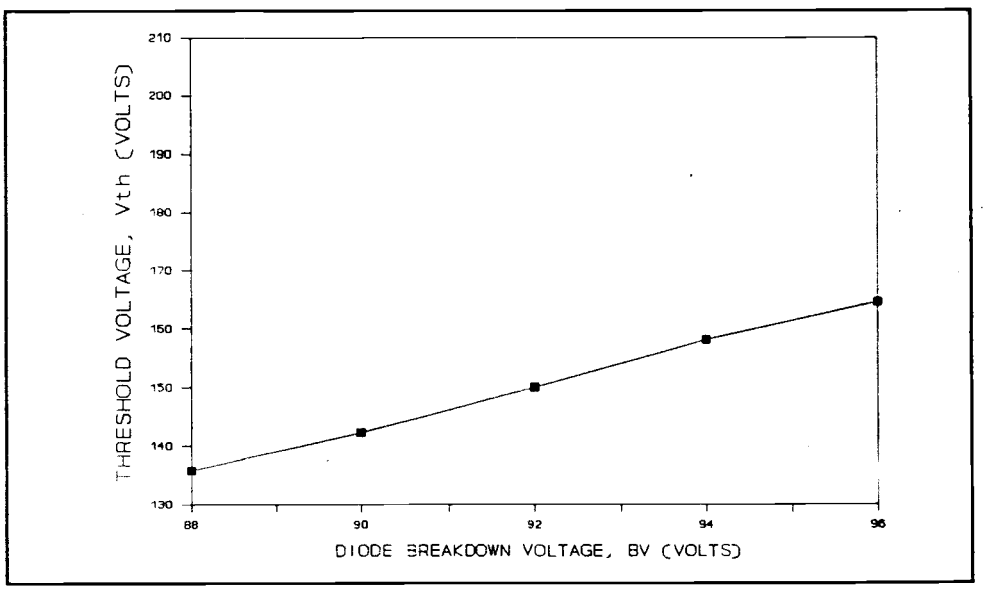

Figure 3-12. SPICE simulated threshold voltage, V_{th2}, versus diode breakdown voltage, BV.

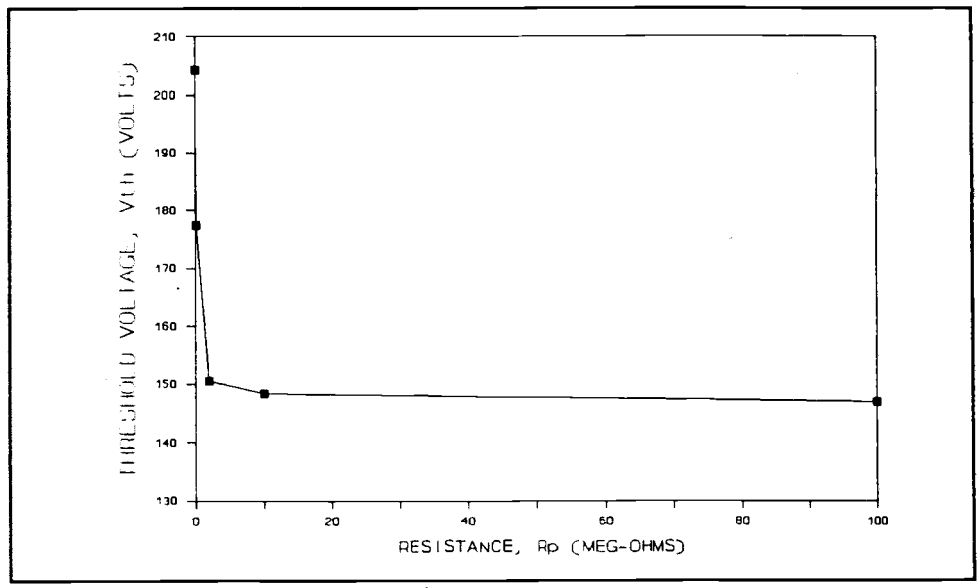

Figure 3-13. SPICE simulated threshold voltage, V_{th2}, versus resistance, R_p.

As shown in Fig. 3-11, R_d causes an increase in threshold voltage with increasing R_d. Increasing BV, as indicated in Fig. 3-12, results in a linear increase in threshold voltage over the BV range considered. Increasing R_p causes a decrease in threshold voltage as shown in Fig. 3-13, also R_p has no effect on threshold voltage for resistances larger than 10^6 ohms.

3.6.3 - C-V curve variations

By examining C-V curves it is possible to relate changes in these curves to variations in specific model parameters which can then be directly related to the physical ACTFEL structure. These changes are examined as

follows. C-V changes due to single parameters are discussed first and then a summary of the changes observed in various C-V regions is provided with an explanation of how to interpret these C-V changes. Refer to Fig. 3-5 for explanation of the terms in the following discussion.

R_{ito}, the ITO resistance, causes three effects as can be deduced from Fig. 3-14. The first effect is a simple RC time constant increase at low voltages in the subthreshold region. The second effect is a small change in the slope of the transition region while the third effect is an increase in the C_{ins} step in the conduction region. The RC time constant effect is consistent with having a resistor in series with a capacitor which introduces a time delay in charging the capacitor. The third effect is explained by examining a simple series RC network as shown in Fig. 3-15.

An analysis of a simple RC series network shows why the capacitance step exists. The following equation for voltage is obtained from a Kirchoff voltage law analysis of the circuit shown in Fig. 3-15,

$$V(t) = i(t) * R + \frac{1}{C}\int i(t)\, dt\,. \qquad (3\text{-}7)$$

Re-arranging this equation and solving for capacitance gives,

$$C = \frac{\int i(t)\, dt}{v(t) - i(t)\, R}\,. \qquad (3\text{-}8)$$

Without the resistor, the capacitance equation used in the C-V analysis, (3-2), is correct. However, the inclusion of a resistance leads to an additional term, i(t)R, which causes the calculated capacitance to be either larger or

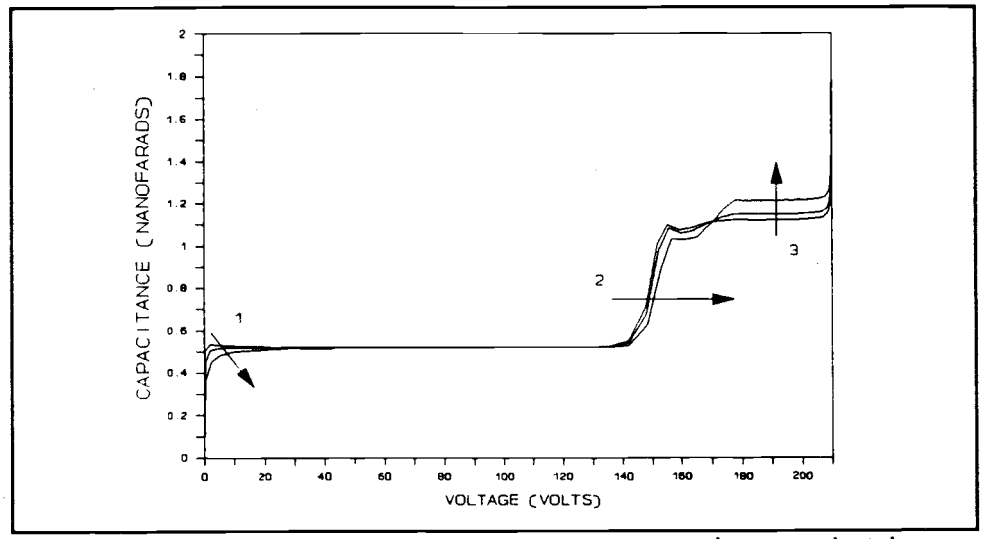

Figure 3-14. C-V curves for parametric variations of R_{ito}. R_{ito} = 0, 30, and 100 ohms. Arrows indicate an increasing value for R_{ito}.

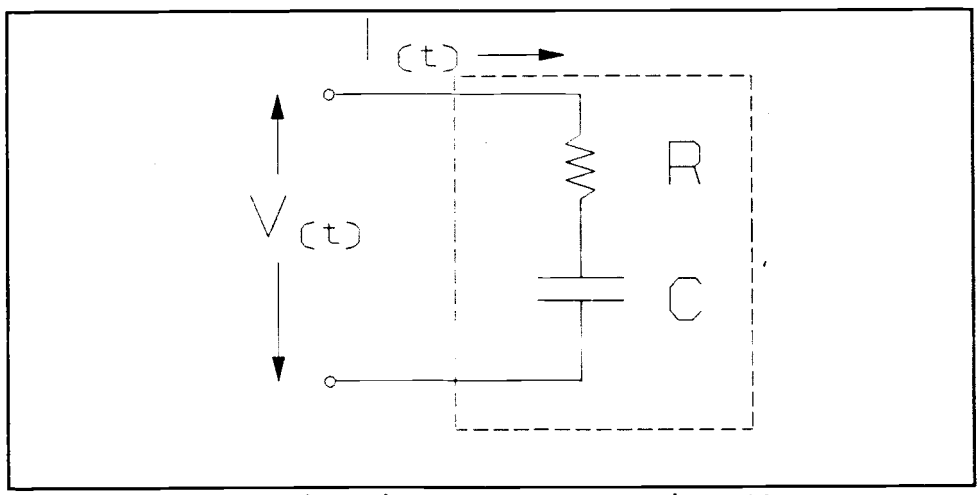

Figure 3-15. Circuit used to examine the capacitance step observed in C-V curves in the conduction region.

smaller than that of the expected capacitance by a factor related to the direction of current flow and the magnitude of the resistance.

R_i variations cause three effects, as shown in Fig. 3-16. First, we observe a small slope in the subthreshold capacitance, C_{tot}. Second, it is found that the threshold voltage shifts rigidly. The third effect is associated with changes in the nature of the insulator capacitance at high voltage in the conduction region. An examination of Fig. 3-17 indicates that R_p, has only one noticeable effect. Increasing R_p introduces a rigid shift in the threshold voltage to lower voltages.

Changing BV, as shown in Fig. 3-18, causes a rigid shift in the threshold voltage.

Fig. 3-19 shows that variations in R_d result in two effects. In the transition region we see that V_{th1} is fixed and V_{th3} moves to higher voltages with increasing R_d. This gives rise to a change in the slope of the capacitance in the transition region. This change in the slope of the transition region is also consistent with an increase in the density of interface states in the pre-clamping regime (threshold region of Fig.3-5). The second effect causes an increase in the difference between C_{il} and C_{iu} in the conduction region with C_{il} decreasing and C_{iu} increasing.

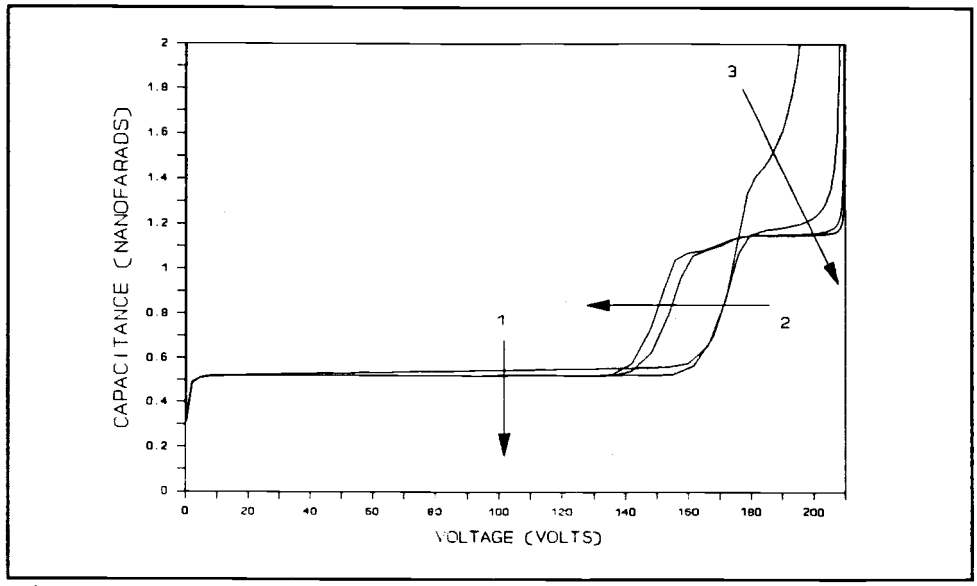

Figure 3-16. C-V curves for parametric variation of R_i. R_i=10k, 100k, 10^6, and 10^{14} ohms. Arrows indicate an increasing value for R_i.

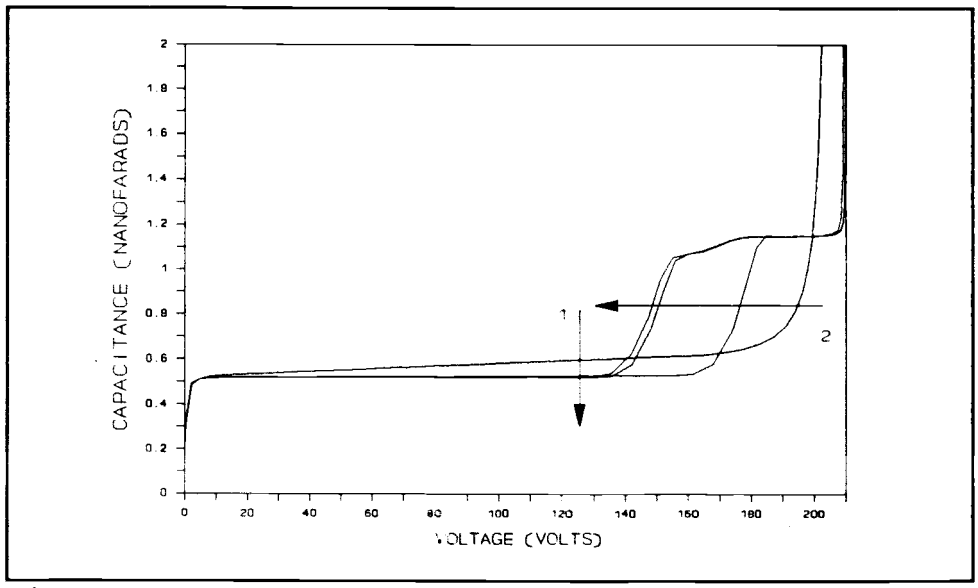

Figure 3-17. C-V curves for parametric variation of R_p.. R_p = 10k,100k,2x10^6, and 10^7 ohms. Arrows indicate an increasing value for R_p.

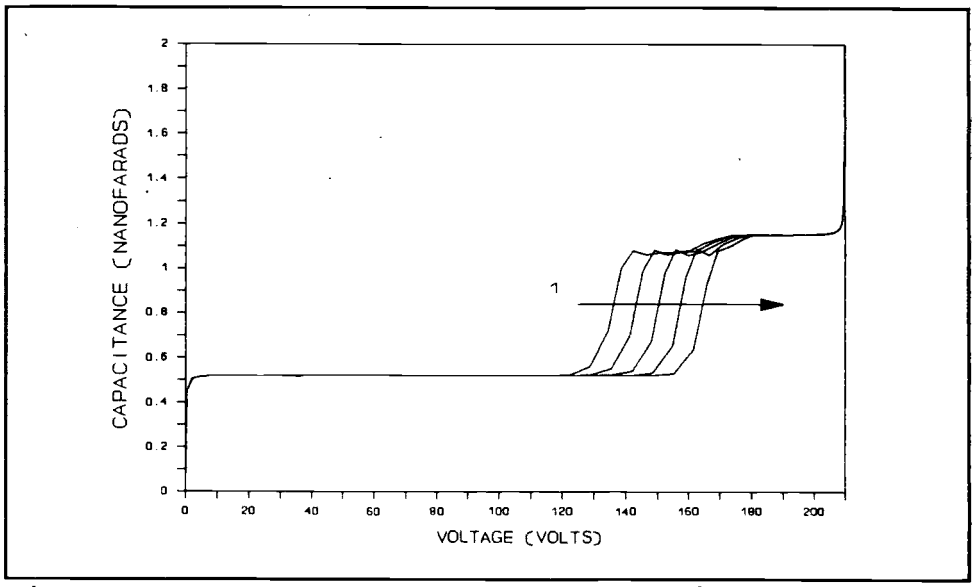

Figure 3-18. C-V curves for parametric variation of BV. BV = 88, 90, 92, 94, and 96 volts. Arrows indicate an increasing value for BV.

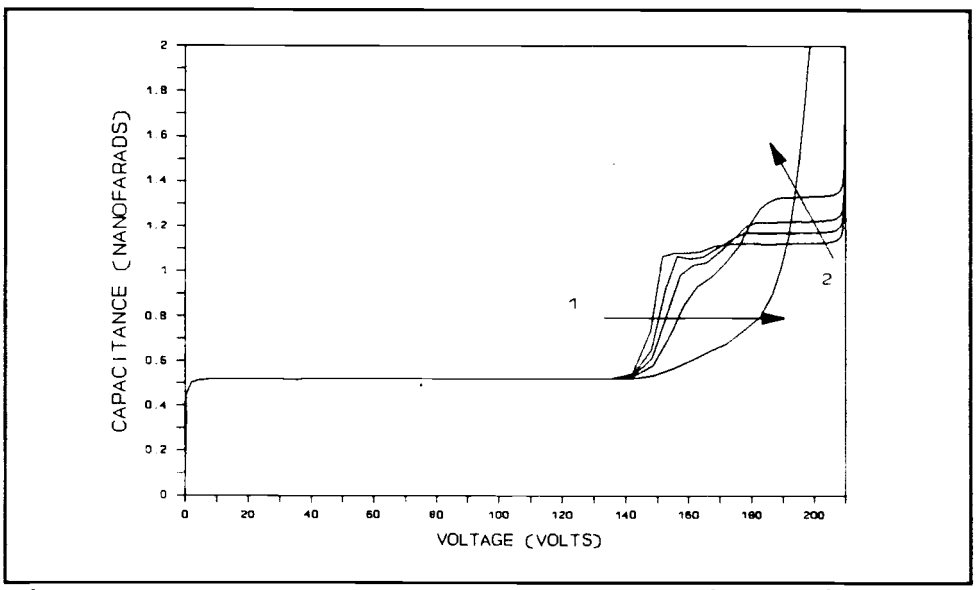

Figure 3-19. C-V curves for parametric variations of R_d. R_d = 0, 50, 100, 200, and 1000 ohms. Arrow indicates an increasing value for R_d.

The changing slope of the capacitance transition in the threshold region of the C-V curves may be explained as follows. R_d affects the abruptness of the C-V threshold with smaller R_d yielding a more abrupt transition. Physically, R_d corresponds to a resistance associated with hot electron injection from interface traps. Thus, R_d is related to the characteristic time for electron emission from an interface trap such that we interpret a smearing out of the C-V transition as arising from traps having time constants of similar magnitude as the characteristic times of the driving waveform.

These changes in the C-V curves that have just been enumerated may be placed into five categories which are summarized in Table 3-2.

1) an RC time constant rise in the capacitance in the subthreshold region,
2) a change of slope of the capacitance transition in the threshold region,
3) a rigid threshold voltage shift in the threshold region,
4) a change in the difference between C_{il} and C_{iu}, and
5) a change in the capacitance rise near V_m in the conduction region.

R_{ito} is the only parameter that causes a change in the RC time constant rise. This effect is expected to be nearly undetectable for R_{ito} less than 100 ohms. When R_{ito} increases above 100 ohms then the effect is more apparent. The value of R_{ito} may be evaluated from C-V analysis by

choosing the appropriate value for R_{ito} in the SPICE simulation that provides agreement with the measured C-V curve.

Table 3-2. Summary of the effect of parameter variations on C-V curves.

	C-V curve effect				
Parameter	RC Rise	Slope Change	Rigid V_{th} shift	C_{il} and C_{iu} Variations	Insulator capacitance rise
R_s	no	no	no	no	no
R_{ito}	yes	yes	no	yes	no
R_i	no	no	yes	no	yes
R_p	no	no	yes	no	no
R_d	no	yes	no	yes	no
BV	no	no	yes	no	no

R_d and R_{ito} are the only parameters that cause a noticeable change in the slope of the capacitance transition in the threshold region. R_d and R_{ito} effects are easily distinguishable since any change in the capacitance of the sub-threshold region indicates that R_{ito} has changed. If there is only a change in the slope in the threshold region then R_d is the parameter that has changed.

R_p, R_i, and BV all cause rigid shifts in threshold

voltage. Assuming insulators of high quality , R_i can be eliminated as a possible cause of rigid shifts in V_{th}. R_p and BV changes are not separable for reasonable values of R_p and BV. For R_p less than $1 x 10^5$ ohms; however, it is possible to separate R_p from BV effects.

R_i variations yield small changes in the capacitance rise in the conduction region. However, since the insulators employed in this study are found to be of high quality, only R_i values of unrealistic magnitudes give rise to such changes.

3.7 SUMMARY

In this chapter the utility of SPICE modeling in conjunction with an equivalent circuit model of the ACTFEL device for the interpretation of C-V curves is demonstrated. It is shown that simple methods may be used to give reasonably accurate SPICE circuit element parameters. Comparison of measured ACTFEL C-V results with SPICE simulations show good agreement, thereby reenforcing the viability of parameters used in the model. Changes in C-V curves are interpretable in terms of SPICE circuit parameters which in turn are related to specific layers of the ACTFEL structure. In this manner, the C-V technique is a useful aid for ACTFEL diagnostics and may be well suited to quality control and lifetime monitoring. It is believed that C-V analysis and SPICE modeling provide new device

physics insight into the nature of ACTFEL operation and are useful methods for exploring ACTFEL aging instabilities.

CHAPTER 4 - ACTFEL AGING INSTABILITY ANALYSIS

4.1 INTRODUCTION

The electronic nature of semiconductor devices is controlled, to a large extent, by the intrinsic and extrinsic doping of the material either in the bulk or at interfaces between different materials. Doping may consist of an addition of impurities or defects to the host material due to processing steps. These impurities or defects form sites at which electrons may be sourced and trapped. The sites are characterized by their specific energies in the energy band.

Whether or not traps are stable in energy and physical location determines the aging characteristics of a device. A measure of the activation energy associated with aging provides the link between device behavior and the microscopic identity of the process giving rise to aging and, thus, aids in understanding the nature of the aging process.

In this chapter the shift in the C-V threshold voltage with short-term aging time and as a function of temperature is measured. The short-term aging kinetics are then analyzed and an activation energy for the initial aging process is deduced. Based on the magnitude of the measured short-term activation energy, a discussion of possible atomic mechanisms responsible for aging and how they occur is provided.

4.2 EXPERIMENTAL TECHNIQUE

4.2.1 - experiment description

The aging experiment consists of monitoring the C-V threshold voltage, V_{th2}, with aging time and as a function of temperature. The experiment is performed using a single glass substrate, provided by Planar Systems, that has 10 aluminum dots. Aging occurs over a temperature range of -50 °C to 80 °C. The aging duration is 45 hours using the standard waveform described in Section 3.3 with a voltage amplitude of 210 volts. Temperature is controlled using a Blue-M environmental furnace. Thermocouples located in the furnace near the sample record the temperature. Threshold voltage sampling is performed automatically with a computer-controlled system using the C-V analysis technique described in Chapter 3. The threshold voltage is obtained graphically from the C-V curves generated. Over the aging duration 56 threshold voltages are determined. Threshold voltage sampling occurs more rapidly during the rapid initial aging and then slows down as the sample approaches its saturated threshold voltage.

Fig. 4-1 shows a block diagram of the ACTFEL aging measurement system. The following equipment is used for this aging experiment.

1) OMEGA microprocessor thermometer model HH22,
2) BLUE-M environmental chamber,
3) Wavetek arbitrary waveform generator model 275,
4) APEX operational amplifier model PA-85,

5) Tektronix 7854 digitizing oscilloscope, and
6) IBM 286 compatible computer with GPIB capability,

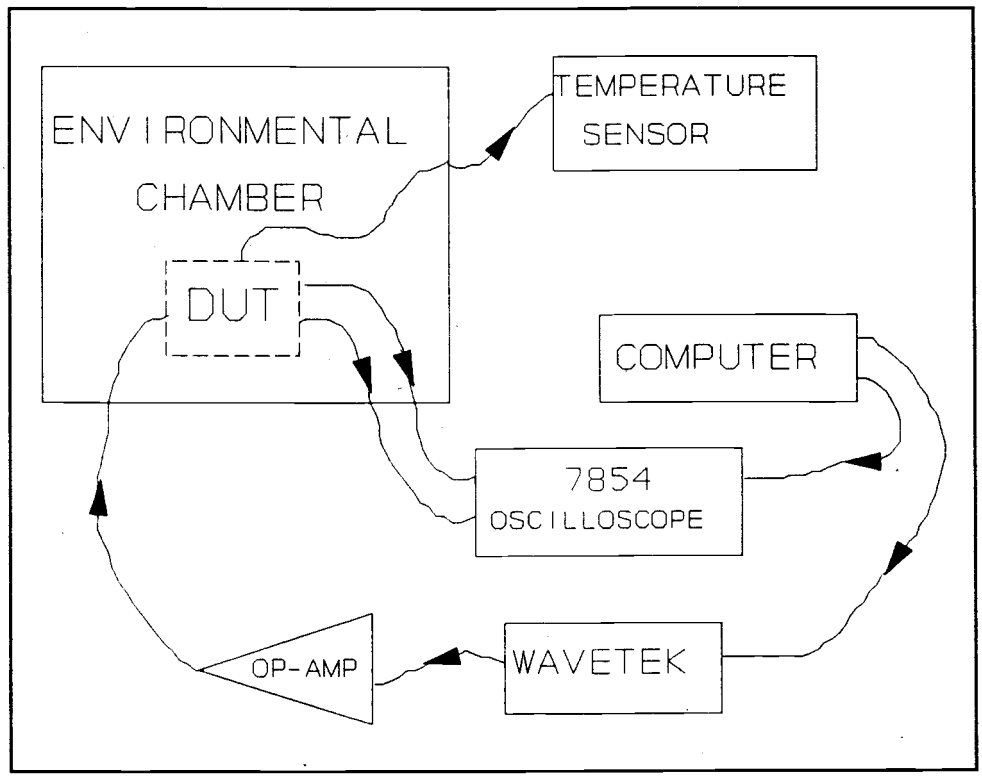

Figure 4-1. Block diagram of the aging experimental setup.

4.2.2 - initial conditions

The ACTFEL sample consists of 10 dots on a 2x2 inch glass substrate which is processed using Planar Systems standard process. A dot consists of a ¼ inch diameter aluminum circle. The standard Planar Systems process is described in Section 2.2.

The Planar Systems ACTFEL device needs a slow warm-up to full operating voltage to ensure self-healing of defects that otherwise could cause burn-out. A room temperature

warm-up of the 10 dots is employed which starts at 10 volts and goes to 210 volts in 3 volt steps which occur every three seconds. This yields a warm-up time of approximately 35 minutes. Threshold voltage is then determined for each dot and is found to vary from 126 to 114 volts. As necessary, each sample dot is pre-aged to obtain V_{th2} = 125 volts, to within 2 percent; this insures that all of the dots are initialized in the same manner.

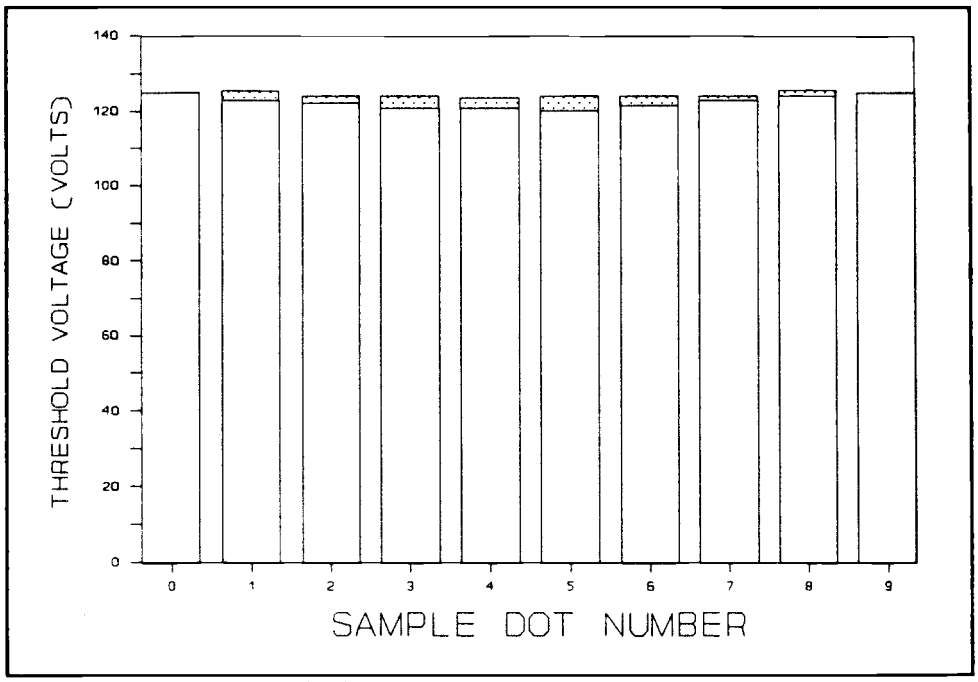

Figure 4-2. Initial room temperature threshold voltages, V_{th2}, for glass 7-26-90-15 and adjusted threshold voltages at which the aging experiments begin.

Figure 4-2 shows the initial threshold voltage after the warm-up procedure and the subsequent adjusted threshold at which the aging experiment begins. It is generally assumed that processing yields consistent thickness and

composition in each layer and so variations in the threshold voltage are attributed to differing trap densities and energies. By forcing each dot to have the same adjusted threshold voltage, it is believed they are initialized in the same manner and that the aging results of each dot can be directly compared. The time necessary to adjust the initial threshold voltage is a maximum of 100 seconds. It is also suspected that some aging may occur due to temperature alone, independent of the application of a voltage waveform; because of this, the aging experiments are performed at the low temperatures first so as to introduce as little shift due to temperature as possible.

4.3 AGING RESULTS

The results of ACTFEL aging experiments using glass number 7-26-90-15 are shown in Figs. 4-4 through 4-11 for the following temperatures: -50 °C, -10 °C, 0 °C, 20 °C, 60 °C, and, 80 °C. A characteristic family of C-V curves and the shift in threshold voltage for each temperature are shown and discussed below.

The family of selected C-V curves shown in Fig. 4-3 are for the 60 °C experiment. These C-V curves show characteristics typical of all aging experiments at various temperatures. In general, it is observed that the threshold voltage shifts rigidly with operating time and C_{tot} and C_{ins} remain essentially constant to within experimental error.

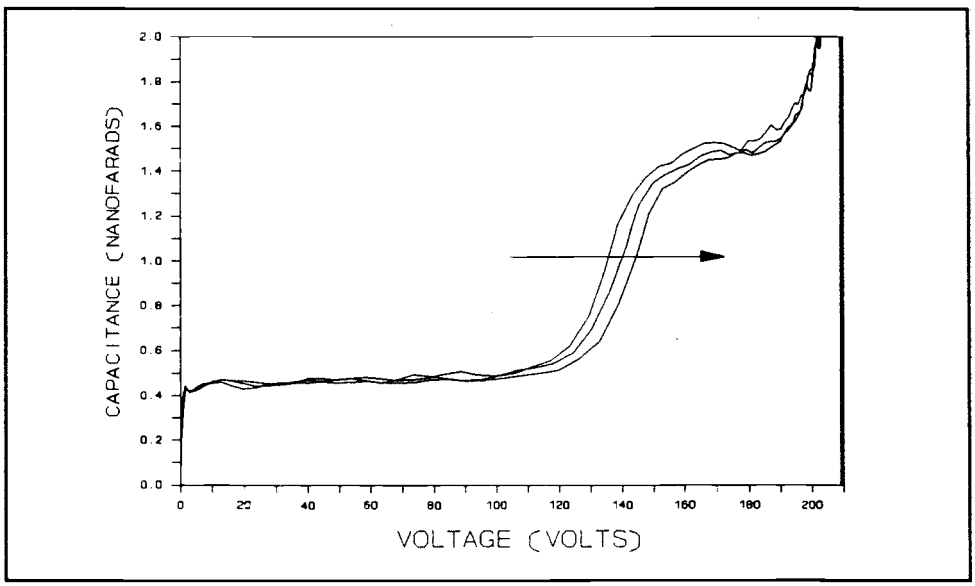

Figure 4-3. Family of C-V curves for the 60 °C experiment with aging times of 1 second, 20 minutes, 9.5 hours. Arrow indicates direction of threshold voltage shift with aging time.

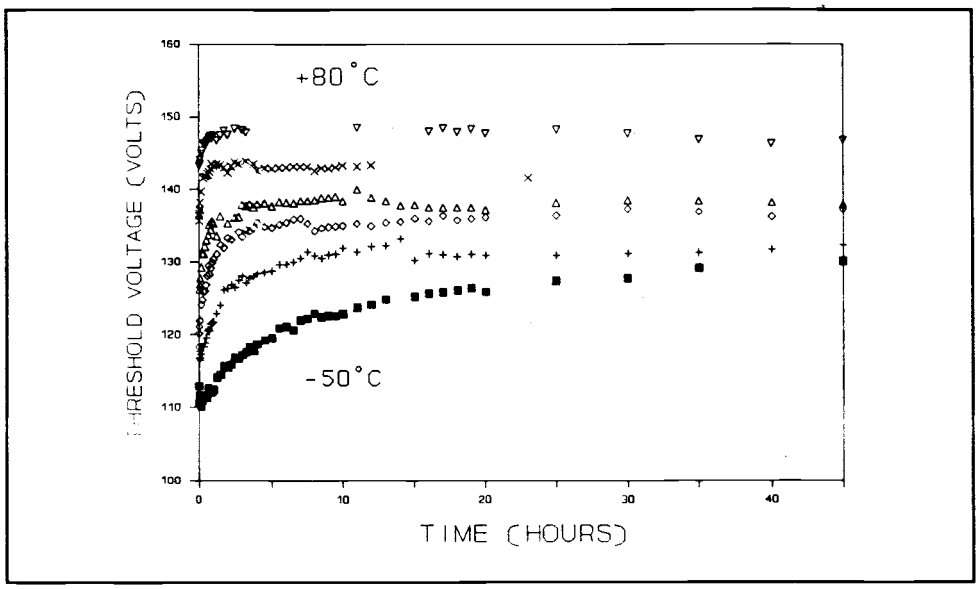

Figure 4-4. Threshold voltage, V_{th2}, for all temperatures as a function of aging time.

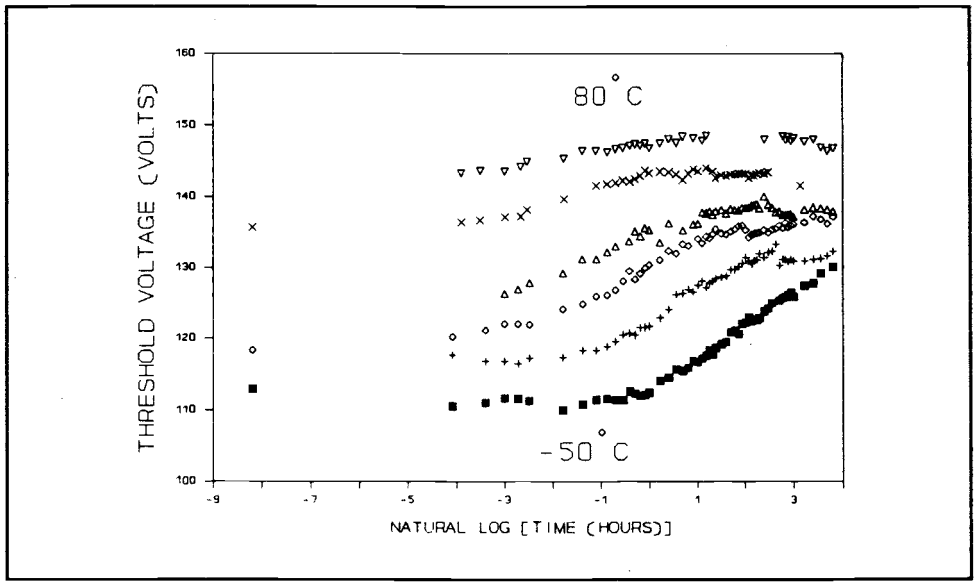

Figure 4-5. Threshold voltage, V_{th2}, for all temperatures as a function of the natural logarithm of aging time.

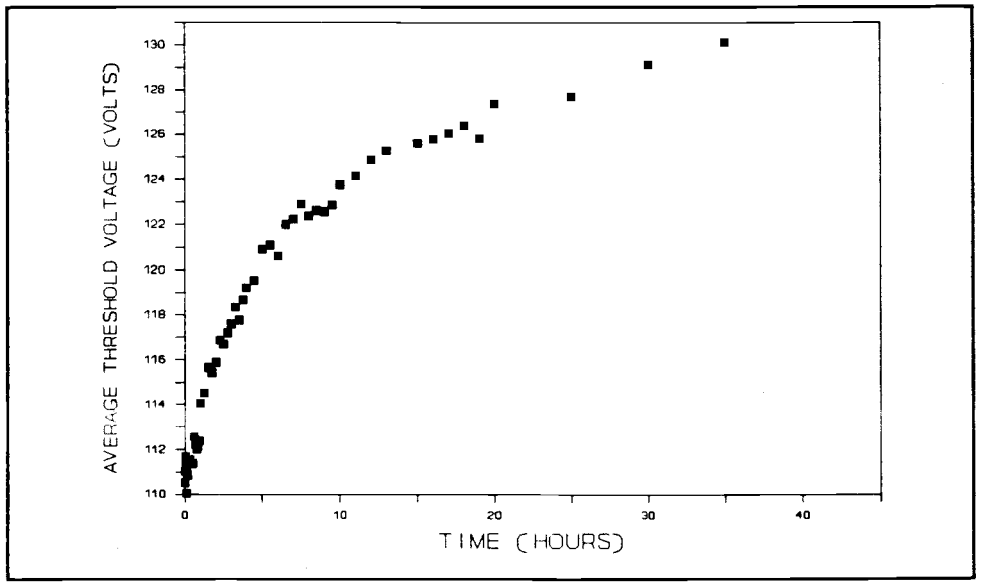

Figure 4-6. Threshold voltage, V_{th2}, as a function of aging time at a temperature of -50 °C.

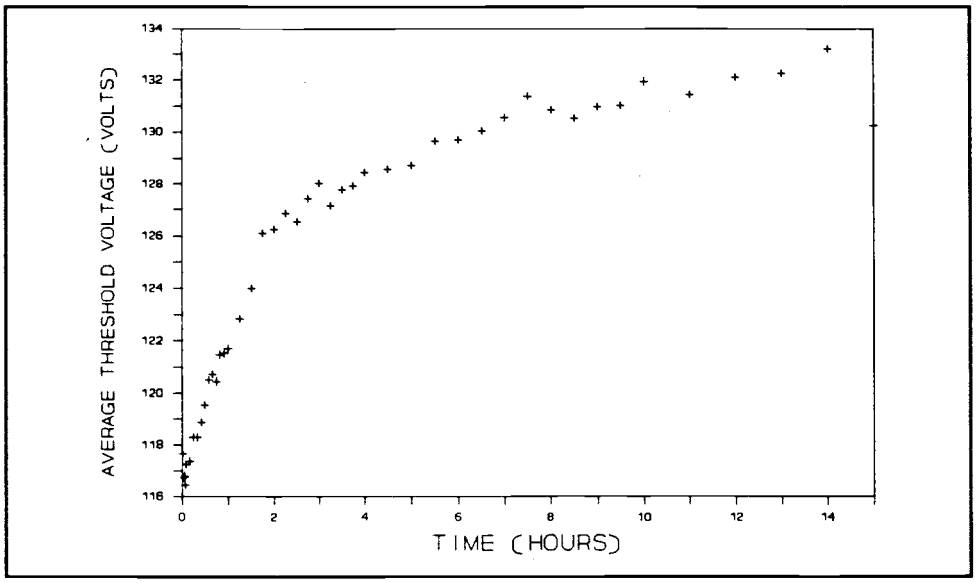

Figure 4-7. Threshold voltage, V_{th2}, as a function of aging time at a temperature of -10°C.

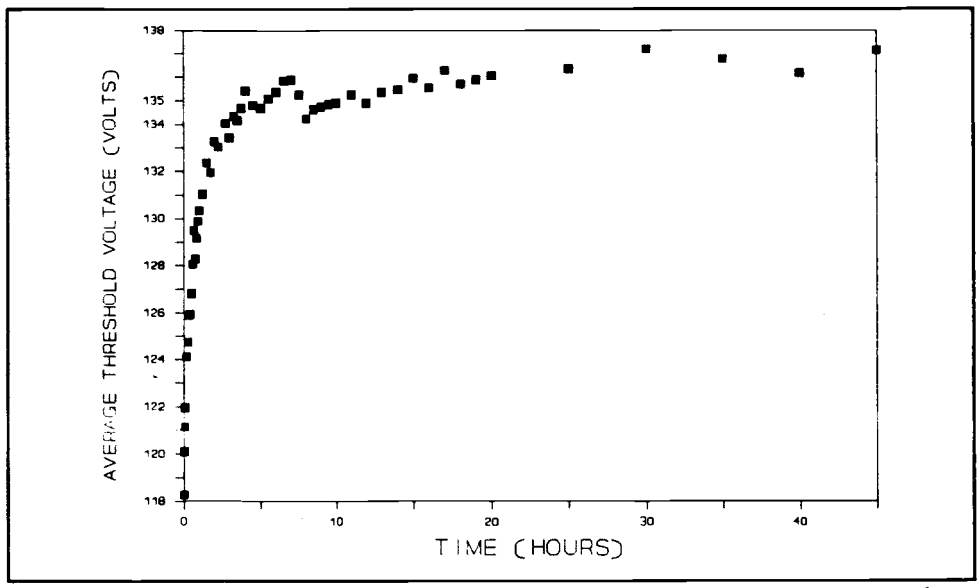

Figure 4-8. Threshold voltage, V_{th2}, as a function of aging time at a temperature of 0 °C.

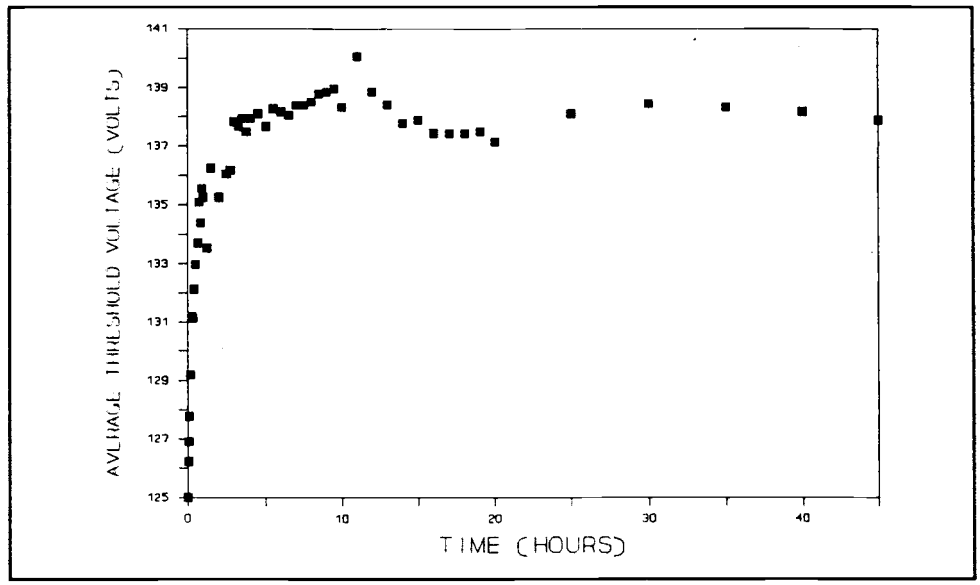

Figure 4-9. Threshold voltage, V_{th2}, as a function of aging time at a temperature of 20 °C.

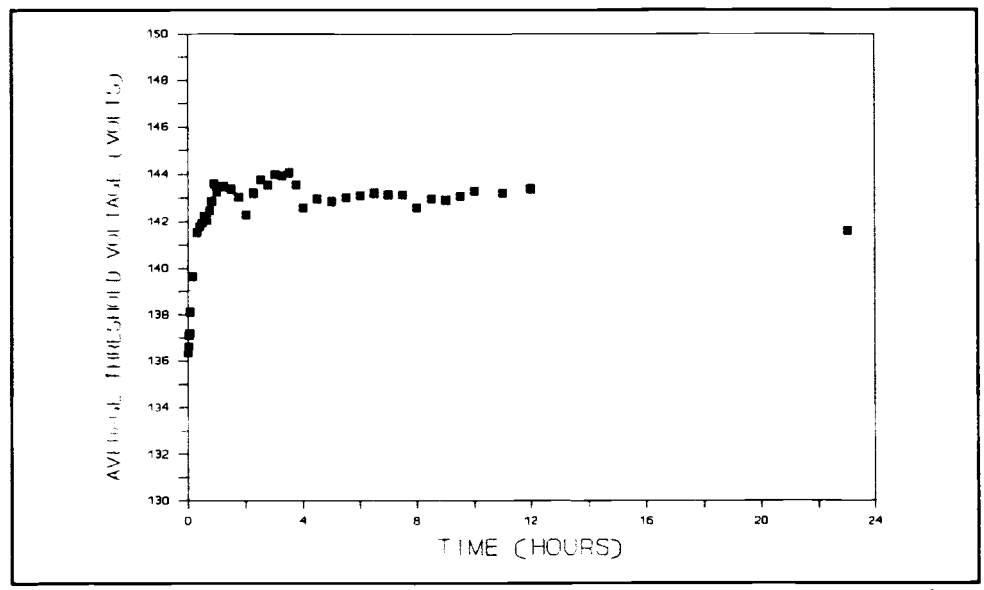

Figure 4-10. Threshold voltage, V_{th2}, as a function of aging time at a temperature of 60 °C.

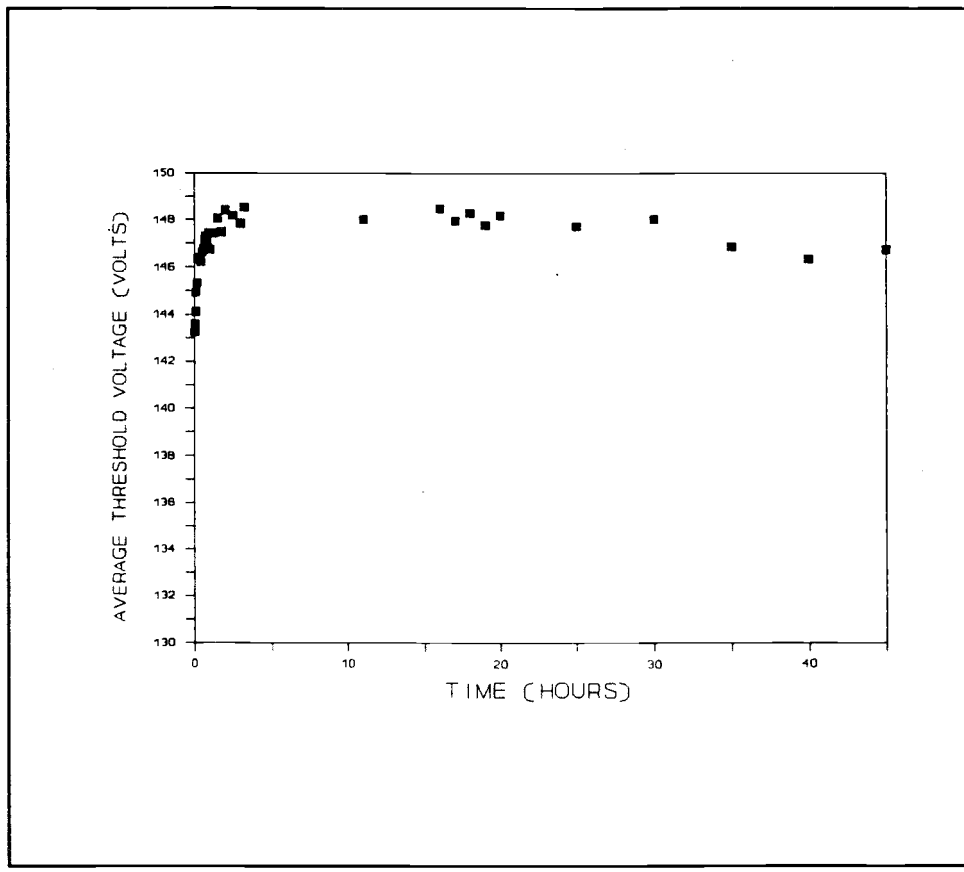

Figure 4-11. Threshold voltage, V_{th2}, as a function of aging time at a temperature of 80 °C.

The characteristics of the threshold voltage shifts are discussed as follows. As can be observed from Figs. 4-4 and 4-5, the aging characteristics can be classified into four regimes:

1) incubation period,
2) logarithmic aging,
3) saturation, and
4) long-term aging.

At lower temperatures there is an incubation period, in which the threshold voltage is essentially constant. This

incubation period lasts one hour at the lowest temperature (-50 °C) and eventually disappears at and above room temperature (20 °C). The incubation period is followed by a period in which the threshold voltage increases logarithmically with aging time. Next, the threshold voltage approaches a saturated value which is temperature-dependent. The logarithmic and saturation regimes are collectively referred to as constituting the short-term aging regime, which is of primary importance in this thesis. As expected, the aging rate increases as temperature increases. At higher temperatures (60 °C and 80 °C) the aging occurs so rapidly that only a very small window of time exists during which the threshold voltage depends exponentially on time. Since the analysis of the short-term aging kinetics depends exclusively on the exponential period, where the change in threshold voltage is linear with respect to the natural logarithm of time, this window must be selected carefully in order to avoid an analysis which includes long-term aging mechanisms and which could result in negative activation energy.

Finally, the last aging regime is denoted long-term aging in which the threshold voltage decreases slowly with increasing aging time. Previous room-temperature aging experiments over an aging period of 65 hours show a tendency for the threshold voltage to subsequently decrease slightly after about 50 hours of aging. This decrease is on the

order of a few volts over this 15 hour period. This effect is not observed in the 45 hour experiments until the temperature exceeds about 60 °C. Thus, choosing an aging time of 45 hours is nearly optimal for the analysis of the primary mechanism of ACTFEL aging. However, termination of the experiment at 45 hours precludes analysis of the mechanism of long-term aging.

During the aging experiment it is observed that the initial threshold voltage for each dot is not necessarily the same as for the pre-aged, room temperature, threshold voltage. Figure 4-12 shows the temperature dependence of the -50 °C dot. This data is obtained after the temperature experiment is completed. The ramping of temperature took less than one hour so little aging occurred during the acquisition of this data. The graph clearly shows a linear dependence of the threshold voltage on temperature. By plotting the initial and final threshold voltage for the aging data at each temperature, as shown in Fig. 4-13, a similar linear dependence with temperature is observed.

The cause of the temperature dependence of the threshold voltage is uncertain. The temperature dependence of the insulator capacitance was checked, using a HP4280A 1MHz capacitance meter, from 20 °C to 95 °C and found to vary only 4 percent. This small variation in the dielectric constant is insufficient to explain the observed threshold voltage temperature-dependence.

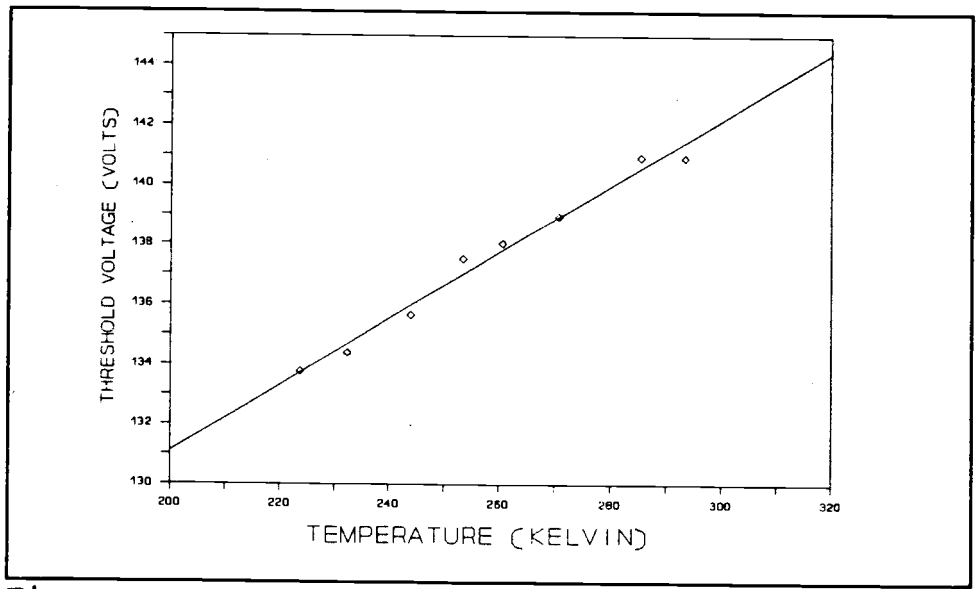

Figure 4-12. Temperature dependence of the -50 °C dot threshold voltage, V_{th2}, after the aging experiment was completed.

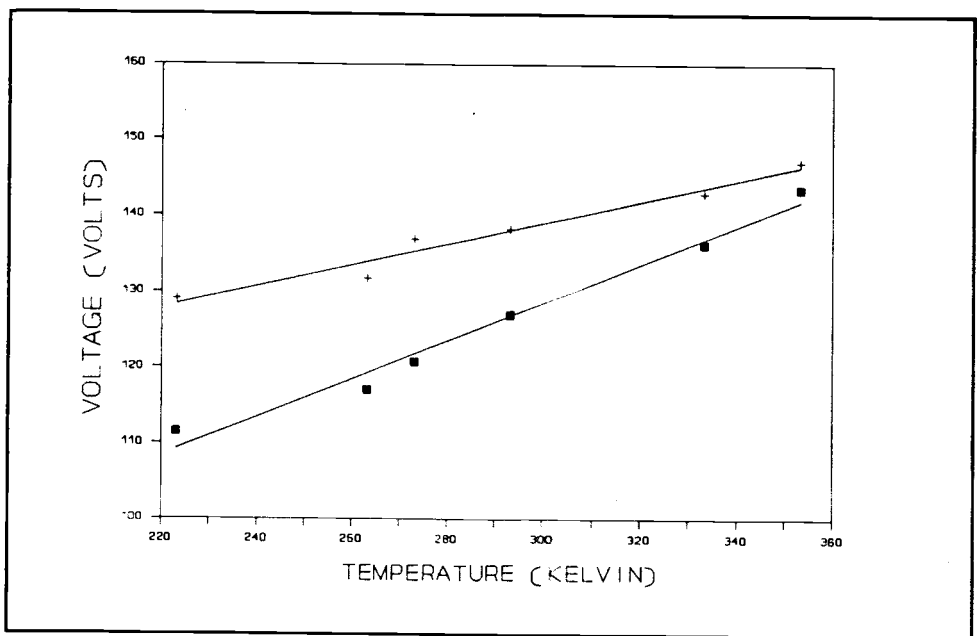

Figure 4-13. Initial and final threshold voltages, V_{th2}, for all aging samples as a function of temperature.

4.4 ACTIVATION ENERGY EXTRACTION

4.4.1 - Arrhenius analysis

Arrhenius proposed that, over a limited range of temperature, the rate constant, α, of a process depends exponentially on temperature as

$$\alpha = A \exp\left(\frac{-E_a}{k_B T}\right) \qquad (4\text{-}1)$$

where **A** is a pre-exponential factor, E_a is the activation energy, and k_B is the Boltzmann constant. Writing (4-1) in logarithmic form gives

$$\ln(\alpha) = -\frac{E_a}{k_B T} + \ln(A) \qquad (4\text{-}2)$$

which yields a straight line when the logarithm of the rate constant, α, is plotted against the reciprocal of the absolute temperature. The slope of this line gives the activation energy whereas the intercept is related to the pre-exponential factor.

Not all experimental results give rise to a rate constant with simple exponential Arrhenius behavior. Specifically, if the incubation and long-term aging periods are temporarily ignored, ACTFEL aging experiments show an increase in the threshold voltage which depends logarithmically on the aging time and a subsequent threshold voltage saturation. Further, there is a temperature-dependence on the threshold voltage that is relatively

independent of aging and which needs to be taken into account. The following equation is found to fit the ACTFEL aging data in the logarithmic and saturation regions and to account for the temperature-dependence of the threshold voltage;

$$\Delta V_{th}(t) = \Delta V_{th}^{SAT}(T)\ [\,1-\exp(-\alpha\, t)\,] \qquad (4\text{-}3)$$

where $\Delta\ V_{th}(t)$ is the measured change in threshold voltage which is evaluated from the experimental aging data, $\Delta V_{th}^{SAT}(T)$ is the difference between the saturation threshold voltage and the initial threshold voltage, and α is the rate constant characteristic of the ACTFEL aging process. Equation (4-3) can be rearranged to yield

$$\alpha\, t = \ln\left[\,1 - \frac{\Delta V_{th}(t)}{\Delta V_{th}^{SAT}(T)}\,\right] \qquad (4\text{-}4)$$

Therefore, a plot of the right hand side of (4-4) versus time should result in a linear relationship in time, the slope of which corresponds to the rate constant, α. If α is extracted for each temperature and plotted versus the inverse of the absolute temperature, the slope of such a plot yields the activation energy for ACTFEL aging.

4.4.2 - activation energy from aging kinetics

Each of the six sets of data shown in Figs. 4-5 through 4-10 is plotted according to Eqn. (4-4) and these normalized

threshold voltage difference curves are given in Figs. 4-14 through 4-19. $\Delta V_{th}^{SAT}(T)$ is found for every temperature from the experimental data and the rate constant, α, is determined from best fit of the linear region of the normalized plots of the change in the threshold voltage as shown in Figs. 4-14 through 4-19. The correlation of fit, R^2, of the linear portion of the curve to α varied from 0.87 to 0.98 with an average fit of 0.92, as is summarized in Table 4-1. The rate constant for each temperature is then plotted as a function of inverse absolute temperature to obtain an Arrhenius plot as shown in Fig. 4-20. A best fit of the experimental data yields the straight line shown in Fig. 4-20 from which the parameters summarized in Table 4-2 are extracted. The slope of this line, which corresponds to the threshold voltage activation energy, has a value of approximately 0.2 eV.

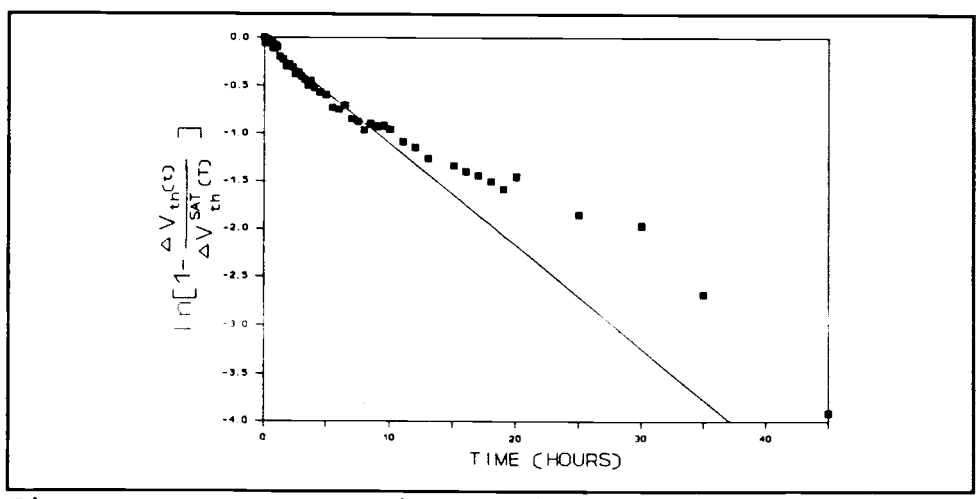

Figure 4-14. Normalized shift in threshold voltage, V_{th2}, as a function of aging time at a temperature of -50 °C.

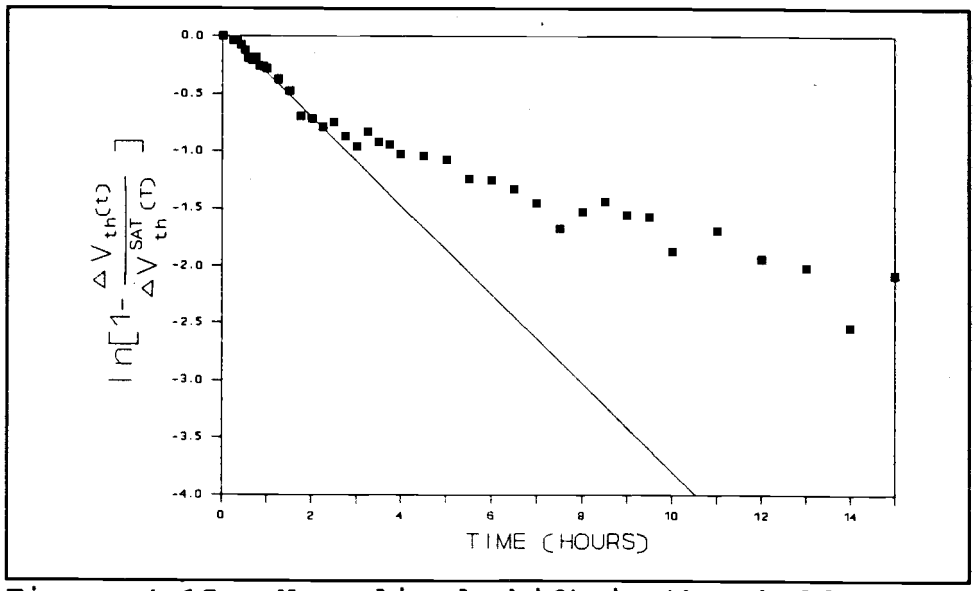

Figure 4-15. Normalized shift in threshold voltage, V_{th2}, as a function of aging time at a temperature of -10 °C.

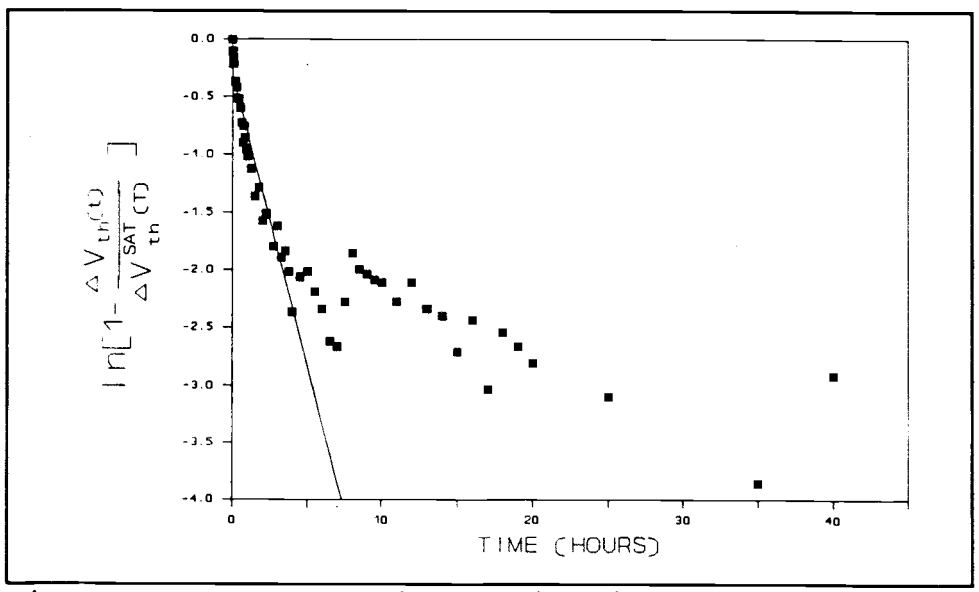

Figure 4-16. Normalized shift in threshold voltage, V_{th2}, as a function of aging time at a temperature of 0 °C.

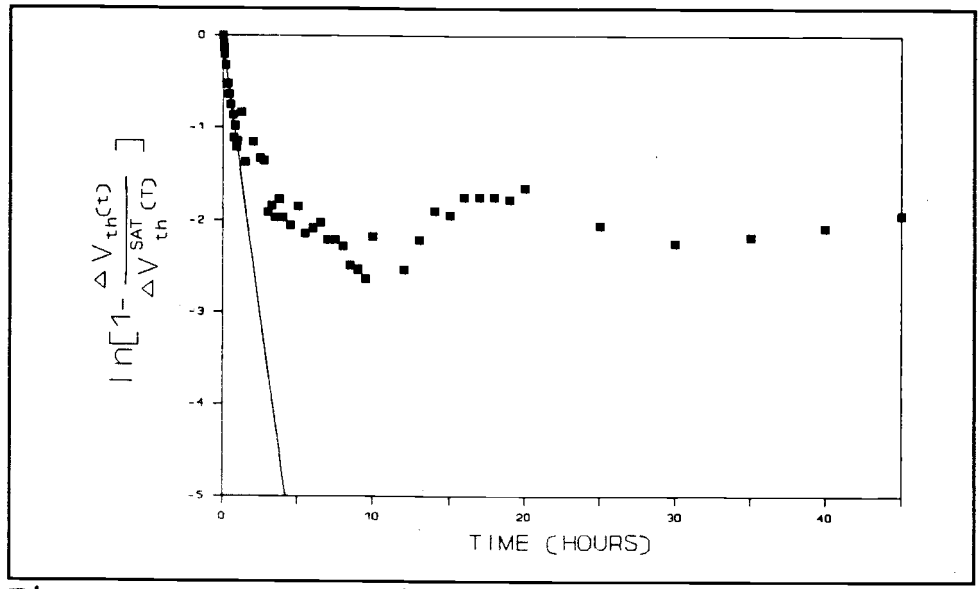

Figure 4-17. Normalized shift in threshold voltage, V_{th2}, as a function of aging time at a temperature of 20 °C.

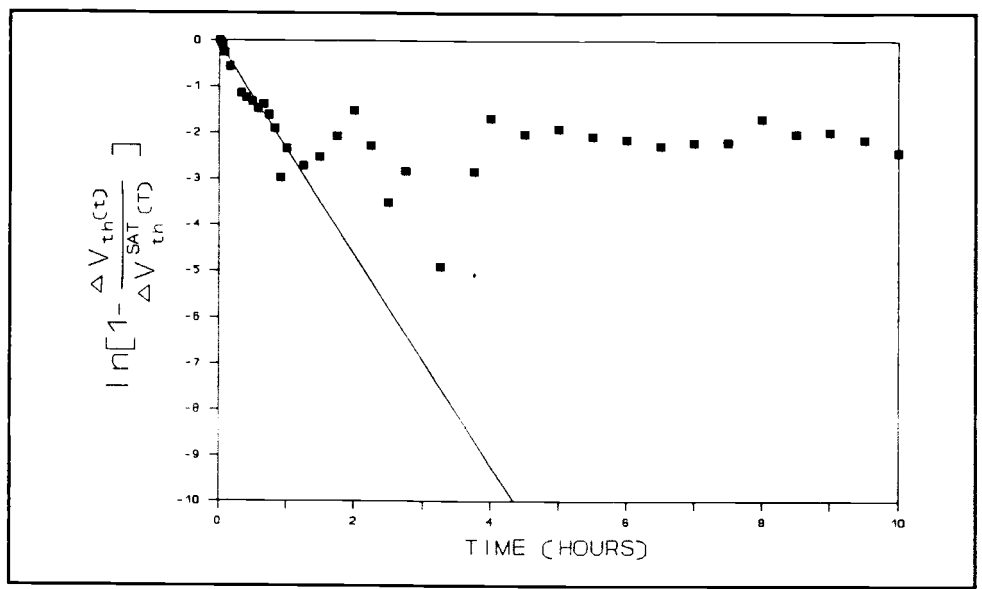

Figure 4-18. Normalized shift in threshold voltage, V_{th2}, as a function of aging time at a temperature of 60 °C.

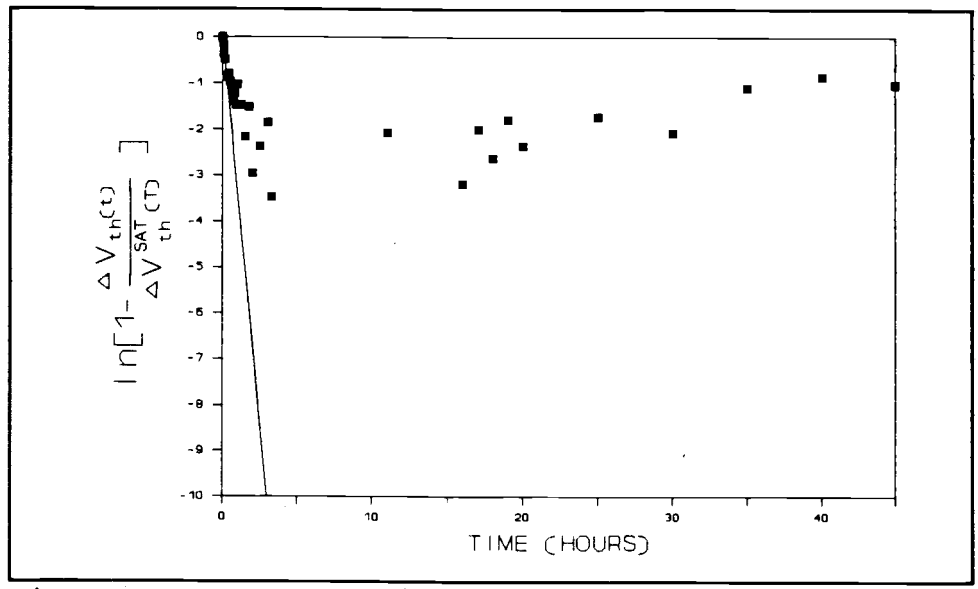

Figure 4-19. Normalized shift in threshold voltage, V_{th2}, as a function of aging time at a temperature of 80 °C.

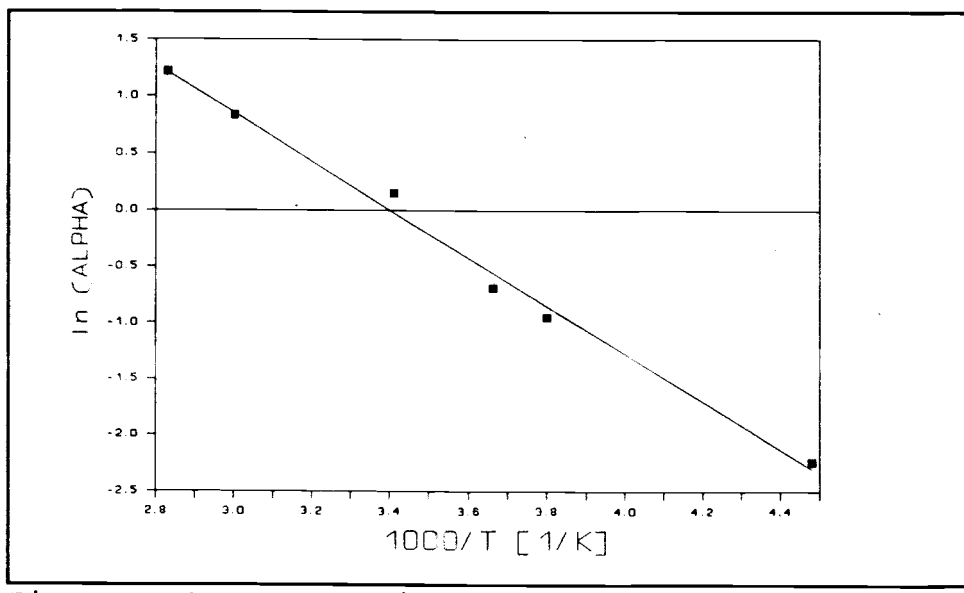

Figure 4-20. Arrhenius plot of the aging experiment data.

Table 4-1. Summary of temperature-dependent rate constants, intercepts, and correlation of fit.

Temperature (°C)	Rate Constant α (1/hrs)	Intercept $\ln[1-\frac{\Delta V_{th}(t)}{\Delta V_{th}^{SAT}(T)}]$	R^2 Fit
-50	-0.1067	-0.0405	0.9689
-10	-0.3870	0.0714	0.9782
0	-0.5046	-0.3171	0.9390
20	-1.1664	-0.1044	0.9601
60	-2.2952	-0.0497	0.9515
80	-3.3781	0.0478	0.8669

Table 4-2. The Arrhenius straight line fit parameters.

Slope	intercept (ln[**A**])	R^2 fit	Pre-exponential factor (sec^{-1})	Activation Energy, E_a (eV)
-2.1286	7.2383	0.9923	0.3866	0.1835

4.5 AGING ELECTROSTATICS

C-V curves for the short-term regime are characterized by:

1) C_{tot} and C_{ins} do not vary appreciably with aging time,
2) the C-V transition region shifts rigidly with aging time, and
3) the threshold voltage increases with aging time.

Consideration 1, that C_{tot} and C_{ins} do not vary appreciably with aging time, implies that the perturbed space charge

which gives rise to threshold voltage shifts with aging must be located near the SiON/ZnS interfaces. The maximum distance from the interface that the centroid of trapped charge is located is denoted as Δd and is given by:

$$\Delta d = \frac{\epsilon A \Delta C}{C^2} \qquad (4\text{-}5)$$

where ϵ is the dielectric constant for the insulator or phosphor, whichever is appropriate, ΔC is the capacitance measurement uncertainty and C^2 is the insulator or phosphor capacitance, whichever is appropriate. Using $\Delta C_{tot} = \pm 0.05 nF$ *and* $\Delta C_{ins} = \pm 0.1 nF$ in Eqn. (4-5) leads to $\Delta d_{ZnS} = 680$ Å and $\Delta d_{ins} = 200$ Å. In other words, the experimental fact that C_{tot} and C_{ins} are constant to within the specified measurement uncertainties implies that the space charge giving rise to aging instabilities is located within 200 Å of the interface in the insulator or within 680 Å of the interface in the ZnS. Indeed, these distances are actually firm upper limits and it is very likely that the trapped charge resides much closer than this to the interface.

Consideration 2, that the C-V transition region shifts rigidly with aging time, implies that the interface state density prior to field-clamping, N_{ss}, does not change significantly with aging. This rigid C-V shift with aging implies, in accord with metal-insulator-semiconductor (MIS)

C-V studies[29], that the observed threshold voltage shift is consistent with an increase in the fixed charge density but not with an increase in the interface state density. Note that fixed and interface state charge are both located at the interface; fixed charge is distinguished by the fact that it is immobile with respect to the applied bias whereas interface states may be charged or discharged by an applied bias and the charge localized at interface states contributes to the conduction current. Fixed charge gives rise to rigid shifts in the C-V curve whereas interface state charge leads to non-rigid C-V shifts; thus, a difference in the slope of the C-V curve is a good indicator that the interface state charge has been perturbed.

Consideration 3, that the threshold voltage increases with aging time, can be attributed to either an increase in the internal, phosphor threshold voltage or to a reduction in the polarization charge, and hence the polarization field. To assess which of these changes is responsible for the observed increase in the threshold voltage, plots of (a) the threshold voltage, V_{th1}, (b) the polarization and conduction charges, Q_{pol} and Q_{cond}, and (c) the internal phosphor electric field at threshold, ξ_p^{th}, as a function of aging time are shown in Fig. 4-21. ξ_p^{th} is determined from the threshold voltage, V_{th1}, and Q_{pol} as follows:

$$\xi_p^{th} = \frac{1}{d_p} \frac{C_{ins}}{(C_{ins} + C_p)} V_{th1} + \frac{Q_{pol}}{d_p C_{ins}} \qquad (4\text{-}6)$$

It is evident from Fig. 4-21 (a) that the experimentally observed increase in the threshold voltage with aging time arises from a decrease in Q_{pol} with aging time. Note that Q_{cond} and Q_{pol} both decrease with aging time in the same manner. Also note from Fig. 4-21 (c) that ξ_p^{th} is constant with respect to aging time.

From the above considerations, the following picture of the aging electrostatics begins to emerge. Some of the conduction charge originally available for transport is trapped as a function of aging time at or very close to the interfaces, giving rise to less conduction and polarization charge. Since there is less polarization charge available, the threshold voltage increases. The electron charge is trapped at deep interface traps which are not dischargeable by the applied voltage; these electron-filled deep traps contribute to fixed charge in contradistinction to interface state charge.

The details of the aging electrostatics can be better appreciated by referring to Fig. 4-22 which illustrates an idealized electron transport and trapping sequence for a device with symmetrical interfaces, which is consistent with the experimentally observed aging trends. Sequence (a) shows the equilibrium situation prior to the application of

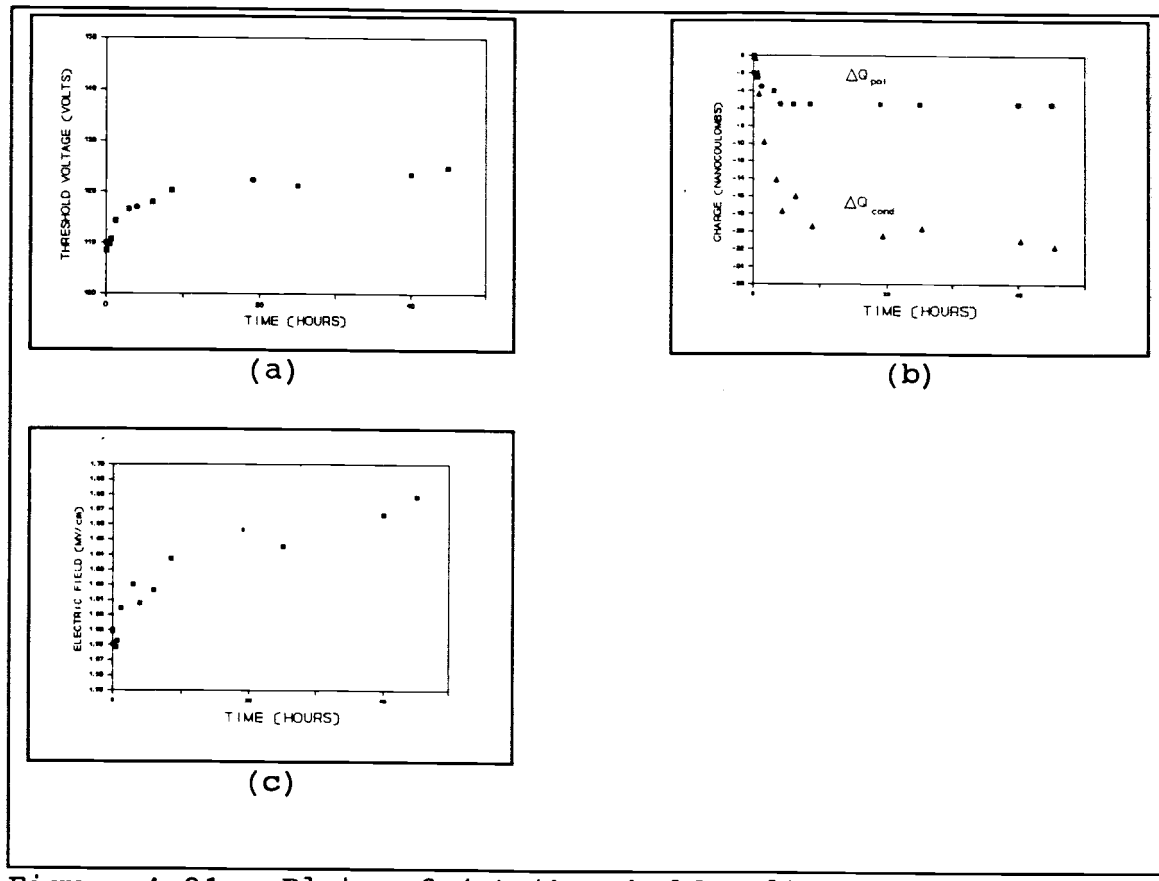

Figure 4-21. Plots of (a) threshold voltage, V_{th1}, (b) charges ,Q_{pol} and Q_{cond}, and (c) phosphor electric field as a function of aging time for glass 7-26-90-15 dot 3 at -10 °C.

a bias in which charge neutrality exists at both interfaces. Sequences (b) and (c) indicate how the interface state occupancy changes with respect to the application of positive and negative pulses if no deep trapping is presumed to occur. Between each sequence the conduction charge, Q_{cond}, is shown and the polarization charge, Q_{pol}, and its associated polarization field lines are also indicated in each sequence. Sequence (c') illustrates electron trapping into a deep level giving rise to fixed charge; note that the

consequence of this trapping is a reduction of Q_{cond}, as shown between (c') and (d), and a reduction in the polarization charge of the subsequent opposite polarity pulse, as indicated in sequence (d). Electron trapping at the other interface is illustrated in sequence (d'). As can be seen by comparing sequences (b) and (c) to (e) and (f), the net effect of trapping electrons in deep levels is to decrease Q_{cond} by an amount equal to the amount of charge trapped and to decrease Q_{pol} by amount equal to one-half of the charge trapped. As indicated in Fig. 4-21 (b), this is consistent with the experimental data. Finally, note that the depth of trap emptying is constant as illustrated in Fig. 4-22; this is a consequence of having a constant ξ_p^{th} since the internal phosphor field controls the depth of detrapping.

4.6 PHYSICAL MECHANISMS OF AGING

As found in the previous section, ACTFEL aging appears to be due to electron trapping at deep levels located at or very near the interfaces. These deep levels are not dischargeable by the electric field so they contribute to the fixed charge in contradistinction to interface state charge. What is the physical nature of these deep, fixed charge traps and how do they arise?

With respect to the second part of the above question, how do the deep, fixed charge traps responsible for ACTFEL

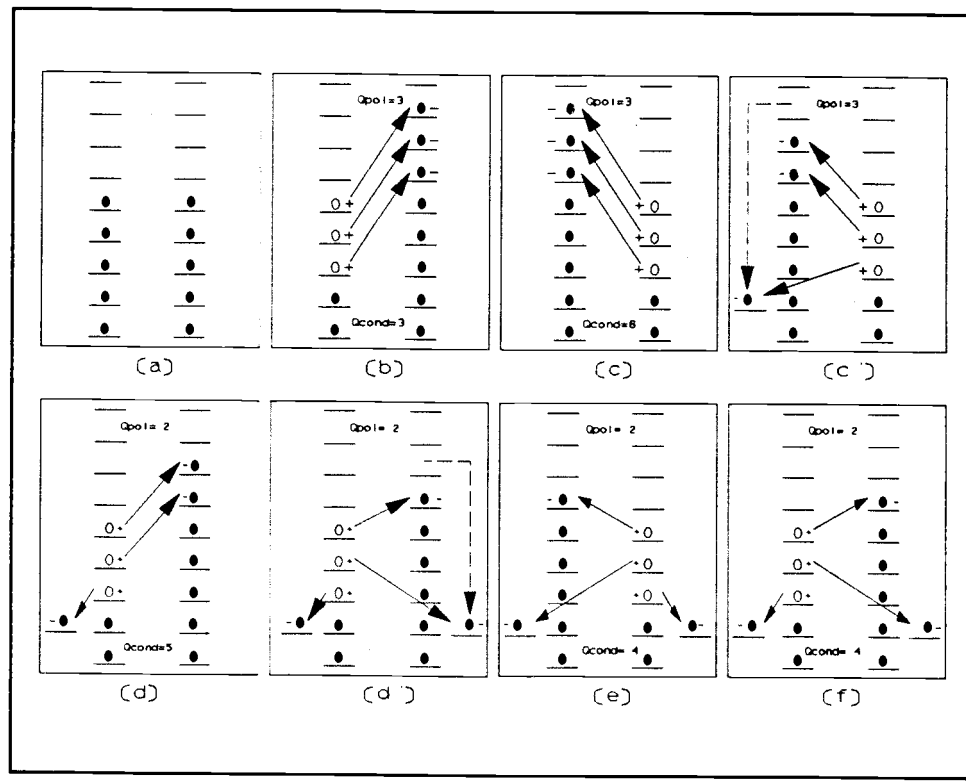

Figure 4-22. Idealized electron transport and trapping sequence for an ACTFEL device with symmetric interfaces. (a) equilibrium; charge neutrality exists, (b) negative bias; no trapping, (c) positive bias; no trapping, (c') maintain positive bias; trap 1 electron, (d) negative bias; no trapping, (d') maintain negative bias; trap 1 electron, (e) positive bias; no further trapping, (f) negative bias; no further trapping.

aging arise, there seem to be two possible answers. First, these deep traps may exist in the initially fabricated ACTFEL device but the capture probability may be very small and, thus, a long aging time may be required before these traps are filled with electrons. The capture probability is particularly small if the electrons to be captured have to surmount an energy barrier, E_B, or tunnel a distance, **x**, into the interface to be captured. In such a case the

capture cross section, σ , is exponentially reduced in comparison to the normal capture cross section, σ_o , as follows:

$$\sigma = \sigma_o \exp\left(\frac{-E_B}{k_b T}\right) \exp\left(\frac{x}{x_t}\right) \qquad (4\text{-}7)$$

where x_t is a characteristic tunneling distance. This type of aging instability, which is subsequently denoted as charge injection and trapping, arises in a wide variety of MIS systems including amorphous silicon[30], InP[31], and CdSe[32]. Charge injection and trapping instabilities are characterized by logarithmic aging kinetics and a very weak temperature dependence[30,33,34]; the aging activation energy has been reported[31] to be 0.04-0.05 eV for InP MIS capacitors and 0.12 eV for CdSe thin-film transistors[32].

Although the logarithmic aging kinetics associated with charge injection and trapping are consistent with the experimental aging data, the activation energy is a bit too large to be consistent with this mechanism. Additionally, recent experiments in this laboratory[36] provide additional evidence that ACTFEL aging does not occur by charge injection and trapping. In these experiments, attempts were made to reset the threshold voltage after aging by photo-depopulation of deep traps. Since the threshold voltage could not be reset optically, it is concluded that the aging is irreversible, which is inconsistent with charge injection

and trapping in which the threshold voltage can be reversibly reset[31].

The second possible way in which the deep traps responsible for aging instabilities arise is that they are generated by atomic rearrangement at the interface. This is the mechanism preferred in this thesis. The aging is envisaged to occur as follows. Energetic hot electrons impinge against the insulator conduction band discontinuity and must dissipate a significant amount of energy, denoted E_{diss}, to thermalize to the bottom of the phosphor conduction band and are subsequently trapped at interface states. If the aging mechanism involves atomic migration, it is most likely that the hot electron thermalization energy, E_{diss}, is of primary importance in facilitating bond breakage and atomic rearrangement in the impact zone located near the interface. The activated atomic species can then migrate away from the impact zone into either the SiON or the ZnS under the influence of electric field and temperature. This is shown in Fig. 4-22.

If atomic migration is responsible for ACTFEL aging the experimentally deduced aging activation energy of 0.2 eV must be identified as the migration energy, ΔH_m, for atomic migration. ΔH_m's for nearest and second-nearest neighbor hopping into a vacancy are estimated using Van Vechten's ballistic model for atomic migration[36]

$$\Delta H_m = \frac{1}{2} m (F d k_B \theta_d / h)^2 \qquad (4\text{-}8)$$

where **m** is the mass of the atom which hops, **F** is a geometric

constant equal to 0.9, **d** is the atomic separation distance, k_B is Boltzmann's constant, θ_d is the Debye temperature, and **h** is Planck's constant. For the purpose of these estimates, the hopping distances are assumed to be the equilibrium

TABLE 4-3. Estimated migration energy, ΔH_m , for nearest- and second-nearest-neighbor hopping.

Hopping atom	ΔH_m (eV) nearest-neighbor	ΔH_m (eV) second-nearest-neighbor
Zn	0.81	2.16
S	0.40	1.05
Si	0.35	0.53
O	0.20	0.94
N	0.17	0.47

nearest- and second-nearest-neighbor atomic distances in ZnS (i.e. 2.35 Å and 3.38 Å) and the Debye temperature of ZnS (θ_d=350 K)[37] is assumed .The estimated values of ΔH_m are collected in Table 4-3. Note that these estimates are not expected to be precise because of inherent limitations of the ballistic model and of the questionable validity of assuming bulk ZnS properties at the interface. With these limitations in mind, an analysis of Table 4-3 suggests that the experimentally observed activation energy of 0.2 eV is most compatible with interdiffusion by nearest-neighbor

hopping at the interface, whereas second-nearest neighbor hopping would seem to be precluded because of the large predicted ΔH_m 's. It should be noted that vacancy self-diffusion in a compound semiconductor such a ZnS is a conceptually simple process if it occurs by second-nearest-neighbor hopping since it occurs only on a single sublattice. In contrast, nearest-neighbor hopping in ZnS is a much more complicated self-diffusion process in which hopping transforms a simple vacancy into a more complicated vacancy antisite defect. Thus, nearest-neighbor hopping naturally gives rise to the creation of defect complexes which could be responsible for the fixed charge, deep levels responsible for aging instabilities. For example, suppose that sulfur vacancies, V_s's, exist at the SiON/ZnS interface, as has been previously suggested by various researchers[38-41]. A possible atomic mechanism for aging instabilities could involve O or N diffusion by nearest-neighbor hopping into a sulfur vacancy which could be described by the following defect reactions,

$$O_O + V_S \xrightarrow[nnh]{} O_S + V_O \qquad (4\text{-}9)$$

$$N_N + V_S \xrightarrow[nnh]{} N_S + V_N \qquad (4\text{-}10)$$

The defect complex specified by the right hand side of the above defect reactions would presumably be the source of the fixed charge, deep levels responsible for ACTFEL aging.

The proposed atomic scenario presumes that the required interdiffusion occurs within atomic distances of the interface. The viability of this assertion can be tested by noting that the amount of trapped charge is approximately equal to $2\left(\frac{C_{ins}+C_p}{C_{ins}}\right)Q_{pol}$ where the factor of 2 arises from the fact that Q_{pol} corresponds to half of the charge trapped and the term in the parenthesis is a correction to charge from externally measured charge to internal charge[35]. The maximum change in Q_{pol} with aging is about 30 nC and $\frac{C_{ins}+C_p}{C_{ins}}$ is about 1.6 so that the total amount of trapped charge is about $8\times10^{12}/cm^2$. If each atomic defect captures only one electron and these defects exist within 100 Å of the interface, this yields a density of atomic defects of order $10^{19}/cm^3$. Thus, a 0.1% concentration of sulfur vacancies initially residing within 100 Å of the interface could give rise to the aging instabilities observed experimentally; this appears to be a viable possibility.

4.7 SUMMARY

The results of an ACTFEL aging study have been presented in this chapter. The activation energy associated with the shift in threshold voltage during the short-term aging period has been found to be 0.2 eV. ACTFEL aging is also characterized by a rigid shift in the C-V transition

region to higher threshold voltages with increasing aging time. Also, the insulator and phosphor capacitances are found to be constant with respect to aging time. The phosphor electric field at threshold is observed to be constant with aging whereas the polarization and conduction charges decrease as a function of aging time, with the magnitude of the change in the conduction charge twice as great as that of the polarization charge.

These experimental observations lead to a model for ACTFEL aging in which hot-electron mediated atomic migration occurs near the SiON/ZnS interfaces, leading to the formation of defect complexes in which transported electrons are trapped in deep, fixed-charge states. The magnitude of the aging activation energy suggest that this atomic migration may occur via nearest-neighbor hopping with insulator atoms (i.e. Si, O, or N) likely hopping into sulfur vacancy sites located in very close proximity (of order 100 Å) of the interface.

CHAPTER 5 - CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

The first thrust of this thesis is the development and refinement of the C-V characterization technique. The C-V technique is subsequently employed in aging studies of ACTFEL devices. The C-V measurement technique, in conjunction with SPICE modelling, is shown to be useful for ACTFEL device physics studies as well as for process monitoring since changes in C-V curve characteristics can be related to specific changes in parameters of the enhanced ACTFEL model whose values are derived from characteristics of the ACTFEL device layers.

Through the use of the C-V technique and SPICE modelling, the following observations can be made:

1) the RC time constant rise in the total capacitance in the subthreshold region near zero bias is due to R_{ito}.

2) a change in the slope of the capacitance transition in the threshold region is due to changes in R_d and R_{ito}.

3) the C-V threshold voltage shifts rigidly for R_i, R_p and BV changes.

4) an apparent step in the insulator capacitance is caused by either R_{ito} or R_d.

5) a rise in insulator capacitance above the expected value is due to R_i.

By using the knowledge gained through the use of SPICE modelling in analyzing aging experiments it is possible to

understand what is occurring internal to the ACTFEL device as a function of aging time. The following characteristics are observed:

1) C_{ins} and C_{tot} are constant with aging time and temperature; this indicates that the charge trapping responsible for aging occurs within a small (<100 Å) distance from the ZnS/SiON interface.

2) the C-V threshold shifts rigidly with aging time; although this could conceivably be attributed to either R_i, R_p, or BV changes, because of previously established SPICE modelling trends, considerations 3) and 4) below appear to exclude any of these as possible explanations. In order to explain this trend from a SPICE modelling point of view, further refinements in the SPICE model are required. Specifically, a circuit element which allows for charge trapping of conduction electrons at the interface is required.

3) Q_{pol} decreases with aging time. This decrease in Q_{pol} is directly related to the decrease in Q_{cond}.

4) Q_{cond} decreases with aging time and this decrease is approximately twice the decrease in Q_{pol}. This is in accordance with a simple model in which conduction electrons are trapped in fixed charge states.

5) The phosphor threshold electric field, E_p, is constant with aging time.

6) There are at least two mechanisms that cause aging; one causes the threshold voltage to increase with aging time and is referred to as short-term aging whereas the other causes a slow decrease in the threshold voltage with aging time and is denoted long-term aging.

7) The ACTFEL device threshold voltage is temperature dependent. The threshold voltage increases with increasing temperature. This trend is evident in both aged (essentially fixed threshold voltage) samples and in unaged samples. This trend shows that trapped charge is both time and temperature dependent.

8) The aging mechanism that causes the shift in threshold voltage appears to be trapping of electrons into deep level, fixed charge states which are created by atomic migration at the interface. This trapping causes the shift in threshold voltage. It is suspected that nearest-neighbor-hopping migration into sulfur vacancies causes the formation of trap sites which are subsequently filled by electrons.

For further understanding of ACTFEL device physics it is necessary to explore the following areas:

1) Aging studies of other material systems that can be used to generate the red, green, or blue colors needs to be performed. As an example, aging studies of atomic layer epitaxially grown ACTFEL samples show radically different aging characteristics compared to sputtered/evaporated devices.

2) Long-term aging studies are necessary in order to understand the mechanism responsible for threshold voltage decreases after long aging times.

3) The enhanced SPICE model needs to be improved or changed to more fully account for the C-V characteristics seen in actual ACTFEL devices. Most importantly it is necessary to account for charge trapping and to more closely match the capacitance transition characteristics in the threshold region of the C-V curve. Also, the

enhanced SPICE model does not adequately describe current transient characteristics.

4) Experiments need to be conducted to explain the linear dependence of the threshold voltage with temperature. C-V and Q-V measurements as a function of temperature should help to provide information needed to explain this trend.

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