AN ABSTRACT OF THE THESIS OF

Ramesh Sivakolundu for the degree of Master of Science in Electrical & Computer Engineering presented on June 10,1988

Title : Implementation of Single Board Computer for real time control of Power Electronic Converter Controlled Variable Speed Generation System

Redacted for Privacy

Abstract approved : _____
Dr H.K.Lauw

Conventional generators are operated at fixed speed, and they lack the advantage of Variable Speed Generators (VSG) i.e.a VSG system is capable to maximize the electro-mechanical energy conversion process by varying the shaft speed. This thesis deals with a VSG system which also preserves all the functional features of a Fixed Speed Generation system, such as, voltage control and reactive power control. The main objective of this thesis is to implement the controllers for real time control of the VSG system on a Single Board Computer.

The structure of the VSG system controller as set up in two hierarchical levels is described. The challenge is to implement all sub-controllers into a single board computer

and yet provide flexibility to the system operator to perform tasks such as parameter adjustments, monitoring and issuing important operation instructions.

The hardware utilized and the software developed for the control is presented. A convenient method of supervisory control is also designed and implemented. The effectiveness of the developed software is verified by detailed measurements. Results are included which demonstrate that the objectives are met completely. Suggestions for further improvements to achieve increased adaptability of the controllers are given.

IMPLEMENTATION OF SINGLE BOARD COMPUTER FOR REAL TIME CONTROL OF POWER ELECTRONIC CONVERTER CONTROLLED VARIABLE SPEED GENERATION SYSTEM

by

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A THESIS

submitted to

Oregon State University

in partial fulfillment of

the requirements for the

degree of

Master of Science

Completed June 10, 1988

Commencement June 1989

APPROVED :

Redacted for Privacy

Associate Professor in charge of major

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Date Thesis is presented JUNE 10, 1988

Typed by Ramesh Sivakolundu

ACKNOWLEDGEMENTS

I wish to place on record my indebtness to my Thesis Advisor Dr. H.K.Lauw for his guidance and inspiration throughout my work. His gracious encouragement and assistance is most sincerely appreciated.

I would like to express my appreciation for the assistance given to me by the Faculty and Staff of the Department of Electrical and Computer Engineering, Oregon State University.

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IMPLEMENTATION OF SINGLE BOARD COMPUTER FOR REAL TIME CONTROL OF POWER ELECTRONIC CONVERTER CONTROLLED VARIABLE SPEED GENERATION SYSTEM

1. INTRODUCTION

A Variable Speed Generation (VSG) system basically is a more effective alternative to the conventional fixed-speed generation system, particularly when dealing with generation of electrical energy from erratic energy resources such as wind, solar and hydro.

The tasks which have been carried out in the course of this thesis are implementation of a microprocessor based control for the VSG system and a terminal interface for supervisory control. The considered VSG system utilizes a doubly-fed generator excited by a power electronic converter on the rotor side. The basic reason that VSG systems were not widely used so far was the crucial problem of supplying the rotor of the doubly-fed machine with currents of varying frequency as determined by the supervisory control logic.

Besides the general requirement to maintain a constant utility grid voltage, the controllability of the stator

terminal voltage made the generation of reactive power with the VSG system feasible.

In chapter 2 of this thesis the VSG system is described and its advantages over the Fixed speed generation system are presented.

Chapter 3 presents the Controller for the VSG system. The hierarchical structure of the feedback control loop, i.e. the local controller and supervisory controller is explained.

In chapter 4 the actual implementation of the control is presented. More details of the hardware involved along with their constraints and development of the software with their limitations are given.

Finally, in chapter 5 the developed software for the implementation of the controller for VSG system is verified and its effectiveness will be demonstrated. It will be shown that the controller is effective over the entire range of operation.

2. DESCRIPTION OF THE VSG SYSTEM

2.1. INTRODUCTION

The Variable Speed Generation (VSG) System basically consists of a doubly-fed generator, a turbine supplying mechanical input power to the generator, a power electronic converter supplying the required excitation waveforms to the generator which is controlled by the local controllers and a supervisory controller of the VSG system.

The main difference between the widely used Fixed Speed Generation System and a VSG system is that the VSG system can operate at maximum efficiency irrespective of varying resource conditions. This efficiency is highly dependent on the mechanical speed of the turbine and maximum efficiency operation is established by adequately controlling this speed through the control of the output frequency of the power electronic converter. Moreover, the considered VSG system is capable of exhibiting all other functional characteristics of a Fixed Speed System. This includes voltage control and reactive power control. A detailed description of the VSG system is presented in this chapter. Aspects of interaction with the adjacent systems is also discussed.

2.2. SYSTEM CONFIGURATION:

FIG 2.1 shows the VSG system, its major subsystem and its connections to the adjacent systems. The VSG system consists of five major components:

(i) The doubly-fed generator which converts mechanical energy into electrical energy.

(ii) The turbine which converts the energy supplied by the primary energy source into mechanical energy.

(iii) The power electronic converter supplying the rotor coils of the doubly-fed machine with the required waveform of either currents or voltages.

(iv) Various sensors providing local controllers and the supervisory controller with necessary information about the operating condition of the VSG system.

The VSG system interacts with the following adjacent systems:

(i) The primary energy source, depending on the application of the VSG system (either water or wind)

(ii) The electric power grid which is connected to the stator terminals of the doubly-fed machine.

(iii) The local controllers which supplies the power electronic converter of the VSG system with the reference value of the rotor currents. It consists of three subcontrollers:

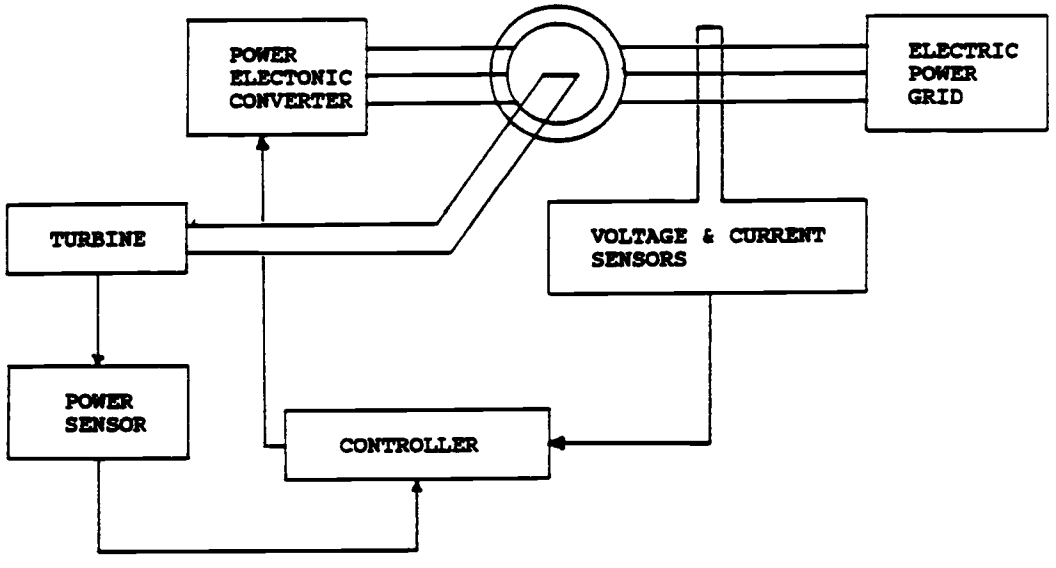

Figure 2.1 : Variable Speed Generation System Configutration

(a) The voltage controller, which ensures that the terminal voltage of the VSG system is maintained at the desired set point.

(b) The efficiency maximizer, whose objective is to operate the system at some optimal speed dependent on the turbine characteristics and the resource condition.

(c) The reactive power controller, which ensures the reactive power demand of the power dispatcher at a remote control center.

2.3. POWER ELECTRONIC CONVERTER

The power electronic converter has the task of providing the rotor-current of the doubly-fed machine with the proper waveform (amplitude and frequency). The power electronic converter synthesizes the rotor currents using some kind of switching process. Semiconductor switches (thyristors or transistors) contaminate the output currents with harmonics of the desired frequency. Consequently, all power electronic converters are provided with an output filter. In the work involved with this thesis, use was made of the series-resonant converter. This converter is one of the major classes of power electronic converters which does not require bulky and expensive low-order harmonic filters. The series-resonant converter contains a resonant circuit which forms a high frequency link between the input and the output switching matrices of the converter.

3. CONTROLLER FOR THE VSG SYSTEM

3.1. INTRODUCTION:

This chapter covers the structure of the various controllers for the VSG system. The controllers for the VSG system are conceived to be hierarchically structured according to two levels :

(i) Local control, which include the voltage controller and efficiency maximizer.

(ii) Supervisory control, which include the reactive power controller, and important decision actions such as start-up, shut-down, on/off logic of reactive power control, on/off logic of efficiency maximizer.

Both the supervisory controller and local controller provide output signals to the waveform synthesizer in the power electronic converter. The supervisory control actions can be instructed and executed in series with the local control actions. The individual controllers are discussed in detail in the following subsections. FIG 3.1 shows the controllers for the VSG system.

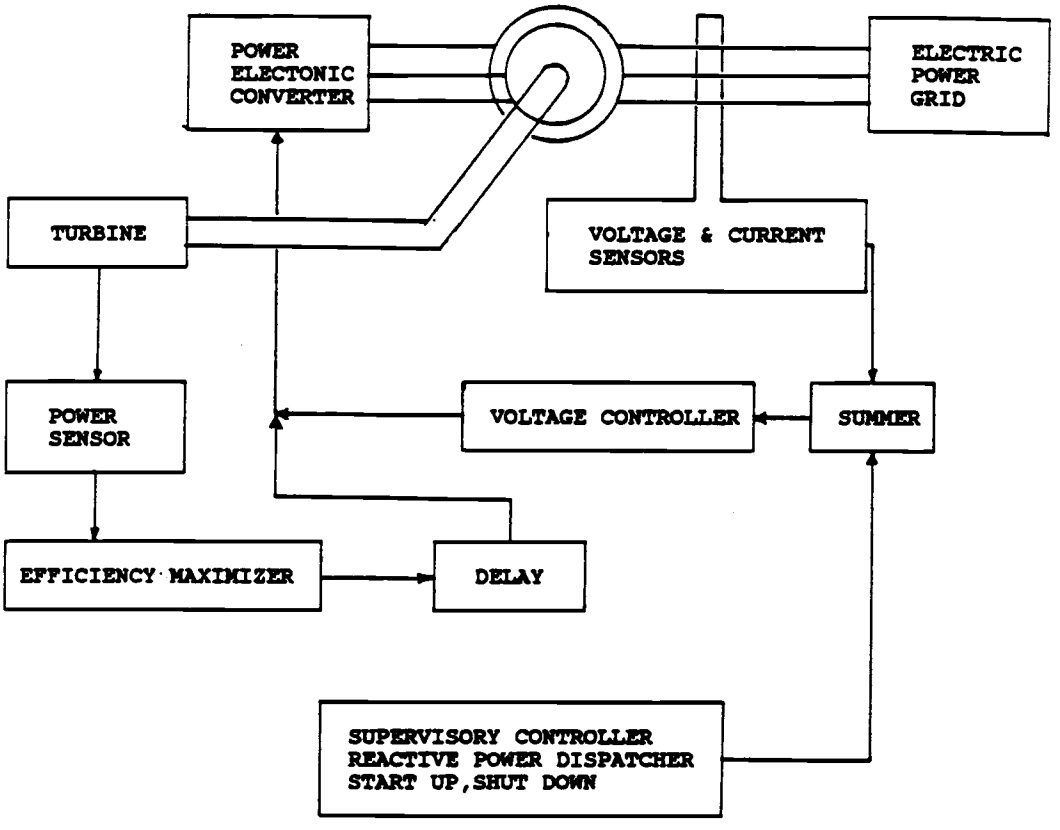

Figure 3.1 : VSG System Controller Configutration

3.2. LOCAL CONTROLLER:

The local controller provides output signals that contain information required by the waveform synthesizer to create the reference signal for the power electronic converter. The information regarding the amplitude of the waveform is obtained from the voltage and/or reactive power controller. The frequency is obtained from other control elements. The local controller components are very critical for proper operation of the VSG system. The important factor is the fact that all elements of the local controller are active in parallel and this requires matching the response speed of the different controllers. The voltage controller, reactive power controller, efficiency maximizer are consecutively treated in more detail in the next three subsections.

3.2.1. Voltage Controller:

The main objective of the voltage controller is obviously to control the rms value of the terminal voltage of the VSG system. The desired voltage level could be determined by the supervisory controller on the basis of reactive power dispatch strategy. On the other hand the system dispatcher can also decide to maintain a certain voltage level to support the voltage of the connecting busbar with changing load demands. The voltage controller is independent of the target setting strategy. The output

controls the amplitude of the rotor current waveform which in turn controls the terminal voltage.

The voltage controller is also required as a stabilizing element to the VSG system if the VSG system is not directly connected to a strong grid. FIG 3.2 shows the block diagram of the voltage regulator. The parameters of this structure can be optimized to meet the performance specifications with respect to response speed, overshoot and settling time.

The voltage controller is structured to be effective for a wide speed range since the VSG system is perceived to be operated at different speeds. The VSG system is non-linear and therefore the linear controller needs to be made adaptive to different operating conditions. However since digital control is employed attempts will be made to exploit the flexibility of adapting the integration gain based on the reference frequency. A detailed discussion and observations will be presented in later chapters.

3.2.2. Efficiency Maximizer:

This controller is important for maximum efficiency in operation of the VSG system under varying resource conditions. However this controller is not that critical to the system, in other words the VSG system need not be shut down when the Efficiency Maximizer fails to function.

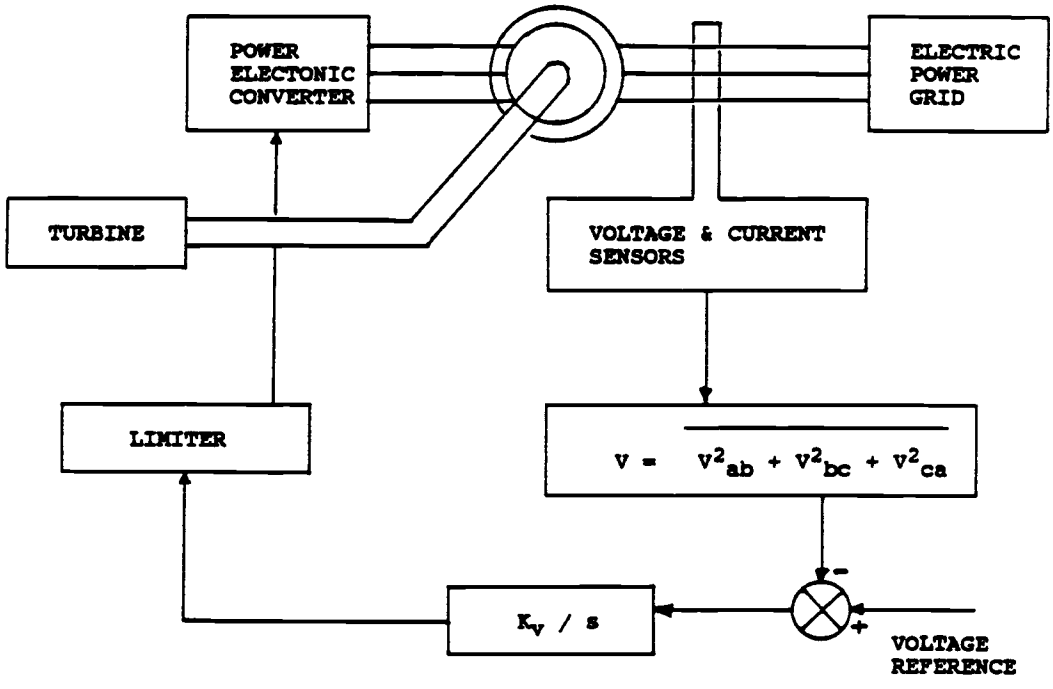

Figure 3.2 : VSG System Voltage Controller Configutration

The efficiency-maximizer is shown in FIG 3.3. It basically comprises of three elements:

(a) Data storage element.

(b) Signal processing unit.

(c) Delay element.

The following provide a detailed discussion of these individual elements.

(a). The data storage element:

The data of the turbine which characterizes the conditions of maximum efficiency operation is stored as a lookup table. The value of the ratio between certain parameters at which the turbine would run at maximum efficiency for any gate position comprises the data of the turbine. The input is the gate position and the output is the ratio which provides the correlation between shaft-speed and the resource conditions at maximum efficiency operation of the turbine.

(b). The signal processing unit:

This unit is supplied with the output of the data storage unit which results in the target shaft-speed. A simple conversion formula can be used to translate target shaft-speed to target frequency of the doubly-fed generator.

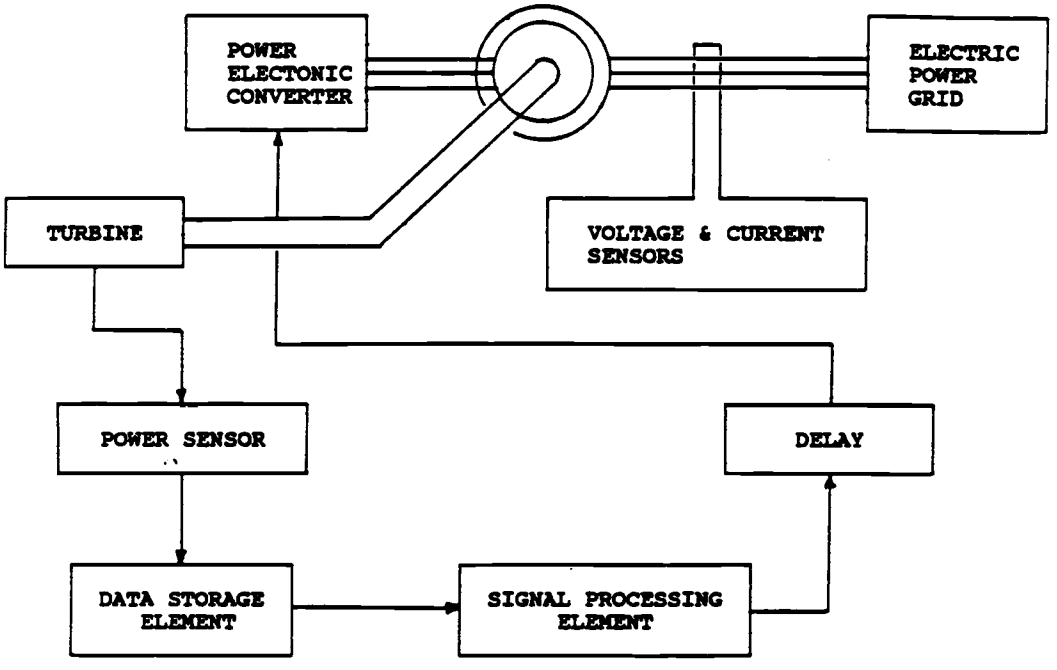

Figure 3.3 : VSG System Efficiency Maximizer Configutration

(c).Delay Unit:

The target rotor-current frequency which is established by the signal processing unit is delayed before it is used as the driving force for signaling the power electronic converter to modify its output waveform frequency. This delay element prevents wear and tear of the system components by unwanted tracking of surge phenomena such as wind gust in wind turbines.

3.3. REACTIVE POWER CONTROLLER :

The reactive power output or the power factor of the VSG system can be controlled to any value. The reactive power can be controlled by simply controlling the amplitude of the rotor current waveform. The voltage controller basically controls this amplitude, thus, the reactive power can be controlled through the voltage controller.

FIG 3.4 shows the block diagram of the controller which is capable of maintaining the reactive power output at any desired setpoint. This setpoint may be set by the dispatcher from a remote control center. The reactive power controller can be considered as a part of the supervisory controller. The reactive power may also be manually controlled by changing the reference voltage of the voltage controller. The gain in the feedback loop of the controller is dependent on the rating of the VSG system. The response speed of the reactive power controller is to be an order of magnitude lower than the response speed of the voltage controller in order to avoid undesirable interactions between the two controllers. Moreover, achieving the highest response speed possible for the voltage controller is necessary in order to assure stable operation of the VSG system if connected to a weak power grid. Response speed of the reactive power controller is not critical.

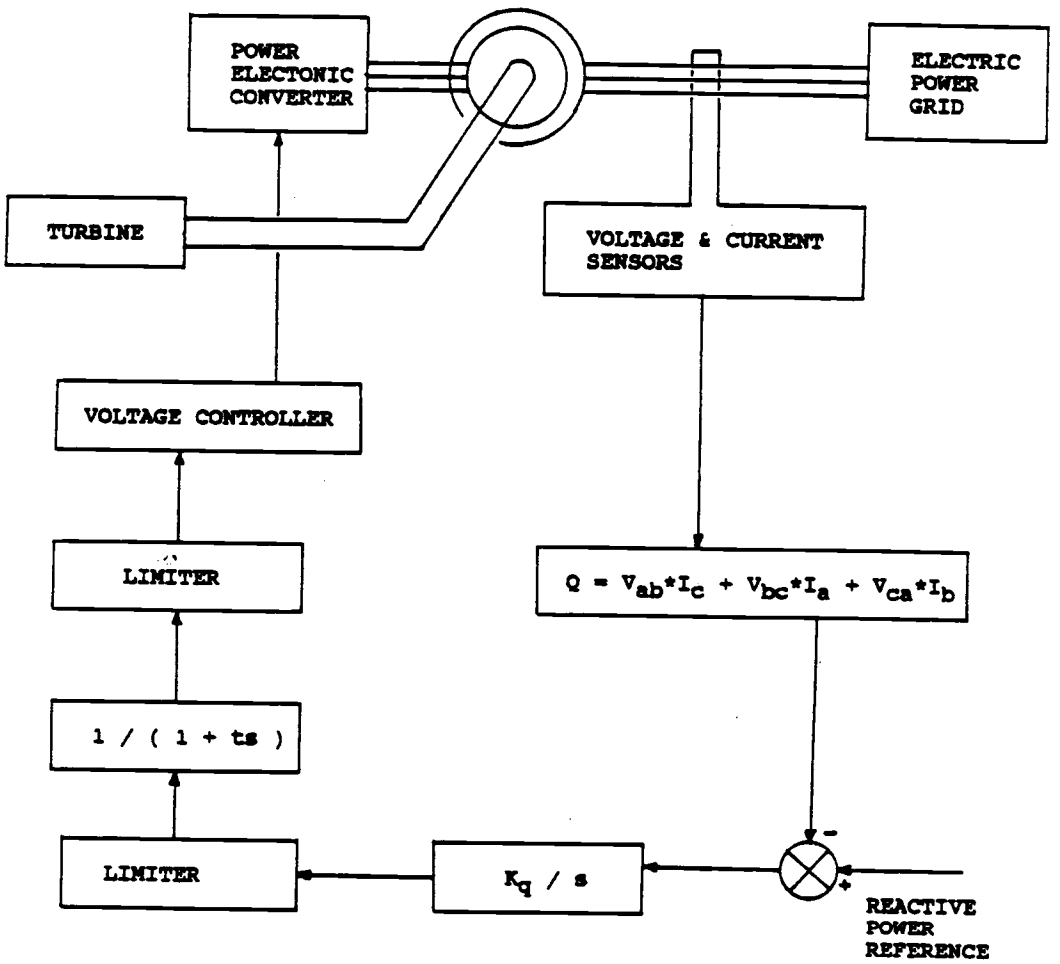

Figure 3.4 : VSG System Reactive Power Controller Configutration

4.IMPLEMENTATION OF THE CONTROL

4.1 INTRODUCTION :

In the previous chapters the VSG system and its control was described briefly. This chapter covers the main work of the thesis, i.e. actual implementation of the controller for the VSG system. The hardware involved in the implementation is described in detail with the limitations and problems faced during the development. The software on the single board computer and the supervisory control device (IBM PC-AT) is discussed in detail. The processing time considerations are presented and significance as well as limitations of the software are highlighted. The possible improvements are also mentioned which could lead to an efficient implementation of the controller for VSG system.

4.2. HARDWARE ELEMENTS :

The control of the VSG system was implemented using a combination of hardware and software elements. The hardware elements were basically the following:

(a) Single Board Computer, which basically is the brain of the whole control.

(b) Data Acquisition and Display, whose main objective was to provide the single board computer with the various signals which are needed by the local and supervisory controllers. The display was to facilitate the supervisor to dynamically vary the integration parameters and observe the variables in the control loop.

(c)Signal Conditioning Unit, which basically acted as a filter/buffer to isolate the various sensor/transducers from the microprocessor control unit.

These hardware elements will be discussed in detail in the following subsections. Limitations of the hardware will also be discussed.

4.2.1. Single Board Computer:

The Single Board Computer is a 16-bit computer system for high-speed, real-time, microprocessor based

applications. It has a 1M-byte on board, dual-port memory module and has the advanced capabilities of the iAPX 286 CPU device. The following is a detailed view of the board's internal operation and describes the board's functional blocks.

Central Processor:

The central processing unit on the single board computer (SBC) is the 80286 CPU device. It can be operated in one of the two operating modes: Real Address mode or Protected Virtual Address Mode (PVAM).

In Real Address mode, the 80286 device can access up to one megabyte of physical memory. In PVAM, the 80286 can access upto 16 megabytes of physical memory and upto 1 gigabytes of virtual memory. PVAM also provides a four level privilege system, memory management and protection features, automatic task switching. The CPU was operated in real mode for this purpose considering the memory requirement for the implementation . The 80286 device contains a prefetch queue (two instructions plus six bytes) that allows the CPU to "look ahead" at the next instructions. The hardware within the 80286 CPU automatically fills the queue during the time that the local bus is idle. This prefetch during idle CPU bus time increases the performance of the board.

The 80286 device uses a "pipelined" timing technique to condense local bus cycles. This feature enhances the

processing speed by allowing higher local bus bandwidth. The 80286 device condenses local bus cycles by allowing the valid address of the next bus cycle to overlap the valid data of the current bus cycle by one system clock cycle, thereby making use of the local data bus and the CPU address bus during the same CPU clock phase.

Interrupt Controllers:

The SBC contains two 8259A Programmable Interrupt Controller (PIC) devices. Each 8259A PIC provides eight independent levels of interrupt priority. One 8259A PIC is configured as a slave PIC to process on-board interrupts; the other 8259A PIC is configured as a master PIC to serve local and high-priority, vectored interrupts, the vectored interrupts from on-board slave devices such as 8274 Multiple Protocol Serial Controller (MPSC) and the slave PIC.

80287 Numeric Processor Extension:

The SBC provides the capability for enhanced numeric processing by using a 80287, Numeric Processor Extension device that supports floating point calculations. The 80286 and 80287 devices execute instructions in parallel until the 80286 device executes WAIT instructions to wait for completion of the 80287 operation.

On-Board Memory:

The on-board memory resources of the SBC consists of two types of memory: 1M byte of dual ported, DRAM and upto 256K-bytes of local (EPROM) memory.

iSBX Bus Interfaces:

The SBC provides low-cost I/O expansion through the iSBX bus interfaces. Each interface can perform either 8-bit or 16-bit operations, depending on user requirements and the capabilities of any MULTIMODULE boards installed.

Serial I/O Interfaces:

The serial I/O on the SBC consists of a programmable 8274 Multiple Protocol Serial Controller (MPSC) device handling the serial interface for the two 26 pin connectors. Depending on how the 8274 is programmed the interfaces can operate in either an interrupt-driven mode or polled mode.

Further detailed information about the Single Board Computer can be obtained from the Hardware Reference Manual (Ref#).

4.2.2 Data Acquisition And Display:

The data on which the local controllers and the supervisory controller act, is acquired from the VSG system by the Analog Input Module and is presented to the SBC. The

Analog Input Multimodule is an expansion board which interfaces with the host SBC through the iSBX bus and plugs into the bus connector. The reference signal to the power electronic converter's waveform synthesizer is converted back to analog form through the Analog Output Module. The Analog Output Multimodule similarly interfaces with the host SBC through the iSBX bus. A detailed discussion about the hardware elements in these expansion boards follows in subsections. The various parameters in the controllers and the data acquired are displayed on the Supervisory controller's terminal (in this case IBM PC-AT) through the 8274 MPSC on the board.

Analog Input Module:

The input module provides the ability to add analog input functions to any host SBC that contains a iSBX bus connector. The input module provides 8 differential or 16 single-ended analog input channels that may be jumper-selected based on the application. For the purpose of this implementation since more than 8 channels were require and therefore 16 single-ended input channels were used. The input module includes a user-configurable gain and voltage range (0 to +5 volts, or -5 to +5 volts). The input module receives all power and control signals through the iSBX bus connector to initiate channel selection, sample and hold operations and analog-to-digital conversions. The ADC has a resolution of 12 bits.

Analog Output Module:

The Analog Output Module is an expansion board to provide quick and easy expansion capabilities for the SBC. It adds the analog output capability to the host SBC that contains an iSBX connector. The module uses an 8041 Universal Peripheral Interface device to control eight analog output channels that may be configured to operate in bipolar voltage output mode, unipolar voltage output mode, or current loop output mode applications. For the purpose of implementation of the control the module was configured to operate in the bipolar voltage output mode. All data to be output through the module is transferred from the host SBC to the module via the iSBX bus connector. The UPI device accepts the binary digital data and generates a 12-bit data word for the Digital-to-Analog converter and a four bit channel decode/enable for selecting the output channels. The board status is available via the iSBX bus connector.

Multiple Protocol Serial Controller:

The SBC communicates through the 8274 MPSC to the other devices. The 8274 was programmed to operate in the polled mode with the Supervisory Controller (IBM PC-AT). A high-level software running on the IBM PC-AT communicated with the SBC in order to display the various parameters involved in the feedback control loops and also the output voltage and currents of the VSG system. Since the communication was

polled mode the Supervisory controller could change the parameters in real-time.

4.2.3. Signal Conditioning Unit:

The main objective of this unit was to isolate the sensors/transducers which transduce the VSG system terminal voltages and currents from the Analog Input Modules. Six channels of the Input module were required (3 for three line voltages and 3 for the line currents). Thus six Op-amps were used to act as buffers and also as filters to remove noise. This was essential since the Input module was sensitive to 2.4 millivolts.

4.2.4. Limitations:

The hardware elements has some limitations as far as their usage was concerned. The Analog Input Module has a multiplexer which selects the channel and in order to input six signals the channels have to be selected sequentially. This results in sampling the various signals at different instants with the conversion time between each channel. The Analog output board refreshes each channel output periodically and thus could be at any particular channel when an update is initiated. This could result in a time delay which becomes critical if the Analog output board is used to generate a repetitive signal.

4.3. SOFTWARE ELEMENTS:

The development of software for the implementation of the VSG system controller, along with the required hardware, is conducted during the course work for this thesis. Most of the software is in assembly language and the display on the terminal is in high level language. The entire software is structured with small procedures for multiplication, division, integration, and filter of the first order, etc. The following subsections describe these in detail. The limitation of the software is also discussed along with possible improvements in the algorithm used.

4.3.1.Description of Sub-Modules:

The software for the implementation of the control makes use of some of these modules as a part of the main program. The following sub-sections describe the modules briefly and bring out the constraints of the Single Board Computer used.

Multiplication and Division Routines:

The multiplication and division is carried out by the 80286 as a single instruction, but there are some constraints involved.

The multiplication instruction performs signed multiplication, with the source operand being multiplied by the contents of a specific internal register and the 32-bit signed result is stored in two specific registers. Care had

to be taken to initialize these registers before the instruction is executed and checked after the multiplication is complete in order to keep track of the entire result.

The division routine whereas performs a signed divide. The dividend is implicit and the divisor is given as an operand. The dividend is in two specific internal registers and care has to be taken if the dividend is a 16-bit number, in the sense that, the register which has the higher bytes be initialized to 0000 (in Hex) or FFFF (in Hex) depending upon the dividend being positive or negative respectively.

Digital Implementation of Integration:

The Integration in digital world is carried out by means of difference equations. Various methods for deriving the difference equations are possible . Trapezoidal rule is known for its inherent stability and ease of implementation. Also the step size, i.e. time between two samples, is not that critical compared to other methods . Thus trapezoidal rule was chosen for this implementation.

Trapezoidal rule for integration of the form

$$Y = (K * X)/s$$

resulted in the following difference equation :

$$Y_o = Y_{-1} + K * (X_o + X_{-1})/(2 * (t_o - t_{-1})) ,$$

where

Y_o : is the current output of the integrator.

Y_{-1} : is the previous output of the integrator.

X_o : is the current input to the integrator.

X_{-1} : is the previous input to the integrator.

t_o : is the current sampling time.

t_{-1} : is the previous sampling time.

This was implemented on the Single Board Computer using assembly language.

Digital Implementation of First Order Filter:

A first order filter, like integration, is implemented using difference equations. Such a filter is of the form

$$Y = (1 / (1 + Ts)) * X .$$

Application of the trapezoidal rule results in the following difference equation :

$$Y_o = Y_{-1} * (Tm - 1)/(Tm + 1) + (X_o + X_{-1})/(Tm + 1) ,$$

where

Y_o : is the current output of the filter.

Y_{-1} : is the previous output of the filter.

X_o : is the current input to the filter.

X_{-1} : is the previous input to the filter.

Tm : is the value (2 * T / (t0 - t-1)).

t_o : is the current sampling time.

t_{-1} : is the previous sampling time.

The time delay between two samples is generally referred to as " delta T " and will be followed in the rest of the text.

The integrator and filter were programmed in assembly language. The initial and final values of input and previous value of the output along with the constants K (the gain of the integrator) and T (time constant of the filter) were passed on as parameters to the procedures. Thus these procedures were made for general purpose use and are called upon as library routines. The final output values were passed on back to the calling procedures.

4.3.2. Main Control Program:

The main control software basically includes the local controllers, i.e. the voltage controller and efficiency maximizer. The main procedures that were a part of this software were integration and first order filtering. The voltage controller, and the efficiency maximizer routines make use of these procedures. They will be discussed in the following subsections.

Voltage Controller :

The voltage controller is the main feedback control loop of the VSG system and is very critical to the effectiveness of other control loops. The algorithm, FIG 4.1, for the implementation of this control is as follows :

(i) Initialize the stack, data segment and other peripheral boards and devices.

(ii) Initialize the variables and parameters.

(iii) Get in the values of line Voltages.

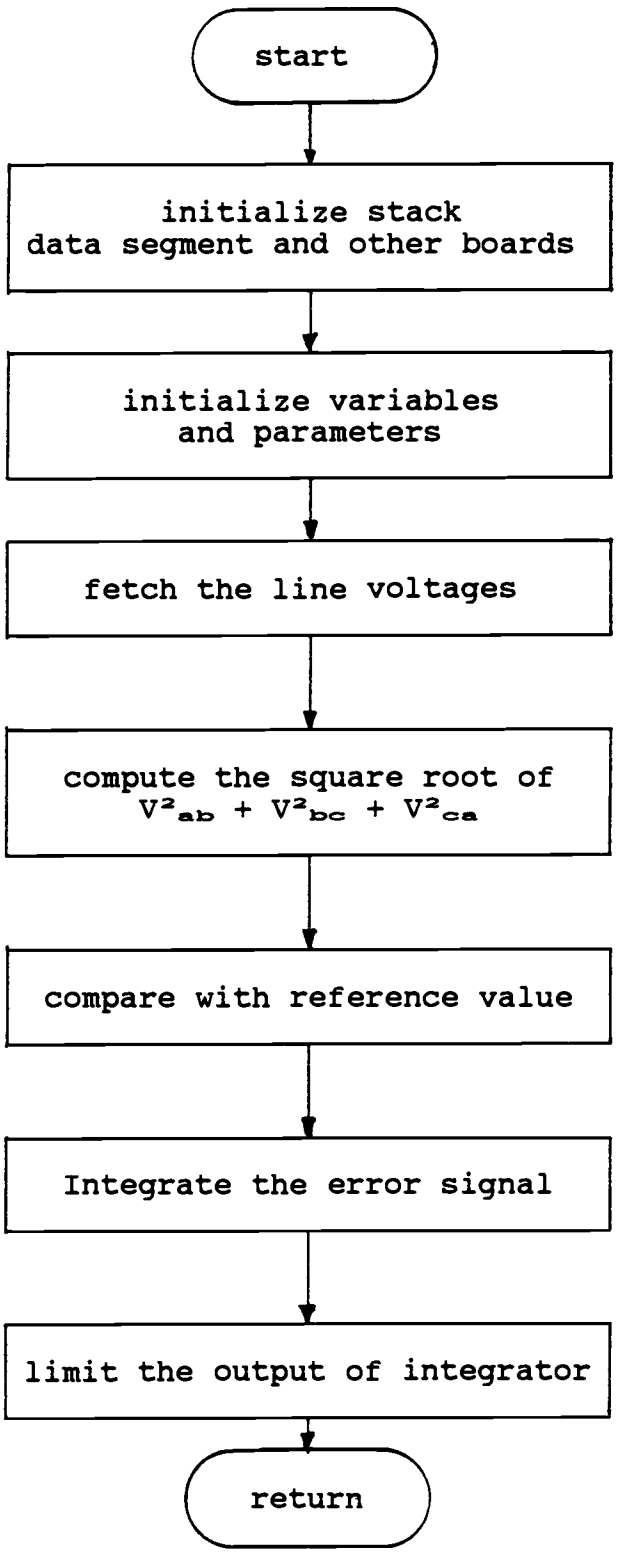

Figure 4.1 : Flow chart for the voltage controller.

(iv) Compute the square root of square of the three line voltages.

(v) Compare with the reference value of the voltage.

(vi) Integrate the error voltage.

(vii) Limit the output to the converter.

The steps (iii) to (vii) are repeated till the supervisory control decides to reset. However before the loop is started the initial and final values and other parameters are initialized. The various steps are described briefly below.

(i) The Stack segment and Data segment is defined in memory and the various variables and parameters used are defined as words of 16 bits each. Also the Analog Input Module and the Analog Output Module is initialized along with the 8274 Multiple Protocol Serial Controller. FIG 4.2 describes the flow of this sub-routine.

(ii) The initial and final values of the various variables are initialized and the integration gains are set to default values. This routine is visited if the VSG system operator wishes to reset the entire control logic without resetting the single board computer. FIG 4.3 describes the flow of this routine.

(iii) The input module converts a bipolar signal (-5 to +5 volts) to a equivalent 12 bit binary number. The 12 bit is scaled by removing the offset and stored as a two's

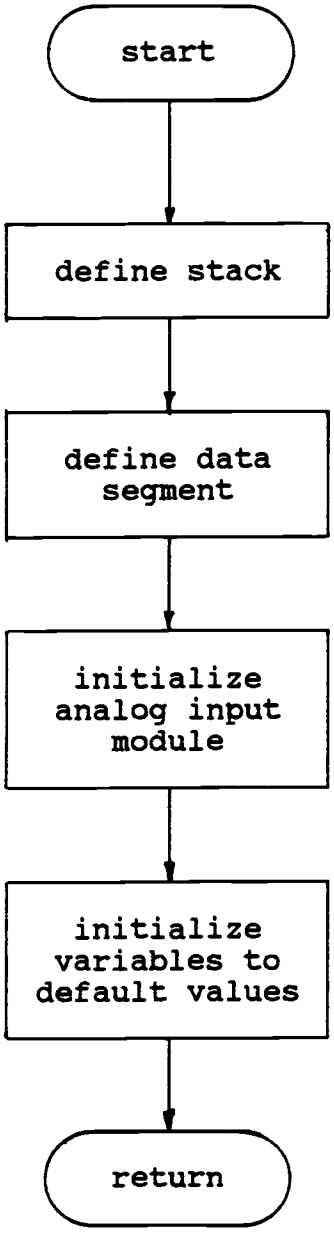

Figure 4.2 : Flow chart for the initialization procedure.

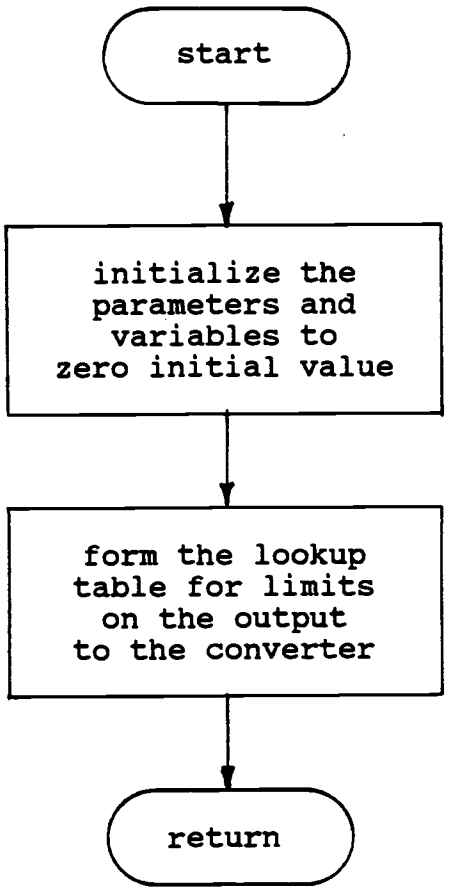

Figure 4.3 : Flow chart for resetting the parameters and variables.

complement number if the converted value is negative. This scaling and negation is done by the software. FIG 4.4 gives the flow of this routine.

(iv) The computation of square root of the sum of squared voltages is carried out in the 80287 Numeric Processor Extension and the special treatment of this operation has led to a reduction of the processing time. FIG 4.5 describes the flow of this routine. The Analog Input Module on the SBC takes about 50 microseconds to convert one analog signal to digital value. During this time the 80287 is executed, in parallel, computing the square of the voltage value which was obtained in the previous analog to digital conversion. The 80287 takes longer time to compute because of the floating point computation process. This correspondingly available time is utilized to fetch in the three voltages as well as the three line currents.

(v) The result of the computation is compared with the desired reference voltage and the error is passed on to the next routine for integration.

(vi) The error voltage is integrated and the output is limited by the next routine. FIG 4.6 gives the flow of this routine. The various initial and final values are passed on in specific variables to a common routine for integration with the gain as one of them. The gain can be changed

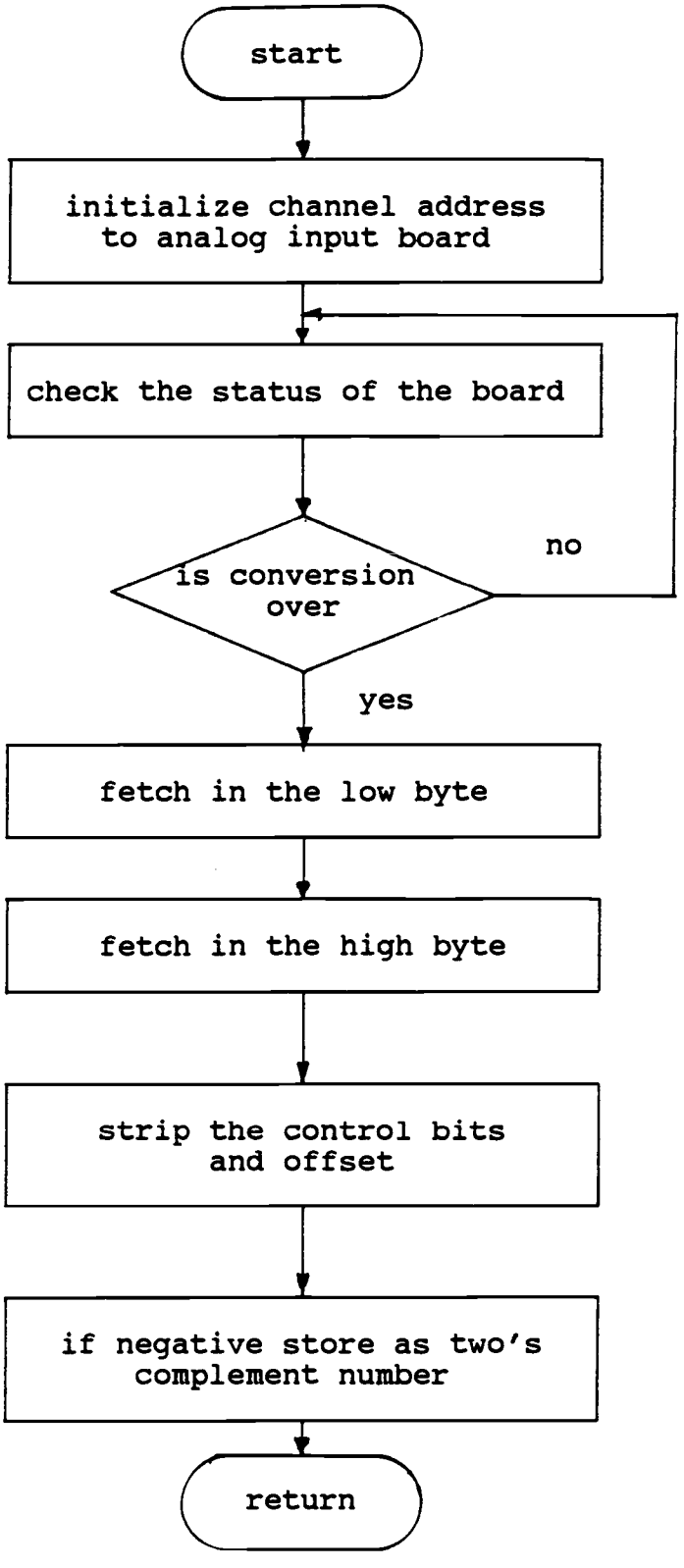

Figure 4.4 : Flow chart for fetching the voltages.

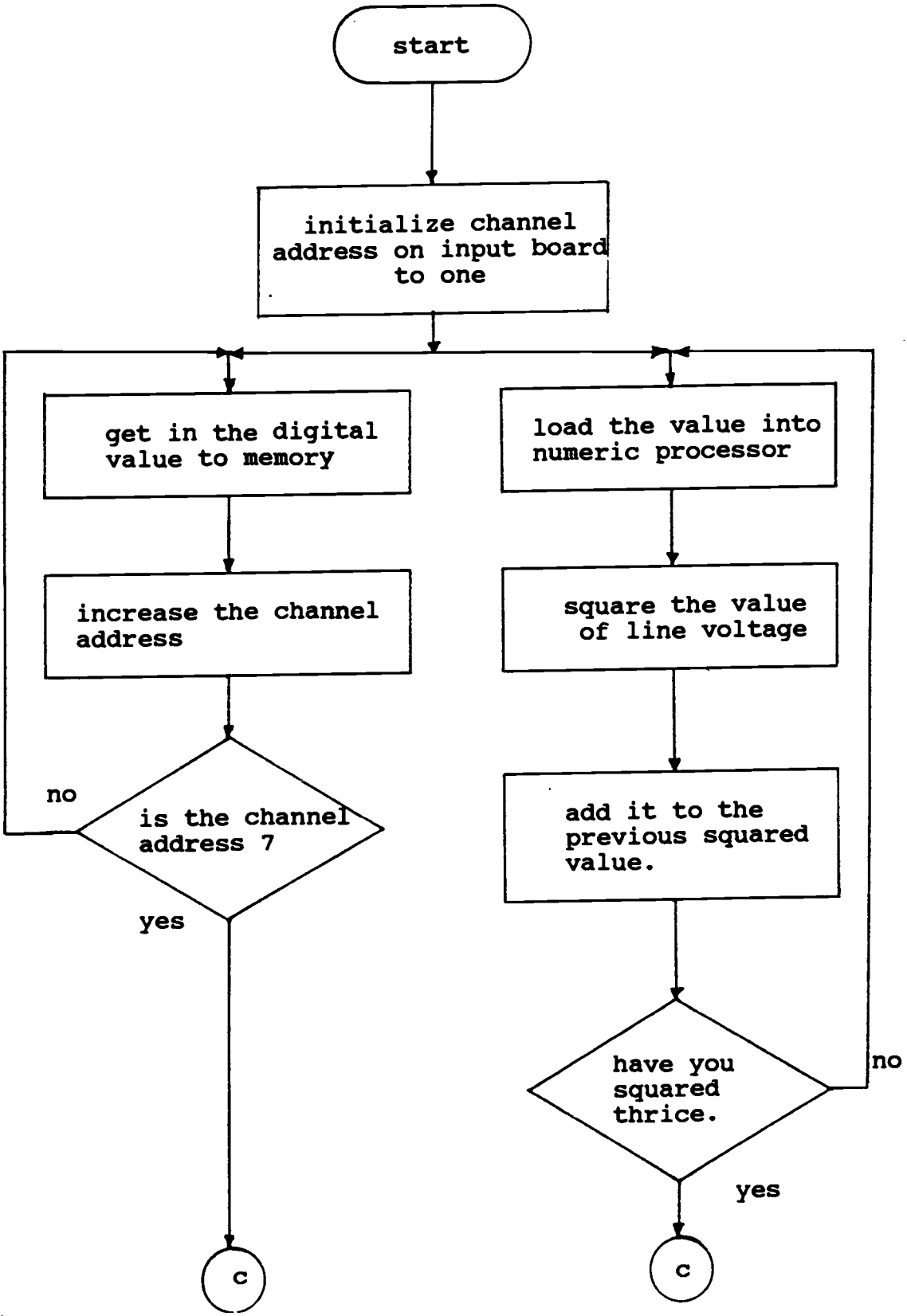

Figure 4.5 : Flow chart for computing square root of sum of squares of voltages.

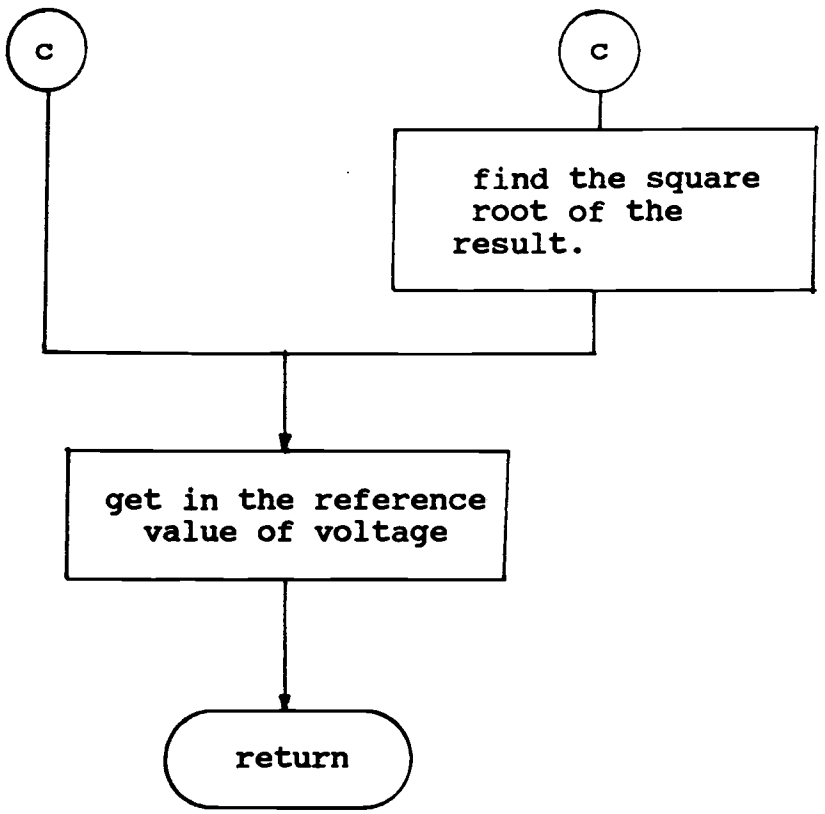

Figure 4.5 : Continued

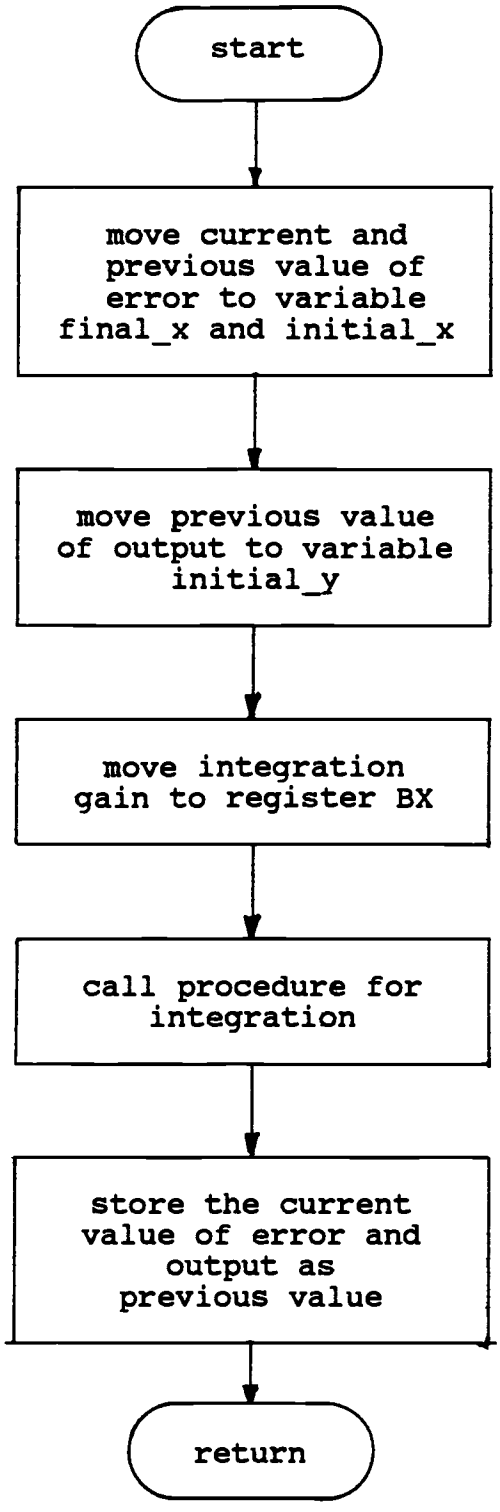

Figure 4.6 : Flow chart for the integration initialization routine.

dynamically by the VSG system operator from the keyboard. The gain is chosen as high as possible (limitation is due to stability) to make the controller sensitive to small variations in the terminal voltage.

(vii) The output of the integrator is limited to prevent the integrator from oscillating and also to prevent damage to the power electronic converter due to excessive reference values. FIG 4.7 describes the flow of this routine. This limit is programmed to be varying with varying frequency reference to the converter and therefore a lookup table had to be installed. Also the lowest value that should be sent out to the power electronic converter is limited to prevent the VSG system from losing synchronism.

Efficiency Maximizer:

This routine basically computes the target speed of the shaft in order to optimize the efficiency of the VSG system. FIG 4.8 describes the algorithm briefly. In order to simulate the efficiency maximizer a D.C. Motor was utilized as a source of mechanical input power to the generator. The power at the output of the D.C. Motor was assumed to be the the gate position and the pressure head was assumed to be constant. Details of the relationship between gate position, pressure head and turbine characteristics [ ] is not discussed. Thus the efficiency maximizer could be realized by changing the excitation to the D.C.Motor which in turn

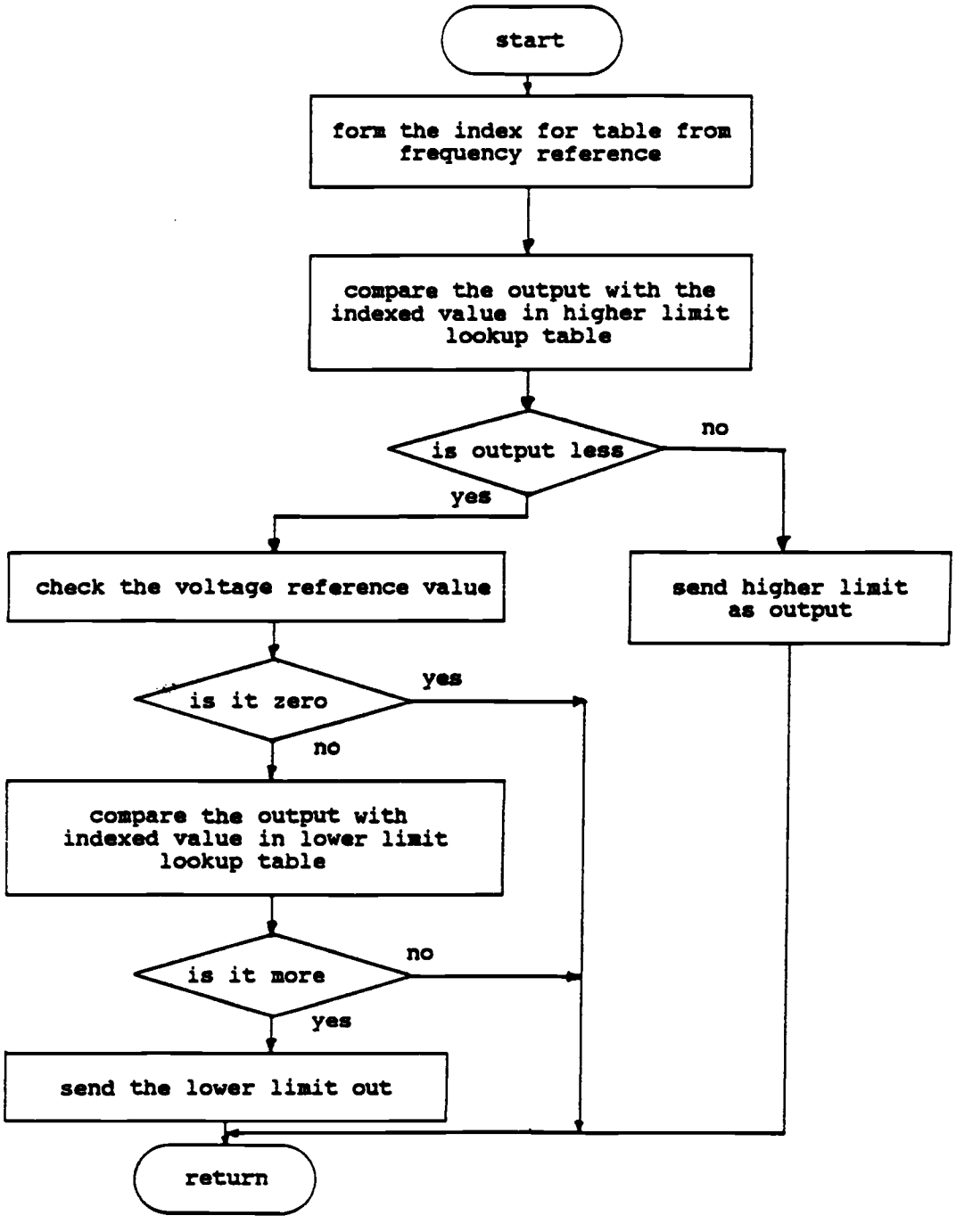

Figure 4.7 : Flow chart for limiting the output to the converter.

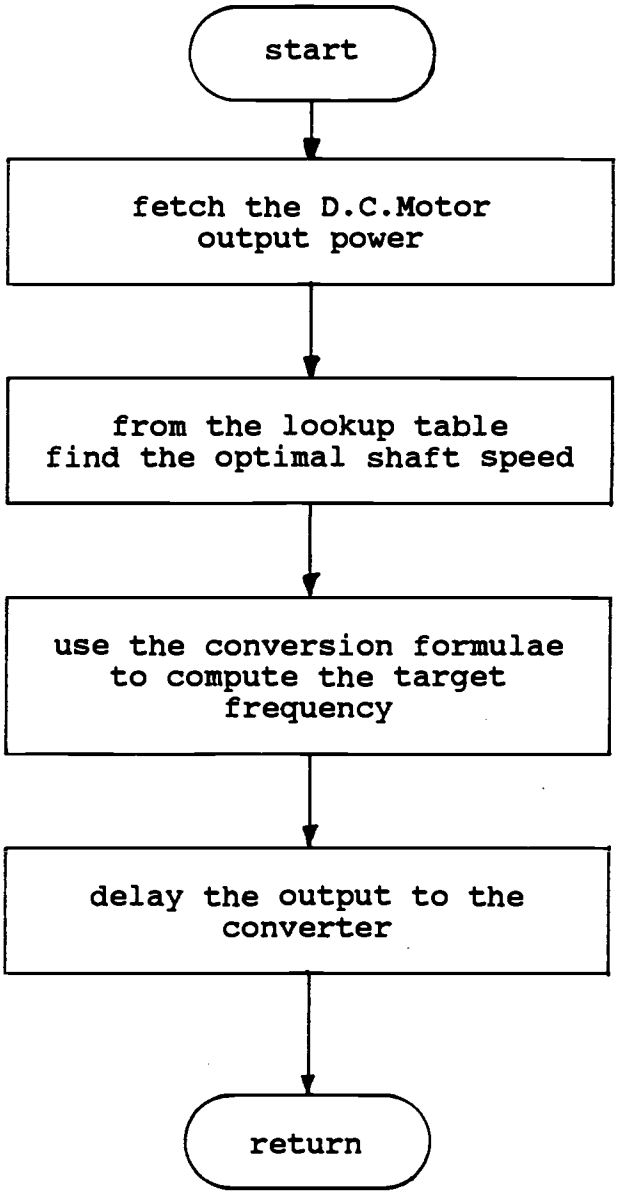

Figure 4.8 : Flow chart for the efficiency maximizer.

would result in a change in the mechanical power input to the generator. This changing power input could be sensed and the corresponding optimal shaft speed could be translated to be the target frequency of the power electronic converter.

The data storage element, which stores the characteristics of turbine for maximum efficiency operation, in the simulation is a lookup table which has the required shaft speed for different power output of the D.C. Motor. The algorithm basically computes the optimal shaft speed for the output power of the D.C. Motor, which is fed in as an input to the efficiency maximizer. This shaft speed is translated to target frequency of the doubly-fed generator using conversion formulae. The change in the shaft speed is realized by controlling the rotor-current frequency. The output of the conversion formulae is delayed before it is used as the driving force for signaling the power electronic converter to modify its output waveform frequency.

4.3.3. Supervisory Control Program :

The supervisory control program includes the reactive power control and the display program. The reactive power controller controls the reactive power output of the VSG system and can be controlled by simply controlling the amplitude of the rotor-current waveform. The control loop contains an integrator and first order filter as well as an equation which computes the reactive power " Q " from the

voltage and current sensor signals. The display program resides in the Supervisory Control Device,which is an IBM PC-AT in this implementation. Its main objective is to provide means of dynamically observing the voltages and currents and other parameters on the terminal including the flexibility of on-line parameter adjustments, such as changing integration gain and filter time constants. More detail is presented in the following sub-sections.

Reactive Power Controller:

The reactive power output or the power factor of the VSG system is controlled by this routine. The reactive power controller can be introduced in the feedback control loop by the VSG system operator after the system has synchronized and stabilized. The output of the reactive power controller becomes the reference value for the voltage controller. The algorithm (FIG 4.9) for the reactive power control is as follows:

(i) Compute the reactive power " Q " from the voltages and currents.

(ii) Compare the reactive power value with the desired reference reactive power value.

(iii) Integrate the error in the reactive power and limit the output.

(iv) Delay the output of the integrator.

(v) Limit the output of the first order filter.

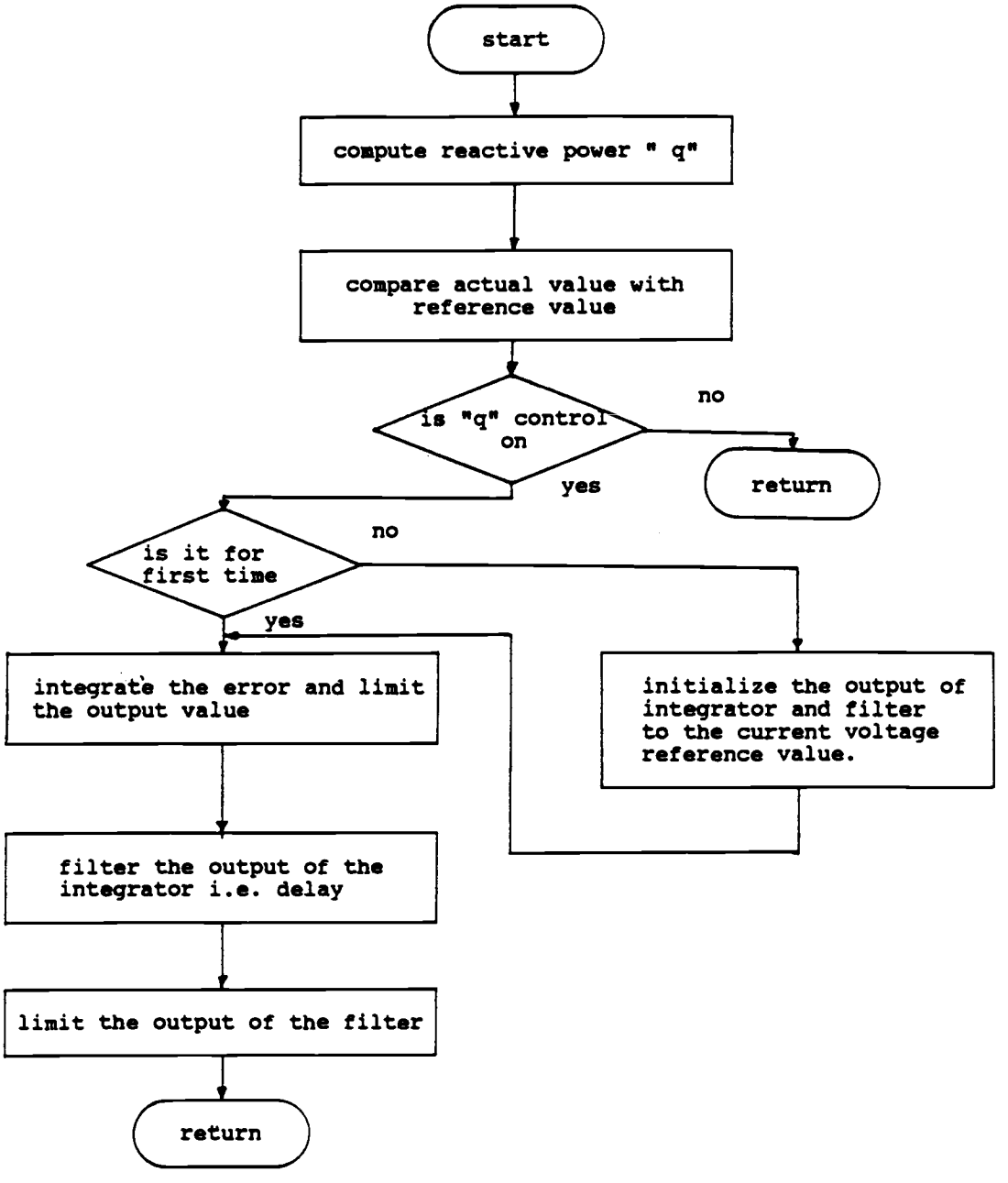

Figure 4.9 : Flow chart for the reactive power controller.

The initial and final values have already been initialized along with the voltage controller parameters. The steps (i) and (ii) are always executed along with the local controllers to provide means of switching over from local control to supervisory control. The reactive power is computed and displayed on the terminal. When the supervisor wants to switch from voltage control to reactive power control he sets the reference reactive power to be close to the actual reactive power to facilitate smooth switching. Then on any reference reactive power could be dispatched and the reactive power controller takes over. After the switch over the steps (iii), (iv) and (v) are executed after the voltage controller and steps (i) and (ii).

(i) The reactive power is computed by

$$Q = V_{ab}I_c + V_{bc}I_a + V_{ca}I_b$$

and the average of the current value and two previous values is taken to reduce the effects of noise. This effect was observed to lead to undesirable oscillations to the terminal voltage as well as shaft speed of the VSG system. FIG 4.10 describes the flow of this routine.

(ii) The average value of reactive power is compared with the reference value of the reactive power and the error is passed on to the integrator.

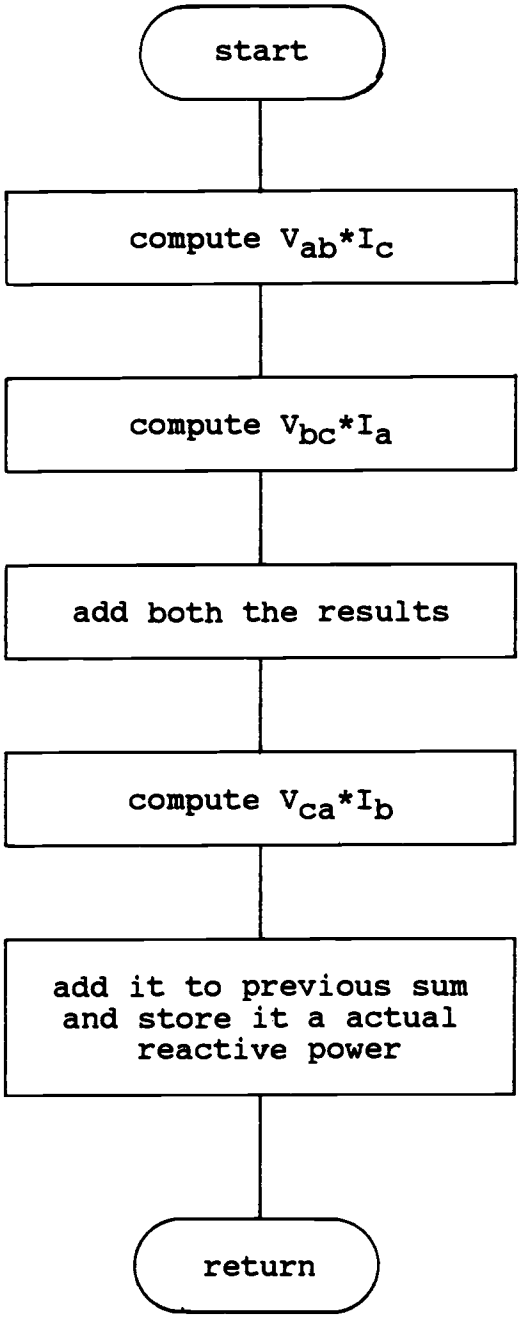

Figure 4.10 : Flow chart for the computation of reactive power.

(iii) The error is integrated and the output is delayed by the next routine. The initial value of the output of the integrator is initialized to be equal to the current reference voltage value to facilitate smooth takeover. The output is limited by a higher limit as well lower limit to prevent the integrator from oscillations. The gain of the integration is under the control of the supervisory software.

(iv) The output of the integrator is delayed since the reactive power controller is the outer feedback loop and needs to be slower than the inner feedback loop for stability of the system. FIG 4.11 shows the flow of this routine. Moreover, in order to make the controller sensitive to small changes in the reactive power the gain of integration is chosen high. Again the initial value of the output of the first order filter is initialized to be equal to the current reference voltage.

Display Program :

The main objective of this program was to facilitate observation of the various VSG system parameters, including a flexible means for on-line adjustments to the integration and filter constants. The program facilitates convenient switching from voltage control to reactive power control. Function keys (F1 - F5) on the keyboard are utilized for the

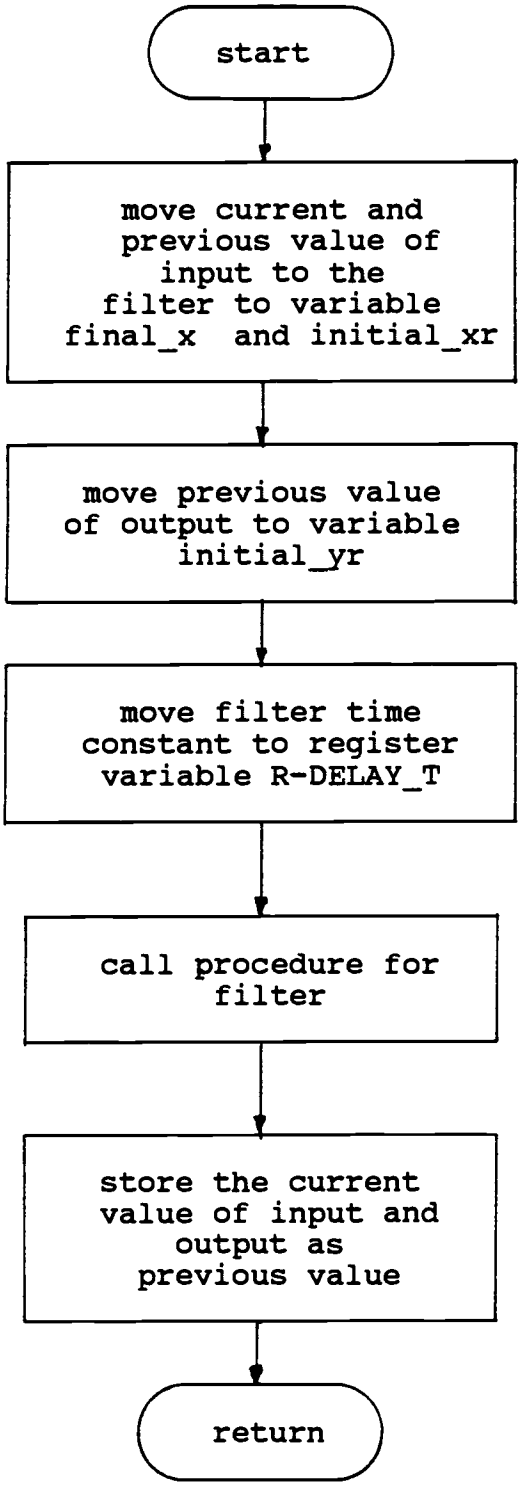

Figure 4.11 : Flow chart for the first order filter initialization routine.

operator's selection of the mode of operation desired, such as reading the variables and parameters, changing the parameters and writing it in the memory of the Single Board Computer. A function key was also provided for continuously reading and updating the variables and parameters on display every three seconds. The program communicated through the RS232 port on the IBM PC-AT and the 8274 Multiple Protocol Serial Controller with the Single Board Computer.

4.3.4. Processing Time :

The processing time optimization was very important for efficient operation of the VSG system. The motive was to sample the voltage and current waveform as many times as possible within a cycle. In order to achieve this attempts were made to use the numeric processor in parallel with the CPU. However to make the software compatible for general purpose use and for easy reading modules for specific purposes were created.

The processing time was kept to a minimum by manipulating the intermediate results in the various computations within the general purpose registers of the Single Board Computer. Memory references were made minimal and unnecessary movement of data was avoided. The 8 MHz clock on the single board computer resulted in a instruction cycle time of 250 nanoseconds (with instructions in queue). The overall processing time was about 1 millisecond for the voltage controller and around 1.4 milliseconds after

inclusion of the reactive power controller. The time for acquisition and conversion of six VSG system parameters and the Voltage and Frequency reference was approximately 400 microseconds. However this time period is used by the Numeric Extension Processor to compute the square root of the sum of squares of the three line voltages. The display software was designed to interrupt the main flow of the controller program in order to transfer a block of memory to the supervisory IBM PC-AT. The transfer was done at 19200 baud and hardly had any effect on the processing time of the entire controller program.

4.3.5. Limitations :

The software has some limitations basically because of the constraints introduced by the Single Board Computer and the Analog Input and Analog Output modules. The major constraint was that all computations had to be done in integers. In order to nevertheless make the controller sensitive enough, efforts were made to scale the variables and offsets were introduced. The program had to keep track of the scalings for proper operation of the controller. Because of the Analog input and Analog output module's resolution of 12-bits, no full advantage of the 16-bit CPU could be taken with the integer calculations.

The difference equations derived for integration required a large gain value in order to make the integration sensitive to small errors, keeping in mind that the time

delay between two samples was around 1.4 milliseconds. Moreover the difference equation for the first order filter led to an undesirable limit cycle saturation. If the error is constant then its contribution to the entire equation also remains constant. However, if this contribution was equal to the amount by which the computation of the first term in the equation decreased from its initial value then the output of the filter eventually becomes a constant. This value might not be the final value expected of the filter. The reason for this undesirable effect is round-off error of the error signal.In order to resolve this problem, the first order filter had to implemented by means of the use of the floating point processor. This resulted in an increase of the processing time by 300 microseconds. However the trade off was effective implementation of the first order filter.

4.3.6. Possible Improvements :

The software could be improved by making full use of the capabilities of the CPU for multitasking and also by making use of idle time of the processor during the conversion effort of the analog input module. This could easily have reduced the processing time by approximately 250 to 300 microseconds. The time delay between two samples was observed by sending a high value through the 8255 PPI before the processing began and sending a low value after the processing ended on the oscilloscope. This was not the ideal way to find the time delay and may result in a different

time delay in each cycle. An efficient method would have been to employ the 8254 Programmable Interval Timer on the single board computer. This would ensure a constant time delay between each sample.

5. VERIFICATION OF THE CONTROL

5.1. INTRODUCTION :

The result of the implementation of the control, as described in chapter 4, is the main topic of discussion in this chapter. The effectiveness of the controllers on the VSG system over the entire range of operation was verified. Adequate response speed of these controllers is demonstrated by actual measurements. The limitations and possible improvements in the implementation of the controllers will also be discussed. The implementation was verified step by step. First the voltage controller was verified on the VSG system and then the reactive power controller was introduced as a supervisory control means.

5.2 VOLTAGE CONTROLLER :

The voltage controller for the VSG system as described in the previous chapters was implemented using the single board computer and the accompanying software. It was verified on the actual VSG system and the following sub-sections discuss the dynamic behavior and the limitations along with ideas for improvement. The observations will be presented in the form of plots and figures which support the arguments in the discussions.

5.2.1. Dynamic Behavior :

The effectiveness of the voltage controller was tested on the VSG system. The feedback loop gain, K_c, was varied over a range of values between 5 and 200 and it was seen that the system was most stable at a gain value of 100 for higher frequencies. The flexibility of digital control was exploited by changing the gain value dynamically in real time and the stability of the VSG system was observed. The VSG system could sustain astep change to the voltage reference of 15% and FIG 5.1 shows the response of the system terminal voltage. The effectiveness of the controller was evident from a sudden load change too. A 10% increase in the load current was created and this resulted in a lower terminal voltage then the reference value. However the controller kept the terminal voltage at the set reference value and FIG 5.2 shows the response of the same.

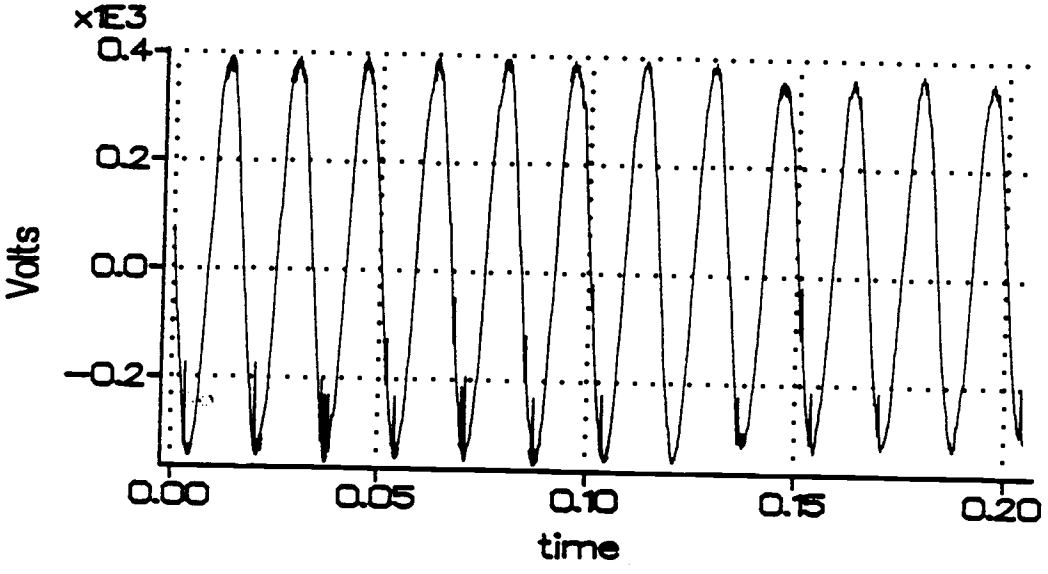

Figure 5.1 : Response of the VSG system to a step change in reference voltage of 15%

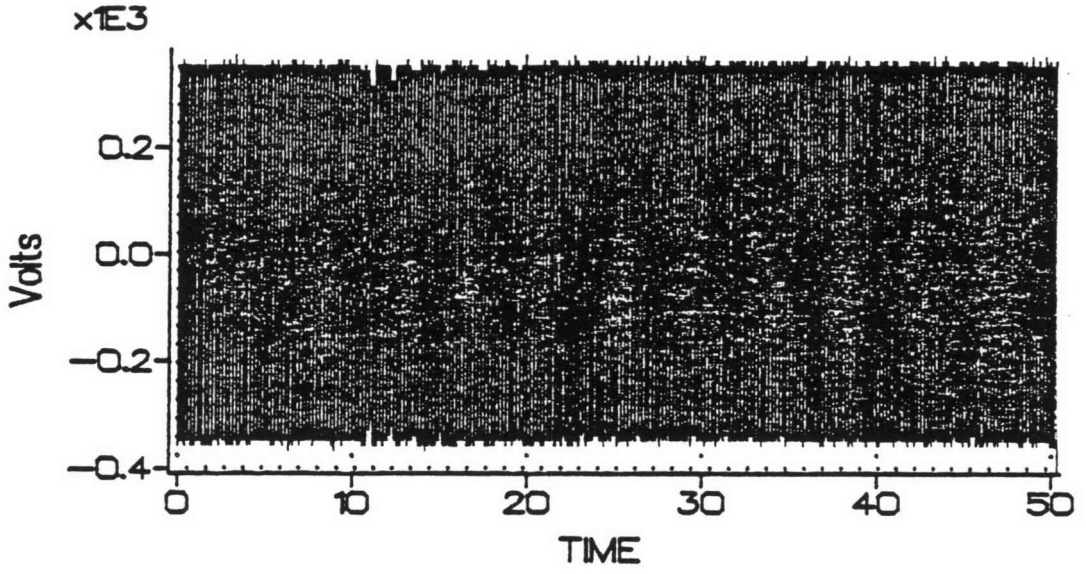

Figure 5.2 : Response of the VSG system to a sudden change in load.

However, the above observation was at a reference frequency of 40 Hz. The system became unstable below a reference frequency of 25 Hz with an integration gain of 100. Attempts were made to make the controller adaptive, in the sense that the closed feedback loop gain was decreased to 10 as the frequency of the VSG system went below 30 Hz. The non-linearity of the system obviously needed the linear controller to adapt for different operating conditions. Most critical was the sensitivity of the system performance to the shaft speed.

The effectiveness of the voltage controller is evident from the fact that the terminal voltage changed to the reference voltage within one cycle.

5.2.2. Limitations and Possible Improvements :

The limitation of the voltage controller as implemented was that the output of the controller needs to be limited in order to avoid an excessive output current of the power electronic converter. Therefore, a higher step change in the voltage reference was actually not effective. This basically was mainly due to the fact that the output of the controller went to the limits and obviously these limits prevented further changes to the terminal voltage. The feedback loop gain value could be chosen based on the specific requirements of the user and the values suggested were found to be effective for the system under consideration.

One of the main problem was to find an ideal value of the feedback loop gain and the non-linearity of the system prevented a single value to be effective over the entire range of operation. A better performance could result if the flexibility and ease with which the gain could be varied is exploited. Such an effort is expected to lead to a self-adaptive controller and is a worthwhile topic of further research.

5.3. REACTIVE POWER CONTROLLER :

The reactive power controller as described in previous chapters was implemented. The response of the VSG system which includes this controller was subject of detailed observations and the following sub-sections discuss them briefly. The reactive power controller is to be considered part of the supervisory controller and provides the voltage controller with a target reference to keep the reactive power of the VSG system at the desired reference value.

5.3.1. Dynamic Behavior :

The reactive power controller was verified by switching from voltage control to reactive power control. It was observed that the system remained stable and the reactive power controller kept the reactive power at the desired reference value.

The response speed of the reactive power controller was kept at an order of magnitude lower than the voltage controller to avoid undesirable interactions between the two controllers. An integration gain value of 20 and filter time constant of 20 seconds was found to be effective for the considered VSG system. This resulted in the reactive power controller sensitive to small fluctuations in reactive power and the filter is included in order to prevent the controller from oscillating. The controller's effectiveness was verified by introducing a step change in the reactive

power reference value. It was observed that the system was stable for a step change of 1000 VARS and FIG 5.3 shows that the corresponding response of the reactive power is quite satisfactory.

Detailed experiments with the reactive power controller's performance under varying shaft-speed conditions have led to the conclusion that reducing the integration gain to a value of 5 as the frequency reference went below 30 Hz is effective in avoiding undesirable interactions between the two controllers.

5.3.2. Limitations and Possible Improvements :

The reactive power output was varying and a better operation of the controller could have been achieved if the averaging process was improved. However since the response speed of the controller was not critical, the performance of the VSG system is not significantly affected. It was also observed that at lower reference frequencies the parameters for integration and filtering were not ideal as they were for higher reference frequencies. It can be expected that more study would result in a reactive power control which is adaptive over the entire range of operating conditions.

Finally, due to hardware problems in the power electronic converter and the single board computer, and also due to lack of time the verification of the efficiency maximizer is not presented here.

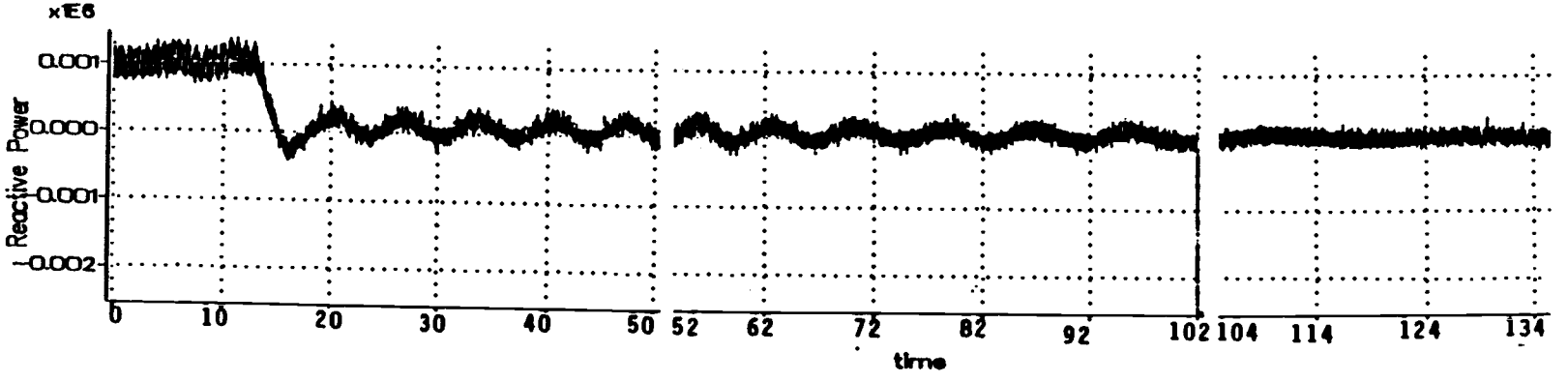

Figure 5.3 : Response of the reactive power controller to a change of 1000 VARs in the reactive power.

6. CONCLUSIONS

The advantages of a Variable Speed Generation (VSG) system over the Fixed Speed Generation system is elucidated. The controllers which are required to maintain maximum efficiency operating conditions of the VSG system, irrespective of varying resources, were briefly discussed.

The controllers were implemented on the actual VSG system and the various constraints involved in the development of the software were presented. The effectiveness of the controllers on the VSG system is evident from the results obtained from the experiments carried out.

The main hardware problem faced during the development was related to ground loops between the various system components. Considerable care had to be taken in order to eliminate the corresponding undesirable effects of noise on the data acquisition effort as well as on assuring the quality of the signal processing.

The processing time had to be as small as possible in order to implement all control tasks effectively. This was achieved by using a fast processor and utilizing the Numeric

Extension Processor in parallel with the main processor. A better implementation could be achieved if the developed software is modified to make full use of the capabilities of the 80286 processor in multitasking. The utilization of the IBM PC-AT as a supervisory control device is only for the purpose of development convenience in the design of the controllers. The Single Board Computer used has the capability to drive a terminal and a keyboard, and could actually include the Display software as well.

The flexibility of the microprocessor based control is exploited in on-line parameter adjustments and, therefore, adaptive control. It was shown that such an effort is critical to the operation of the VSG system at varying shaft speeds. Recall that the shaft speed variation is needed to maintain maximum efficiency operation if the resource conditions vary.

The results of the implemented real time controller for the VSG system on the Single Board Computer demonstrates that the controller is capable of producing the desired terminal voltage as specified by the reactive power dispatch strategy.

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