AN ABSTRACT OF THE THESIS OF

Bangda Yang for the degree of Master of Science in Electrical and Computer Engineering presented on December 1, 2010.
Title: Feedforward Noise Cancelling Techniques.

Abstract approved:

_____

Pavan Kumar Hanumolu

Supply noise is one of the major considerations in almost all analog building blocks. In the past, adequate supply rejection is usually achieved with circuit isolation or excess capacitive coupling. However, this brute force method requires large silicon area and degrades feedback bandwidth. In this study, a method of enhancing the power supply rejection (PSR) of a system by using a fast feed-forward path to cancel the noise is investigated. This method is applied to a 25mA, 0.18μm low drop-out regulator (LDO) as well as a 1.5mW, 500MHz to 2.5GHz charge pump phase locked loop (PLL). Simulation results show that this feedforward noise cancellation (FFNC) method improves PSR of either system by at least 20dB up to a noise frequency of 10MHz. Measurement of the two prototype circuits that have been fabricated in National Semiconductor's CMOS9T5V 0.18μm process show an improvement of at least 16dB in PSR at 10MHz. A background calibration method that is used to provide the correct gain for the FFNC is also designed and tested

Key Words: Supply Noise, Active Cancellation, Background Calibration, LDO, PLL

©Copyright by Bangda Yang
December 1, 2010
All Rights Reserved

Feedforward Noise Cancelling Techniques

by

Bangda Yang

A THESIS

Submitted to

Oregon State University

in partial fulfillment of
the requirements for the
degree of

Master of Science

Presented December 1, 2010

Commencement June 2011

Master of Science thesis of Bangda Yang presented on December 1, 2010

APPROVED:

_____

Major Professor, representing Electrical and Computer Engineering

_____

Director of the School of Electrical Engineering and Computer Science

_____

Dean of the Graduate School

I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

_____

Bangda Yang, Author

ACKNOWLEDGEMENTS

First I would like to thank my advisor, Professor Pavan Kumar Hanumolu. Professor Hanumolu generously accepted me into his group after mentoring me through my undergraduate thesis. Every group meeting he has given us valuable feedbacks and suggestions, and has patiently and openly guided us whenever problems came up. I am grateful to have such a major professor with both profound technical knowledge and willingness to help. I also would like to thank Professor Un-ku Moon and Professor Gabor Temes to take time to serve on my committee.

I worked with Brian Drost on this project and his contribution to this thesis is just as valuable, if not more. So I would like to him for giving me his insights on circuit design throughout our countless discussions. I also would like to give thanks to other group mates in the Kelley office: Sachin Rao, Qadeer Khan, Amr Elshazly, Nima Maghari, Jon Guerber, and Jeff Pai, for their numerous random discussions the filled me with suggestions and encouragements both inside and outside the research group.

National Semiconductor has funded the prototype chip of this project, and provided support with the fabrication of the chip. I am fortunate to have the tape-out experience with their fabrication process without having to deal with the financial cost. Last but not least I would like to thank my mom for the years of love and support.

TABLE OF CONTENTS

Page

TABLE OF CONTENTS (CONTINUED)

Page

LIST OF FIGURES

LIST OF FIGURES (CONTINUED)

FEEDFORWARD NOISE CANCELLATION TECHNIQUES

BANGDA YANG

FEEDFOWARD NOISE CANCELLATION TECHNIQUES

1. INTRODUCTION

Electronic noise in the power supply, or supply noise, affects all circuits that are powered by it. Supply noise in general degrades circuit performance, and is one of the major design challenges in many analog building blocks. Two example circuits that are especially sensitive to supply noise are low dropout regulators (LDOs) and phase locked-loops (PLLs). The supply noise in LDOs is mainly fed through the pass transistor to the output as voltage noise. The supply noise in PLLs is mainly fed through the most sensitive building block, the voltage controlled oscillator (VCO), and translated to deterministic jitter at the output. The goal of this work is to use a fast feedfoward path to cancel supply noise and reduce the noise passed to the output.

1.1 Supply Noise in LDOs

A LDO regulator is a linear feedback circuit that is used to provide a stable voltage source for the following circuits under different load current conditions. An important property of a LDO is the shielding of the fluctuation from the supply [1]-[4]. Therefore, it is great interest to design a high power supply rejection (PSR) LDO that serves as a buffering block between the noisy analog input circuits such as DC-DC converters and the following noise sensitive circuits.

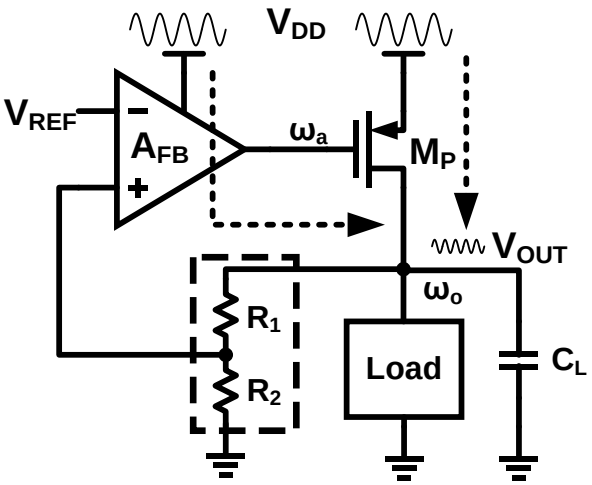

Figure 1: Typical LDO with Noise Paths to Output

A conventional LDO shown in Figure 1 contains an error amplifier (A_{FB}), a pass transistor (M_P), a load capacitor (C_L) and a compensation capacitor (C_C). Resistive divider formed by R_1 and R_2 shown in dashed box are used to adjust the output voltage (V_{OUT}). Since they do not affect supply noise property of the LDO, they are omitted for the LDO used in this investigation. The negative feedback provided by the A_{FB} and M_P forces V_{OUT} to be close to reference voltage (V_{REF}) within the feedback bandwidth. Supply noise can transfer to the output through M_P, or through the supply of the A_{FB}. The noise from the A_{FB} supply mainly depends on its power supply rejection ratio (PSRR) of the A_{FB} [5], and is significantly smaller than the noise from the M_P at frequencies beyond the dominant pole, where degradation in PSR is of most concern [3]. Since LDO is a linear feedback system, AC analysis provides a description of how the system responds to fluctuation on the supply. For this LDO, two dominant poles are present [1]–[4]. One sits at the output of the A_{FB} (ω_a) and the other one sits at V_{OUT} (ω_o). One of the two poles must be forced as the dominant pole to make the system stable. Even though the LDO is the stable whether ω_o or ω_a is set as the dominant pole, the LDO's PSR response is vastly

different [3] [6]-[8]. Assuming all noise signals are come through M_P, the transfer function from supply to output (V_{OUT}/V_{DD}) is derived as [6]-[8]:

$$\frac{V_{OUT}(s)}{V_{DD}(s)} = \left(\frac{R_L}{R_L + r_0}\right)\frac{1}{(1+s/\omega_o)\left[1+LG(s)\right]} \quad (1)$$

where $LG(s) = \dfrac{A_a A_0}{(1+s/\omega_o)(1+s/\omega_a)}$ is the loop gain of the LDO,

$A_o = g_m(r_0 \,||\, R_L)$ is the DC gain of M_P, A_a is the amplifier DC gain

The PSR AC response of a typical LDO based on Equation 1 is plotted in Figure 2. The graph contains two cases when either ω_a or ω_o is set as the dominant pole. When the ω_a dominates, PSR rolls up after ω_a because the feedback loop gain is reduced. This roll-up continues until the unity-gain frequency (ω_{UGB}), where PSR remains flat because the noise is only reduced by the resistive divider formed between M_P and the equivalent load resistance, R_L. PSR improves after ω_o because the C_L starts to reduce the output impedance. In the second case where the ω_o dominates, the PSR remains flat from DC until ω_{UGB} because the reduction in loop gain is cancelled with the decrease in the output impedance. At frequencies beyond ω_{UGB}, loop gain stays constant and ω_o continues to improve the rejection.

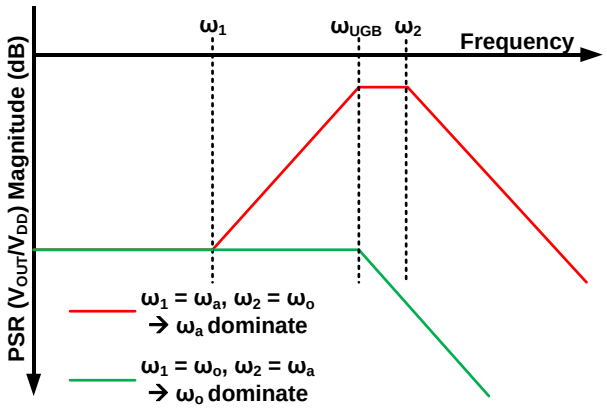

Figure 2: LDO PSR Response of Different Pole Locations

Base on these observations, it is desirable to make ω_o dominant to eliminate the peaking in the PSR. However, in order to maintain a small dropout voltage across M_P, large device sizes must be used to reduce the overdrive voltage. Using large device size increases the gate parasitic capacitance and lowers ω_a [3]. ω_o also changes with different load currents and C_L sizes specified for transient response. In the past, the brute force method of improve PSR is to simply use a large C_L in the µF range so that even at high load current, ω_o is still the dominant pole. However, for on-chip applications, the size of the load capacitor is severely limited to a few hundreds of picofarads. ω_a is further lowered because the amplifier is often designed as a transconductance (g_m) cell with high output resistance in order to conserve current in the output stage. Therefore, it is more practical to have ω_a as the dominant pole. C_C to supply is used, as in Figure 1, in instead of Miller compensation [4] due to degradation in PSR caused by the noise coupling through the C_C. Making ω_a dominant brings the challenge of reducing the peaking of PSR at $\omega_{UGB.}$

Several techniques have been introduced in recent years to mitigate supply noise without using a large, off-chip C_L. One idea is to isolate the output from the supply with higher pass transistor resistance by using a NMOS [1]. This method however, creates higher dropout voltage and requires extra charge pump circuit to raise the gate voltage. The noise from the charge pump must also be filtered out. Another way to combat supply noise is to use feed-forward path to actively cancel the noise [2]. The circuit, however, still used a 4µF off chip load capacitor, and also used fixed resistors and two amplifiers to set feedforward gain. Using multiple amplifiers limits feedforward bandwidth and fixed resistors fixes feedfoward gain and makes the cancellation unusable for different load conditions. The goal of this investigation is to design a LDO without any off-chip capacitance and achieve respectable PSR up to 10MHz under different load and dropout conditions.

1.2 Supply Noise in PLLs

A PLL is a feedback system that is used to generate a high frequency clock from a low frequency reference clock. Charge pump based PLLs are widely used for its low static phase offset, simplicity and effectiveness. A conventional charge pump based PLL diagram is shown in Figure 4. The PLL works as follows: phase-frequency detector (PDF) extracts the difference, or phase error, between the output clock (Φ_{OUT}) and the reference clock (Φ_{REF}) and generates a pair of pulse signals. The pulses are then fed to a charge pump (CP). With the addition of a loop filter (C_1, R, C_2) the output either ramps up or down depending on the phase error. This control voltage (V_{CTRL}) from CP then changes the frequency of the voltage controlled oscillator (VCO) accordingly. The divider (1/N) is added to create a higher multiple of reference clock frequency. At steady state, the V_{CTRL} stabilizes. Φ_{OUT} and Φ_{OUT} are then considered to be "locked."

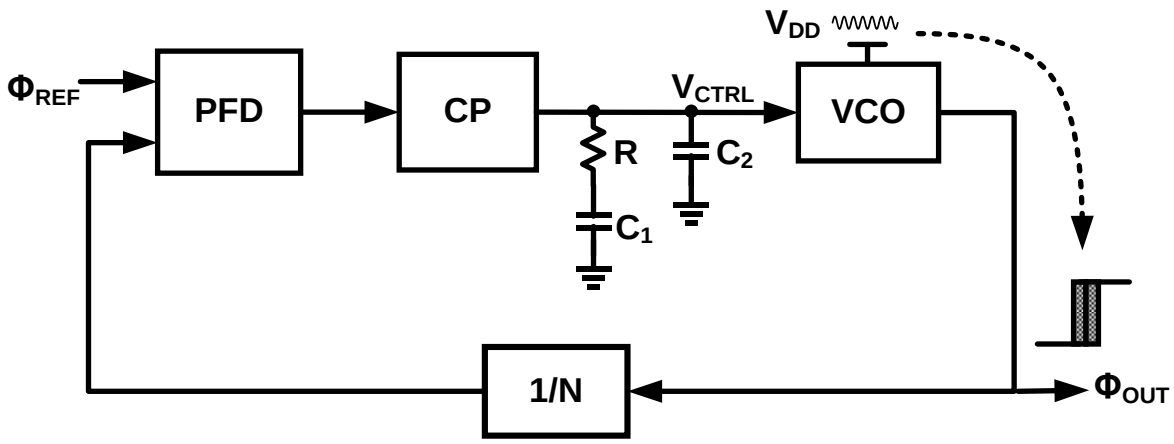

Figure 3: Conventional Charge Pump PLL with Supply Noise Paths to Output

Since all PLL building blocks are attached to the supply, each block will have noise transfer to the output. The amount of noise, however, differs greatly due to the supply rejection property of the block and its transfer characteristic to the output [6]-[7] [10].

Because PLL output is a clock signal, the noise at the output is translated into jitter, the clock edge variation in time domain. Therefore one of the major performance goals of a PLL is to minimize the overall jitter in the output. To quantify jitter as a function of supply noise, power supply noise rejection (PSNR) is used, defined as [10]:

$$\text{PSNR[dB]}=20\log_{10}\left(\frac{T_j / T}{\Delta V_{DD}}\right) \quad (2)$$

Where T_j is the peak-to-peak jitter of a clock signal with period T. ΔV_{DD} is the amplitude of a sinusoidal supply noise. For example, a PLL with a PSNR of -10dB operating at 2GHz experiencing a ΔV_{DD} of 100mV has a peak-to-peak jitter of 31.6ps. Even though all PLL blocks contribute noise to the output, VCO is the most sensitive block and dominates noises coming from other parts [6]-[10].

Ring oscillator based VCO is widely used because it offers higher gain, wider tuning range and is simpler to implement and design [6]. Therefore, tackling the supply noise coming through the VCO has been studied extensively [6]-[10]. The conventional approach is to use a LDO to regulate the supply of the VCO so that it shields the noise from the ring oscillator based VCO, as pictured in Figure 6.

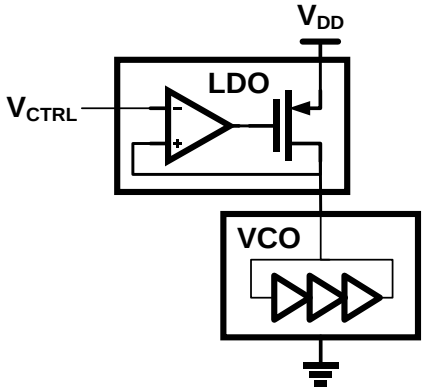

Figure 4: LDO Supply Regulated VCO

As discussed in the last section, making the output pole (ω_o) dominant provides LDO with better supply noise suppression. This, however, is even more difficult to achieve in this case because the LDO poles are inside the PLL loop. The LDO poles jeopardize PLL stability unless they are pushed to much higher frequency than the PLL bandwidth, which requires very high power consumption. [7] uses a replica based LDO to compensate the poles of the LDO. The fast replica loop introduces a zero in the LDO loop so that ω_{oa} is closer to ω_o. This architecture, however, still suffers power penalty or else all the LDO poles would fall inside the PLL bandwidth. The other goal of this work is to improve the PSNR of a PLL by applying the same feedfoward noise cancellation techniques that is used in the LDO.

1.3 Thesis Organization

Chapter 2 introduces the feedfoward noise cancellation (FFNC) technique and provides a theoretical analysis on the effectiveness of the feedfoward cancellation technique. The analysis is followed by a discussion on background calibration required to provide the correct gain. The purposed architectures for the LDO and PLL based on FFNC are introduced in the end.

Chapter 3 discusses the detailed circuit implementations for both the LDO and the PLL.

Chapter 4 shows the measured silicon prototype results for both circuits.

Chapter 5 discusses the significance of the result and draws upon the conclusion.

2. FEEDFORWARD NOISE CANCELLATION

Feedforward techniques have been widely used in control systems and circuits, mainly for its fast transient response. The high bandwidth, direct path from input to output provided by feedforward can also be used to cancel noises that the system feedback is too slow to correct. Whereas feedback uses its loop gain to suppress undesired deviations at low frequencies, feedforward comes to play at higher frequencies when the loop gain degrades. This chapter introduces the feedforward noise cancellation (FFNC) technique, discusses the limitations of FFNC, introduces the calibration idea for the FFNC to function under different load conditions, and proposes the architectures of LDO and PLL that implement FFNC.

2.1 Feedforward Noise Cancellation in LDO

LDO has supply rejection from its feedback at low frequencies, and if the error amplifier pole ω_a were made to be dominant, then the rejection rolls off at -20dB/dec after ω_a. In other words, the supply rejection is limited by the bandwidth of the system. It is possible to expend the rejection bandwidth of the system by adding a feedforward path from the input to the output. Since this feedforward path is not limited by the dominant pole $\omega_{a,}$ it improves the rejection on top of the rejection provided by feedback.

2.1.1 Low Frequency Noise Cancellation Model

To take a closer look at how the feedforward cancellation works, Figure 1 depicts the open loop first order, low frequency, small-signal model of a LDO with PMOS pass transistor M_P.

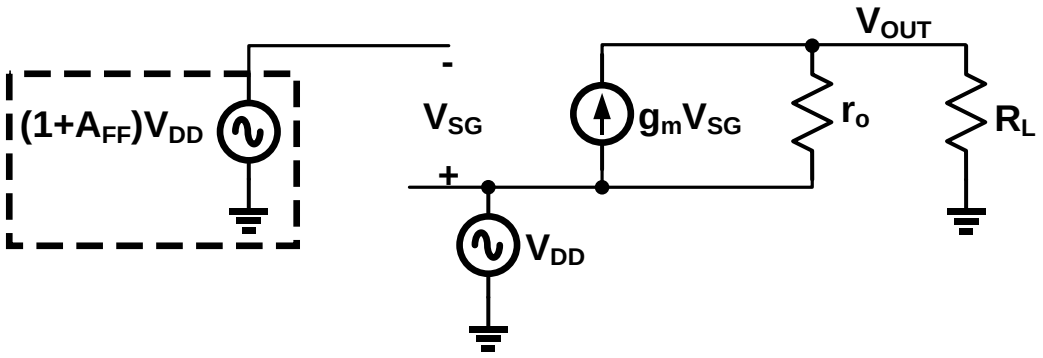

Figure 5: Open Loop First Order Small-signal LDO with Feedforward Gain

Similar to Equation 1, the supply-to-output transfer function can be derived as:

$$\frac{V_{OUT}}{V_{DD}} = \left(\frac{R_L}{R_L + r_0} \right)(1 + g_m r_0) \qquad (3)$$

Equation 3 shows that for the first-order model, M_P's output resistance r_0 forms a voltage divider with the load resistance R_L, and the noise current from the g_m source effectively amplifies the output noise by a factor of $g_m r_0$. The g_m noise current can be eliminated when the gate and source of M_P experience the same swing. However, even if all the noise current from g_m source is cancelled through perfect coupling, there is still the current coming through r_0. One way to cancel the noise current is to add an amplified version of the supply noise at the gate of the M_P, shown inside the dashed box. This way V_{SG} is controlled by the gain A_{FF}, and the g_m source would sink the appropriate amount of current so that the net noise current flowing through R_L is zero. Ideally, to find the gain required to cancel the noise current, set $V_{OUT} = 0$:

$$A_{FF} = \frac{-\cancel{(1+R_L/r_0)V_{OUT}} + \cancel{(R_L/r_0)V_{DD}}}{g_m \cdot \cancel{R_L \cdot V_{DD}}} = \frac{1}{g_m r_0} \qquad (4)$$

Equation 3 shows that the ideal gain required to cancel the noise is approximately the inverse of M_P's intrinsic gain, $1/g_m r_0$, if the gate and source of M_P are perfectly coupled. This simple analysis is mainly to provide an insight into the cancellation and an estimate for the optimal gain required for noise cancellation at low frequencies. In practical circuit design, setting the gain to a fixed value of $1/g_m r_0$ severely limits the effectiveness of cancellation. First of all, g_m and r_0 are small-signal parameters that cannot be measured directly. They are also heavily depended on many different conditions, such as the load current, I_D. While g_m varies approximately proportional to I_D, r_0 varies approximately inversely with I_D. Therefore as I_D changes, the required gain also changes. Other variation including process voltage and temperature (PVT) would also alter the gain required for cancellation. To improve noise cancellation at different load conditions, a calibration method which will be discussed later this chapter is required.

2.1.3 Effect of LDO Feedback

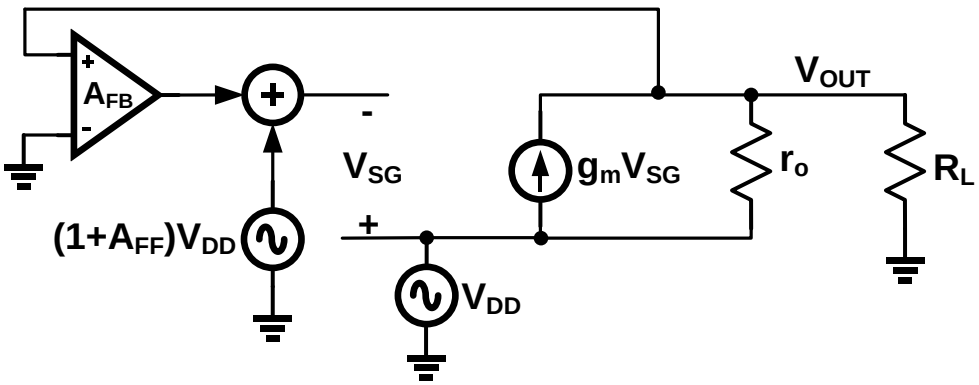

Figure 6: First-order LDO Noise Cancellation Model with Feedback

The previous analysis assumed open-loop feedforward operation. However, since the LDO is always operating inside a main feedback loop, care must be taken to make sure the feedforward path does not interfering with the feedback operation. The first-order model of a LDO with feedforward and feedback loop is shown in Figure 6. The supply-to-output transfer function is then derived as:

$$\frac{V_{OUT}}{V_{DD}} = \left(\frac{R_L}{R_L + r_0} \right) \frac{\left[1 - g_m r_0 A_{FF}\right] \Rightarrow \text{Feedforward}}{\left[1 + A_{FB} g_m (r_0 \parallel R_L)\right] \Rightarrow \text{Feedback}} \tag{5}$$

The denominator of Equation 5 is the noise suppression provided by the feedback, which is approximately the loop gain of the feedback system, and the numerator is the cancellation provide by the feedforward. This shows that feedback and feedforward are decoupled and can work together. Adding in the two main poles from feedback, ω_o and ω_a, the denominator of Equation 5 becomes that of Equation 1, while no change is done in the numerator. Even when there is a pole in the feedforward path, it only degrades the effectiveness of the feedforward cancellation and does not compromise the feedback loop stability since it is outside of loop.

2.2 Feedforward Noise Cancellation Limitations

The results in Equation 5 shows that the amount of supply noise cancellation is only limited by how close one can make the ideal feedforward gain to be $1/g_m r_0$. However, in practical circuit design, many factors limit the effectiveness of FFNC. Three major factors include parasitic capacitances, feedforward bandwidth, and transistor non-linearity. Gaining some intuitions on these topics also help the designer prioritizing circuit characteristics to maximize the effectiveness of noise cancellation.

2.1.2 Effect of Parastic Capacitances at High Frequencies

The results shown in Equation 4 apply to low frequency noises when the parasitic capacitances play an insignificant role. The major parasitic capacitances of a MOS transistor include junction capacitance C_{DB} and C_{SB}, as well as overlap capacitances C_{GS} and C_{GD}. Since M_P is a P-channel MOS transistor, the bulk is tied to the source to reduce the threshold voltage V_T. In doing so, C_{SB} is shorted. C_{GS} is coupled between the two voltage sources and does not play a significant role. Therefore the two most relevant parasitic capacitances are C_{GD} and C_{DB}, as depicted in Figure 7.

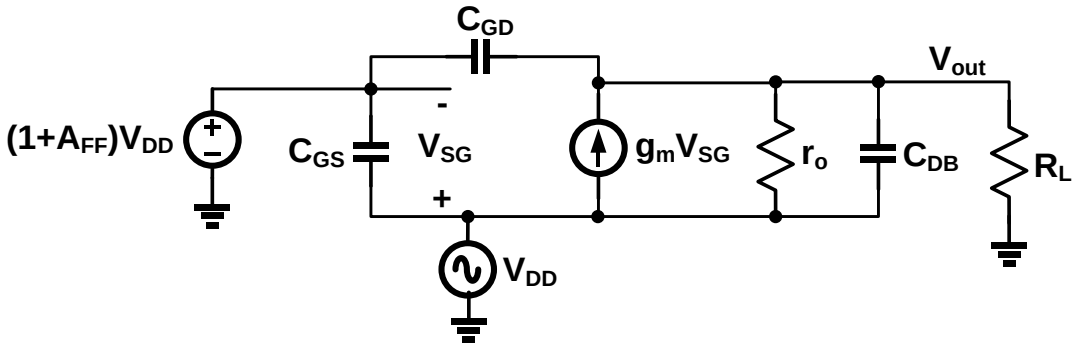

Figure 7: LDO Noise Cancellation Model with Major Parastic Capacitances

The ideal gain for noise cancellation is derived as:

$$\frac{V_{OUT}}{V_{DD}} = \frac{s(C_{GD} + C_{DB}) + 1/r_0}{g_m - sC_{GD}} \tag{6}$$

The result in Equation 6 gives some insight as to how the ideal gain should change in frequency in order for complete noise cancellation at output. At low frequencies, the capacitances are open and the gain should be $1/g_m r_0$. The gain stays at $1/g_m r_0$ up the zero frequency $1/[r_0(C_{GD} + C_{DB})]$, beyond which the gain increases since C_{DB} is shorting out r_0. At very high frequencies, the overall gain at the gate approaches to the capacitive divider formed by C_{GD} and C_{DB}. The response is plotted in Figure 8 with typical transistor values.

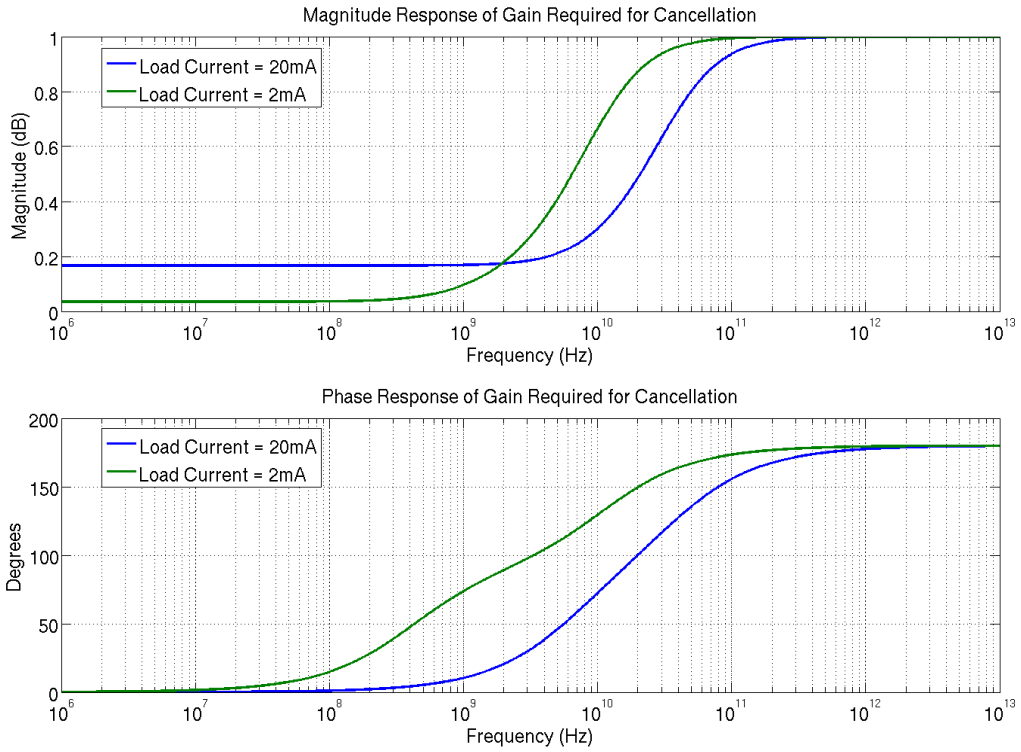

Figure 8: Magnitude and Phase of the Ideal Gain for Cancellation

The plot also shows how load current affects the required gain. At low load current when the intrinsic gain is large, the required gain for cancellation is small. The point at which the gain rolls off also occurs at a lower frequency because of the larger r_0. The opposite occurs under higher load current. The phase plot also shows a sign inversion at very high frequencies.

The conclusion from this short analysis is that beyond certain frequency based on transistor M_P's small-signal parameters, both magnitude and phase of the gain required for noise cancellation changes and becomes increasingly harder to obtain. Fortunately, even under the worst case at low load current, the roll-off in gain does not occur beyond the output pole of the LDO. This thesis focuses on the band frequencies where the PSR starts to degrade and peaks at the point when the output starts to take effect.

2.1.3 Effect of Feedforward Bandwidth

The bandwidth of the feedforward path is limited by the parasitic resistance and capacitance when combining the signal at the gate of the pass transistor. The bandwidth of the feedforward path plays a critical role in the overall effectiveness of the cancellation. Following the same first-order model in the previous analysis, but now assume there is a feedforward pole at ω_p. In other word, the gain is now:

$$A_{FF} = \frac{1/(g_m r_0)}{1 + s/\omega_P} \tag{7}$$

The supply-to-output transfer function now becomes:

$$\frac{V_{OUT}}{V_{DD}} = \frac{R_L}{R_L + r_0}\left(\frac{s/\omega_P}{1 + s/\omega_P}\right) \tag{8}$$

This simple analysis shows that the pole in the feedforward path directly limits FFNC. This is because the pole causes a variation in the ideal gain at all frequencies. Another physical explanation is that finite bandwidth will always introduces a delay and thus no matter how close the gain is to the ideal value, there will always be some left over noise from the subtraction. Putting some numbers into perspective, if the feedforward pole is at 400MHz, then the maximum rejection FFNC can provide for a noise frequency of 10MHz is approximately 1/40, or -32dB. Maximizing feedforward bandwidth such as reducing the output resistance of the feedforward amplifier and the parasitic capacitances, in particular C_{GD} is the priority of circuit design.

A plot of a typical PSR with feedforward cancellation with some static DC cancellation error is shown in Figure 9. Even though feedforward alone is limited by its bandwidth, the rejection is added on top of that provided by feedback and the resistive divider.

Therefore, it is desirable to have feedforward provide the cancellation for frequencies for which the feedback is least effective.

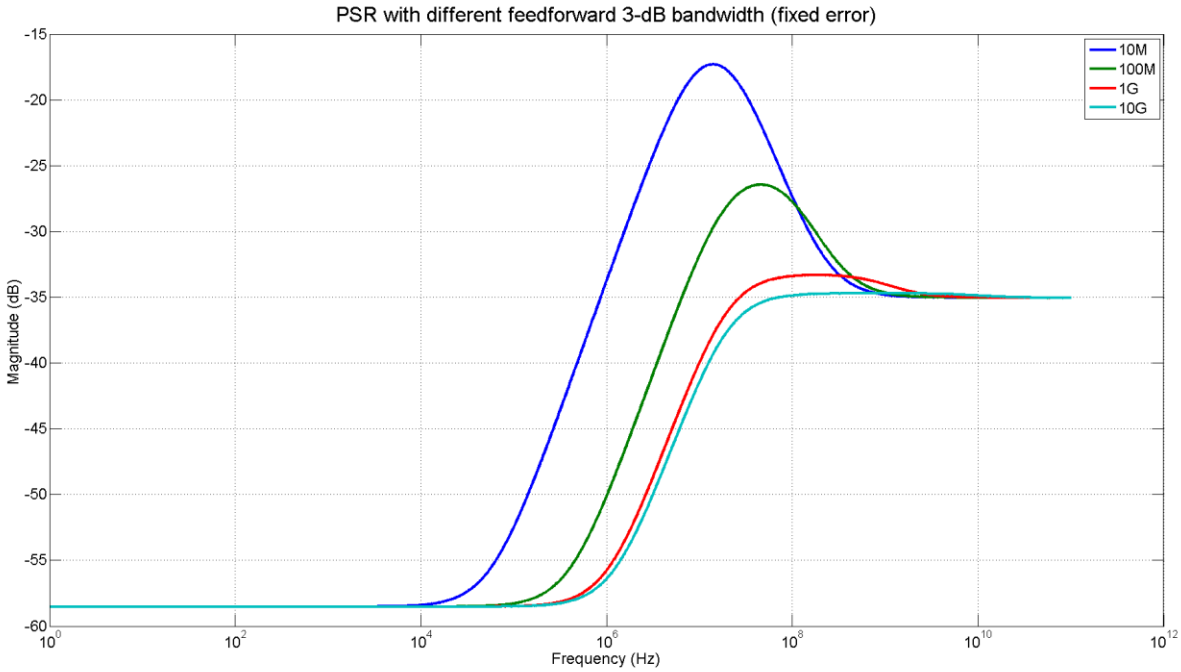

Figure 9: Effect of Feedforward Bandwidth on PSR

2.1.3 Effect of Transistor Non-linearity

The previous analysis assumes a linear model where small-signal parameters are independent of supply noise amplitude. But in actual circuit, both g_m and r_0 of the M_P are function of output voltage. This dependence causes higher order harmonics at the output. Referring to a typical LDO as in Figure 1, both r_0 and g_m are non-linear function of V_{DD}. In most cases r_0 causes more non-linearity than g_m because $\delta I_D/\delta V_{GS}$ is more linear than $\delta V_{DS}/\delta I_D$. The gate is coupled to the source so the contribution from g_m is insignificant compared to r_0. Figure 10 shows a plot of r_0 as a function of V_{DS}. The nonlinearity worsens for V_{DS} less than 200mV.

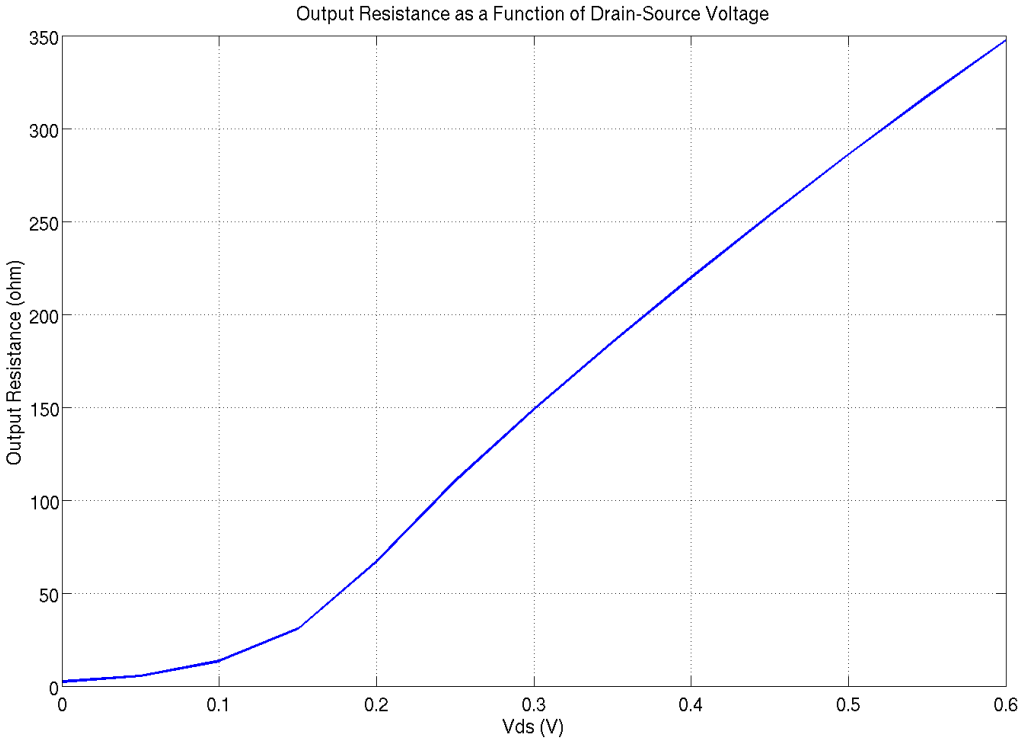

Figure 10: Pass Transistor Output Resistance vs. V_{DS}

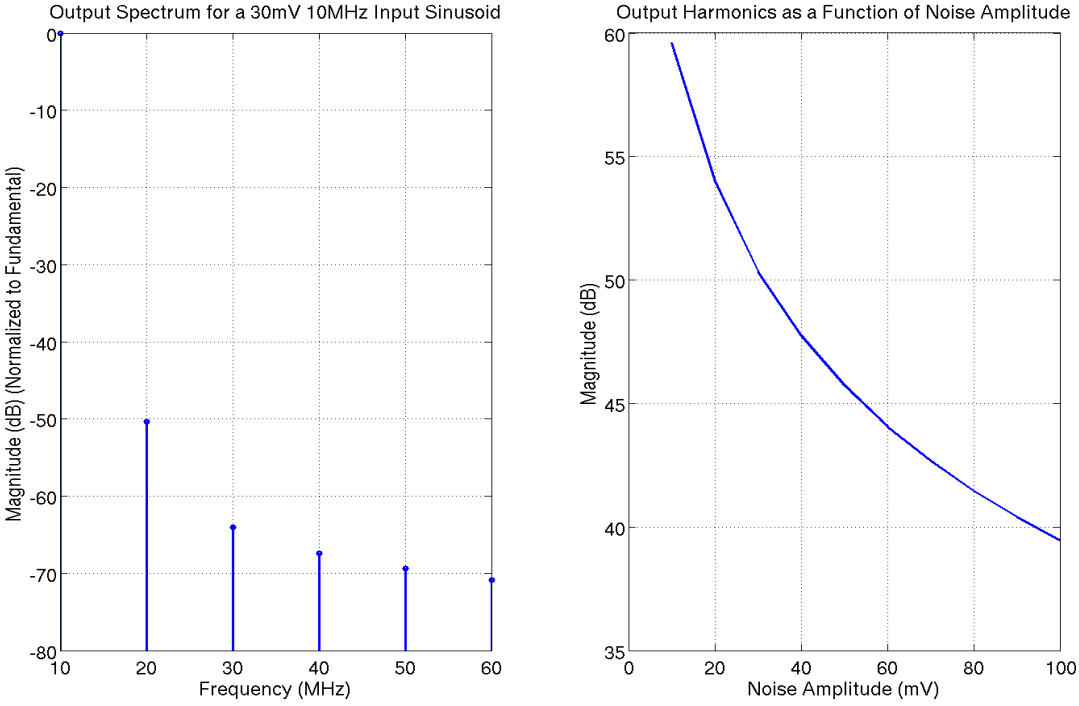

Figure 11: LDO Output Spectrum and Harmonic Difference vs. Noise Amplitude

One drawback of noise cancellation is that it cannot suppress the higher harmonics caused by g_m and r_0. Since both are functions of different variables, hand analysis becomes tedious and gives little insight. Therefore, several simulation plots are generated to show the significance of non-linearity. Using the circuit in Figure 1, Figure 11 shows output spectrum for a 30mV, 10MHz sinusoid input on V_{DD}, as well as the difference between the fundamental and second harmonic as a function of noise amplitude.

As one can see from Figure 11, noise peak-to-peak amplitude greater than 80mV gives a second harmonic, which cannot be cancelled by this method, is only -40dB below the fundamental. This is confirmed by another simulation with the noise cancellation applied to the LDO. Before and after cancellation, as shown in Figure 12, the fundamental is reduced by -32dB while the second harmonic rises because of the increasing small-signal variations in V_{DS}.

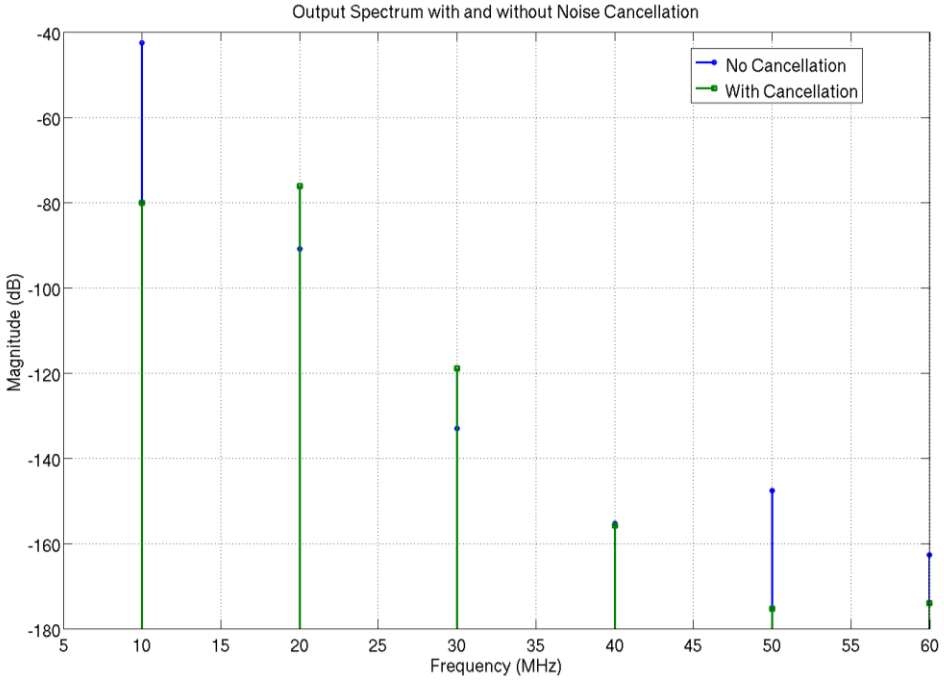

Figure 12: Output Spectrum with Noise Cancellation

2.3 Feedforward Noise Cancellation in PLL

PLL has natural rejection at both low frequency and high frequency due to integration. At low frequency, the PLL's high DC gain suppressed phase noise. At high frequency, the integration from the VCO reduces the noise. The worst case PSR occurs at around the PLL bandwidth [6]-[8] [10]. In other words, the PSR is of most concern only in the vicinity of the PLL bandwidth. Therefore, as long as noise cancellation is effective within this region, the overall PSR is improved. Ring oscillator based VCO are highly sensitivity to supply noise. The easiest way to control the oscillation frequency is to use a pass transistor, M_P, to control to current supplied to the VCO, as shown in Figure 11.

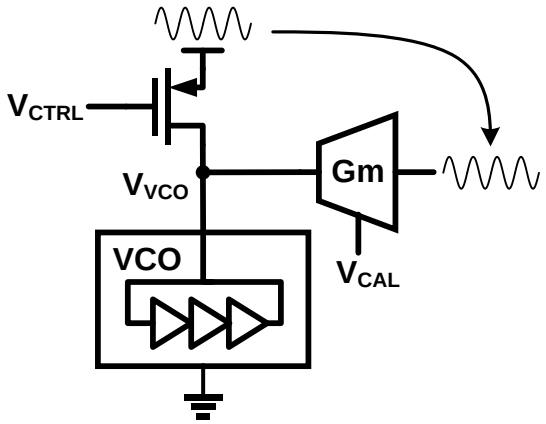

Figure 13: VCO with Noise Cancellation

In Figure 13, V_{CTRL} is the control voltage produced by the charge pump. The noise cancellation can be done the same way as for the LDO. However, since the VCO's current consumption is at least an order of magnitude smaller than LDO's load current, the feedforward amplifier G_M can be place at the virtual supply of the ring oscillators to cancel noise current directly. Since current summation occurs at V_{VCO}, the ideal gain is in terms of transconductance, for the first-order model is changed to:

$$G_M = \frac{1}{V_{DD}} \frac{V_{DD} - V_{VCO}}{r_0} = \frac{1}{r_0} \quad \textbf{(9)}$$

This makes sense since GM is only required to eliminate current through r_0. Regardless of what the exact value is for noise cancellation, similar to LDO cancellation, any variations in load current, or any other process, voltage and temperature (PVT) variations would make it into a different value. Therefore, a method calibration must be used to find the optimal value for the different load and PVT conditions.

2.4 Background Calibration

A method of calibration is required to bring the feedforward gain to an optimal value. The amount of gain needed for noise cancellation is closely related to the correlation between the noise signal and the output signal. If the two signals are highly correlated, then the noise at the output is in phase with the supply noise, and the output noise is only due to the resistive divider formed by r_0 and R_L. A positive noise current into R_L means that the feedforward gain is not high enough. On the other hand, if the two signals are uncorrelated, then the output noise is 180° out of phase with the supply noise. This 180° phase shift of the noise current at the output is because of too much gain. Base on this reasoning, the correlation between the noise signal and the output signal would indication whether the feedforward gain should increase or decrease. In steady state, the correlation output, V_{CAL}, should settle, with some ripple, to an optimal value. The output noise would also be 90° out of phase with the supply. The calibration using concept of correlation is illustrated in Figure 14.

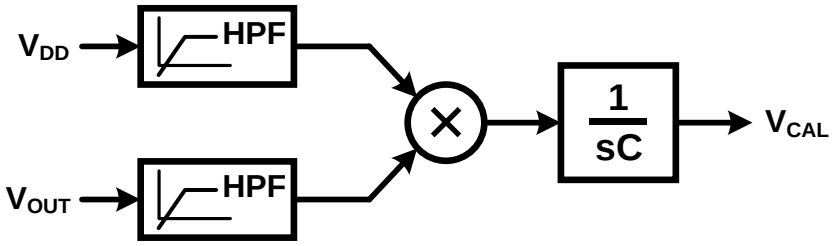

Figure 14: Calibration Block Diagram

In Figure 14, the supply noise and the output are mixed together, and are subsequently low pass filtered. The mixing operation performs a correlation on the two signals, with the output DC level representing the amount of correlation. Since the feedforward signal is high passed before it is added to the feedback signal, no DC component is fed to the mixing operation. The calibration bandwidth is still designed to be at least an order of magnitude slower than the main loop bandwidth to avoid large ripples on the settling voltage.

Since the PSR of an LDO rolls up after the first pole, this causes a zero and the phase response experiences a phase shift of 90°. The phase shift continues until ω_{UGB}, when the pole in the PSR response cancels with the zero. This means calibration can only operate near ω_{UGB}. This is not a severe problem because the worst case PSR occurs near ω_{UGB}, where it is of most concern. Another option is to use feedback control signal instead of the output. Because the VCO's virtual supply is not regulated to a known voltage, the feedback control voltage is used instead.

2.5 Proposed Architectures

2.5.1 LDO Architecture

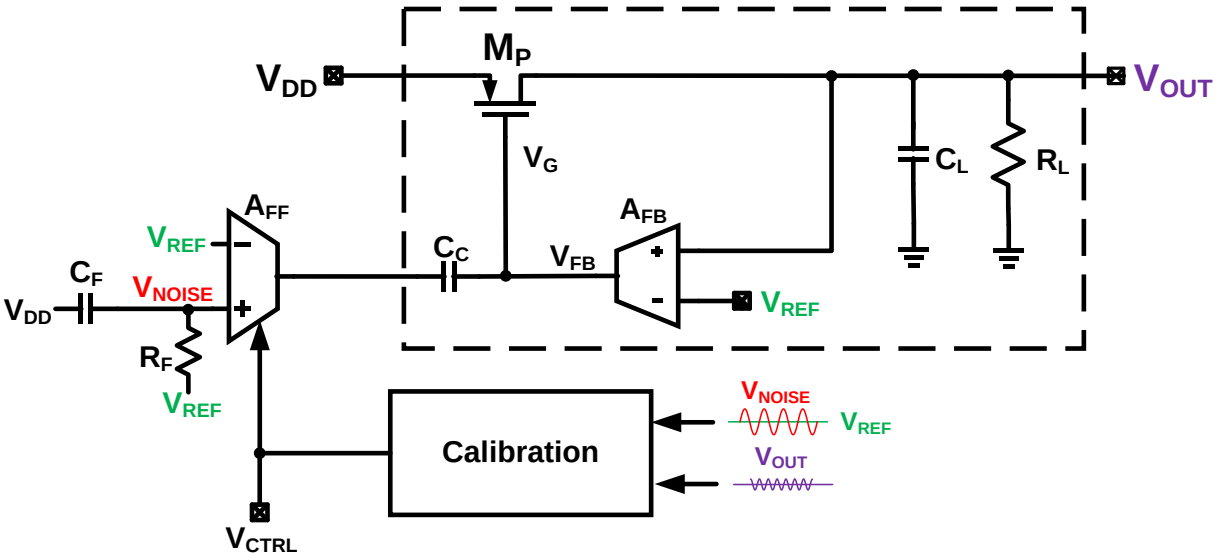

Figure 15: Purposed LDO Architecture Block Diagram

The proposed architecture for cancelling the supply in a LDO is shown in Figure 15. Inside the dashed box is the conventional LDO. The supply noise is fed through a variable gain transconductance amplifier A_{FF}, and combined with the main LDO feedback signal through current summation at V_G. The speed of this feedforward path is only limited by the pole approximated by the output resistance of A_{FF} and the parasitic capacitance C_{GD} of the pass transistor M_P. Since the output resistance of A_{FF} is designed to be orders of magnitude smaller than the output resistance of the feedback amplifier A_{FB}, the feedfoward bandwidth is decoupled from feedback bandwidth. In order to make the input to A_{FF} differential, a high pass filter is used to add the reference voltage V_{REF} to the supply noise while maintaining the V_{REF} as the DC voltage for both inputs. The calibration circuit performs a correlation between V_{NOISE} and V_{OUT}, and the calibration output is fed to the control input of A_{FF}.

2.5.2 PLL Architecture

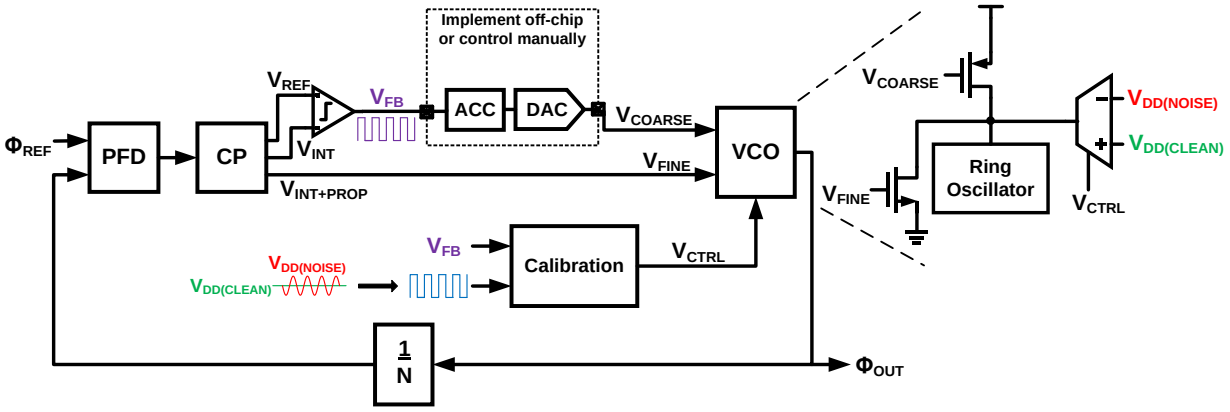

Figure 16: Purposed PLL Architecture Block Diagram

The proposed architecture for using a feedforward path to cancel the supply noise of a charge-pump PLL is shown in Figure 16. The conventional charge-pump PLL include a phase-frequency detector PFD, a charge pump CP, a voltage-controlled oscillator VCO and a clock divider 1/N. In addition to the conventional CPPLL setup, the VCO is split tuned by a high gain, slow varying

coarse signal, V_{COARSE}, and a low gain, fast varying fine control, V_{FINE}. The reason for using two control signals is to decouple the conflicting requirement of having a low VCO gain, K_{VCO}, for optimal noise performance and a high K_{VCO} for a wide tuning range. The coarse control is implemented digitally off-chip with an accumulator and a digital-to-analog converter (DAC).

Similar to the LDO, the supply noise is fed through a variable transconductance amplifier, A_{FF}, before added to the output. Since VCO draws much smaller amount of current, the virtual supply of the VCO is used for the addition instead the V_{COARSE} to maximize the bandwidth at higher power consumption. Since the coarse control path, V_{FB}, is quantized into a digital signal, the supply noise is also quantized to a digital signal using a comparator before the two signals are correlated digitally in the calibration circuit.

3. CIRCUIT DESIGN

Last chapter discussed, in theory, how the feedforward cancellation functions to cancel the supply noise. But in practice the performance is limited by the implementation of the idea. This chapter presents the detailed circuit schematics of both the LDO and the PLL, and provides explanations on how each building block operates and is designed to meet the specification.

3.1 LDO Circuit Design

The design of the LDO has been briefly discussed in the introductory chapter. One of the two major poles, ω_a or ω_o as the dominant pole in order to stabilize the system. For on-chip application where load capacitance is small, ω_a must be made dominant, and the degradation of PSR that came with the choice is the main alleviation brought by the purposed feedforward cancellation. Since the feedfoward bandwidth is limited by the parasitic of the pass transistor M_P, minimum length is used. Two amplifiers, one for the feedback loop gain and one for adjusting the feedforward gain, are required. A fast comparator for the calibration is also designed.

3.1.1 Feedback Amplifier

The main feedback loop amplifier A_{FB}, alone with the pass transistor M_P, must have high enough gain to achieve a low DC offset and small input-referred noise. A NMOS input, single stage folded cascode amplifier is designed and the schematic is shown in Figure 17. Since the M_P is

PMOS, the output of A_{FB} is PMOS diode-tided to couple the noise onto the output. This way the supply noise current through the g_m source of M_P is reduced. In other words, the PSRR of the amplifier is unity up to the bandwidth of the amplifier. The amplifier, together with M_P, has a loop gain of at least 65dB, shown in Figure 18. It also has a phase margin of at least 80º, a unity gain bandwidth of 2.5MHz, and consumes 20uA of current.

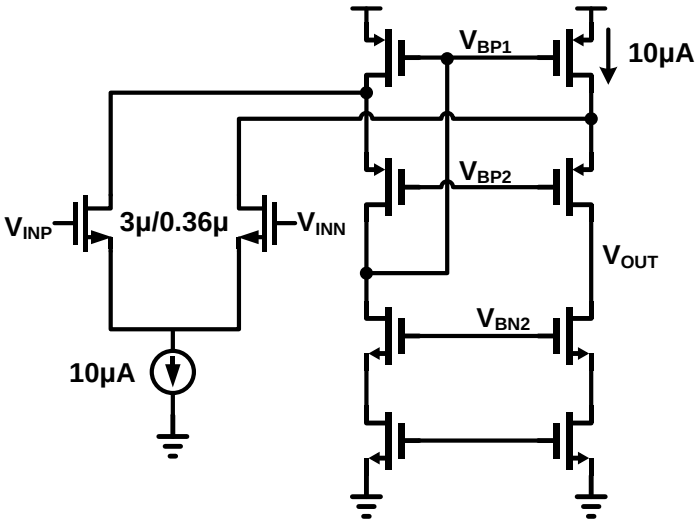

Figure 17: Feedback Amplifier Schematic

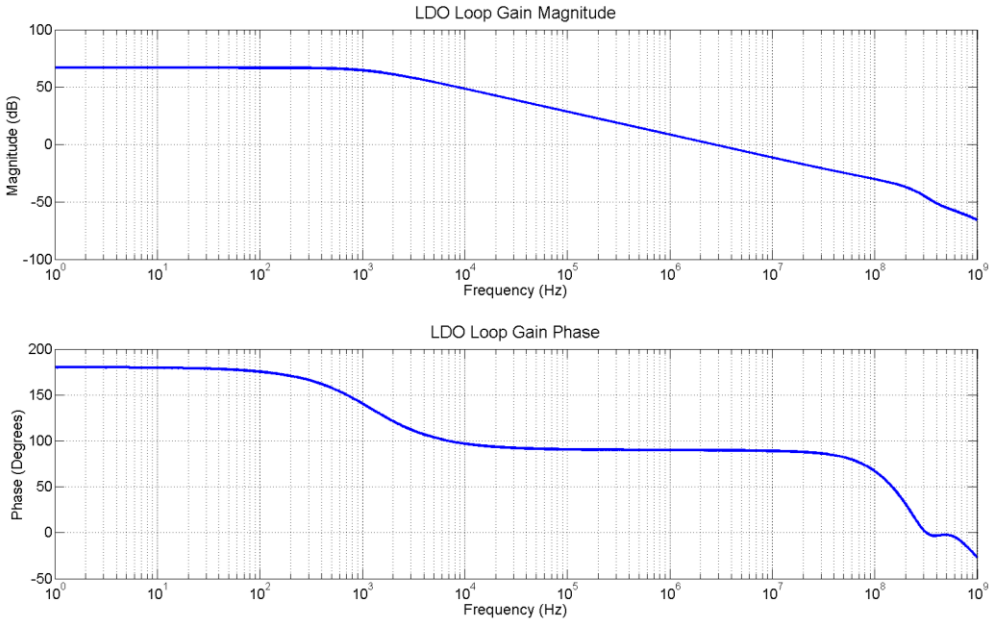

Figure 18: LDO Loop Gain Response

3.1.2 Feedforward Amplifier

The feedforward amplifier is used to adjust the gain for noise cancellation. The bandwidth directly limits the effectiveness of cancellation. With a noise frequency at 10MHz, a feedforward bandwidth of 300MHz provides roughly 30 times, or 30dB, of attenuation. A NMOS differential pair with resistive load is chosen for its simplicity. The control voltage governs the tail current source. The schematic of the amplifier is shown in Figure 19.

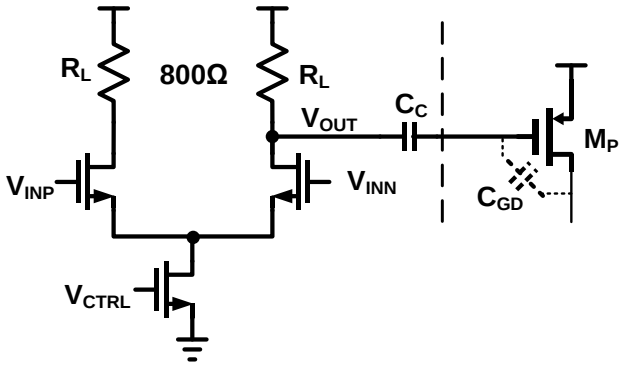

Figure 19: Feedforward Amplifier Schematic

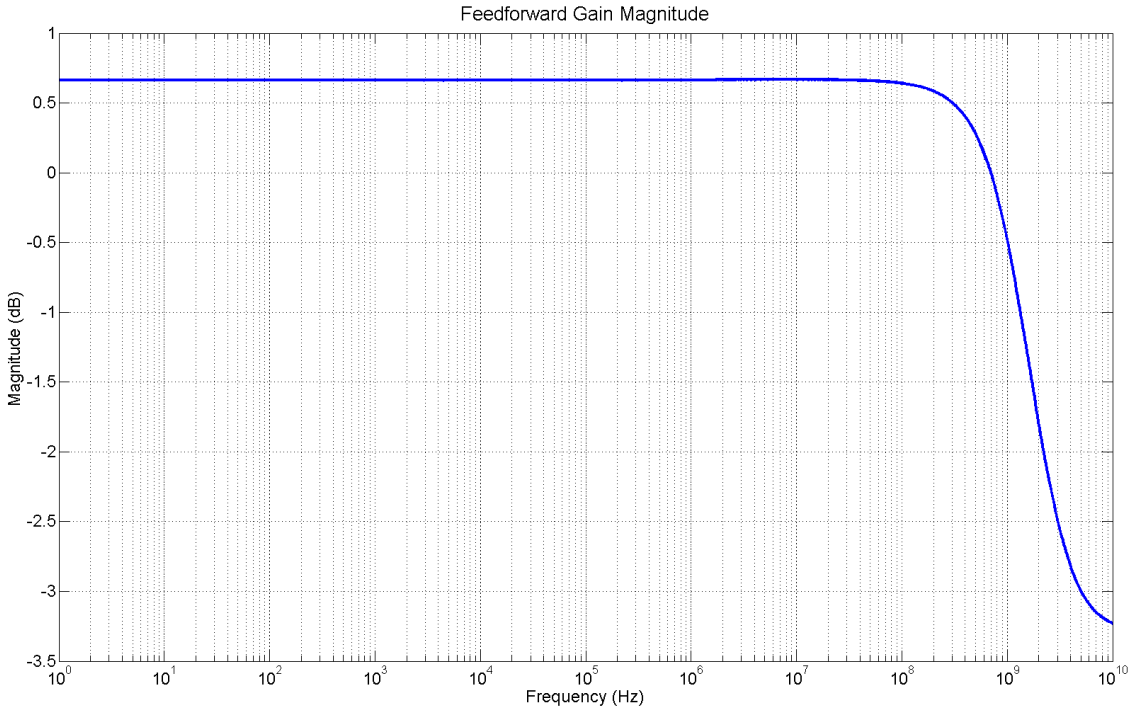

Figure 20: Feedforward Gain Magnitude at Gate of Pass Transistor

The feedforward bandwidth can be approximated as the pole formed by the output resistance and M_P parasitic capacitance C_{GD}. A plot of the simulated AC response from supply to the gate of M_P, V_G of Figure 15, is shown in Figure 20. The plot depicts the roll-off of feedforward gain at around 400MHz.

3.1.3 Calibration Circuit Design

The calibration circuit must be able to correlate the supply noise with the output noise. The two signals, V_{OUT} and V_{NOISE}, are first mixed using a circuit technique known as chopping [11]. Then the average of the mixed output is extracted by a GM-C filter, which is used as the control voltage V_{CTRL}. The schematic of the calibration circuit is shown in Figure 21.

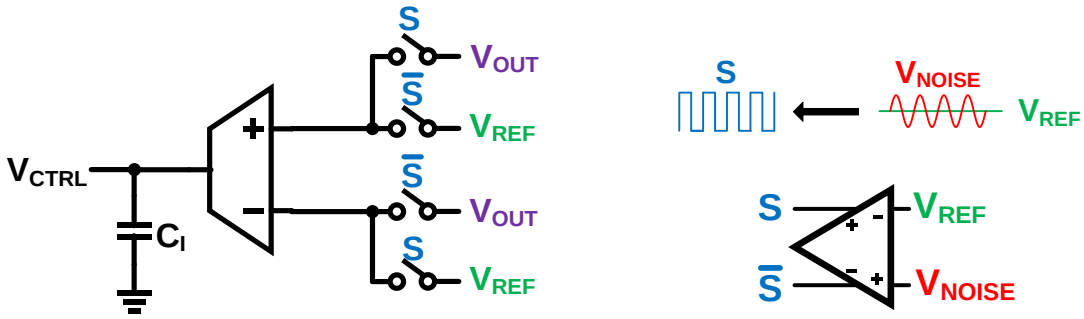

Figure 21: Calibration Circuit Schematic

The supply noise riding on a DC of V_{REF} is first quantized into a one-bit signal by the comparator. The quantized digital signal S is then used to switch back-and-forth polarity of the connection between V_{OUT} and V_{REF}. Simplified diagrams showing three common cases of circuit operation are in Figure 22. In the first case, the cancellation voltage is too low, so the LDO output noise is nearly in phase with the supply noise. Therefore, a positive DC value is embedded in the mixed signal. The second case is when the cancellation is too high, causing the output noise to be nearly 180° out of phase from the supply noise. Therefore, a negative DC value is produced in the mixed output. The third case is when the control voltage settles close to the optimal value and dithers up and down the 90° phase shift, with the mixed signal having an average of zero.

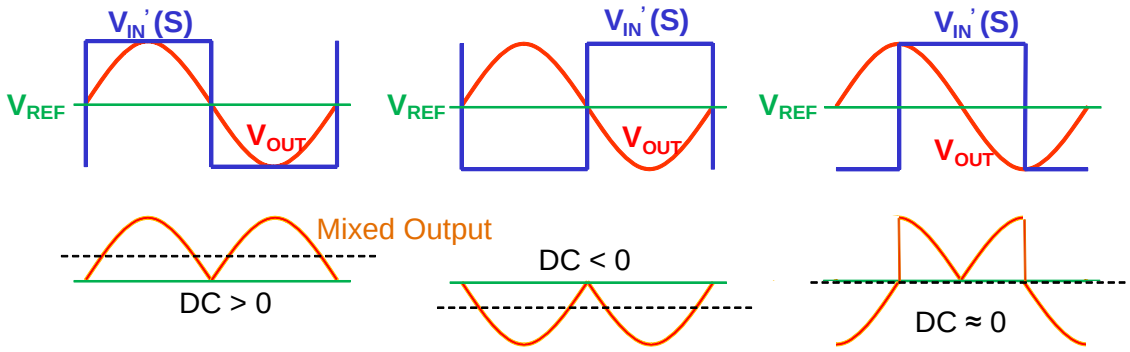

Figure 22: Calibration Waveforms

Together with output capacitor C_I, the transconductance amplifier used in the chopping operation acts as an integrator. So a high DC gain, low bandwidth amplifier is required. A NMOS input, two-stage folded cascode is used, and its schematic is shown in Figure 23. The second stage is cascode compensated for stabilizing the calibration loop. The amplifier achieves an open loop gain of 118dB.

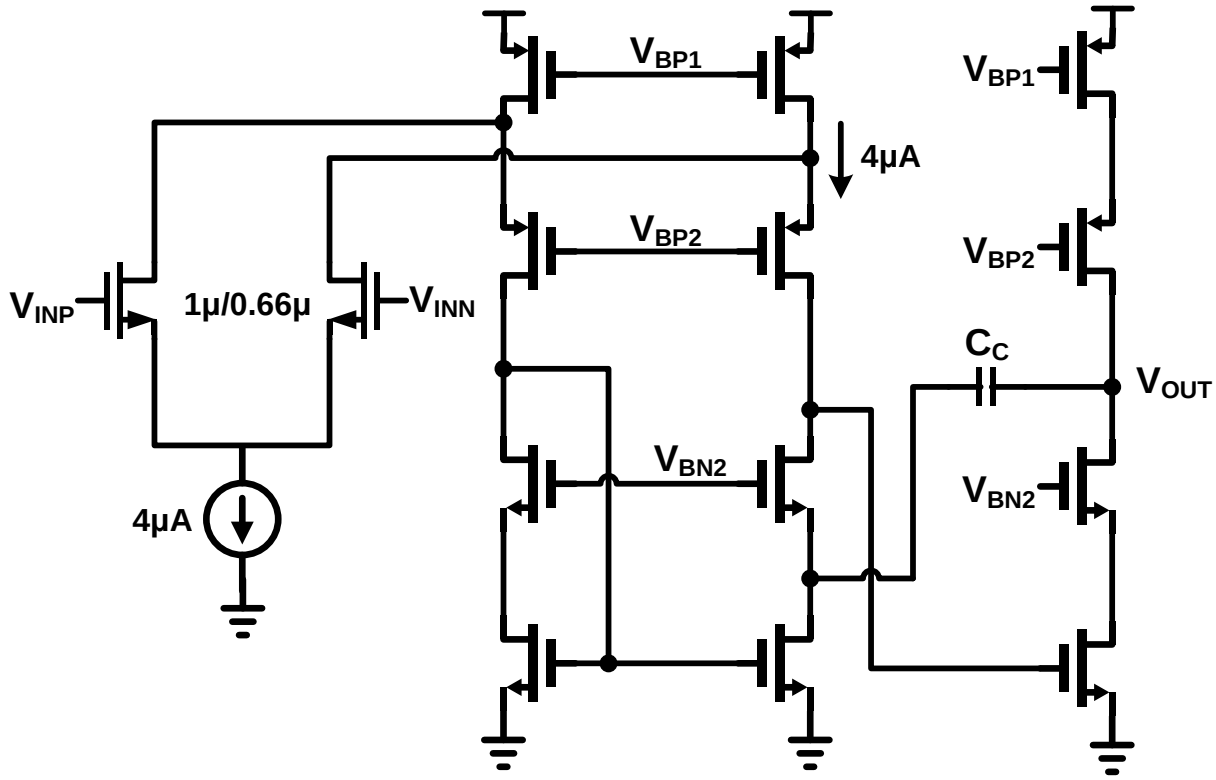

Figure 23: Calibration Amplifier Schematic

3.1.4 LDO Simulation Results

An AC simulation of LDO's PSR with all the building block in transistor level is shown in Figure 24. The simulation was under the condition of a resistive load current of 20mA, a dropout voltage of 300mV and a load capacitance of 20pF. The green curve is the PSR of the conventional LDO with the amplifier pole, ω_a, as the dominant pole. The blue curve is the PSR of the system without the rejection from the main feedback loop. The combined PSR is shown in red, where one can see the improvement the feedforward is providing in the region of most concern, namely from 1MHz to 10MHz.

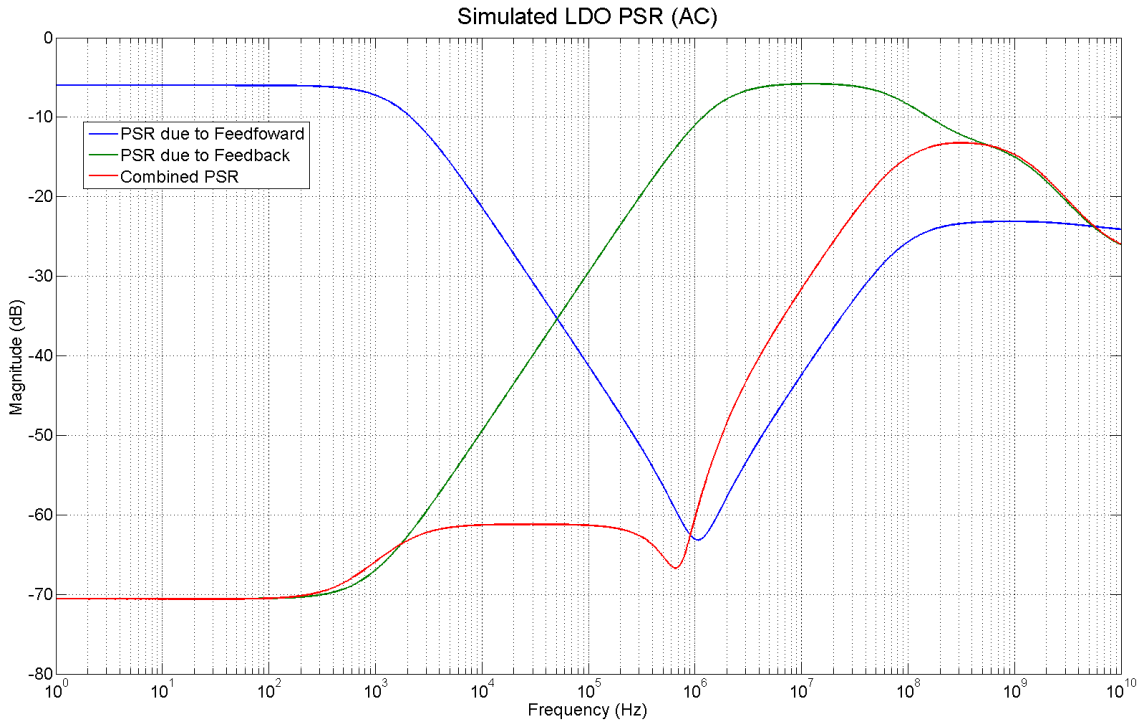

Figure 24: Simulation LDO PSR AC Response

The transient output of the calibration circuit is shown in Figure 25. The top graph shows the control voltage approaching the optimal control voltage. The bottom plot depicts the output converging to the consistent, stable noise amplitude. The final noise amplitude is determined by the second harmonic coming from pass transistor distortion.

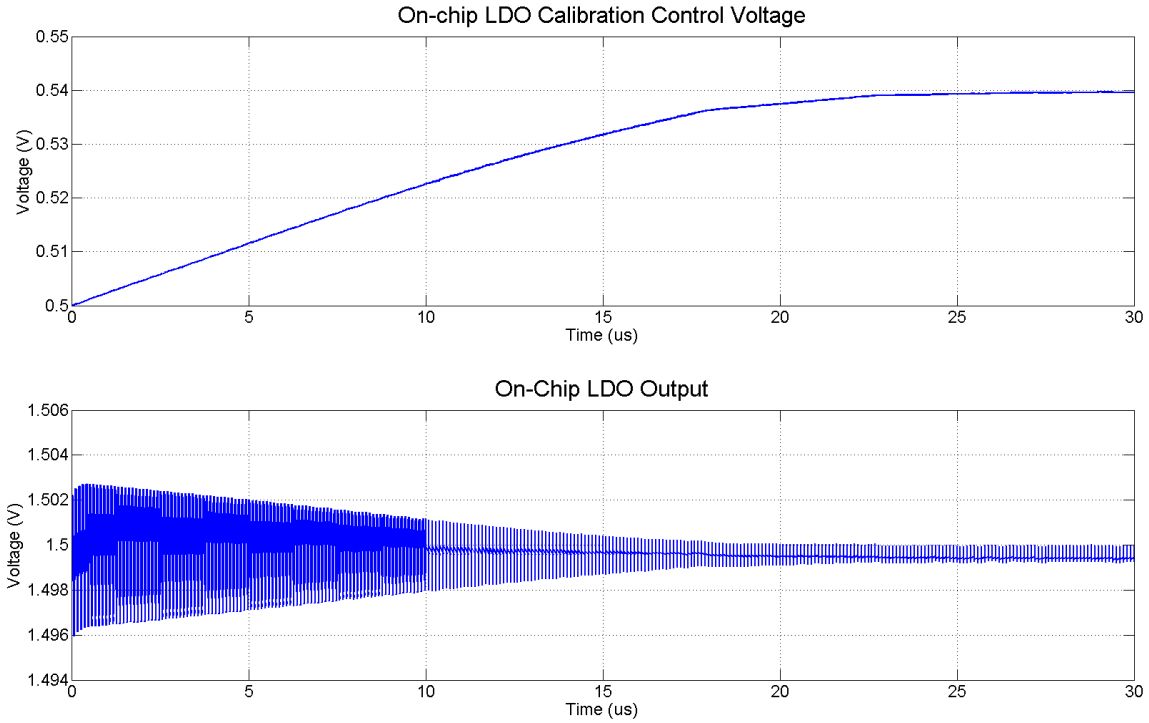

Figure 25: Simulated Control Voltage and LDO Output

The simulated LDO performance is summarized in Table 1. The supply DC V_{DD} is set to 1.8V, and the dropout voltage V_{DROP} is fixed at 300mV. Different load current conditions are simulated to see their effects on the cancellation. Peak-to-peak noise amplitude of 30mV is used in simulation. The PSR is measured as the noise amplitude difference in the transient simulation, after the control voltage is settled. A small decoupling capacitor of 22pF is added to the output.

I_L(mA)	**2**		**10**		**25**	
LG_{MAG} (dB)	72		67		62	
LG_{PM} (Deg)	84		90		91	
V_{CTRL} (mV)	483		523		581	
	No FFNC	FFNC	No FFNC	FFNC	No FFNC	FFNC
PSR (dB) @ 10MHz	-6.78	-29.02	-5.85	-27.81	-4.51	-26.3

Table 1: Simulated LDO Noise Cancellation Summary

3.2 PLL Circuit Design

The proposed PLL shown in Figure 16 contains the conventional components: PFD, CP, VCO and divider. A variable transconductance amplifier is also included to cancel supply noise similar to the LDO. In addition, split-tuned VCO technique is implemented with both coarse and fine path to expand the tuning range without sacrificing noise performance. In most cases, the VCO is the dominant noise source of the PLL, and it is effectively high-pass filtered by the feedback. Therefore, extending PLL bandwidth, ω_{PLL}, reduces the overall integrated noise. This approach is limited by the sampling effect such that the ω_{PLL} can be at most about 1/10 of the reference frequency, F_{REF}. In this design, the output frequency varies from 500MHz to 1.5GHz with a fixed divider of 4. This means F_{REF} varies from 125 to 375 MHz, which limits the bandwidth to 12.5MHz. However, the design can be improved if the bandwidth increases proportionally with F_{REF}. This technique is called bandwidth tracking and is implemented in this design to reduce jitter without requiring large increases in power.

3.2.1 Voltage Controlled Oscillator

A six-stage inverter-based differential VCO was chosen, shown in Figure 26.

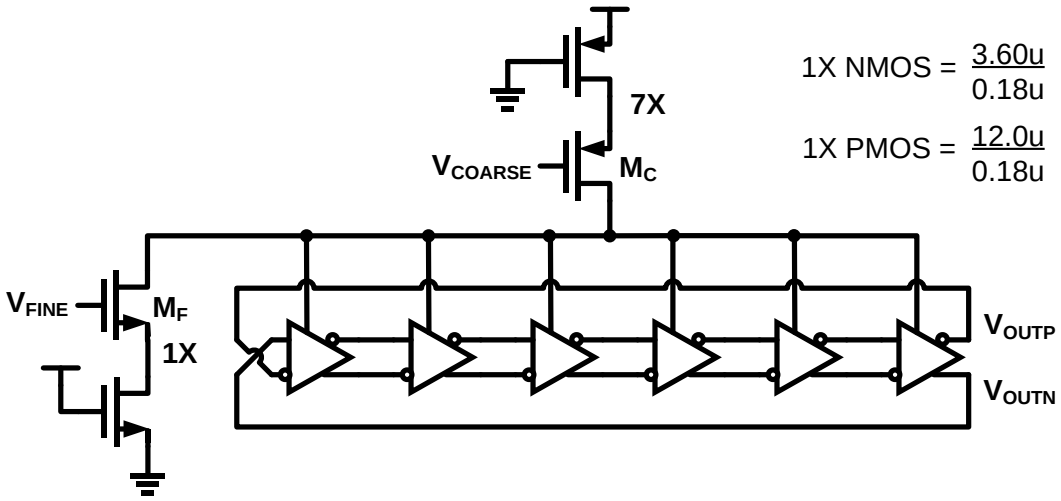

Figure 26: VCO Schematic

Six stages were chosen as a balance between phase noise and sufficient tuning range. Two pass transistors, M_C and M_F, are added to control the current to the delay cells. The larger M_C provides the coarse control to the split-tuned oscillator while the M_F provides the fine control. Therefore VCO gains, K_{VCO}, for the two paths are different and depend on the size ratio of the pass transistors. A ratio of seven is chosen to minimize the fast but noisy fine control and to maximize the slow but clean coarse control. The two paths are added by current summation at the supply node to the delay cells. This VCO architecture is compatible with bandwidth tracking since the VCO current can be mirrored from the PMOS transistor back to the charge pump.

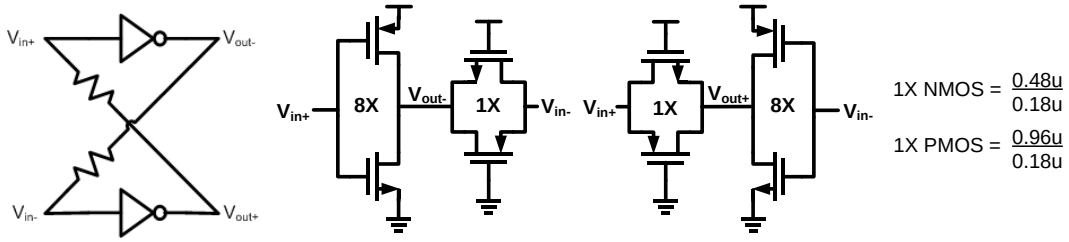

Figure 27: Inverter Cell Schematic

Each pseudo-differential inverter cell uses cross-coupled resistive elements to line up the phases between the two outputs, as shown in Figure 27. Using resistive elements instead of latches at the output of each stage avoids speed penalty required to overcome values stored in the latches. The resistive elements are implemented with minimum sized transmission gates. The width of inverters is eight times the minimum size, and the lengths are all set to minimum. This VCO has a phase noise to power ratio comparable to a single-ended inverter ring. The current consumption of the VCO is approximately proportional to the square of the frequency since the amplitude of the approximately oscillation scales with frequency:

$$I_{VCO} \propto V_C^2 \Rightarrow I_{VCO} \propto f_{VCO}^2 \quad \textbf{(10)}$$

This allows the square law device to provide a fairly linear K_{VCO}. The transfer characteristics for the coarse path and the phase noise for the VCO are shown below. The fine path transfer characteristic and K_{VCO} has the same trend as the coarse path except scaled by a factor of 7.

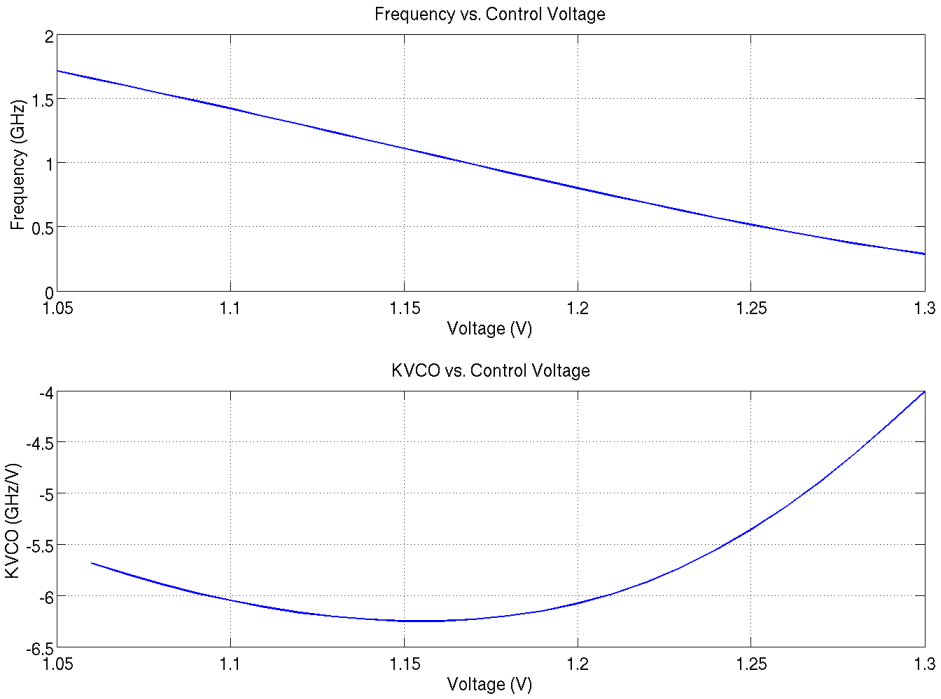

Figure 28: VCO Transfer Characteristics

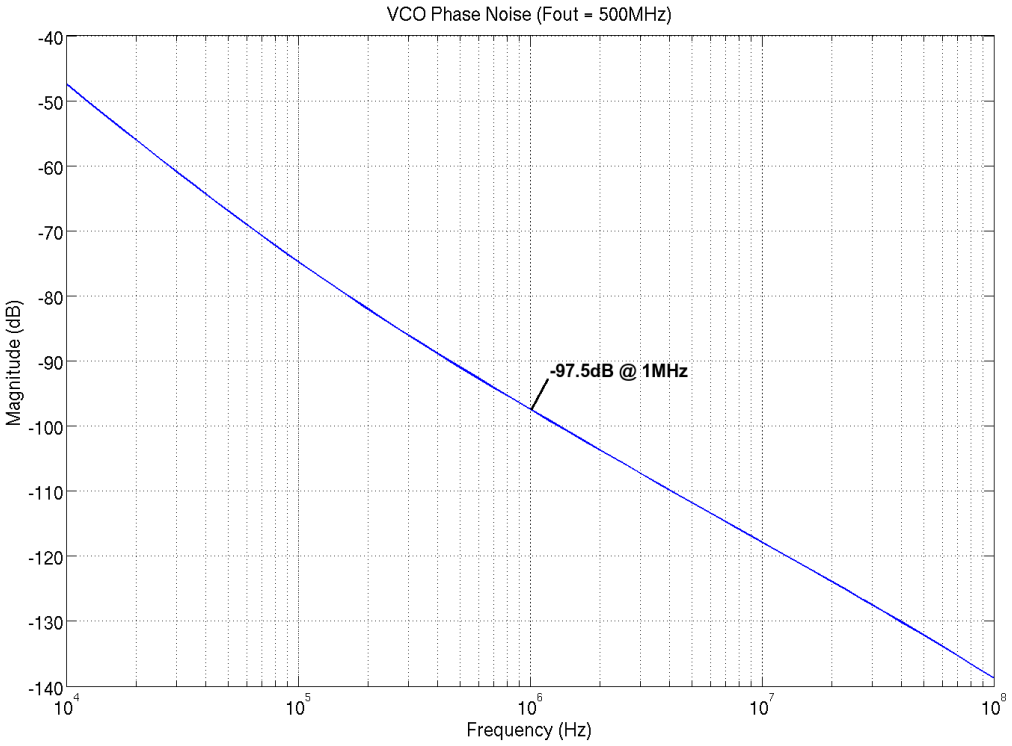

Figure 29: VCO Noise at 500MHz

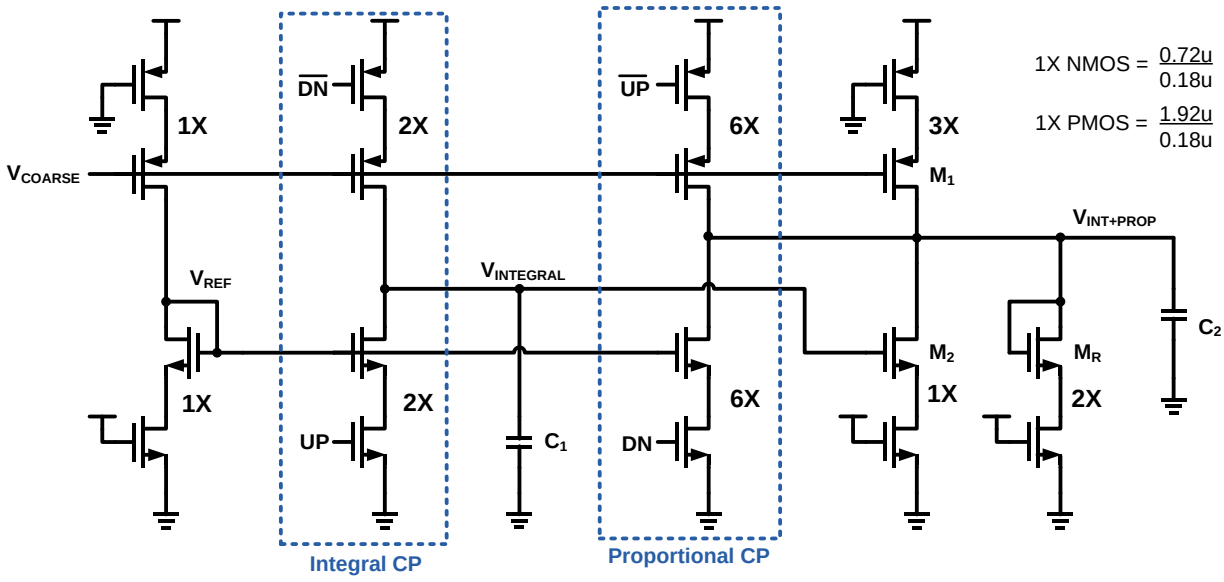

Figure 30: Charge Pump Schematic

3.2.2 Charge Pump

The classic charge pump is replaced with two charge pumps. The integral path charge pump is source switched and pumps into the main loop filter capacitor, shown as C_1 in Figure 30. The proportional path charge pump is a scaled version of the integral path charge pump, in fact 3 times larger to reduce the C_1 size. The proportional charge pump discharges into the node that is used as the fine control for the VCO. This node has both integral and proportional component since M_2 adds the integral path to the proportional path via current summation.

This charge pump accomplishes bandwidth-tracking as follows: the diode-tied loop filter resistor M_R and the current summation transistor M_2 are biased by M_1, whose current is mirrored from the VCO. Since the currents are mirrored from the coarse control voltage, V_{COARSE}, coming from the VCO the CP currents scale with the frequency squared. In addition, M_R's small-signal resistance is $1/g_m$ and it is being biased by a mirrored version of the VCO current, its small-signal resistance is inversely proportional to frequency. The current and resistance scaling causes the loop bandwidth to be proportional to the VCO frequency, while keeping the phase margin constant.

The fine control voltage is fed to a comparator, and subsequently an accumulator and a DAC that produces V_{COARSE}, shown in Figure 31. The bandwidth of the coarse path is set to be much lower than the fine path, resulting in the coarse path having negligible effect on the loop dynamics. However, the high gain of the coarse path forces the two inputs of the comparator to be approximately equal. This is used to force the fine control voltage to be the same as the bias voltage. The same drain-source voltages between the biasing and the charge pump transistors eliminates current mismatch.

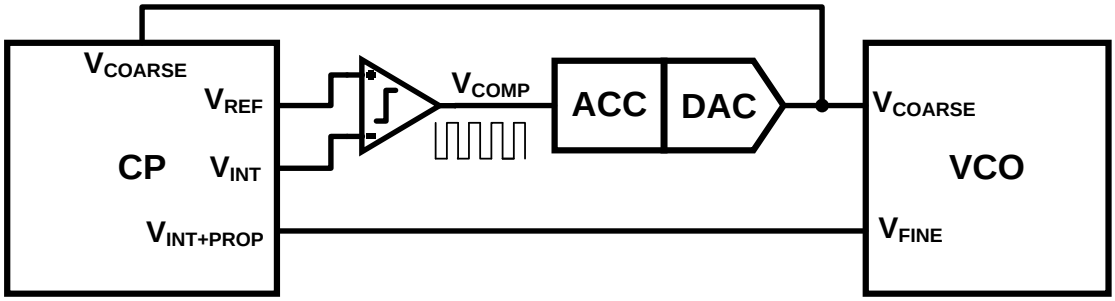

Figure 31: Block Diagram of the Control Voltage for VCO

By sizing the transistors appropriately, the current mismatch in the integral path is also eliminated. The sizing is done such that the current through M_1 equals the currents through M_R and M_2 when both the integral and fine control voltages are equal to the NMOS bias voltage, V_{REF}, at steady state.

The addition of the integral charge pump also gives the design an extra degree of freedom. M_2 and M_R form a gain stage whose gain can be adjusted through sizing. The 1:2 ratio gives a gain of 0.5, which means the size of C_1 can be reduced by 2X over a standard CP design. In addition, the current ratio between the proportional and integral charge pumps can be adjusted. In this design, it is 3X, which means an additional 3X reduction of C_1, which is why it is less than 1pF. Any reduction in C_1 increases noise, but these increase are negligible compared to VCO and resistor noise.

3.2.3 Phase Frequency Detector

The schematic for the standard pass-transistor phase-frequency detector (PFD) is shown in Figure 32. The main reason for selecting this PFD is its simplicity and low power features compared to the NAND and the glitch-latch PFD. The reset delay adds negligible effects on the overall performance of the PLL. Transistors all have minimum length due to the switching nature of the circuit. Invertors of size 1X, 2X and 4X and a 2X1 NAND gate are implemented are shown in Figure 33. Large inverters at the output are needed to drive the charge pump switches.

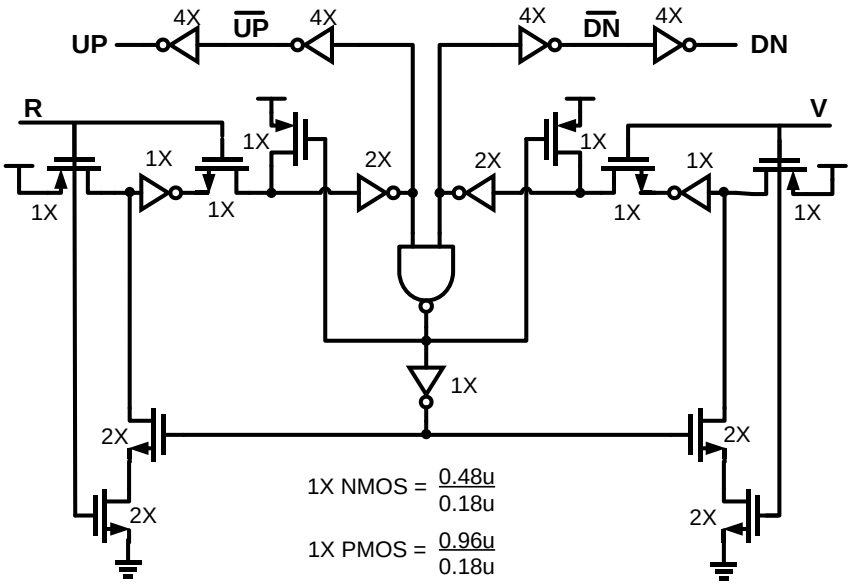

Figure 32: Pass Transistor PFD Schematic

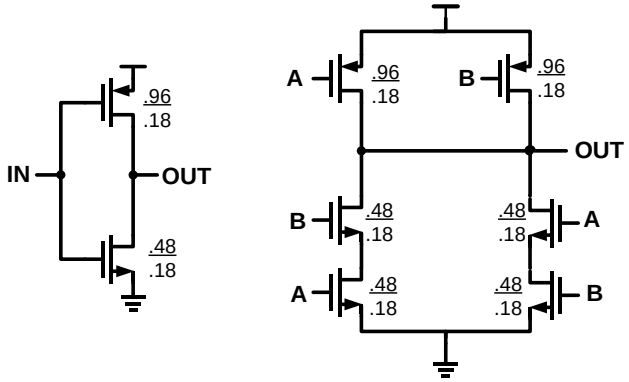

Figure 33: 1X Inverter (Left) and NAND (Right) Schematic

3.2.4 Clock Buffer and Feedback Divider

The clock buffer circuit is shown in Figure 34. It is positioned after the VCO to increase VCO output swing. A 1pF capacitor is used at the input to AC couple the signal and a 50KΩ is added to boost the input resistance. Other side benefits of the buffer include shorter rise/fall time and duty cycle correction.

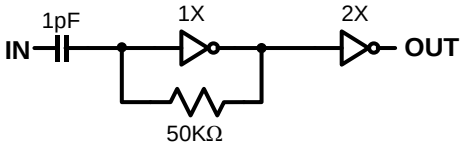

Figure 34: Clock Buffer Schematic

The schematic for the clock divider is provided in Figure 35. Two T flip-flops (T-FF) connected in series cut down the input frequency by four times. The T-FF is implemented as a true single-phase clocked (TSPC) flip flop for its simpler clocking scheme and lower load capacitance.

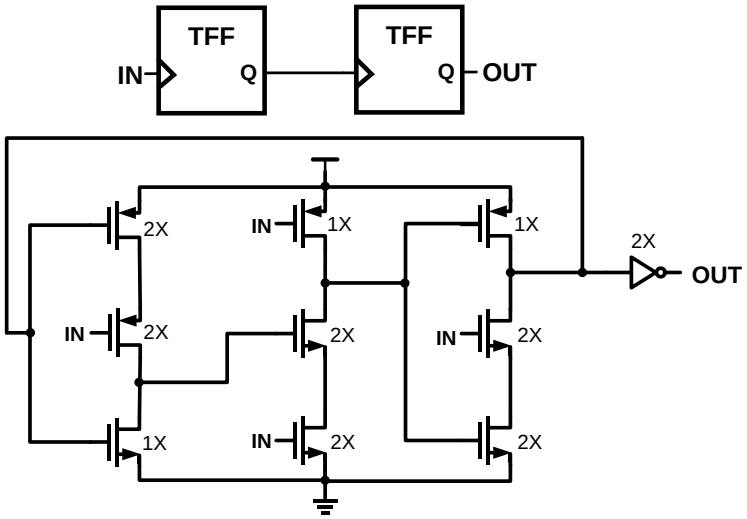

Figure 35: Clock Divider Schematic

3.2.5 Feedforward Noise Cancellation Circuit

The feedforward noise cancellation is done at the virtual supply node of the ring oscillator. The variable gain amplifier is similar to the one used for the LDO, with a NMOS tail source transistor

controlling the bias current, and thus the gain of the amplifier. The two inputs are at tied directly to V_{DD} and a clean version of V_{DD}. The load is designed as current mirror to create a high resistant output so that current summation can be done directly to the virtual supply. Therefore, two transistors are added to level shift the input common mode to ensure the two input transistors stay in saturation. The schematic of the variable amplifier is shown in Figure 36.

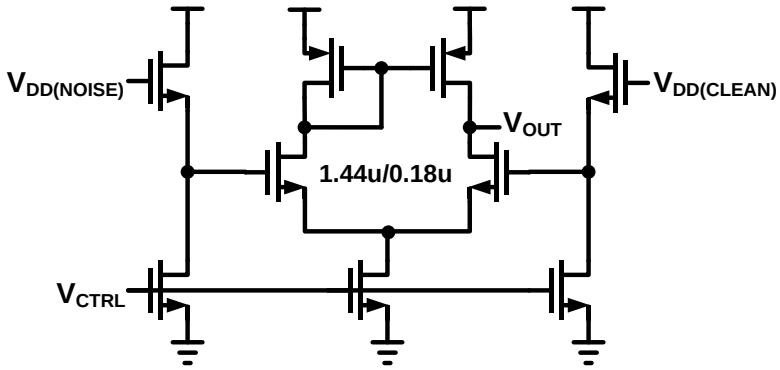

Figure 36: FFNC Variable Amplifier Schematic

The calibration is done similar to the LDO. Since the two inputs to the calibration block are digital signals, the simple approach is to use a XNOR gate with sub-sequent filtering of the output. The block diagram of the calibration circuit is shown in Figure 37.

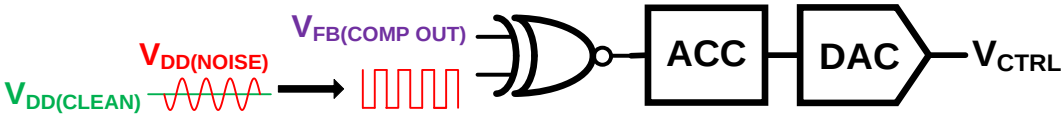

Figure 37: PLL FFNC Calibration Block Diagram

3.2.5 PLL Simulation Results

	500MHz	**1GHz**	**1.5GHz**
I_{CP}(μA)	45.6	111.8	202.3
K_{VCO} (GHz/V)	0.87	1.04	0.992
F_{UGB} (MHz)	10.7	17.5	22.4
Power (μW)	673	1347	2227
Peak-Peak Jitter with 2MHz, 10mV Noise	**No Noise**	**No FFNC**	**With FFNC**
	10.82	46.42	12.76

Table 2: Simulated PLL Performance Summary

4. PROTOTYPE TEST AND MEASUREMENT

Prototypes of both the LDO and the PLL using the FFNC method have been laid out and fabricated through the National Semiconductor's 0.18µm CMOS9T5V process. An evaluation board is also designed and assembled for the testing of the chip. An offset error inside the calibration amplifier prevented the calibration output to settle to the correct voltage. But by manual adjustment of the control voltage, the measured PSR of the LDO shows improvement of 16dB at a noise frequency of 10MHz. The PLL shows an improvement of 15dB in PSNR with FFNC active. The measurement results also show that control voltage required is a strong function of dropout voltage and load current.

4.1 Prototype Layout

The layout of the prototypes is shown in Figure 38, occupying a total area of 0.065mm^2.

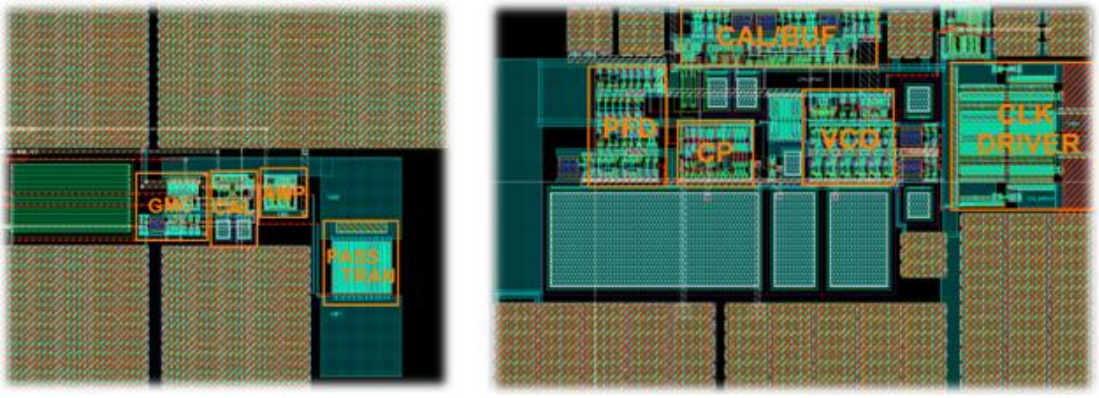

Figure 38: Layout of LDO (Left) and PLL (Right)

4.2 LDO Prototype Results

The test measurement setup for the LDO is shown in Figure 39. A clean power supply is used to generate the reference voltage and set the DC of the input supply. A signal generator is used to generate the single tone sinusoid and AC coupled onto the clean supply. The control voltage for FFNC has been manually adjusted to find the best-case PSR.

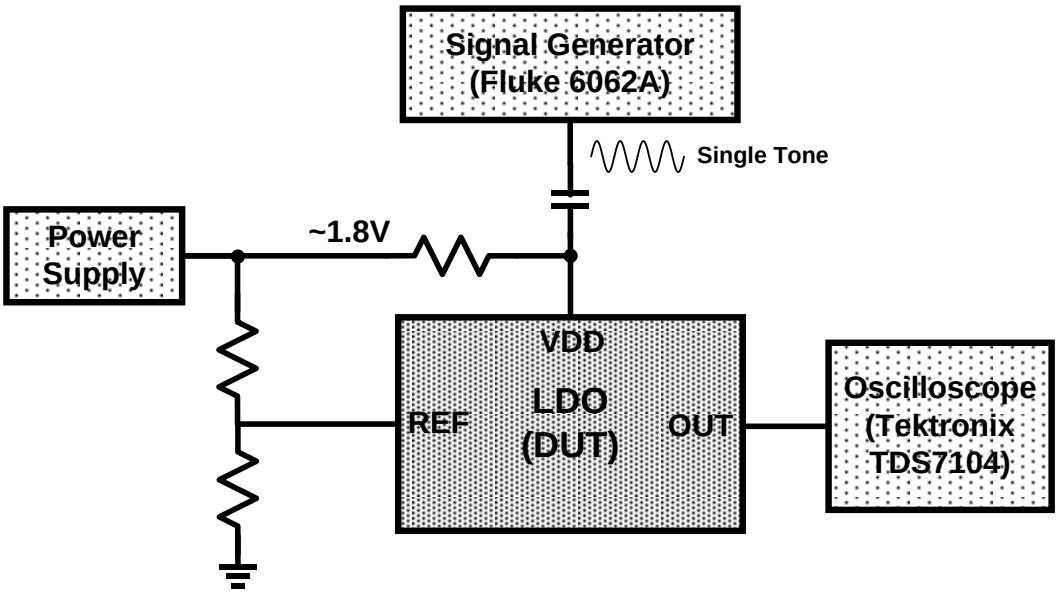

Figure 39: LDO Test Measurement Setup

4.1.1 Measured LDO PSR Results

The measured LDO PSR with and without FFNC is shown in Figure 40. The LDO has a load current of 10mA, a dropout voltage of 300mV, and noise amplitude of 10mV. The plot shows that FFNC is most effective below the 10 MHz noise frequency. With a noise frequency between 500 KHz and 5 MHz, the FFNC provides 25dB to 35dB of extra rejection. At 10MHz, cancellation provides 16dB of extra rejection, and quickly diminishes after 10MHz because of the finite feed-forward bandwidth. This plot also shows that the actual feed-forward bandwidth is lower than the simulated bandwidth of 400MHz due to layout and PCB parasitic capacitances. Nonetheless, the results do show a functional LDO with significant improvement in PSR using the FFNC method.

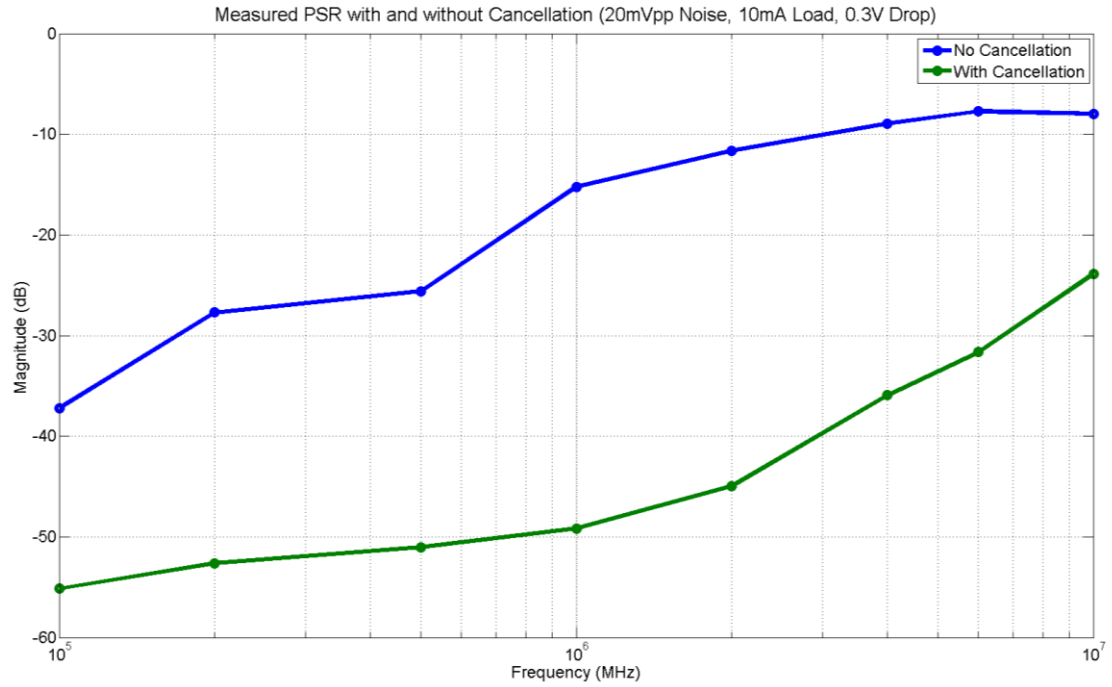

Figure 40: Measured PSR with and without FFNC

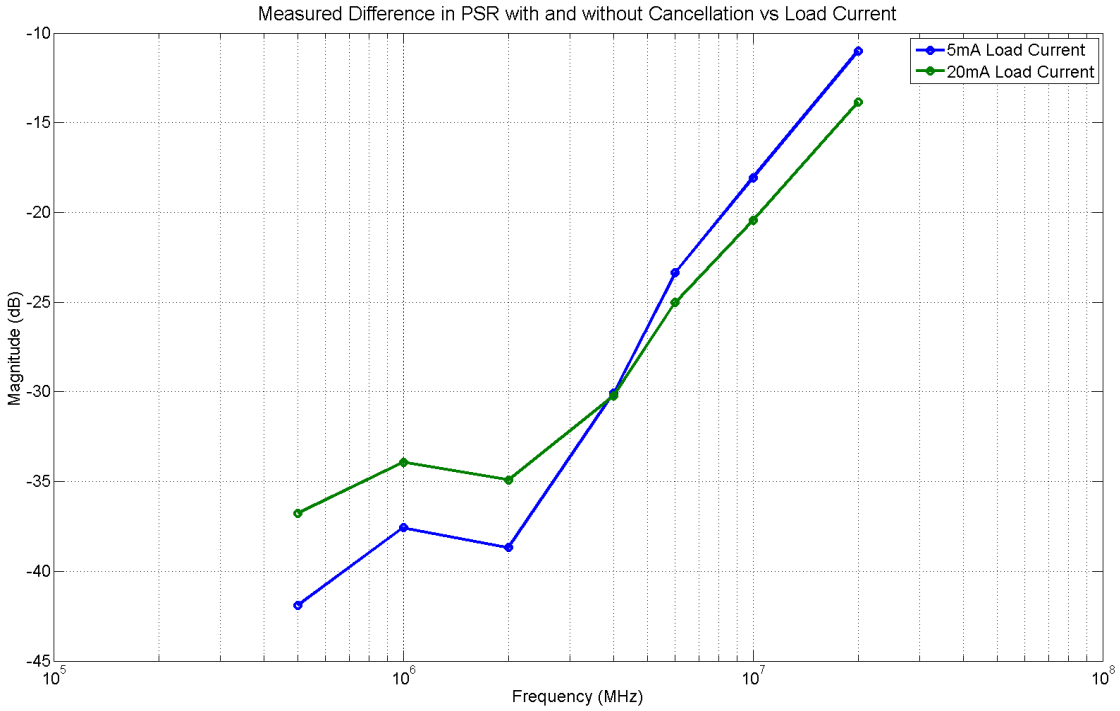

Figure 41: Measured PSR Improvement for Different Load Currents

In Figure 41, PSR improvement is plotted with two load current conditions while dropout voltage is fixed at 300mV and noise amplitude is fixed at 10mV. This plot shows comparable PSR improvement for both load currents, even though currents consumed by FFNC as a percentage of load current is different.

As mentioned in Section 2.1.3, the non-linearity of the pass transistor introduces distortion and degrades the effectiveness of cancellation. A plot of measured PSR with two different noise amplitudes is shown in Figure 42. Peak-to-peak noise amplitudes of 10mV and 50mV are used, and degradation in PSR is worse at lower frequencies.

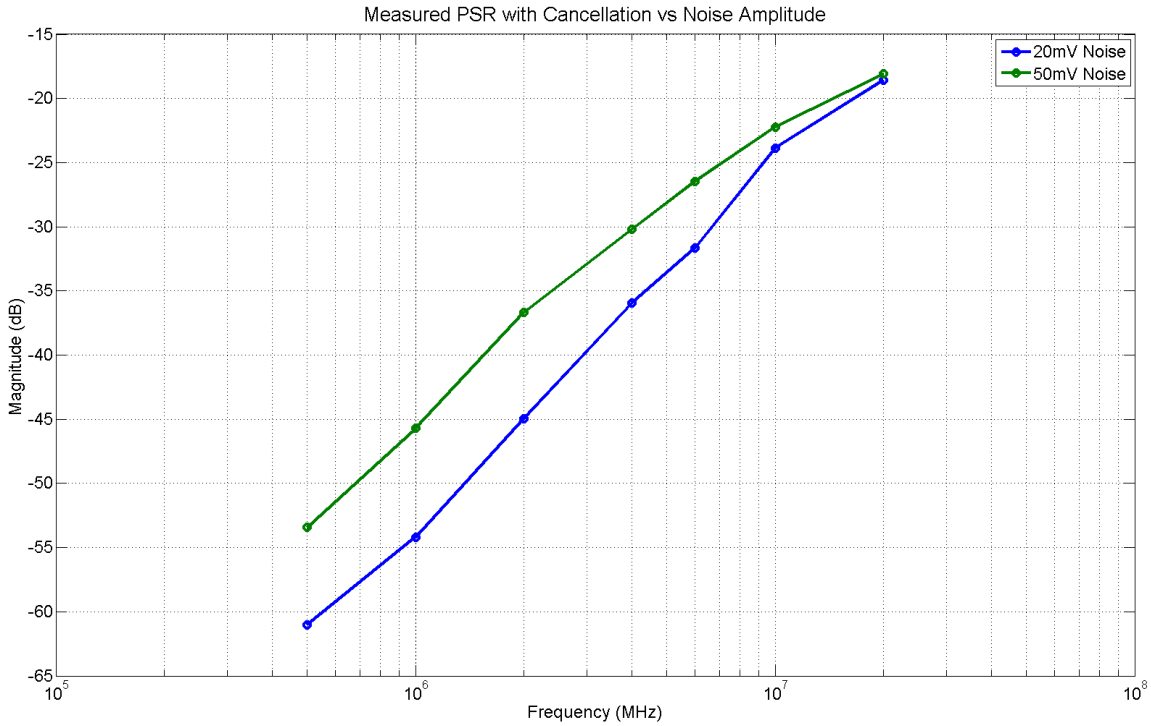

Figure 42: Measured PSR for Different Noise Amplitude

4.1.2 Measured Control Voltage Variations

The next few plots investigate how load current, dropout voltage and noise amplitude affect the optimal control voltage for FFNC. The noise frequency is fixed at 2MHz. As load current increases, the overall gain of the pass transistor decreases and a larger swing at the gate is

required to replicate the same signal at the output. Since a NMOS is used as the tail source as shown in Figure 19, an increase of signal swing at the gate translates into higher control voltage. Figure 43 presents the control voltage as a function of load current, along with the corresponding best-case PSR at each load current. The roughly linear relationship makes sense because the feed-forward gain increase in a square root fashion in order to cancel the loss in pass transistor gain in the same fashion. The PSR also indicates that FFNC works best from 5mA to 20mA.

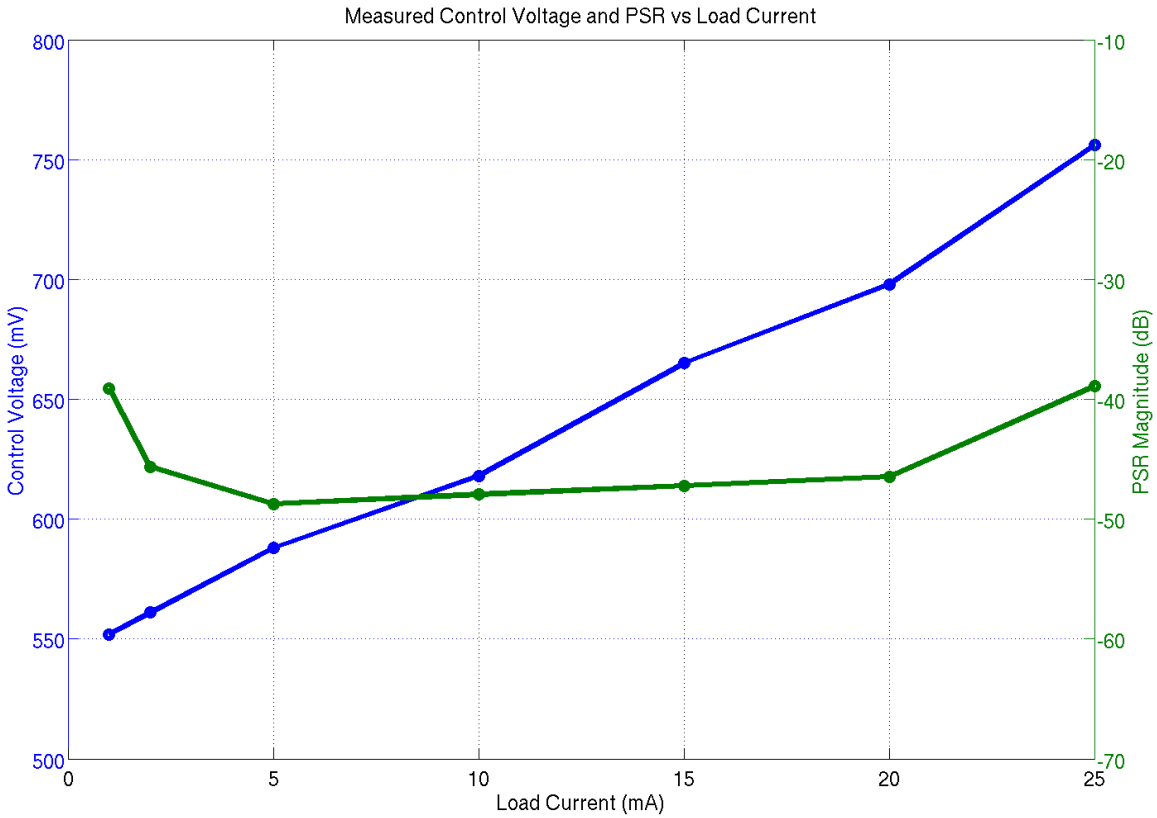

Figure 43: Measured Control Voltage and PSR as a Function of Load Current

The variation in control voltage as a function of dropout voltage is plotted in Figure 44. The required control voltage increases considerably below a dropout of 200mV because the pass transistor is going into triode region. The large increase in control voltage is also partially due to the tail source approaching triode region inside the variable gain amplifier. For practical use of FFNC in the current design, it is desirable to keep the dropout above 200mV.

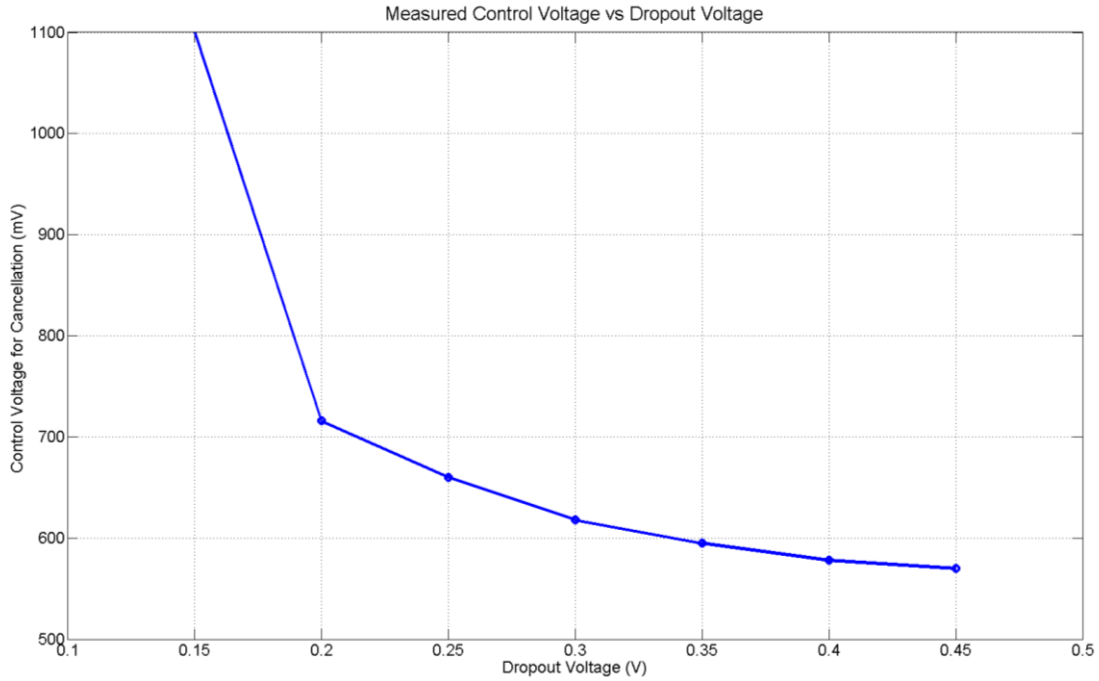

Figure 44: Measured Control Voltage as a Function of Dropout Voltage

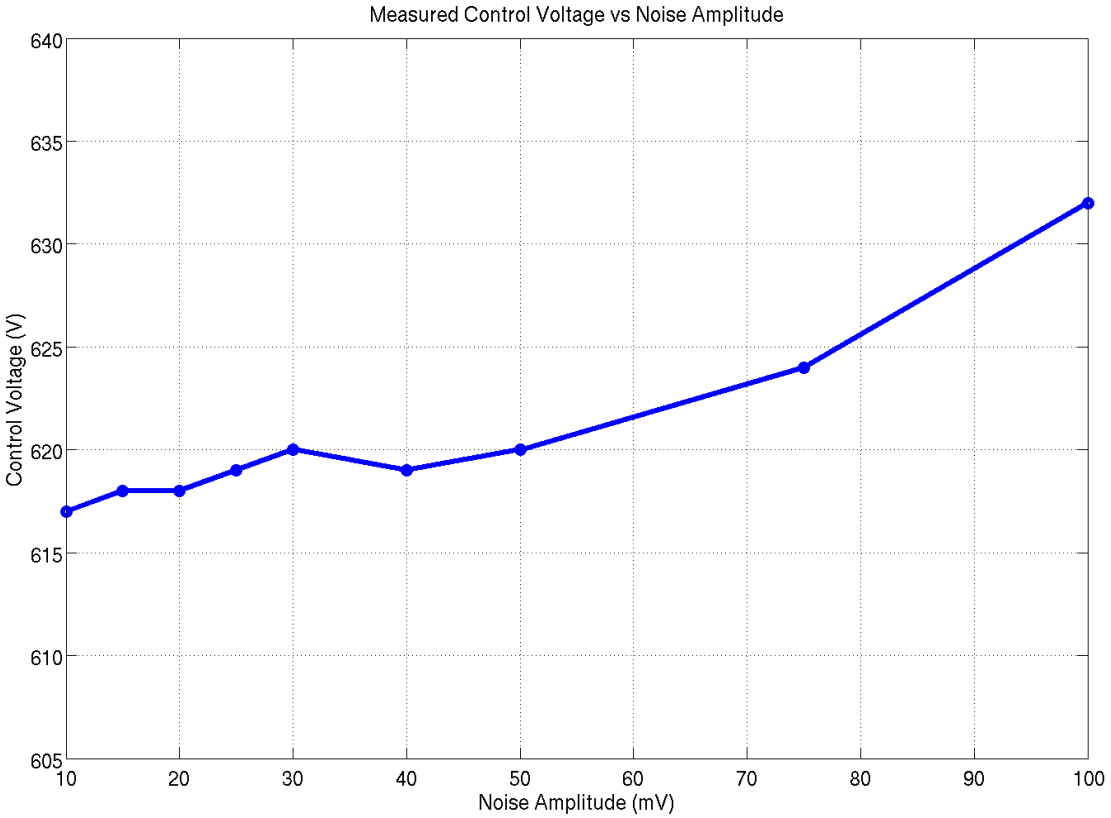

Figure 45: Measured Control Voltage as a Function of Noise Amplitude

The plot of control voltage as noise amplitude is varied is shown in Figure 45. This plot indicates that for noise amplitude smaller than 50mV, the control voltage stays between 615mV and 620mV. The increase in required control voltage when noise amplitude increases to 100mV is due to noise been dominated by second harmonic. Recall from Section 2.1.3, as control voltage approaches to the optimal value, only the fundamental is suppress by cancellation, but the second harmonic increases due to increasing pass transistor V_{DS} variation.

4.1.3 Additional LDO Measurements

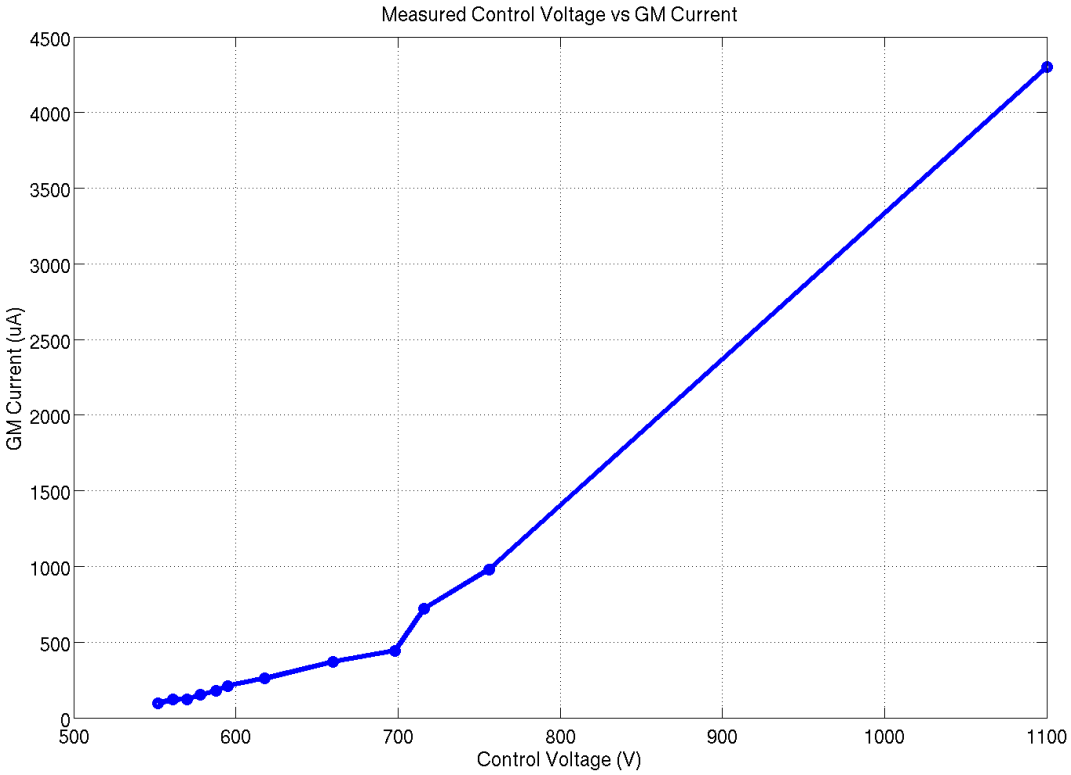

Figure 46: Variable Amplifier Current Consumption as a Function of Control Voltage

The plot depicted Figure 46 shows the amount of current consumed by the variable transconductance amplifier, as a function of control voltage. Since the amplifier is a differential pair with NMOS tail current source, increasing NMOS gate voltage would eventually push the NMOS into triode. This is the main reason the IV characteristic is more linear than square beyond

800mV, because the tail source is going into triode region. For most applications, the current consumption is below 500uA. The other main sources of power consumption are the feedback amplifier and calibration amplifier. Since the bandwidth of both feedbacks is low, the total current consumed in both amplifiers is less than 100uA at worst case. Therefore, at a dropout voltage of 300mV, the LDO has an overall efficiency of:

$$\eta = \frac{P_{OUT}}{P_{IN}} \approx \frac{(1.5\text{V})(20\text{mA})}{1.8(20\text{mA} + 100\mu\text{A} + 500\mu\text{A})} = 80.9\% \qquad \textbf{(11)}$$

If FFNC is disabled in the LDO, the efficiency becomes 82.9%. The overall efficiency of the LDO may degrades due to changes in load current or dropout voltage, but the net loss due to FFNC stays more constant at 2% because the variable amplifier current scales with load current. If one were to obtain the same -20dB PSR at 10MHz with the brute force method of increasing feedback bandwidth ten times to 20MHz, the loss in efficiency would be much worse.

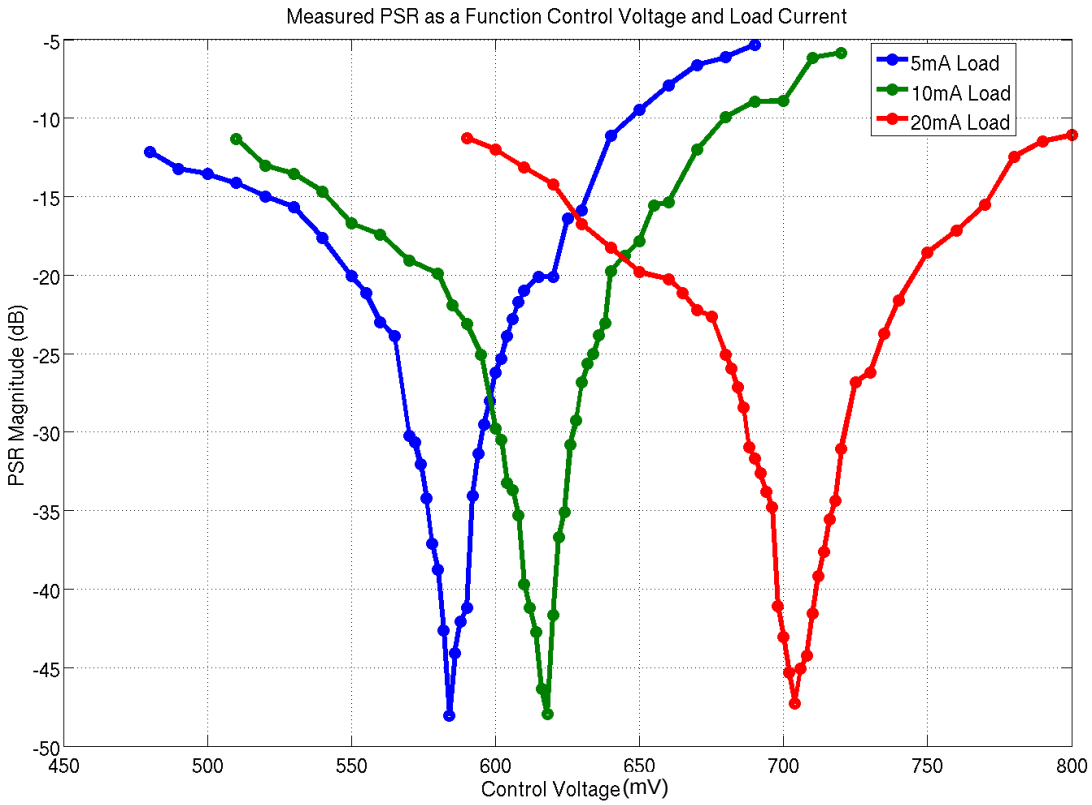

Figure 47: Measured PSR as a Function of Control Voltage under Different Load Current

The plot in Figure 47 depicts the measured PSR by sweeping the control voltage. As control voltage is swept, the PSR experiences a drop near the optimal point. This plot shows that the change is more gradual, with most of rejection is achieved within 3mV of the optimal point. The PSR as a function control voltage for different dropout is plotted in Figure 48. As expected, higher control voltage is required for lower dropout.

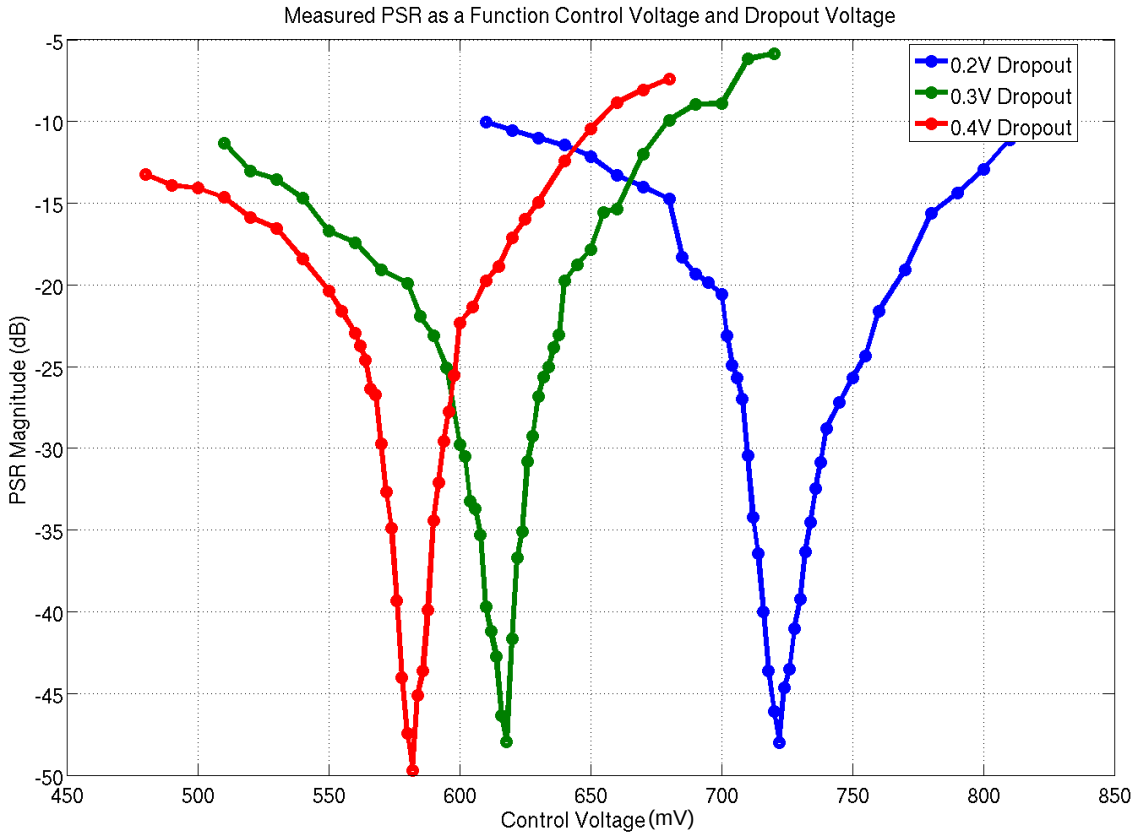

Figure 48: Measured PSR as a Function of Control Voltage under Different Dropout Voltage

The measured PSR as a function of control voltage when two different noise amplitudes are injected is shown in Figure 49. Two conclusions can be drawn from this plot: 1.) control voltage is a weak function of noise amplitude, and 2.) the best-case PSR that can be achieved by FFNC is limited by the second harmonic at the output.

The first implication is already confirmed in Figure 45. As explained in Section 2.2, increasing noise amplitude degrades the best-case PSR due to increasing distortion from the pass transistor output resistance. But the optimal voltage desired to cancel the fundamental of noise signal stays

constant. As control voltage increases, the second harmonic of the output noise also increases because the increasing pass transistor V_{DS} swing. Even though the fundamental can be suppressed down to –30dB, the second harmonic dominates the overall signal and limits the best-case PSR to around –20dB.

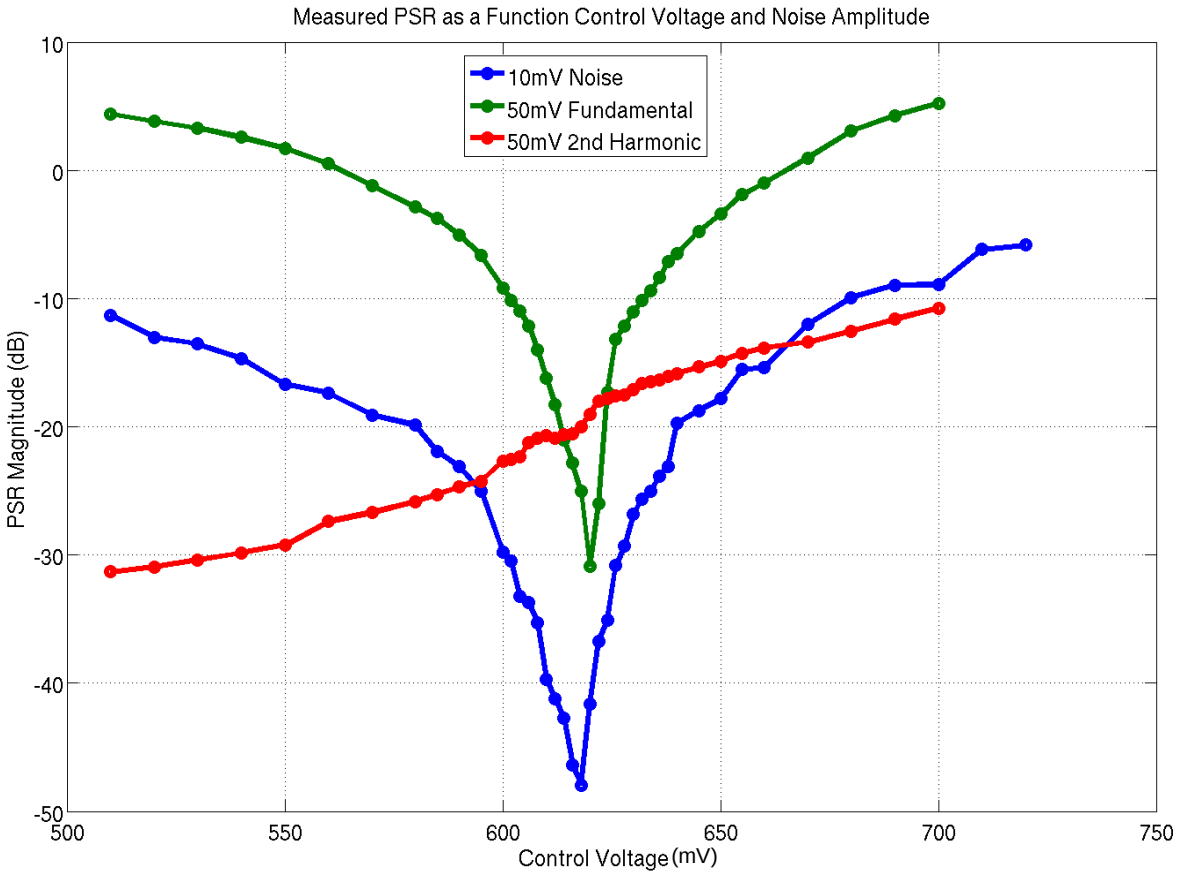

Figure 49: Measured PSR as a Function of Control Voltage under Different Noise Amplitude

4.3 PLL Measurement Results

The PLL test setup is similar to the LDO, and is shown in Figure 50. A signal generator is used to create the supply noise at one sinusoidal tone, and is then coupled to the V_{DD} of the VCO. The power supply also generates clean supply for the rest of the PLL blocks. An arbitrary waveform generator is used to create the reference clock for the PLL. The output clock off the PLL is first

observed with a communication serial analyzer for jitter and then with a spectrum analyzer for spurious tones. Insufficient comparator output drive in the implementation of the prototype prevented the comparator output to come cleanly off-chip. Therefore, the coarse control, shown as V_{COAESE} in Figure 16, is adjusted manually for the results shown in this section. V_{COAESE} is changed within the vicinity of the expected output frequency until the fine control takes over the loop dynamics. The control voltage for FFNC, V_{CTRL} in Figure 16, is also set manually off-chip.

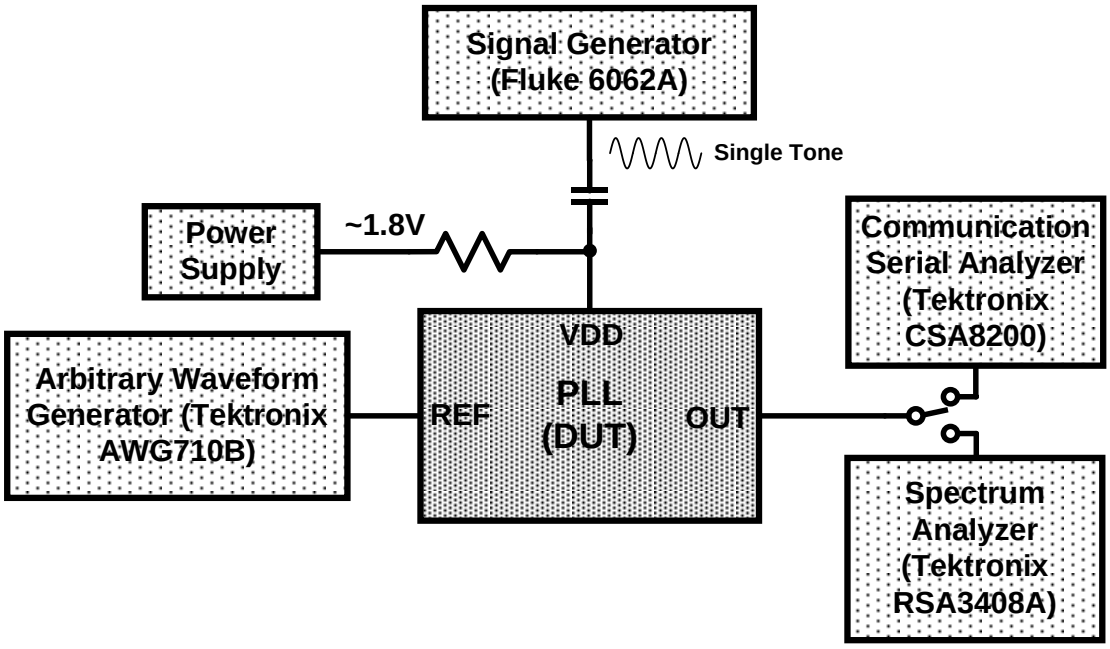

Figure 50: PLL Test Setup

Given a supply noise at a single tone, a histogram of the zero-crossings of the output clock rising edge is plotted on the communication serial analyzer to find the peak-to-peak jitter. The screenshots of a typical jitter measurement is shown in Figure 51 through Figure 53. Since the performance of most concern is the additional jitter introduced by supply noise, sampled average of four is used for acquisition. The averaging function lowers the overall peak-to-peak is without changing supply noise rejection property of the PLL or FFNC. These plots are for a supply noise of 10mV at 8MHz, for which the deterministic jitter is reduced from 100.2ps down to 36.8ps with FFNC active.

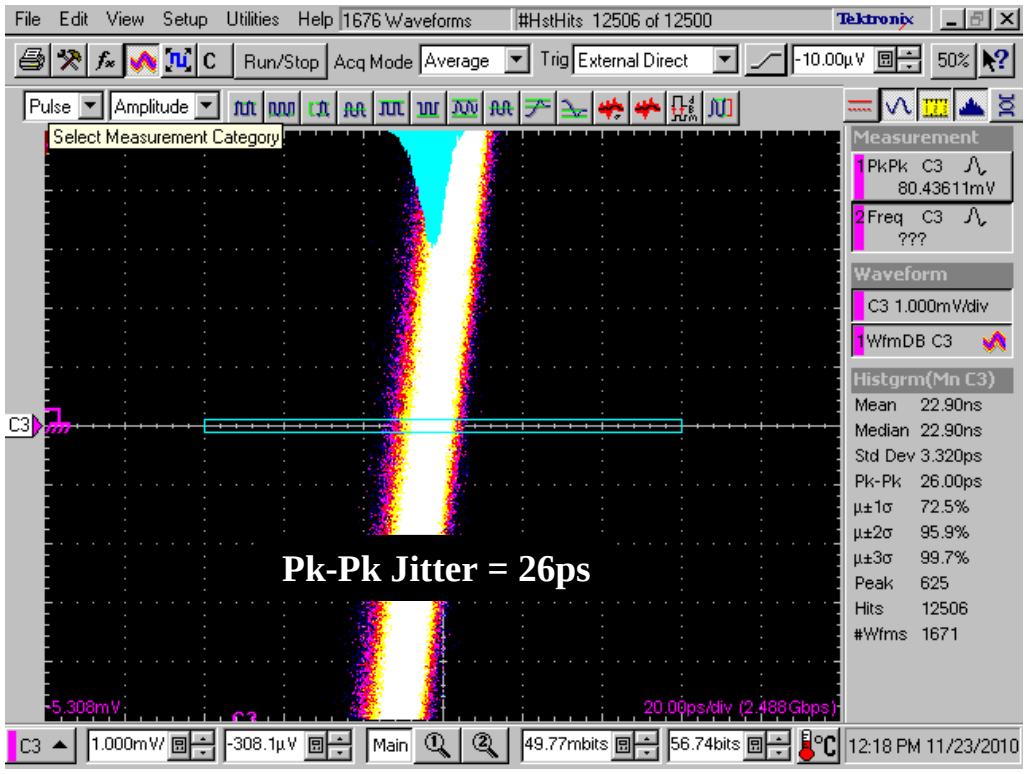

Figure 51: Output Clock Rising Edge Histogram, No Supply Noise

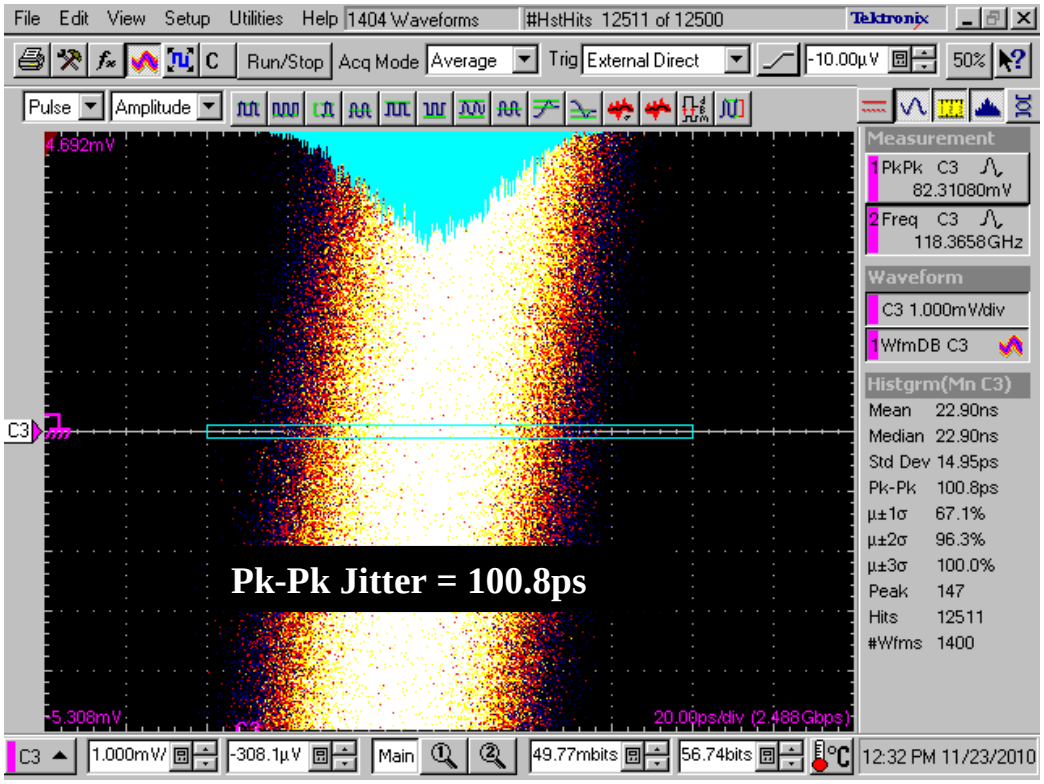

Figure 52: Output Clock Rising Edge Histogram, with 10mV noise at 8MHz, no FFNC

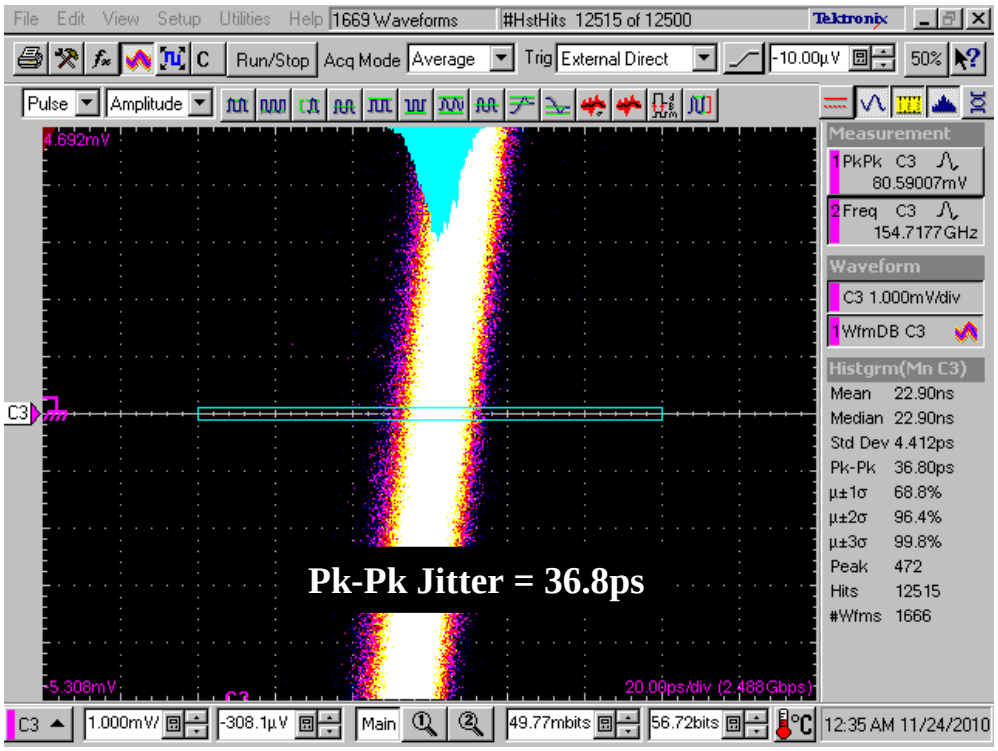

Figure 53: Output Clock Rising Edge Histogram, with 10mV noise at 8MHz, with FFNC

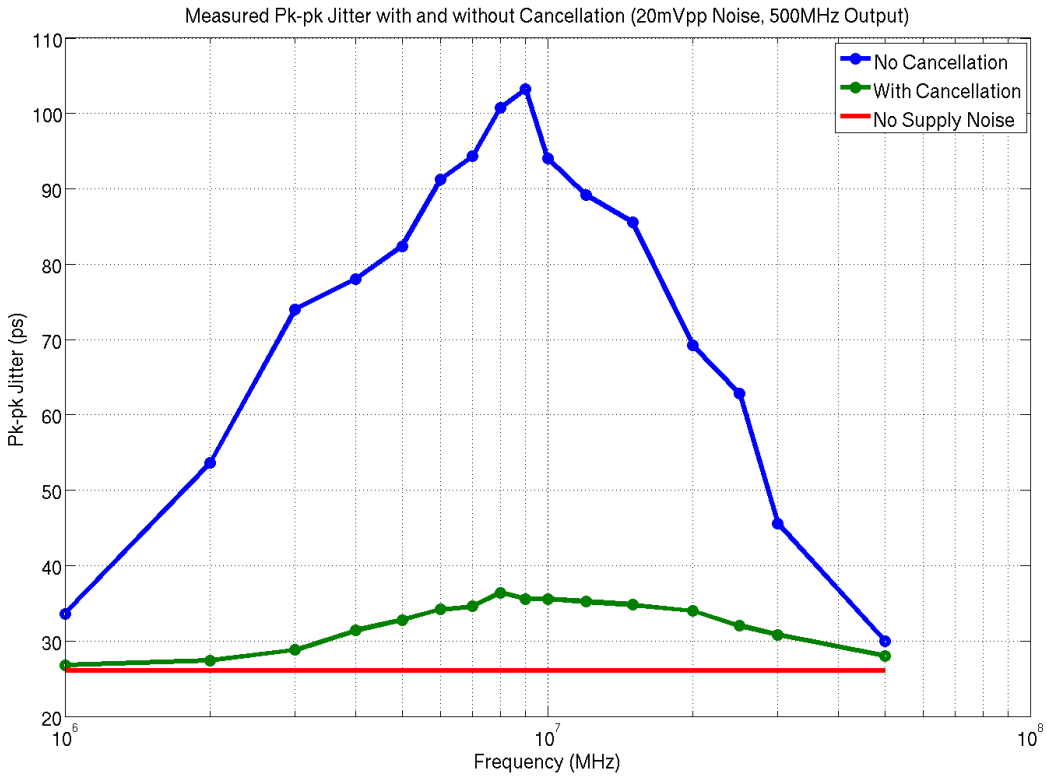

Figure 54: Measured Peak-to-peak Jitter as a Function of Noise Frequency, with and without FFNC

The measured peak-to-peak jitter as a function of noise frequency is plotted in Figure 54. The plot does show improvements for all noise frequencies from 1MHz to 50MHz. The VCO supply-to-output jitter transfer function experience a bandpass characteristic as expected. The maximum jitter value for the case is 36.8ps with FFNC active. Base on Equation 1, this improvement translates to a PSNR of:

$$\Delta PSNR = 20\log\left(\frac{T_{j1}/T}{\Delta V}\frac{\Delta V}{T_{j2}/T}\right) = 20\log\left(\frac{103.2-26}{36.8-26}\right) = 17.25\text{dB} \qquad \textbf{(12)}$$

The 17dB PSNR improvement is comparable to the 16dB improvement in worse-case PSR of a LDO at 10MHz, shown in Figure 40.

To further confirm the results, measurements on the spectrum analyzer are also plotted from Figure 55 through Figure 58. Without supply noise, the reference spurs are at a value of –52.8dBc/Hz. With an input noise of 10mV at 8MHz, the supply noise spurs peak to –38.5dBc/Hz. By using FFNC, the supply noise spurs are suppressed down to –52.3dBc/Hz.

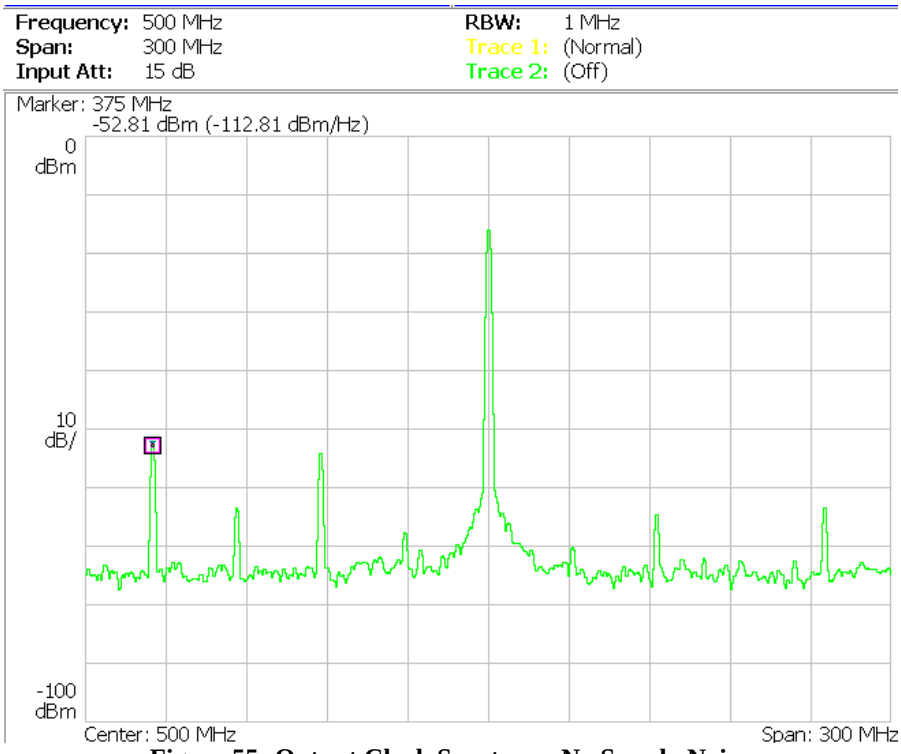

Figure 55: Output Clock Spectrum, No Supply Noise

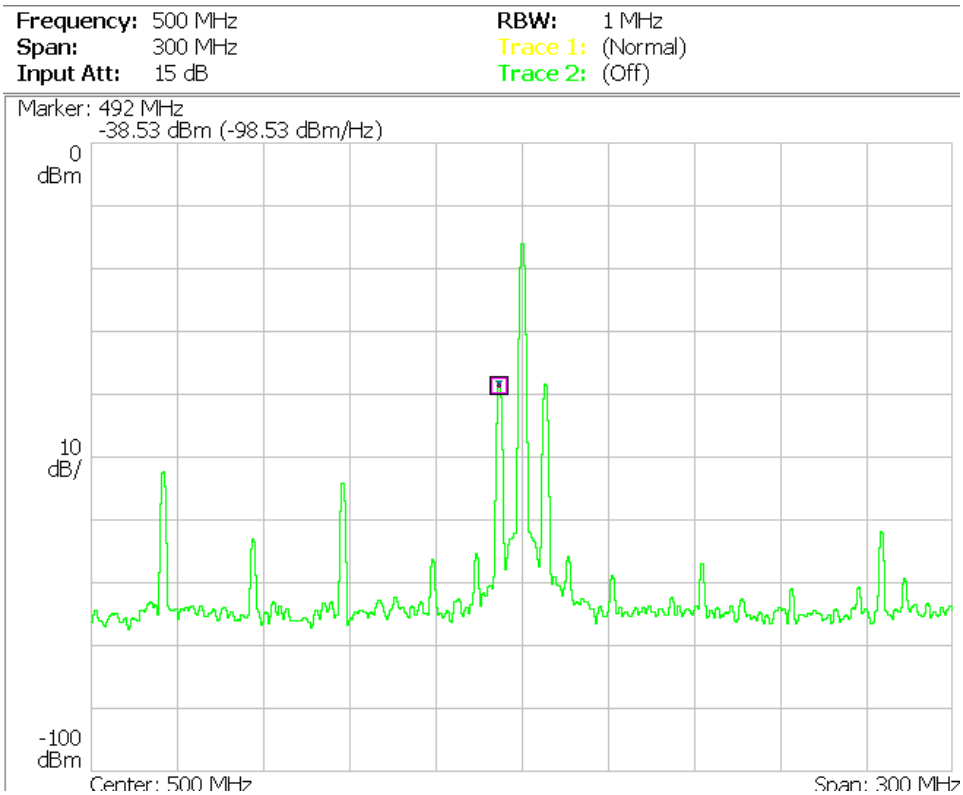

Figure 56: Output Clock Spectrum, 10mV Supply Noise Added at 8MHz, No FFNC

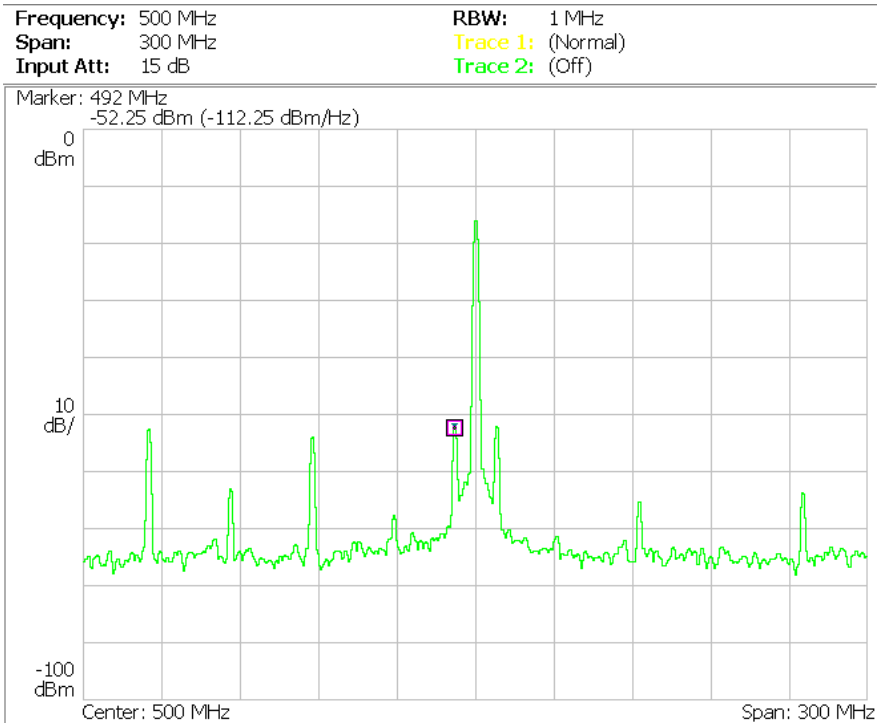

Figure 57: Output Clock Spectrum, 10mV Supply Noise Added at 8MHz, with FFNC Active

5. CONCLUSION

A method of improving the power supply noise rejection property of circuits by using a fast feedforward path to cancel the noise is investigated in this paper. By analyzing the idea, circuit design and simulation, as well as prototype measurement, several conclusions are drawn from this investigation:

- The feedforward noise cancellation (FFNC) method is confirmed in both LDO and PLL by providing an addition of 22dB of rejection in simulation and 16dB in prototype measurement.
- The deviation between simulation and measurement is mainly because of a lower feedfoward bandwidth in the prototype. The feedfoward bandwidth is found to have direct impact on the effectiveness of the cancellation. Maximizing the bandwidth should be the topmost concern for designing the circuit with FFNC.
- The control voltage for FFNC is highly sensitive to variation in load current and dropout voltage, but not so much to noise amplitude and frequency. Therefore, for stable load and dropout conditions, the control voltage can be set once manually with a test signal.
- A method of background calibration by correlating the supply and output is also designed and functional in simulation. Large random offset and insufficient logic drive strength in the prototype prevented the correct settling of the calibration output, but these common circuit issues can be fixed by conventional methods in the future revision of the prototype.

References

[1] V. Gupta and G. A. Rincon-Mora, "A 5mA 0.6um CMOS Miler-Compensated LDO Regulator with –27dB Worst-Case Power-Supply Rejection Using 60pF on On-Chip Capacitance," *ISSCC Dig. Tech. Papers*, pp.520-521, Feb. 2007.

[2] M. El-Nozahi, et.al. "A 25mA 0.13um CMOS LDO Regulator with Power Supply Rejection Better Than -56dB up to 10MHz Using a Feedforward Ripple-Cancellation Technique." *ISSCC Dig. Tech. Papers*, pp. 330-331, Feb. 2009.

[3] V. Gupta and G. A. Rincón-Mora, "Analysis and design of monolithic, high PSR, linear regulators for SoC applications," in *Proc. IEEE SOC Conf.*, Santa Clara, 2004, pp. 311-315.

[4] S.K. Hoon, et al. "A Low Noise, High Power Supply Rejection Low Dropout Regulator for Wireless System-on-Chip Applications," *IEEE Custom Int. Circuits Conf*, pp.759-762, Sept. 2005.

[5] M. Steyaert and W. Sansen. "Power Supply Rejection Ratio in Operational Transconductance Amplifiers," *IEEE Tran Circuit and Systems*, vol. 37 no.9 Sept. 1990.

[6] A. Arakali, S. Gondi, and P. Hanumolu, "Low-Power Supply-Regulation Techniques for Ring Oscillators in Phase-Locked Loops Using a Split-Tuned Architecture," *IEEE J. Solid State Circuits*, vol.44, no.8, pp. 2169-2181, Aug. 2009.

[7] A. Arakali, S. Gondi, and P. Hanumolu, "A 0.5-to-2.5GHz supply-regulated PLL with noise sensitivity of -28dB," *IEEE Custom Int. Circuits Conf.*, pp. 443-446, Sep. 2008.

[8] E. Alon, et at., "Replica Compensate Linear Regulators for Supply-Regulated Phase-Locked Loops." *IEEE J. Solid State Circuits*, vol.41, no.2, pp. 413-424, Feb. 2006.

[9] C. Lee, K. McClellan and J. Choma Jr., "A Supply-Noise-Insensitive CMOS PLL with a Voltage Regulator Using DC-DC Capacitive Converter," *IEEE J. Solid-State Circuits*, pp. 1453-1463, Oct., 2001.

[10] A. Arakali. "Low-Power Techniques for Supply-Noise Mitigation in Phase-Locked Loops." PhD Dissertation. Oregon State University. Corvallis, OR. Jan. 2010.

[11] P. Godoy and J. L. Dawson, "Chopper Stabilization of Analog Multipliers, Variable Gain Amplifiers, and Mixers," *IEEE J. Solid State Circuits*, vol.43, no.10, Oct. 2008